A 7.1 mW, 10 GHz All Digital Frequency Synthesizer With Dynamically Reconfigured Digital Loop Filter in 90 nm CMOS Technology

Song-Yu Yang, Wei-Zen Chen, and Tai-You Lu

***Abstract*—A 10 GHz all digital frequency synthesizer (ADPLL) with dynamic digital loop filter is presented. Governed by a proposed locking process monitor (LPM), the digital loop filter is automatically reconfigured during the frequency acquisition and phase tracking process. The loop bandwidth is also self-adjusted during the locking process so as to achieve fast lock and low noise simultaneously. A skew-compensated phase accumulator is proposed for high speed operation, which preserves the advantages of low power dissipation while eliminating the accumulated timing skew issue. With less than 7 μs locking time, the measured rms jitter from a 9.92 GHz carrier is about 0.9 ps. The ADPLL core consumes 7.1 mW from a 1 V supply, and the digital I/O cells drains 2.7 mW from a 3.3 V supply for chip measurement. Implemented in a 90 nm CMOS technology, the core area is only 0.352 mm^2.**

***Index Terms*—ADPLL, phase-locked loop, phase accumulator, frequency divider, phase-frequency detector, bang-bang phase detector.**

I. Introduction

ALL-DIGITAL phase-locked loop (ADPLL) frequency synthesizers have drawn tremendous research efforts recently as the technology paradigm shifts into the nano-meter CMOS arena [1]–[6]. They circumvent several design issues that conventional charge-pump based PLLs encounter, including capacitor leakage, current mismatch, and limited dynamic range under low supply voltage. Besides, the bulky passive loop filter is replaced by more cost-effective digital filter, which can be further scaled down along with the advancements in IC technology. Additionally, the digital based design facilitates sophisticated scheme for performance optimization, and also the portability of silicon intellectual property (SIP) for technology migration. Thus, they are more attractive for SoC integration.

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Major design issues of the frequency synthesizer are focused on phase purity/timing jitter, reference spur, and locking time. In frequency hopping system and some system clock scenarios where the PLL is disabled during the sleeping mode, the locking speed is of special interests. On the other hand, for the portable devices, the power dissipation is also of special concern. To avoid severe trade-off among the desired properties, some auxiliary circuits are needed to monitor the locking process and dynamically adjust the loop parameters accordingly. To accelerate the locking speed, typically, the frequency acquisition process is monitored by a frequency detector [7]–[9] to coarsely tune the oscillator output frequency. On the other hand, a common approach to switch loop bandwidth is by adjusting charge pump current and zero resistors in PLLs [10]. It corresponds to a gear shifting in ADPLL implementation [11]. These techniques can drastically reduce the settling time. However, as the frequency resolution of FD is usually limited, the overall locking time will be dominated by the final phase tracking process.

In this design, an all digital phase-locked loop frequency synthesizer with dynamic digital loop filter is proposed [6]. Governed by a proposed locking process monitor (LPM), the digital loop filter is automatically reconfigured and the loop bandwidth is self-adjusted during the frequency acquisition and phase tracking process. The settling time in both modes is reduced significantly. The locking speed is accelerated by order of magnitude in contrast to the prior art in [8], [11]. It features less than 7 μs locking time and 0.9 ps rms jitter while manifesting operating frequency up to 10 GHz.

This paper is organized as follows. Section II describes the ADPLL architecture, its operation principles, and system analysis. Section III describes the detail circuit implementation, including digital controlled oscillator (DCO), phase accumulator, and the locking process monitor (LPM). The experimental results are shown in Section IV. Finally, Section V draws the conclusion.

II. ADPLL Architecture

The architecture of the proposed ADPLL is illustrated in Fig. 1, which is composed of a dual-mode phase frequency detector (DPD), a PI digital loop filter composed of programmable integral (α) and proportional (β) paths, a locking process monitor (LPM), an *LC* based digital controlled oscillator (DCO), a divide-by-4 prescaler, and two phase accumulators PAC1 and PAC2.

To relax the speed requirement of the phase accumulator, the PAC1 accumulates quarter of the frequency multiplication

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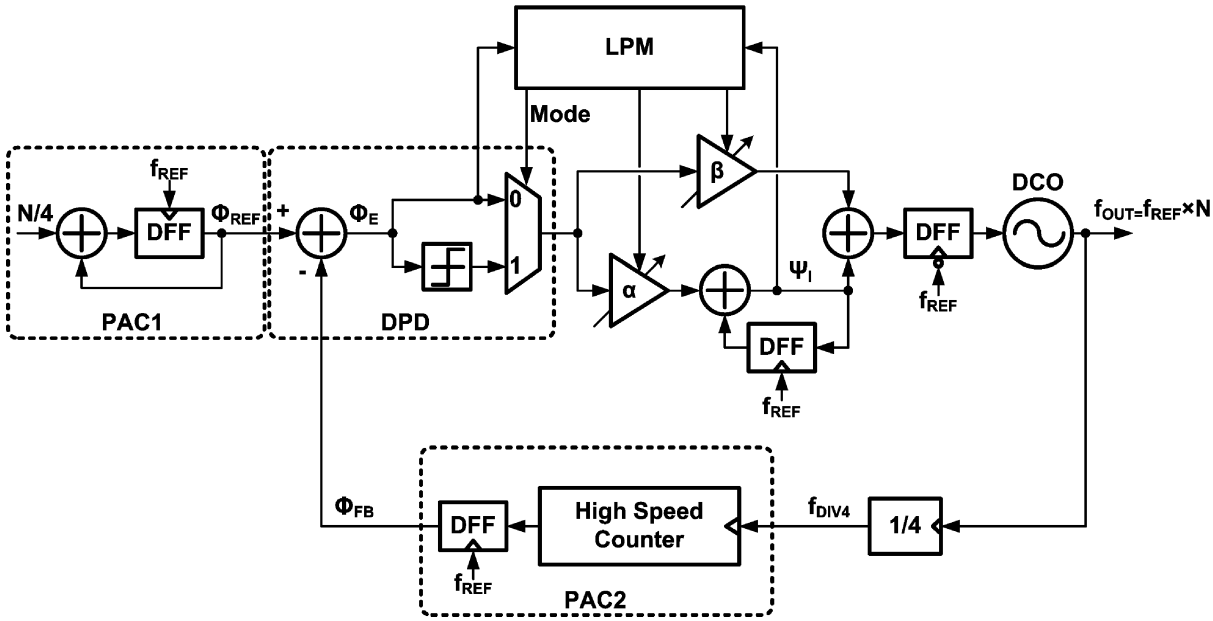

Fig. 1. Dynamically reconfigured all digital phase locked loop architecture.

factor $(N/4)$. On the other hand, PAC2 follows a divide-by-4 prescaler, accumulating the prescaler output phase. The quantized phase difference (Φ_E) between $f_{\rm REF}$ and $f_{\rm OUT}/N$ is resolved by a subtractor, and then filtered by the digital loop filter to adjust DCO's output frequency. To accelerate the locking speed and extend locking range, the DPD is operated in the linear mode during frequency acquisition (FA), and is turned into binary mode during the phase tracking (PT) process. Both modes are moderated by the LPM. The LPM will also dynamically adjust the loop parameters according to the phase error and the status of loop filter, which will be further discussed in the following sections.

A. Frequency Acquisition (FA) Mode

In the initial phase of the locking process, the loop is preset in the frequency acquisition mode. Fig. 2(a) illustrates a frequency locked loop architecture [7], [9], which is mainly composed of a phase accumulator, a frequency detector, and a loop filter. The DCO output frequency $f_{\rm OUT}$ is detected by counting clock edges in a reference period (Fig. 2(b)), which is derived by a phase accumulator followed by a differentiator. If $f_{\rm target}$ is the target locking frequency, N is the target number of counts in a reference period, and M is the counted DCO cycles, we have

$$N = \frac{f_{\rm target}}{f_{\rm REF}} \tag{1}$$

and

$$M = \frac{f_{\rm OUT}}{f_{\rm REF}}. \tag{2}$$

Then the difference between target frequency and current DCO output frequency can be derived as

$$f_{\rm target} - f_{\rm OUT} = f_{\rm REF} \cdot (N - M). \tag{3}$$

If the integrator of loop filter is moved to the input of the subtractor, the frequency locked loop becomes equivalent to the main architecture in Fig. 1 by disabling the integral path of the loop filter. During this mode, the DPD is operated in the linear mode where the output is proportional to frequency error to accelerate frequency locking. The frequency detector output continuously adjusts the DCO output frequency. In contrast to the prior art in [7], no reset cycle is needed for frequency detection in this design. It also accelerates the locking speed.

To investigate the locking behavior during FA mode, the system transfer function can be derived as [12]

$$\frac{f_{\rm OUT}N(z)}{N(z)} = \frac{2f_{\rm REF}K_{\rm FA}z^{-0.5}}{1 + (K_{\rm FA} - 1)z^{-1} + K_{\rm FA}z^{-2}} \tag{4}$$

where

$$K_{\rm FA} = \frac{K_{\rm DCO}\beta_{\rm FA}}{8f_{\rm REF}} \tag{5}$$

can be adjusted by tuning DCO gain $(K_{\rm DCO})$ and the proportional path gain $(\beta_{\rm FA})$ during frequency acquisition. The root loci analysis shown in Fig. 3(a) indicates that the $K_{\rm FA}$ must be less than 1 to maintain system stability. Fig. 3(b) shows the step response. It reveals that a larger $K_{\rm FA}$ leads to a faster locking time, but also results in larger overshooting during transition.

After Φ_E variation is settled within one LSB, the frequency acquisition loop is locked and LPM will launch the phase tracking mode. Due to the quantization error of the phase accumulator, the long term frequency error is limited to one adjustable frequency step

$$\Delta f_{\rm FA} = f_{\rm OUT} - f_{\rm target}|_{\rm FA\ locked} = \pm\frac{1}{2}K_{\rm DCO}\beta_{\rm FA} \tag{6}$$

which is also proportional to $K_{\rm FA}$. It shows a trade off between locking speed and accuracy.

B. Phase Tracking (PT) Mode

During this mode, the integral path is then activated, and the whole system is turned into a 2nd order phase-locked loop.

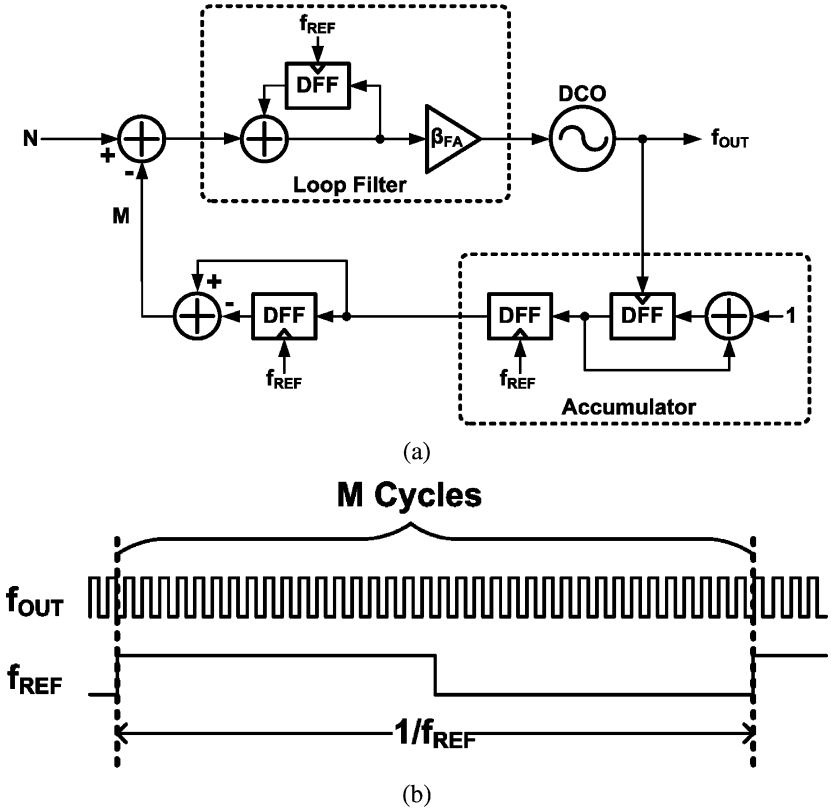

Fig. 2. (a) Frequency locked loop architecture and (b) frequency counter.

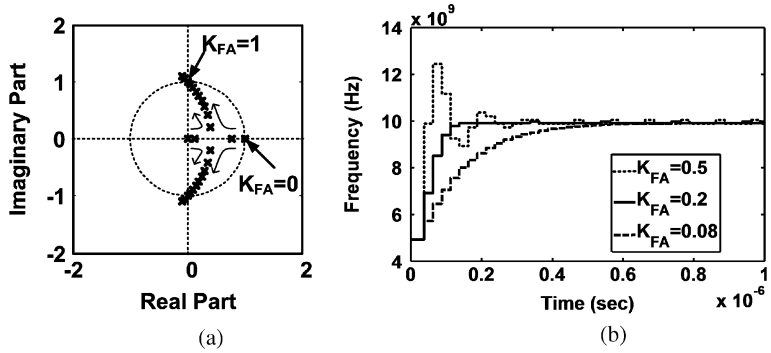

Fig. 3. (a) Root loci of frequency locked loop and (b) step response.

Meanwhile, PAC1 and PAC2 are reset, while the content of the integrator in the loop filter (Ψ_I) is preset to the current DCO control code. Afterwards, the DPD is switched to the binary phase detection mode without resorting to sophisticated time to digital converter, leading the loop to become a bang-bang PLL. By employing the binary PD, the dynamic behavior of the ADPLL resembles a 2nd order $\Delta\Sigma$ modulator [13].

Fig. 4 shows the phase trace of the bang-bang PLL during locking process [14]. Here the x axis shows the un-quantized phase error (ϕ_E), and the y axis illustrates the output of integral path of loop filter. Due to the non-linear phase detection, the bang-bang loop cannot lock onto a fix point on the phase plane. Instead, the condition of loop stability is referred to whether the phase error can settle within a bounded orbit. The constraint for stability can be derived as [14]

$$\frac{\alpha}{\beta} \leq \frac{2}{2D+1} \tag{7}$$

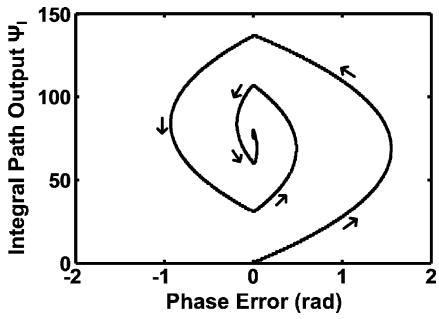

Fig. 4. Phase trace of bang-bang PLL.

where D is the loop delay normalized to a reference period.

The phase noise performance of the bang-bang PLL is further investigated by linearizing PD gain using Markov chain approximation [15], as is shown in Fig. 5. For the solid and dot lines that have the same integral path gain, a larger β will broaden the

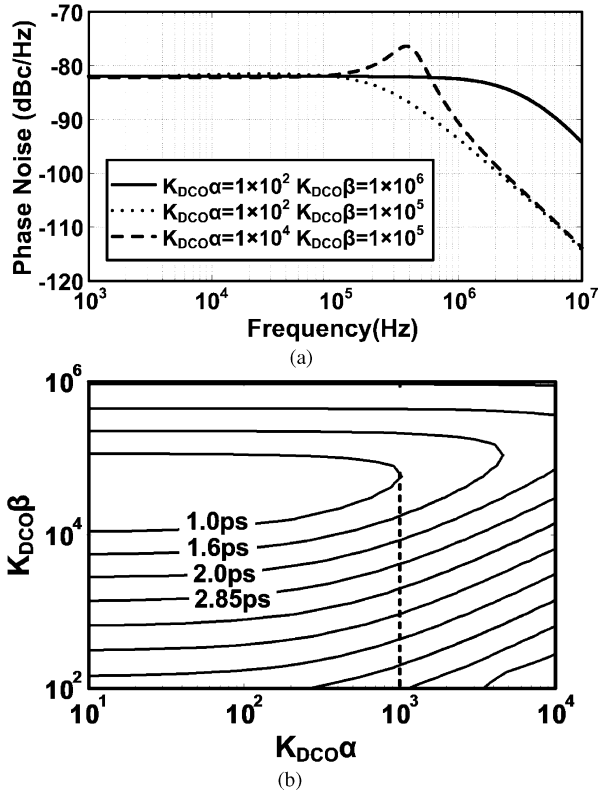

Fig. 5. (a) Phase noise performance and (b) output RMS jitter versus loop parameters.

loop bandwidth and speed up the locking process. But it may result in larger steady state jitter if the bang-bang jitter becomes a dominant noise source. On the contrary, for the dot and dash lines that have the same β, increasing α will degrade the phase margin and lead to jitter peaking, though it can also accelerate the locking speed.

The power spectrum density of phase noise performance under different loop parameters reflects in the integral timing jitter. Fig. 5(b) summarizes the jitter contours. For a constant β, it can be seen that a larger α will degrade timing jitter due to jitter peaking. On the other hand, for a constant α, the timing jitter can be improved by increasing the loop bandwidth β to a certain extent. However, this situation will be inverted if the in-band quantization noise of the bang-bang PD dominates the overall jitter performance. Thus, a severe trade-off between locking speed and jitter optimization exits without dynamic digital loop filter. Fig. 5(b) also reveals that, for a target rms jitter of less than one pico-second, a DCO gain of less than 1-kHz per LSB is required (minimum $\alpha = 1$). It imposes another design challenge for both high frequency and low noise design.

III. Circuit Implementation

A. Locking Process Monitor (LPM)

To overcome the trade-off between locking speed and jitter performance, the α and β are dynamically adjusted during locking process, and is moderated by a proposed locking process monitor (LPM). According to the $\Delta\Sigma$ modulation analogy in the bang-bang PLL behavior [13], the variation of quantized phase error Φ_E will become bounded in the steady state. The mean value of Ψ_I, $\overline{\Psi_I}$, represents the locking frequency of the PLL. Thus, the proximity of frequency lock can be detected by monitoring the ripple superimposed on $\overline{\Psi_I}$, which will diminish as the loop approaching the locking state. Based on this principle, the LPM is realized as shown in Fig. 6(a).

The LPM senses the quantized phase error Φ_E and the integral path output Ψ_I, so as to adjust α, β, and the operation mode accordingly. It is composed of an operation mode controller, peak/bottom hold detectors, a gradient polarity detector (GPD), registers, and decision logic for adjusting α and β. The PLL is initialized as a frequency acquisition loop when the frequency switching command is issued. On the other hand, it is switched to the phase tracking mode as the variation of phase error Φ_E falls within one LSB.

According to the timing diagram in Fig. 6(b), the peak and bottom values of Ψ_I occur when the polarity of Φ_E is inverted (i.e., the slop of Ψ_I changes its polarity), and is detected by the GPD. Meanwhile, the GPD generates $\Phi_{\rm sc}$ pulses to extract the peak/bottom value. The local maximum (Ψ_p) and minimum (Ψ_b) of Ψ_I can then be updated by the peak/bottom hold detector, which is toggled by $\Phi_{\rm sc}$. To rapidly determine its locking status, $\overline{\Psi_I}$ is estimated by averaging its successive peak and bottom values of Ψ_I

$$\overline{\Psi_I} = \frac{\Psi_p + \Psi_b}{2} \tag{8}$$

and the consecutive $\overline{\Psi_I}$ are then stored and compared through registers and decision circuit. The criterion of approaching lock $(\overline{\Psi_I} \approx \text{constant})$ can be expressed as

$$\left|\overline{\Psi_I(n+m)} - \overline{\Psi_I(n)}\right| \leq k \tag{9}$$

where k is the locking window and m denotes the time interval between two adjacent peak/bottom values. As $\overline{\Psi_I}$ settles within consecutive samples, the loop parameters α, and β are then reduced gradually towards its optimum value in the steady state under the constraint of loop stability, making the loop bandwidth being dynamically adjusted from a wide band mode to a narrow band mode. By adopting this control scheme, it accelerates locking speed without cycle slip while keeping low reference spur and timing jitter in the locked state.

Fig. 7 shows the simulation result of the locking behavior with and without the aid of LPM. For the same steady state loop bandwidth, the simulated locking time with the proposed scheme is about 5 μs, while that without LPM is about 50 μs. In other words, it improves the locking speed by about 10 times.

B. Phase Accumulator

In the ADPLL, the phase accumulator PAC2 is typically implemented as a synchronous counter and thus consumes significant power. Contrarily, an asynchronous accumulator can reduce power though. The accumulated timing skew due to flip-flop clock to data output delay (t_{cq}) can exceed one input clock period. Thus, the achievable multiplication factor (N) is severely limited especially with high input frequency. To overcome this problem, a novel skew-compensated asynchronous

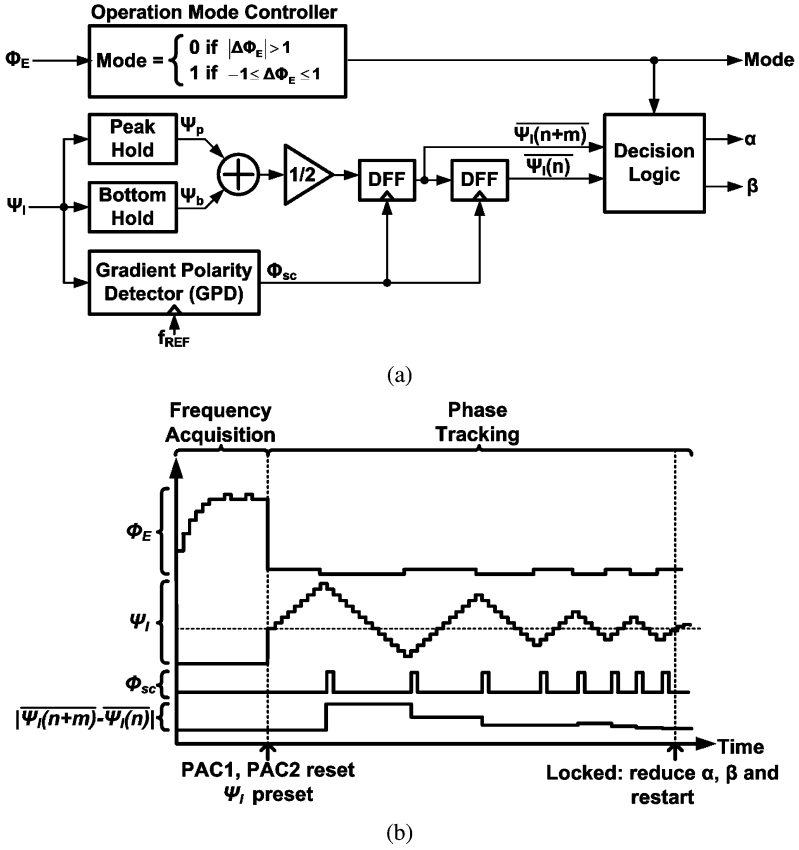

Fig. 6. (a) Locking process monitor architecture and (b) timing diagram.

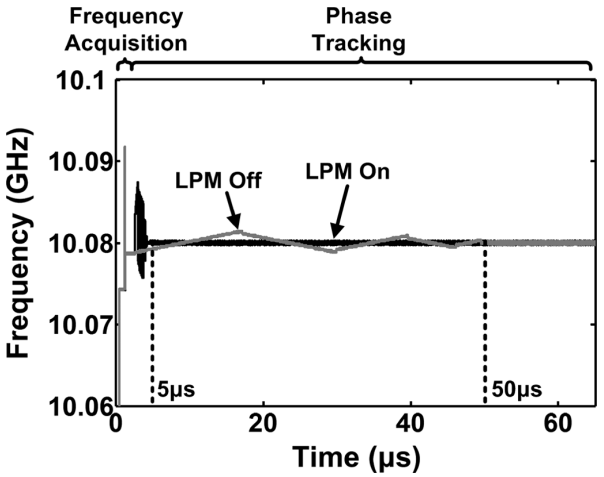

Fig. 7. Comparison of locking behaviors with and without the aid of LPM.

phase accumulator is proposed. It preserves the advantages of low power dissipation while eliminating the accumulated timing skew issue.

Fig. 8(a) shows the detailed block diagram, which is constructed by an asynchronous counter, resampling registers (S_{D0}–S_{D7}), and sampling phase generator. When $f_{\rm REF}$ comes in to fetch the contents in PAC2, the sampling phase S_1 for the 1st stage of the asynchronous counter is generated by resampling $f_{\rm REF}$ through 2 D flip-flops to avoid metastability. To circumvent the skew problem caused by clock to data output delay, instead of sampling all outputs of the counter at the same time, a series of sampling phases are generated to capture the contents of the counter.

Fig. 8(b) illustrates the timing diagram of the critical case when the contents of the asynchronous counter change from $(0,0,\ldots,0)$ to $(1,1,\ldots,1)$. In this case the overflow signal propagates from the first stage to the last stage, leading to a maximum timing skew. In the sampling phase generator, S_1 is then postponed by D-latches D_{L1}–D_{L3} that are toggled by the falling edge of the 1st–3rd stage divider outputs f_{D1}–f_{D3}, to generate the sampling phases S_2–S_4. Thus, a minimum setup time of $4T_{\rm DCO} - t_{cq} = 4/f_{\rm OUT} - t_{cq}$ can be guaranteed when retrieving the contents of the ripple counter. The stages 4 to 8 are all resampled by S_4 since a setup time of $16T_{\rm DCO} - 5t_{cq}$ is sufficient for flip-flop operating at $f_{\rm OUT}/64$ and below. The PAC2 output is then stored in $S_{D0}-S_{D7}$ as $\Phi_{\rm FB}[0-7]$. By compensating for accumulated timing skew, the uncertainty in phase detection by band-bang detector is limited to one clock cycle. It also prevents the detectable frequency resolution bounded by (6) from getting worse.

C. Digitally Controlled Oscillator (DCO)

Fig. 9 illustrates the DCO schematic, which is based on LC-tank oscillator architecture. The output frequency is varied by digitally tuning the varactor bank. A differential planar inductor of 1.2 nH is adopted. The quality factor of the inductor is about 9 at 10 GHz. The varactor is based on N-channel inversion mode device, and its simulated Q at 10 GHz is about

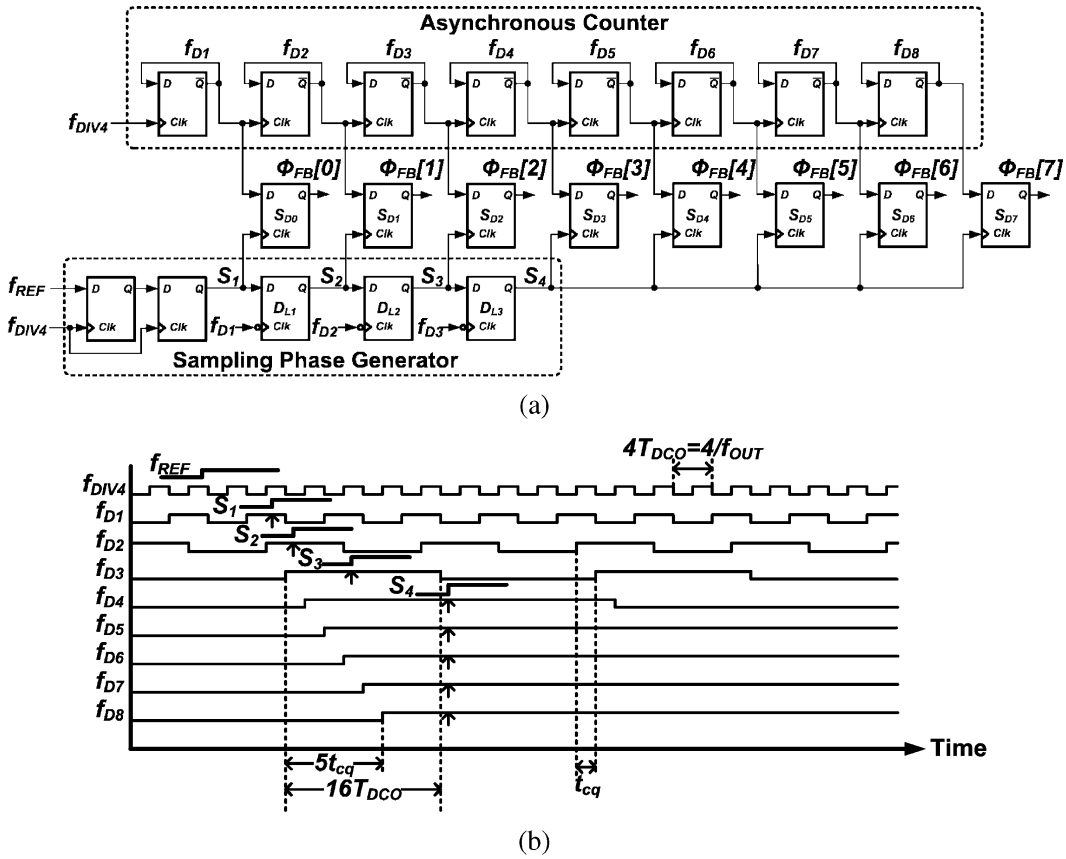

Fig. 8. (a) Skew compensated phase accumulator and (b) timing diagram.

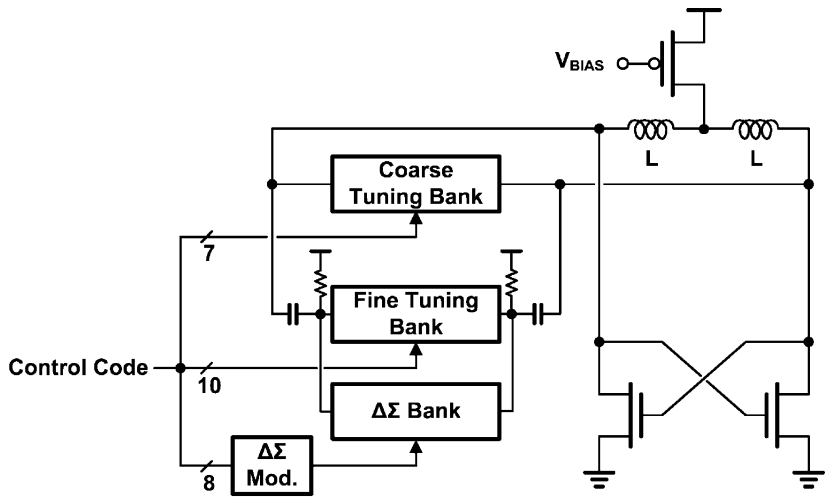

Fig. 9. DCO architecture.

25. The DCO core circuit is biased by a pMOS current source with on-chip regulator to minimize flicker noise and improve PSRR.

As are discussed in the previous sections, to achieve sub-pico second RMS jitter, the DCO resolution must be better than 1-kHz per LSB. To reduce chip area of the varactor bank, the frequency tuning is accomplished by a 7 bits coarse tuning bank, followed by a 10 bits fine tuning bank to ensure linearity. The frequency resolution is further enhanced to 250 Hz per LSB by employing high speed dithering through an 8-bit second order $\Delta\Sigma$ modulator.

IV. Experimental Results

The experimental prototype has been fabricated in a 90 nm CMOS process. Fig. 10 shows the chip micrograph. The chip size is 0.902 mm^2, which is mainly occupied by the *LC* resonator and the digital IO cells. The core area is only 0.352 mm^2. The ADPLL core consumes 7.1 mW from a 1 V supply, among

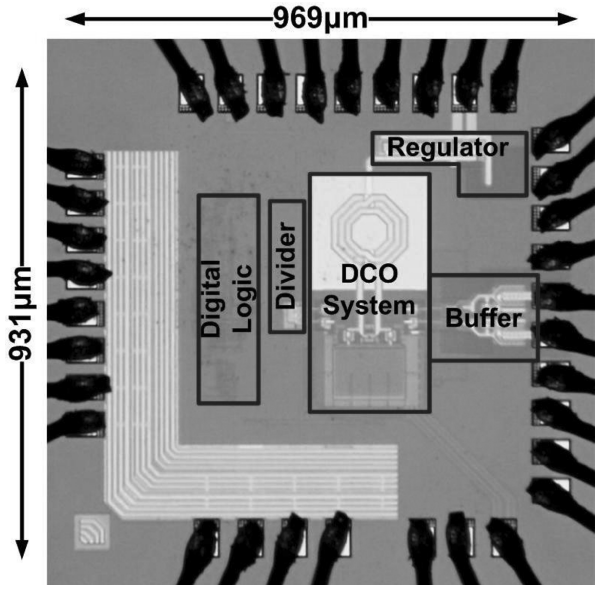

Fig. 10. ADPLL chip micrograph.

which the phase accumulator consumes 0.97 mW, the prescaler consumes 1.33 mW, the DCO consumes 3.9 mW, and logic circuitries dissipate 0.9 mW. Additionally, the digital I/O cells drain 2.7 mW from a 3.3 V supply for chip measurement.

The phase noise and PLL output spectrum are both measured using Agilent E4448A spectrum analyzer. With 40 MHz reference frequency and a multiplication factor of 248 ($N = 248$), the measured phase noise form the 9.92 GHz carrier is shown in Fig. 11. The phase noise at 1 MHz offset is about -100 dBc/Hz. By frequency domain measurement, the integrated timing jitter from 50 kHz to 80 MHz is about 1.1 ps, and is about 1.13 ps when the integrated bandwidth is extended to 1 GHz. The timing jitter is mainly dominated by the in-band noise.

For a bang-bang PLL loop with a loop delay of D clock cycle, and the ratio between integral (α) and proportional path gain (β) be $R(R = \alpha/\beta)$, the limit cycle oscillation frequency $(\omega_{\rm m})$ can be derived as [14]

$$\omega_m = \frac{\omega_{\rm ref}}{4L} \tag{10}$$

where L is the integer number that satisfies the following constraint:

$$\frac{D(2+R-RD)}{2+R-2RD} \le L \le \frac{(2-RD)(D+1)}{2-R-2RD}. \tag{11}$$

In this design, $\alpha = 1, \beta = 256$, and $D = 0.5$ in the steady state. By substituting the design parameters into (10) and (11), the DCO output frequency is modulated in a rectangular waveform at $\omega_m = 10$ MHz due to bang-bang operation, whose peak to peak frequency deviation $(\Delta\omega_{\rm pp})$ is about $2\beta K_{\rm DCO}$. By Fourier series expansion, cyclic tones at $\omega_{\rm DCO} \pm n\omega_m$ can be seen around the DCO output frequency $\omega_{\rm DCO}$.

Fig. 12 shows the measured output spectrum from a 9.92 GHz carrier. Spurious tones at 10 MHz and 30 MHz offset are respectively -51 dB and -70 dB below the main carrier. The reference spur at 40 MHz offset is about -72 dB below the main carrier. For wireless communication applications, spurious tones should

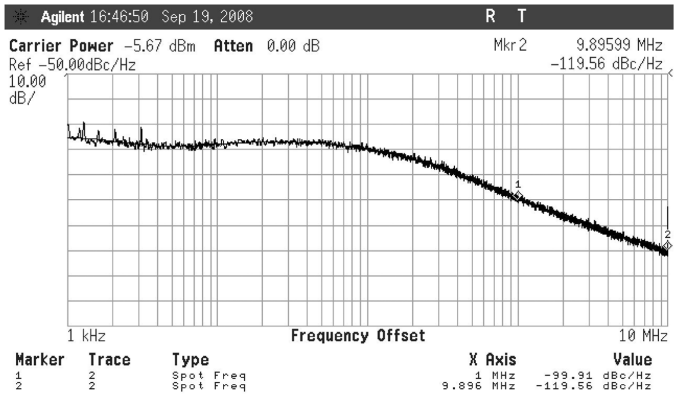

Fig. 11. Phase noise performance.

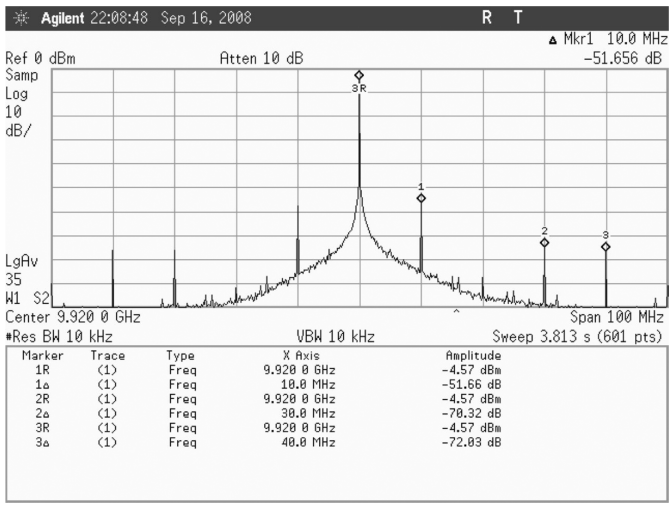

Fig. 12. Output spectrum.

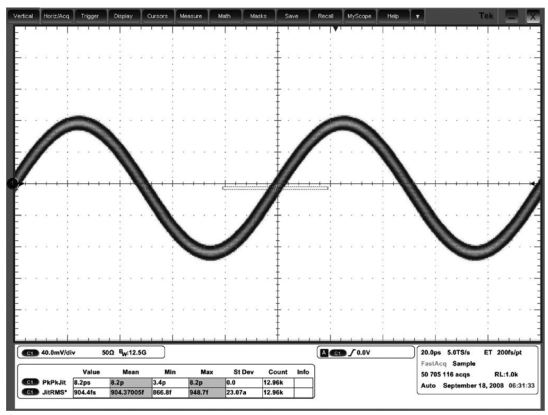

Fig. 13. Measured time domain waveform.

be suppressed to avoid reciprocal mixing issues, which can be achieved by adjusting β to decrease $\Delta\omega_{\rm pp}$.

The time domain performance is characterized using Tektronix DPO71254 oscilloscope. Fig. 13 shows the time domain waveform. The measured rms jitter is about 0.9 ps, including random jitter, periodic jitter, and the trigger jitter of the instrument for about 100 fs (rms). The jitter measured in time domain is quite close to that characterized in the frequency domain, and

TABLE I
PERFORMANCE BENCHMARK

Reference	Tech.	Supply	Power	Frequency range	Phase Noise	Locking Time	Reference Frequency/ Multiplication Factor
[1] 05' JSSC	90nm	1.2V	19.6mW(1) (4.9 mW/GHz)	3.2GHz~4.0GHz	-165dBc/Hz @ 20MHz(2)	10μs	26MHz (N=31.7)
[2] 05' JSSC	130nm	1.5V	19.5mW (4.02 mW/GHz)	2.08GHz~2.25GHz 3.16GHz~3.66GHz 4.1GHz~4.85GHz	-118dBc/Hz @1MHz	N/A	200MHz (N=24)
[3] 08' JSSC	65nm	0.9V	17.2mW (3.37 mW/GHz)	0.5GHz~5.1GHz	-112dBc/Hz @1MHz(3)	N/A	500MHz (N=8)
[4] 08' ISSCC	130nm	1.5V	39mW (NA)	N/A	-132dBc/Hz @3MHz	20μs	50MHz (N=74)
[5] 08' ISSCC	130nm	N/A	40mA (10mA/GHz)	3.2GHz~4.0GHz	-126dBc/Hz @1MHz	N/A	26MHz (N=138.98)
This Work	90nm	1.0V	7.1mW (0.71 mW/GHz)	9.75GHz~10.17GHz	-100dBc/Hz @1MHz	6.9μs	40MHz (N=248)

(1) Power dissipation for DCO and time-to-digital converter only

(2) Measured from 900 MHz carrier

(3) Measured from 4 GHz carrier

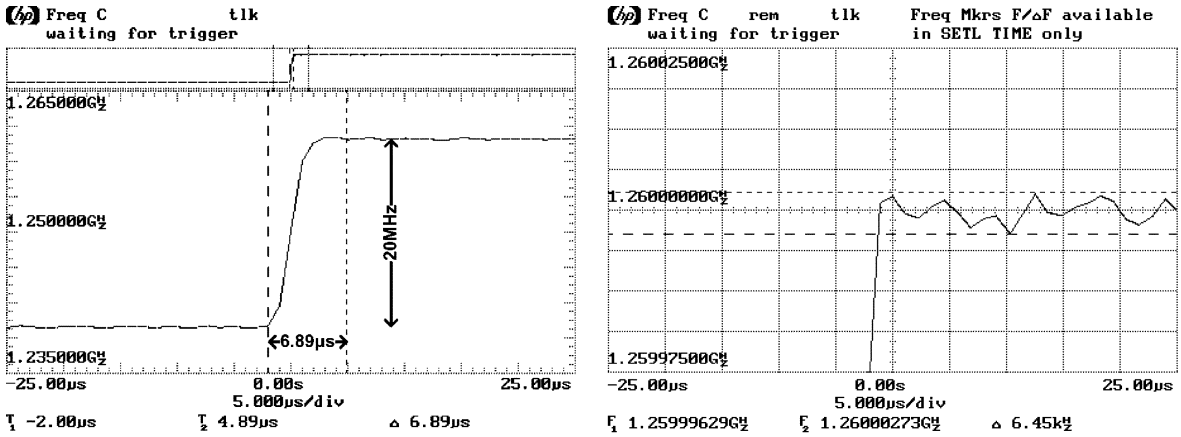

Fig. 14. (a) Measured locking time and (b) the zoomed-in locking behavior.

the timing jitter deteriorated by the spurious tones is negligible compared to its random jitter.

For locking behavior characterization, the divide-by-8 output is measured to comply with the input bandwidth of the modulation domain analyzer (Agilent 53310A). When the output frequency hops form 9.92 GHz to 10.08 GHz, the measured settling time within 20 ppm accuracy is about 6.89 μs, as is shown in Fig. 14(a). Fig. 14(b) shows the zoom-in version of the locking characteristic.

Table I summarizes the ADPLL performance and benchmark with the state of the art in the literature. The proposed architecture manifests the highest output frequency, fastest locking time, highest multiplication factor, and also highest power efficiency in terms of GHz/mW.

V. CONCLUSION

This paper presents a 10 GHz all-digital frequency synthesizer with less than 1 ps rms jitter and less than 7 μs locking time. The ADPLL manifests fast locking speed as well as low jitter performance by the dual mode phase and frequency detection scheme and dynamically reconfiguring the digital loop filter, which is governed by the proposed LPM engine. Also, the output jitter is comparable to most analog PLLs without resort

to sophisticated TDC. Finally, a novel skew-compensated asynchronous phase accumulator is proposed. Operating as an asynchronous counter, it preserves the advantages of power scaling while capable of high speed operation and providing high division ratio.

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