# The Role of High-κ TiHfO Gate Dielectric in Sputtered ZnO Thin-Film Transistors



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# The Role of High-$\kappa$ TiHfO Gate Dielectric in Sputtered ZnO Thin-Film Transistors

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In this study, we demonstrate the role of a titanium hafnium oxide (TiHfO) gate dielectric in improving the overall electronic performance of a ZnO thin-film transistor (TFT). $Ti_xHf_{1-x}O$ ($x = 0.63$) was fabricated by the rf co-sputtering technique. Using TiHfO as the gate dielectric, the device fabricated in this study exhibits a threshold voltage of 0.34 V, a subthreshold swing of 0.23 V/dec, a field-effect mobility of 2.1 $cm^2 V^{-1} s^{-1}$, and an ON/OFF current ratio of $10^5$. The small subthreshold swing and low positive threshold voltage are attributed to the higher value of $\kappa$ of 40 for the dielectric. This result enables device operation below 2 V, allowing its use in low-power driving circuits in display applications.


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## 1. Introduction

Recently, ZnO thin-film transistors (TFTs) have become emerging devices in the fields of microelectronics and optoelectronics.[1–18] Owing to their good device performance, low-cost fabrication process, and their potential for realizing transparent and flexible active circuits, ZnO TFTs are strongly expected to replace conventional silicon TFTs for many applications such as display backplanes and even driving circuits. Silicon oxide ($SiO_2$),[3–8] silicon nitride ($Si_3N_4$),[9–11] and aluminum oxide ($Al_2O_3$)[12–14] have been conventionally adopted as the gate insulators of ZnO TFTs since they are convenient for device fabrication. However, the low dielectric constants of these dielectrics lead to poor gate control over the driving current, resulting in ZnO TFTs suffering from a high threshold voltage ($V_T$), poor subthreshold swing ($SS$), and high operation voltage. A promising approach to solving these problems and realizing high-performance ZnO TFTs is to enhance the gate capacitances of TFTs. In this regard, it is preferable to introduce dielectric materials with a higher $\kappa$ value, since lowering the physical thickness of conventional gate insulators will worsen the gate leakage.

Recently, considerable effort has been devoted to investigating suitable high-$\kappa$ materials for the gate dielectrics of ZnO TFTs.[15–18] A high-$\kappa$ material must meet a variety of requirements to be suitable for the gate insulator for field-effect devices with a metal–oxide–semiconductor (MOS) structure such as metal–oxide–semiconductor field-effect transistors (MOSFETs) or TFTs. These requirements include a sufficient wide bandgap, a suitable band offset relative to the channel material, low trap density, high thermodynamic stability, simple process compatibility, and predictable reliability.[19] Among the numerous high-$\kappa$ dielectrics, $HfO_2$ has good electronic properties and high thermal stability but only a moderate $\kappa$ value. $TiO_2$ is known for its much higher $\kappa$ value than other binary oxide materials, but its disadvantage is its relatively narrow bandgap, which is responsible for the worse gate leakage current due to the higher probability of Schottky emission. The other problem of pure $TiO_2$ is its low crystallization temperature; the crystallization of $TiO_2$ usually leads to a dramatic increase in leakage current.[20] The mixture of $TiO_2$ with another medium-$\kappa$ dielectric is expected to simultaneously result in an elevated dielectric constant, an acceptable bandgap, and a higher crystallization temperature.[20–24] In this study, we integrate $HfO_2$ into $TiO_2$, and the ternary oxide TiHfO exhibits a $\kappa$ value of 40 with an acceptable gate leakage.[22–24] Using the TiHfO gate dielectric, this ZnO TFT exhibits the promising results of a low $V_T$ of 0.34 V, a small $SS$ of 0.23 V/dec, an average $I_{on}/I_{off}$ ratio of $10^5$, and an average $\mu_{FE}$ of 2.1 $cm^2 V^{-1} s^{-1}$.

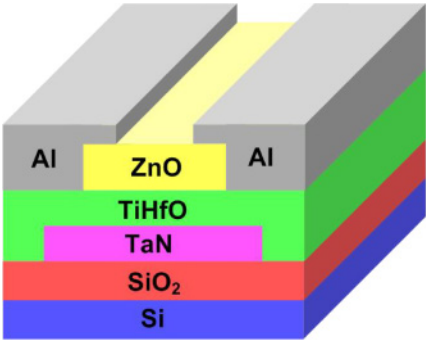


**Fig. 1.** (Color online) Schematic diagram of the bottom-gate ZnO TFT with TiHfO gate dielectric.

## 2. Experiments

Figure 1 shows a schematic cross-sectional view of a bottom-gate ZnO TFT. A Si wafer with a 500-nm-thick wet oxide on it was used as the substrate. Then a 50-nm-thick TaN layer was deposited by reactive sputtering as the bottom gate electrode. Before the deposition of the high-$\kappa$ gate dielectric, $NH_3^+$ plasma treatment was applied to improve the TaN/high-$\kappa$ interface. This treatment can effectively reduce the gate leakage and preserve the high capacitance density.[20] This was followed by the deposition of a 50-nm-thick TiHfO film by rf co-sputtering using $TiO_2$ and $HfO_2$ targets in a gas mixture of $O_2$/Ar with ratio 1 sccm/10 sccm. To form a denser texture and repair the defects in the high-$\kappa$ dielectric, the prepared samples were subjected to post-deposition annealing (PDA) in oxygen ambient at 300–600 °C to evaluate the effect of temperature on the defects in the high-$\kappa$ dielectric and device character-

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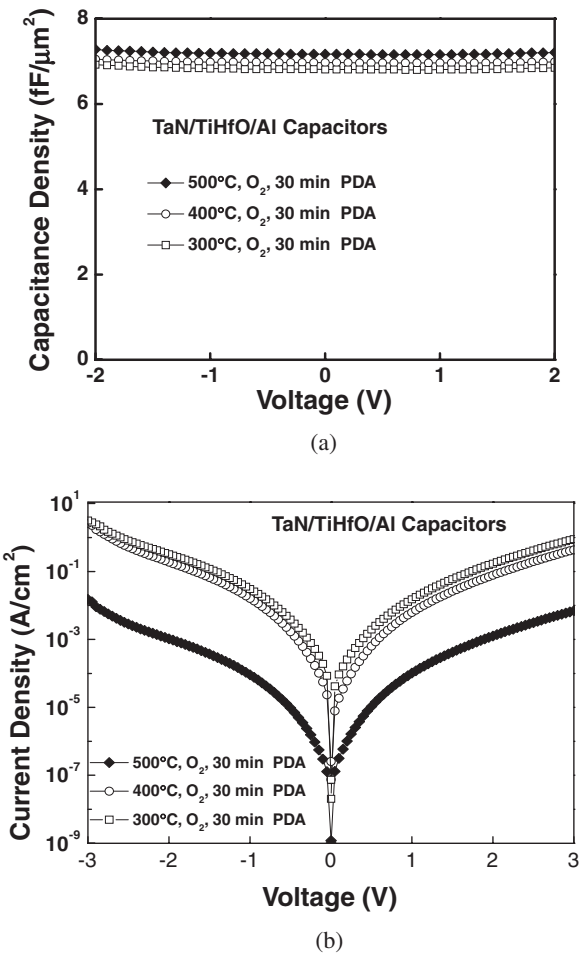


**Fig. 2.** (a) *C*–*V* and (b) *J*–*V* characteristics of TaN/TiHfO/Al capacitors annealed at different PDA temperatures.

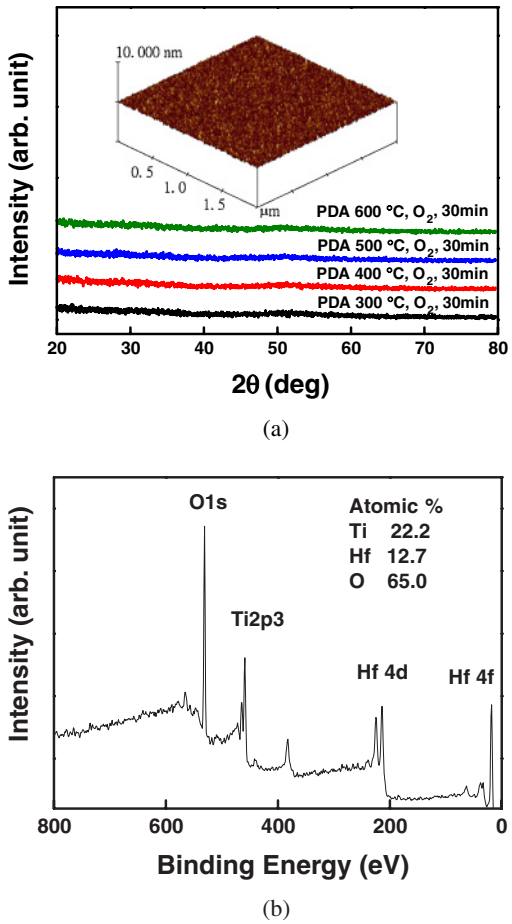


**Fig. 3.** (Color online) (a) XRD analysis of TiHfO films annealed at 300–600 °C and AFM image of the TiHfO top surface on the TaN/$SiO_2$/Si substrate. (b) XPS spectrum of a TiHfO film annealed at 500 °C.

istics. After that, a ZnO film was deposited by sputtering using a ZnO target (99.99%) at room temperature in an $Ar/O_2$ (10 : 1) 10 mTorr gas mixture. Finally, 300-nm-thick Al was deposited using a thermal coater to form the source and drain contacts. For expedience, all device patterns were defined through shadow masks with a gate size of $50 \times 500\,\mu m^2$, without regard to the effects of lithographic and etching processes. To evaluate the properties of the high-$\kappa$ material, metal–insulator–metal (MIM) capacitors were also fabricated to estimate the gate capacitance and gate leakage current. The devices were characterized by current density–voltage (*J*–*V*) and capacitance–voltage (*C*–*V*) measurements using an HP4156C semiconductor parameter analyzer and an HP4284A precision LCR meter, respectively.

## 3. Results and Discussion

Figure 2 shows the *C*–*V* and *J*–*V* characteristics of the prepared TaN/TiHfO/Al MIM capacitors. From the capacitance density of $7\,fF/\mu m^2$ and the physical thickness of 50 nm, we estimated that this TiHfO dielectric has a high $\kappa$ value of about 40, which could greatly improve the driving current of ZnO TFTs. The leakage current of the capacitor annealed at 500 °C is about two orders of magnitude lower than that of the capacitors annealed at 300 and 400 °C. However, the capacitor annealed at 600 °C did not exhibits normal *C*–*V* and *J*–*V* characteristics, probably due to the degradation of the bottom TaN gate upon heating at a relatively high temperature for a long time. Figure 3(a) shows the result of X-ray diffraction (XRD) analysis of TiHfO films annealed at 300–600 °C. The amorphous TiHfO after PDA is helpful for reducing the gate leakage current. In the inset of Fig. 3(a), we show an atomic force microscopy (AFM) image of the surface of a TiHfO film deposited on the bottom TaN gate. The surface roughness of an insulator has a direct impact on the interface between the gate and channel for a bottom-gate TFT. The root-mean-square (RMS) roughness of 0.63 nm revealed by this image is negligible compared with the 50 nm thickness of the insulator. Figure 3(b) shows the X-ray photoelectron spectroscopy (XPS) spectrum of $Ti_xH_{1-x}O$ after 500 °C annealing in $O_2$ ambient for 30 min. The existence of Ti, Hf, and O is clearly shown in the XPS spectrum, from which the composition was determined to be $Ti_{0.63}Hf_{0.37}O$. This composition is consistent with our previous studies on MIM dynamic random access memories (DRAMs),[23,24] in which excess $TiO_2$ was shown to cause a severe leakage problem while an insufficient amount of $TiO_2$ resulted in no appreciable increase in the $\kappa$ value. This composition gives a reasonable $\kappa$ value of 40, which is between the values of 25 for $HfO_2$ and 50–80 for $TiO_2$.[19] Figure 4 shows a comparison of $I_D$–$V_G$ characteristics for ZnO TFTs with high

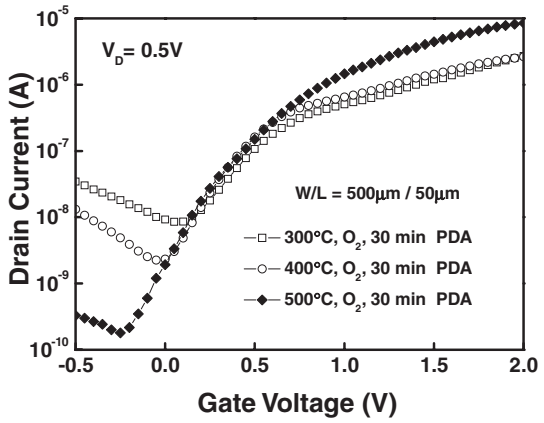


**Fig. 4.** Comparison of $I_D$–$V_G$ characteristics of ZnO TFTs with TiHfO gate dielectric annealed at 300–500 °C.

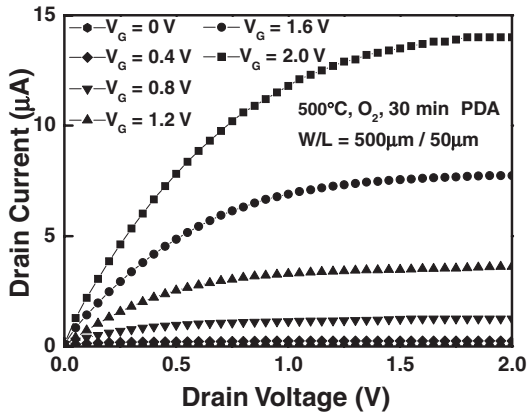


**Fig. 5.** Output characteristics of a ZnO TFT after PDA at the optimal temperature of 500 °C. The dimensions of W/L are 500 μm/50 μm.

$\kappa$ annealed at 300–500 °C. The reverse leakage current was about two orders of magnitude higher after annealing at 300 and 400 °C than after annealing at 500 °C, probably because more unrepaired defects exist after lower-temperature treatment. Figure 5 shows the output characteristics of a ZnO TFT for a gate voltage ranging from 0 to 2 V with steps of 0.4 V. These curves demonstrate typical enhancement-mode operation with a hard saturation phenomenon under operation at a small $V_G$ and $V_D$ of less than 2 V. We attempted to fabricate a ZnO TFT that can operate under 2 V. Currently, when considering the commonly used display devices such as liquid crystal displays (LCDs), electronic paper, and organic light-emitting diodes (OLEDs), 2 V seems too low. However, as a step toward realizing displays with low operation voltages, and hence low power consumption, it is important to achieve TFTs that can operate under 2 V. We chose a dielectric thickness of 50 nm with consideration of the target voltage of 2 V. In particular, this thickness resulted in a sufficiently low gate leakage current at voltages of less than 2 V. Figure 6 shows the transfer characteristics of a ZnO TFT annealed the optimal temperature of 500 °C. The OFF current is about $10^{-10}$ A and the ON/OFF ratio of drain current ($I_{on}/I_{off}$) is approximately $10^5$. The field-effect mobility ($\mu_{FE}$) can be extracted using the following equation:

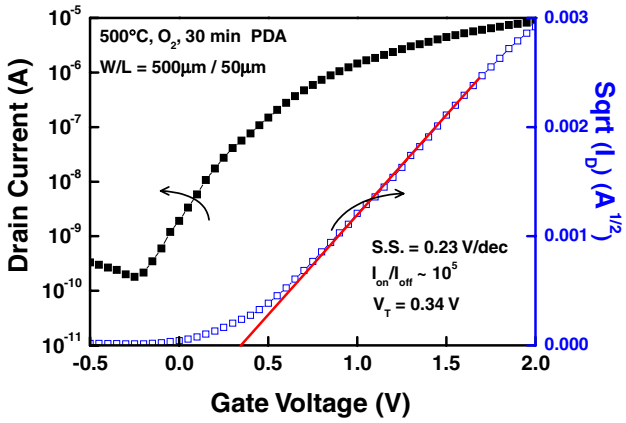


**Fig. 6.** (Color online) Transfer characteristics of a ZnO TFT after PDA at the optimal temperature of 500 °C. $\mu_{FE}$ and $V_T$ were determined from the linear $I_D^{1/2}$ vs $V_G$ plot.

$$I_D = \frac{C_i \mu_{FE} W_G}{2L_G}(V_G - V_T)^2, \tag{1}$$

where $C_i$ is the gate capacitance per unit area of the gate insulator, $W_G$ is the channel width, $L_G$ is the channel length, and $V_T$ is the threshold voltage. This device exhibited a low $V_T$ of 0.34 V and an acceptable $\mu_{FE}$ of 2.1 $cm^2 V^{-1} s^{-1}$, which were obtained by curve fitting to the plot of $I_D^{1/2}$–$V_G$. This mobility is satisfactory for LCD pixel transistors since it is better than that of hydrogenated amorphous silicon (a-Si:H), which has a typical mobility of below 1 $cm^2 V^{-1} s^{-1}$, and has been used in TFTs.[25]

The subthreshold swing (*SS*) can also be determined from the transfer curve using the following definition:

$$SS = \frac{dV_G}{d\log I_D} \tag{2}$$

From the transfer characteristics shown in Fig. 6, a small *SS* of 0.23 V/dec is acquired.

Table I shows a comparison of the major characteristics of ZnO TFTs with various gate dielectric materials. The performance of the TiHfO ZnO TFT is comparable to that of other devices. This device has a higher mobility than devices based on $SiN_x$, $Al_2O_3$, $CeSiO_x$/PVP and $HfO_2$ gate dielectrics, possibly due to the smaller roughness of the high-$\kappa$/ZnO interface (as a result of $NH_3$ plasma treatment) and the lower bulk trap density in high-$\kappa$ dielectric (resulting from the relatively thin gate dielectric). In addition to the merit of low operation voltage, the ZnO TFT with a TiHfO gate dielectric also exhibits a steep subthreshold swing, and a small positive threshold voltage. The *SS* of TFTs can also be expressed by the following equation:[26]

$$SS = \frac{kT}{q}\ln 10\left(1 + \frac{C_{it} + C_{dep}}{C_i}\right), \tag{3}$$

where $C_{it}$, $C_{dep}$, and $C_i$ are the interface charge capacitance, depletion capacitance, and gate insulator capacitance, respectively. Therefore, a desired small *SS* can be obtained by directly increasing $C_i$ ($C_i = \varepsilon_{high\text{-}\kappa}/t$, where $\varepsilon_{high\text{-}\kappa}$ and $t$ are the dielectric constant and thickness of the insulator, respectively), which we achieved by using TiHfO, whose $\kappa$ is 40, in this work.

**Table I.** Comparison of ZnO TFTs with various gate dielectrics.

| | TiHfO (This work) | $SiO_2$[8] | $SiN_x$[9] | $Al_2O_3$[13] | $CeSiO_x$/PVP[15] | $HfO_2$[18] |
|---|---|---|---|---|---|---|
| Thickness (nm) | 50 | 110 | 180 | 160 | 50/40 | 100 |
| $\mu_{FE}$ ($cm^2\,V^{-1}\,s^{-1}$) | 2.1 | 15 | 1.698 | 1.13 | 0.48 | 1.3 |
| $V_T$ (V) | 0.34 | 5 | 2.5 | 0.8 | 0.3 | 0.3 |
| $SS$ (V/dec) | 0.23 | — | 3.82 | 1.65 | — | 0.5 |
| $I_{on}/I_{off}$ | $10^5$ | $10^7$ | $10^5$ | $10^6$ | $5 \times 10^3$ | $10^6$ |
| Operation voltage (V) | 2 | 30 | 10 | 30 | 3 | 7 |

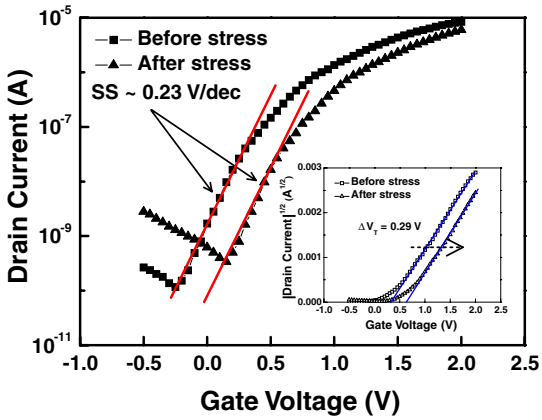


**Fig. 7.** (Color online) Typical shift in transfer characteristic upon application of gate bias stress of +2 V for $10^4$ s.

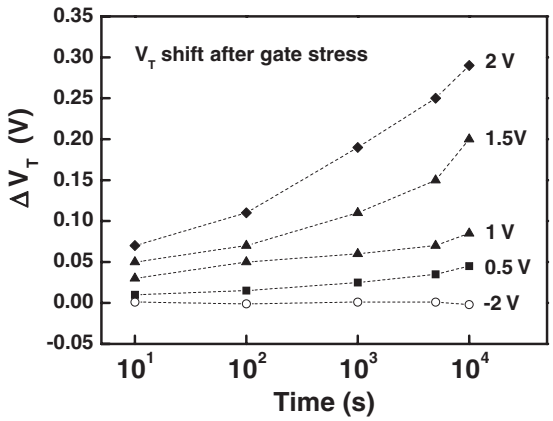


**Fig. 8.** Variation of $\Delta V_T$ with the duration of stress for different applied biases.

Although the value of $V_T$ for an oxide semiconductor TFT is strongly affected by the formation conditions of the active layer such as the fabrication technique used,[2] the atomic composition,[3] and the physical thickness,[7] etc., an enhancement mode operation is usually favored in the circuit design. Moreover, the lowering of $V_T$ for an enhancement mode TFT is greatly required, which can also be achieved by increasing $C_i$ as indicated by the following expression:[26]

$$V_T = \phi_{ms} - \frac{Q_{tot}}{C_i} - \frac{Q_{dep}}{C_i} + 2\phi_F, \qquad (4)$$

where $\phi_{ms}$ is the work function difference between the gate metal and the semiconductor, $\phi_F$ is related to the Fermi level and the intrinsic level of the semiconductor, $Q_{tot}$ is the total oxide charge, and $Q_{dep}$ is the depletion charge. As a result, a higher capacitance may result in a lower threshold voltage.

The electrical stability of the ZnO TFT was evaluated under constant gate bias stress. Figure 7 shows a comparison of two transfer characteristics of a virgin TFT device before and after stress. After a 2 V stress on the gate for $10^4$ s, the transfer curve shifted in the positive direction, causing change in threshold voltage ($\Delta V_T$) of 0.29 V, which was calculated from the characteristics in the inset of Fig. 7. The slopes of these two transfer curves are almost unchanged, which indicates that no significant interface states are created by the process of gate bias stress. Figure 8 shows the variation of $\Delta V_T$ with the duration of bias stress for different applied voltages. It can be seen that $\Delta V_T$ increases with increasing duration of bias stress and increasing magnitude of the applied positive voltage. A negative bias stress does not cause any change in $\Delta V_T$ since the negative bias tends to deplete the n-type channel, and hence no available carriers are trapped in the dielectric or interface to alter $V_T$.

## 4. Conclusions

High-performance bottom-gate ZnO TFTs with high-$\kappa$ TiHfO as a gate insulator with an acceptable $\mu_{FE}$ of 2.1 $cm^2\,V^{-1}\,s^{-1}$, a low $V_T$ of 0.34 V, a small $SS$ of 0.23 V/dec, and a average $I_{on}/I_{off}$ of $10^5$ have been fabricated and characterized. The excellent $SS$ and the low positive $V_T$ are due to the high $\kappa$ value of the TiHfO gate insulator. These results reveal that TiHfO is a promising gate dielectric material for ZnO TFTs applied in display backplanes.

## Acknowledgments

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