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Automated bonding position inspection on multi-layered wire IC using machine vision

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No available method can automatically verify the correctness of the wire bonding positions on a multi-layered wire IC. This paper presents a novel method that integrates image processing and wire bonding simulation techniques. The proposed method first takes the IC leadframe image and calculates the lead information before actual wire bonding begins. The wire bonding position information is then generated to simulate the actual wire bonding process. The generated pseudo bonding information is then compared with that from a referential machine. This approach can check the wire bonding position correctness before any actual wire bonding is executed. This approach can fully solve the mal-detection and lost detection problems that may occur in other available methods. The experimental results show that the proposed bonding position check (BPC) method is robust and fast enough for applied multi-layered wire IC inspection synchronously with the wire bonding process.

Keywords: vision inspection; bonding position check

1. Introduction

Wire bonding is a process that makes the connection between an IC chip and the base material. The leadframe and substrate are the two types of commonly used base materials. Bonding the wires onto the IC chip is a very critical procedure because the original connection areas of an IC chip are too small to be welded onto the PCB. Some base material is devised and used as the connecting medium between the IC chip and the PCB. Each of the connections on an IC chip is called a pad. The interval between two adjacent pads is generally referred to as a pitch. The internal connector on the base material is called a lead. Typically, a gold wire of high purity (99.99%) is used to connect the pad and corresponding lead. A bonding ball is formed on the pad, while a bonding stitch is formed on the lead. One lead may consist of more than one bonding stitch. The image of an entire chip with 216 leads and 312 surrounding wires is shown in Figure 1. The image of a single leadframe unit without the IC chip is shown in Figure 2. A part of the enlarged wire-bonded IC image is illustrated in Figure 3.

In ordinary IC packaging foundries, the R&D department first generates the bonding diagram with the wire bonding positions according to required spec, as shown in Figure 4(a). Subsequently, production engineers set up the bonding machine with the correct wire bonding positions based on the given bonding diagram. With the increasingly

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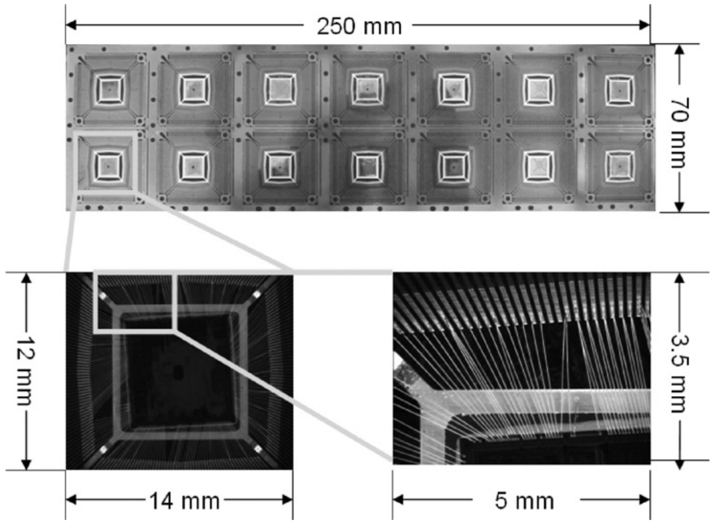


Figure 1. Diagram of IC chips with bonding wires on the base material (leadframe).

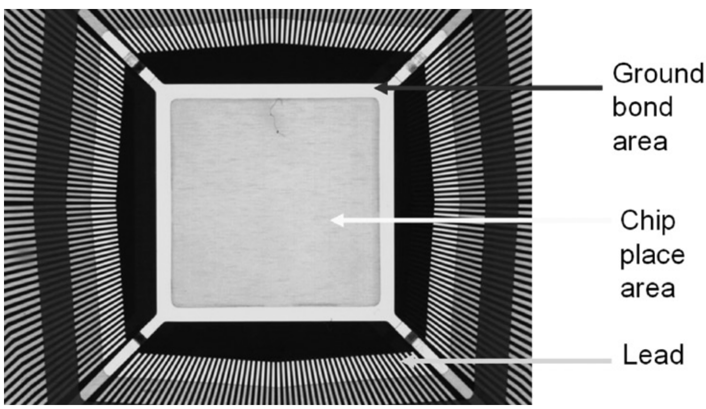


Figure 2. Image of a single leadframe unit before the die is attached.

complicated IC functions, the number of wires has reached several hundreds. For example, the number of wires in a leadframe IC can range up to 300. It takes about 2 to 3 hours for an engineer to set up the corresponding positions for the wires to be bonded. During the tedious set up process, it is inevitable that mistakes will occur in the wire bonding positions, resulting in incorrect wire bonding. Figure 4(b) is an illustration of a magnified part of Figure 4(a). Figure 4(c) shows a magnified correct bonding image of a part of Figure 4(a). Figure 4(d) shows an example of incorrect bonding in which a wire was bonded onto the wrong lead.

For each production order, IC packaging foundries need several bonding machines to work at the same time to reduce the cycle time. The engineer duplicates the bonding program from the first set up bonding machine into other bonding machines. In duplicating the bonding program, engineers must calibrate the bias of the wire

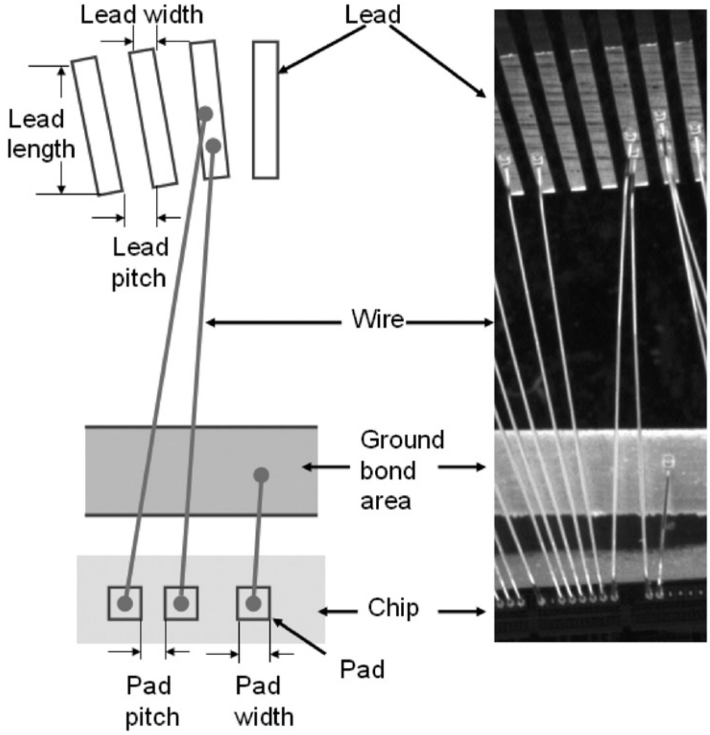


Figure 3. Enlarged image of an illustration of a wire-bonded IC.

bonding positions for all of the bonding machines. This process is prone to incorrect wire bonding position set up during this very tedious process. For example, the wire bonding positions of different bonding machines will be affected by the illumination bias of each machine. The bonding position of each wire must be adjusted manually. Even on the same bonding machine, the wire bonding positions must frequently be adjusted manually throughout the bonding process. As with the lead position variation, the leadframe-based material is fabricated by punching or etching and has the problem of high variation and low accuracy for each lead. This implies that in the punching or etching process a lead will invariably be shifted and the engineer must adjust the wire bonding positions in order to fit the variation. Figure 4(e) shows a wire bonded to a position that is slightly higher than the designed position. However, it is still bonded on the same lead and is accepted as a correct bond. Figure 4(f) shows a ground bond that is shifted slightly to the right but is still in the acceptable position. Another issue, electroplating quality, will also affect the leadframe quality and consequently affects the wire bonding positions.

Because wrong bonding is a serious problem that is non-reworkable, it is critical that every wire bonding position be correct. Most IC packaging foundries rely on humans with the aid of microscopes to check the wire bonding position correctness (ASTM 1999). Such manual inspection is prone to errors and cannot work synchronously with the bonding machines. This paper presents a novel method for automatically inspecting the wire bonding position correctness of the multi-layered wire IC. The proposed approach also works synchronously with the bonding machine. The rest of this paper is organised

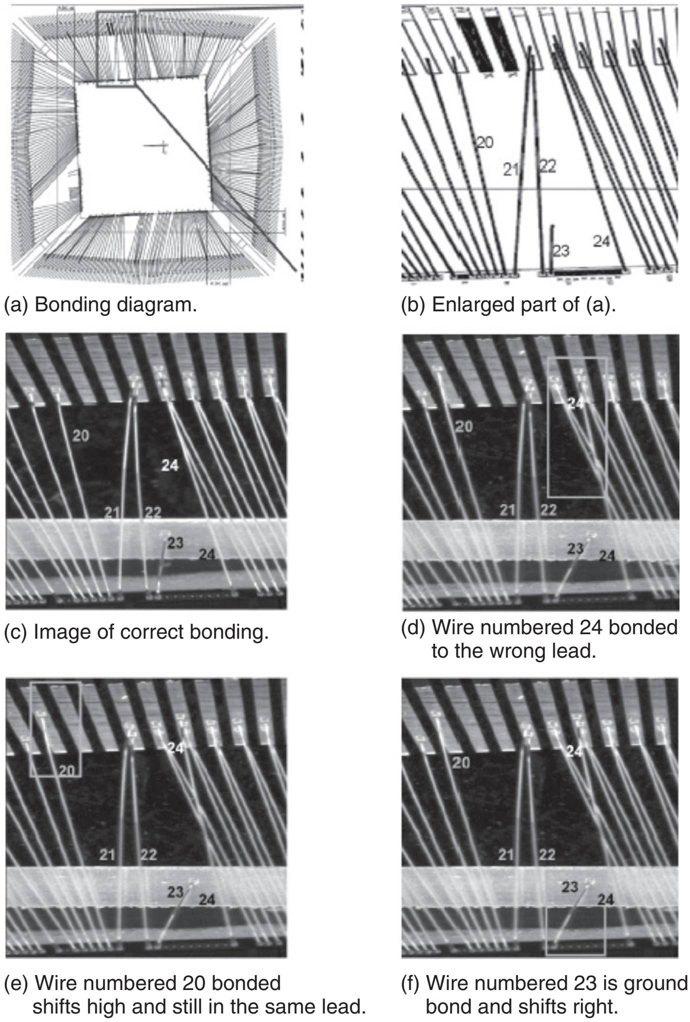


Figure 4. Diagram of a wire-bonded IC.
Note: (b) is an enlarged image of a part (a); (c), (d), (e), and (f), are enlarged images of the same bonding samples.

as follows. Section 2 presents a survey of the research on wire bonding position inspection. The proposed method is described in Section 3. Some inspection experiments and the performance analysis of the proposed approach are presented in Section 4. Section 5 presents our conclusions and suggested future research.

2. Literature review

In the wire bonding inspection process the inspectors focus on: (a) the position of the bonding wire; and (b) the contour and position of the bonding ball (Ahmed *et al*. 1990). Khotanzad *et al*. (1992, 1994) presented an automatic system for evaluating bonding ball quality. Sreenivasan *et al*. (1993) presented a method to compute the bonding ball's shape, size and location to determine its quality. All of their systems (Ahmed *et al.* 1990, Khotanzad *et al.* 1992, 1994, Sreenivasan *et al.* 1993) can determine the location of the bonding ball from a 2D image of an IC wafer and extract bonding ball geometrical information. Tsukahara *et al.* (1991) presented a vision inspection system for IC bonding wire that uses high contrast image capture and an accurate bonding-ball measurement algorithm based on sub-pixel and morphological techniques.

With the development of automatic optical inspection (AOI) technology, the IC packaging foundries attempted to improve the wire bonding position inspection using an AOI system. The AOI system has emerged as an effective inspection approach in PCB assembly (Imagen Inc. 2009, Machine Vision Products Inc. 2009, Tsai and Su 2009), but is still not ready for wire bonding position inspection in IC packaging foundries. Ayoub (2006) pointed out the AOI system problems with wire bonding position inspection. The commercial systems still need to enhance the signal to noise ratio, extend the defect coverage from single wire ICs to multi-layered wire ICs and increase the inspection speed. The ability to separate the wire from a complex varying background between the die and pad is an important aspect of post-wire-bond inspection. Accomplishing this task requires smart illumination and inspection algorithms to work together to increase the signal-to-noise ratio between the wire and its surroundings. Wang *et al.* (2002) presented a machine vision inspection technique with a defect detection algorithm for the bonding ball and bonding wire. Their experimental results showed that a good lighting condition can improve the recognition rate.

Ngan and Kang (1988) presented an algorithm for inspecting the bonding wire. They used Hough transformation to determine the straight-line equation of the bonding wire. A fibre optic ring light was used as the light source to highlight the bonding wires. Ye *et al.* (2000) presented an inspection system that applied a stereo vision technique to detect the defects related to the 3D profile of bonding wires. They proposed that the illumination system should maximise the light reflected from the bonding wires and minimise the light reflected from the surface of the chip. Perng *et al.* (2003, 2007a,b) devised a vision inspection system equipped with a structured lighting system to highlight the bonding wire. Their system can be used for the on-line inspection of single layer wire ICs. In the multi-layered wire IC case, such as that shown in Figures 5 and 6, none of the existing 2D image inspection methods (Ngan and Kang 1988, Ahmed *et al.* 1990, Tsukahara *et al.* 1991, Khotanzad *et al.* 1992, 1994, Sreenivasan *et al.* 1993, Ye *et al.* 2000, Wang *et al.* 2002, Perng *et al.* 2003, 2007a,b, Tsai and Su 2009) can be applied because the image of the wires in the lower layer would be hidden or shadowed by the wires in the upper layer.

Some other researchers (Sanderson *et al.* 1988, Chia *et al.* 1996, Tian and Tsui 1996) recovered the 3D shape using a photometric method and structured lighting system. However, multiple images are required in this research to determine the surface normal. Kim and Koh (2007) discussed the shadow problem for in-line shape inspection of LEDs using pattern projection techniques. Because of the high ratio of the outside wall to the width of the inside base area, conventional measurement techniques for projecting patterns in off-optical axis easily fail to perceive the entire shape of LEDs and produce noisy results due to the shadow problem. Kim and Koh also presented a sensor system utilising a dual projection system. Using two measurement results acquired from pattern projections switching with different incident angles, shadow-free results can be acquired but this only resolves the shadow problem for the outside wall, not for the hidden or shadowed problem by the wires in the upper layer.

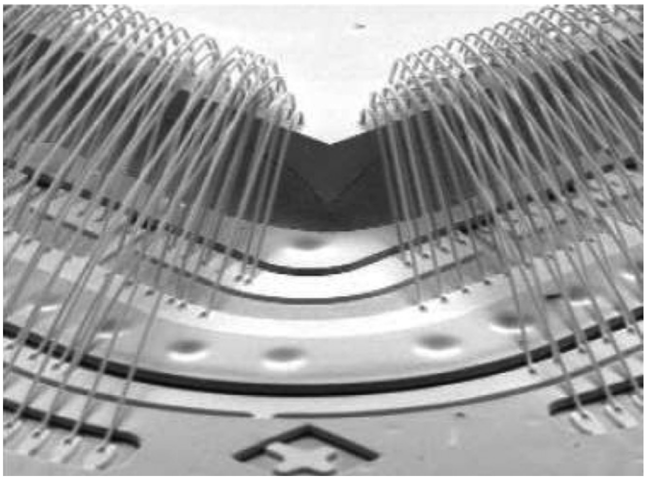


Figure 5. Multi-layered wire bonding (Brunner *et al.* 2004).

Figure 6. Enlarged image of multi-layered wire bonding (Brunner *et al.* 2004).

Lim *et al.* (1992) presented an auto-focusing technique to measure the height and diameter of the bonding ball. Their method can also be used for the inspection of missing bonds and wire loop height measurements. Because a high-magnification microscope was used in their system, only the image of the wires in the focused plane could be captured clearly, while the wires in the other planes were hard to observe or inspect. KAIJO Corporation (2009) used an auto-focusing technique to develop a wire bonding AOI system (WI-110). The KAIJO Corporation claimed that their system could correctly inspect multi-layered wire products. The WI-110 system searches for the bonding ball position on the pad side first and defines it as the starting point. Next, the loop height of the wire is measured from the starting point until the ending point is found, and then converts the loop height of each point in the wire and converts this into the wire track. The auto-focusing technique inspection speed is very slow. The KAIJO machine took 8 seconds to inspect a single wire (WI-110 2009). Since the available AOI machine for the wire bonding inspection is not sufficiently fast, only off-line inspection machines were adopted.

Pacheco *et al*. (2005) presented an advanced time domain reflectometry (TDR) technique to detect the defects in multi-layered wire ICs. Only a laboratory prototype was implemented because of the high cost of this system.

Kulicke & Soffa Industries Inc. (KNS) presented a process program comparator (PPC) technique with their KNet system (KNS 2009). Image verification is not required because such an inspection approach is based only on the bonding sequence and the coordinate value of the ending point of each wire. The major drawback of the PPC method is that the PPC method does not have any actual visual inspection and does not utilise the actual lead position information. Some serious mal-detection (false negative, the wire is bonded in the correct position but is recognised as an incorrect bond) or lost detection (false positive, the wire is bonded onto the wrong lead but is recognised as a correct bonding case) problems were encountered when their system was applied to a product composed of leadframe-based material. Compared with the other substrate-based IC product material fabricated using a mask, the leadframe-based material is fabricated by punching or etching and has the problem of high variation and low accuracy for each lead on it. Although KNS provided a fast and on-line inspection solution for multi-layered wire ICs, their method could only be applied to a product composed of substrate-based material. Until now, no commercial equipment existed that could meet all of the wire bonding position inspection requirements.

We propose a novel method that solves the wire image hidden problem for multi-layered wire ICs and the mal-detection problem for leadframe-based material ICs. The proposed method integrates the image processing and wire bonding simulation techniques to automatically inspect the correctness of wire bonding positions. This approach can check the correctness of the wire bonding position before any actual wire bonding operation is executed. Post-wire-bond image identification is not required because such an inspection approach is based only on the information of the bonding sequence, the coordinate values of both end points of each wire and the base material image. In other words, there is no need to be concerned about whether the image of the wires in the lower layer will be blocked or hidden by the shadow of the wires in the upper layers. Therefore, the proposed approach can be used for inspecting the bonding position of multi-layer wire ICs.

A summary of the previous research, available commercial systems and the proposed method for wire bonding position inspection is given in Table 1.

3. Wire bonding position check

For each production order in an IC packaging foundry the engineer must first set up the bonding program with detailed verification for one bonding machine, which is used as a reference machine (RM). The engineer subsequently duplicates the RM's bonding program into other bonding machines. The bonding machines with the copied bonding program are called waiting verification machines (WVMs). In duplicating the bonding program it is necessary to calibrate the bias of all WVMs. Therefore, the bonding position set up is

Table 1. Summary of the previous research, available commercial systems, and the proposed BPC method for wire bonding position inspection.

Method	Attributes							
	Image verification	Inspection timing	Multi-layered wire inspection	Leadframe-based material inspection	Inspection speed	On/off-line inspection	Affected by complex background	Cost
2D image inspection method (Wang *et al*. 2002)	Yes	Post-bonding	Bad	Good	Fast	On-line	Yes	High
Inspection with structure lighting (Perng *et al*. 2007b)	Yes	Post-bonding	Bad	Good	Fast	On-line	No	High
Auto- focusing (WI-110 2009)	Yes	Post-bonding	Good	Good	Very slow	Off-line	Yes	High
TDR technique (Pacheco *et al*. 2005)	Yes	Post-bonding	Good	Good	Very slow	Off-line	Yes	Highest
PPC method (KNS 2009)	No	Pre-bonding	Good	Bad	Fast	On-line	No	Low
The proposed BPC method	Yes	Pre-bonding	Good	Good	Fast	On-line	No	Low

prone to errors. Verifying and ensuring that the wire bonding positions are the same in every WVM as the RM is a critical procedure.

In modern bonding machines the actual wire bonding operation is triggered according to the coordinate values of the starting point (pad side) and ending point (lead side) of the bonding program. That is, when the coordinate values of the bonding program are set in the correct positions, the actual bonding position of each wire will be bonded correctly. The proposed BPC method utilises this advantage to simulate the actual wire bonding operations for wire bonding position verification. This approach can prevent incorrect bonding before the actual wire bonding process is executed.

The proposed BPC method first captures the image of a single leadframe unit without the IC chip and bonding wire. The BPC method then labels each lead on the image with a unique pseudo code for the later simulation process. The bonding program is obtained from the bonding machine through the SEMI SECS/GEM communication protocol. Each of the [X, Y] coordinate values for the wire bonding positions is obtained by decoding the bonding program. Based on the captured leadframe image and the coordinate values of the wire bonding positions, the BPC method simulates an actual wire bonding operation for the WVM to calculate the end point (lead side) location of each wire and obtains a numbered pseudo code for each corresponding lead. The WVM pseudo code of each lead is compared with the RM to verify whether the wires were bonded correctly.

The proposed BPC method solves the multi-layered wire inspection problem and the mal-detection problem that may occur in other available methods. The entire BPC method is composed of five parts, as illustrated in Figure 7 and described below.

Part 1. Extract the lead information for the bonding position checking

Step 1.1: Capture the leadframe image as $I(l)$.

Step 1.2: Normalise the captured image orientation to align it in a predefined position.

Step 1.3: Binarise $I(l)$ into $I_b(l)$ so that each lead on $I_b(l)$ will be a solid line. A near-bimodal distribution of the grey-level histogram of $I(l)$ will be obtained as shown in Figure 8. The valley-emphasis method (Ng 2004) is used to auto-select an optimal threshold value.

Step 1.4: Label each solid line (lead) on the binary image $I_b(l)$ with a unique pseudo code. The pseudo code starts from 1, as shown in Figure 9(a). All of the pixels of the same solid line are given the same pseudo code. A labelled image $I_c(l)$ will then be derived from the binary image $I_b(l)$. Store the set of pseudo codes in a 2D array $I_c(l)$[x, y], where [x, y] is the coordinate value of each pixel, as shown in Figure 9(b).
Note: a pseudo code set is used for bonding position verification.

Step 1.5: Define the calibration marks in the image.
The calibration mark is used as a reference when a leadframe is moved to the bonding area, a process that may usually cause the leadframe to shift and rotate. Ordinarily, there are four calibration marks, two on the lead side and two on the pad side. Here we only need to define the lead side calibration marks in the image. If we define the upper left corner of the image as the origin $(X, Y) = (0, 0)$ of this image, the coordinates for the two calibration marks in the image can then be determined accordingly, say IL1 (X_{IL1}, Y_{IL1}), IL2 (X_{IL2}, Y_{IL2}) from the left to the right, as shown in Figure 10. In a later

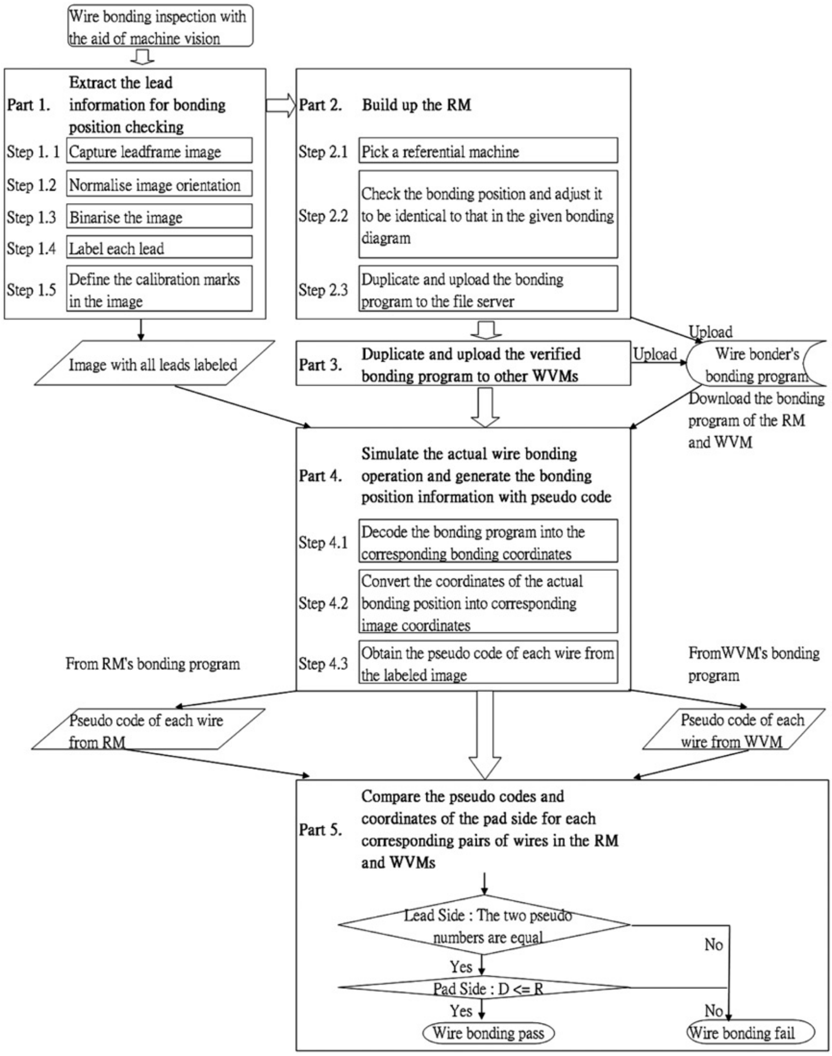


Figure 7. Flow chart of wire bonding position inspection in the proposed BPC method.

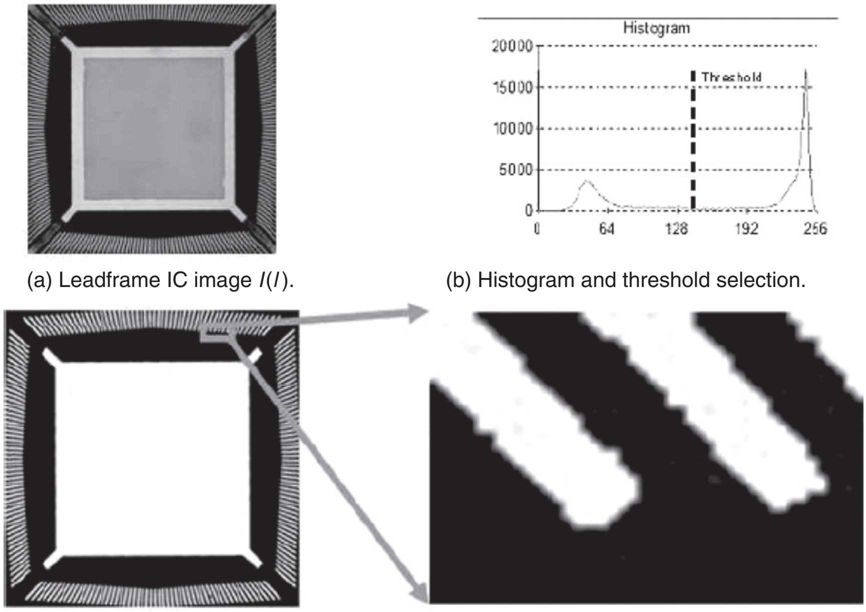
procedure, the coordinates of these calibration marks are used as the basis to convert the coordinates of the actual bonding positions into corresponding image coordinates.

Part 2. Build up the RM

Three sub-steps are executed to build one bonding machine as the RM and upload the bonding program onto the host computer by which the RM was controlled.

Step 2.1: The engineer randomly selects one bonding machine as an RM.

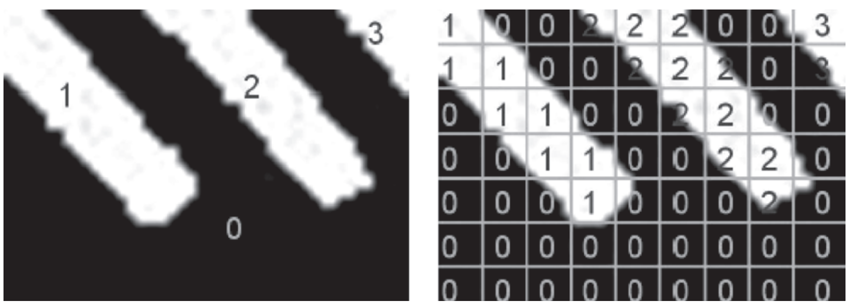
Step 2.2: The engineer checks the bonding positions of the wires bonded using the RM and adjusts them to ensure that they are the same as those in the designed bonding diagram.



(a) Leadframe IC image $I(l)$. (b) Histogram and threshold selection.

(c) Binary image $I_b(l)$. (d) An enlarged sub-image of (c).

Figure 8. Threshold selection for a leadframe IC image.



(a) Labelled image (b) Store the pseudo code in array [x, y].

Figure 9. Binary image $I_b(l)$ labelling.

Step 2.3: The engineer uploads the bonding program from the RM onto the host computer via the SEMI SECS/GEM communication protocol.

Part 3. Duplicate and upload the verified bonding program to other WVMs

The engineer duplicates and uploads the verified RM bonding program to other bonding machines, called WVMs, for mass production. Because of the machine bias, it is inevitable that the wire bonding position set up operation will have errors during duplication. The wire bonding positions bonded by all WVMs must be verified to ensure that they are identical to those bonded by the RM.

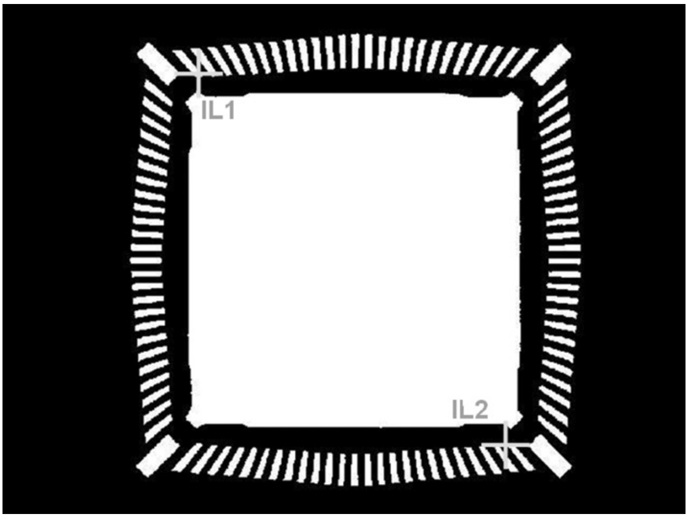


Figure 10. Illustration of the calibration marks in the leadframe image generated from Part 1.

Part 4. Simulate the actual wire bonding operation and generate the wire bonding position information for each wire with pseudo code

The bonding position of each wire is checked using the RM bonding program and the leadframe image. A bonding program contains the following information:

(1) The bonding sequence of each wire and the coordinates of the starting point (pad side) and the ending point (lead side) for each wire.
(2) The calibration mark coordinates on both the leadframe and the IC chip.

The following steps will simulate the actual WVM wire bonding operation to obtain the coordinate values that will be bonded onto which lead.

Step 4.1: Decode the bonding program into the corresponding bonding coordinates. In practice, there are different types of bonding machines in a bonding production line. Each type of bonding machine has its own coordinate-encoding rule. To obtain the actual XY coordinates of the bonding positions on the lead and pad sides of each wire, the uploaded bonding program must be decoded using the original encoding rule. In the case of the RM, the XY coordinates of the end point of each wire (j), $P_l(X_{RM(j)}, Y_{RM(j)})$ on the lead side and $P_c(X_{RM(j)}, Y_{RM(j)})$ on the pad side are recorded and used as the referential coordinates. Similarly, for WVMs, the XY coordinates of the end point of each wire (j), $P'_l(X_{WVM(j)}, Y_{WVM(j)})$ on the lead side and $P'_c(X_{WVM(j)}, Y_{WVM(j)})$ on the pad side are recorded and used as the waiting verification coordinates. The actual XY coordinates of the four calibration marks, two on the lead side and two on the pad side, can also be decoded from the bonding program. The XY coordinates of the two calibration marks on the lead side can be recorded as L1 (X_{L1}, Y_{L1}), L2 (X_{L2}, Y_{L2}) from left to right. The other two calibration marks on the pad side can be recorded as P1 (X_{P1}, Y_{P1}), P2 (X_{P2}, Y_{P2}) from left to right.

Step 4.2: Convert the coordinates of the actual wire bonding positions into the corresponding image coordinates.

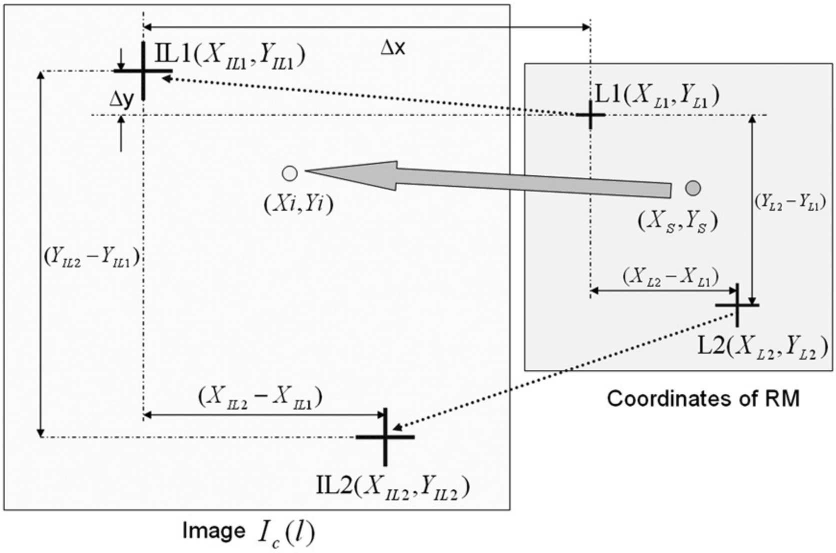


Figure 11. Mapping the end point coordinates of RM wires onto the image $I_c(l)$.

Here, we use the lead side as the first example, as shown in Figure 11. The wire bonding position of each point on the lead side will then be magnified by:

$$\ell x = (X_{\mathrm{IL2}} - X_{\mathrm{IL1}})/(X_{\mathrm{L2}} - X_{\mathrm{L1}}) \tag{1}$$

$$\ell y = (Y_{\mathrm{IL2}} - Y_{\mathrm{IL1}})/(Y_{\mathrm{L2}} - Y_{\mathrm{L1}}). \tag{2}$$

Assuming that there is a wire bonding position with coordinates (Xs, Ys) on the lead side, this position will be mapped onto the image $I_c(l)$ with the coordinates (Xi, Yi) according to Equations (3) and (4) below:

$$Xi = X_{\mathrm{IL1}} + (Xs - X_{\mathrm{L1}}) \times \ell x \tag{3}$$

$$Yi = Y_{\mathrm{IL1}} + (Ys - Y_{\mathrm{L1}}) \times \ell y. \tag{4}$$

Step 4.3: Obtain the pseudo code for each wire from the labelled image.
Based on the end point coordinate (Xi, Yi), the pseudo code of each pixel in the labelled image $I_c(l)$ can be obtained from the 2D array $I_c(l)$ $[Xi, Yi]$. For example, the end point $P_l(X_{RM(j)}, Y_{RM(j)})$ of a wire (j) on the lead side of the RM will be converted into new coordinates using Equation (5) as follows:

$$[Xi, Yi] = \left[\left(X_{\mathrm{IL1}} + \left(X_{RM(j)} - X_{\mathrm{L1}}\right) \times \ell x\right),\ \left(Y_{\mathrm{IL1}} + \left(Y_{RM(j)} - Y_{\mathrm{L1}}\right) \times \ell y\right)\right]. \tag{5}$$

The ending point of wire (j) will have the pseudo code of:

$$I_c(l)\left[\left(X_{\mathrm{IL1}} + \left(X_{RM(j)} - X_{\mathrm{L1}}\right) \times \ell x\right),\ \left(Y_{\mathrm{IL1}} + \left(Y_{RM(j)} - Y_{\mathrm{L1}}\right) \times \ell y\right)\right]. \tag{6}$$

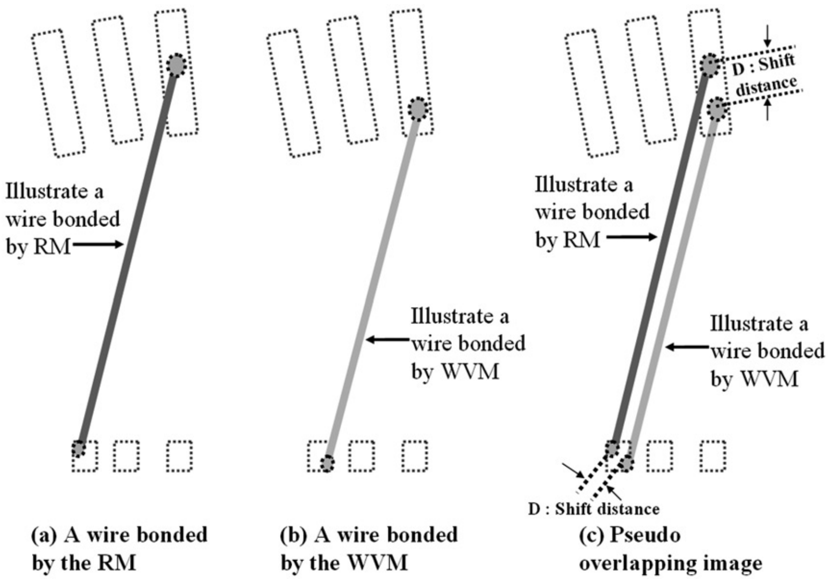


Figure 12. Illustration of the pseudo-overlapping image of two pairs of corresponding wires: (a) designed positions for both end points of a wire to be bonded by the RM; (b) computed positions for both end points of a wire to be bonded by a WVM; and (c) an illustration of the shift distance of the positions of corresponding wires bonded by the two machines.

Part 5. Compare the pseudo codes and coordinates of the pad side for each corresponding pair of wires in the RM and WVMs

IC packaging foundries need several bonding machines (WVMs) to work at the same time. These WVMs have to be checked one by one. Here we will follow the bonding sequence to check the corresponding pair of wires of RM and WVM. On the lead side, we can compare the pseudo codes for a corresponding pair of RM and WVM wires to verify whether the wire bonding positions bonded by the WVMs are correct or not. On the pad side, each point on the IC chip is practically bonded with high accuracy and low variation so that the traditional PPC method can still be applied. The distance (D) between the RM and WVMs coordinates is then calculated. Theoretically, the end point coordinates for a pair of corresponding RM and WVM wires should be equal. For good wire bonding we should have the wire bonding position controlled within a shift distance (D) which should be less than a pre-defined shift tolerance range (R). When the distance is greater than the pre-designed allowable range (R), this wire is marked as an incorrect bond (see Figure 12). Here, R is set equal to the pad pitch. The algorithm for the wire bonding position comparison is given below.

Algorithm. Wire bonding position comparison
Input: the pseudo code of each wire on the lead side and the XY coordinate value for the starting point of every wire on the pad side.
Output: the detected wire with incorrect bonding.
Procedure:
For j = 1 to N **do**/* N is the total number of bonding wires */

Case lead side: /* Check the bonding positions in the lead side ***/**

$$\textbf{If} \begin{pmatrix} I_c(l)\left[\left(X_{\mathrm{IL}1} + \left(X_{RM(j)} - X_{\mathrm{L}1}\right) \times \ell\mathrm{x}\right), \left(Y_{\mathrm{IL}1} + \left(Y_{RM(j)} - Y_{\mathrm{L}1}\right) \times \ell\mathrm{y}\right)\right] \\ -I_c(l)\left[\left(X_{\mathrm{IL}1} + \left(X_{WVM(j)} - X_{\mathrm{L}1}\right) \times \ell\mathrm{x}\right), \left(Y_{\mathrm{IL}1} + \left(Y_{WVM(j)} - Y_{\mathrm{L}1}\right) \times \ell\mathrm{y}\right)\right] \end{pmatrix} = 0$$

/* Check whether the pseudo code of $P_l(X_{RM(j)}, Y_{RM(j)})$ in reference machine is equal to the pseudo code of $P_l'(X_{WVM(j)}, Y_{WVM(j)})$ in the waiting verification machine.

All pixels of the same lead have the same pseudo code. The pixels of different leads have different pseudo code. If the pseudo codes for the end points of a pair of wires in the corresponding RM and WVM are equal, we can locate the corresponding wires in the same numbered lead. */

Then the wire bonding has passed
Else the wire bonding has failed
End if
End case

Case pad side: /* Check the bonding positions in the pad side ***/**
If (D $\leq$ R)
Then the wire bonding has passed
Else the wire bonding has failed

/* $\mathrm{D} = \sqrt{\left(X_{RM(j)} - X_{WVM(j)}\right)^2 + \left(Y_{RM(j)} - Y_{WVM(j)}\right)^2}$;

R = Shift tolerance range */

End if
End case
End for
End procedure

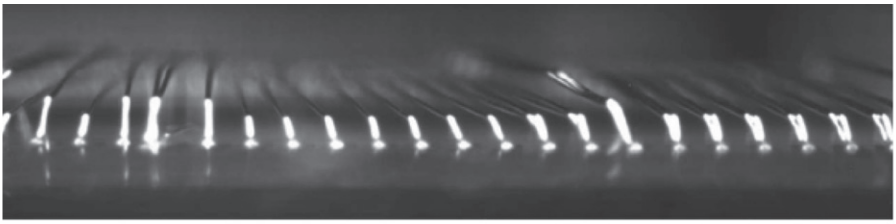
4. Experimentation and result analysis

The major factors considered in the wire bonding position inspection in IC packaging foundries are: (a) the mal-detection rate and lost detection rate; particularly for multi-layered wire IC inspection; (b) the reliability of the applied method in a mass production environment; and (c) the inspection speed. These factors are used as the performance indicators for examining the advantages/disadvantages of the 2D image inspection method (Perng *et al.* 2007b), the PPC method and the proposed BPC method.

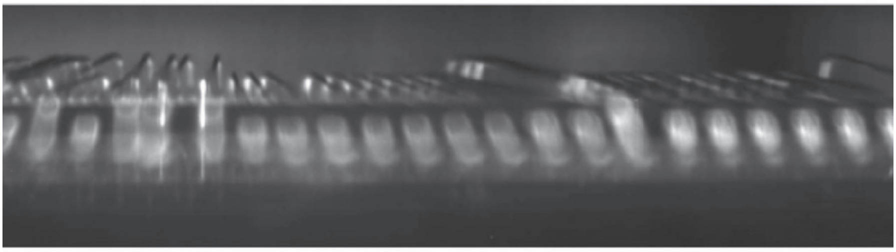
In Section 4.1, we use a multi-layered wire IC chip to compare the inspection performance of the 2D image inspection method, the PPC method and the proposed BPC method by employing the mal-detection rate and lost detection rate. In Section 4.2, we discuss the feasibility of the proposed BPC method when applied in a mass production environment with 145 bonding machines. In Section 4.3, we discuss the inspection speed of the proposed BPC method and a comparison with two available inspection methods.

4.1 *Experimentation related to inspection of multi-layered wire IC with wrong bonding*

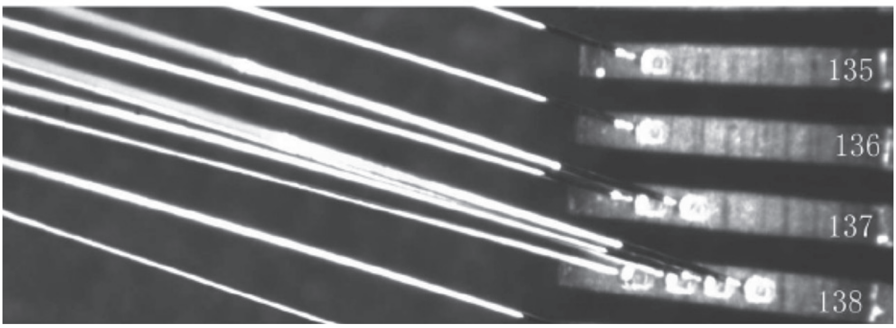
The first inspection experimentation involves a multi-layered wire IC chip with 216 leads. The base material of this IC chip is a Cu leadframe. The lead width, lead length, lead pitch, pad width and pad pitch of this IC chip, respectively, are 4, 26, 3.7, 2.24 and 0.2 mils. There are a total of 312 bonding wires including 41 ground bonds. The mal-detection rate



(a) Image taken by focusing on the lead side.



(b) Image taken by focusing on the pad side.



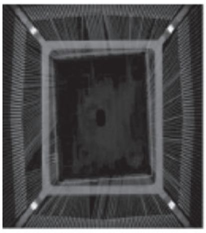
(c) Image taken from the top side.

Figure 13. Enlarged partial images of a sample IC used in experimentation (Section 4.1).

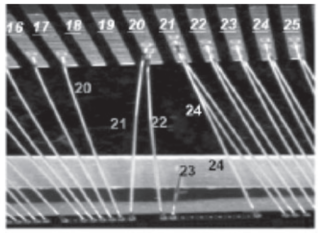
and lost detection rate are used as the performance indicators for the 2D image inspection method (Perng *et al.* 2007b), the PPC method and the proposed BPC method comparison.

Figure 13 illustrates three partially enlarged images of this sample IC. Figures 13(a) and 13(b) show that there are multi-layered wires on this IC. From Figure 13(c), it is obvious that the lead numbered 138 has four bonding points. Only three wires extending from the lead numbered 138 can be seen because one wire is hidden by the wires in the upper layer. This situation will cause the mal-detection problem when the 2D image inspection method is applied even though the bond is correct.

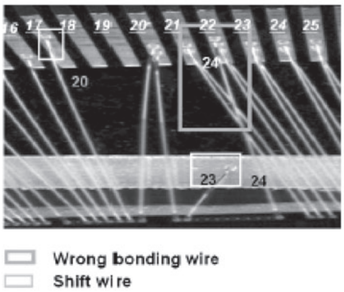
We randomly selected three wires (wires numbered 16, 20, and 23 in Figure 14(c) and Table 2) and adjust the wire bonding positions manually to let them shift away from the original wire bonding positions in the WVM, but still retain them on the same lead (i.e., to ensure correct bonding). Similarly, we randomly selected the other wire (wire numbered 24 in Figure 14(c) and Table 2) and adjusted its wire bonding position manually to allow it to shift away from the original bonding lead to cause an incorrect bond in the WVM. Initially, the shift tolerance range R of the lead side is set equal to the lead pitch (3.7 mils).



(a) Full image of an IC after bonding.

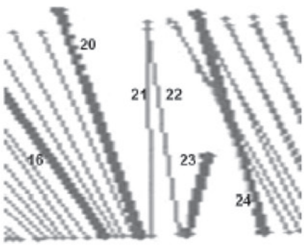


(b) Enlarged part of (a). Correctness bonding from RM.

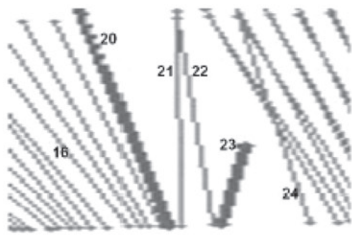


(c) Wire numbered 24 was bonded to the wrong lead (from lead 21 to lead 22) Two wires numbered 17 and 23 were bonded with shift but still in the same lead.

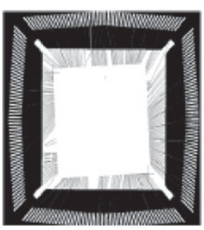
(d) PPC method with R = 3.7 mils.



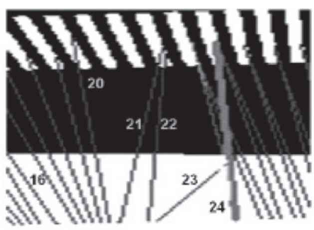
(e) Enlarged part od (d). Wires numbered 16, 20, 23 and 24 were verified as incorrectly bonded wires by PPC method with R = 3.7 mils.



(f) PPC method with R = 9.7 mils. wires numbered 20 and 23 were verified as incorrectly bonded wires.



(g) BPC method.



(h) Enlarged part of (g). Only the wire numbered 24 was verified as an incorrectly bonded wire.

Figure 14. Experimental results from inspecting a sample multi-layered wire IC.

Table 2. Experimental results of applying PPC method to a multi-layered wire IC with one man-made wrong bonding wire.

Wire number	End point coordinates bonded by RM		End point coordinates bonded by WVM		Shift distance (D)	Bonding in the correct lead	PPC result for R = 3.7	PPC result for R = 11.99
	X	Y	X	Y				
15	283.61	46.89	284.77	46.20	1.35	Y	P	P
16	292.84	49.91	295.77	53.37	4.53	Y	F (Mal-detection)	P
17	300.48	49.48	301.76	48.95	1.38	Y	P	P
18	307.85	48.97	309.15	48.19	1.52	Y	P	P
19	315.29	48.17	316.54	48.07	1.25	Y	P	P
20	322.88	47.95	321.24	36.08	11.99	Y	F (Mal-detection)	P
21	344.22	42.71	345.5	42.14	1.4	Y	P	P
22	344.95	46.52	346.17	46.02	1.32	Y	P	P
23	351.97	117.4	362.4	116.14	10.51	Y	F (Mal-detection)	P
24	351.01	38.1	359.45	37.72	8.45	N	F	P (Lost detection)
25	351.71	42.19	352.89	41.69	1.29	Y	P	P
26	352.32	46	353.57	45.48	1.35	Y	P	P

Note: The lead length is 26 mils. This means that the maximum possible shift distance of the wire is 26 mils and the bonded wire will still be on the targeted lead. In the last two columns on the right-hand side, 'P' indicates that the system check has passed and 'F' denotes that the system check has failed. The lead pitch is 3.7 mils, R is set to be 3.7 mils first and there are three mal-detected wires. When R is set to 11.99 mils, the mal-detection rate will be reduced. However, releasing R will also cause the lost detection problem.

We then repeat the wire bonding position inspection steps as described in Section 3, by increasing the value of R by 2 mils each time when the PPC method is applied until no mal-detection can be found (see Table 3).

The experimental results are recorded in Table 2, Table 3 and Figure 15. A part of the image is shown in Figure 14. Figure 14(a) shows the full image of the chip. Figure 14(b) is the partially enlarged image of the IC with the correct bonding wire in the RM. Figure 14(c) depicts the partially enlarged image of the IC with an incorrectly bonded wire in the WVM. Figures 14(d), 14(e), and 14(f) illustrate the results from applying the PPC method. The slim lines in Figures 14(e) and 14(f) denote that these wires were verified as correctly bonded wires using the PPC method. The fat lines in Figures 14(e) (wires numbered 16, 20, 23, and 24) and 14(f) (wires numbered 20 and 23), respectively, represent the fact that they are incorrectly bonded wires. These wires were verified using the PPC method. Figures 14(g) and 14(h) are the results from applying the BPC method. In Figure 14(h), the slim lines express the fact that the wires were verified as being correctly bonded using the BPC method. The fat line (wire numbered 24) represents the fact that it is an incorrectly bonded wire that was verified using the BPC method.

With regard to Table 2 and Figure 15(a), when the PPC method was applied, mal-detection occurred in the lead side. Comparing Figure 14(c) with Figure 14(e), we can see that even though the two wires numbered 20 and 23 shifted away from the designed wire bonding position, they were still bonded onto the correct lead. The PPC method verified it as being bonded incorrectly when R is 3.7 mils. The mal-detection problem could be reduced if R could be considered equal to the maximum possible D. However, releasing R might cause the lost detection problem. For example, when R was increased to 9.7 mils (Figure 14(f) and Table 3), wire number 16 is not mal-detected any more. However, the lost detection case occurred for wire number 24. Because the PPC method checks the correctness of wire bonding positions only on the basis of the shift distance, that is, since it does not have the actual information on the lead position, not all incorrect bonds can be detected. Some correct bonds may even be incorrectly detected as defective.

On the other hand, in Figures 14(g) and 14(h), as a result of applying the proposed BPC method, no mal-detection or lost detection cases occurred. That is, despite the shade from the wires in the upper layer hiding the wires in the lower layer, as Figure 13(c) shows, the proposed BPC method can successfully be applied for multi-layered wire IC inspection. When the BPC method was applied, because the actual information on the lead positions was utilised, no mal-detection or lost detection occurred. All of the bonding positions for the wires can be correctly verified.

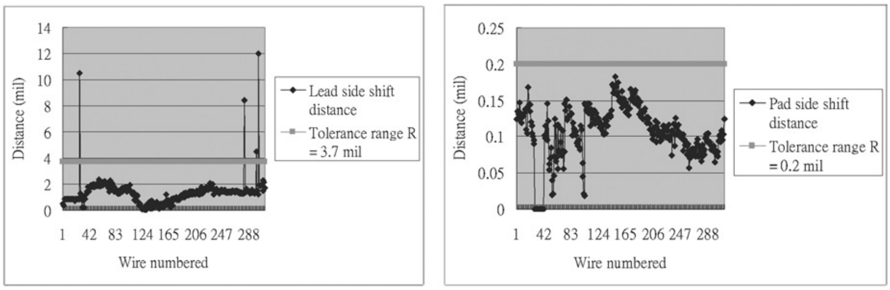
On the lead side inspection, both PPC and BPC use the same algorithm. The shift tolerance range R of the pad side is set equal to the pad pitch (0.2 mils). Figure 15(b) showed the pad side comparison result and all wires were identified as correct bonding ($D < 0.2$ mil). No mal-detection or lost detection in the pad side inspection was encountered.

4.2 *BPC method application in a mass production environment*

To evaluate the feasibility of the proposed BPC method in a mass production environment, we implemented the proposed BPC method and the PPC method to a production line of 145 bonding machines. There were three different models – UTC370, MaxumPlus, and MaxumUltra, of the 145 bonding machines. One machine of these three

Table 3. Experimental results from a multi-layered wire IC inspection with one man-made incorrect bonding wire. The 2D image inspection method, the PPC method and the proposed BPC method are compared based on the mal-detection rate and lost detection rate by increasing the shift tolerance range 2 mils each time. The initial shift tolerance range is set equal to the lead pitch (3.7 mils).

	Tolerance range											
	3.7 mil		5.7 mil		7.7 mil		9.7 mil		11.7 mil		13.7 mil	
Inspection method	Mal-detection	Lost detection	Mal-detection	Lost detection	Mal-detection	Lost detection	Mal-detection	Lost detection	Mal-detection	Lost detection	Mal-detection	Lost detection
2D image inspection method	14	0	14	0	14	0	14	0	14	0	14	0
PPC method	3	0	2	0	2	0	2	1	1	1	0	1
BPC method	0	0	0	0	0	0	0	0	0	0	0	0



(a) The shift distances of lead side. (b) The shift distances of pad side.

Figure 15. The shift distance between WVM and RM of each wire in lead side and pad side.

models was chosen randomly as an RM for that model. The other machines were used as WVMs. In this experiment both the PPC and proposed BPC methods were executed.

There are seven different lead counts for the QFP (Quad Flat Package) product to be inspected in the production line, as given in Table 4. Each of these QFP products has several leadframe layouts. Furthermore, even the same leadframe layout for different QFP products may have several different devices (different bonding or different chips). In this experiment, we randomly selected one device from each of the same lead count products. The mal-detection rate is the performance indicator. The results from applying the proposed BPC and PPC methods to a mass production environment are listed in Table 4.

Table 4 shows that the PPC method will result in mal-detection. The mal-detection rate is higher than 66%, particularly for the products with a ground bond. That is because the allowable shift tolerance range in the ground bond is equal to the entire ground bond area (see Figure 3). Conversely, there is no mal-detection in the proposed BPC method.

4.3 *Inspection speed comparison*

The proposed BPC method was implemented using Visual Basic and MIL 6.0. The computer hardware was a PC powered by an Intel Celeron 1.6 GHz CPU. Only Parts 4 and 5 of Section 3 were included in the inspection speed computation. Although Part 1 requires extra manual effort to process the image, it must be executed only once for the same device (same bonding and same chip). All of the inspection methods (Perng *et al.* 2007b, WI-110 2009), except the PPC method, will need the same set up time for a new machine. Parts 2 and 3 are standard operations for the wire bonding process. It is not necessary to include these operations in the inspection time computation.

The proposed BPC method requires only 3.4944 seconds to check an IC with 312 wires. In other words, less than 0.0112 seconds are required for checking a single wire. For those methods that include image processing operations, the inspection speed is much slower than the proposed BPC method. Because the PPC method includes no image processing operation, its inspection speed is faster than the proposed BPC method. A brief comparison of the BPC method with other inspection methods is presented in Table 5.

At present, the fastest commercial bonding machine requires about 0.06 seconds to bond a single wire (KNS 2007). The proposed BPC method for a multi-layered wire IC is fast enough to work synchronously with the wire bonding production line.

Table 4. Experimental results from the application of the proposed BPC method and the PPC method in a mass production environment. The performance indicator is focused upon the mal-detection rate.

Type group					Inspection method					
					PPC method			BPC method		
Lead count	Wire count	Machine QTY	Machine type	Ground bond	Mal-detection rate	Max # of mal-detected wire	Average of mal-detected wire	Mal-detection rate	Max # of mal-detected wire	Average of mal-detected wire
64	116	4	UTC370	Y	75%	8	2.75	0	0	0
100	100	54	UTC370	Y	94.44%	12	5.48	0	0	0
128	131	7	UTC370	N	42.86%	2	0.57	0	0	0
144	144	11	MaxumPlus	N	9.09%	20	1.82	0	0	0
176	183	20	MaxumPlus	N	10%	42	2.6	0	0	0
216	312	46	MaxumUltra	Y	95.65%	76	9.82	0	0	0
256	357	3	MaxumUltra	Y	66.67%	7	4.33	0	0	0

Table 5. Comparison result of the speed of different wire bonding position check methods.

Algorithm	Speed (second per wire)
PPC method	0.008
The proposed BPC method	0.0112
The fastest commercial bonding machine (KNS 2007)	0.06
2D image inspection method (Perng *et al*. 2007b)	0.08
Auto-focusing method (WI-110 2009)	8*

Note: *KAIJO WI-110 system searches for the bonding ball position on the pad side first and defines it as the starting point (2 sec/point). Next, the loop height of the wire is measured from the starting point until the ending point is found (6 sec/point) and then the loop height of each point in the wire will be converted into the wire track. That is, KAIJO machine will take 8 seconds to inspect a single wire.

5. Conclusions and suggestions for further research

5.1 *Conclusions*

A novel BPC method that can automatically inspect the correctness of wire bonding positions was proposed and implemented. The proposed BPC method was implemented on several different bonding machine models such as the MaxumPlus, MaxumUltra, and UTC370. It is the first system that can automatically check the correctness of wire bonding positions for multi-layered wire ICs. The experimental results showed that the proposed BPC method is very efficient and effective. It can completely solve the mal-detection and lost detection problems that may occur in other available wire bonding position check methods. The proposed BPC method is better for a ground bond product than other available methods.

5.2 *Further studies*

Some wire bonding defects such as broken wire, shorted wire, or sagged wire might happen during the wire bonding process. Because the shade from the wires in the upper layer may hide the wires in the lower layer, the defects in multi-layered ICs are difficult to inspect using a 2D image processing approach. It is worthwhile to pursue an effective and efficient method for inspecting wire bonding defects in multi-layered ICs.

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References

Ahmed, M., *et al.*, 1990. INSPAD: a system for automatic bond pad inspection. *IEEE Transactions on Semiconductor Manufacturing*, 3 (3), 145–147.

ASTM, 1999. *Standard practice for visual inspection of semiconductor lead-bonding wire*. West Conshohocken, PA: ASTM International.

Ayoub, G.T., 2006. Inspecting post wire-bond interconnects. *Advanced Packaging* magazine [online]. Available from: http://ap.pennnet.com/Articles/Article_Display.cfm?Section=ARTCL&ARTICLE_ID=252780&VERSION_NUM=2&p=36 [Accessed 1 March 2009].

Brunner, J., Qin, I.W., and Chylak, B., 2004. Advanced wire bond looping technology for emerging packages [online]. Kulicke & Soffa Industries Inc. Available from: http://www.kns.com/uploadfiles/dgallery/0008.pdf [Accessed 1 march 2009].

Chia, T.L., Chen, Z., and Yueh, C.J., 1996. Curved surface reconstruction using a simple structured light method. *In*: *Proceedings of the* 13*th IEEE international conference on pattern recognition*, 25–30 August 1996, Vienna, Austria, 844–848.

Imagen Inc., 2009. Printed circuit board inspection [online]. Available from: http://www.imagen-inc.com [Accessed 1 March 2009].

KAIJO Corporation, 2009. Wire bonding AOI System [online]. Available from: http://www.kaijo.co.jp [Accessed 1 March 2009].

Khotanzad, A., Banerjee, H., and Srinath, M.D., 1992. A vision system for inspection of ball bonds in integrated circuits. *In*: *Proceedings of the IEEE workshop on applications of computer vision*, 30 November– 2 December, Palm Springs, CA, 290–297.

Khotanzad, A., Banerjee, H., and Srinath, M.D., 1994. A vision system for inspection of ball bonds and 2-D profile of bonding wires in integrated circuits. *IEEE Transactions on Semiconductor Manufacturing*, 7 (4), 413–42.

Kim, M.Y. and Koh, K.-I., 2007. Shadow-free moire interferometer with dual projection for in-line inspection of light emitting diodes. *International Journal of Optomechatronics*, 1 (4), 404–424.

KNS, 2007. *Maxum ultra datasheet* [online]. Kulicke & Soffa Industries Inc. Available from: http://www.kns.com/UPLOADFILES/DGALLERY/WB2.PDF [Accessed 1 March 2009].

KNS, 2009. *Bonder connectivity* [online]. Kulicke & Soffa Industries Inc. Available from: http://www.kns.com/KNS07/Templates/showpage.asp?DBID=1&LNGID=1&TMID=87&FID=507&PID=1312 [Accessed 1 March 2009].

Lim, H.O., Zhang, W., and Koh, L.M., 1992. Automated visual inspection for IC wire-bond using auto-focusing technique. *In*: *Proceedings of the IEEE/CHMT international electronics manufacturing technology symposium*, 4–6 October 1993, Santa Clara, CA, USA, 31–36.

Machine Vision Products Inc., 2009. SMT and Semicon AOI solution [online]. Available from: http://www.visionpro.com [Accessed 1 March 2009].

Ng, H.F., 2004. Automatic thresholding for defect detection. *In*: *Proceedings of the third IEEE international conference on image and graphics*, 18–20 December 2004, Hong Kong, China, 532–535.

Ngan, K.N. and Kang, S.B., 1988. automated inspection of IC bonding wires using Hough transform. *In*: *Proceedings of* 14*th conference of industrial electronics society*, *vol*. 4, 24–28 October 1988, Hyatt Regency, Singapore, 938–942.

Pacheco, M., *et al.*, 2005. Advanced fault isolation and failure analysis techniques for future package technologies. *Intel Technology Journal*, 9 (4), 337–352.

Perng, D.B., Chou, C.C., and Lee, S.M., 2003. A new wire bonding inspection system by machine vision. *In*: *Proceedings of* 17th *international conference of production research*, 3–7 August 2003, Blacksburg, Virginia, USA.

Perng, D.B., Chou, C.C., and Lee, S.M., 2007a. Design and development of a new machine vision wire bonding inspection system. *The International Journal of Advanced Manufacturing Technology*, 34 (3–4), 323–334.

Perng, D.B., Chou, C.C., and Lee, S.M., 2007b. Illumination system for wire bonding inspection. *Applied Optics*, 46 (6), 845–854.

Sanderson, A.C., Weiss, L.E., and Nayar, S.K., 1988. Structured highlight inspection of specular surfaces. *IEEE Transactions on Pattern Analysis and Machine Intelligence*, 10 (1), 44–55.

Sreenivasan, K.K., Srinath, M.D., and Khotanzad, A., 1993. Automated vision system for inspection of IC pads and bonds. *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, 16 (3), 333–338.

Tian, Y.L. and Tsui, H.T., (1996). 3D shape recovery from two-color image sequences using a genetic algorithm. *In*: *Proceedings of the* 13th *international conference on pattern recognition*, vol. 4, 25–29 August 1996, Vienna, Austria, 674–678.

Tsai, D.M. and Su, Y.J., 2009. Non-referential, self-compared shape defect inspection for bond pads with deformed shapes. *International Journal of Production Research*, 47 (5), 1225–1244.

Tsukahara, H., Nakashima, M., and Sugawara T., (1991). Automated visual inspection system for IC bonding wires using morphological processing. In: *Proceedings of SPIE*, vol. 1384, 5 November 1990, Boston, MA, USA, 15–26.

Wang, M.J., Wu, W.Y., and Hsu, C.C., 2002. Automated post bonding inspection by using machine vision techniques. *International Journal of Production Research*, 40 (12), 2835–2848.

WI-110, 2009. The specification of post wire-bond inspection machine [online]. Sanlien Technology Corp. Available from: http://www.sanlien.com.tw/web/homepage.nsf/foundationview/B2A893A7D1C934794825718C0011F969 [Accessed 1 March 2009].

Ye, Q.Z., Ong, S.H., and Han, X., 2000. A stereo vision system for the inspection of IC bonding wires. *International Journal of Imaging System Technology*, 11 (4), 254–262.