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Muh-Cherng Wu [a], Chang-Fu Shih [a] & Chen-Fu Chen [a]

[a] Department of Industrial Engineering and Management, National Chiao Tung University, 1001 Dah-Shei Road, Hsin-Chu City, Taiwan (ROC)

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Muh-Cherng Wu*, Chang-Fu Shih and Chen-Fu Chen

Department of Industrial Engineering and Management, National Chiao Tung University, 1001 Dah-Shei Road, Hsin-Chu City, Taiwan (ROC)

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This paper proposes the proposition that the fab ceiling height may become a bottleneck for throughput in a large-scale semiconductor fab. To justify the proposition, we propose a systematic approach for the design of the fab ceiling height. In this approach, we develop a queuing network model to evaluate the cycle time performance of a fab design under a target throughput. This queuing network model is adapted from Connor *et al*. [1996. A queueing network model for semiconductor manufacturing. *IEEE Transactions on Semiconductor Manufacturing*, 9 (3), 412–427] by additionally treating the transportation facilities as finite-capacity resources. Numerical experiments were carried out. The results indicate that a large-scale fab with an inappropriate ceiling height may limit the installation of transportation capacity, which, in turn, limits the utilisation of tool capacity, and thus lowers the fab throughput that can be achieved.

Keywords: production management; semiconductor manufacture

1. Introduction

Semiconductor manufacturing is capital intensive. A fab (i.e. a semiconductor factory) for manufacturing 12 inch wafers may cost about 2–3 billion dollars, of which equipment expenditure accounts for about 75%. Therefore, maintaining the equipment at a high utilisation is very important. One may propose to obtain high equipment utilisation by building the fab as large as possible, rather than building multiple small fabs. The rationale behind this is that consolidating multiple functionally identical workstations into one tends to increase equipment utilisation, due to the effect of capacity pooling.

When constructing a new large-scale fab, most companies adopt a *space-ahead* strategy. That is, the whole space required for the large-scale fab is built in advance and equipment is gradually moved in over time based on market demand. The space-ahead strategy arises due to two concerns. First, the relative cost of equipment is much higher than fab space. Second, the lead time for acquisition of fab space is much longer than that of equipment.

Compared with a small fab, the transportation distance for a large-scale fab would be longer due to the requirement of a larger fab space. As a result, the transportation system for material handling may unexpectedly become the bottleneck for a large-scale fab. One idea for solving this problem is to increase the number of transportation tracks, which

*Corresponding author. Email: mcwu@mail.nctu.edu.tw

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are usually installed overhead in fabs. However, such an installation might not be feasible due to the limit of the fab ceiling height, which was determined in the early stage of fab construction. An appropriate design for the fab ceiling height might thus be very important.

The issue concerning the fab ceiling height limit has not been raised in the literature. In a small fab, such an issue would not arise because the transportation distance is relatively short, and transportation would not be the bottleneck. For a large-scale fab, running at an early stage (i.e. equipment capacity not fully installed), this issue would not arise either because the number of jobs transported in the fab would be relatively small. For a large-scale fab running at a mature stage (i.e. equipment capacity fully installed), the transportation system may unexpectedly become the bottleneck.

This paper proposes the proposition that the fab ceiling height may become a bottleneck for throughput in a large-scale fab. To do so, we propose a systematic approach for the design of the fab ceiling height. In this approach, we use a queuing network model to evaluate the cycle time performance for a fab design under a target throughput. This queuing network model is adapted from Connors *et al.* (1996) by additionally treating the transportation facilities as finite-capacity resources. Numerical experiments are carried out to support the proposition.

The remainder of this paper is organised as follows. Section 2 reviews the relative literature, including tool planning, transportation design and facility layout for fabs. Section 3 describes the queuing network model. Section 4 presents the systematic approach for the design of the fab ceiling height. Numerical experiments are presented in Section 5 and concluding remarks in Section 6.

2. Literature review

Building a new semiconductor fab involves a sequence of decisions: tool planning, facility layout, and automatic material handling system (AMHS) design and management. Prior studies have established significant milestones, yet the design of the fab ceiling height has rarely been considered. An analysis of prior studies is presented below.

The decision for tool planning is to determine the optimal number of tools (i.e. machines) for a fab with a target performance. Some studies have modeled this decision as an integer program (Swaminathan 2000, Hood *et al.* 2003). Others have used a queuing network model as a fab performance evaluator in order to obtain an optimal tool portfolio (Connors *et al.* 1996, Wu *et al.* 2005).

Two survey papers have been published (Gaurav and Sunderesh 2006, Montoya-Torres 2006) on semiconductor facility layout and AMHS design/management. One decision for the facility layout addresses how to design a fab configuration (Peters and Yang 1997, Pillai *et al.* 1999). The other addresses how to cluster tools into groups and determine an optimal placement for each tool group (Geiger *et al.* 1997, Meyersdorf and Taghizadeh 1998, Hseih and Hung 2004).

The decisions for AMHS design involve the layout of transportation networks (Mackulak and Savory 2001, Ting and Tanchoco 2001), determining the number of vehicles (Egbelu 1987, Talbot 2003), and determining the methods for connecting transport (Lin *et al.* 2003). In contrast, AMHS management is concerned with traffic control issues, such as the dispatching priority of vehicles (Kuo and Huang 2006),

the traffic zone control strategy (Wang and Lin 2004), and the determination of efficient transportation paths for vehicles (Jang *et al.* 2001).

In contrast to prior studies, we focus on the design of the fab ceiling height; that is, how many layers of transportation networks would be required for a large-scale fab. The greater the number of transportation layers, the higher is the required fab ceiling height.

3. Queuing network model

The queuing network is an analytic method that can be used to model a factory and evaluate its performance. Much literature on the development of the queuing network model for a semiconductor fab has been published (Nazzal and Mcginnis 2007, Shanthikumar *et al.* 2007). In this research, we propose a queuing network model by adapting that developed by Connors *et al.* (1996).

In a queuing network, a type of *workstation* is modeled as a *queue*, where a workstation denotes a group of functionally identical machines. A job to be processed by a particular workstation is taken to be an *entity* arriving at the queue that models the workstation. The greater the job arrival rate to a queue, the higher is the utilisation of the queue, and the longer is the job's cycle time to pass through the queue. A semiconductor fab, comprising a group of workstations, is a network of queues. With a job reentry characteristic, a job in a fab may visit a workstation multiple times. The cycle time for a job to pass through a fab can be obtained by adding all the cycle times of its visiting queues.

Taking the queuing network developed by Connors *et al.* (1996) as a performance evaluation system for a fab, its input/output relationship can be described as

$$CT = f(Th, PX, MX).$$

The output of the system is CT (the average cycle time for a job to pass through the fab). The input involves three components: Th (throughput of the fab), PX (product mix), and MX (machine mix). The throughput (Th) denotes the number of jobs produced by the fab monthly. The product mix (PX) denotes the relative percentage of each type of product produced. The machine mix (MX) denotes the number of tools for each tool type. For a particular set of MX and PX, the larger Th is, the larger CT is; their relationship is called a *throughput–CT curve* and is shown in Figure 1. The throughput curve may vary under different sets of MX and PX.

In the queuing network model (Connors *et al.* 1996), it is implicitly assumed that the transportation capacity is infinite; as a result, the transportation time between any two workstations is zero. We adapted their queuing network model by taking transportation

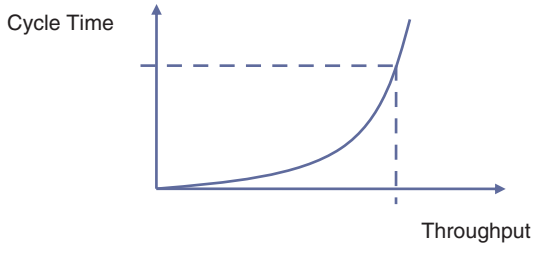

Figure 1. Relationship between cycle time and throughput.

facilities as finite-capacity resources. The greater is the traffic rate, the greater is the possibility of having a traffic jam, and the longer is the *CT*. That is, the input/output relationship of our queuing network model can be described as

$$CT = f(Th, PX, MX, Traffic),$$

where *Traffic* denotes the transportation capacity installed in the fab.

The modeling of *Traffic* is done by taking a *finite* length of transportation track as a queue. Such modeling requires an explicit description of the fab layout. In this research, we assume the fab layout is a *spine* configuration. As shown in Figure 2, the main transportation system is located in the centre; and several bays are located on the two sides. A bay is a space that accommodates several types of workstation. The main transportation system, designed to be *two-way* eligible for traffic, is used to transport jobs among different bays. In each bay, a local transportation system, designed to be *one-way* eligible for traffic, is used to transport jobs within the bay.

In Figure 3, there are several nodes in the transportation layout. A node represents either a station (e.g., node *s1* in *Bay_1*) for loading a job from/to a workstation in a bay, or a turning point (e.g., node *t1* in *Bay_1*) on transportation paths. A transportation path

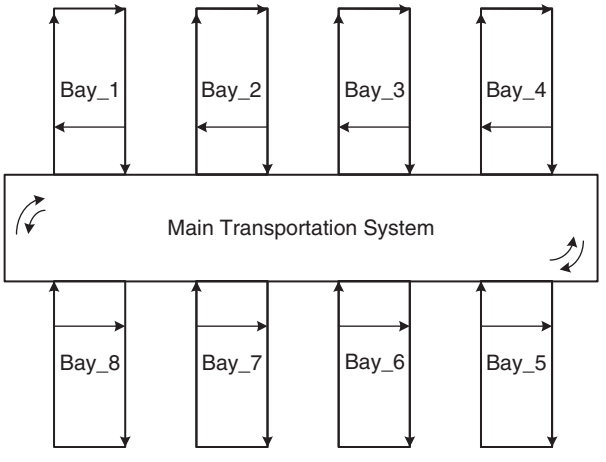

Figure 2. Spine configuration of a semiconductor fab.

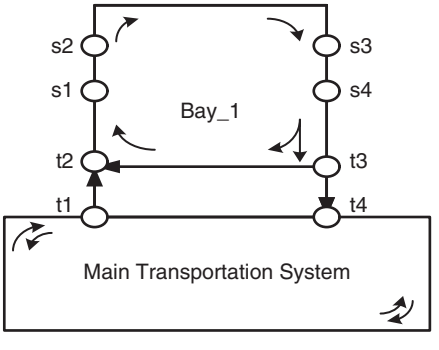

Figure 3. Main transportation is two-way and bay transportation is one-way.

between any two consecutive nodes (also called a *transportation segment*) is modeled as a queue. The traffic rate over a transportation segment is modeled as the arrival rate of the queue. The traffic rates in different transportation segments may be different, due to varying traffic requirements among different bays. By inclusion of queues for modeling transportation segments, we create a larger queuing network than that reported previously (Connors *et al*. 1996).

4. Design of the fab ceiling height

Traditionally, each transportation path in a fab layout is a *single-layer* design. One way to increase the transportation capacity is by changing a single-layer into a *multiple-layer* transportation system. The more transportation layers there are, the greater the transportation capacity, and the higher the fab ceiling requirement.

As already stated, we have proposed a queuing network model, $CT = f(Th, PX, MX, Traffic)$. Based on this model, we have developed an approach to design the ceiling height for a fab. Consider such a fab design problem, where Th_0 (target throughput), PX_0 (product mix) and a target CT_0 (average cycle time) are given, then we need to determine MX (the machine mix or the required number of tools for each tool type) and *Traffic* (the required number of layers for each transportation path).

To describe the fab design approach, we define $M = (m_1, \ldots, m_k)$ as a particular MX, where m_i denotes the number of tools for tool type i, and define $T_r = (r_1, \ldots, r_q)$ as a particular *Traffic*, where r_j denotes the number of layers for transportation path j. We assume that all transportation paths are equipped with the same number of layers, that is $r_i = r_j$ for $1 \le i,\ j \le q$. For example, $T_r = (2, \ldots, 2)$ denotes a two-layer transportation system.

This assumption is based on two rationales. First, given a ceiling height eligible for installing a two-layer transportation system, practitioners would prefer to equip *each* transportation path with two layers—in a one-stop project. Evolutionally adding the number of transportation paths might seriously interrupt production and is not encouraged. Secondly, the cost of the transportation facility is much less than that of the machine. Therefore, if the fab ceiling is high enough, increasing the transportation capacity by a *whole* layer might not cost much, compared with the benefit that may arise due to greater machine utilisation. For an advanced 12 inch wafer fab, the total expenditure is about 3.6 billion dollars. The expenditure for adding one more transportation layer (including hardware and software) is around 60 million dollars, about 1.6% of the original total expenditure. That is, it would be beneficial to add one more transportation layer if such a facility enhancement can increase throughput by more than 1.6%.

The fab design approach is described by a procedure called *Fab_Ceiling_Design*.

Procedure *Fab_Ceiling_Designs*

- Step 1: Design MX by assuming that all transportation times are zero.
  That is, given Th_0, PX_0 and CT_0, determine MX.
  Represent the obtained MX by $M^* = (m_1^*, \ldots, m_k^*)$.
- Step 2: Design *Traffic* by considering the limit of the transportation capacity.
  That is, given Th_0, PX_0 and CT_0 and M^*, determine *Traffic*.
  Represent the obtained *Traffic* by $T_r^* = (r_1^*, \ldots, r_q^*)$, where $r_1^* = \cdots = r_q^*$.

In procedure *Fab_Ceiling_Design*, its two steps are both based on a marginal allocation algorithm (Connors *et al.* 1996), with only a minor difference. Details of the two steps are described below by two procedures, respectively called *Design_MX* and *Design_Traffic*.

Procedure *Design_MX*

- Step 1: Determine an initial solution M^0, not considering the cycle time constraint.
  - Given Th_0 and PX_0, we intend to determine a minimum number of tools for each tool type.
  - Based on the operation times for each product route, we can aggregate all operations associated with each tool type, and compute its monthly required machine time, and in turn determine the required minimum tool number.
  - Represent the obtained solution by $M^{(0)} = (m_1^0, \ldots, m_k^0)$.
- Step 2: Determine M^*.
  - Given Th_0, PX_0, CT_0 and $M^{(0)}$, we intend to determine M^*.
  - Transportation times are assumed to be zero. The queuing network for modeling a fab is $CT = f(Th, PX, MX)$.
  - Use the marginal allocation method to add tools

Set $i = 0$ and *flag* = 'start'
While (flag = 'start') Do
$CT^{(i)} = f(Th_0, PX_0, MX^{(i)})$
If $CT^{(i)} > CT_0$ then
$m_{j^*}^{(i+1)} = m_{j^*}^{(i)} + 1$ (j^* is the tool type with the highest utilisation)
$m_j^{(i+1)} = m_j^{(i)}$, for $j \neq j^*$, $1 \leq j \leq k$
$i = i + 1$
Else *flag* = 'stop'
Endif
Endwhile
Set $M^* = M^{(i)}$

Procedure *Design_Traffic*

- Step 1: Design *Traffic*; considering the limit of the transportation capacity.
  - Given Th_0, PX_0 and CT_0 and M^*, determine *Traffic*.
  - Use the marginal allocation method to add transportation capacity

Set $i = 1$ and *flag* = 'start'
While (flag = 'start') Do
$CT^{(i)} = f(Th_0, PX_0, M^*, T_r^{(i)})$, where $T_r^{(i)} = (i, \ldots, i)$
If $CT^{(i)} > CT_0$ then $i = i + 1$
Else *flag* = 'stop'
Endif
Endwhile
Set $T_r^* = T_r^{(i)}$.

5. Numerical experiments

Numerical experiments were carried out to justify the importance of the fab ceiling height design. Test data are supported by a fab that manufactures 12 inch wafers, but its identity has been withheld for proprietary reasons. Three types of products are produced. The number of operations for manufacturing products A, B and C are, respectively, 781, 700 and 650. The average processing time for an operation is about 30 min. The fab layout is a spine configuration that involves 15 bays, 60 workstations, and 150 transportation segments. That is, there are 210 servers in the queuing model.

Assumptions associated with the calculation of transportation time are described below. The transportation speed is $4.0\,\mathrm{m\,s^{-1}}$. The area of a fab that produces 45k wafers per month is $100\,\mathrm{m} \times 200\,\mathrm{m}$, and its total tool number is about 660 for a particular product mix $(A:B:C)=(5:2:3)$. The area required for a fab is proportional to the total number of tools. That is, a fab that has 800 tools would require an area of $(800/660) \times 100\,\mathrm{m} \times 200\,\mathrm{m}$, which can be interpreted as $[(800/660)^{1/2} \times 100\,\mathrm{m}] \times [(800/660)^{1/2} \times 200\,\mathrm{m}]$. This implies that the distance of a particular transportation path in a larger fab would be $(800/660)^{1/2} = 1.10$ times that of a smaller fab. As a result, the transportation time would also become longer, 1.10 times that of the smaller fab.

For a particular product mix $(A:B:C)=(5:2:3)$ with a target cycle time $CT_0 = 35$ days, we attempt to evaluate the fab performance under various transportation layer designs for different target throughput Th_0 (number of output wafers per month). As shown in Table 1, at a lower Th_0 (e.g., 25k), a single-layer design is sufficient to fully utilise the tool capacity. Yet, at a higher Th_0, using a single-layer design may result in under-utilisation of tool capacity and yield a low actual throughput—only 80% of the target throughput when $Th_0 = 30$k. The larger Th_0 is, the more serious the tool under-utilisation problem. Tool under-utilisation is due to the fact that the single-layer transportation system *unexpectedly* becomes the bottleneck of the manufacturing system. Therefore, increasing the number of transportation layers would overcome this deficiency. For example, to fully utilise tool capacity, we need a two-layer design when $Th_0 \in \{30\text{k}, 35\text{k}, 40\text{k}\}$ and we need a three-layer design when $Th_0 \in \{45\text{k}, 50\text{k}, 55\text{k}, 60\text{k}\}$.

As stated above, the investment required to add one more transportation layer is about 60 million dollars. To determine how many transportation layers to use for a production scenario, we need to carry out a cost/benefit analysis. Let $Q_{i,i+1}$ represent the annual

Table 1. Transportation layer designs for various Th_0 (number of output wafers per month) for a product mix $(A:B:C)=(5:2:3)$ with $CT_0 = 35$ days.

Target (Th_0)	Tool number	Area ratio (%)	Transportation time ratio (%)	One-layer design actual throughput (k)	Two-layer design actual throughput (k)	Three-layer design actual throughput (k)
25k	382	57.79	76.02	25	25	25
30k	448	67.78	82.33	24.2	30	30
35k	518	78.37	88.52	27.33	35	35
40k	594	89.86	94.80	25.53	40	40
45k	661	100	100	24.2	44.08	45
50k	727	109.98	104.87	23.08	46.15	50
55k	798	120.73	109.88	22	44	55
60k	875	132.38	115.05	21.03	42.08	60

Table 2. Rates of return resulting from the addition of one more transportation layer, where $R_{i\to j}$ denotes the rate of return by moving from i layers to j layers.

Target (Th_0)	Rate of return ($r=40\%$, $p=2500$)	
	$R_{1\to 2}$	$R_{2\to 3}$
25k	0	0
30k	5.80	0
35k	7.67	0
40k	14.47	0
45k	19.88	0.92
50k	23.07	3.85
55k	22.00	11.00
60k	21.05	17.92

increase in throughput on addition of one more layer to a fab originally equipped with i transportation layers. For the case $Th_0 = 45$k in Table 1, we can compute

$$Q_{1,2} = (44.08\text{k} - 24.2\text{k})^{*}12 = 238.56\text{k wafers year}^{-1}$$

and

$$Q_{2,3} = (45.0\text{k} - 44.08\text{k})^{*}12 = 11.04\text{k wafers year}^{-1}.$$

Let r be the gross margin per wafer and p the average selling price per wafer. According to industry experience, we reasonably assume $r=40\%$, $p=2500$ dollars, and all fab equipment completely depreciates in 5 years. Then, on a 5-year time horizon, the benefit of moving from one layer to two layers is $5Q_{1,2}rp = 1192.8$ million dollars. The rate of return in this case is $1192.8/60 = 19.88$—a tremendous payback! Accordingly, we obtain that the rate of return by moving from two layers to three layers is only 0.92—it is not so profitable to move to a three-layer design. Table 2 shows the rate of return obtained for each throughput case of Table 1. From Table 2 we can see that adding one more transportation layer can yield a significant payback in many cases. Therefore, we should give thoughtful consideration to the ceiling height for a large-scale semiconductor fab.

Table 1 also reveals an interesting research issue—the optimal scale of a semiconductor fab. At $Th_0 = 60$k, 875 tools are needed for a single-fab design, yet 896 (448*2) tools are required if we build two fabs (each with $Th_0 = 30$k). The tool cost for adopting a two-fab design would be higher. However, a two-layer transportation design is needed for the two-fab configuration, whereas a three-layer transportation design is needed for a single-fab configuration. As a result, the cost of the transportation facility for the two-fab design as well as the operational cost of clean room space would become lower. The trade-off of the aforementioned costs points out the importance of examining the optimal scale for a semiconductor fab.

Note that, at a particular Th_0, different product mixes might require different layer designs. For example, in Table 3, for $Th_0 = 30$k, a single-layer design is appropriate when $(A:B:C) = (4:3:3)$, but is not so satisfactory when the product mix is $(A:B:C) = (5:2:3)$. Likewise, when $Th_0 = 45$k, we need a three-layer design for $(A:B:C) = (5:2:3)$, but only a two-layer design for $(A:B:C) = (4:3:3)$.

Table 3. Impact of different product mixes on layer design at a particular Th_0.

Target (Th_0)	Product mix	Tool number	One-layer design actual throughput (k)	Two-layer design actual throughput (k)	Three-layer design actual throughput (k)
30k	5:2:3	448	24.2	30	30
	4:3:3	447	30	30	30
	3:2:5	445	30	30	30
45k	5:2:3	661	24.2	44.08	45
	4:3:3	659	24.45	45	45
	3:2:5	661	25.05	45	45

6. Concluding remarks

This paper highlights the importance of the *fab ceiling height* when building a new semiconductor fab. To efficiently utilise tool capacity, one trend is to build the fab as large as possible in order to exploit the effect of capacity pooling. Yet, the transportation distance for a large-scale fab is longer; as a result, the transportation facility might unexpectedly become the bottleneck. This in turn would lead to the under-utilisation of tool capacity and decrease the throughput. To install a greater transportation capacity, a higher fab ceiling height might be needed. This point is often ignored even by experienced architects, who are used to designing a *single-layer* ceiling height for a fab.

We believe that a large-scale fab equipped with only a single-layer transportation system may reduce the fab throughput. We can overcome this deficiency by installing a two- or three-layer transportation system, which in turn requires a higher ceiling height. To justify this proposition, we have developed a queuing network model to evaluate the performance of a fab. This queuing network is adapted from Connors *et al.* (1996) by additionally considering the transportation facilities as finite-capacity resources. Numerical experiments support our proposition.

One extension of this research would be to examine the optimal scale of a semiconductor fab. The larger the fab, the better its tool capacity utilisation, but the higher are its transportation installation costs as well as the operational cost of clean room space due to the requirement of a higher fab ceiling height.

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