15 GHz High-Isolation Sub-Harmonic Mixer With Delay Compensation

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***Abstract*—A 15-GHz high-isolation sub-harmonic mixer (SHM) with delay compensation is demonstrated in this letter using 0.35 $\mu\mathrm{m}$ SiGe heterojunction bipolar transistor (HBT) technology. The proposed SHM consisting of two parallel stacked-LO mixer cores with opposite LO I/Q inputs substantially improves port-to-port isolation. A mathematical analysis regarding the isolation properties is also included in this letter. Further, a conventional stacked-LO SHM (w/o compensation) is also implemented with the same device sizes and bias conditions for a fair comparison. SHMs w/ and w/o compensation have similar conversion gain of 9/10 dB and noise figure of 14/13.5 dB when $f_{\mathrm{LO}} = 7.5$ GHz. However, the delay compensation technique improves the 2LO-RF/IF isolation by 34/35 dB, the LO-RF/IF isolation by 8/9 dB, and the RF-IF isolation by 22 dB.**

***Index Terms*—Heterojunction bipolar transistor (HBT), Marchand balun, polyphase filter, SiGe, sub-harmonic mixer (SHM).**

I. INTRODUCTION

SUB-HARMONIC mixers (SHMs), including stacked-LO and leveled-LO (top-LO or bottom-LO) topologies [1]–[3], are commonly employed in a direct-conversion receiver for their high LO rejection [2] and lessened self-mixing/dc-offset problems. A BJT-type stacked-LO SHM requires about 10 dB less LO power than a leveled-LO SHM does because the equivalent twice LO frequency (2LO) is generated by a current commutation mechanism instead of the transistor nonlinearity [3]. It is important to minimize the LO power requirement because a high LO power requirement results in significant dc power consumption for LO output buffers, especially at high frequencies. However, a current phase delay occurs between the top and bottom mixing cells of a conventional stacked-LO SHM due to the finite time delay of the transistors [3], [4]. As a result, the dc offset and isolation performance are degraded even if the LO signals are perfectly differential-quadrature. In practice, the LO/2LO/RF leakage to the IF output can be filtered out by cascading a low-pass channel filter; however, the LO/2LO leakage to the RF port may mix with itself to generate an output dc offset. Moreover, the leakage may even couple to the antenna and radiate. The received LO signal after radiation and random reflection may then self-mix to generate a time-varying dc offset which cannot be calibrated out using dc-offset cancellation techniques [5].

A SHM using a fully symmetrical LO doubler core [4] was demonstrated in our previous work [6]; however, eight extra transistors and unbalanced current density of mixer transistors in that topology limit the performance, including the maximum operating frequency and isolation performance with the same dc power consumption. In this letter, a SHM with delay compensation to achieve greatly improved port-to-port isolation is proposed. Our proposed topology was also implemented using $0.15\mu\mathrm{m}$ pseudomorphic high electron mobility transistor (pHEMT) technology operating at 40 GHz [7]. However, the large difference in mobility between the two-dimensional electron gas (2-DEG) channel and electrons in AlGaAs donor layer cause the pHEMT device to be sensitive to process variation. A small difference in gate recess etching results in a strong drain current variation. Thus, isolation performance was limited by a large device mismatch. On the other hand, the I-V curve in SiGe HBT technology depends on the material bandgap. The advance in modern epitaxial techniques improves SiGe HBT device match greatly by controlling the bandgap precisely. Due to the better device match in the SiGe HBT technology, 2LO-RF/2LO-IF/LO-RF/ LO-IF/RF-IF isolation in this work is 35/37/29/37/32 dB better than that reported in [7] for the compensated pHEMT SHM.

II. CIRCUIT DESIGN

A. Sub-Harmonic Mixers w/ and w/o Delay Compensation

Fig. 1 shows the schematic of 15 GHz SHMs w/ and w/o delay compensation. Each stacked-LO core $(\mathrm{Q}_1-\mathrm{Q}_8/\mathrm{Q}_9-\mathrm{Q}_{16})$ consists of two Gilbert cells in cascode configuration with a 90° LO input phase offset [1]. The LOI is applied to the top cell of the main SHM and LOQ to the bottom one while the opposite connections are applied to the top/bottom cells of the compensation core. The double-balanced topology ideally achieves infinite LO-RF/IF isolation; however, any signal/device mismatch and substrate coupling degrade both the isolation and even-order distortion performance. Further, the emitter voltage (V_E) of a BJT-type differential pair, indicated in Fig. 1, can be formulated as (1) whose fundamental frequency is $2f_{\mathrm{LO}}$. For the SHM with delay compensation, V_E becomes (2) because both LOI and LOQ signals affect this node. To clearly validate the improvement in isolation performance, the fast Fourier transform (FFT) of V_E in both SHMs at $2f_{\mathrm{LO}}$ with respect to LO voltage swing (V_{LO}) is plotted in Fig. 2(a). Ideally, the 2LO frequency component can be strongly suppressed by the proposed compensation circuit. This cancellation phenomenon has been discussed using a graphic explanation of transient waveforms for MOS mixers

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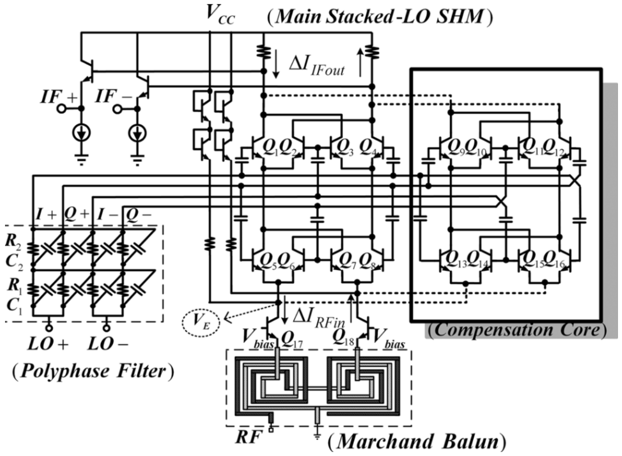


Fig. 1. Schematic of the SiGe HBT sub-harmonic mixers w/ and w/o delay compensation. (LO bias circuit is not shown for simplicity).

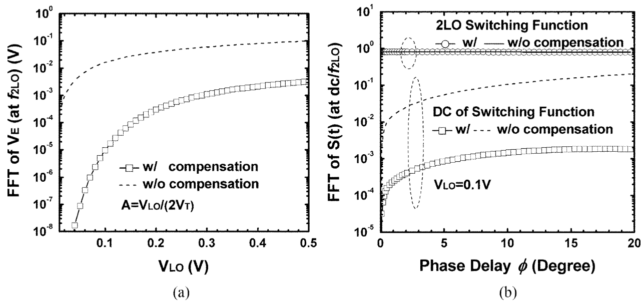


Fig. 2. (a) Fast Fourier transform (FFT) of the emitter voltage V_E at $2f_{\mathrm{LO}}$ with respect to LO voltage swing (b) FFT of the switching function $S(t)$ at dc and $2f_{\mathrm{LO}}$ with respect to a phase delay for both sub-harmonic mixers.

but with different circuit implementations, a 4x SHM [5] and a merged LNA and I/Q mixer [8]

$$V_{E(w/o)} = V_{DC} + V_T \ln\left[\cosh(A\cos\omega_{\mathrm{LO}}t)\right] \tag{1}$$

$$V_{E(w/)} = V_{DC} + V_T \ln\left[\cosh(A\cos\omega_{\mathrm{LO}}t) + \cosh(A\sin\omega_{\mathrm{LO}}t)\right] \tag{2}$$

$$S(t)_{(w/o)} \equiv \frac{\Delta I_{IFout(w/o)}}{\Delta I_{RFin}} = \tanh(A\cos\omega t)\times\tanh[A\sin(\omega t+\phi)] \tag{3}$$

$$\begin{aligned} S(t)_{(w/)} &\equiv \frac{\Delta I_{IFout(w/)}}{\Delta I_{RFin}} \\ &= \frac{1}{2}\begin{bmatrix} \tanh(A\cos\omega t)\times\tanh[A\sin(\omega t+\phi)] \\ +\tanh(A\sin\omega t)\times\tanh[A\cos(\omega t+\phi)] \end{bmatrix} \end{aligned} \tag{4}$$

where $A = V_{\mathrm{LO}}/2V_T$ and ϕ represents the phase delay between the top and bottom cells, respectively.

Next, the sub-harmonic switching function $S(t)$, defined as the ratio of the output IF current and input RF current, can be formulated as (3) [9] and (4) for the SHMs w/o and w/ compensation, respectively. That is, the differential RF input current passes through $S(t)$ and generates IF output. On the other hand, a dc imbalance (dc component of ΔI_{in}) results in a leakage of $S(t)$ containing a 2LO frequency component to outputs.

The FFT of the switching function $S(t)$ for both SHMs at dc and $2f_{\mathrm{LO}}$ with respect to a phase delay (ϕ) is shown in Fig. 2(b). The dc of $S(t)$ results in an RF leaky path to output without a frequency translation. Using the compensation circuit, the dc term of $S(t)$ can be highly suppressed while the 2LO switching performance still maintains as shown in Fig. 2(b).

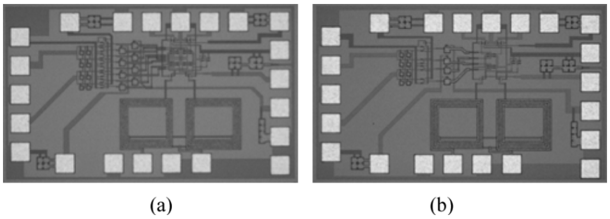

(a) (b)

Fig. 3. (a) Photograph of the SiGe HBT sub-harmonic mixers w/ compensation (b) w/o compensation.

In addition, the current bleeding technique is used to boost the conversion gain by drawing out the dc current from the mixer core to allow larger loading resistances, thus resulting in a lower transistor cut-off frequency (f_t). In this work, the current density of transistors in the SHM without compensation is $0.4\ \mathrm{mA}/\mu\mathrm{m}^2$ with a 40-GHz f_t. The transistor in the SHM with compensation has a current density of $0.2\ \mathrm{mA}/\mu\mathrm{m}^2$ with a 30-GHz f_t because the two stacked-LO cells are in parallel. The phase delay between the top and bottom cells can be approximated as $(180^\circ/\pi)\times\tan^{-1}(f/f_t)$ which is the current phase delay of a common-base configuration. Conventionally, if no delay compensation is applied, the phase delay (usually $\gg 10^\circ$ at high frequencies) greatly degrades the RF-IF isolation, even if the LO signal is perfectly differential-quadrature. Note that, a wideband common-collector voltage buffer is employed at each I/Q output to validate the pure isolation performance without additional suppression of LO leakage [3], [6], [7]. The mathematic analyses (1)–(4) are based on the exponential transfer curve which is still preserved at different temperatures for a SiGe HBT device. Thus, the isolation improvement by the compensation core is still significant over temperature.

B. Passive Differential/Quadrature Generator

Differential-quadrature LO signals are generated by a two-section polyphase filter from differential LO signals. For the designed center frequency of 7.5 GHz, the resistances and capacitances are 50 Ω and 0.424 pF in the first section and are 100 Ω and 0.212 pF (two 0.424-pF capacitors in series) in the second section. The progressive increase of the resistances somewhat relaxes the voltage loss. Additionally, all the dc biases of the following mixer cores are fed from 5-kΩ resistors.

An RF Marchand balun [7] consisting of two quarter-wavelength spiral edge-coupled coupled lines is used to generate differential signals as shown in Fig. 1. Each coupled line has a line width, line spacing and outer diameter of 8 $\mu\mathrm{m}$, 2 $\mu\mathrm{m}$ and 270 $\mu\mathrm{m}$, respectively.

III. MEASUREMENT PERFORMANCE

Photographs of the SHMs w/ and w/o delay compensation are shown in Figs. 3(a) and 3(b), respectively. The supply voltage is 3.3 V with the total current consumption of 8 mA (5 mA in mixer core; 1.5 mA in each IF I/Q buffer) for both circuits. The conversion gain with respect to RF frequency is shown in Fig. 4.

With an LO power of $-2\ \mathrm{dBm}$, the SHMs w/ and w/o compensation have a peak conversion gain of 10/11 dB at $\mathrm{RF} = 8\ \mathrm{GHz}$ with an RF bandwidth of 5–17 GHz which is dominated by the RF Marchand balun. The EM simulated frequency response of the Marchand balun is also shown in Fig. 4. The

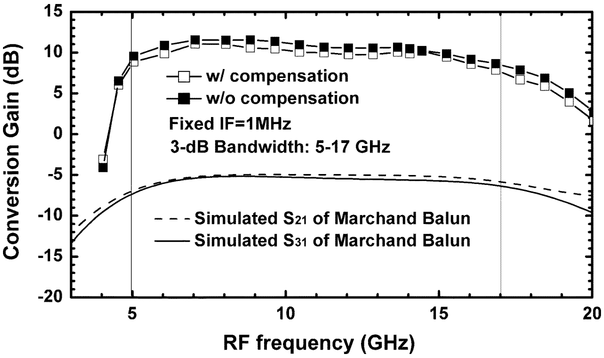
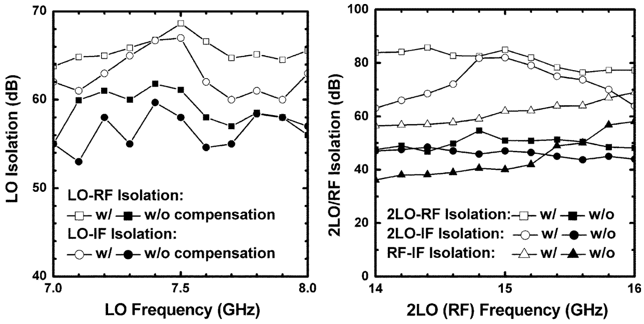


Fig. 4. Conversion gain of the SiGe HBT sub-harmonic mixers w/ and w/o compensation as a function of RF frequency.



(a) (b)

Fig. 5. (a) LO-RF/IF isolation (b) 2LO-RF/IF and RF-IF isolations of the SiGe HBT sub-harmonic mixers w/ and w/o compensation.

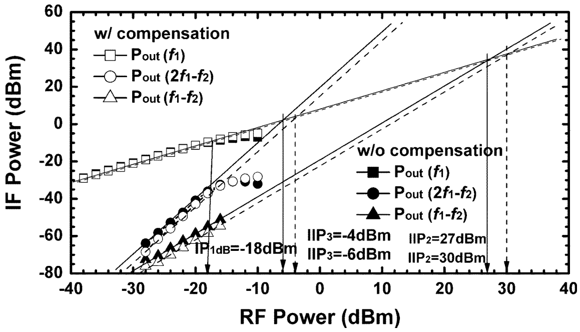


Fig. 6. Power performance including $\mathrm{IP}_{1\,\mathrm{dB}}$, IIP_3, and IIP_2 of the SiGe HBT sub-harmonic mixers w/ and w/o compensation.

isolation performance at $f_{\mathrm{LO}} = 7.5$ GHz (center frequency of the polyphase filter) and $f_{\mathrm{RF}} = 15.001$ GHz is shown in Fig. 5. By the compensation technique, large improvement covering a wide bandwidth is obtained. The 2LO-RF/IF isolation is improved by 34/35 dB, LO-RF/IF isolation by 8/9 dB and RF-IF isolation by 22 dB at 15 GHz. To verify the effect of process variation, five random samples are measured. Thus, the 2LO-RF/IF isolation performance of the SHM w/ compensation still shows at least 30 dB improvement than that of the SHM w/o compensation.

Fig. 6 shows the power performance of the SHMs w/ and w/o compensation at $f_{\mathrm{LO}} = 7.5$ GHz, $f_{\mathrm{RF1}} = 15.001$ GHZ and $f_{\mathrm{RF2}} = 15.0012$ GHZ; thus, the $\mathrm{IP}_{1\,\mathrm{dB}}$, IIP_3 and IIP_2 are $-18/-18$ dBm, $-4/-6$ dBm, and $30/27$ dBm, respectively. The input return loss of both SHMs is better than 11 dB from 5 to 30 GHz. The SHMs w/ and w/o compensation achieve conversion gain of 9/10 dB with 200-MHz IF bandwidth and double-sideband noise figure of 14/13.5 dB when $f_{\mathrm{LO}} = 7.5$ GHz as shown in Fig. 7. The thermal noise of an active mixer is dominated by the RF Marchand balun and the input trasnconductance stage; thus, the overall noise figure is similar for both SHMs because of the identical transistor sizes and bias conditions.

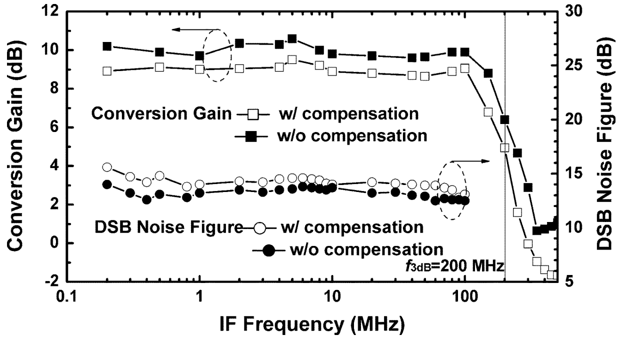


Fig. 7. Conversion gain and double sideband noise figure of the SiGe HBT sub-harmonic mixers w/ and w/o compensation.

IV. CONCLUSION

A SiGe HBT 15-GHz SHM using a delay compensation technique maintains similar gain and noise figure but greatly improves port-to-port isolation, including LO/2LO-RF, LO/2LO-IF and RF-IF isolation when compared with a conventional stacked-LO topology for the same transistor sizes, bias conditions and power consumption.

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