Analysis and Design of the 0.13-μm CMOS Shunt–Series Series–Shunt Dual-Feedback Amplifier

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***Abstract*—This paper demonstrates the design methodology of the shunt–series series–shunt dual-feedback Meyer wideband amplifier. The small-signal S-parameters are obtained for the first time using the pole-and-zero analysis, thus giving the RF designers a detailed insight into the Meyer amplifier. A 10-GHz wideband amplifier is demonstrated in this paper, using 0.13-μm CMOS technology to verify our design theory. The experimental results of the S-parameters highly agree with our theory.**

***Index Terms*—Dual feedback, Meyer amplifier, series–shunt feedback, shunt–series feedback, wideband amplifier.**

I. Introduction

RECENTLY, high-frequency and wideband communication applications, such as the 60-GHz (WLAN, ultrawideband (UWB), and even Direct Broadcast Satellite (DBS)/low noise block (LNB), have arisen. In the past, the DBS or LNB receivers have required a high-frequency LNA to receive the desired signal and a wideband buffer amplifier for additional gain amplification [1]–[3] when the gain of the first-stage LNA is insufficient. In addition, the 60-GHz WLAN front-end receiver [4], [5] has become more and more important, and this application may also require some extra gain block, depending on the system architecture and frequency planning. The UWB system inevitably needs a wideband LNA to increase the sensitivity of the entire receiver chain through 3–10-GHz RFs. There are already tremendous research topics about the wideband LNA [6]–[14] for UWB.

The wideband amplifier is a general-purpose gain building block, and the main requirement of a wideband amplifier is its gain and input/output matching bandwidth. It is worthwhile to mention that not only the gain bandwidth but also the matching bandwidth has to meet the system requirement to provide extra gain to any RF system. The $P_{1\,\mathrm{dB}}$ gain saturation point, the linearity performance, and the noise performance are also important criteria to judge whether a wideband amplifier is good or not. In the past, the microwave distributed amplifier has dominated the wideband application [15]–[17]. However, the distributed amplifier wastes too many valuable chip estates, and thus, the cost cannot be low. Recently, the mainstream technology is the feedback amplifiers [6]–[11], [18], [19].

Most of the feedback wideband amplifiers are single-stage amplifiers with inductive peaking techniques [6]–[10], [20]. Although the lumped feedback amplifiers have already saved a lot of space when compared with the distributed counterparts, the on-chip peaking inductors still consume extra chip space. As a result, the other useful two-stage amplifier topologies consisting of resistive feedback loops are more attractive for a low-cost consideration [21]–[27]. Among so many wideband amplifier topologies, there are basically two most popular two-stage wideband amplifier configurations—the Meyer (shunt–series series–shunt feedbacks) topology [21]–[23] and the Kukielka (shunt–series shunt–shunt feedbacks) topology [11], [24]–[26].

The Kukielka topology is a Cherry–Hopper amplifier [28] with a global shunt–series feedback loop [11], [26]. The Cherry–Hopper amplifier basically consists of a transconductance amplifier in the first stage and a transimpedance amplifier in the second stage. The Kukielka amplifier preserves the broadband characteristic of the Cherry–Hopper amplifier, and the global shunt–series feedback loop can further increase the bandwidth. The input and output matching is achieved simultaneously by the global shunt–series feedback loop and the local shunt–shunt feedback loop. The design methodology of the Kukielka amplifier has already been well established in [11] and [26].

In this paper, those design equations considering the S-parameters of the Meyer wideband amplifier are determined. The Meyer topology is a two-stage amplifier with two global shunt–series and series–shunt feedback loops, and this schematic makes the Meyer configuration totally different from the Kukielka topology. However, the gain bandwidth and the input/output matching bandwidth can be simultaneously achieved by two feedback loops, as shown in Fig. 1. Because there are two global feedback loops in the Meyer topology, the input and output common-mode level, as well as the bias currents, is well defined, as shown in Fig. 1.

In our previous work on the Kukielka amplifier [26], the loop gain T is always less than one when the input matching is achieved. Therefore, the bandwidth is limited because the amplifier has an overdamped gain response. The capacitive peaking technique was employed to extend the bandwidth but the peak gain is 2 dB more than the dc gain and the group

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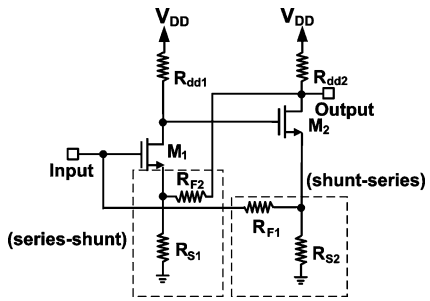

Fig. 1. Circuit schematic of the Meyer (shunt–series and series–shunt) amplifier.

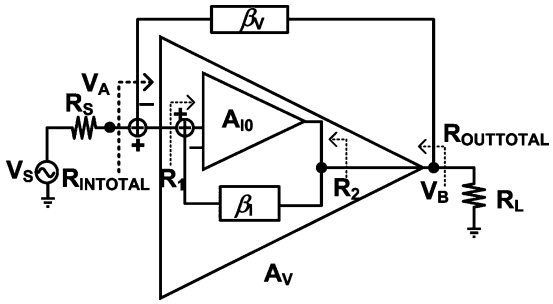

Fig. 2. Block diagram of the Meyer wideband amplifier.

delay has a variation of 20 ps within the 3-dB bandwidth. On the contrary, our proposed topology eliminates this fundamental constraint; thus, the input/output matching can be achieved while the loop gain T is still flexible. Without using the capacitive peaking, the 10-GHz bandwidth is achieved with a maximally flat gain response and only a 5-ps group-delay variation within the bandwidth.

Previous works [21], [22] have discussed the design equations of the Meyer amplifier using bipolar junction transistor (BJT) technologies; however, the previously reported approach has limitations for the CMOS technologies caused by an invalid analytical approximation, as described in the following sections of this paper. To realize the insights of the Meyer wideband amplifier, we use the pole-and-zero analysis [29], [30] to determine all of the design equations of the S-parameter. This paper provides a consistent method to determine the frequency response of the gain and the terminal impedance matching when compared with [21] and [22]. Methods to solve the small-signal parameters between this paper and previous counterparts are discussed at the end of Section II. It is worthwhile to mention that the method we have proposed in this paper is more complete and general, particularly for the deep submicrometer CMOS technologies.

To our best knowledge, the small-signal S-parameters of the Meyer topology has been established for the first time in this paper. Section II presents the detailed design parameters of the Meyer amplifier, including the gain, input/output impedances, loop gain, poles, and S-parameters. A Meyer amplifier based on these design principles is discussed in Section III. Measurement results are shown in Section IV, and Section V concludes this paper.

II. Analysis of the Meyer Wideband Amplifier

A. DC Voltage Gain, Input Resistance, and Output Resistance of the Meyer Wideband Amplifier

The Meyer configuration consists of two feedback loops, as shown in Fig. 1. One of the feedback loops is the shunt–series global feedback, consisting of R_{F1} and R_{S2}, between the first- and second-stage common-source amplifiers. This feedback loop is a current-sampling shunt-mixing loop; therefore, the feedback loop provides current–current feedback [30]. On the other hand, the global series–shunt feedback is a voltage-sampling series-mixing feedback loop, consisting of R_{F2} and R_{S1}, and provides voltage–voltage feedback [30]. The shunt–series and series–shunt feedback loops are represented by β_I and β_V, respectively.

Because the Meyer configuration contains two feedback loops, the A- and β-circuits are too complicated to find. However, the Meyer wideband amplifier can be decomposed step by step as follows. Fig. 2 shows the block diagram of the Meyer amplifier. As shown in Fig. 2, the Meyer amplifier can be treated as a voltage amplifier A_V with a voltage–voltage feedback loop β_V. Moreover, the A-circuit A_V of the Meyer amplifier is a current feedback amplifier. As long as the open loop current gain A_{I0} and the feedback loop β_I are found, the voltage gain to the load A_V can be determined by

$$A_V = A_I \times \frac{R_2 \| R_L}{R_1} = \frac{A_{I0}}{1 + A_{I0}\beta_I} \times \frac{R_2 \| R_L}{R_1}. \quad (1)$$

R_1 and R_2 are the dc input and output resistances of the current feedback amplifier. Therefore, the total closed-loop gain of the Meyer amplifier from input node A to output node B is

$$A_{\mathrm{Vtotal}} = \frac{V_B}{V_A} = \frac{A_V}{1 + A_V\beta_V}. \quad (2)$$

The analytic forms of β_V and β_I will be defined later in the following section.

Fig. 3 shows the decomposition sequences of the Meyer amplifier. First, the Meyer topology shown in Fig. 1 can be decomposed into the circuit shown in Fig. 3(a). Fig. 3(a) contains a voltage amplifier and a voltage feedback loop β_V. It is interesting that the A-circuit shown in Fig. 3(a) is actually a current amplifier with a shunt–series feedback loop. Hence, the A-circuit shown in Fig. 3(a) can be further decomposed into a current amplifier with a feedback loop β_I, as shown in Fig. 3(b).

First, the overall open-loop voltage gain (V_B/V_A) of the Meyer topology can be described as (2). A_V can be obtained by solving the closed-loop current gain A_I, the input resistance R'_{IN}, and the output resistance R'_{OUT}, including the loading effect [30] of the wideband amplifier circuit, as shown in Fig. 3(b). Therefore

$$\begin{aligned} A_{\mathrm{Vtotal}} &= \frac{A_I \times \frac{R'_{\mathrm{OUT}} \| R_L}{R'_{\mathrm{IN}}}}{1 + A_I \times \frac{R'_{\mathrm{OUT}} \| R_L}{R'_{\mathrm{IN}}} \times \beta_V} \\ &= \frac{\frac{A_{I0}}{1+A_{I0}\beta_I} \times \frac{R'_{\mathrm{OUT}} \| R_L}{R'_{\mathrm{IN}}}}{1 + \frac{A_{I0}}{1+A_{I0}\beta_I} \times \frac{R'_{\mathrm{OUT}} \| R_L}{R'_{\mathrm{IN}}} \times \beta_V}. \end{aligned} \quad (3)$$

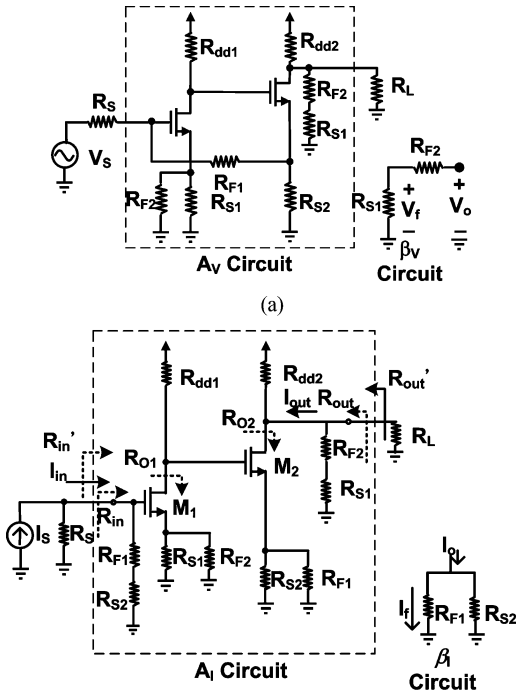

Fig. 3. (a) A_V and β_V circuits of the Meyer amplifier after first decomposition. (b) A_I and β_I circuits after second decomposition.

Next, we calculate the A_{I0}, $R'_{\rm IN}$ (the input resistance when the shunt–series feedback is taken into consideration), and $R'_{\rm OUT}$ (the output resistance when the series–shunt feedback is taken into consideration) of the current amplifier, as shown in Fig. 3(b). The A_{I0} is straightforward

$$\begin{aligned} A_{I0} &= \frac{I_{\rm out}}{I_{\rm in}} \\ &\cong (R_{F1}+R_{S2}) \times G_{m1} \times (R_{dd1}\|R_{O1}) \times G_{m2} \\ &= (R_{F1}+R_{S2}) \times \frac{g_{m1}}{1+g_{m1}\cdot(R_{S1}\|R_{F2})} \\ &\quad \times (R_{\rm dd1}\|R_{O1}) \times \frac{g_{m2}}{1+g_{m2}\cdot(R_{S2}\|R_{F1})} \end{aligned} \tag{4}$$

where the resistance R_{O1} is the output resistance when looking into the drain node of the transistor M_1. The input resistance of the current amplifier is

$$R'_{\rm IN} = \frac{R_{\rm IN}}{1+A_{I0}\beta_I} = \frac{(R_{F1}+R_{S2})}{1+A_{I0}\beta_I}. \tag{5}$$

Thus, the total dc input resistance of the Meyer amplifier can be determined by

$$R_{\rm INTOTAL} = \frac{(R_{F1}+R_{S2})\times(1+A_V\beta_V)}{(1+A_{I0}\beta_I)} \tag{6}$$

with the feedback factors

$$\beta_I = -\frac{R_{S2}}{R_{S2}+R_{F1}} \quad \beta_V = -\frac{R_{S1}}{R_{S1}+R_{F2}}. \tag{7}$$

Similarly, the output resistance can be obtained by

$$R'_{\rm OUT} = R_{O2}\|(R_{F2}+R_{S1})\|R_{\rm dd2} \cong (R_{F2}+R_{S1})\|R_{\rm dd2}. \tag{8}$$

where the resistance R_{O2} is the output resistance when looking into the drain node of the transistor M_2. The resistance R_{O2} is greatly increased because the source node of the transistor M_2 is in series with a large shunt–series feedback resistance [30]. Therefore, the R_{O2} is very large [30], and the value of R_{O2} can be neglected when R_{O2}, $(R_{F2}+R_{S1})$, and $R_{\rm dd2}$ are parallel. Thus, the dc total output impedance of the Meyer amplifier is equal to

$$R_{\rm OUTTOTAL} = \frac{R'_{\rm OUT}}{(1+A_{V0}\beta_V)} \cong \frac{(R_{F2}+R_{S1})\|R_{\rm dd2}}{(1+A_{V0}\beta_V)}. \tag{9}$$

Using the circuit shown in Fig. 3, A_V now can be described as follows:

$$\begin{aligned} A_V &= \frac{A_{I0}}{1+A_{I0}\times\beta_I} \times \frac{\rm R'_{OUT}\|R_L}{R'_{\rm IN}} \\ &= \frac{A_{I0}}{1+A_{I0}\times\beta_I} \times \frac{(R_{F2}+R_{S1})\|R_{\rm dd2}\|R_L}{\frac{(R_{F1}+R_{S2})}{1+A_{I0}\times\beta_I}} \\ &= A_{I0} \times \frac{(R_{F2}+R_{S1})\|R_{\rm dd2}\|R_L}{(R_{F1}+R_{S2})}. \end{aligned} \tag{10}$$

The total dc voltage gain of the Meyer amplifier is

$$\begin{aligned} A_{V\,\rm total} &= \frac{A_V}{1+A_V\times\beta_V} \\ &= \frac{A_{I0}\times\frac{(R_{F2}+R_{S1})\|R_{\rm dd2}\|R_L}{(R_{F1}+R_{S2})}}{1+A_{I0}\times\frac{(R_{F2}+R_{S1})\|R_{\rm dd2}\|R_L}{(R_{F1}+R_{S2})}\times\beta_V}. \end{aligned} \tag{11}$$

Consequently, as shown in Figs. 1 and 2, the dc voltage gain from the voltage source V_S to the load R_L can be described as

$$A_{V\,\rm DC} = \frac{V_B}{V_S} = \frac{R_S}{R_S+R_{\rm in\,total}} \times \frac{A_V}{1+A_V\times\beta_V}. \tag{12}$$

The dc values of the voltage gain, the input resistance, and the output resistance of the Meyer wideband amplifier are determined by (6), (9), and (12).

B. System Transfer Function

In order to determine the frequency response of the small-signal voltage forward transmission coefficient S_{21}, we have to determine the system transfer function of the Meyer amplifier. From (11), the system transfer function must be

$$\begin{aligned} A_{V\,\rm total}(s) &= \frac{A_V(s)}{1+A_V(s)\times\beta_V} \\ &= \frac{A_{I0}(s)\cdot K}{1+A_{I0}(s)\cdot K\times\beta_V} \\ &= \frac{A_{I0}\cdot K}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)+A_{I0}\cdot K\times\beta_V} \end{aligned} \tag{13}$$

where $A_{I0}K$ is the voltage gain and K is a ratio of resistances

$$K = \frac{(R_{F2} + R_{S1}) \| R_{\mathrm{dd2}} \| R_L}{(R_{F1} + R_{S2})}. \tag{14}$$

Therefore, the loop gain T of the Meyer amplifier can be described as

$$\begin{aligned} T &= A_{I0} K \beta_V \\ &= -(R_{F1} + R_{S2}) \times \frac{g_{m1}}{1 + g_{m1} \cdot (R_{S1} \| R_{F2})} \\ &\quad \times (R_{\mathrm{dd1}} \| R_{O1}) \times \frac{g_{m2}}{1 + g_{m2} \cdot (R_{S2} \| R_{F1})} \\ &\quad \times \frac{(R_{F2} + R_{S1}) \| R_{\mathrm{dd2}} \| R_L}{(R_{F1} + R_{S2})} \times \frac{R_{S1}}{R_{S1} + R_{F2}}. \end{aligned} \tag{15}$$

The denominator in (13) can be expressed as

$$s^2 + s(\omega_1 + \omega_2) + (1 + T)\omega_1\omega_2. \tag{16}$$

Next, as long as ω_1 and ω_2 are determined, the frequency response of the system-transfer function can be obtained. The original two poles (ω_1 and ω_2) change to two complex poles (P_1 and P_2), caused by the voltage feedback loop. The feedback poles P_1 and P_2 can be calculated as

$$P_1, P_2 = -\frac{1}{2}(\omega_1 + \omega_2) \pm \frac{1}{2}\sqrt{(\omega_1 + \omega_2)^2 - 4(1 + T)\omega_1\omega_2}. \tag{17}$$

The characteristic (16) can be changed to the following standard form:

$$s^2 + s\frac{\omega_0}{Q} + \omega_0^2 = 0 \tag{18}$$

where ω_0 is the natural frequency and can be described as

$$\omega_0 = \sqrt{(1 + T)\,\omega_1\omega_2} \tag{19}$$

and Q is the quality factor

$$Q = \frac{\sqrt{(1 + T)\,\omega_1\omega_2}}{\omega_1 + \omega_2}. \tag{20}$$

There are various pole/zero locations for the frequency responses of a feedback amplifier design. For example, the inverse Chebyshev and Cauer responses have specific transmission zeros which cannot be applied to our all-pole system in this paper. On the other hand, the Chebyshev response has a wider bandwidth but a worse group-delay flatness in a given gain-ripple condition while the Bessel–Thomson response has an equal-ripple delay response but a narrower gain bandwidth. Compared with the aforementioned choices, the Butterworth (maximally flat) response is a good tradeoff among the gain, group-delay flatness, and the bandwidth. Moreover, to maximize the speed of the overall two-stage amplifier system, the two separate poles (ω_1 and ω_2) of each single-stage amplifier are set the same. Consequently, in order for the transfer function (18) to have the maximally flat response, the Q has to be 0.707. Since ω_1 equals to ω_2, the loop gain ($T = A_{I0}K\beta_V$) should be one by (20) in this paper. Furthermore, as the Q value is lower than 0.707, for example, the two-pole Bessel–Thomson response, the bandwidth is sacrificed but the system is more stable since the two complex poles are far from the imaginary axis in the complex frequency domain. On the contrary, as the Q value is higher than 0.707, e.g., the two-pole Chebyshev response, the gain peak exists and is inclined to instability because the poles are close to the imaginary axis. Thus, a Q of 0.707 is a good choice for stability concerns.

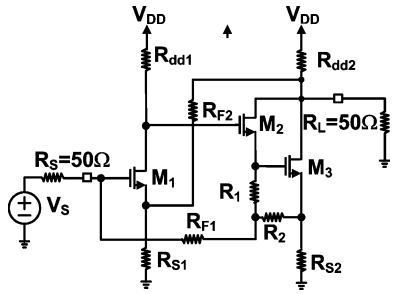

Fig. 4. Final topology of the modified Meyer wideband amplifier.

C. Pole Locations of the Meyer Amplifier

Different from the Kukielka amplifier, the Meyer topology does not use the Cherry–Hopper structure for the basic amplifier. A simple common-source amplifier definitely suffers from a poor frequency response; therefore, the speed of the second stage must be improved. In practical applications, the Darlington configuration can be used for the second stage in the Meyer amplifier. Fig. 4 shows the typical topology of the Meyer wideband amplifier including the source impedance R_S and the loading impedance R_L. As shown in Fig. 4, the Meyer amplifier consists of two source degenerative stages; the first stage is a common-source amplifier, and the second stage is a Darlington frequency doubler.

Assume that the Meyer amplifier is a two-pole system, the first pole is the dominant pole of the first-stage common-source amplifier, and the second pole is the dominant pole of the second-stage Darlington amplifier. The equivalent small-signal model used for solving the first pole of amplifier A_{I0} is shown in Fig. 5(a). Neglecting the biasing resistors R_1 and R_2, the first pole can be obtained by the open-circuit time constant method [31]

$$\omega_1 = \frac{1}{C_{\mathrm{gs1}}R_{\mathrm{gs1}} + C_{\mathrm{gd1}}R_{\mathrm{gd1}}} \tag{21}$$

where the R_{gs1} is approximated

$$\frac{[R_S \| (R_{F1} + R_{S2})] + (R_{S1} \| R_{F2})}{1 + g_{m1}(R_{S1} \| R_{F2})} \tag{22}$$

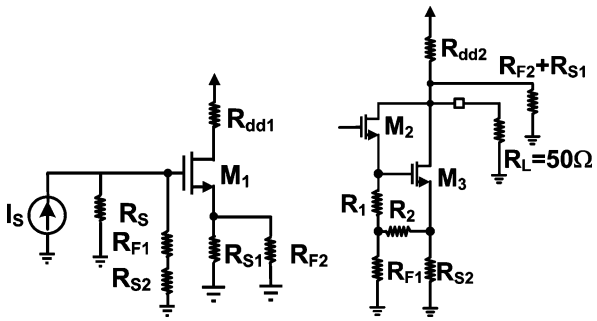

Fig. 5. Small-signal model for solving (a) the first pole and (b) the second pole.

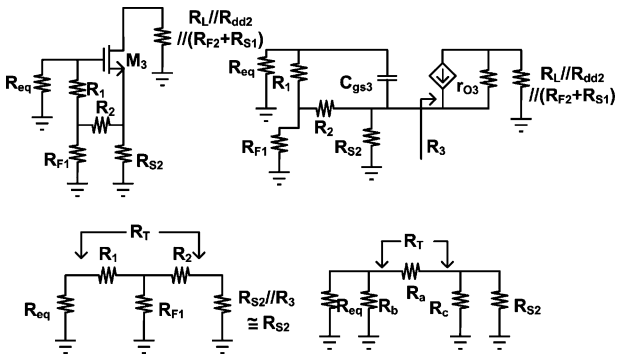

Fig. 6. Small-signal model of the Darlington stage used to solve the frequency response.

while the resistor R_S (the source impedance) is 50 Ω and $R_{\rm gd1}$ equals

$$R_{\rm gd1} = R_1' + R_{L1}' + \frac{g_{m1}}{1 + g_{m1}(R_{S1}||R_{F2})} R_1' R_L' \tag{23}$$

where $R_1' = R_S||(R_{F1} + \mathrm{R}_{S2})$ and $R_{L1}' \cong R_{\rm dd1}$.

The second pole can be obtained by the small-signal model shown in Fig. 5(b). Although the second stage is a Darlington pair, the dominant pole can be approximated by [30]

$$\omega_2 \cong \frac{1}{C_{\rm gs} R_{\rm gs} + C_{\rm gd} R_{\rm gd}}. \tag{24}$$

The transconductance g_{m2} of the common-drain transistor M_2 is normally much smaller than that of the transistor M_3 in the Darlington configuration. Consequently, the capacitance of $C_{\rm gd2}$ and $C_{\rm gs2}$ can be neglected, and only the capacitance of $C_{\rm gs3}$ and $C_{\rm gd3}$ is taken into consideration. Therefore, the dominant pole of the Darlington stage is approximated by calculating the pole of the transistor M_3. Some parameters must be found before calculating $R_{\rm gs}$ and $R_{\rm gd}$.

Assuming that the resistor R_{S2} is small enough, which is usually valid for the CMOS amplifiers, since the CMOS transistor g_m is naturally much smaller, the resistors $R_{\rm gs}$ and $R_{\rm gd}$ can be determined using the small-signal model shown in Fig. 6. The resistor $R_{\rm eq}$ is the output resistance of the source node of the transistor M_2, and it is approximated as

$$R_{\rm eq} \cong \frac{1}{g_{m2}}. \tag{25}$$

As shown in Fig. 6, the resistances can be calculated by changing the T-network (R_1, R_2, and R_{F1}) into the Π-network (R_a, R_b, and R_c) [32]. Thus, the resistances are

$$\begin{cases} R_a = \frac{R_1 R_2 + R_1 R_{F1} + R_2 R_{F1}}{\mathrm{R}_{F1}} \\ R_b = \frac{R_1 R_2 + R_1 R_{F1} + R_2 R_{F1}}{\mathrm{R}_{1}} \\ R_c = \frac{R_1 R_2 + R_1 R_{F1} + R_2 R_{F1}}{\mathrm{R}_{2}}. \end{cases} \tag{26}$$

Therefore, the $R_{\rm gs}$ and $R_{\rm gd}$ can be derived as [30]

$$\begin{aligned} R_{\rm gs} &= \left[R_a || \left(\frac{(R_c||R_{s2}) + (R_{\rm eq}||R_b)}{1 + g_{m3}(R_c||R_{s2})} \right) \right] \\ R_{\rm gd} &= \Bigg((R_{\rm eq}||R_b)||R_2' + R_L' \\ &\qquad + \frac{g_{m3}}{1 + g_{m3}(R_c||R_{s2})} (R_{\rm eq}||R_b) R_L' \Bigg) \end{aligned} \tag{27}$$

where

$$\begin{aligned} R_2' &= (R_a + (R_c||R_{s2}) + g_{m3} R_a (R_c||R_{s2})) \\ R_L' &= R_L||R_{\rm dd2}||(R_{F2} + R_{S1}). \end{aligned} \tag{28}$$

Because the source impedance (R_S) and load impedance (R_L) are both 50 Ω, the S_{21} of the amplifier is just the same as the voltage gain with a scaling factor of two by definition. Therefore, according to (21) and (24), S_{21} can be determined once the A_{I0} and K are obtained by (4) and (14)

$$S_{21}(s) = 2 \times \frac{V_B}{V_S} = \frac{2 \times A_{V\,\rm DC}}{\left(1 + \frac{s}{P_1}\right)\left(1 + \frac{s}{P_2}\right)}. \tag{29}$$

According to [6], [7], and [9], we intentionally assume that all the S-parameters have the same poles (P_1 and P_2); therefore, the S-parameters can be obtained by following:

$$S_{11}(s) = \frac{R_{\rm INTOTAL} - R_S(=50\ \Omega)}{R_{\rm INTOTAL} + R_S(=50\ \Omega)} \frac{\left(1 + \frac{s}{Z_1}\right)\left(1 + \frac{s}{Z_2}\right)}{\left(1 + \frac{s}{P_1}\right)\left(1 + \frac{s}{P_2}\right)} \tag{30}$$

$$S_{22}(s) = \frac{R_{\rm OUTTOTAL} - R_L(=50\ \Omega)}{R_{\rm OUTTOTAL} + R_L(=50\ \Omega)} \frac{\left(1 + \frac{s}{Z_3}\right)\left(1 + \frac{s}{Z_4}\right)}{\left(1 + \frac{s}{P_1}\right)\left(1 + \frac{s}{P_2}\right)}. \tag{31}$$

The zeros Z_1 and Z_2 can be obtained by solving the root of the denominator in (17), by changing R_S into $-R_S$ [26], [29], [30]. Similarly, the zeros Z_3 and Z_4 are the root of the denominator in (17), by changing R_L into $-R_L$.

D. Simplified Design Equations and Design Methodology

Although the design equations of the dc values and pole locations are found in the previous sections, it is still difficult to give the designer an approach to arrange the values of resistors

in order to optimize the gain, the input/output resistances, and the bandwidth. However, the first-order design methodology of the Meyer amplifier is very clear, based on some practical assumptions. As shown in (19), if the designer wants the largest bandwidth, the ω_1 must equal ω_2, and $A_{I0}K\beta_V$ has to equal one. If the loop gain $(A_{I0}K\beta_V)$ is equal to one, then (32) is true, as shown at the bottom of the page. Therefore, the input and output resistances can be simplified into (33) and (34), as shown at the bottom of the page. As we can see, these equations are helpful for the designers to determine the values of the resistors when the gain-bandwidth product is maximized. In order to obtain the first-order design equation, some extra but reasonable assumptions must be made. Assuming that β_I and β_V are too small to achieve the unity loop gain, the term $R_{F1}+R_{S2}$ and the term $R_{F2}+R_{S1}$ therefore has to be large enough. For the output impedance matching, the resistance $R_{\rm dd2}$ in (34) can be described as

$$2\times 50 = R_{\rm dd2}. \tag{35}$$

Therefore, the resistance of the loading resistor $R_{\rm dd2}$ must be near 100 Ω for the perfect impedance matching. Under the same assumptions, (33) can be simplified to

$$50 = \frac{2R_L R_{S1} R_{\rm dd2}(R_{F1}+R_{S2})}{(R_{F2}+R_{S1})R_{S2}R_L + (R_{F2}+R_{S1})R_{S2}R_{\rm dd2}}. \tag{36}$$

Using the results in (14) and (35), the voltage gain of the A-circuit, as shown in Fig. 3(a), is

$$A_{I0}\cdot K = 33 G_{m1} R_{dd1} G_{m2}. \tag{37}$$

Consequently, the first-order design flow for the maximum gain-bandwidth product is summarized as follows.

1) Assume $A_{I0}K\beta_V = 1$, and thus, $R_{\rm dd2}$ approximates 100 Ω for the output impedance matching.
2) Design the pole locations by (21) and (24). The first pole must be equal to the second pole.
3) The values determined in design flow 2) have to be checked by (36) to perform the input impedance matching.

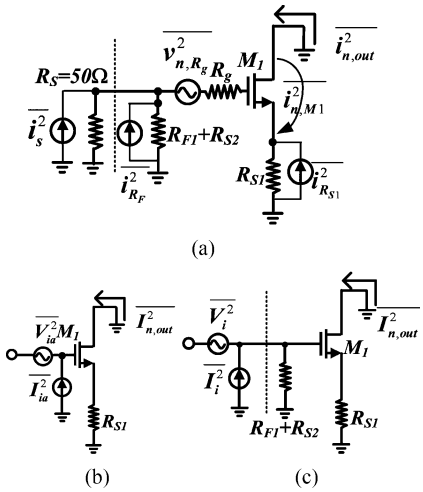

Fig. 7. (a) Noise contributions of the first stage. (b) Equivalent input-referred noise voltage/current of the first stage before feedback. (c) After feedback.

4) Recursively repeat processes 1)–3) until the optimized values of the S-parameters are found.

E. Noise Analysis

The demonstrated work is a cascade amplifier with dual feedback loops. The noise contribution from the second stage can be neglected because the gain of the first stage is high enough $(>10$ dB$)$ [11]. Therefore, we can obtain the noise figure by simply calculating the total short-circuit output noise current spectral density from the first stage.

There are several key noise sources in the first stage, as shown in Fig. 7(a). The channel thermal noise current spectral density of a MOSFET in the saturation region is modeled as $\overline{i_d^2} = 4kT\cdot NEF\cdot g_m\Delta f$, where $NEF=\gamma g_{d0}/g_m$ represents the noise excess factor while g_{d0} is the zero-bias conductance. The parameter γ is a bias-dependent factor which equals 2/3 only for a long-channel device but it is much greater than 2/3 for a short-channel device [3], [33]. In addition, the gate resistance (R_g) and the source degeneration resistance (R_{S1}) also need to be considered. Fortunately, the gate resistance of the MOSFET

$$\begin{aligned} A_{I0}K\beta_V = 1 &\cong (R_{F1}+R_{S2})\times G_{m1}\times R_{\rm dd1}\times G_{m2}\times \frac{(R_{F2}+R_{S1})\|R_{\rm dd2}\|R_L}{(R_{F1}+R_{S2})}\times\frac{R_{S1}}{(R_{F2}+R_{S1})} \\ \therefore G_{m1}R_{\rm dd1}G_{m2} &= \frac{(R_{F2}+R_{S1})R_{\rm dd2}+(R_{F2}+R_{S1})R_L+R_{\rm dd2}R_L}{R_{S1}R_{\rm dd2}R_L}. \end{aligned} \tag{32}$$

$$\begin{aligned} R_{\rm INTOTAL} &= \frac{(R_{F1}+R_{S2})\times 2}{(1+A_{I0}\beta_I)} = \frac{2(R_{F1}+R_{S2})}{1+(R_{F1}+R_{S2})G_{m1}R_{\rm dd1}G_{m2}\frac{R_{S2}}{R_{F1}+R_{S2}}} \\ &= \frac{2R_L\times R_{S1}\times R_{\rm dd2}(R_{F1}+R_{S2})}{R_{S1}R_{\rm dd2}R_L + R_{S2}[(R_{F2}+R_{S1})R_L+(R_{F2}+R_{S1})R_{\rm dd2}+R_LR_{\rm dd2}]} \end{aligned} \tag{33}$$

$$R_{\rm OUTTOTAL} = \frac{(R_{F2}+R_{S1})\|R_{\rm dd2}}{2} = \frac{(R_{F2}+R_{S1})R_{dd2}}{2(R_{F2}+R_{S1}+R_{\rm dd2})}. \tag{34}$$

has a small effect on the gain performance, owing to the relatively high input impedance looking into the gate node.

The equivalent input-referred noise voltage ($\overline{V_{ia}^2}$) and noise current ($\overline{I_{ia}^2}$) of the first stage without feedback, as shown in Fig. 7(b), are written as follows [9], [35]:

$$\overline{V_{ia}^2} = 4kTR_g\Delta f + 4kTR_{S1}\Delta f + 4kT\cdot NEF\cdot\frac{1}{g_{m1}}\Delta f \tag{38}$$

$$\overline{I_{ia}^2} = 4kT\cdot\frac{NEF}{g_{m1}}\Delta f\cdot|\omega C_{\text{eff}}|^2 \tag{39}$$

where C_{eff} is composed of $C_{\text{gs1}}/(1+g_{m1}R_{S1})$ and a parasitic capacitance shunted to ground.

As shown in Fig. 7(c), since the shunt-type feedback resistance only affects the equivalent input-referred noise current but not the noise voltage [11], [35], $\overline{V_i^2}\approx\overline{V_{ia}^2}$ still holds, and the equivalent input-referred noise current density ($\overline{I_i^2}$) can be modified as

$$\begin{aligned}\overline{I_i^2} &= \overline{I_{ia}^2}+\frac{\overline{V_{ia}^2}}{R_F^2}+\frac{4kT}{R_F}\Delta f\\ &= 4kT\cdot\frac{NEF}{g_{m1}}\Delta f\cdot|\omega C_{\text{eff}}|^2\\ &\quad+\frac{4kTR_g\Delta f+4kTR_{S1}\Delta f+4kT\cdot\frac{NEF}{g_{m1}}\Delta f}{R_F^2}+\frac{4kT}{R_F}\Delta f.\end{aligned} \tag{40}$$

Consequently, the overall noise figure is given by

$$\begin{aligned}NF &= 1+\frac{\overline{V_i^2}+\overline{I_i^2}R_S^2}{4kTR_S\Delta f}\\ &= 1+\left(1+\frac{R_S^2}{R_F^2}\right)\frac{R_g+R_{S1}+\frac{NEF}{g_{m1}}}{R_S}+\frac{R_S}{R_F}\\ &\quad+NEF\cdot\frac{R_S}{g_{m1}}C_{\text{eff}}^2\omega^2.\end{aligned} \tag{41}$$

Equation (41) gives a direct insight that the noise figure increases when the feedback resistor $R_F(=R_{F1}+R_{S2})$ decreases (i.e., the amount of feedback ($\beta_I = R_{S2}/(R_{F1}+R_{S2})$) increases) while the ideal noiseless feedback does not change the noise figure performance [35]. However, if R_F is large enough, the noise performance is determined by the size and the bias of the transistor M_1, not the resistor R_F. Moreover, the noise arises at high frequencies due to the capacitance at the gate node.

F. Linearity

Fig. 8 is the block diagram of a nonlinear circuit with a feedback loop. Equation (41) shows that, without considering the feedback loops, the linearity performance of a cascade amplifier usually dominates at the latter stage since the gain of the first stage is high. The mathematical expressions of the input/output relations of the nonlinear amplifier before/after feedback are described in (43) [36]. Although the linear gain degrades by a factor of $(1+A_1\beta)$ after feedback, the third-order distortion can be much more reduced. As a consequence, the third-order

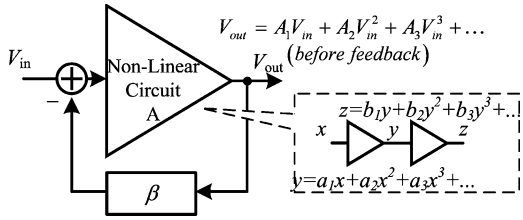

Fig. 8. Block diagram of a nonlinear circuit with a feedback loop.

output-referred intercept point (OIP_3) can be predicted to have an improvement of $10\log(1+A_1\beta)$ dB as described in (44).

$$\frac{1}{V_{OIP3}^2}\approx\frac{1}{a_1^2b_1^2V_{OIP3,1}^2}+\frac{1}{b_1^2V_{OIP3,2}^2} \tag{42}$$

$$\begin{cases}v_{\text{out}}(\text{before f.b.}) = A_1v_{\text{in}}+A_3v_{\text{in}}^3+\cdots\\ v_{\text{out}}(\text{after f.b.}) = \frac{A_1}{1+A_1\beta}v_{\text{in}}+\frac{A_3}{(1+A_1\beta)^4}v_{\text{in}}^3+\cdots\end{cases} \tag{43}$$

$$V_{OIP3}(\text{after f.b.}) = V_{OIP3}(\text{before f.b.})\times\sqrt{1+A_1\beta}. \tag{44}$$

Since the loop gain $T = A_V\beta_V$ is set as unity for the Butterworth gain response of the proposed dual-feedback amplifier, the linearity performance does not improve much.

G. Comparisons of the Small-Signal Parameters in This Paper and Previous Works

Compared with the previous works [21], [22], and [26], the derived circuit parameters in this paper, such as the total terminal impedances and gain in this paper, are more general, because the transistor g_m need not be very large in our assumption. According to the work in [22], there is a major assumption that the current gain of the transistor is large enough (which is true for the bipolar transistors), and thus, both of the current and voltage feedback loops have an equal feedback loop gain with the closed-loop voltage gain. This assumption is employed to obtain the input and output impedance in [22]. Obviously, the higher current gain makes the bandwidth lower, since the gain-bandwidth product is a constant in the feedback amplifier design. However, the g_m of the CMOS transistor is usually much smaller than that of the BJT transistor; hence, the current gain of MOS transistors may not be large enough, and this assumption is not suitable for the CMOS Meyer wideband amplifier.

In addition, as described by [21] and [22], the derived S_{21} is approximated to

$$S_{21}\cong\frac{1}{2}\frac{R_{F2}+R_{E1}}{R_{E1}}. \tag{45}$$

The source degenerative resistor R_{E1} in (45) equals the source degeneration resistor R_{S1} in this paper. As shown in (45), the term S_{21} is proportional to $1/\beta_V$, which is based on the very huge loop gain of the voltage feedback path, and only the voltage feedback loop (consisting of resistors R_{F2} and R_{S1}) is taken into consideration in this special case. Under this circumstance, the loop gain is greatly larger than one; therefore, the bandwidth is not optimized. The result of S_{21} in (45) implies that only the voltage feedback loop dominates the dual feedback system; however, this is not true for analyzing the terminal impedance matching, particularly for CMOS technologies.

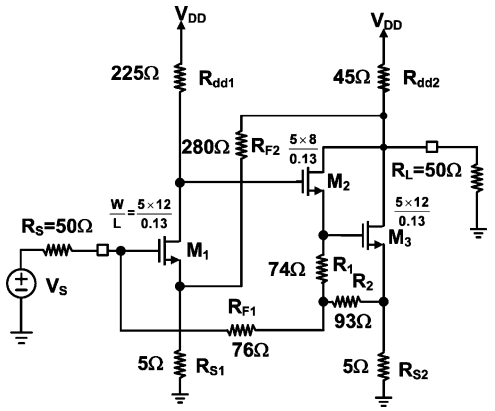

Fig. 9. Demonstrated 0.13-μm CMOS Meyer wideband amplifier with its component values.

Consequently, the approaches of [21] and [22] for determining the terminal impedances and the gain are based on the conflicting assumptions in a single circuit. This paper has not provided completely unique information but a general formula to determine the gain and input/output impedance.

III. Circuit Design

In this section, a shunt–series series–shunt dual feedback wideband amplifier is demonstrated using 0.13-μm CMOS technology. The advanced 0.13-μm CMOS technology is suitable to implement the high-performance RFICs. The circuit schematic and the designed values of the resistors are shown in Fig. 9. This Meyer amplifier is designed and implemented with CMOS technology to verify our theory because of its excellent cutoff frequency provided by the technology. This Meyer amplifier is designed without the source capacitive peaking technique in order to simplify the prediction of the pole locations.

A successful wideband amplifier must contain the following specifications: wide gain bandwidth and matching bandwidth, acceptable noise performance, and reasonable linearity. In order to achieve the goals, a proper dc biasing point and the device size should be decided first.

The dc biasing current and device size influence the noise and linearity performance. A larger dc with a smaller MOS device increase the f_T, and thus, the gain and noise performance upgrade [6], [7], and [9]. However, a higher gain generally introduces a worse linearity performance, and a smaller device size causes more mismatches between devices, although the Meyer amplifier is single ended. A small device also may increase the gate resistance, and thus, the noise degrades [6], [7], and [9].

In this paper, some tradeoffs between noise performance, gain, bandwidth, and linearity are made. In order to extend the bandwidth up to 10 GHz with a dc gain larger than 16 dB, the linearity is traded a little bit. In addition, the first stage of the Meyer amplifier basically dominates the noise performance of the two-stage Meyer amplifier. The f_T of the first-stage common-source amplifier shall be as high as possible. Unfortunately, a higher f_T requires a larger dc, and thus, the voltage drop across resistor R_{S1} will be too large. As a result, we optimized the circuit elements, as shown in Fig. 9.

As shown in Fig. 9, a Darlington pair is employed in the second stage of the demonstrated Meyer amplifier. The wideband amplifier is implemented using 0.13-μm CMOS technology. The minimum gate length of this technology is 0.13-μm, and the maximum cutoff frequency f_T is around 80 GHz. As shown in Fig. 9, the first-stage common-source transistor M_1 has a gate length of 0.13 μm and 12 gate fingers. Similarly, gate length, finger number, and finger width are shown in Fig. 9. Some tradeoffs are made in order to optimize the circuit performance in terms of gain, port matching, noise figure, and linearity. The small-signal parameters of transistors M_1, M_2, and M_3 are summarized in Table I.

TABLE I
Equivalent Small-Signal Parameters of the CMOS.

	M_1	M_2	M_3
g_m (mS)	30	24	54
C_{gs} (fF)	40	21	97
C_{gd} (fF)	32	12	38

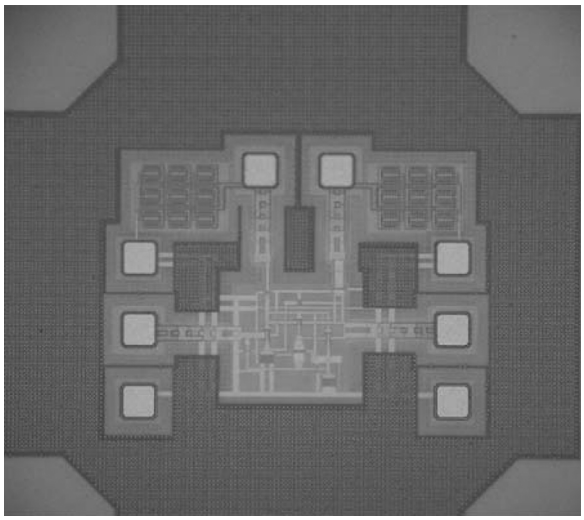

Fig. 10. Die photograph of the 0.13-μm CMOS shunt–series series–shunt dual feedback amplifier.

IV. Measurement Results

The die photo of the 0.13-μm CMOS wideband amplifier is shown in Fig. 10. The input RF ground–signal–ground (GSG) pads are on the left, while the output RF GSG pads are on the right. There are two dc bias pads on the top. As shown in Fig. 10, the chip consumes an area of $800\times800\,\mu\text{m}^2$. The wideband amplifier only needs a chip area of $150\times150\,\mu\text{m}^2$, and the probing pads, metal dummies, and poly dummies occupy the remaining 96% chip area. This is because the 0.13-μm process requires dummies to perform the chemical–mechanical polishing process. The dc supply is 2.5 V, and the current consumption is 24 mA.

An HP8510 network analyzer, in conjunction with the cascade on-wafer probe station, is used to measure the S-parameter performances. Fig. 11 shows the measured power gain S_{21} of the fabricated wideband amplifier. In addition, the predicted S_{21}, by our theory, and the simulated S_{21} are shown in the same figure for comparison. The Meyer amplifier has a 17-dB gain with a 10-GHz bandwidth.

Fig. 12 shows the measured, predicted, and simulated S_{11} values while the measured, predicted, and simulated S_{22} values are shown in Fig. 13. The measured input and output return losses

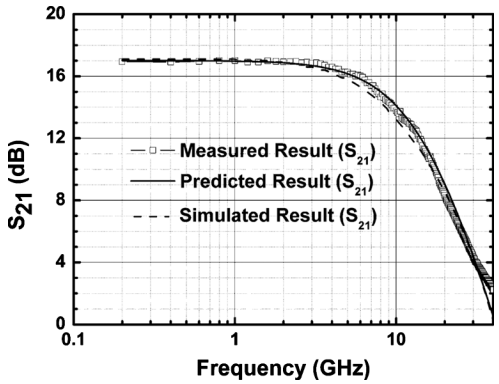

Fig. 11. Measured, predicted, and simulated S_{21} values of the 0.13-μm CMOS Meyer wideband amplifier.

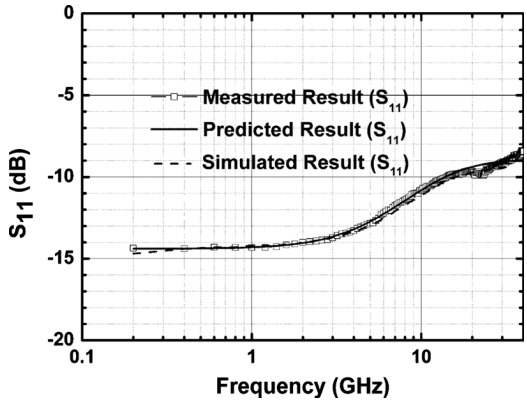

Fig. 12. Measured, predicted, and simulated S_{21} values of the 0.13-μm CMOS Meyer wideband amplifier.

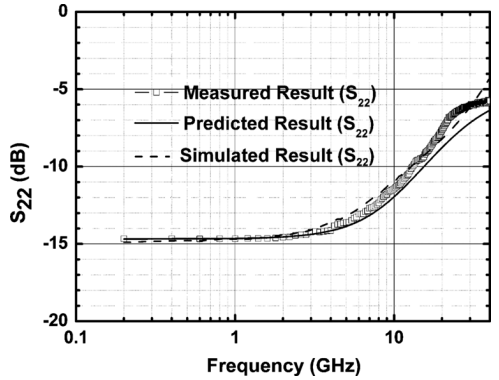

Fig. 13. Measured, predicted, and simulated S_{21} values of the 0.13-μm CMOS Meyer wideband amplifier.

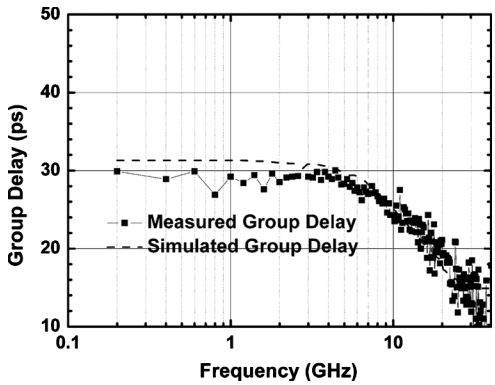

Fig. 14. Measured and simulated group delay of the 0.13-μm CMOS Meyer wideband amplifier.

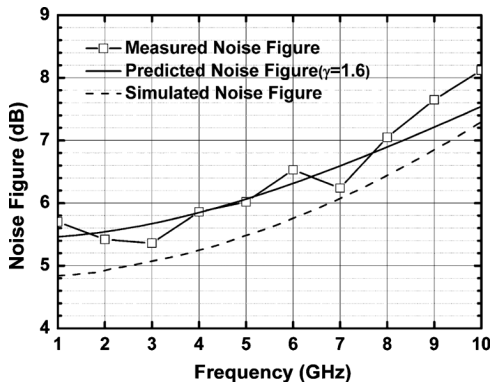

Fig. 15. Measured and simulated noise figure of the 0.13-μm CMOS Meyer wideband amplifier.

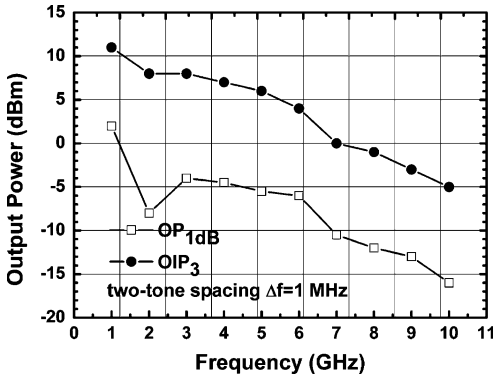

Fig. 16. Measured power performance of the 0.13-μm CMOS Meyer wideband amplifier.

are less than -10 dB in the 3-dB gain bandwidth, respectively. Consequently, the predicted results and also the simulated results highly agree with the experimental S-parameter results. Fig. 14 shows the measured and simulated group delay of the Meyer wideband amplifier. Because the maximal flat response is chosen, the group delay is thus smooth, not like Chebyshev or Cauer responses.

The measured noise figure of the Meyer wideband amplifier is shown in Fig. 15. The measured noise figure is lower than 8.2 dB in the 3-dB gain bandwidth. The simulated and predicted noise performances are also shown in Fig. 15. Here, the predicted noise figure is calculated with the modification of $NEF = 1.6$. However, the measured noise figure is, on average, 0.5 dB higher than our simulation results because the BSIM3 model only provides long-channel noise modeling parameters which are not suitable for the advanced CMOS technologies nowadays [33], [37], but the simulation still shows the same trend as the measured data. Compared to the reported CMOS wideband amplifiers [6], [7], and [9], the measured curve trend of the noise figure as a function of the RF frequency is also the same. The noise figure increases rapidly as the RF frequency becomes higher.

Fig. 16 shows the measured $OP_{1\,\mathrm{dB}}$ and OIP_3 of the demonstrated Meyer wideband amplifier. The power performances degrade as the operating frequency gets higher. The $OP_{1\,\mathrm{dB}}$ is -16 dBm, and the OIP_3 is -5 dBm when the frequency equals 10 GHz.

V. Conclusion

The first-order design methodology of the shunt–series series–shunt double-feedback Meyer wideband amplifier has been developed. A 10-GHz wideband amplifier has been demonstrated using a 0.13-μm CMOS technology. Experimental results highly agree with our theory, and the design tradeoffs are discussed. The small-signal S-parameters are obtained by the approach of pole-and-zero analysis; therefore, the insight of the Meyer wideband amplifier is given to the RF designers. The fabricated 0.13-μm CMOS wideband amplifier has a 17-dB gain, a -10-dB input return loss, and a -10-dB output return loss with a 10-GHz bandwidth. The noise figure of the demonstrated amplifier is lower than 8.2 dB, while the $OP_{1\mathrm{dB}}$ and OIP_3 are better than -16 and -5 dBm, respectively, over the usable bandwidth.

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