國 立 交 通 大 學

電子工程學系 電子研究所

碩 士 論 文

高介電常數介電層在金氧半元件
及動態隨機存取記憶體上之特性研究

Investigation of High-κ Dielectrics on MOS Devices and DRAM

研 究 生：張祐慈 Yu-Tzu Chang

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中華民國 九十四 年 六 月

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摘要

隨著動態隨機存取記憶體(DRAM)科技之研究進入21世紀，元件尺寸不斷的微縮是其持續發展的動力。然而經由閘極介電層與汲極－基板接面穿隧而增加的漏電流是DRAM電晶體微縮所必須考慮的重要問題。為了滿足低待機電源之應用，利用高介電常數材料(high-κ)來取代二氧化矽是不可或缺的趨勢。本篇論文主要研究課題為高介電常數材料的特性，諸如崩潰電場、電荷捕獲以及溫度相關之可靠度問題，以期將高介電常數材料應用在閘極介電層與DRAM上。

本論文首先利用尖端放電電荷非接觸式半導體氧化層量測方法研究臭氧氣體沉積後退火溫度對於氧化鉭(Ta_2O_5)薄膜之影響。研究結果發現介電層厚度隨著退火溫度升高而增加，推測是由於界面層之成長所造成。電容之平帶電壓位移在經過臭氧氣體沉積後退火後由正位移轉為負方向之位移，是因為臭氧氣體沉積後退火會造成薄膜內被捕獲電子減少或者是電洞捕捉量增加。軟崩潰電場的增加以及均勻性的劣化主要是由於界面氧化層成長不均所導致。此外，高溫臭氧氣體沉積後退火能夠填補矽基板與氧化鉭薄膜界面之懸鍵進而降低界面缺陷密度。

其次，我們研究一種以臭氧水在室溫成長的薄氧化層基本特性。實驗結果發現臭氧水氧化層之成長速率與去離子水中臭氧濃度成正比。同時其具有自我限制的飽和成長特性可以改善經過爐管或是快速高溫氧化成長薄膜之厚度不均。臭氧水氧化層亦可以用來改善矽表面粗糙度達41%，很適合當作閘極介電層之前的界面處理來降低閘極的漏電流。其次，比較不同界面處理對於二氧化鉿(HfO_2)閘極介電層電容特性之影響。結果顯示，經過臭氧水氧化層界面處理的元件具有較低的漏電流，可忽略的磁滯效應以及良好的介電可靠度，因此為改善高介電常數材料與矽基板界面特性之絕佳候選。

最後分別以捕獲效率、電導峰值位移以及缺陷產生率來探討不同界面處理對於二氧化鉿閘極介電層電荷捕獲特性的影響。臭氧水氧化層界面處理在經過600^{o}C沉積後退火之後形成較佳的界面，因此相較於氨氣及快速高溫氧化前處理擁有最低的捕獲效率，界面缺陷劣化及缺陷產生率。然而，在未經過600^{o}C沉積後退火處理之前，臭氧水氧化層由於低成長溫度所導致之不完全氧化以及較粗糙的界面，因此特性較差。此外，亦研究了二氧化鉿閘極介電層之漏電流傳輸機制，實驗顯示在有效電場小於3.5 MV/cm時，其相對應之漏電流傳輸機制為蕭基特發射主導，當電場界於3.5~6 MV/cm時，則是由Fowler-Nordheim穿隧所主導。

Investigation of High-κ Dielectrics on MOS Devices and DRAM

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Abstract

As DRAM enters the 21st century, the course of DRAM technology development continues to be driven by the need for smaller cell sizes. One major problem which must be considered in scaling of the DRAM transistor is increased leakage due to tunneling currents in the gate insulator and in the drain–body junction. It stresses the urgent need for high dielectric constant (κ) gate dielectrics for low stand-by power application. In this thesis, the dielectric properties of high-κ dielectrics, some reliability issues such as breakdown field, charge trapping and temperature-dependence behaviors were extensively studied for both gate dielectric and DRAM applications.

The first objective of this thesis is the effects of O_3 post deposition annealing temperature on the properties of Ta_2O_5 which were investigated by COCOS (Corona Oxide Characterization of Semiconductor) non-contact metrology. It was found that the dielectric thickness was increased as raising annealing temperature, which could be ascribed to the thick interfacial layer (IL) growth. Moreover, the flat band voltage shift changed from positive to negative due to the electron traps elimination and partially hole traps generation in the film.

Non-uniform interfacial layer oxidation after O_3 annealing was supposed to cause the increasing of the field strength and break the the soft breakdown distribution. It had been supposed that high temperature ozone annealing could compensate the dangling bond at the interface of Si/Ta_2O_5 proceed to minimize the interface trap density and improve the uniformity.

Secondly, the basic properties of the ozone oxide were studied. The growth rate of ozone oxide was increased as raising the ozone quantity contained in DI water. A saturated oxidation was observed in the growth curves and the resultant self-limiting property could improve the thickness uniformity after furnace or/and rapid thermal oxidation. Ozone oxide could improve Si surface roughness by 41%, which was beneficial to suppress the leakage current density of the stacked gate dielectric. Then the influences of surface treatment prior to HfO_2 gate dielectric deposition were investigated. As a result, sample with Ozone treatment revealed small leakage current, negligible hysteresis and excellent dielectric reliability, which was considered to be one of the most potential alternative to improve the interface properties between high-κ dielectrics and silicon surface.

Finally, the surface treatment effects on the charge trapping characteristics the HfO_2 gate dielectric were researched in terms of trapping efficiency, conductance peak shift, and SILC defect generation. Ozone oxide performed the lowest trapping efficiency, D_{it} degradation and defect generation rate after 600^{o}C PDA than NH_3 or RTO treatment partially due to the better interface properties. However, Ozone-samples without PDA expressed poor results, which might be caused by the incomplete oxidation and rougher interface owing to the low growth temperature. The current transport mechanism was also investigated. When E_{eff}<3.5 MV/cm, the corresponding current transport mechanism was Schottky emission under gate injection conditions. F-N tunneling dominated the conduction mechanism during 6>Eeff>3.5 MV/cm.

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CHAPTER 1

Introduction

1.1 Background

Dynamic random access memory (DRAM) technology has progressed at a rapid pace since the invention of the one-transistor/one-capacitor cell (Fig. 1.1) in the late 1960s [1], with an introduction of a new generation and chip density quadrupling every three years. The decade of the 1990s has seen DRAM manufacturing advance from the 4Mb to the 256Mb generations [2]. According to the International Technology Roadmap for Semiconductor (ITRS) 2004 [3], the DRAM half pitch and the generation at production have reached 80nm and 1Gbits, respectively in 2005 (Table 1.1). The high volumes that DRAM manufacturing guarantees and the relatively predictable product roadmap have made DRAM the vehicle that drives a large part of the manufacturing infrastructure for the microelectronics industry. DRAM technology is optimized for low cost and high yield, with a particular focus on low-leakage devices and the storage capacitor.

A DRAM cell (Fig. 1.1) consists of a MOSFET (also referred to as the array-access transistor or transfer device) in series with a storage capacitor. The wordline contacts the gate of the transfer device, and the bitline contacts the source/drain of the transfer device that is not connected to the storage capacitor. Data is written by turning on the transfer device by raising the wordline and writing a high or low voltage level onto the storage capacitor via the bitline. Data is stored by turning off the transfer device by lowering the wordline, trapping the voltage/charge on the storage capacitor. In industry standard DRAM, data is conventionally

read by precharging the bitline midway between the high and low levels, turning on the transfer device, and sensing the bitline voltage change (the signal voltage) caused by charge sharing between the storage capacitor and the parasitic bitline capacitance.

As DRAM enters the 21st century, the course of DRAM technology development continues to be driven by the need for smaller cell sizes. One major problem which must be considered in scaling of the DRAM transistor is increased leakage due to tunneling currents in the gate insulator and in the drain–body junction. It suggests that at the current rate of progress, Table 1.1 stresses the urgent need for high dielectric constant (κ) gate dielectrics for low stand-by power application after the year 2006 [4]. For this reason, several alternative materials for silicon dioxide are currently being investigated. High-κ materials, including aluminum oxide (Al_2O_3), hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) etc [5]-[8], shown in Table 1.2**,** are the potential candidates to replace SiO_2. The most benefit for high-κ dielectrics is leakage current reduction by several orders of magnitude at the same EOT compared to SiO_2. However, in device performance point of view, a suitable gate dielectric candidate should also meet the other requirements, including high thermal stability, high carrier mobility, small oxide charges, good stress immunity and silicon process compatible.

The storage capacitor is another area of focus for DRAM cell-size reduction. Methods of reducing the amount of silicon real estate occupied by the storage capacitor while maintaining sufficient capacitance have included the following: Thinning of the capacitor dielectric, use of insulating materials with a higher dielectric constant (κ), and three dimensional capacitor structures [9]. The ability to maintain large-surface-area capacitors in such small cells is made possible by three-dimensional capacitor structures that are built either above the silicon surface (stacked capacitors) [10], or in the silicon substrate (trench capacitors) [11]. Dielectrics with higher dielectric constants (relative dielectric constant 20) than the NO (nitride–oxide) dielectric commonly used by DRAM manufacturers through the

0.15-μm generation, is needed for both stacked and trench designs. One of the most important features for a material to be used as the insulating dielectric in DRAM is the low leakage current. Tantalum pentoxide (Ta_2O_5) and barium strontium titanate (BSTO) are the most likely candidates for the 0.12-μm and 0.1-μm generation, respectively.

1.2 Motivation

Over the years, the use of amorphous, thermally grown SiO_2 as a gate dielectric offers several key advantages in CMOS processing including a stable (thermodynamically and electrically), high-quality Si-SiO_2 interface as well as superior electrical isolation properties. In modern CMOS processing, defect charge densities are on the order of 10^{10} cm^{-2}, midgap interface state densities are ~ 10^{10} $cm^{-2}eV^{-1}$ and hard breakdown fields of 15 MV/cm are routinely obtained and are therefore expected regardless of the device dimensions. These outstanding electrical properties clearly present a significant challenge for any alternative gate dielectric candidate [12, 13].

There are a wide variety of films with higher κ values than SiO_2, ranging from Si_3N_4 with a κ value of 7, up to Pb-La-Ti (PLT) with a κ value of 1,400. Unfortunately, many of these films are not thermodynamically stable on silicon, or are lacking in other properties such as a high breakdown voltage, low defect density, good adhesion, thermal stability, low deposition temperature, ability to be patterned easily and low charge states on silicon. Currently interest seems to be centered on films such as HfO_2 with κ values of 25~30, enabling a 6.4x to 10.3x increase in film thickness for equivalent performance. Transistors based on these films showed excellent overall performance presenting possible solutions to the need for thinner EOT with low leakage. Therefore, HfO_2 performs promising

competitiveness due to its relatively high free energy of reaction with Si (47.6 kcal/mole at 727°C) [14], and relatively high band gap (~5.8eV) among the high-k contenders [15]. However, the crystallization temperature of HfO_2 is quite low, which restricts the thermal budget after the deposition and brings about the high leakage current and non-uniformity associated with grain boundaries.

Once the geometrical options to maintain sufficient capacitance at smaller ground rules have been exhausted, capacitor dielectrics with higher dielectric constant κ offer an attractive path to achieving enhanced capacitance per area. It should be pointed out here that high-κ use as a gate oxide is distinct from high-κ use in DRAM capacitors. In a DRAM capacitor, the objective is to maximize capacitance per unit area. The capacitor is frequently fabricated after the transistors and sees less thermal processing. DRAM capacitor oxides can be sandwiched between various electrode materials that allow high-κ materials to be used that can't be used as a gate oxide where contact with silicon is a requirement. Ta_2O_5 with high dielectric constant (κ>22) is the most widely studied high-k material with applications in the DRAM industry. Except to the advantage of high dielectric constant, its dielectric constant is independent of the applied voltage and it can be easily removed by using CF_4 [16]. The material is used in MIS capacitors in conjunction with a suitable top electrode such as TiN. Both CVD and ALD processes are known for the deposition of Ta_2O_5. However, Ta_2O_5 films also have disadvantages, such as its small band gap (~4.5eV), poor thermal stability with Si substrate, and unstable microstructure. Therefore, Ta_2O_5 is suitable for stacked capacitor applications but does not withstand the thermal budget required for trench DRAMs.

Both tantalum pentoxide (Ta_2O_5) [17, 18] and hafnium oxide (HfO_2) [8], [19]-[22] had been proved as promising materials for DRAM application for this and next generations. Nonetheless, the effects of these kinds of high-κ dielectrics on DRAM are seldom understand. To further realize the dielectric properties of these high-κ dielectrics, some reliability issues

such as breakdown field, charge trapping and temperature-dependence behaviors are extensively studied for both gate dielectric and DRAM applications.

1.3 Organization of the Thesis

In this thesis, the dielectric properties of high-κ dielectrics, some reliability issues such as breakdown field, charge trapping and temperature-dependence behaviors were extensively studied for both gate dielectric and DRAM applications. Chapter 1 showed the background and the motivation for the applications of the high-κ dielectrics.

In chapter 2, the effects of O_3 post deposition annealing temperature on the properties of Ta_2O_5 were researched by COCOS non-contact metrology.

In chapter 3, the influences of surface treatments prior to hafnium oxide (HfO_2) deposition were investigated. Comparisons between various surface treatments, including: ozone water oxidation (Ozone), rapid thermal oxidation (RTO) and ammonia (NH_3) nitridation were studied.

In chapter 4, the surface treatment effects on the charge trapping characteristics of the HfO_2 gate dielectric were studied in terms of trapping efficiency, conductance peak shift, and SILC defect generation. The current transport mechanism was also investigated.

At the end of this thesis, the conclusions and the recommendations for the topics which could be further researched were given in chapter 5.

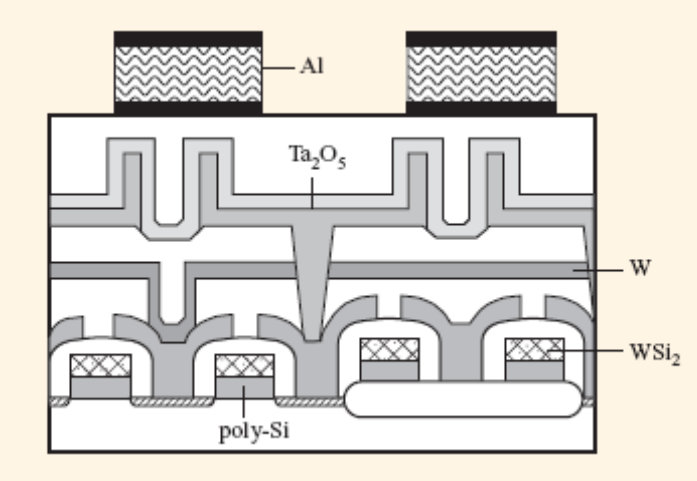


Fig. 1-1 Schematic cross section of stacked capacitor cell suitable for 0.15μm [Ref. 10].

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM 1/2 Pitch (nm)	100	90	80	70	65	57	50
DRAM cell size (μm^2)	0.082	0.065	0.048	0.036	0.028	0.019	0.015
DRAM storage cell dielectric: EOT (nm)	3.5	2.3	1.8	1.3	0.8	0.8	0.8
Generation at production	1G	1G	1G	2G	2G	4G	4G

Manufacturable solutions, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known

Table 1.1 DRAM technology requirements [Ref. 3]

	High-κ Dielectrics		
	HfO_2	ZrO_2	Al_2O_3
Bandgap (eV)	**6.02**	**5.82**	**8.3**
Barrier Height to Si (eV)	**1.6**	**1.5**	**2.9**
Dielectric Constant	**~30**	**~25**	**9**
Heat of Formation (Kcal/mol)	**271**	**261.9**	**399**
ΔG for Reduction ($MO_x + Si \rightarrow M + SiO_x$)	**47.6**	**42.3**	**64.4**
Thermal expansion coefficient (10^{-6} K^{-1})	**5.3**	**7.01**	**6.7**
Lattice Constant (Å) (5.43 Å for Si)	**5.11**	**5.1**	**4.7 - 5.2**
Oxide Diffusivity @ 950°C (cm^2/sec)		**$1x10^{-12}$**	**$5x10^{-25}$**

Table 1.2 Materials properties of high-κ dielectrics, Al_2O_3, ZrO_2, and HfO_2.

CHAPTER 2

Effects of O_3 PDA Temperature on the Properties of Ta_2O_5 Measured by COCOS Metrology

2.1 Introduction

MOS-oxide-semiconductor (MOS) devices are the most widely used devices in the semiconductor industry. For example, MOS capacitors are used as the storage elements in dynamic random access memory (DRAM) applications. While most properties are scaled down with successive generations, the DRAM bit cell capacitance must remain a relatively constant value determined by the sense amplifier operation and robustness against alpha-particle-induced soft errors. The shrinkage of bit cell area with each generation leaves us with three approaches for maintaining constant capacitance per bit: (1) reducing the thickness of the dielectric; (2) increasing the area by forming three-dimensional (3D) capacitor structures, and (3) increasing the dielectric constant through the introduction of new high-permittivity materials.

A conventional MOS device uses SiO_2 as the material for the insulator layer. The characteristics of the MOS device are dominated by the characteristic of the insulator layer. The development of high-density DRAM has been accomplished by reducing the thickness of the SiO_2 storage capacitors to maintain the required charge storage level. One of the most important features for a material to be used as the insulating dielectric in DRAM is the low leakage current. However, as the insulator thickness decreases, the SiO_2 insulator layer often fails due to electron tunneling and the leakage current problem becomes severe. Therefore,

various high dielectric constant (κ) materials have been recommended to replace SiO_2 for solving the leakage problem. If the leakage current of the high-κ material is lower than that of the conventional SiO_2 film under the same equivalent oxide thickness (EOT), it will be suitable candidate to replace the conventional oxide for DRAM application.

Currently, Ta_2O_5 thin films are considered as one of the most promising materials that can be used for high-density DRAM applications, but many electrical and physical properties of this high-κ material are still under research. Tantalum pentoxide is a potential film material because of its high dielectric constant (>22). Except to the advantage of high dielectric constant, Ta_2O_5 film also has some important advantages.

1. The dielectric constant is independent of the applied voltage.
2. Ta_2O_5 film can be easily removed by using CF_4 [16].

Tantalum pentoxide has been extensively studied by many techniques: radio-frequency [23, 24], magnetron [25, 26] or ion-beam sputtering [27], thermal oxidation, pulsed laser deposition (PLD) [28], chemical vapor deposition (CVD) [29, 30], sol-gel processing [31, 32] and anodization of thin Ta or TaN film [33].

One of the unresolved problems of Ta_2O_5 which is typical of many high-k dielectrics is the unavoidable formation of an interfacial SiO_2 layer which minimizes the interface state density and reduces the intermixing of Si and Ta_2O_5, but at the same time it decreases the global dielectric constant of the film. As a result, the obtained dielectric constant is not adequate to reach an equivalent dielectric thickness of less than 2 nm with an acceptable leakage current level, the presence of 2-nm-thick interfacial SiO_2 compromises the benefits of

Ta_2O_5 as a high-κ. Besides, as-deposited Ta_2O_5 films exhibit sufficient leakage current [18], [34]-[36] due to the organic impurities and/or oxygen vacancies. It has been known that the leakage current can be decreased by post-deposition treatment (650-800^oC) [35, 36] and ozone annealing [18], [34]. In this chapter, the effect of ozone annealing on the properties of Ta_2O_5 films grown by metal-organic chemical vapor deposition (MOCVD) was investigated.

2.2 Experiment Details

12 inch p-type (100) silicon wafers were cleaned by standard RCA processes with HF-last for the removal of the particles and native oxides. Prior to high-κ dielectrics deposition, the samples were prepared by NH_3 nitridation at 700^oC for 1 minute to generate an ultra-thin oxynitride layer (~4.5 Å). After the surface treatment, 85Å Ta_2O_5 was then deposited at 430^oC by TEL Trias^{TM} Ta_2O_5 deposition system (Fig. 2-1). Each tantalum pentoxide film was subjected to two high temperature post deposition annealing (PDA) steps. The first annealing was performed in the ozone gas ambient at temperatures ranging from 500^oC to 700^oC for 5 minutes and was called O_3 annealing. The second was done in oxygen atmosphere at 800^oC for 1 minute, and was called lamp annealing. The cross section, split conditions, and the total process flow were shown in Fig. 2-2. The physical gate oxide thickness was determined by Rudolph ellipsometer in two kinds of mode: refractive index (n) & absorption index (k) fixed and n & k opened. The electrical properties and reliability characteristics of the Ta_2O_5 films measured using SDI FAaST series tools. The dielectric constant (κ value) was extracted by non-contact dielectric capacitance data from COCOS non-contact metrology. The flat band voltage, interface trap density, and the soft breakdown trends with O_3 annealing temperature were also investigated in this chapter.

2.3 Results and Discussions

In this chapter, the effects of O_3 post deposition annealing temperature on the properties of Ta_2O_5 were investigated by COCOS non-contact metrology. The measurement methodology of COCOS technique was introduced first.

2.3.1 COCOS Non-Contact Metrology [37, 38]

COCOS (Corona Oxide Characterization of Semiconductor) metrology enables gate dielectric to be quickly monitored in a non-contact manner for all wafer sizes including 300mm. The method uses corona charging in air to deposit an electric charge on a dielectric thus charging the electric field in the dielectric and in semiconductor.

Figure 2.3 shows the measurement cycle that incorporates corona charging, shifting of the sample under the probe and the contact potential difference (CPD) measurement. A blanket of corona charge is placed on SiO_2 by passing the wafer under a corona wire. Charge uniformity and dose control is achieved with a combination of the wafer translation and rotation.

An energy band diagram of the silicon with SiO_2 film is given in Fig. 2.4. The reference metal electrode is separated from the top SiO_2 surface by about 1mm. The electric field between the electrode and the wafer is compensated by a bias opposite in sign but equal in value to V_{CPD}. V_{CPD} is determined by the work function difference between the reference electrode and the measured wafer; the potential drop across the oxide V_{ox}, and also due to a modified value of semiconductor surface barrier, V_{SB}.

$$V_{CPD} = \Phi_{ms} + V_{SB} + V_{ox} \qquad (2\text{-}1)$$

The COCOS technique can also be used to determine dielectric capacitance. The corona charge deposited on the surface of an oxide changes the voltage drop across the oxide where the capacitance of the oxide is:

$$C_{ox} = \frac{\Delta Q_c}{\Delta V_{ox}} \qquad (2\text{-}2)$$

The flat band voltage condition is obtained by placing the corona charge of appropriate polarity until all oxide charge becomes compensated and V_{SB}=0. Illumination of silicon under the CPD probe reduces V_{SB}, but it does not affect V_{ox}. For depletion type surface barrier, it is relatively easy to flatten the surface barrier completely and to obtain V_{SB}≈0. So the flat band voltage is considered to be the V_{CPD} value when the difference between the V_{CPD} curves in the dark and under illumination is zero.

$$V_{FB} = V_{CPD}^{dark} = V_{CPD}^{light} \qquad (2\text{-}3)$$

Another very important dielectric parameter determined by COCOS technique is Q_{TOT}. Q_{TOT} is the total charge state of the oxide/semiconductor system necessary to achieve the flat band condition. From Q_{TOT} measurement, the charges need to compensate the interface trapped charge at flat band Q_{it}^{FB} and the oxide charge Q_{ox} could be determined.

$$Q_{TOT} = Q_{ox} + Q_{it}^{FB} + Q_{surf} \qquad (2\text{-}4)$$

The density of the interface traps, D_{it}, is calculated as a ratio $\Delta Q_{it}/\Delta V_{SB}$ where ΔV_{SB} is the change in the surface barrier due to deposited quantum of corona charge. It can be seen from the relationship that the interface trap charges, ΔQ_{it}, corresponding to a given quantum of corona charge: $\Delta Q_{it} = \Delta Q_c - \Delta Q_{sc}$. The interface trap was manifested by the plateau on the V_{SB} vs. corona dose curve. A D_{it} spectrum across the band gap can be obtained by plotting D_{it} versus V_{SB}.

The last parameter that can be extracted from COCOS method is the soft breakdown

field. Positive corona charge on the top oxide surface is used to increase the electric field in the oxide, which lowers the oxide conduction band. Once the Fowler-Nordheim (F-N) tunneling takes place the electron tunneling current compensates the corona ionic current i.e .$J_{F\text{-}N} = J_{corona}$. Subsequent measurement of the oxide voltage (i.e. the CPD value) corrected for the surface barrier gives the value of the (F-N) tunneling threshold and provides a measure of the oxide soft breakdown.

2.3.2 Investigation of O_3 Annealing Effect on the Ta_2O_5 Films

Fig. 2-5(a) compared the physical Ta_2O_5 film thickness as a function of O_3 annealing temperature determined by Rudolph ellipsometer in n & k opened mode. The dielectric thickness was increased as raising annealing temperature, which could be ascribed to the thick interfacial layer (IL) growth. The corresponding refractive index of the Ta_2O_5 films was shown in Fig. 2-5 (b). The decreasing of the refractive index was due to the increasing of the film thickness. It should be note that the n & k fixed mode results was the same for four times measurement while n & k opened mode had a little variation which could response for real thickness.

The dielectric capacitance of the Ta_2O_5 films as a function of PDA temperature was indicated in Fig. 2-6 (a). A lower κ-value interfacial layer in series would reduce the dielectric capacitance. Figure 2-6 (b) presented the effective dielectric constant (κ) calculated from the capacitance.

$$\kappa = \frac{C_{ox} \times T_{Ta_2O_5}}{\varepsilon_0} \qquad (2\text{-}5)$$

The decrease of the effective dielectric constant is essentially consistent with the increase of interfacial layer thickness caused by high temperature O_3 annealing.

The V_{CPD} in the dark and under illumination was systematically measured after incremental corona charging and a V_{CPD} versus corona charge (Q_c) plot was generated as shown in Fig. 2-7 for different O_3 annealing conditions. The flat band voltage (V_{FB}) was considered to the point of intersection between the V_{CPD} curves in the dark and under illumination. Figure 2-8 illustrated the flat band voltage shift and the total charge to flat band (Q_{TOT}) as a function of arising annealing temperature. For the as-deposited condition, the V_{FB} shift toward positive direction indicated electron trapping occurred. After O_3 annealing the flat band voltage shift changed to negative, this meant that the ozone annealing on Ta_2O_5 reduced the number of electron traps and increased the number of hole traps existing in the film. Furthermore, the Q_{TOT} decreased as rising the O_3 annealing temperature. Previous studies [18], [34], [39] suggest that reactive oxygen species such as ozone effectively reduce the density of oxygen vacancies in non-treated Ta_2O_5 films and suppress the leakage current. Furthermore, ozone treatment changes a structural parameter such as the Ta-O bonding length of Ta_2O_5 [40]. It is considered that the reduction of electron traps and the generation of hole traps by the ozone annealing is related to the change of stoichiometry of Ta_2O_5 from oxygen-deficient to oxygen-abundant, or to the change in the Ta-O bonding length. Figure 2-9 was the full mapping of the flat band voltage, it could be seen that the uniformity increased as arising annealing temperature.

The interface trap was manifested by the plateau on the V_{SB} vs. corona dose curve as in Fig. 2-10. A D_{it} spectrum across the band gap can be obtained by plotting D_{it} versus V_{SB} as shown in Fig. 2-11. Figures 2-12 and 2-13 compared the amount and the full mapping of interface trap densities as increasing the O_3 annealing temperature, respectively. It had been supposed that high temperature ozone annealing could fix the dangling bond at the interface of Si/Ta_2O_5 proceed to minimize the interface trap density and improve the uniformity.

Figure 2-14 compared the soft breakdown field with and without corona temperature

stress (CTS) at 170°C for 5 minutes. The soft breakdown field was defined as the onset of the Fowler-Nordheim tunneling from the silicon to the dielectric. The difference of the field was due to sub-tunneling leakage current through the Ta_2O_5. The Weibull distributions of soft breakdown fields for the samples were shown in Fig. 2-15. Non-uniform interfacial layer oxidation after O_3 annealing was supposed to cause the increasing of the field strength and break the distribution. This tendency could be seen in the full mapping of the soft breakdown field displayed in Figs. 2-16 and 2-17.

2.4 Summary

In this chapter, the effects of O_3 post deposition annealing temperature on the properties of Ta_2O_5 were investigated by COCOS non-contact metrology. The dielectric thickness was increased as raising annealing temperature, which could be ascribed to the thick interfacial layer (IL) growth. A lower κ-value interfacial layer in series would reduce the dielectric capacitance after high temperature annealing. Moreover, the flat band voltage shift changed from positive to negative due to the electron traps elimination and partially hole traps generation in the film. It had been supposed that high temperature ozone annealing could compensate the dangling bond at the interface of Si/Ta_2O_5 proceed to minimize the interface trap density and improve the uniformity. Non-uniform interfacial layer oxidation after O_3 annealing was supposed to cause the increasing of the field strength and break the the soft breakdown distribution.

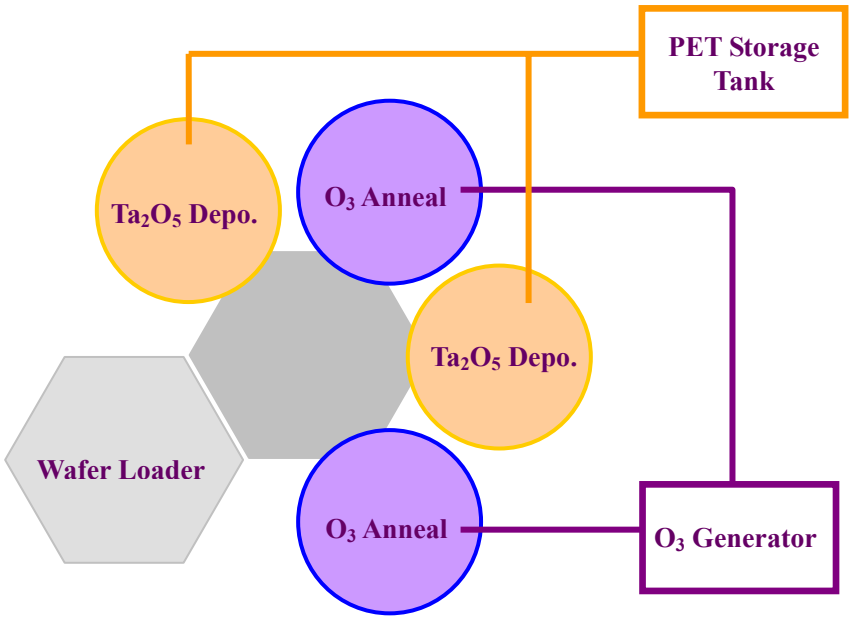
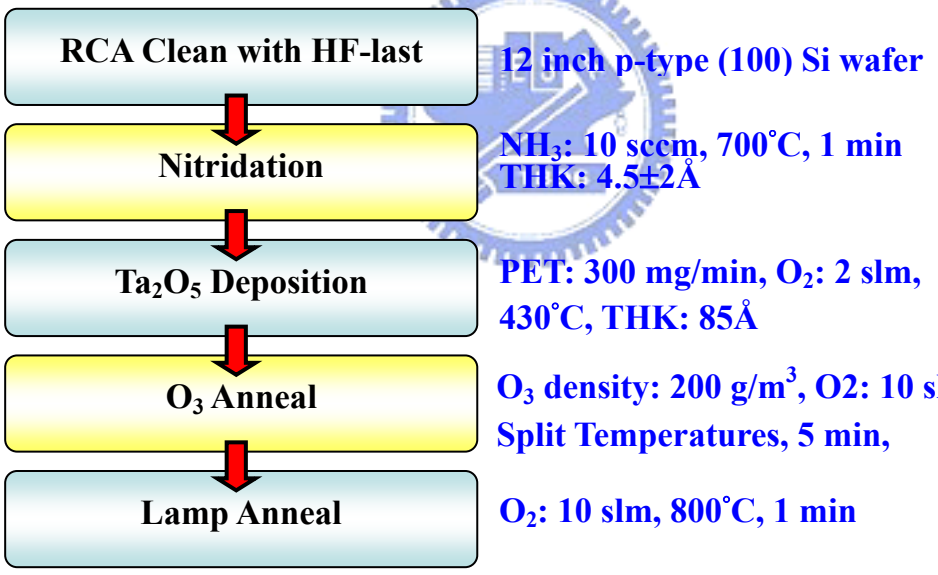
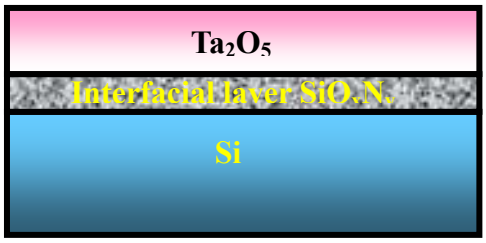


Fig. 2-1 PSC TEL Trias^{TM} Ta_2O_5 deposition system.





	Density (g/cm^3)	Temperature (℃)	Time (min)	Pressure (torr)
1		As - deposit		
2		500		
3		550		
4		600		
5		650		
6		700		

Fig. 2-2 Ta_2O_5 films process flow, device cross section and split conditions.

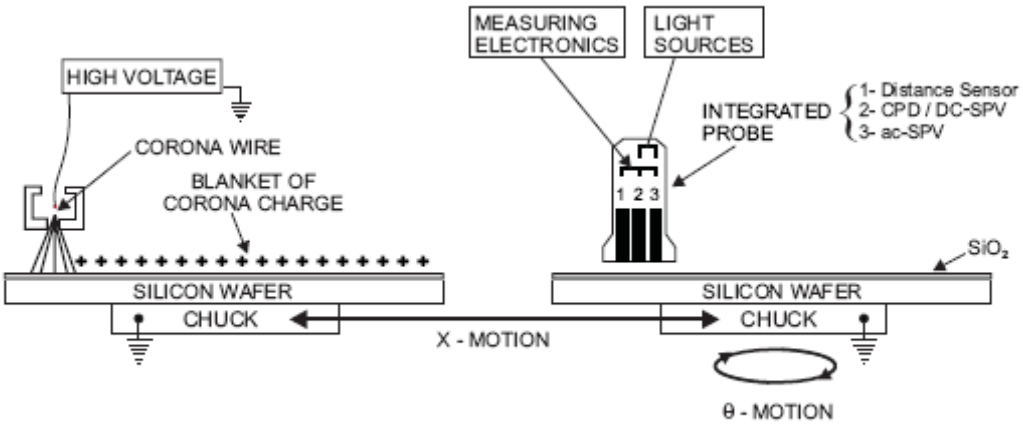
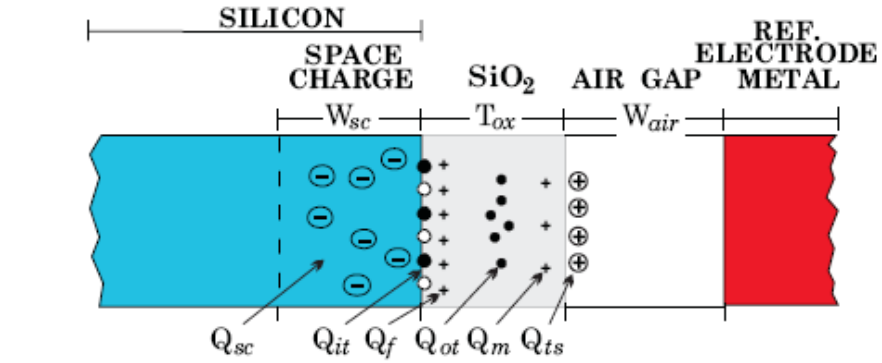
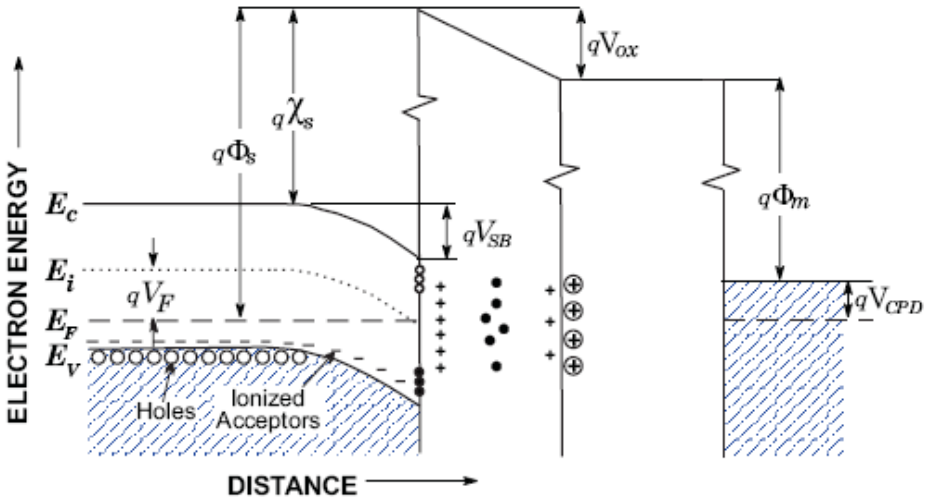


Fig. 2-3 Arrangement for corona charging and measurement used in SDI COCOS metrology [Ref. 37].



Q_{sc} Space Charge
Q_{it} Interface Trap Charge
Q_f Oxide Fixed Charge
Q_{ot} Oxide Trapped Charge
Q_m Mobile Ionic Charge
Q_{ts} Top Surface Charge

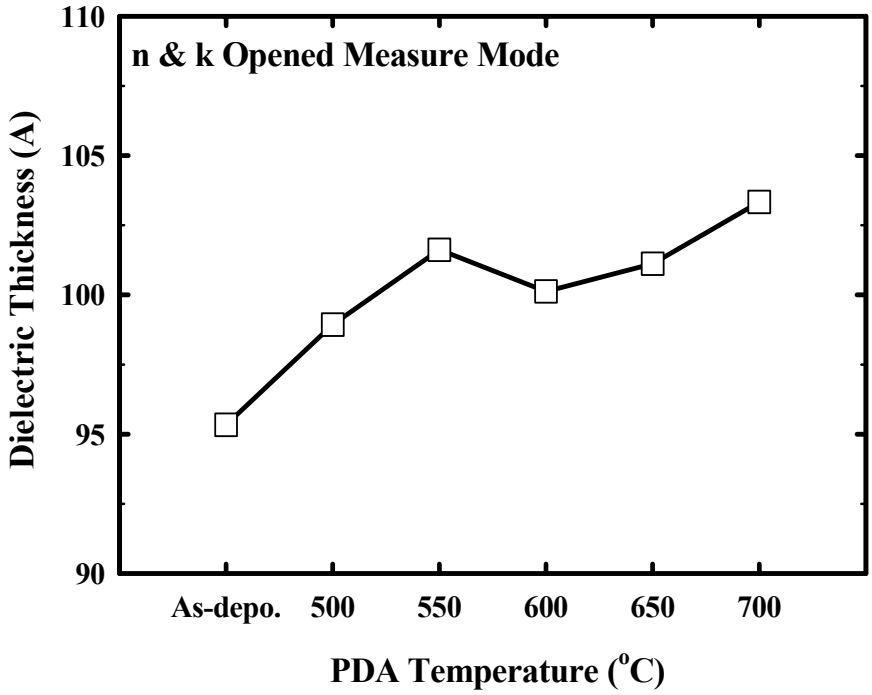


$$V_{CPD} = \Phi^{\circ}_{ms} + V_{SB} + V_{ox}$$

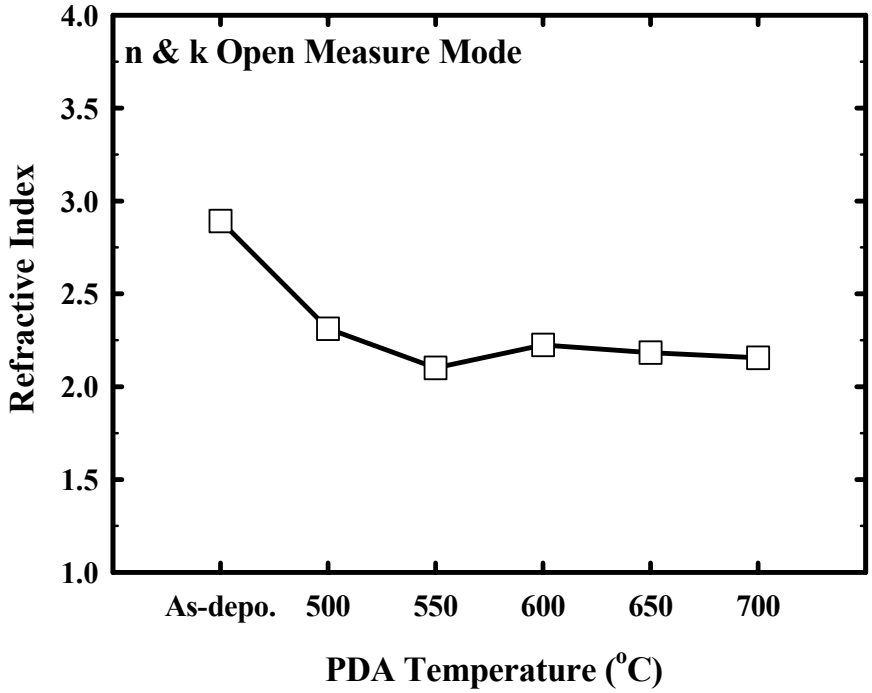
$$\Phi^{\circ}_{ms} = \Phi_m - (\chi_s + \frac{E_g}{2} + V_F)$$

E_c Conduction Band Energy
E_i Intrinsic Energy
E_F Fermi Energy
E_V Valence Band Energy
$q\Phi_s$ Semiconductor Work Function
$q\Phi_m$ Work Function of Ref. Electrode
$q\chi_s$ Semiconductor Electron Affinity
V_F Bulk Fermi Potential
V_{SB} Semiconductor Surface Barrier
V_{ox} Oxide Voltage

Fig. 2-4 Surface band diagram for Si/SiO_2 system with a CPD reference electrode [Ref. 37].



(a)



(b)

Fig. 2-5 (a) The physical Ta_2O_5 film thickness as a function of O_3 annealing temperature determined by Rudolph ellipsometer in n & k opened mode. (b) The corresponding refractive index of the Ta_2O_5 films.

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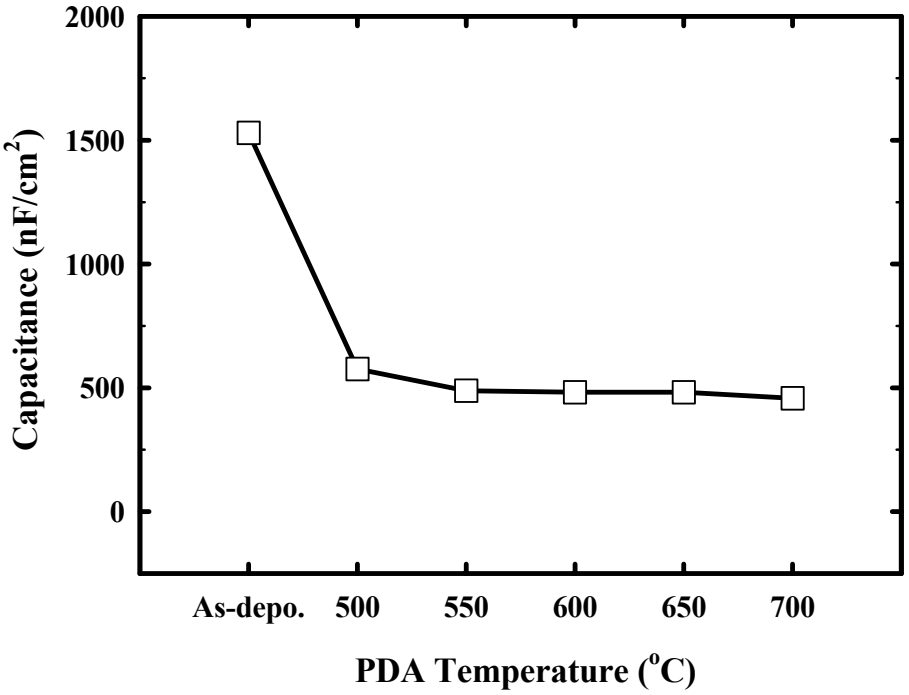
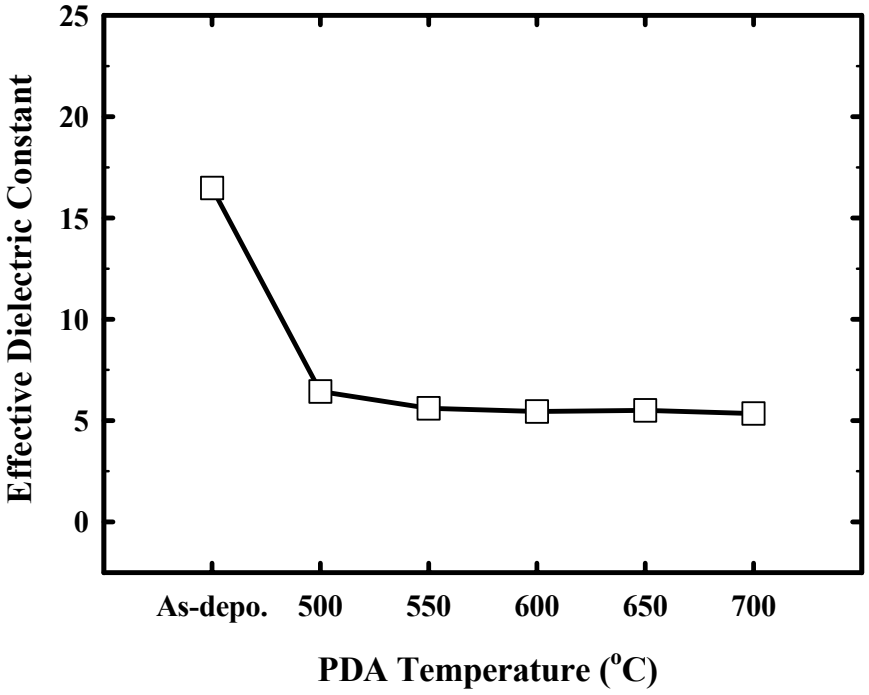
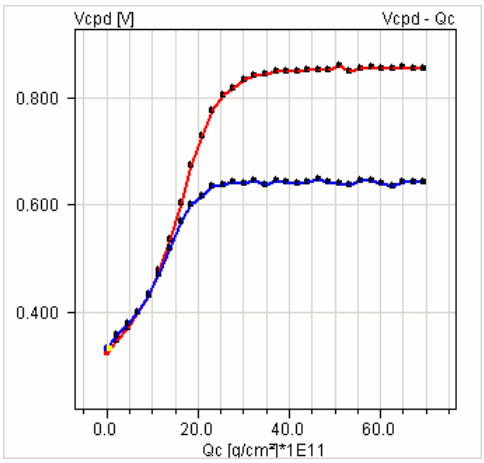


(a)

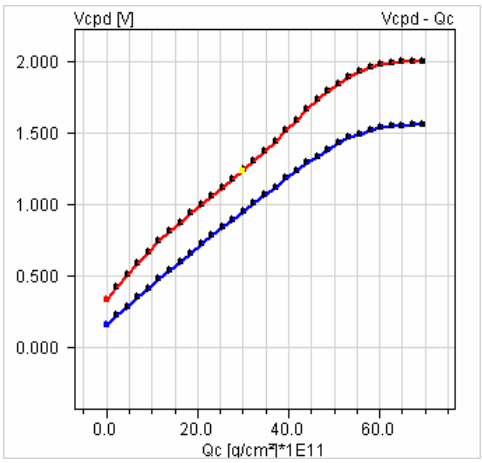


(b)

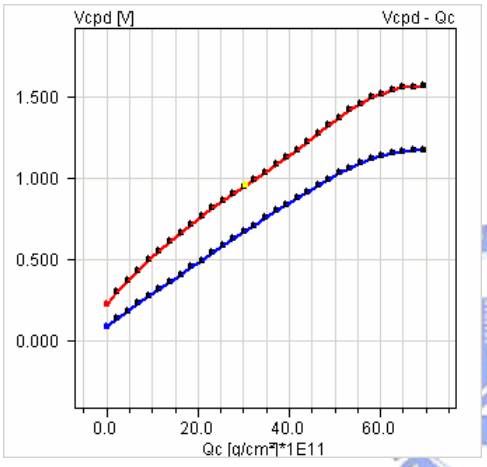
Fig. 2-6 (a) The dielectric capacitance (b) the effective dielectric constant (κ) of the Ta_2O_5 films as a function of PDA temperature.



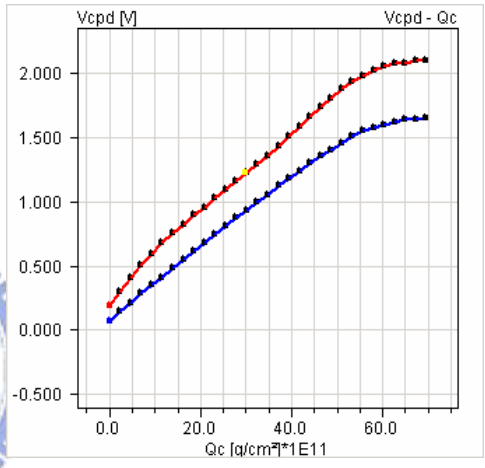
(a) As-depo.



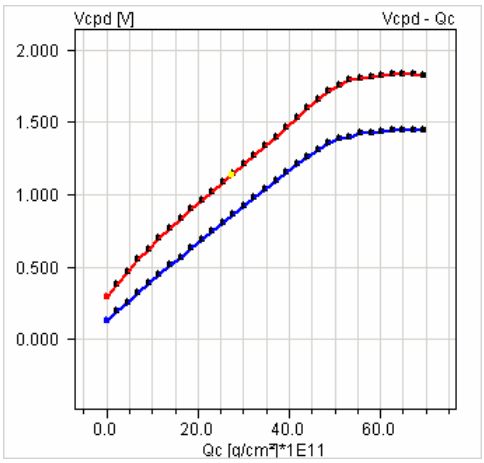
(d) 600°C



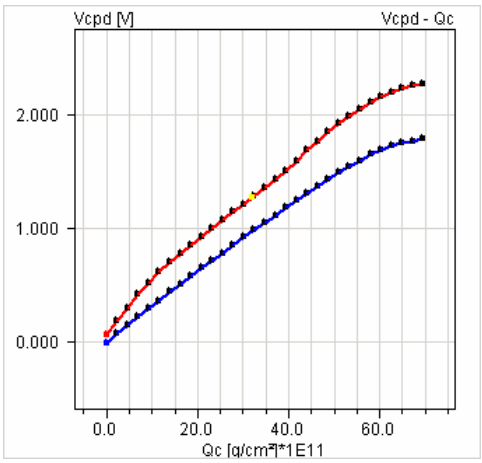
(b) 500°C



(e) 650°C

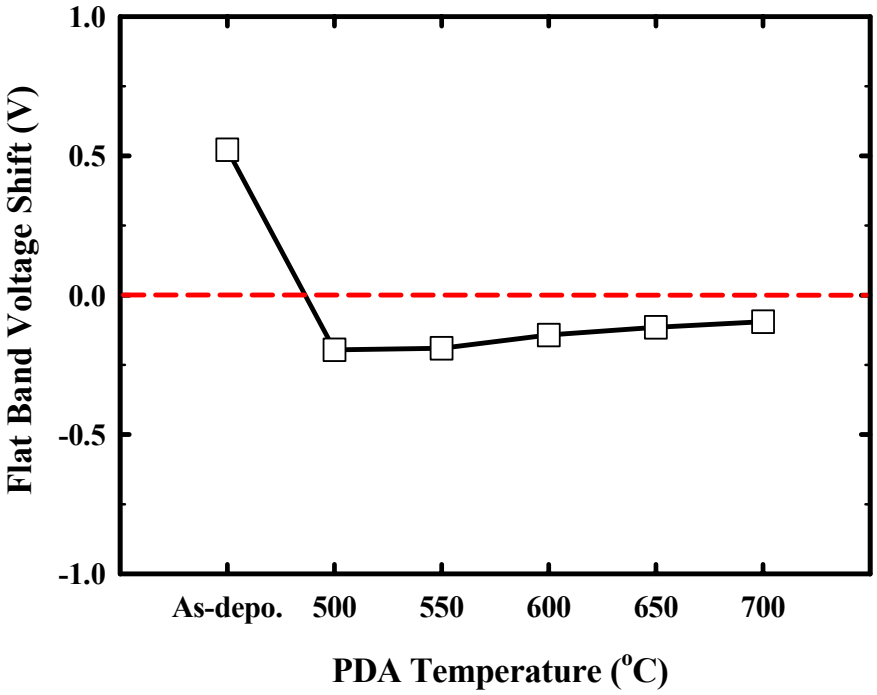


(c) 550°C

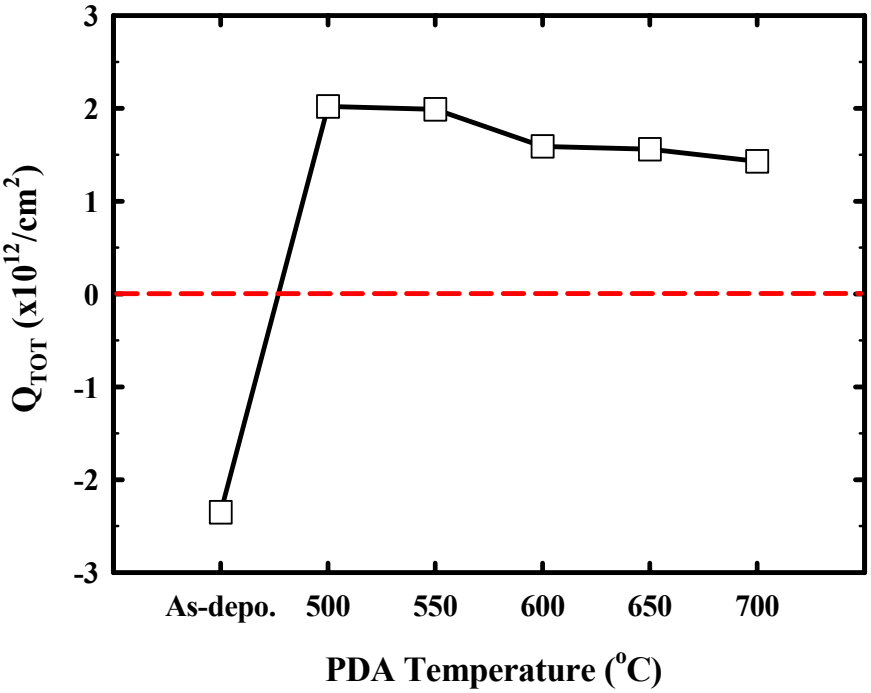


(f) 700°C

Fig. 2-7 (a) ~ (f) Contact potential difference versus corona charge plot illustrating the determination of flat band voltage. Red line was the V_{CDP} in the dark and the blue one showed the V_{CPD} under illumination.



(a)



(b)

Fig. 2-8 (a) The flat band voltage shift (V_{FB}) and (b) the total charge to flat band (Q_{TOT}) as a function of arising annealing temperature.

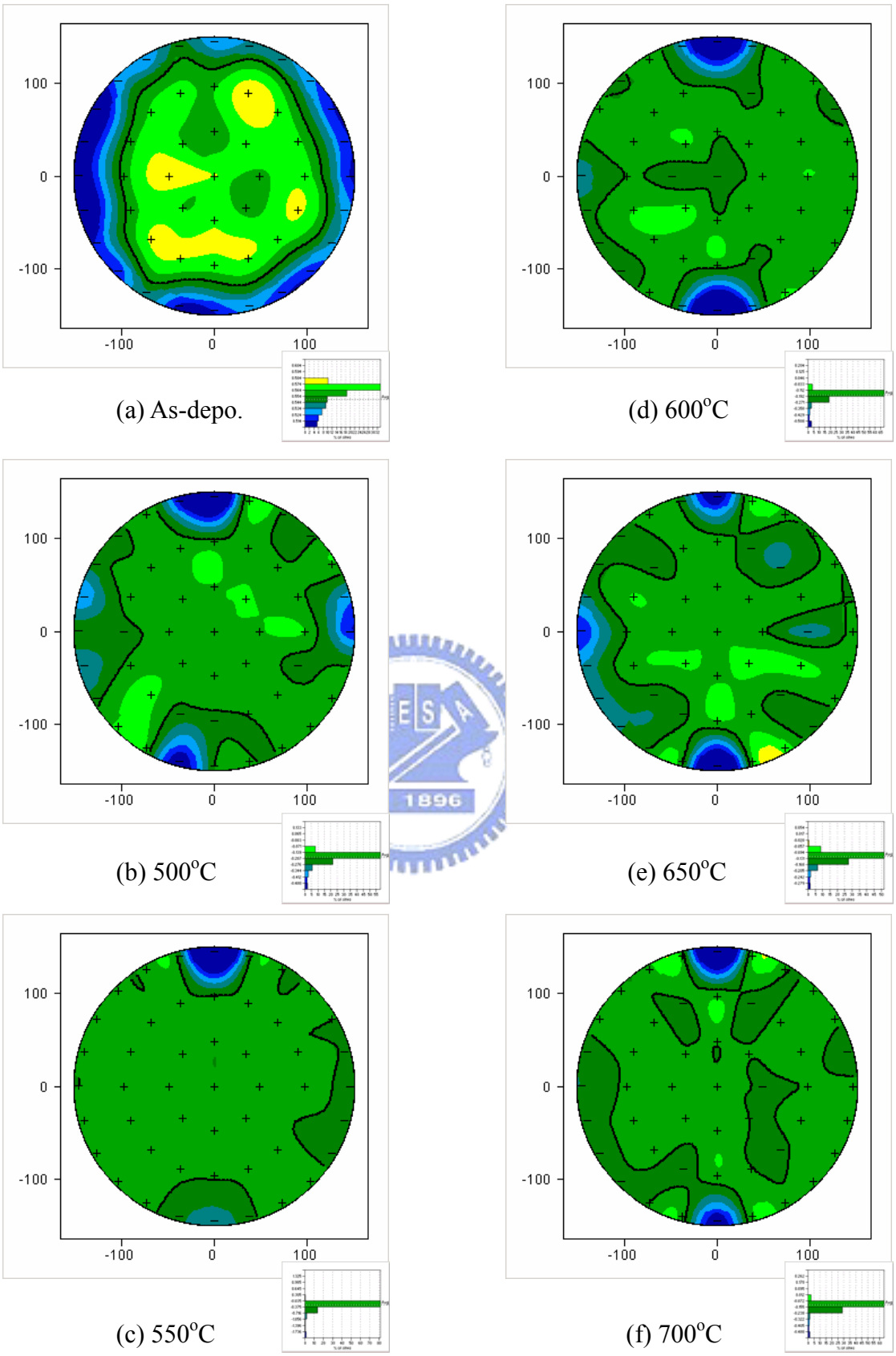
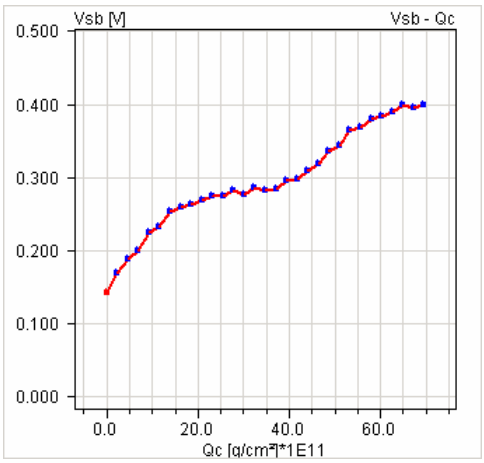
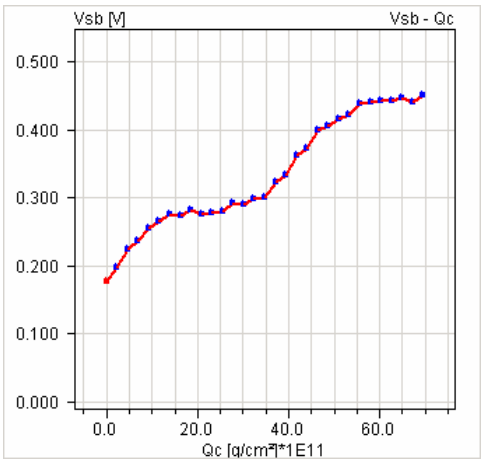


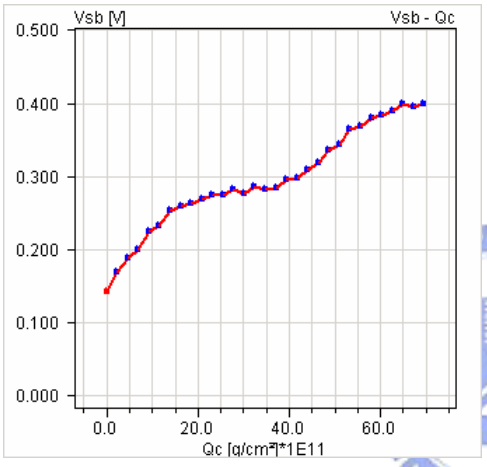
Fig. 2-9 The full mapping of the flat band voltage.



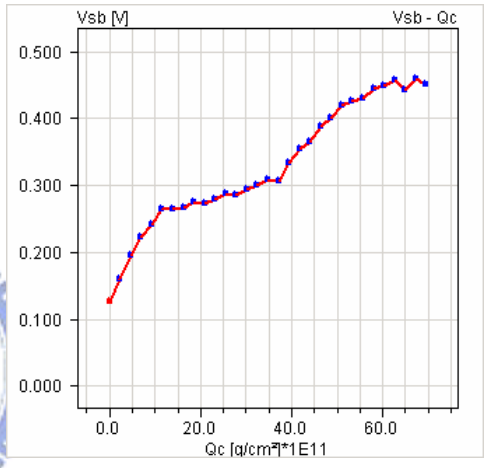
(a) As-depo.



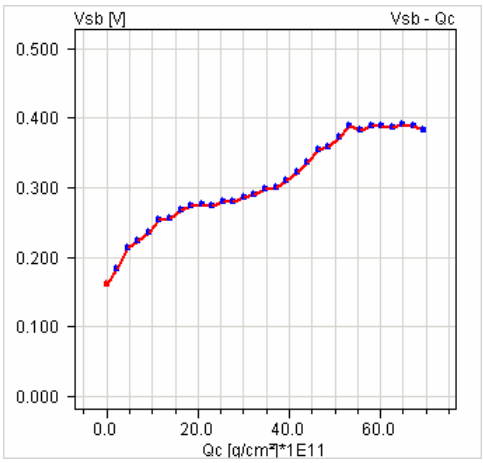
(d) 600°C



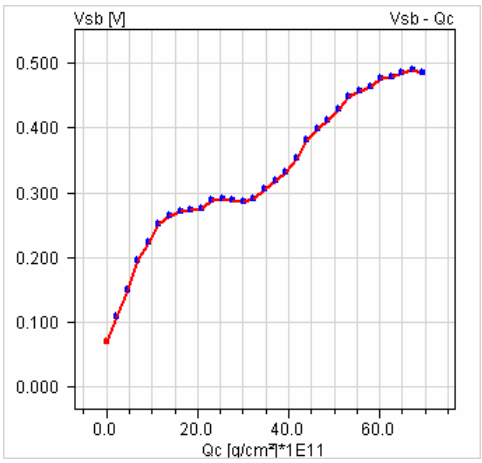
(b) 500°C



(e) 650°C

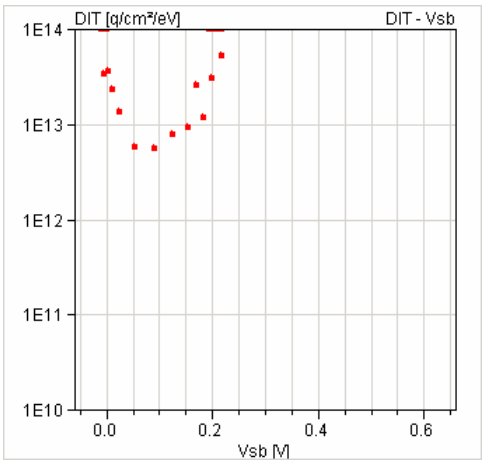


(c) 550°C

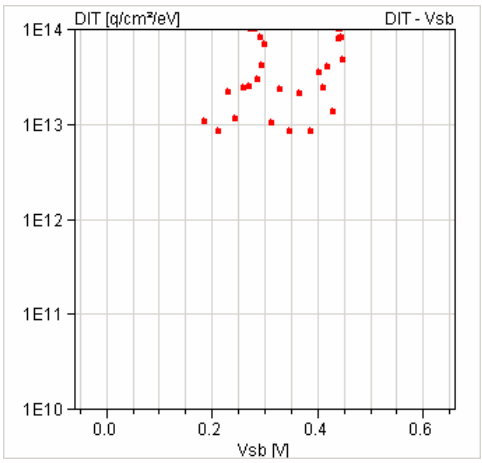


(f) 700°C

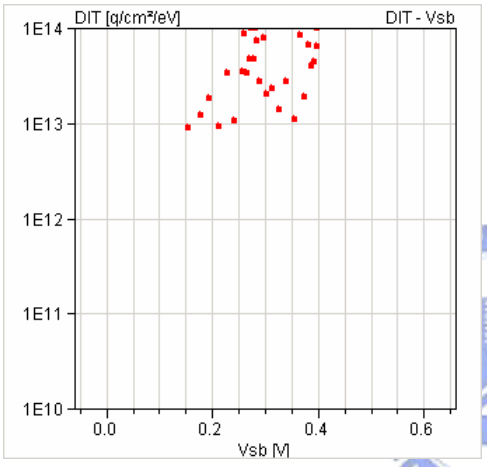
Fig. 2-10 The interface trap was manifested by the plateau on the V_{SB} vs. corona dose curve.



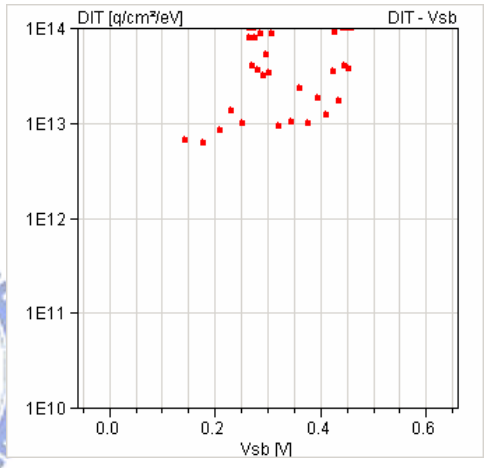
(a) As-depo.



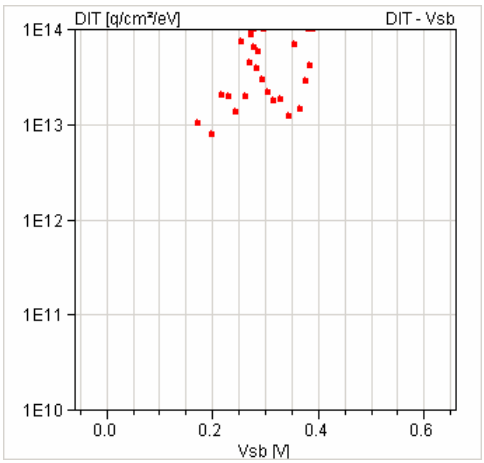
(d) 600°C



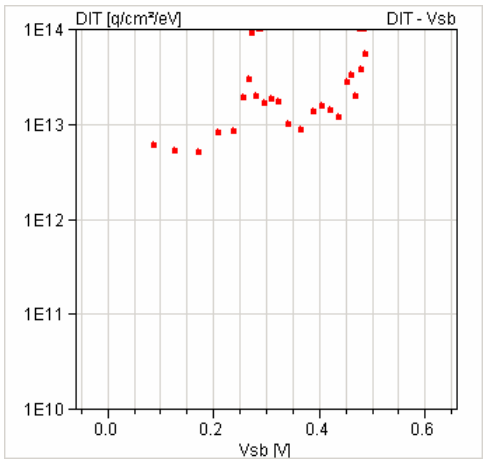
(b) 500°C



(e) 650°C



(c) 550°C



(f) 700°C

Fig. 2-11 A D_{it} spectrum across the band gap obtained by plotting D_{it} versus V_{SB}.

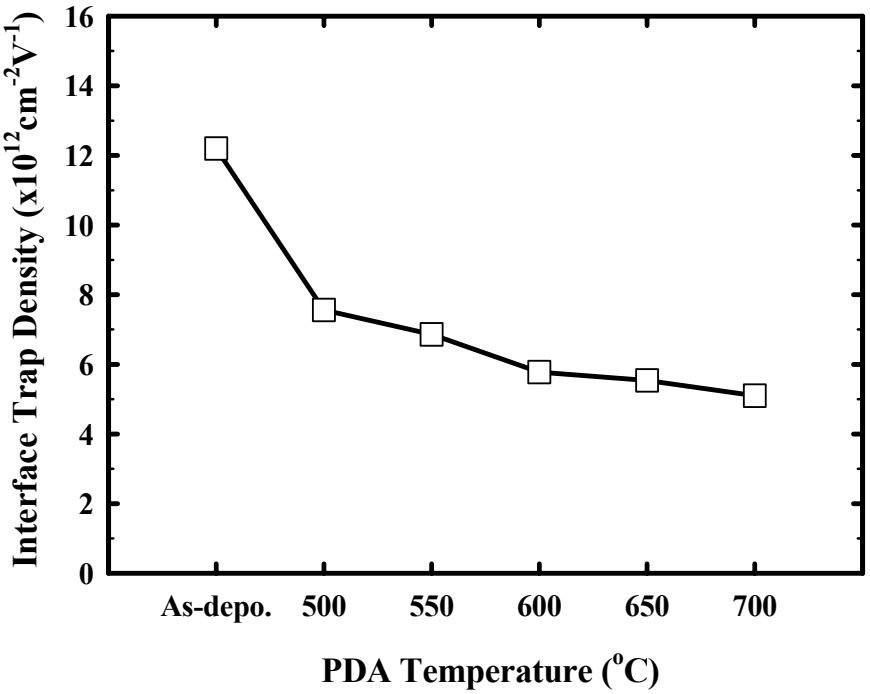


Fig. 2-12 Comparison the amount of interface trap densities as increasing the O_3 annealing temperature.

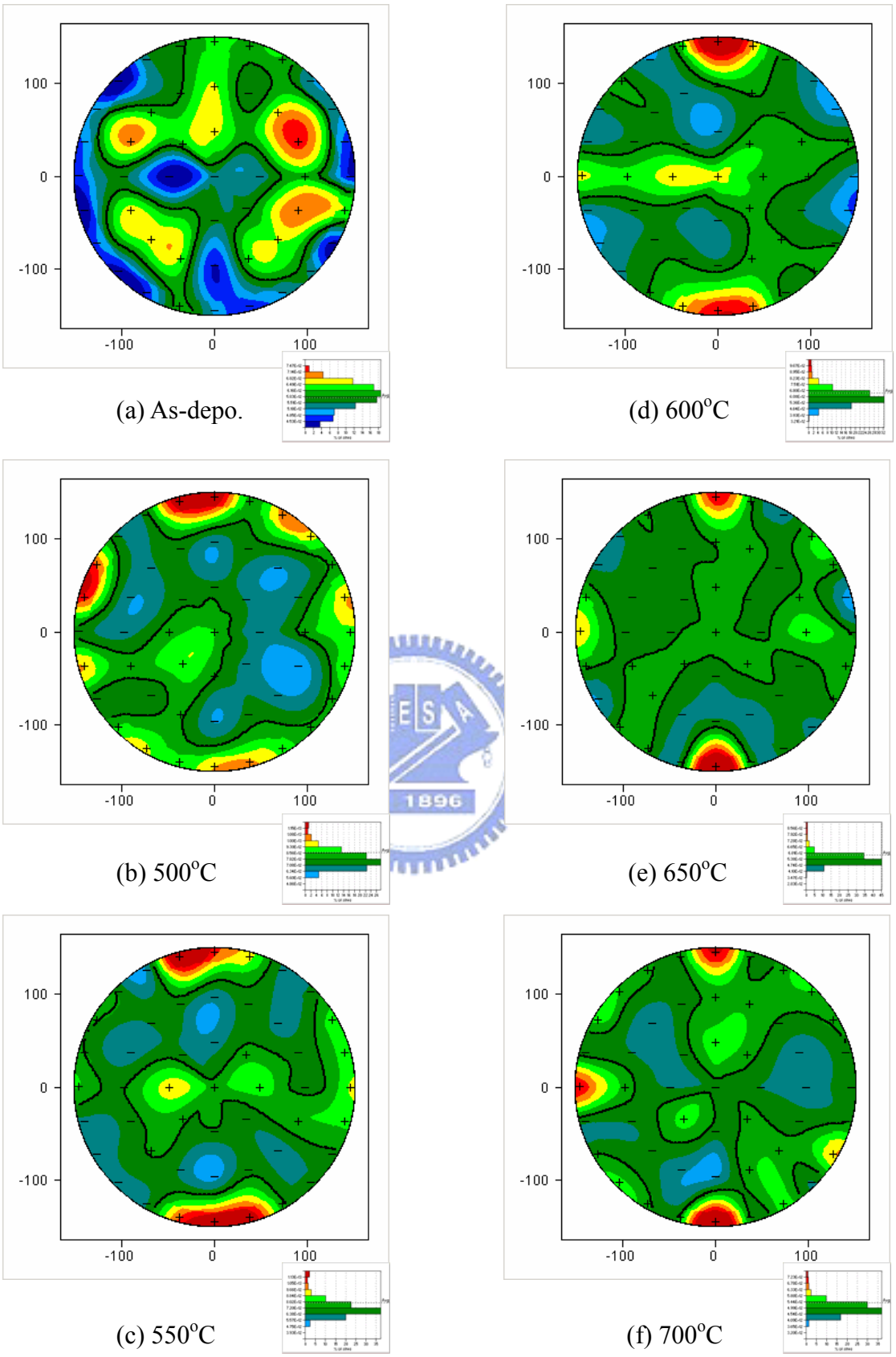


Fig. 2-13 The full mapping of the interface trap density.

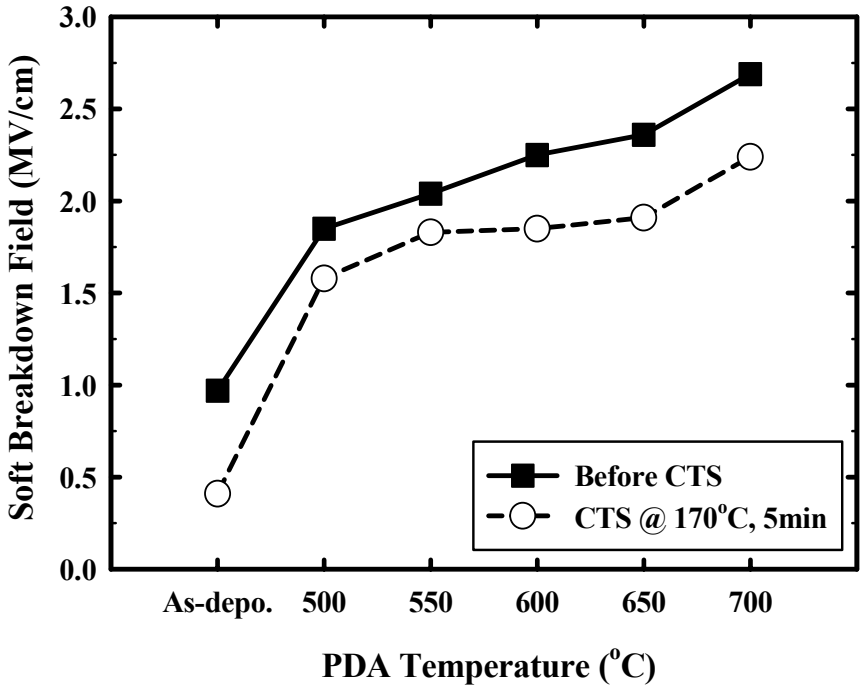
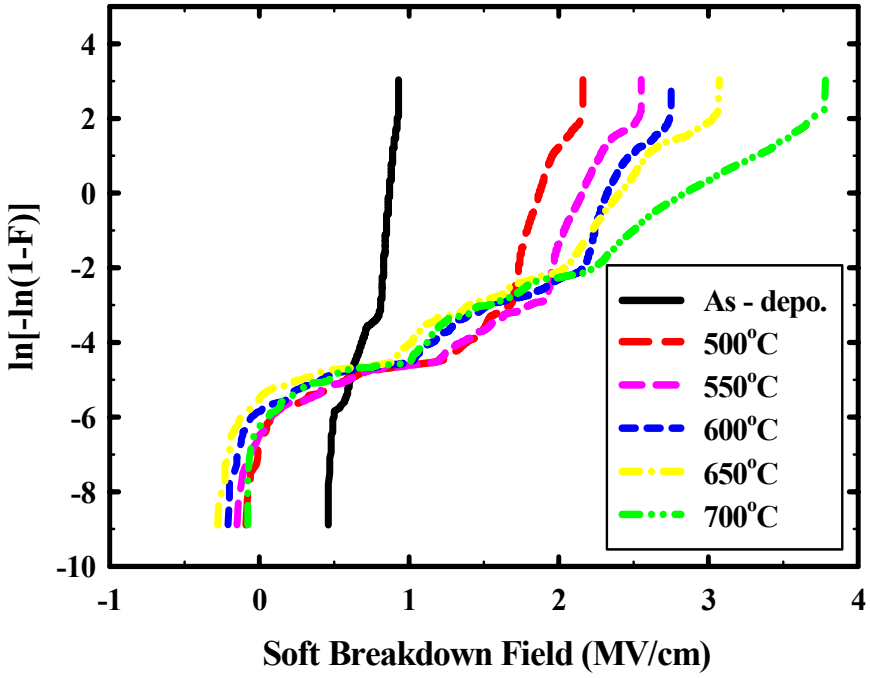
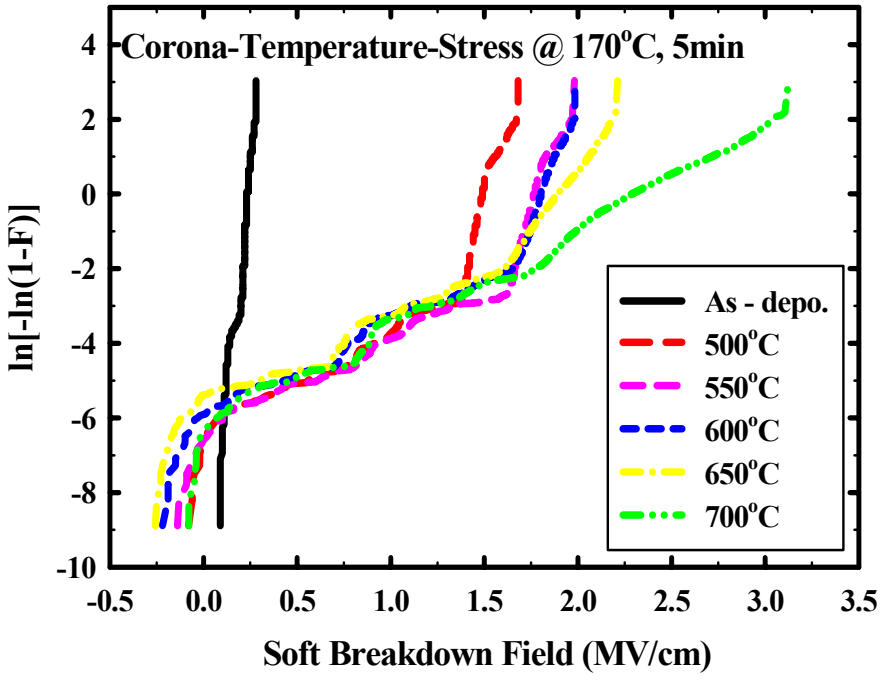


Fig. 2-14 Soft breakdown field variation with and without corona temperature stress (CTS) at 170°C for 5 minutes.

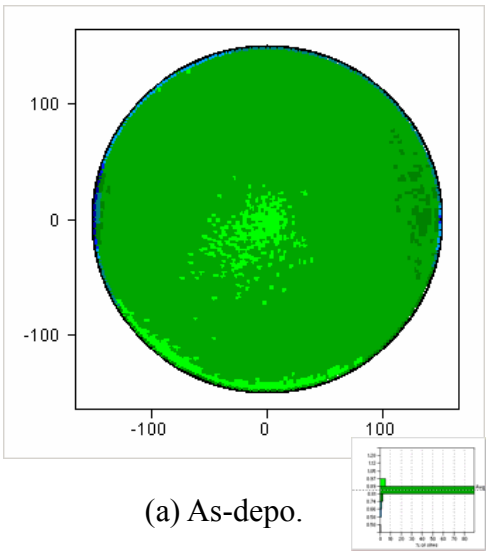


(a)

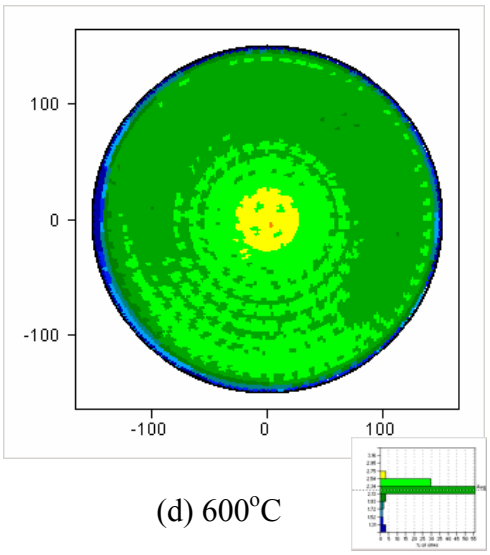


(b)

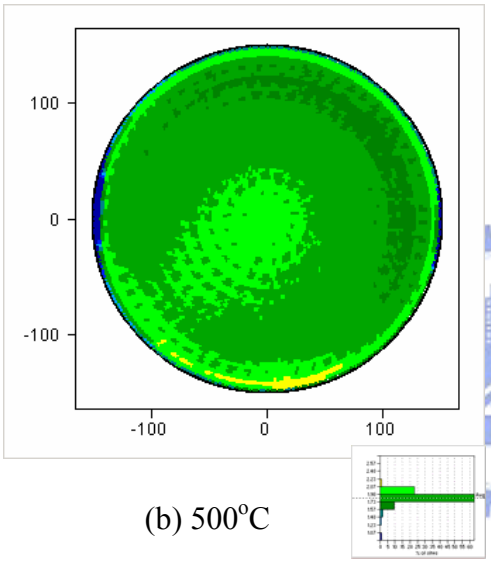
Fig. 2-15 The Weibull distributions of soft breakdown fields (a) without and (b) with corona temperature stress (CTS) at 170°C for 5 minutes.



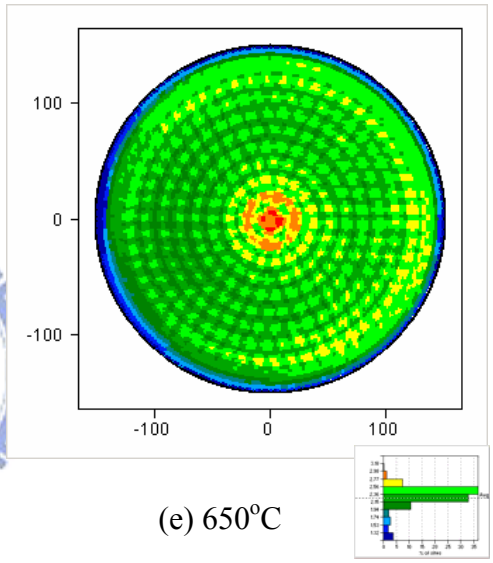
(a) As-depo.



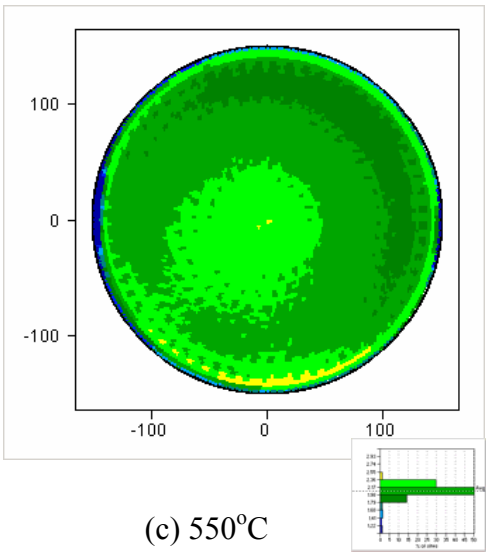
(d) 600°C



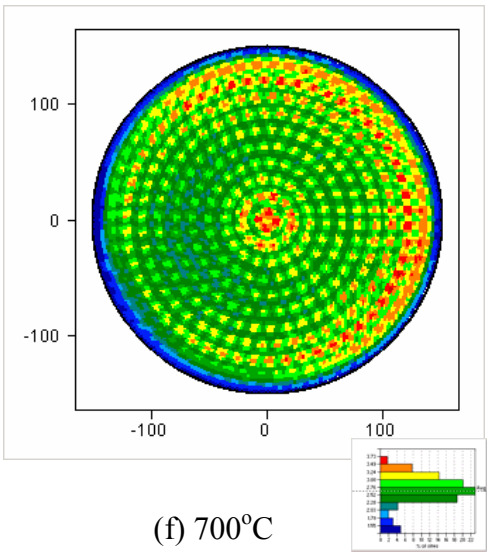
(b) 500°C



(e) 650°C



(c) 550°C



(f) 700°C

Fig. 2-16 The full mapping of the soft breakdown field.

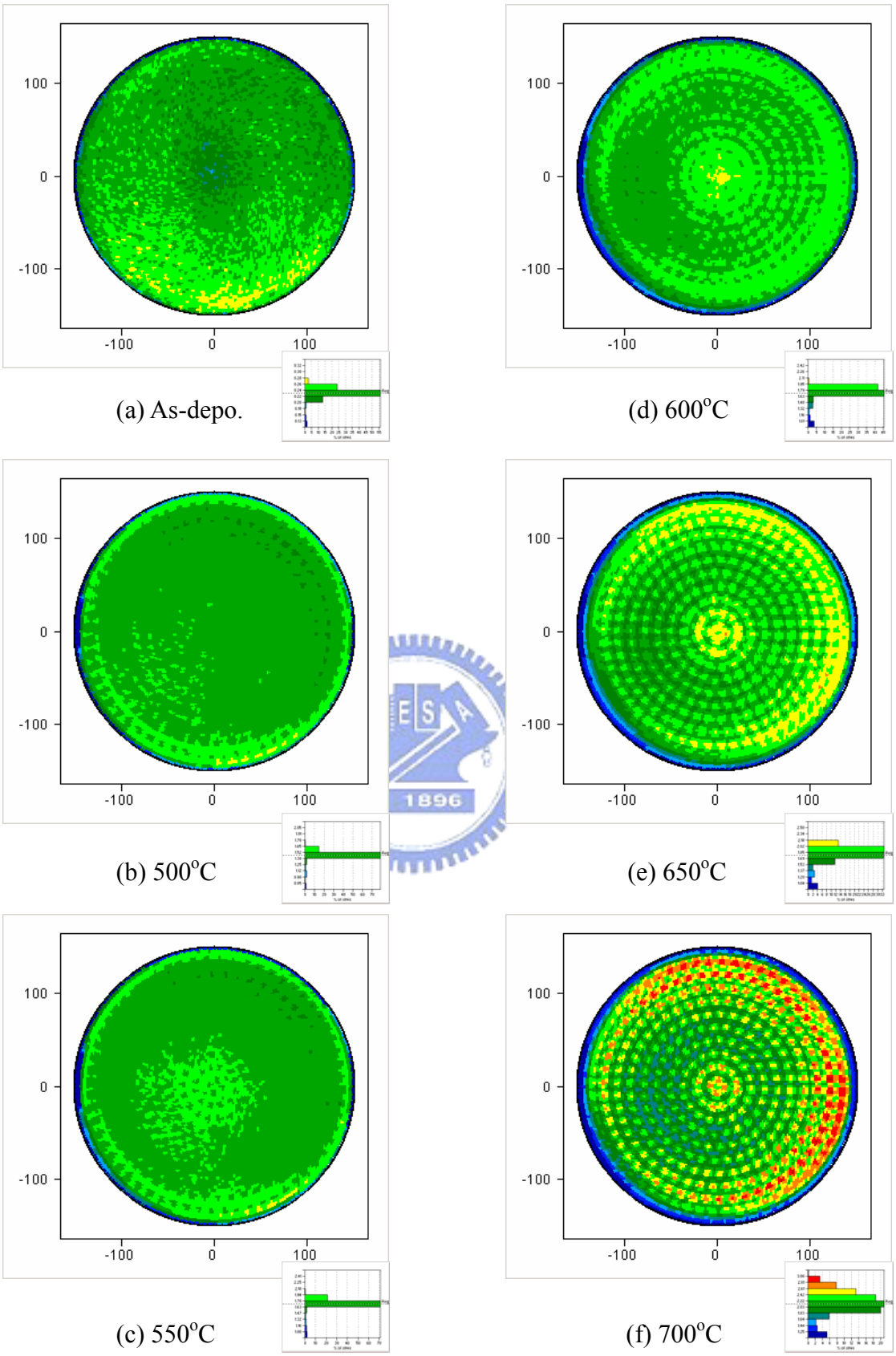


Fig. 2-17 The full mapping of the soft breakdown field during corona temperature stress (CTS) at 170°C for 5 minutes.

CHAPTER 3

Ozone Surface Treatment on the Characteristics and Reliabilities of HfO_2 MOS Devices

3.1 Introduction

The shrinkage in metal-oxide-semiconductor field effect transistor dimensions is accompanied by a scaling of gate oxide thickness. It is well known that the scaling of conventional SiO_2 is approaching the predicted limit due to large direct tunneling leakage current, thereby presenting a fundamental challenge to continual scaling [3]. Therefore, an alternative gate dielectric material is needed to replace SiO_2. High-κ dielectrics, such as HfO_2, are the potential candidates because a thicker film is utilized to reduce the direct tunneling leakage current while maintaining the same gate capacitance [41]-[44]. However, the control of SiO_2-like interface between high-κ dielectrics and silicon substrate pays more and more important, since the device performances and reliability characteristics are strongly affected by the interface quality [44]. Nitridation of the Si surface using NH_3 prior to the deposition of high-κ gate dielectrics has been shown to be effective in achieving the low EOT (equivalent oxide thickness) and preventing boron penetration [45, 46]. However this technique results in higher interface charges [47], which leads to higher hysteresis and reduced channel mobility. Ozone-formed oxide (ozone oxide) has superior characteristics. Even when the formation temperature is less then 400°C, ozone oxide has a high film density comparable to that of the device-grade oxide film formed at higher temperature (e.g. 900°C) [48], a low interface trap density ($D_{it} \sim 10^{10}$ cm^2) [49], and a much thinner structural transition layer near the SiO_2/Si

interface[48], [50]. The aim of this experiment was to investigate the interfacial issues at HfO_2/silicon interface. The ozone surface treatment was employed to improve the interface quality between HfO_2 and silicon substrate. Moreover, the rapid thermal oxidation (RTO) and the ammonia (NH_3) surface treatment were also investigated as the reference in this thesis.

3.2 Experiment Details

3.2.1 Experiment Details of Ozone Oxide Growth

6 inch p-type (100) silicon wafers were cleaned by standard RCA processes with HF-last for the removal of the particles and native oxides. Figure 3-1 showed the schematic diagram of ozone water system. The ozone generator (AnserosPAP-2000) decomposed the oxygen molecular to generate ozone gas by high electrical field. The ozone gas was mixed with DI water in the dissolve unit and then pumped into the tank of wet bench. By changing the oxygen flow, DI water flux, and ozone generation power, the ozone concentration in the DI water could be adjusted. Ozone oxide was grown by immersing the Si wafer into the ozone water at room temperature. The relationship between the ozone concentration in the DI water and thickness change of ozone oxide was under investigation. Ellipsometer was utilized to measure the thickness and the etching rate in the hydrofluoboric acid (HF) of ozone oxide. The micro-roughness of the wafer surface and the interface between ozone oxide/silicon were detected by atomic force microscopy (AFM).

3.2.2 Process Flow of HfO_2 MOS Devices with Surface Treatments

LOCOS isolated MOS capacitors were fabricated on 6 inch p-type (100) silicon wafers.

After forming LOCOS isolation, wafers were cleaned by standard RCA processes with HF-last. Prior to high-κ dielectrics deposition, the samples were prepared either by Ozone, NH_3 or RTO. Diluted ozone water (2ppm) was used to grow an ultra-thin ozone oxide about 7~8Å (measured by ellipsometer). NH_3 nitridation was performed in a high temperature furnace at 800°C for 1 hour to generate an ultra-thin oxynitride layer (~7 Å). RTO was also intended to deposit a thin SiO_2 layer (~8Å), at 800°C using a rapid thermal process system for 30 seconds. After one of the surface treatments, 50Å HfO_2 was then deposited at 500°C by MOCVD system, as shown in Fig. 3-2, followed by a high temperature post deposition annealing (PDA) at 600°C in the nitrogen ambient for 30 seconds. Aluminum metal served as the gate electrode was created by a thermal evaporation system. After gate electrodes patterned and contact holes etched, backside contact was formed. The cross section and the total process flow were shown in Fig. 3-3. Square capacitors of 1×10^{-4} cm^2 areas with LOCOS isolation are used to evaluate the gate oxide integrity. The equivalent oxide thickness (EOT) was extracted by fitting the measured high-frequency (10 kHz) capacitance-voltage (*C-V*) data from Hewlett-Packard (HP) 4284 LCR meter under accumulation condition. UCLA CVC simulation program was utilized to obtain the accurate flat band voltage (V_{FB}). The *C-V* hysteresis phenomenon was measured by sweeping the gate voltage from accumulation to inversion then back. The tunneling leakage current density-electric field (*J-E*) and the reliability characteristics of MOS capacitors were measured by semiconductor parameter analyzer HP 4156C.

3.3 Results and Discussions

In this chapter, the influences of surface treatments prior to hafnium oxide (HfO_2)

deposition were investigated. Comparisons between various surface treatments, including: ozone water oxidation (Ozone), rapid thermal oxidation (RTO) and ammonia (NH_3) nitridation were studied.

3.3.1 Basic Property Investigation of the Ozone Oxide

The growth curves of ozone oxide as a function of ozone water concentration were shown in Fig. 3-4. The growth rate was increased as raising the ozone quantity contained in DI water from 1ppm to 10ppm. A saturated oxidation was observed in the growth curves and the resultant self-limiting property could improve the thickness uniformity after furnace or/and rapid thermal oxidation.

Figure 3-5 compared the etching rate in diluted HF solution between ozone oxide and chemical oxide formed by RCA clean process. A higher etching rate for ozone oxide was discovered near the transition region. Generally, volume expansion due to silicone oxidation can generate compressively strained Si local structures with an excess of silicon atoms in the interface, and distort Si–O–Si bonds at the Si/SiO_2 interface compressively [51]. Therefore, an imperfect, lower density transition layer was existed at the Si/SiO_2 interface. In contrast, the utilization of ozone water to growth ultra-thin oxide may form a defect-free SiO_2 network formation in the transition region, which generates more reactive oxygen atoms to saturate the Si dangling bonds [51]. The formation of a more homogeneous structure at the Si/SiO_2 interface responded to a higher etching rate for the denser transition layer.

Appropriate surface treatment prior to high-κ dielectric deposition is necessary to improve the interface characteristics between high-κ dielectric and silicon substrate. In order to investigate the improvement of interfacial properties between HfO_2 and Si substrate, silicon surface roughness was measured by AFM before and after surface treatment, which can be

achieved by dipping within dilute HF solution (HF:H_2O=1:500). Figs. 3-6 to 3-8 displayed the AFM results for ammonia (NH_3) nitridation, rapid thermal oxidation (RTO), and ozone water oxidation (Ozone) surface treatments, respectively. The surface roughness improvement was defined as the difference before and after the surface treatment, as shown in Fig. 3-9. After ozone water oxidation, the Si surface roughness was reduced from 1.37Å to 0.79Å (improved 41.38%), which was beneficial to suppress the leakage current density of the stacked gate dielectric. On the other hand, NH_3 and RTO treatment prior to HfO_2 deposition was less help to ameliorate Si surface roughness, which may be ascribed to higher stress introduced than Ozone treatment.

3.3.2 Comparison of Surface Treatments Prior to HfO_2 Deposition with PDA Effect

Figure 3-10 showed the normalized capacitance-voltage (*C-V*) characteristics of HfO_2 stacked gate dielectrics with various surface treatments for samples (a) without PDA and (b) with 600^{o}C PDA. Post deposition annealing could reduce the interface trap density exhibited by less kink and more sharp *C-V* characteristics. Apparent *C-V* deterioration was observed in NH_3-treated sample due to the excess nitrogen concentration compels more Si bonding constraints at the interface [52]. The *C-V* curve of Ozone-treated capacitors was kink free and exhibited good interface properties.

High-κ dielectric densification and interfacial oxidation mechanism were competed during high temperature annealing process which caused the little variations in equivalent oxide thickness (EOT) showed in Fig. 3-11. Ozone treatment slightly increased the EOT after 600^{o}C PDA supposed to the incomplete oxidation in bulk ozone oxide owing to the low growth temperature.

The hysteresis of various surface treatments was compared in Fig. 3-12. The hysteresis

voltage was defined as the flat band voltage difference between the forward and backward swept *C-V* curves, which might be contributed from the trapped charges within high-κ bulk or interface. The samples without surface treatment revealed large hysteresis; even subsequently high temperature annealing would reduce *C-V* hysteresis. Similarly, NH_3 nitridation also exhibited large hysteresis, regardless of the high temperature annealing. Fortunately, surface oxidation resulted in excellent hysteresis behavior, for both RTO and Ozone treatment. Moreover, Ozone-treated sample exhibited almost hysteresis-free characteristics.

Figure 3-13 presented the dependence of V_{FB} shift on surface treatment with and without PDA. NH_3 nitridation exhibited large negative V_{FB} shift compared to sample without treatment indicated positive charges accumulation after surface nitridation. After 600°C PDA, NH_3-treated sample showed obvious V_{FB} recovery due to interfacial N exchanged by O from annealing ambient. On the other hand, RTO- and Ozone-treated samples possessed less V_{FB} shift than NH_3 nitridation which demonstrated superior interface than NH_3-treated sample. Negative V_{FB} shift of Ozone-treated sample after PDA may indicate the increment of positive charges, which should be further investigated.

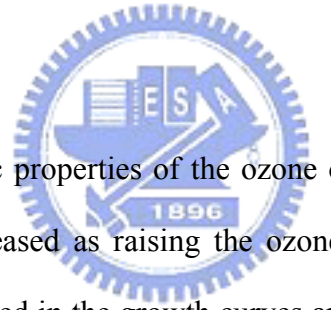
Leakage current density of HfO_2 stacked gate dielectrics with various surface treatments as a function of effective electric field (E_{eff}) for samples (a) without PDA and (b) with 600°C PDA were demonstrates in Fig. 3-14. Both RTO and Ozone treatment could suppress the leakage current than sample without surface treatment, partially due to smoother interface roughness. As indicated in Fig. 3-15(a) for samples without PDA, surface treatments could lower the leakage current density at 6 MV/cm at least two orders. Figure 3-15(b) revealed that a suitable PDA can further improve the dielectric properties.

Synthesized above mentioned in Fig. 3-16, PDA and surface treatment could reduced current density at least 2 orders of magnitude with smaller than 3Å EOT increment. The calculated effective dielectric constant as a function of surface treatments was ranging from 8

to13, as observed in Fig. 3-17.

The time-zero dielectric breakdown (TZDB) and the time-dependent dielectric breakdown (TDDB) reliability investigation were shown in Figs. 3-18 and 3-19, respectively. Surface treatments prior to high-κ dielectrics deposition and PDA can promote the reliability. Sample without surface treatment was supposed to have poor interface between HfO_2/Si, which will degrade the dielectric reliability. After surface treatments, the interface quality was improved, and the reliability therefore became superior. The ozone oxide treatment also revealed comparable results with RTO even under higher stressing voltage.

3.4 Summary



In this chapter, the basic properties of the ozone oxide were studied first. The growth rate of ozone oxide was increased as raising the ozone quantity contained in DI water. A saturated oxidation was observed in the growth curves and the resultant self-limiting property could improve the thickness uniformity after furnace or/and rapid thermal oxidation. The formation of a more homogeneous structure at the Si/ozone oxide interface performed a higher etching rate for the denser transition layer. Ozone oxide could improve Si surface roughness by 41%, which was beneficial to suppress the leakage current density of the stacked gate dielectric.

Then the influences of surface treatment prior to HfO_2 gate dielectric deposition were investigated. Significantly large fixed charges and hysteresis of NH_3 nitridation would degrade device performance. Albeit RTO treatment exhibited comparable leakage current with Ozone treatment, the time-to-breakdown value was still also less than Ozone treatment. As a result, sample with Ozone treatment revealed small leakage current, negligible hysteresis and

excellent dielectric reliability, which was considered to be one of the most potential alternative to improve the interface properties between high-κ dielectrics and silicon surface.

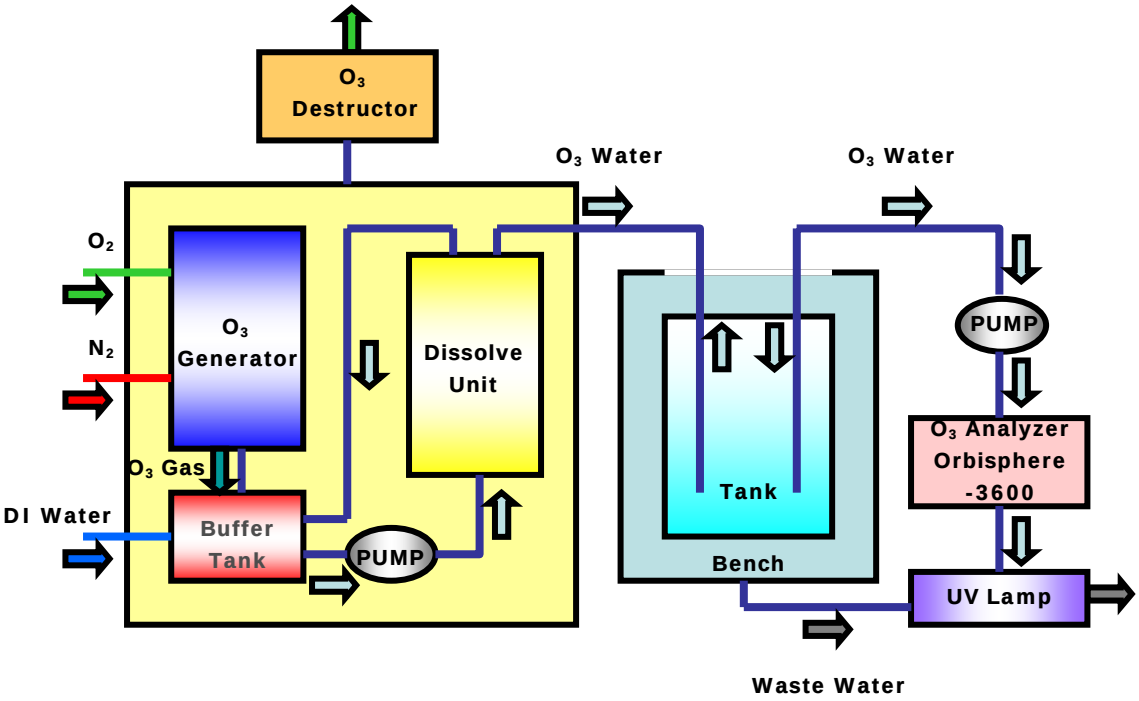


Fig. 3-1 Schematic diagram of ozone oxide growth system.

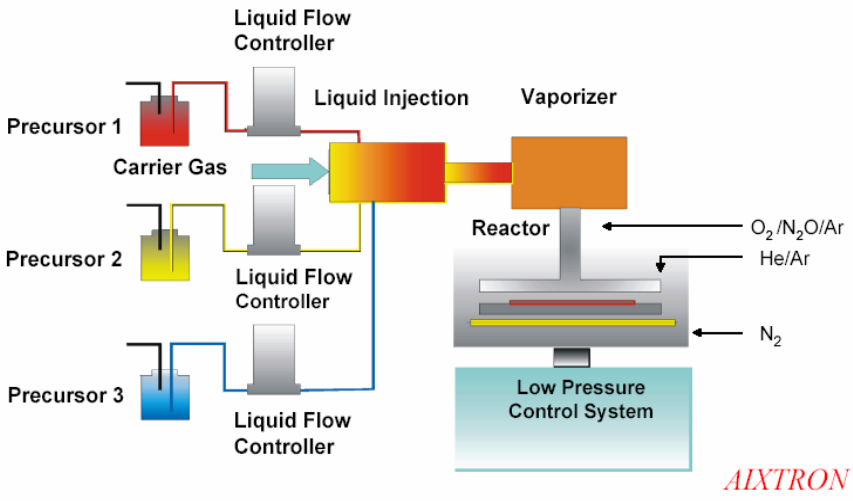


Fig. 3-2 Schematic diagram of MOCVD system structure.

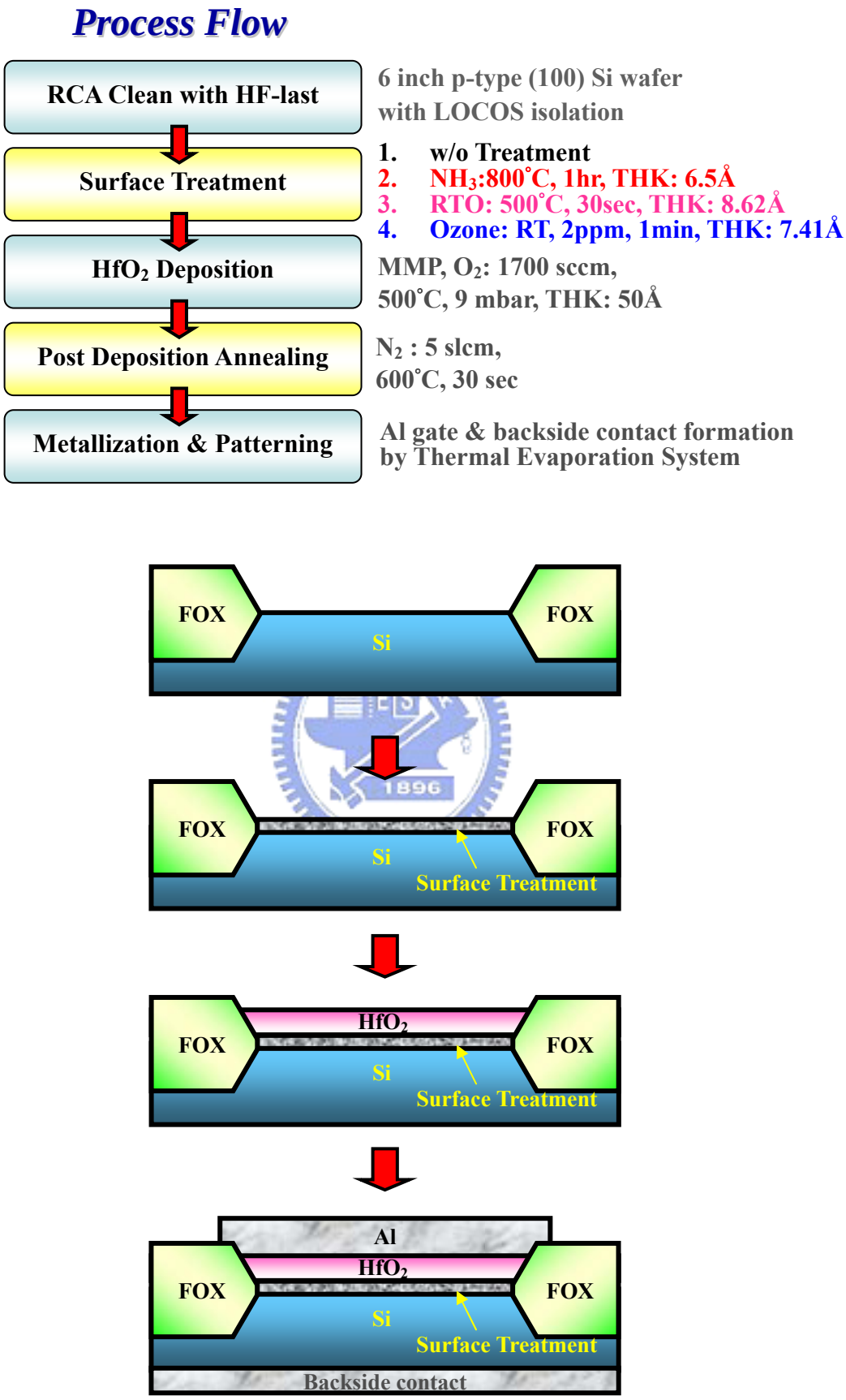


Fig. 3-3 HfO_2 MOS devices process flow, device cross section and split conditions.

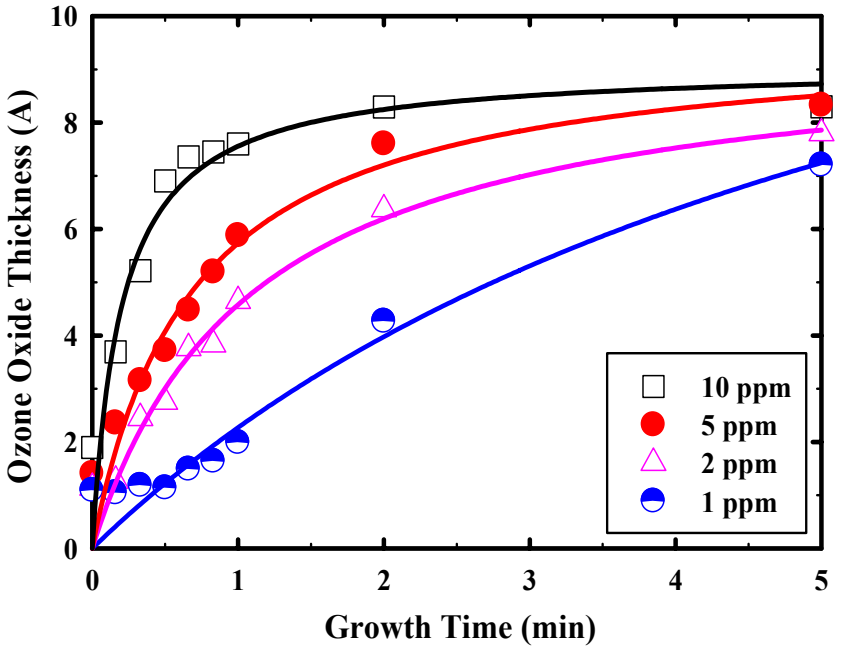


Fig. 3-4 The growth curves of ozone oxide as a function of ozone water concentration.

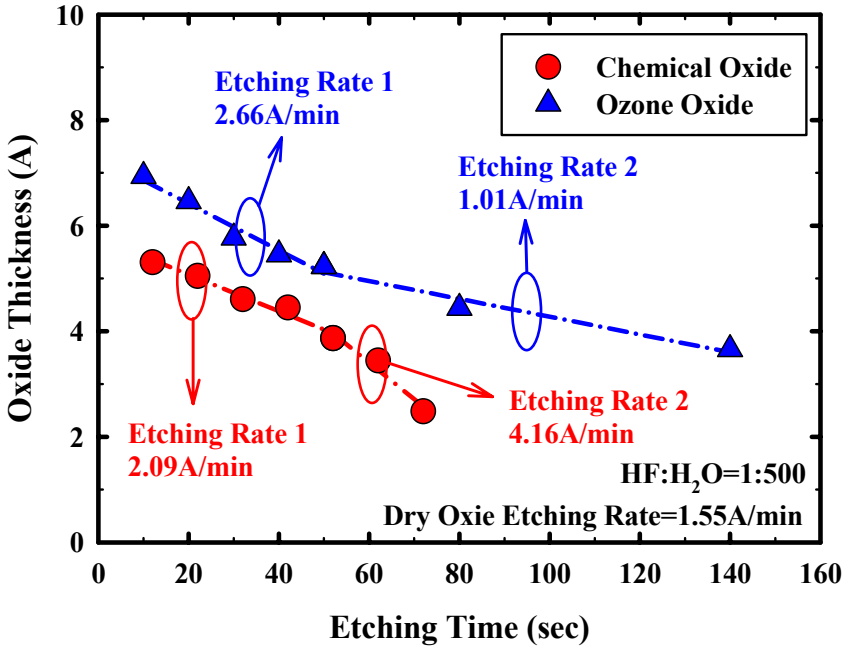
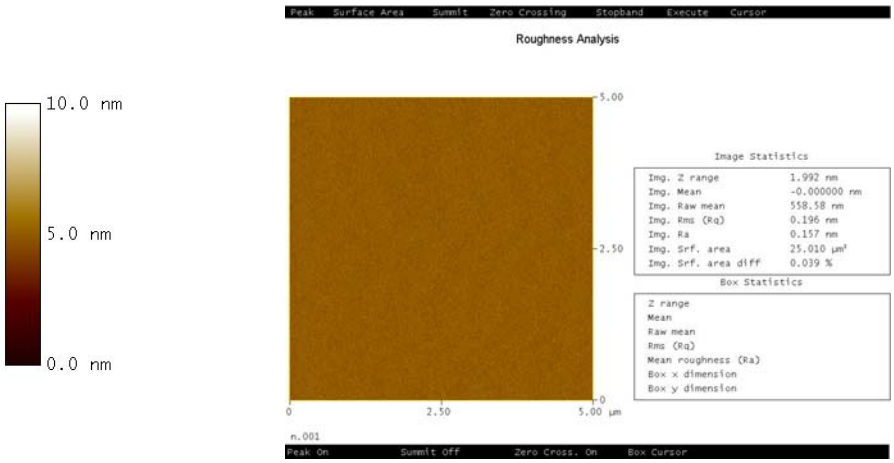
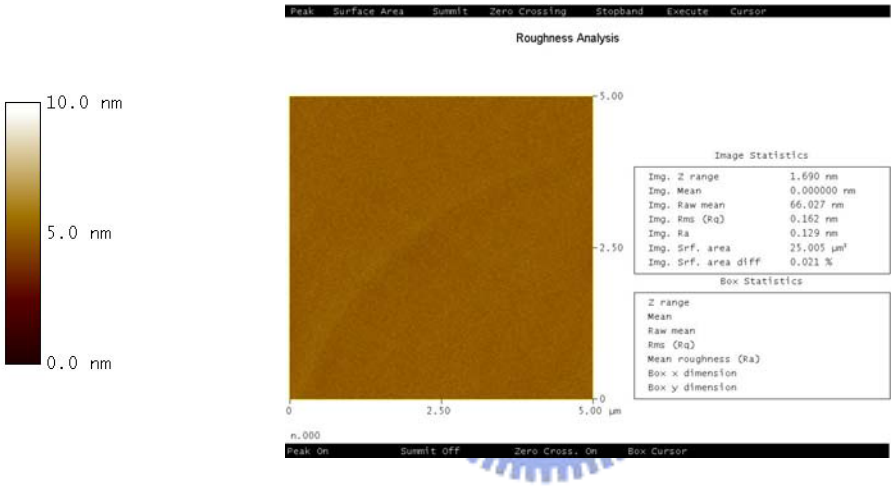


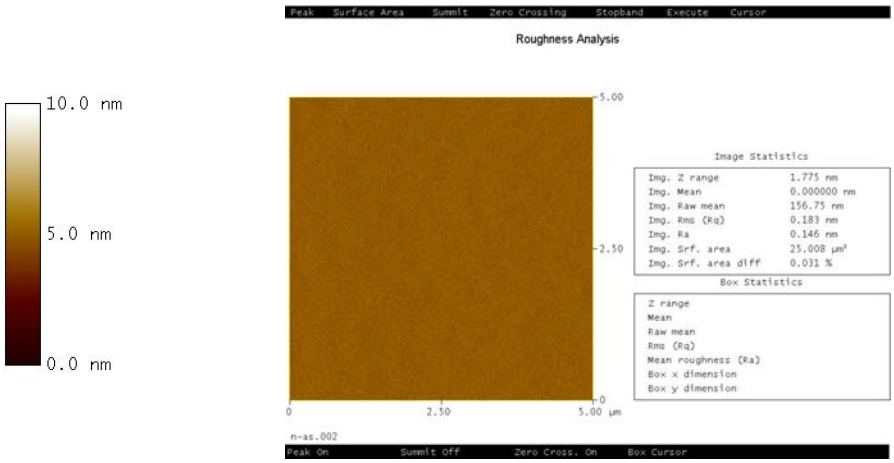
Fig. 3-5 Comparison the etching rate of ozone oxide at HF: H_2O=1:500 to chemical oxide formed by RCA clean without HF-last.



(a) Bare-Si Roughness RMS Average =1.98 Å

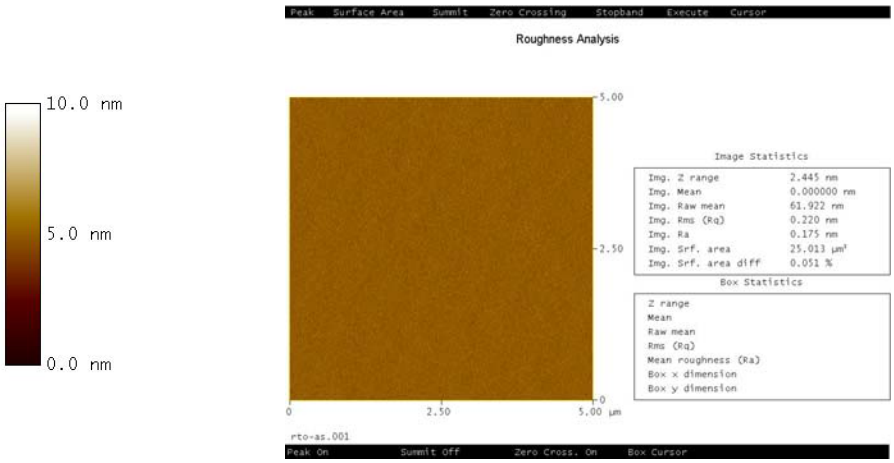


(b) NH_3 Nitridation Roughness RMS Average =1.85 Å

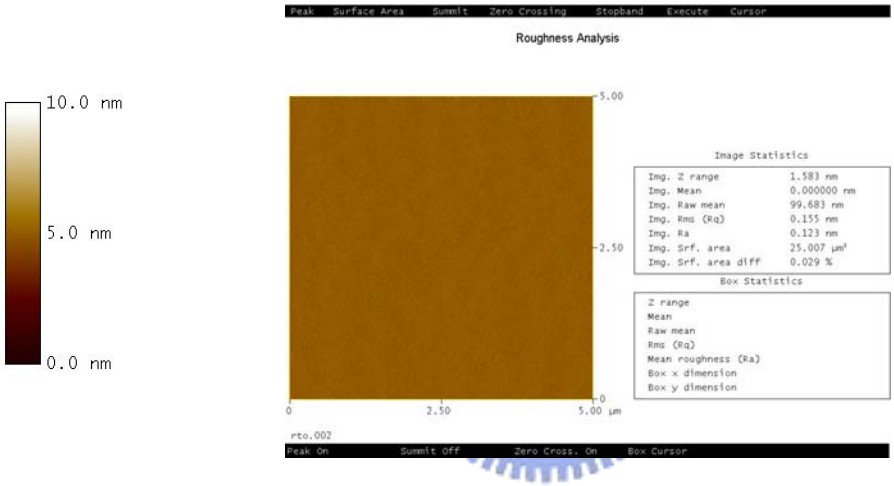


(c) HF-dipped Roughness RMS Average =1.81 Å

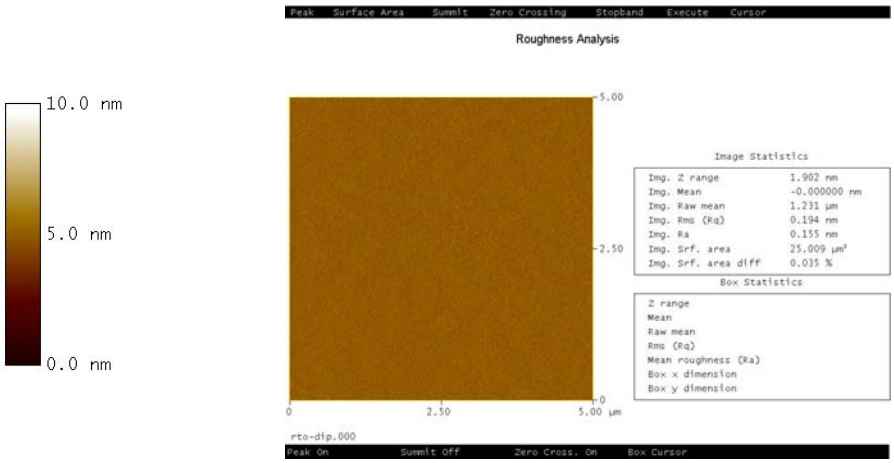
Fig. 3-6 AFM results of NH_3 treatment for Si surface roughness improvement.



(a) Bare-Si Roughness RMS Average =2.13 Å

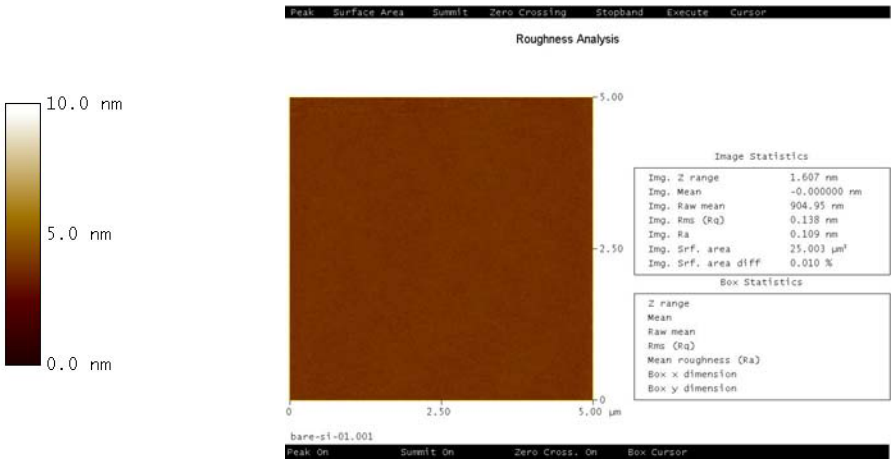


(b) RTO Roughness RMS Average =1.47 Å

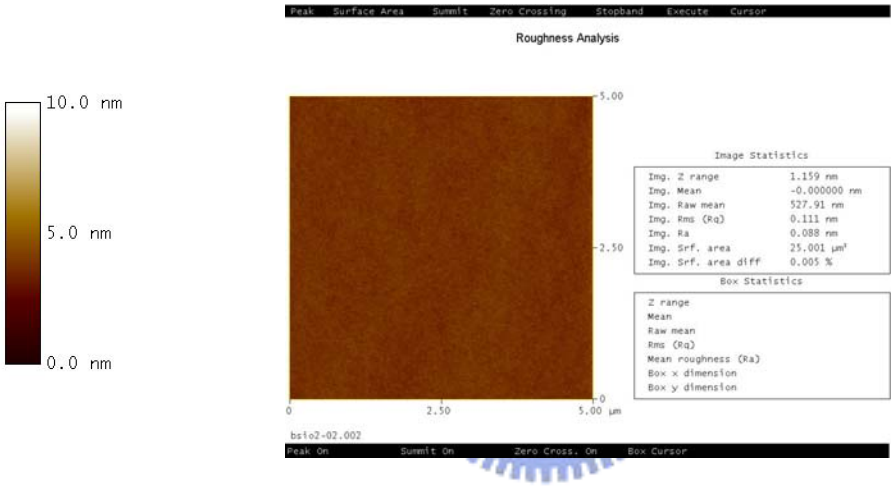


(c) HF-dipped Roughness RMS Average =1.92 Å

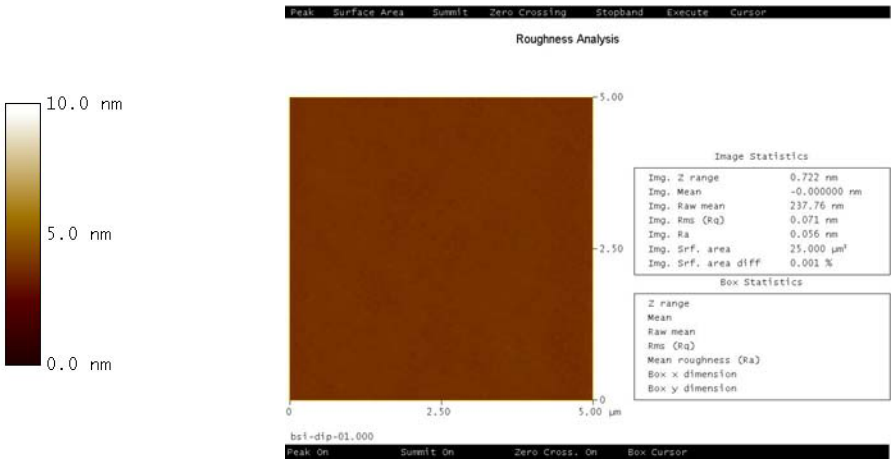
Fig. 3-7 AFM results of RTO treatment for Si surface roughness improvement.



(a) Bare-Si Roughness RMS Average =1.37 Å



(b) Ozone oxide Roughness RMS Average =1.09 Å



(c) HF-dipped Roughness RMS Average =0.79 Å

Fig. 3-8 AFM results of ozone oxide treatment for Si surface roughness improvement.

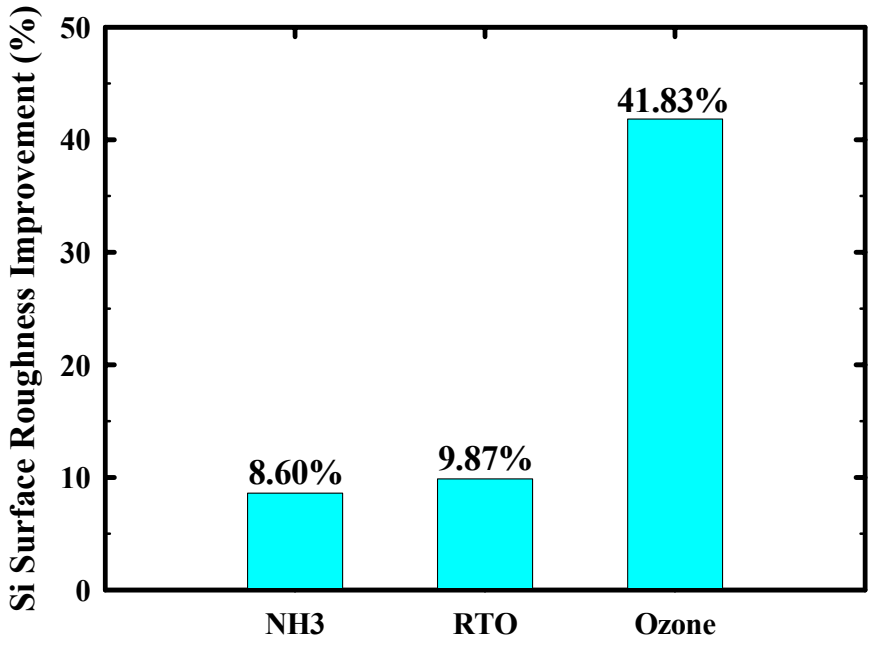
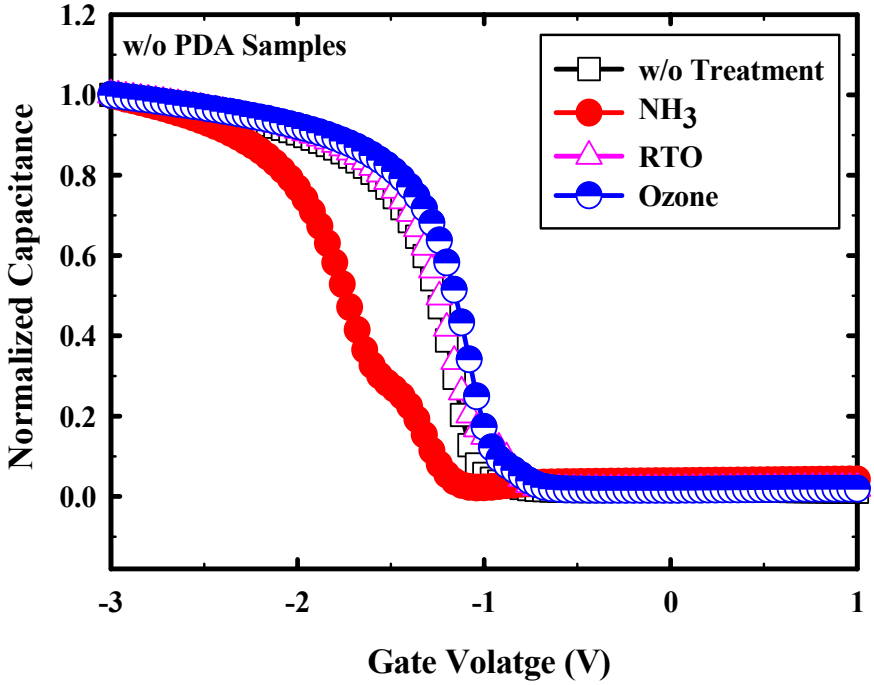
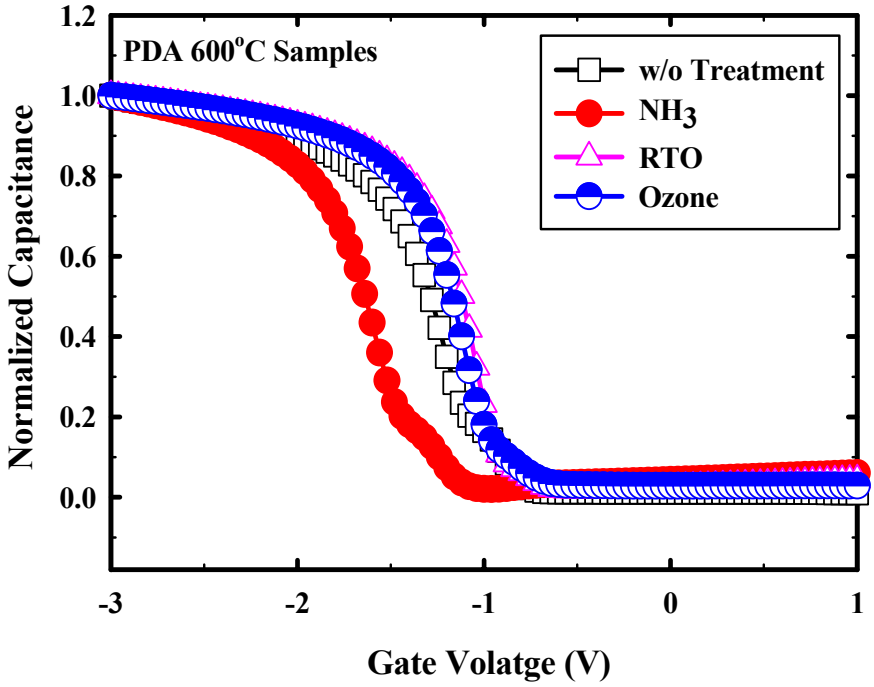


Fig. 3-9 Comparison of the Si surface roughness improvement for three kinds of surface treatments.

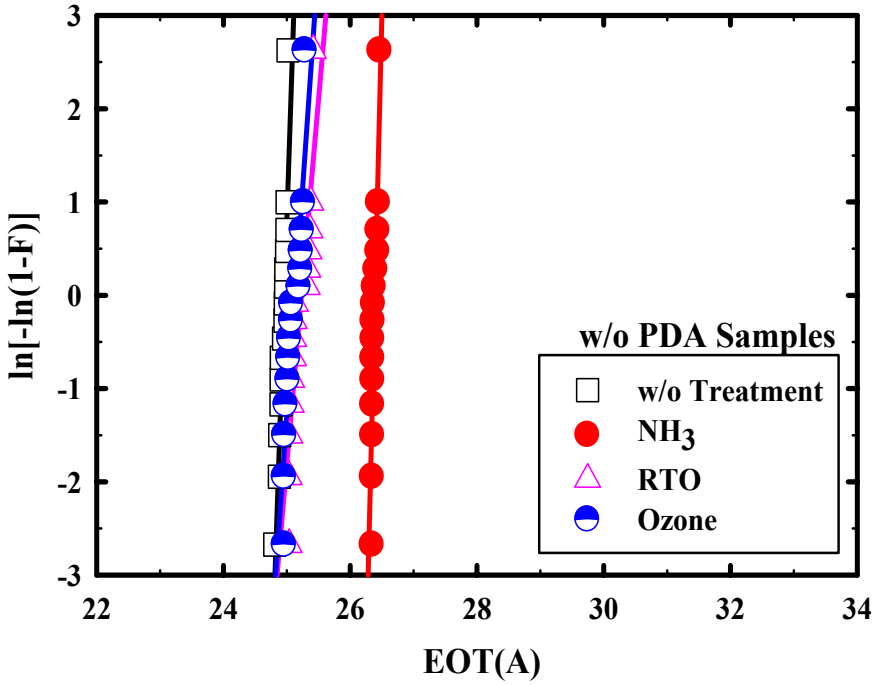


(a)

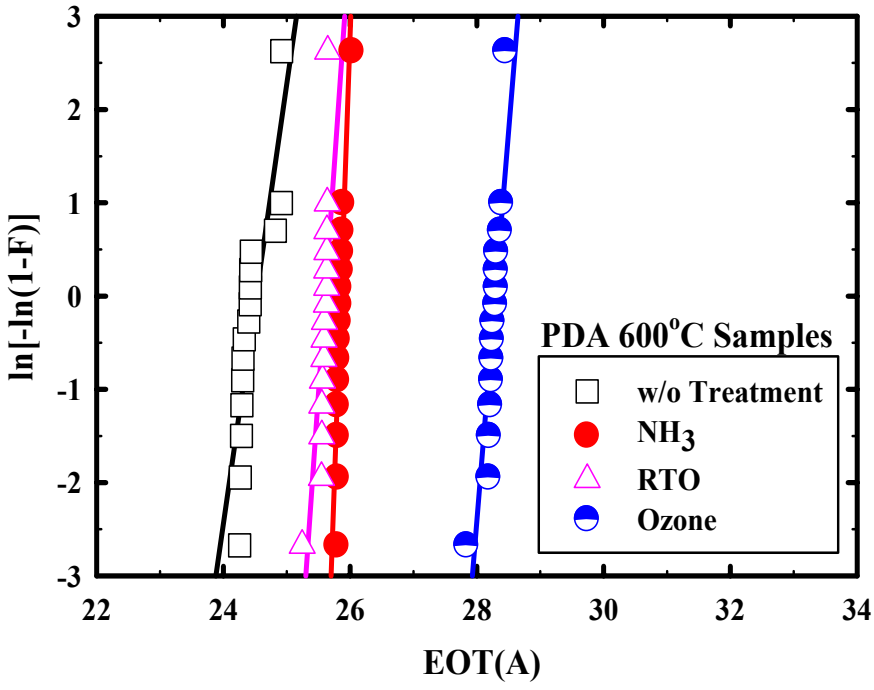


(b)

Fig. 3-10 Normalized C-V characteristics of HfO_2 stacked gate dielectrics with various surface treatments (a) without PDA and (b) with 600°C PDA.



(a)



(b)

Fig. 3-11 EOT Weibull distributions for samples (a) without PDA and (b) with 600°C PDA.

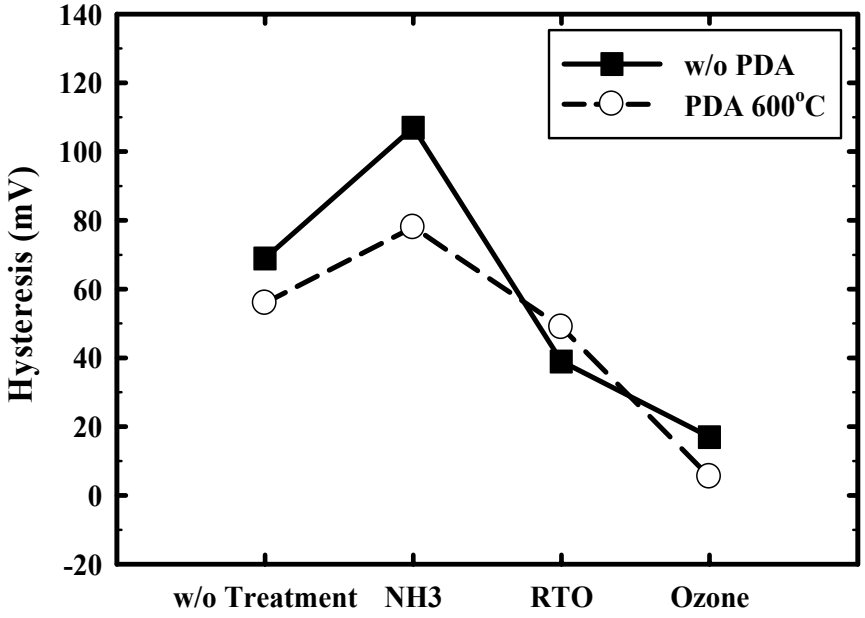


Fig. 3-12 Hysteresis comparison between several surface treatments.

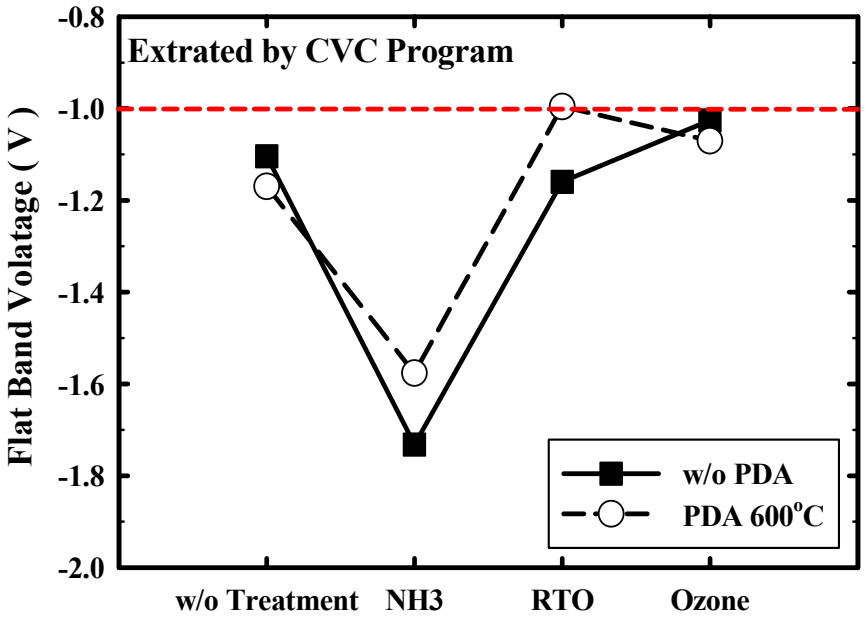
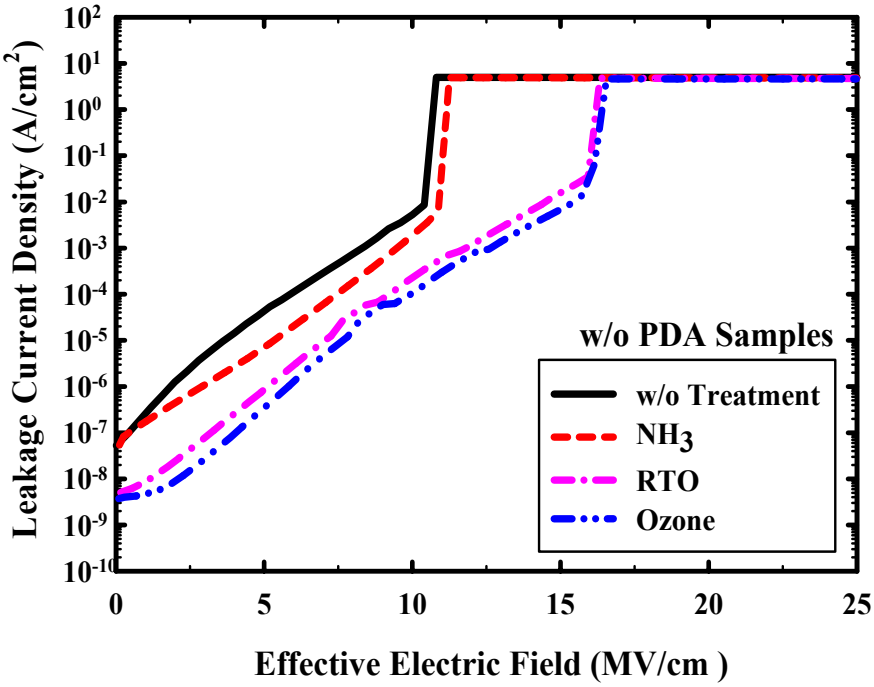
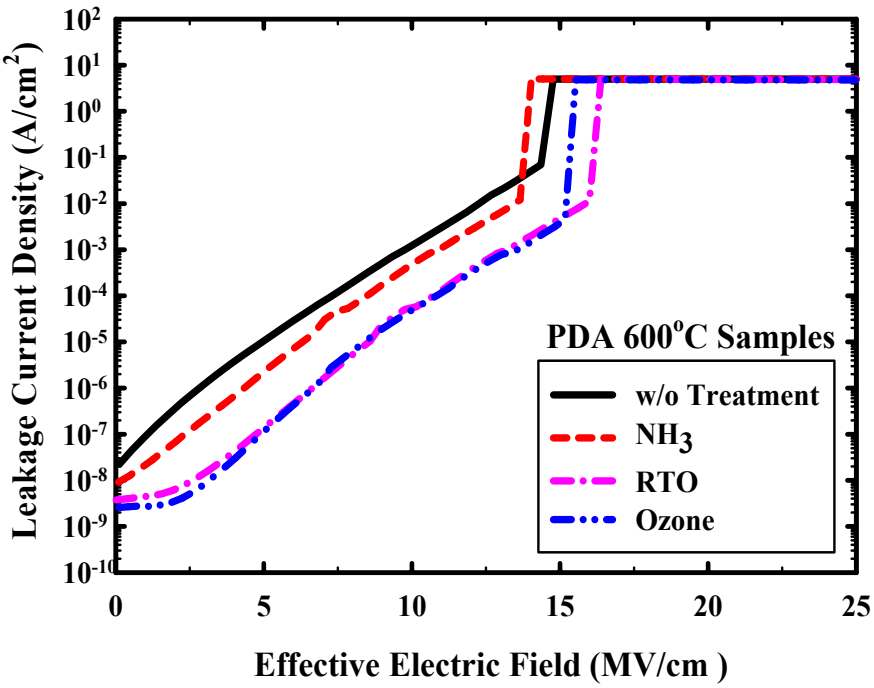


Fig. 3-13 Flat-band voltage variation as a function of surface treatments.

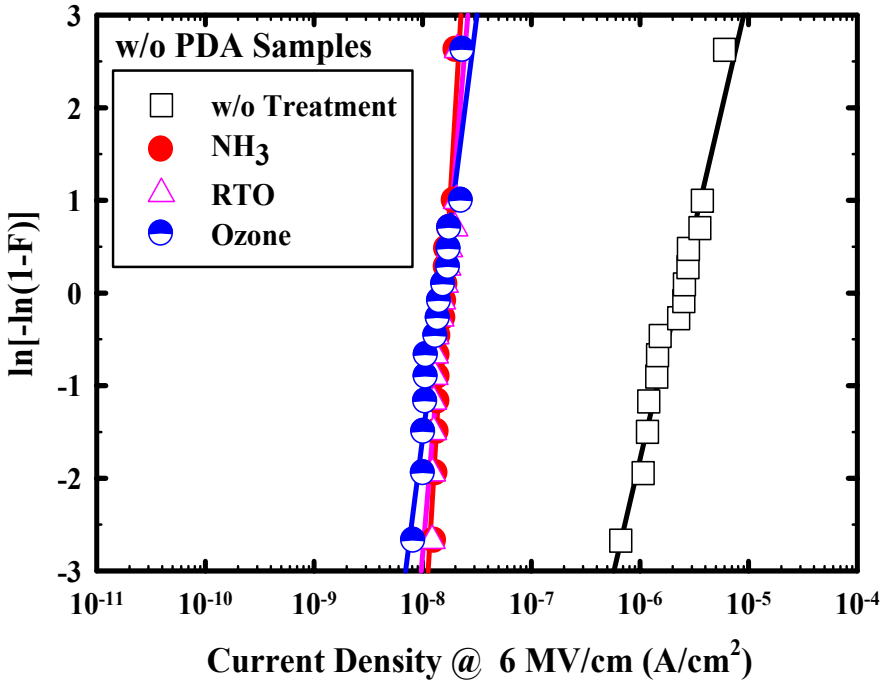


(a)

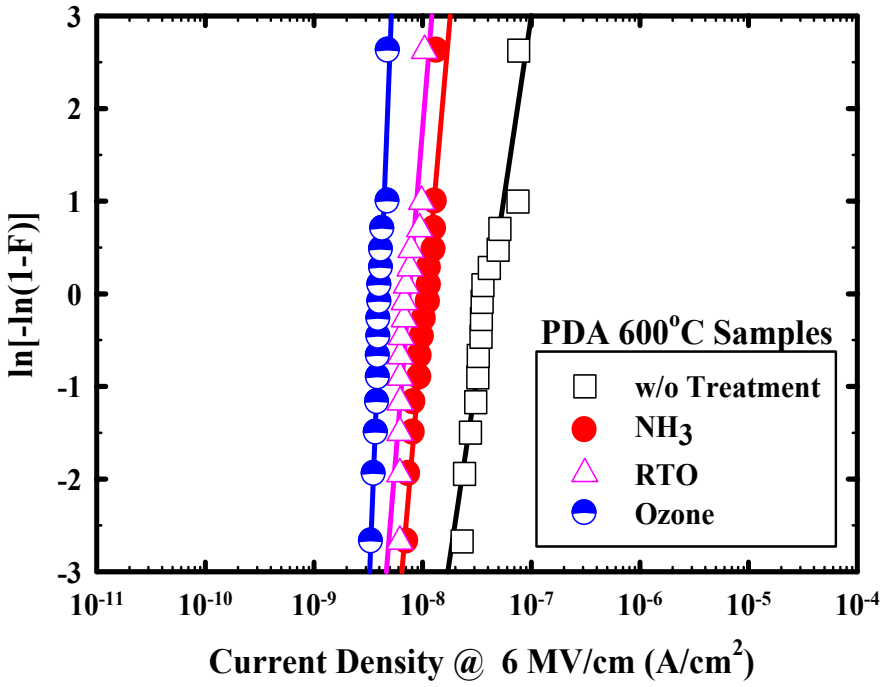


(b)

Fig. 3-14 Leakage current density of HfO_2 stacked gate dielectrics with various surface treatments as a function of effective electric field (a) without PDA and (b) with 600°C PDA.



(a)



(b)

Fig. 3-15 Leakage current density Weibull distributions at 6 MV/cm for samples (a) without PDA and (b) with 600°C PDA.

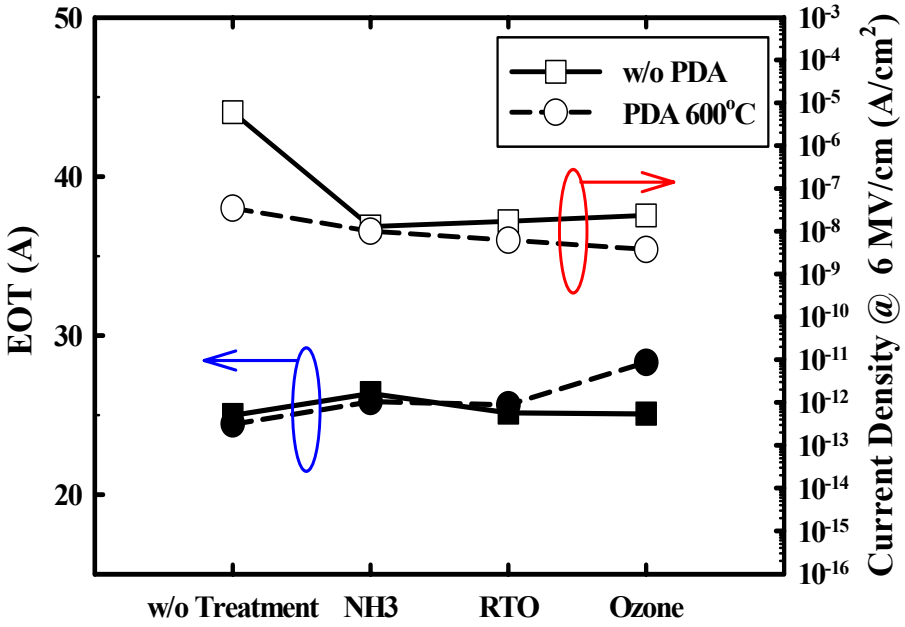


Fig. 3-16 Assembled the EOT and leakage current density at 6 MV/cm performances for different surface treatments.

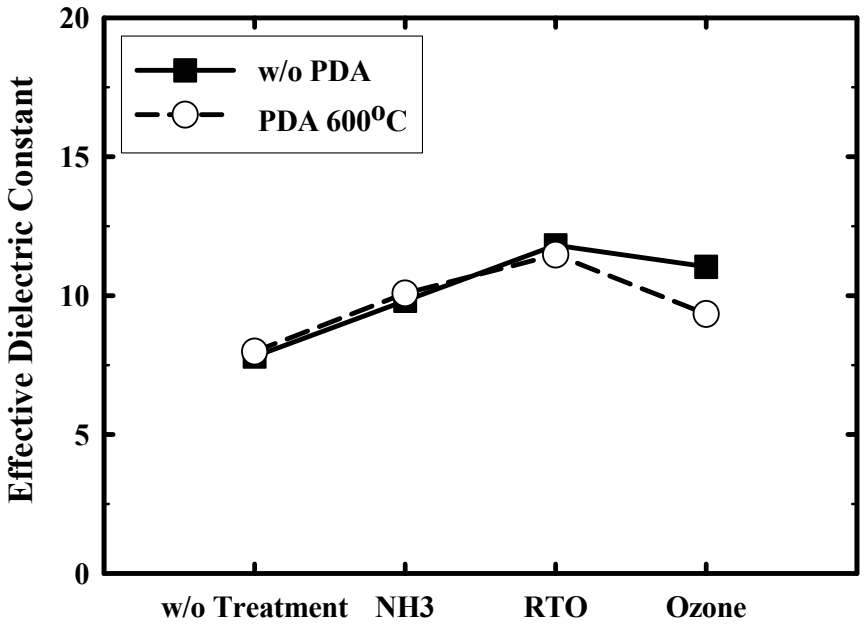
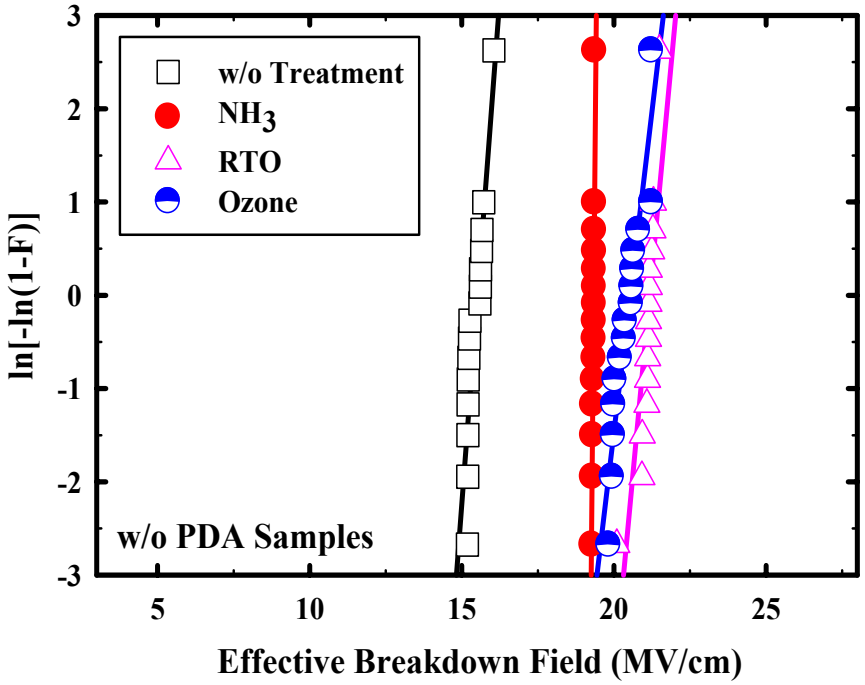
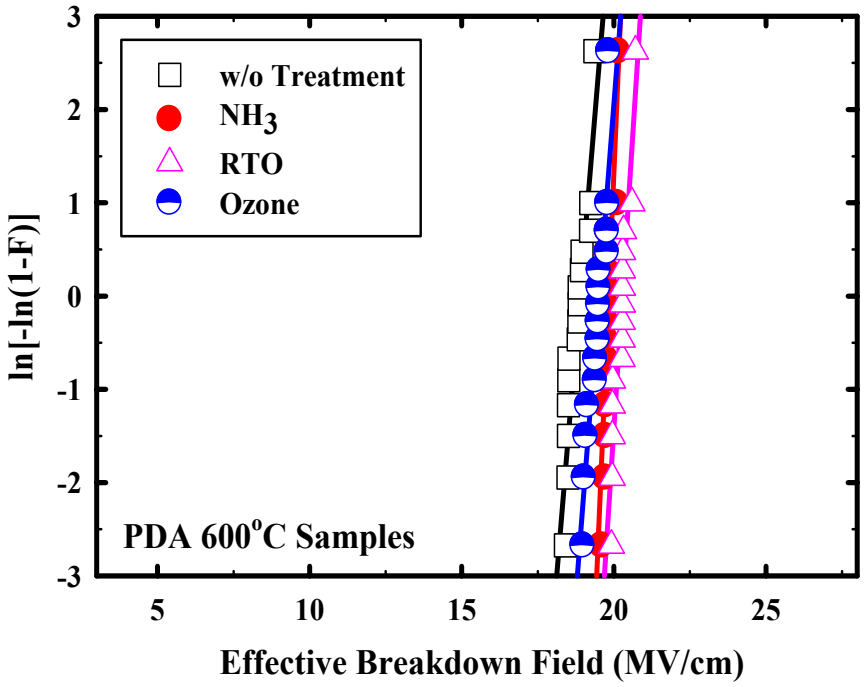


Fig. 3-17 Effective dielectric constant variation as a function of surface treatments.

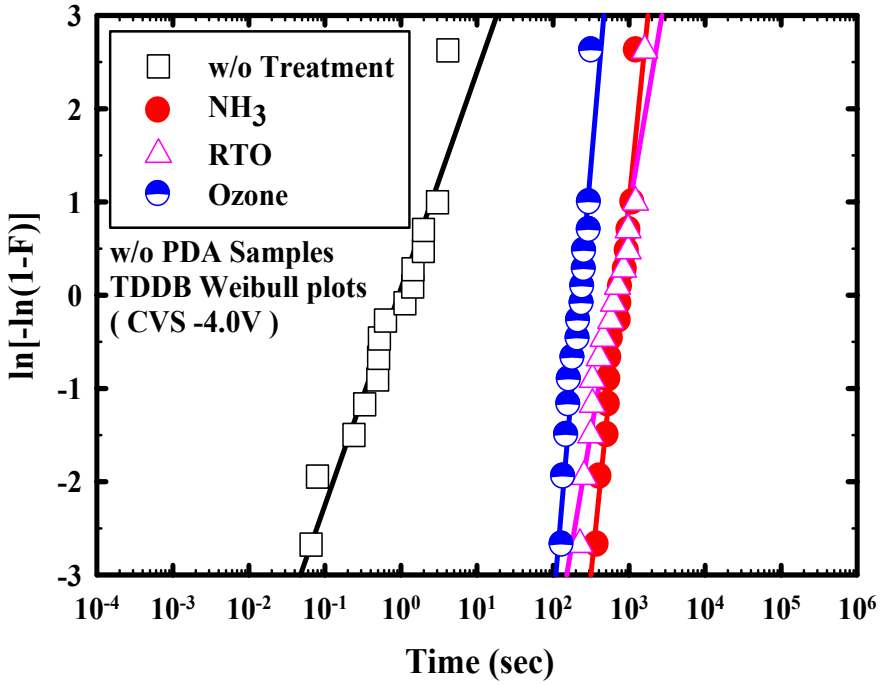


(a)

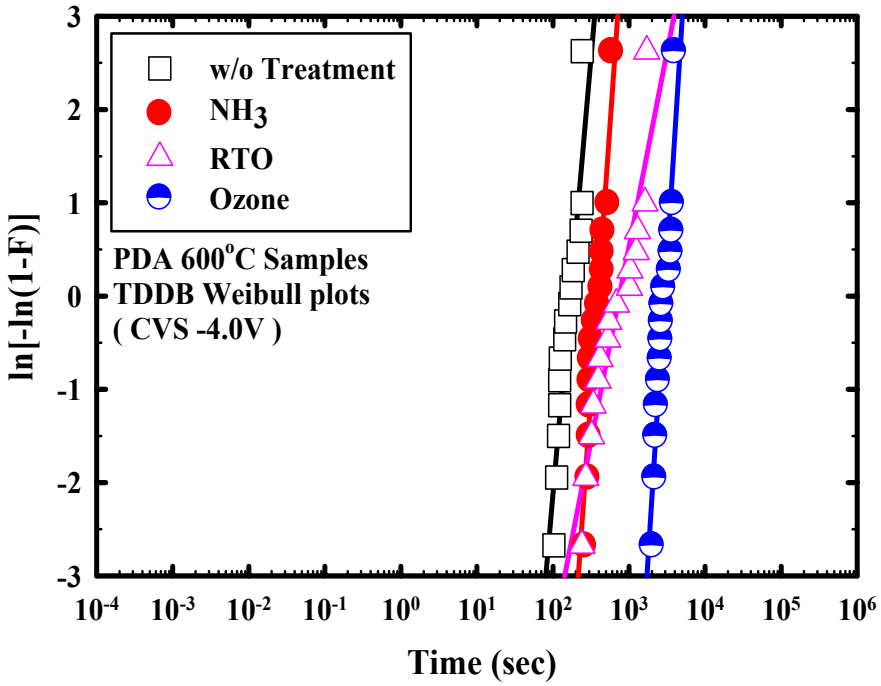


(b)

Fig. 3-18 TZDB reliabilities for samples (a) without PDA and (b) with 600°C PDA.



(a)



(b)

Fig. 3-19 TDDB reliabilities for samples (a) without PDA and (b) with 600°C PDA.

CHAPTER 4

Trapping Characteristics and Current Transport Mechanism of the HfO_2 Gate Dielectric

4.1 Introduction

According to the International Technology Roadmap for Semiconductors (ITRS), the further miniaturization of the integrated circuits in gigascale technology requires the use of high dielectric constants (high-κ) materials as charge storage insulators as well as alternative gate dielectrics in metal-oxide-semiconductor field-effect transistors (MOSFETs) [3]. Consequently, the high-κ oxides have been extensively studied to overcome the problems associated with the extremely thin conventional thermal SiO_2. For example, these materials have to be introduced in integrated circuits to satisfy the increasing demands of the high-density capacitors for dynamic random access memory (DRAM) applications [54]-[55]. Recently many efforts have been devoted to understand the electrical properties including defects produced under various treatments of MOS structures with high permittivity insulators. Very little is known about the reliability of the high-κ dielectrics. The degradation of the insulator in MOS devices is one of the most important issues for the ultralarge-scale integrated circuits and the reliability characteristics are greatly influenced by the bulk and interface traps. The problem with the high-κ dielectrics is that very often these traps exist in unacceptably high levels due to a nonstoichiometric composition and/or microstructure imperfections which usually are present in the as-fabricated films. These defects act as traps for the charge carriers injected into or generated in the dielectric. In order to meet the future

needs of the high-κ dielectrics reliability, a physical understanding of the conduction and degradation mechanisms is required for these materials. In this chapter, the surface treatment effects on the charge trapping characteristics and current transport mechanism of the HfO_2 gate dielectric were studied.

4.2 Experiment Details

Mainly, the samples measured in this chapter were the same with those in chapter 3. LOCOS isolated MOS capacitors were fabricated on 6 inch p-type (100) silicon wafers. After forming LOCOS isolation, wafers were cleaned by standard RCA processes with HF-last. Prior to high-κ dielectrics deposition, the samples were prepared either by Ozone, NH_3 or RTO. Diluted ozone water (2ppm) was used to grow an ultra-thin ozone oxide about 7~8Å (measured by ellipsometer). NH_3 nitridation was performed in a high temperature furnace at 800^{o}C for 1 hour to generate an ultra-thin oxynitride layer (~7Å). RTO was also intended to deposit a thin SiO_2 layer (~8Å), at 800^{o}C using a rapid thermal process system for 30 seconds. After one of the surface treatments, 50Å HfO_2 was then deposited at 500^{o}C by MOCVD system, followed by a high temperature post deposition annealing (PDA) at 600^{o}C in the nitrogen ambient for 30 seconds. Aluminum metal served as the gate electrode was created by a thermal evaporation system. After gate electrodes patterned and contact holes etched, backside contact was formed. Square capacitors of 1×10^{-4} cm^2 areas with LOCOS isolation are used to evaluate the gate oxide integrity.

Hewlett-Packard (HP) 4284 LCR meter was utilized for capacitance-voltage (*C*-*V*) and conductance-voltage (*G*-*V*) data obtained. UCLA CVC simulation program was utilized to obtain the accurate flat band voltage (V_{FB}). The tunneling leakage current density-electric

field (*J-E*) and the reliability characteristics of MOS capacitors were measured by semiconductor parameter analyzer HP 4156C. The temperature dependence of the gate leakage current was studied to understand the current transport mechanisms. The leakage currents were measured from 25°C to 150°C for gate electron injection (negative V_G).

4.3 Results and Discussions

In this chapter, the surface treatment effects on the charge trapping characteristics the HfO_2 gate dielectric were studied in terms of trapping efficiency, conductance peak shift, and SILC defect generation. The current transport mechanism was also investigated.

4.3.1 Surface Treatment Effects on the Charge Trapping Characteristics of HfO_2 Dielectrics

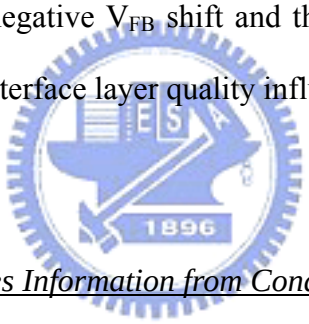
4.3.1.1 Trapping Efficiency Characteristics

Figure 4-1 depicted the effects of surface treatment on transient charge trapping behaviors of HfO_2 dielectrics with and without PDA under a constant voltage stress (CVS) of -3.8V. The decrease in the absolute gate current was obviously coming from hole trapping behavior. Figure 4-2 was the corresponding flat band voltage shift toward negative direction due to the positive charges trapped, i.e. hole trapping after stress. For going to details about reliability phenomenon, Fig. 4-3 demonstrated trapped charges under CVS with various injection charges and the slop was defined as the trapping efficiency (showed in Fig. 4-4) used to compare the dielectric quality.

In order to obtain low trapping efficiency, dielectrics with low bulk and interface trap

density should be deposited. However, the sample without surface treatment and PDA was not shown here because of significant degradation after CVS. Even though post deposition annealing could improve the dielectric quality, the trapping efficiency was still not as good as the samples with surface treatments. Ozone oxide exhibited the lowest trapping efficiency after 600^{o}C PDA than NH_3 or RTO treatment partially due to the better interface properties. On the other hand, the inferior trapping characteristics of Ozone-samples without PDA might be caused by the incomplete oxidation owing to the low growth temperature, which could be evidenced on lower etching rate shown in Fig. 3-5.

The corresponding band diagram including the two leakage current components under CVS condition was drawn in Fig. 4-5. Hole current from substrate was considered to be the dominant terms owing to the negative V_{FB} shift and the decreasing of absolute gate current which consisted with that the interface layer quality influence the carriers injection.



4.3.1.2 Interface Trap Properties Information from Conductance Measurements

The conductance-voltage (*G*-*V*) measurement [56] is a useful and sensitive tool for investigating interface characters between Si and dielectrics. In the conductance method, interface trap levels are detected through the energy loss resulting from changes in interface traps occupancy produced by small variation of gate voltage. The small-signal equivalent parallel conductance of MOS capacitor G_p displays different behavior depending on the dominant loss mechanism. For a chosen ac frequency, vary the gate bias from accumulation to midgap. In accumulation, majority carrier density is very large near the Si/dielectric interface, so those interface trap capture rates are very rapid compared to the ac frequency. Interface trap levels respond immediately to the ac voltage, and no loss occurs. In depletion, majority carrier density at the Si/dielectric interface is reduced. Capture rates slow down, and interface

trap levels cannot keep in phase with the ac voltage. A loss therefore occurs. Still further in depletion, near midgap, majority carrier density becomes insufficient that almost no carriers are exchanged between interface trap levels and the silicon. Hence the loss is also low. In short, interface trap loss goes through a peak as a function of gate bias. Maximum loss occurs for the gate bias where majority carrier density makes the interface trap capture rate compare to the ac frequency.

Figure 4-6 illustrated the *C*-*V* and *G*-*V* curves variation after CVS for Ozone-treated samples with and without PDA. The conductance peak shift and the value increase were corresponding to the flat band voltage shift and the degraded D_{it}, respectively. Figure 4-7 compared the variation of conductance peak value after CVS for several surface treatments. Two components should be noted: first is the initial conductance peak value and the second one is the change of the conductance peak value after CVS. Figure 4-8(a) compared the initial conductance peak values corresponding to the initial amount of D_{it} for various surface treatments. The sample without surface treatment and PDA was not shown because of the dielectric degradation after CVS. Post deposition annealing could reduce the conductance peak value as well as the interface trap density. NH_3 nitridation exhibited large conductance peak value compared to sample without treatment indicated higher interface charges after surface nitridation. Ozone oxide performed the lowest D_{it} values than NH_3 or RTO treatment due to the better interface properties.

The comparison of the peak value change after CVS was displayed in Fig. 4-8(b). Both surface treatments and PDA could suppress the D_{it} generation. However, Ozone-samples without PDA expressed poor results might cause by the rougher interface than 600^{o}C PDA samples shown in the HRTEM cross-sectional images in Fig.4-9.

4.3.1.3 SILC Reliabilities and Defect Generation Rate Properties

Stress-Induced-Leakage-Current (SILC) is an increase in gate oxide leakage current resulting from the application of a stress voltage or current [57]-[60]. It is an important concern in scaling gate oxide thickness because it can decrease DRAM refresh times, degrade EEPROM data retention, and increase MOSFET off-state power dissipation. During constant negative voltage stress, hole current from the substrate was injected through the interfacial layer and HfO_2 gate dielectric of the MOS capacitor. Then, positive charge defects can be repeatedly generated in the gate dielectric.

To further investigate the degradation of reliability induced by defect generation in HfO_2 dielectrics with various surface treatments, the SILC ($\Delta J/J_0$) at the low electrical field of E_{eff} = 1.5 MV/cm as a function of injected charge is shown in Fig. 4-10. Figure 4-11 extracted the defect generation rate (P_g) from the linear portion of the relationship between ($\Delta J/J_0$) and Q_{inj} [61]. PDA could generally improve the films quality and further lowering the defect generation rate. The samples without surface treatment were not shown because of the leakage current after CVS exhibited a soft breakdown phenomena. It could be seen that the values of P_g for NH_3 and Ozone treatment samples was relative low. For NH_3-treated dielectric, strong Si−N bonding at the Si/dielectric interface against the defects generated, while for Ozone-treated dielectric, the robust interface properties would contribute to less P_g. RTO exhibited a poor defect generation resistance limited its applications.

Figure 4-12 presented the SILC for Ozone surface treatment with and without PDA. Dielectric without PDA performed a serious leakage current during $-|V_{FB}|<V_G<0$ while others happened at $V_G<-|V_{FB}|$. The corresponding mechanism might be due to the low voltage SILC (LV-SILC) [62] caused by tunneling via a large amount of interfacial traps created from stress, rather than through bulk oxide traps. The difference in the SILC mechanism for Ozone oxide treatment caused by PDA should carefully investigate by eliminating other process

temperature effect such as implant activation.

4.3.2 Conduction Mechanism of the Ozone Surface Treatment HfO_2 Dielectrics

The temperature dependence of the gate leakage current was studied to understand the current transport mechanisms. The leakage currents were measured from 25°C to 150°C for gate electron injection (negative V_G). For the low electrical field case (<3.5 MV/cm), the experimental results fit the Schottky emission theory very well, as shown in Fig. 4-13. The leakage current governed by the Schottky emission yielded the following relationship:

$$J = A^* T \exp\left[\frac{-q(\phi_B - \sqrt{q\xi / 4\pi\varepsilon_i}}{kT}\right] \qquad (4\text{-}1)$$

A Schottky barrier height of 0.95 eV between Al gate and HfO_2 was extracted from these data. The corresponding dynamic dielectric constant (ε_d=9.46) was in the range between the optical dielectric constant (ε_{op}=4 for HfO_2) ant the static dielectric constant obtained from *C-V* (ε_s=9.5), which ensured the conduction mechanism. The band diagram of Al/HfO_2/SiO_2/Si capacitor simulated the low electrical field injection condition was illustrated in Fig. 4-14. It may be worth noting that, in the case of gate injection, because the Al/ HfO_2 barrier height is smaller than the energy trap energy, Schottky emission mechanism dominates over the Frenkel-Poole (F-P) mechanism, therefore it is not possible to obtain the F-P trap energy from the above procedure.

Figure 4-15 showed the Fowler-Nordheim (F-N) tunneling fit in the high field range (>3.5 MV/cm). The slop of the fitted line followed the relationship:

$$B_{Al} = -\frac{8\pi(2qm^*)^{1/2}}{3h}\Phi_{Al}^{3/2} \qquad (4\text{-}2)$$

where m* is the electron effective mass for HfO_2 and Φ_{Al} is the Al/HfO_2 barrier height. The

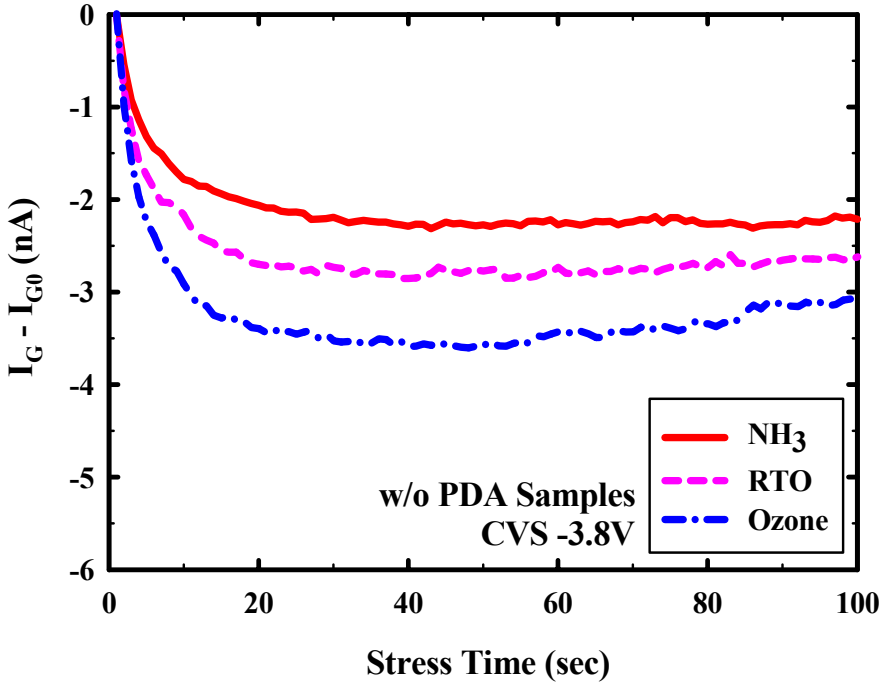
barrier height value obtained from the FN tunneling characteristics (0.99 eV) was consistent with the Al/HfO_2 barrier height (0.95 eV) we obtained earlier from Schottky emission analysis with an effective mass of 0.1 m_0 [63]. The band diagram of Al/HfO_2/SiO_2/Si capacitor during the high electrical field carrier injection was illustrated in Fig. 4-16.

In section 4.3.1.1, we concluded that the hole current from substrate was considered the dominant conduction mechanism. However, in the temperature dependence measurement, the hole current term was masked by electron current, since electron current was more sensitive to temperature variation than hole current, which could be proved by carrier separation measurement demonstrated in Fig. 4-17 [64].

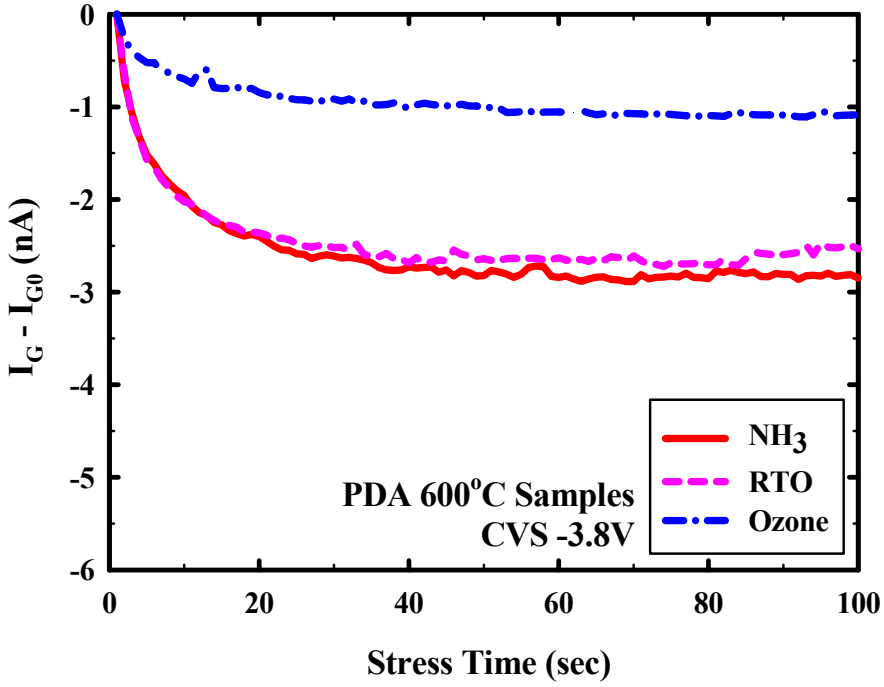
4.4 Summary

In this chapter, the surface treatment effects on the charge trapping characteristics the HfO_2 gate dielectric were studied in terms of trapping efficiency, conductance peak shift, and SILC defect generation. Ozone oxide performed the lowest trapping efficiency, D_{it} degradation and defect generation rate after 600^{o}C PDA than NH_3 or RTO treatment partially due to the better interface properties. However, Ozone-samples without PDA expressed poor results, which might be caused by the incomplete oxidation and rougher interface owing to the low growth temperature. The low D_{it} generation and P_g value of NH_3-treated dielectric was ascribed to the strong Si−N bonding at the Si/dielectric interface against the defects creation. Unfortunately, higher interface charges for as-deposited NH_3-treated dielectric would limit nitridation application. RTO also exhibited a poor defect generation resistance than Ozone-treated dielectric. The current transport mechanism was also investigated. When E_{eff}<3.5 MV/cm, the corresponding current transport mechanism was Schottky emission

under gate injection conditions. F-N tunneling dominated the conduction mechanism during 6>Eeff>3.5 MV/cm.

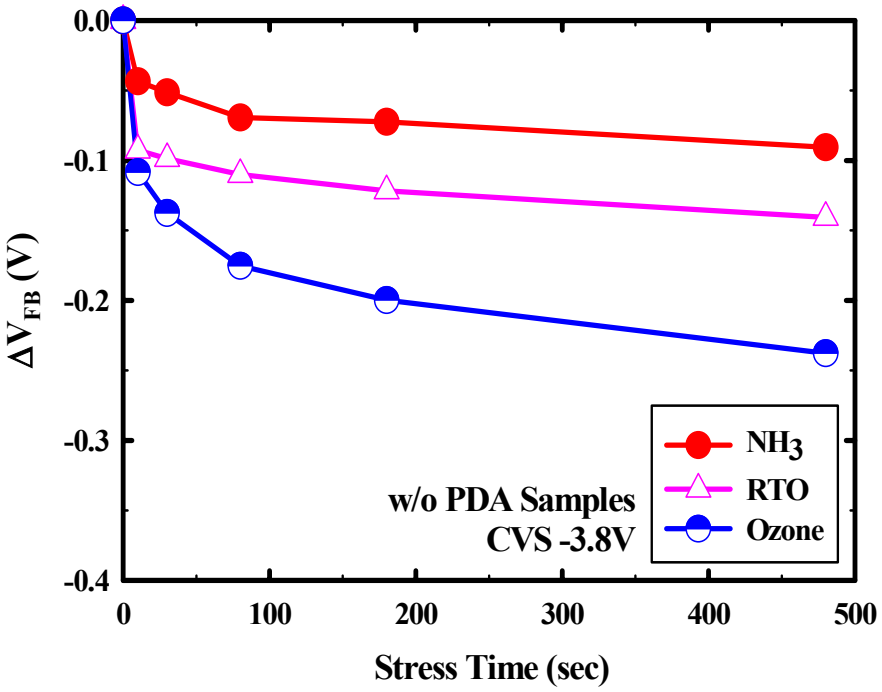


(a)



(b)

Fig. 4-1 Effects of surface treatment on transient charge trapping behaviors of HfO_2 dielectrics (a) without PDA and (b) with 600°C PDA under a constant voltage stress (CVS) of -3.8V.



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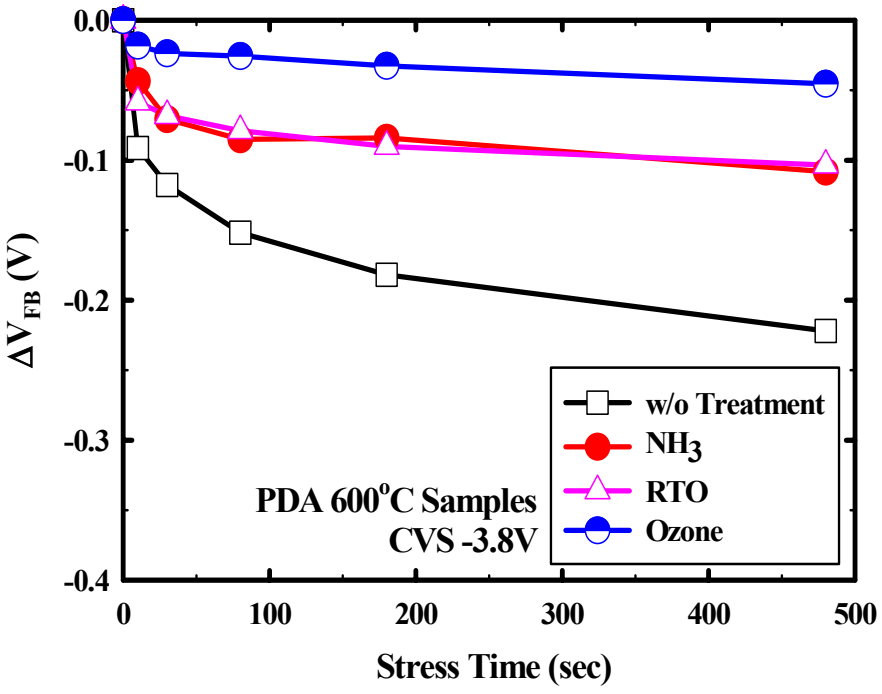
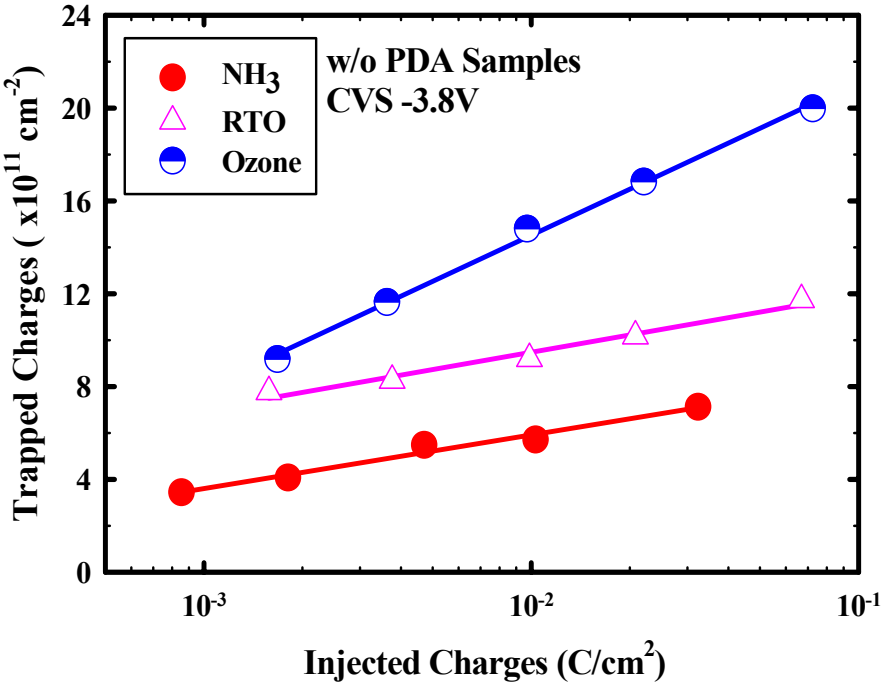
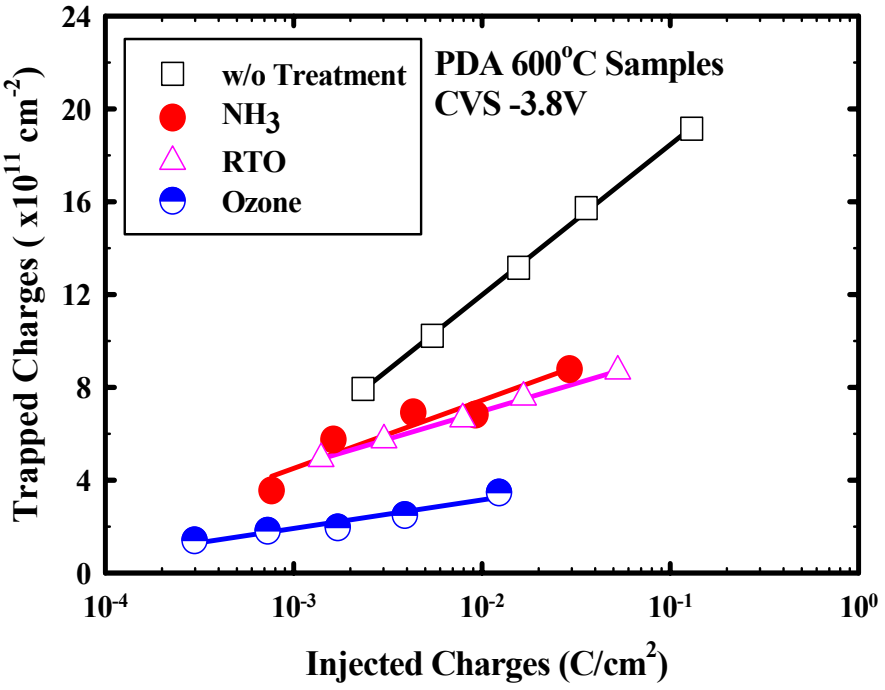


(b)

Fig. 4-2 The corresponding flat band voltage shift of HfO_2 dielectric (a) without PDA and (b) with 600°C PDA for various surface treatments under a CVS of -3.8V.



(a)



(b)

Fig. 4-3 Trapped charges comparison of HfO_2 dielectric (a) without PDA and (b) with 600°C PDA for various surface treatments.

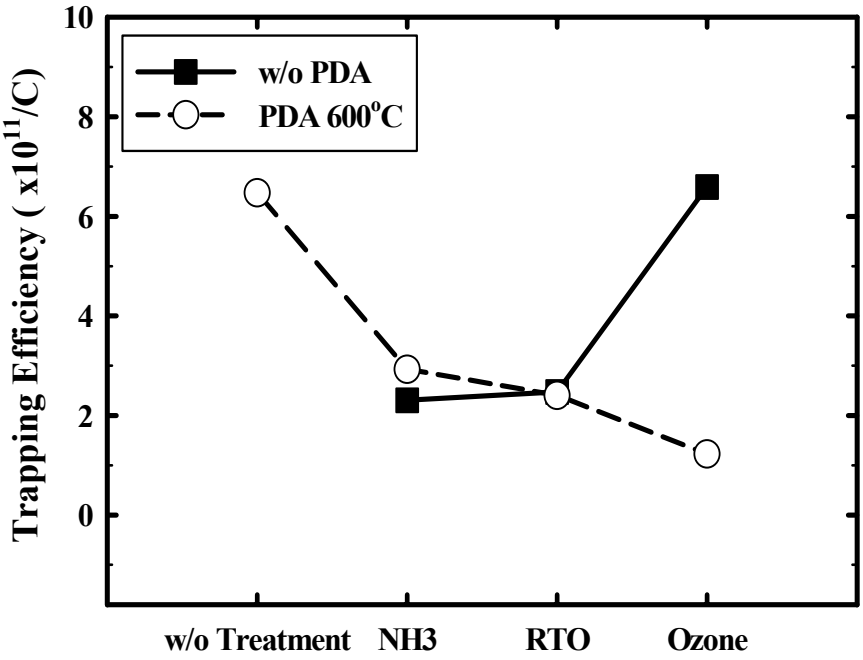


Fig. 4-4 Comparison of the trapping efficiency between several surface treatments.

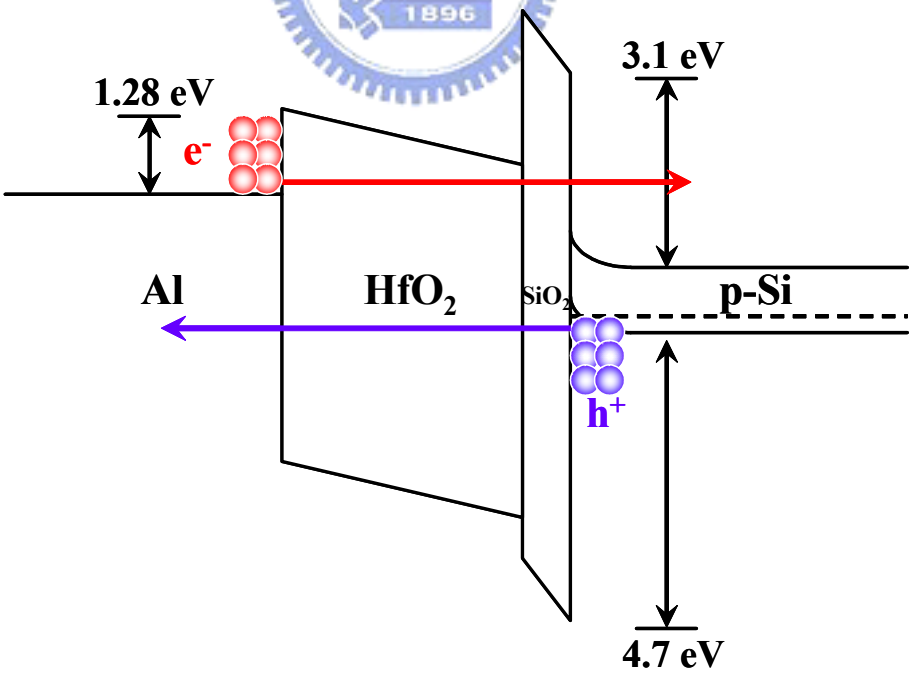
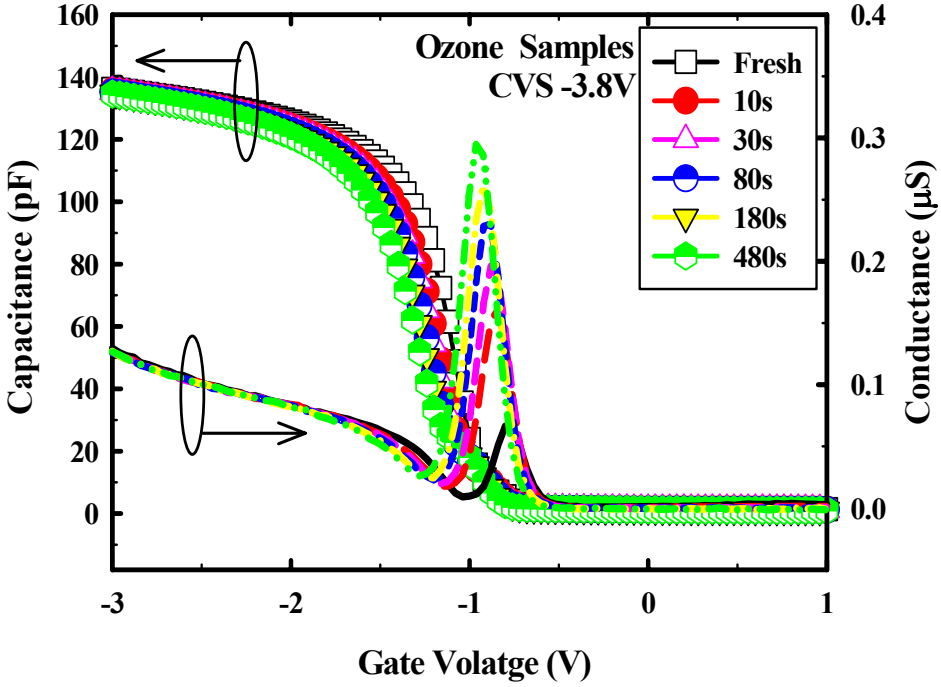
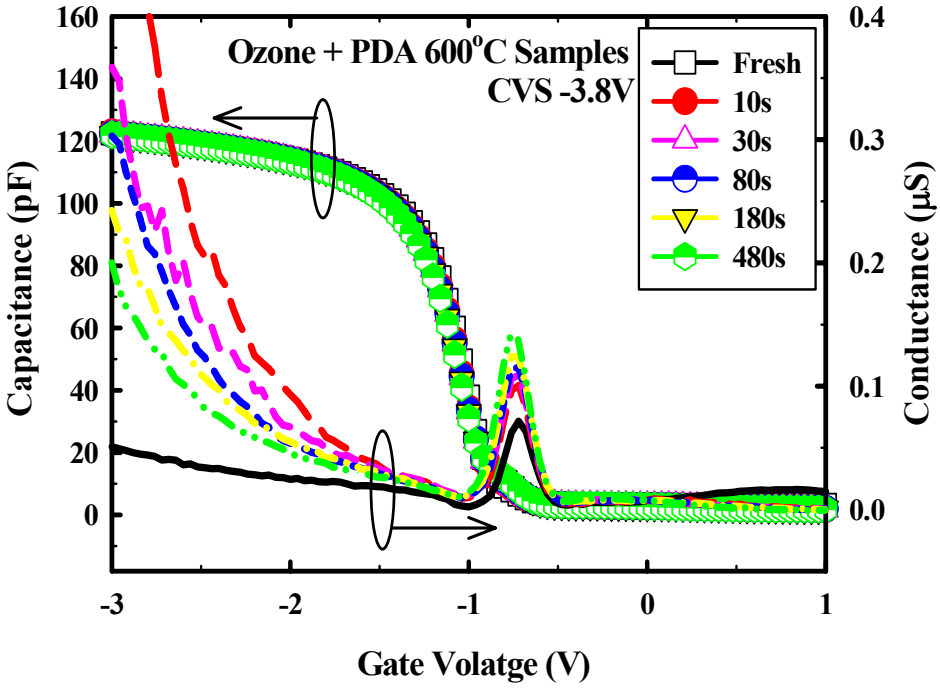


Fig. 4-5 The band diagram of Al/HfO_2/SiO_2/Si capacitors included the two leakage current components under CVS condition.

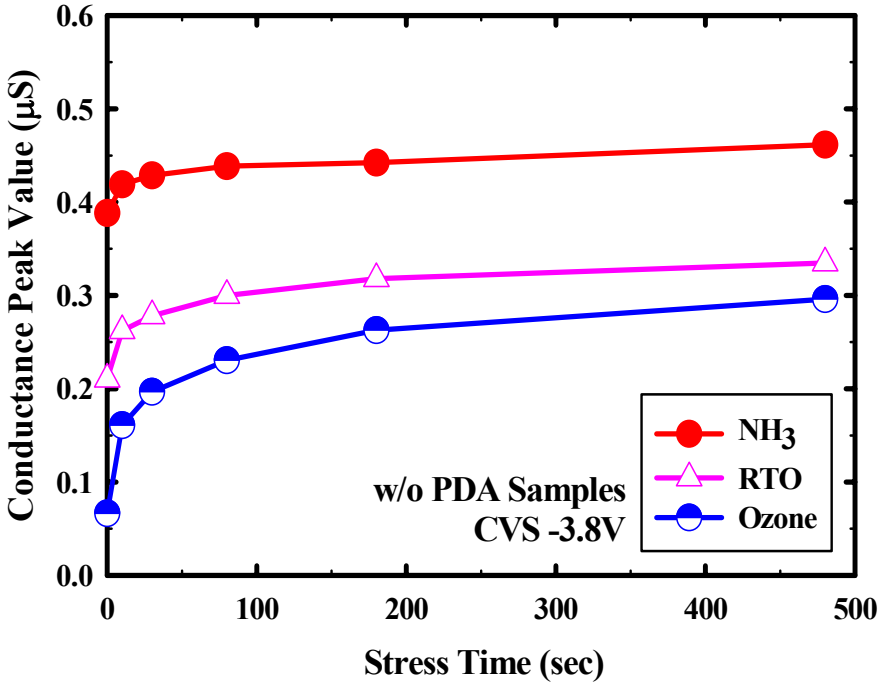


(a)

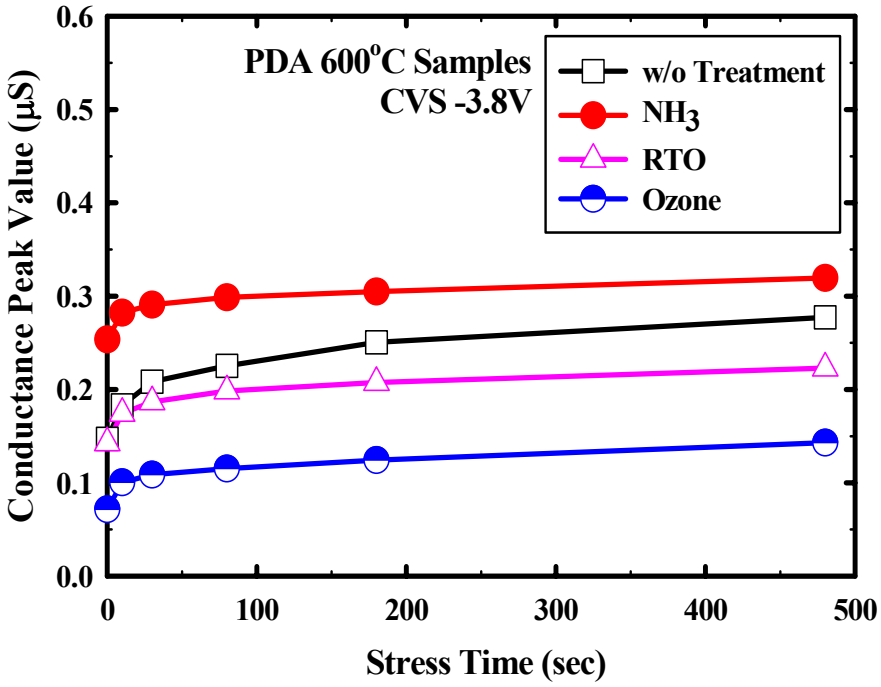


(b)

Fig. 4-6 The *C-V* and *G-V* curves of Ozone-treated HfO_2 dielectric (a) without PDA and (b) with 600°C PDA under a CVS of -3.8V.

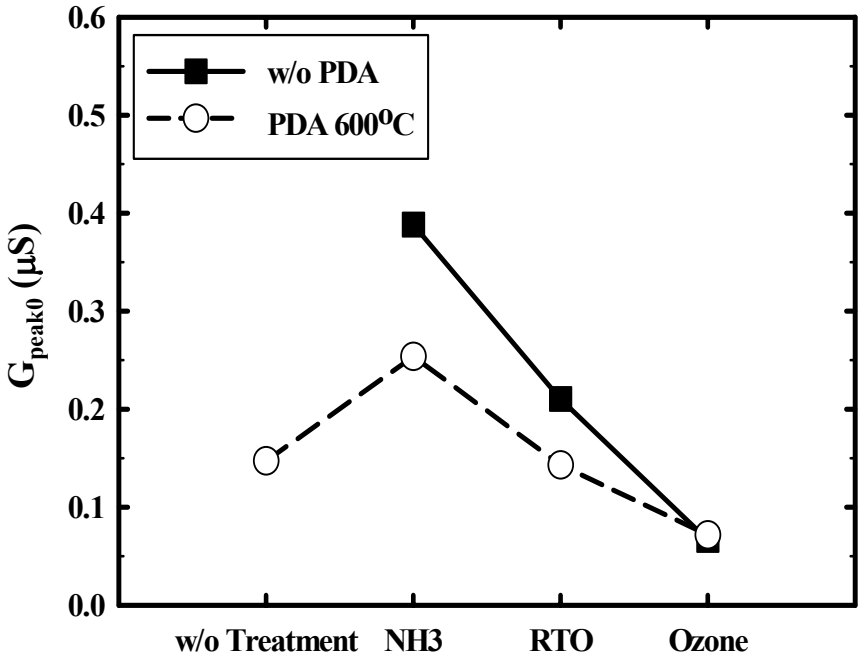


(a)

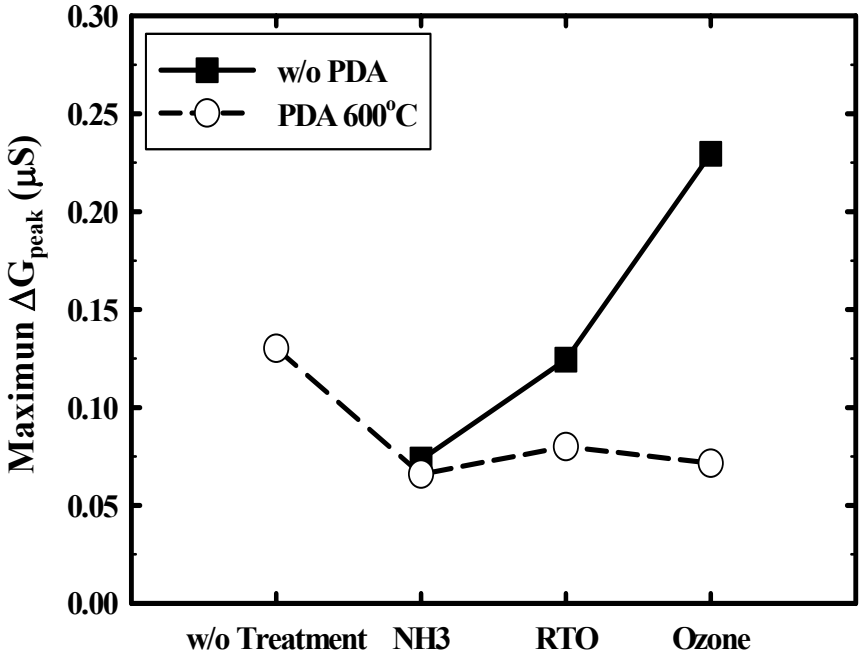


(b)

Fig. 4-7 The changes of the conductance peak value of HfO_2 dielectric (a) without PDA and (b) with 600°C PDA for various surface treatments under a CVS of -3.8V.

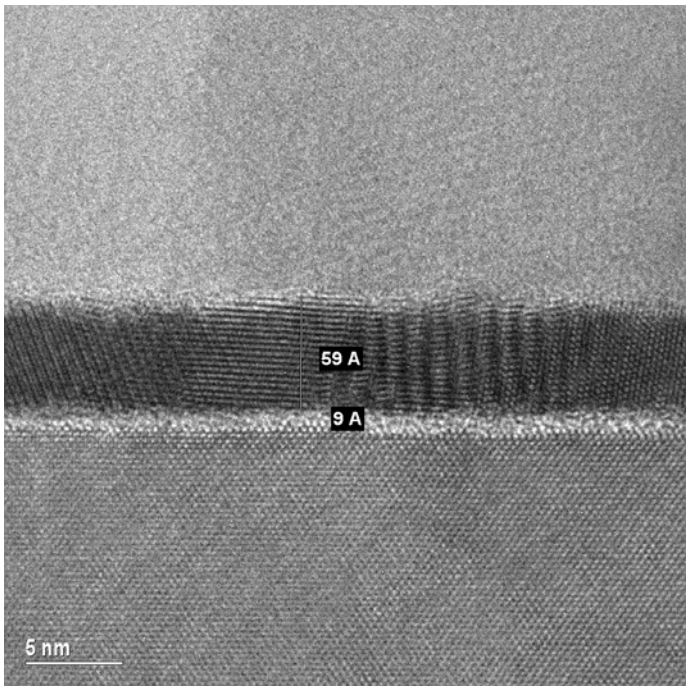


(a)

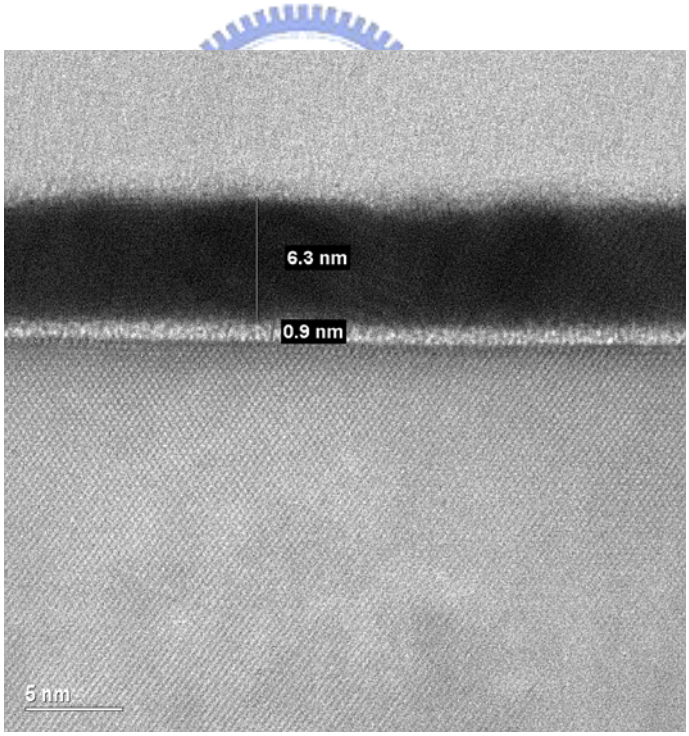


(b)

Fig. 4-8 Comparison of (a) the initial conductance peak value and (b) the change of the conductance peak value after CVS for several surface treatments.

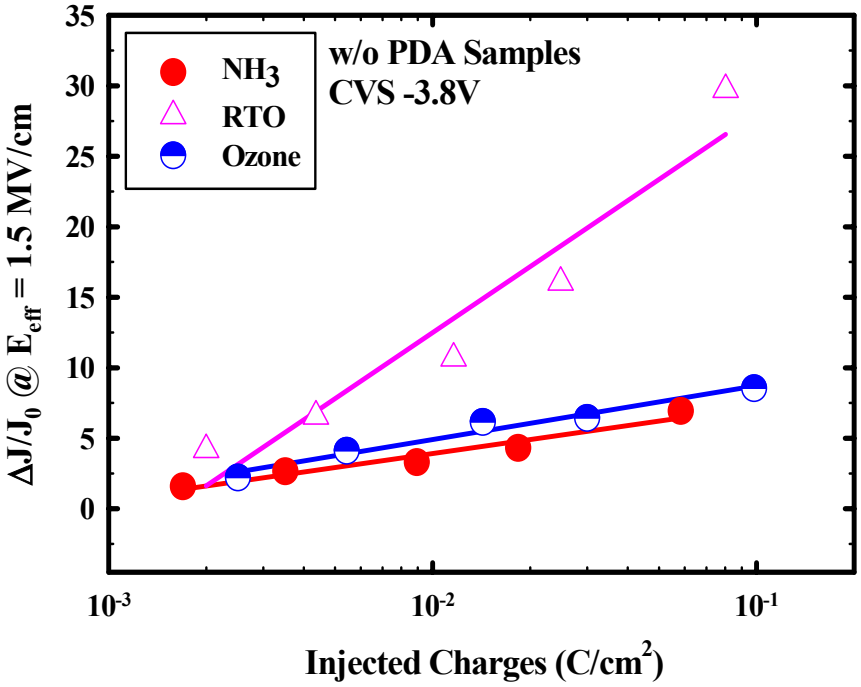


(a)

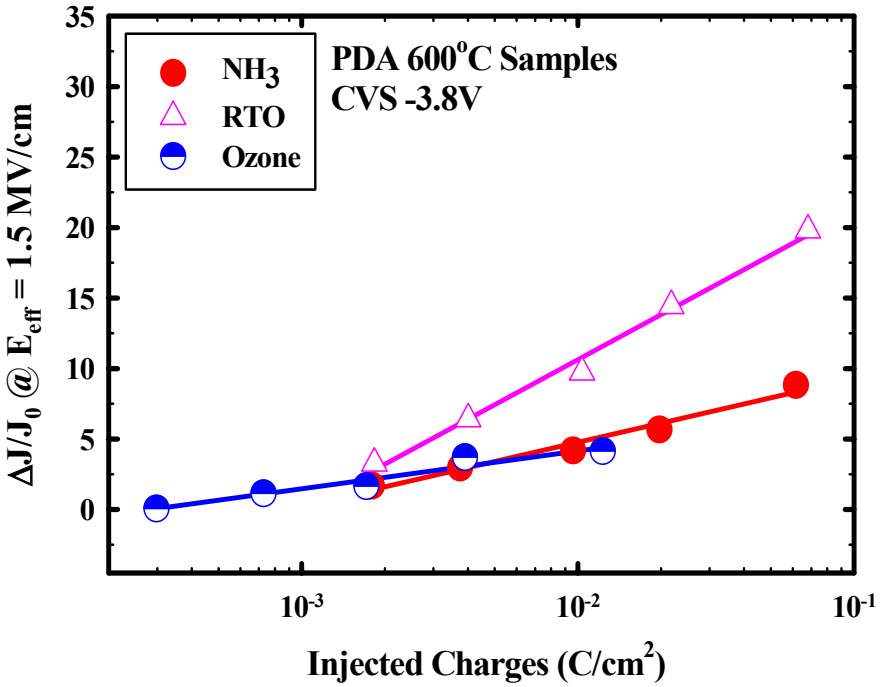


(b)

Fig. 4-9 The HRTEM cross-sectional images of Ozone-treated HfO_2 dielectric (a) without PDA and (b) with 600^{o}C PDA.



(a)



(b)

Fig. 4-10 The SILC ($\Delta J/J_0$) at E_{eff} = 1.5 MV/cm as a function of injected charge of HfO_2 dielectric (a) without PDA and (b) with 600°C PDA under a CVS of -3.8V.

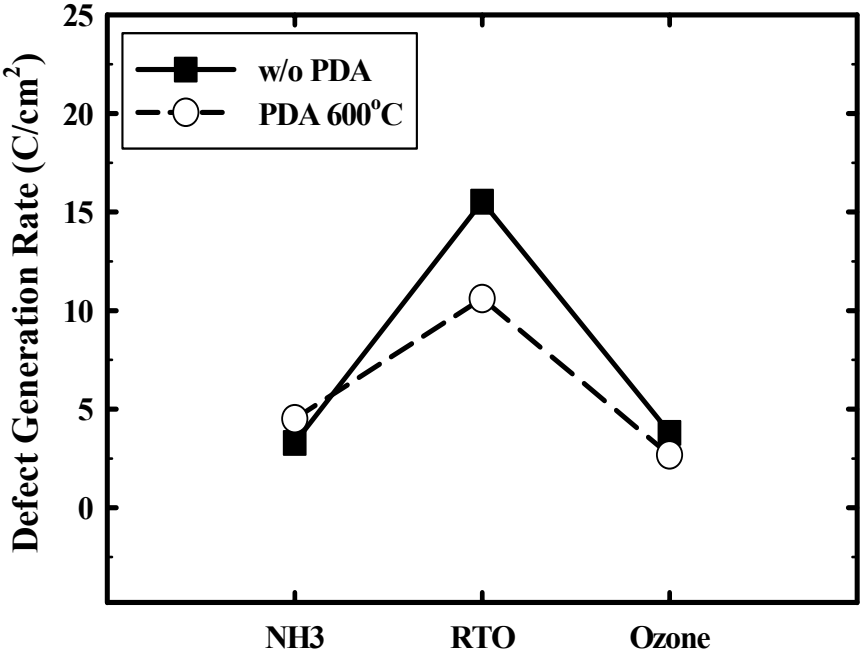
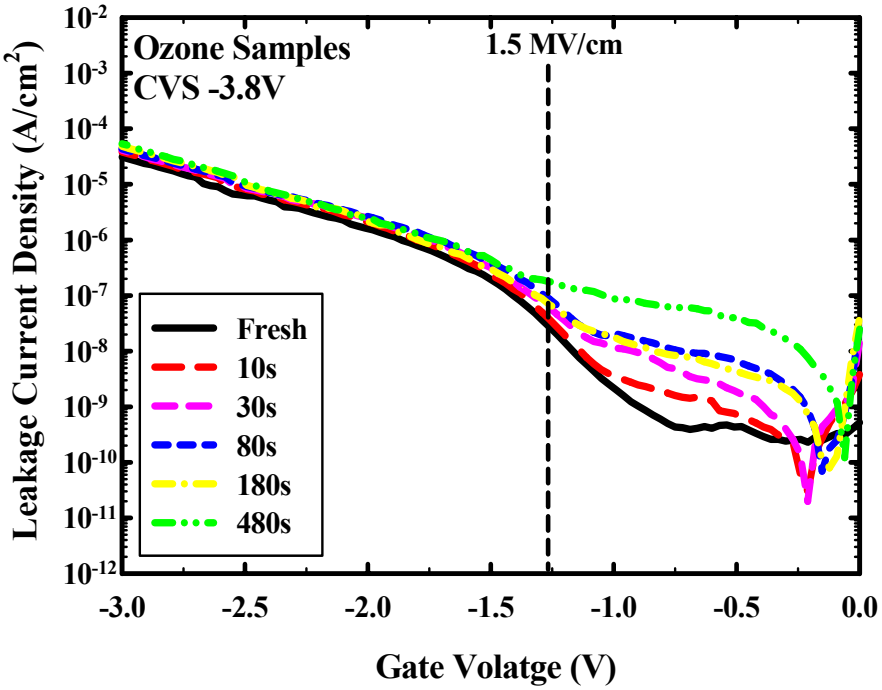
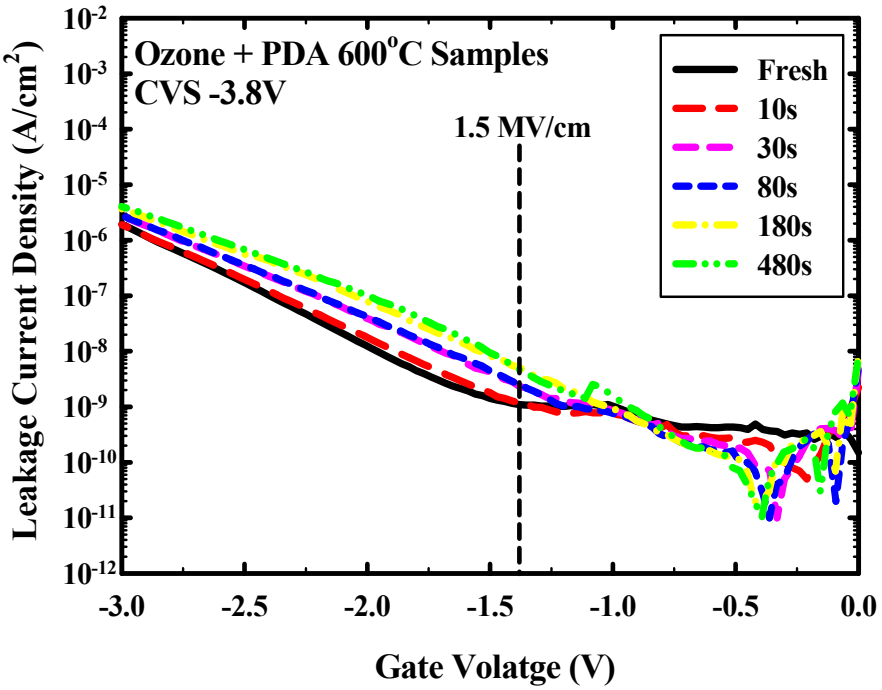


Fig. 4-11 Comparison of the defect generation rates between several surface treatments.



(a)



(b)

Fig. 4-12 The SILC characteristics of Ozone-treated dielectric (a) without PDA and (b) with 600°C PDA under a CVS of -3.8V.

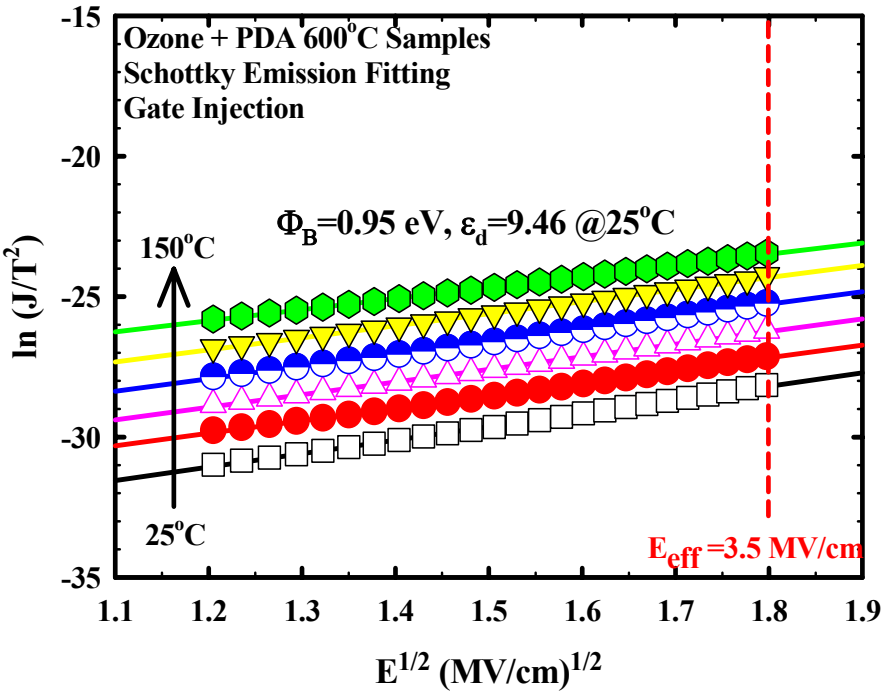


Fig. 4-13 The Schottky emission fitting in the low field range (<3.5 MV/cm) for Ozone-treated dielectric with 600°C PDA.

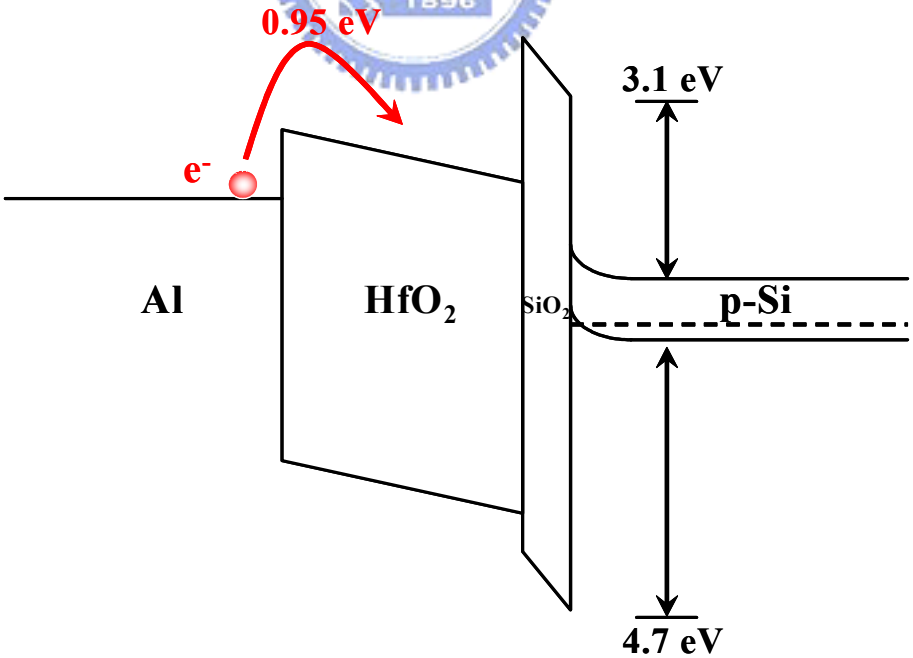


Fig. 4-14 The band diagram of Al/HfO_2/SiO_2/Si capacitor simulated the low electrical field injection condition.

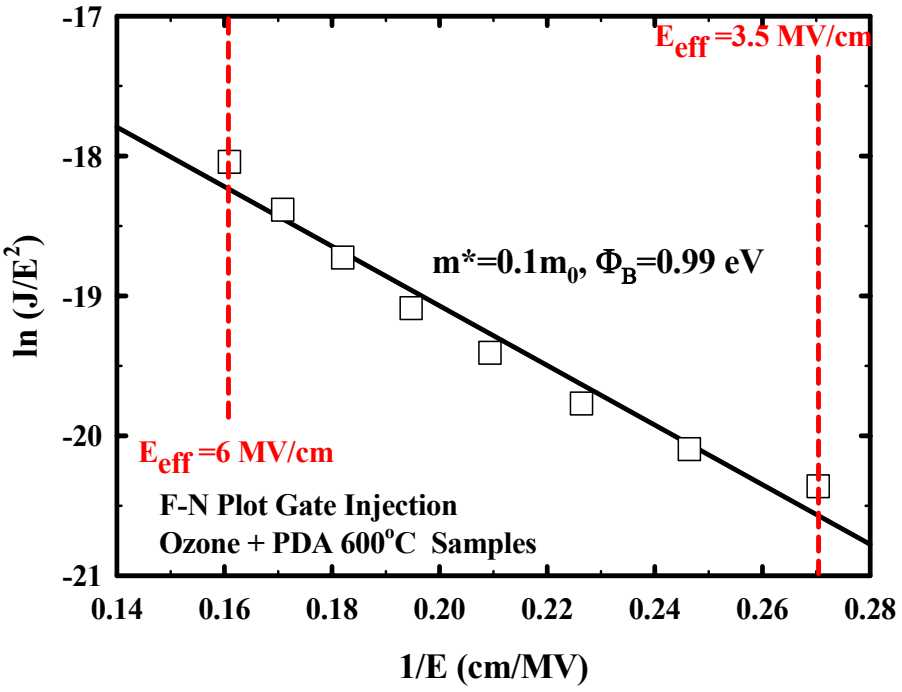


Fig. 4-15 The Fowler-Nordheim (F-N) tunneling fitting in the high field range (>3.5 MV/cm) for Ozone with PDA 600°C samples.

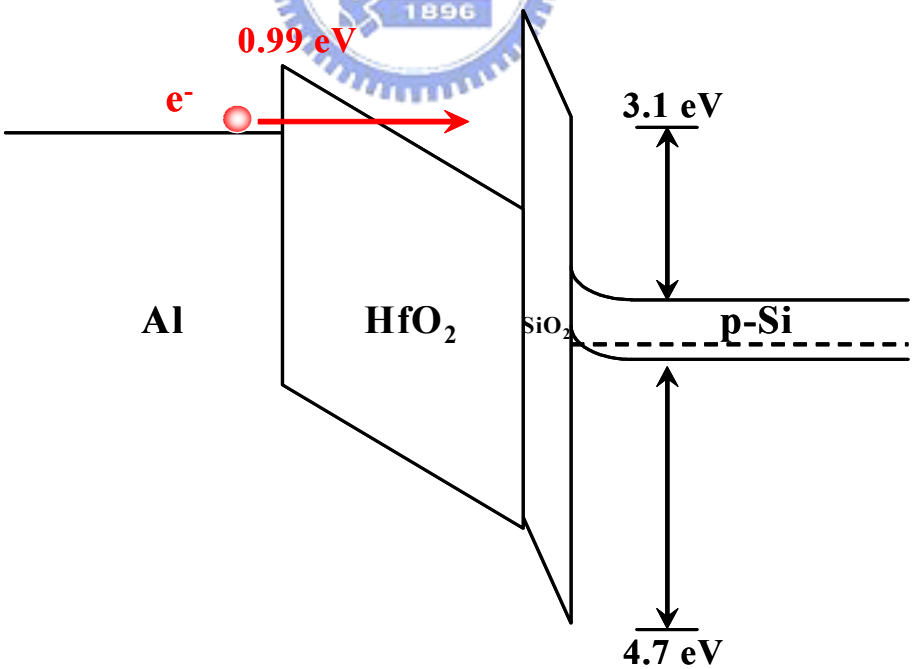


Fig. 4-16 The band diagram of Al/HfO_2/SiO_2/Si capacitor simulated the high electrical field injection condition.

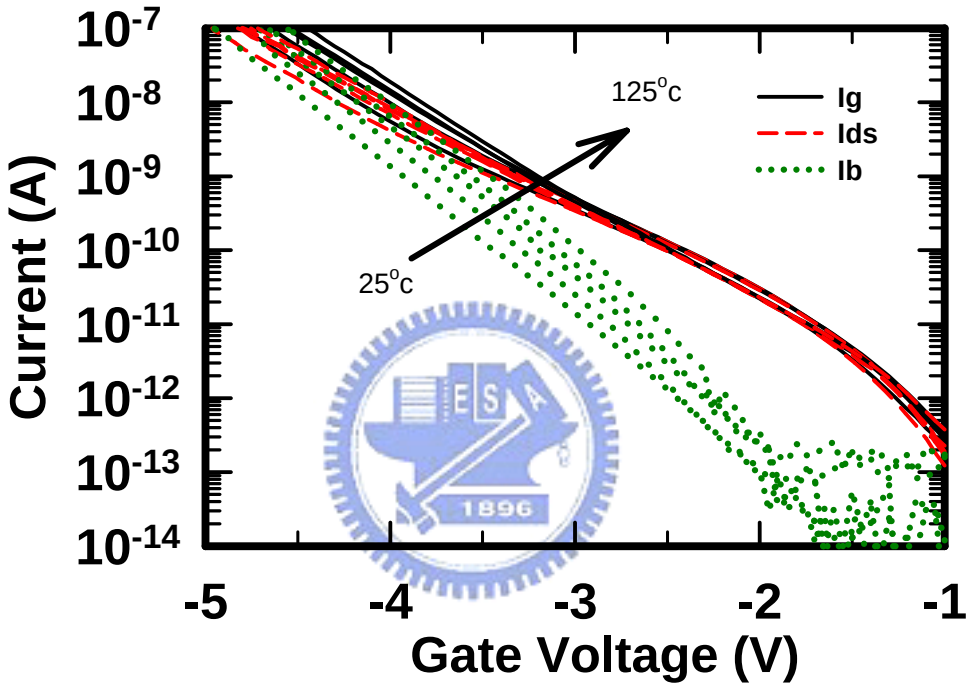


Fig. 4-17 Carrier separation in the temperature dependence measurement [Ref. 64].

CHAPTER 5

Conclusions and Recommendations for Future Works

5.1 Conclusions

Firstly, the effects of O_3 post deposition annealing temperature on the properties of Ta_2O_5 were investigated by COCOS non-contact metrology. The dielectric thickness was increased as raising annealing temperature, which could be ascribed to the thick interfacial layer (IL) growth. A lower κ-value interfacial layer in series would reduce the dielectric capacitance after high temperature annealing. Moreover, the flat band voltage shift changed from positive to negative due to the electron traps elimination and partially hole traps generation in the film. It had been supposed that high temperature ozone annealing could compensate the dangling bond at the interface of Si/Ta_2O_5 proceed to minimize the interface trap density and improve the uniformity. Non-uniform interfacial layer oxidation after O_3 annealing was supposed to cause the increasing of the field strength and break the the soft breakdown distribution.

The basic properties of the ozone oxide were studied first in chapter 3. The growth rate of ozone oxide was increased as raising the ozone quantity contained in DI water. A saturated oxidation was observed in the growth curves and the resultant self-limiting property could improve the thickness uniformity after furnace or/and rapid thermal oxidation. The formation of a more homogeneous structure at the Si/ozone oxide interface performed a higher etching rate for the denser transition layer. Ozone oxide could improve Si surface roughness by 41%, which was beneficial to suppress the leakage current density of the stacked gate dielectric.

Then the influences of surface treatment prior to HfO_2 gate dielectric deposition were investigated. Significantly large fixed charges and hysteresis of NH_3 nitridation would degrade device performance. Albeit RTO treatment exhibited comparable leakage current with Ozone treatment, the time-to-breakdown value was still also less than Ozone treatment. As a result, sample with Ozone treatment revealed small leakage current, negligible hysteresis and excellent dielectric reliability, which was considered to be one of the most potential alternative to improve the interface properties between high-κ dielectrics and silicon surface.

Finally, the surface treatment effects on the charge trapping characteristics the HfO_2 gate dielectric were researched in terms of trapping efficiency, conductance peak shift, and SILC defect generation. Ozone oxide performed the lowest trapping efficiency, D_{it} degradation and defect generation rate after 600^{o}C PDA than NH_3 or RTO treatment partially due to the better interface properties. However, Ozone-samples without PDA expressed poor results, which might be caused by the incomplete oxidation and rougher interface owing to the low growth temperature. The low D_{it} generation and P_g value of NH_3-treated dielectric was ascribed to the strong Si−N bonding at the Si/dielectric interface against the defects creation. Unfortunately, higher interface charges for as-deposited NH_3-treated dielectric would limit nitridation application. RTO also exhibited a poor defect generation resistance than Ozone-treated dielectric. The current transport mechanism was also investigated. When E_{eff}<3.5 MV/cm, the corresponding current transport mechanism was Schottky emission under gate injection conditions. F-N tunneling dominated the conduction mechanism during 6>Eeff>3.5 MV/cm.

5.2 Recommendations for Future Works

1. More HRTEM images to evidence thickness variation and interfacial layer reaction.
2. More physical analysis to understand the properties of the ozone oxide.
3. Fully fabricated MOSFET with high-κ dielectrics and various surface treatment to study the device characteristics.

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