# 國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

# 1.6 Gbps 更低擺幅差動訊號傳輸之傳送器
# A 1.6Gbps RSDS Serial-Link Transceiver

研 究 生　：　鍾竣帆

指導教授　：　吳錦川　教授

中華民國九十四年九月


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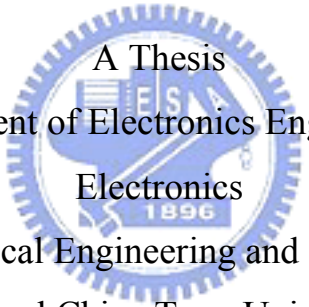

A Thesis

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中華民國九十四年九月

# 1.6 Gbps 更低擺幅差動訊號傳輸之傳送器

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## 摘要

隨著積體電路製程技術的進步,對於需要高頻寬和低延遲晶片之間資料傳輸也隨之增加,傳輸介面的電路所能達到的單位時間最大傳輸量往往是整體系統速度的關鍵限制。

本篇論文是描述一個應用於高速串列數位影像傳輸介面,使用低擺幅差動訊號傳輸之傳送器的設計,並致力於設計兩種資料傳輸速度操作在 1.6Gbps 的傳送器，這兩種傳輸器的差別在於傳輸時脈的不同，第一種傳輸器傳 100MHz 的時脈，第二種傳 800MHz 的時脈。

傳送器由一個八相位鎖相迴路、虛擬隨機位元串列產生器、四對一多工器、時脈處理電路、輸出資料和時脈驅動器所組成，其中，八相位鎖相迴路的輸入頻率為 400MHz,輸出為八個相位，平均分佈且頻率同為 400 MHz 的時脈訊號，所包含的電路有相位/頻率偵測器、電荷幫浦、迴路濾波器、四級差動壓控振盪器和一個除四的除頻器。此鎖相迴路所產生的平均分佈時脈提供給虛擬隨機位元串列產生器和四對一多工器，並將一組並列資料轉為串列輸出，時脈處理電路將時脈處裡過後，最後，將此時脈及串列資料傳送至傳輸線上，即完成整個傳送器的設計。

接收器使用具有磁滯現象的比較器將傳送過來的資料和時脈放大成數位訊

號。然後，第一種接受器使用 100MHz 產生平均分佈且頻率同為 400 MHz 的時脈訊號來取值，

第二種接受器使用輸入資料頻率一半的時脈 800MHz 來取值。最後，解多工器將時脈資料回復電路的輸出轉變成八個平行資料通道。

# A 1.6Gbps RSDS Serial-Link Transceiver

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## Abstract

As the IC fabrication technology advances, the need for high-bandwidth and low-latency inter-chip data transfer has also increased. Most of time, the key limitation of a whole system is the maximum data amounts of the transmission interface circuit transmitted in each unit time.

This thesis describes the design of a high-speed serial link I/O interface. We have devoted to design two types of the transceiver at 1.6Gbps.The difference between Type 1 transceiver and Type 2 transceiver is the frequency of the output clock. Type 1 transceiver transfers 100MHz clock; Type 2 transceiver transfers 800MHz clock.

The transmitter is composed of a eight-phase PLL, PRBS circuits, 4-1 multiplexers, clock process circuit and an output data and clock driver. Among these devices, the input frequency of the eight-phase PLL is 100MHz, and it outputs eight uniformly distributed clocks with 400 GHz frequency. The PLL consists of a

Phase/Frequency Detector, a Charge Pump, a Loop Filter, a four-stage differential VCO and a divided-by-four divider. It offers the PRBS and the 4-1 multiplexer with four uniformly distributed clocks to convert parallel pseudo-data into serial stream. Then, the serial data is transmitted by an output data driver. In the end, the transmitter drives the serial data and clock onto the transmission bus.

The receiver uses the comparator with hysteresis to amplify the incoming data and clock to full swing. Then, Type 1 receiver uses 100MHz clock to generate four uniformly distributed clocks with 400 GHz frequency to sample data. Type 2 receiver uses 800MHz

operating at half of the input data rate Finally, the de-multiplexer converts the serial outputs to four parallel data channels.

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論文研究能夠完成，要感謝在307實驗室的諸多學長，謝謝你們這兩年的指導，並要感謝阿瑞、周政賢、權哲等學長的教導，讓我獲益良多，在此衷心的感謝你們。還要感謝一同在527奮鬥的夥伴，鍵樺、志朋、傑忠、啟佑、靖驊、弼嘉、建樺、阿信、瑋銘、岱原、吳諭，特別感謝同屬吳錦川老師旗下的各位伙伴們，在平時一起研究討論而在研究之餘能夠互相打氣並一同歡樂，使的課業繁重的研究生生活增添了許多的樂趣與活力，

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謹以此篇論文獻給所有關心我的人與我所關心的朋友。

鍾竣帆

國立交通大學

中華民國九十四年九月

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# Chapter 1
# Introduction

## 1.1 MOTIVATION

As the IC fabrication technology advances, the internal clock frequency in microprocessors is up to gigabits-per-second range. However, unlike internal clocks, chip-to-chip or chip-to-board signaling gains little benefit in terms of operating frequency from the increased silicon integration. These advancements have led to some chips being limited by the chip-to-chip data communication bandwidth.

Because of the performance of many digital systems is limited by the interconnection bandwidth between different modules and chips, high-speed data links play a key role of the whole system.

In the last decade, high-speed I/O interfaces were achieved by massive parallelism with the disadvantages of increased complexity and cost for the IC package and the printed circuit board (PCB). However, such method also consumes huge power and induces unavoidable electro-magnetic interference (EMI) during signal transmission.

In order to save power, area and cost, the number of I/O pads in systems should be reduced. Therefore, parallel-based technologies need to be changed to serial-based technologies. The serial link technology can lower the numbers of transmission lines to decrease power, volumes, cost and EMI. The population applications are optical communication, USB, IEEE-1394, TMDS, PECL, LVDS and RSDS.

## 1.2 Thesis Organization

The thesis is organized into six chapters. Chapter 1 introduces the motivation and the organization of this thesis. Chapter 2 describes the background behind this thesis research. It also discusses the reduced-swing differential signaling (RSDS) standard. The detail DC specifications and applications of both standards are presented. In Chapter 3, the conception and architecture of Phase-Locked Loop (PLL) will be described. Chapter 4 shows the whole architecture of the transmitter including the simulation results. Chapter 5 presents the building block of receiver. Chapter is the conclusion of this thesis and shows the future work.

# Chapter 2
# Background

## 2.1 BASIC SERIAL-LINK TRANSCEIVER

### 2.1.1 ARCHITECTURE

The components of basic serial-link transceiver architecture are a parallel-to-serial conversion circuit, a transmitter, a channel, a receiver, and a serial-to-parallel conversion circuit, as shown in **Fig. 2-1**. The data before transmitted are usually parallel data stream in order to increase the bandwidth of the link. Therefore, a parallel-to-serial conversion circuit is needed before sending data to the transmitter. The transmitter converts digital information to analog signal on the transmission medium. This medium which signals travel on is commonly called the communication channel such as the coaxial cable or the twisted pair cable. The receiver on the other end of the channel recovers the signal to the original digital information by amplifying and sampling the signal. The termination resistors which match the impedance of the channel can minimize signal reflection in order to have better signal quality. The clock circuit at the receiver is used to adjust the receiver clock based on the received clock to let the sampling point at the middle of the received data. Then, a serial-to-parallel conversion circuit is used to convert the serial data back to N parallel bits in order to be processed by following digital circuits.

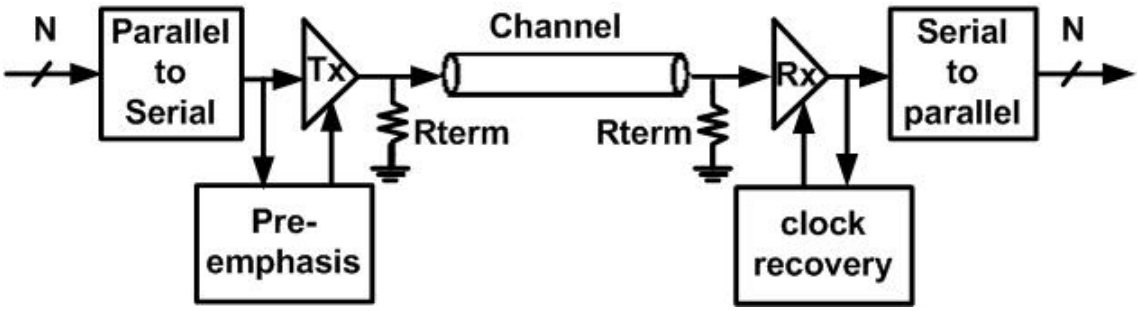


**Fig. 2-1 Block diagram of the basic serial link**

## 2.1.2 HIGH-SPEED AND LOW-POWER TRANSCEIVER CIRCUITS DESIGN

A high performance transceiver circuit must consider speed, power consumption, cost and noise. However, the four factors are trade-off to each other. On balance, the low output signal swing and differential data transmission are the good choice for designing a high performance transceiver circuit. Signals transmitted with low voltage swing can minimize power dissipation and enable operation at very high speed. The differential transmission can provide adequate noise margin in practical systems since signals are transmitted with low voltage swing.

The controversial point is to use the differential transmission. It costs twice of connectors and transmission lines. However, reliable single-ended signals require many ground pins (many high-speed chips provide one ground pin for every two signal pins) and run significantly slower. And for noise concern, any noise that is coupled into both transmission lines of the signal path will be rejected at node 1 and node 2 in receiver, as shown in **Fig. 2-2**, due to the common-mode rejection of the differential amplifier. Besides, for EMI aspect, differential signals tend to radiate less

EMI than single-ended signals due to the canceling of magnetic fields.

There are currently many different transmission technologies that are applied for different I/O interfaces. The comparison between these different transmission technologies is shown in Table 1.2.

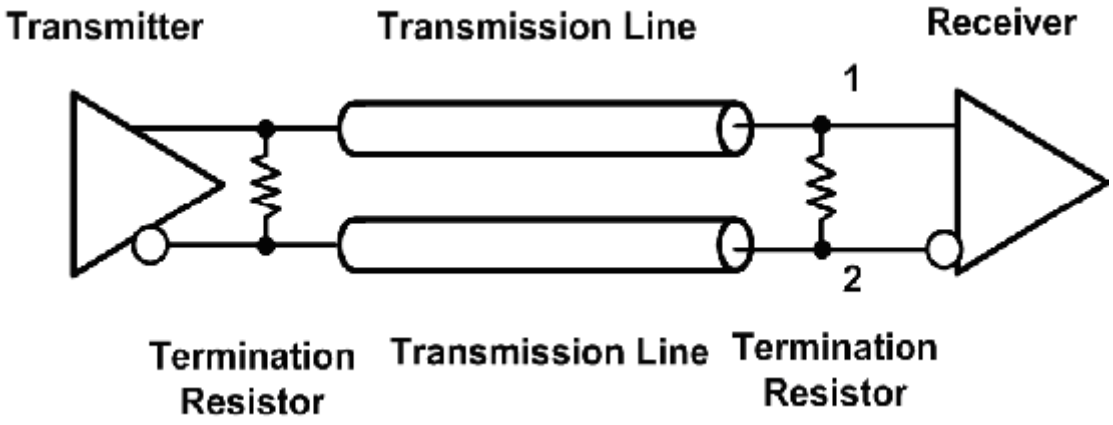


**Fig. 2-2 Reduce noise and suppress EMI effect by using the differential transmission technology.**

# 2.2 Signaling Circuits

The transmitter drives a HIGH or LOW analog voltage onto the channel and is designed for a particular output-voltage swing based on the system specification. The design issues are to maintain small voltage noise and timing noise on the signal. There are two types of output drivers to drive the output: voltage-mode drivers and current-mode drivers. Voltage-mode drivers, as shown in **Fig. 2-3 (a)**, are switches that switch the line voltage. Because the switches are implemented with transistors, the driver appears as a switched resistance. To switch the voltage fully, a small resistance is needed which typically requires a large switching device. In contrast,

current-mode drivers, as illustrated in **Fig 2-3 (b)**, are switching current sources. The output impedance of the driver is much higher than the line impedance. It is also called high impedance signaling. Therefore, the transmitter bandwidth is typically not an issue even with significant output capacitance. The voltage to be transmitted on the line is determined by the switched current and the line impedance or an explicit load resistor. The driver can be simply implemented by biasing the MOS transistor in its saturation region. Current-mode drivers are slightly better in terms of insensitivity to supply-power noise because they have high output impedance and hence the signal is tightly coupled only to $V_{OH}$, the signal return path. The output current does not vary with ground noise as long as the current source bias signal is tightly coupled to the ground signal. The disadvantage with current-mode drivers is that, in order to keep the current sources in saturation, the transmitted voltage range must be well above ground that increases power dissipation.

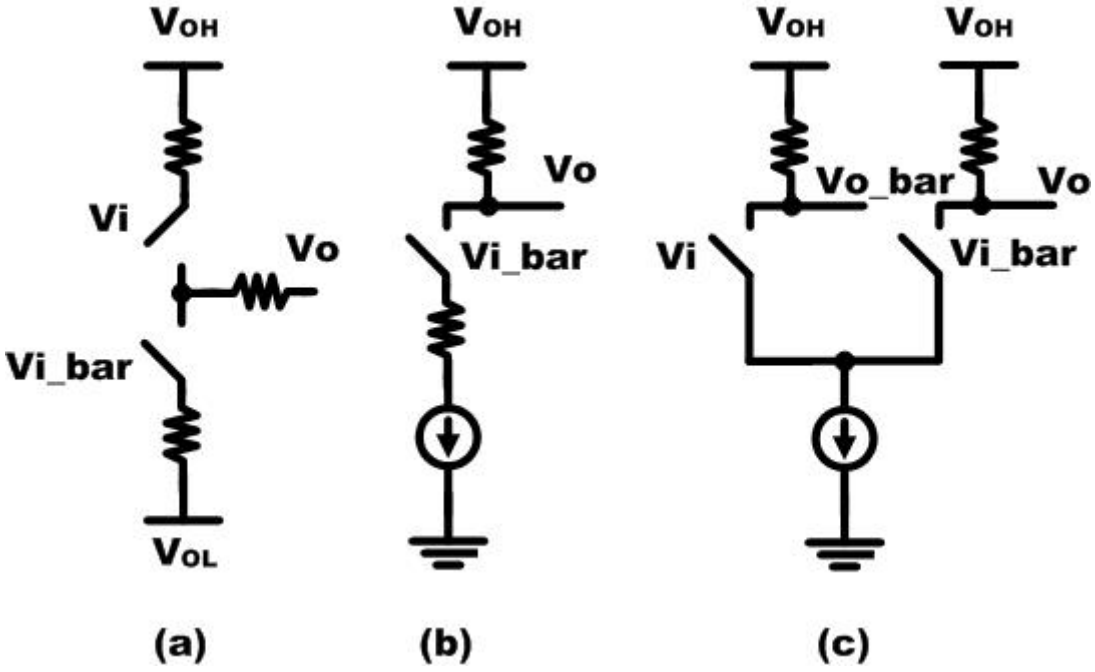


**Fig. 2-3 Transmitter with different transmitter architectures: voltage-mode (a), current-mode (b), and differential (c)**

For better supply-noise rejection, the differential mode can be adopted, as shown in **Fig. 2-3 (c)**, because the supply noise is now common-mode. Since the current remains roughly constant, the transmitter induces less switching noise on the supply voltage that could benefit other transmitted or received signals on the same die. To reduce reflections at the end of the transmission line, the transmitter needs to be terminated. An off-chip termination resistor could introduce significant impedance mismatches because of the package parasitic components. To incorporate the resistor, with current-mode drivers, an explicit on-chip resistor at the driver can act as the termination resistor. If a resistive layer is not available, a transistor in its linear region can be used as the resistor. With voltage-mode drivers, the design is slightly more complex because the switch resistance should match the line impedance $Z_0$. This may be done either through proper sizing of the driver or by over-sizing the driver and compensating with an external series resistor, as shown in the **Fig. 2-3 (a).**

# 2.3 INTRODUCTION TO RSDS

## 2.3.1 Scope

Reduced Swing Differential Signaling (RSDS) is a signaling standard that defines the output characteristics of a transmitter and inputs of a receiver along with the protocol for a chip-to-chip interface between flat panel timing controllers and flat panel column drivers. RSDS technology is originated from the LVDS technology .The RSDS interfaces tend to be used in flat panel display applications with resolutions between VGA (600 × 480 pixels) and UXGA (1600 × 1200 pixels). The RSDS technology provides many benefits to flat panel display applications which include following items:

- Reduced bus width – enables smaller and thinner flat panel column driver boards.
- Low power dissipation – extends system run time.
- Low EMI generation – eliminates EMI suppression components and shielding.
- High noise rejection – maintains signal image.
- High throughput – enables high resolution flat panel displays.

RSDS is a differential interface with a nominal signal swing of 200 mV. It retains the many benefits of the LVDS interface which is commonly used between the host and the panel for a high bandwidth, robust digital interface. The RSDS applications are within a sub-system, the signal swing is reduced further from LVDS to lower power even further.

## 2.3.2 Electrical Specifications and Bus Configurations

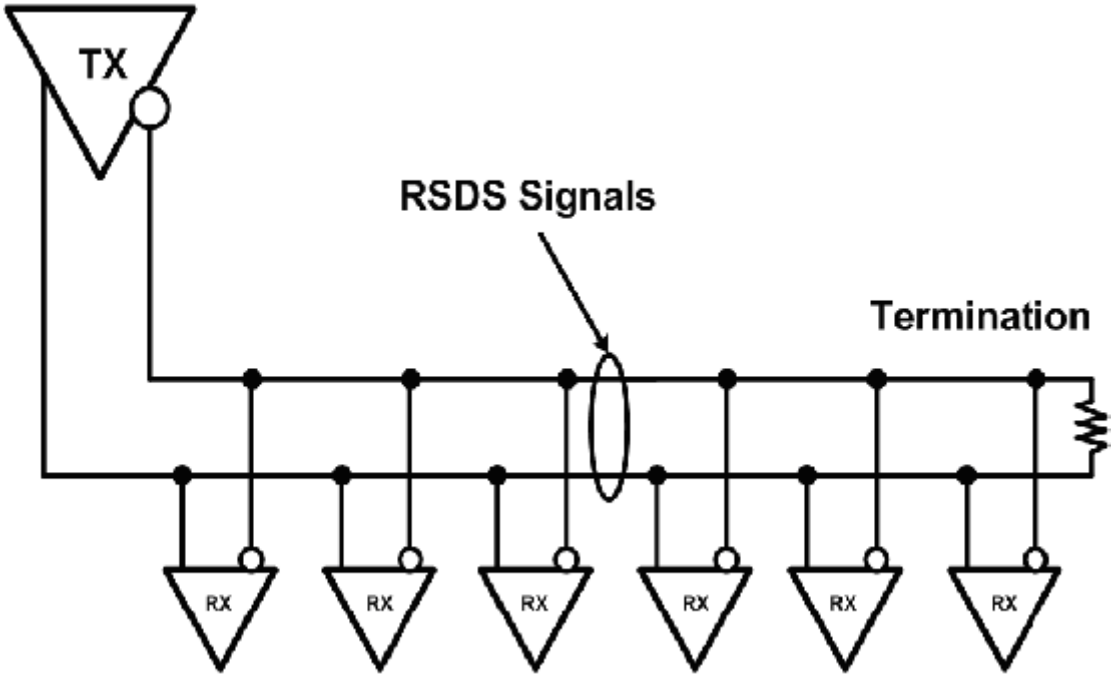


**Fig. 2.4 The RSDS interface configuration. The interface contains three parts: a**

**transmitter, receivers and a balanced interconnecting medium with a termination.**

An RSDS interface circuit is shown in **Fig. 2.4.** The interface contains three parts: a transmitter, receivers and a balanced interconnecting medium with a termination. The transmitter and receiver are defined in terms of direct electrical measurements in **Table 2.1.** The RSDS is a versatile interface that may be configured differently depending upon the end application requirements.

| TX/RX | Parameter | Definition | Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|---|
| TX | $V_{OD}$ | Differential Output Voltage | $R_L$ = 100 Ω | 100 | 200 | 400 | \|mV\| |
| TX | $V_{OS}$ | Offset Voltage | $V_{OD}$ = 0.2 V | 1.1 | 1.3 | 1.5 | V |
| TX | $t_r$ / $t_f$ | Transition Time | | | 2 | | ns |
| RX | $V_{TH}$ | Differential Threshold | | | | ± 100 | mV |
| RX | $V_{IN}$ | Input Range | $V_{ID}$ = 0.2 V | 0.1 | | 1.4 | V |
| – | $R_T$ | Termination | | 95 | 100 | 105 | Ω |
| – | $Z_O$ | Differential impedance of interconnect | | 90 | 100 | 110 | Ω |

**Table 2.1**
**Electrical specifications of RSDS transmitter and receiver**

Considerations include the location of the timing controller (TCON), the resolution and the color depth of the flat panel displays.

The common implementations include the following bus types:

- **Type 1** – Multi-drop bus with double terminations.
- **Type 2** – Multi-drop bus with single end termination.

- **Type 3** – Double multi-drop bus with single termination.

**In a type 1** configuration, the source (TCON) is located in the middle of the bus via a short stub as shown in **Fig. 2.5**. The bus is terminated at both ends with a nominal termination of 100 Ω. The interconnecting medium is a balanced coupled pair with nominal differential impedance of 100 Ω. The number of RSDS data pairs is 9 or 12 depending upon the color depth supported. In this configuration, the RSDS driver which is at the output part of the TCON will see a DC load of 50 Ω instead of 100 Ω.For this case, output drives of the RSDS driver must be adjusted to comply to the $V_{OD}$ specification with the 50 Ω load presented by the type 1 configuration.

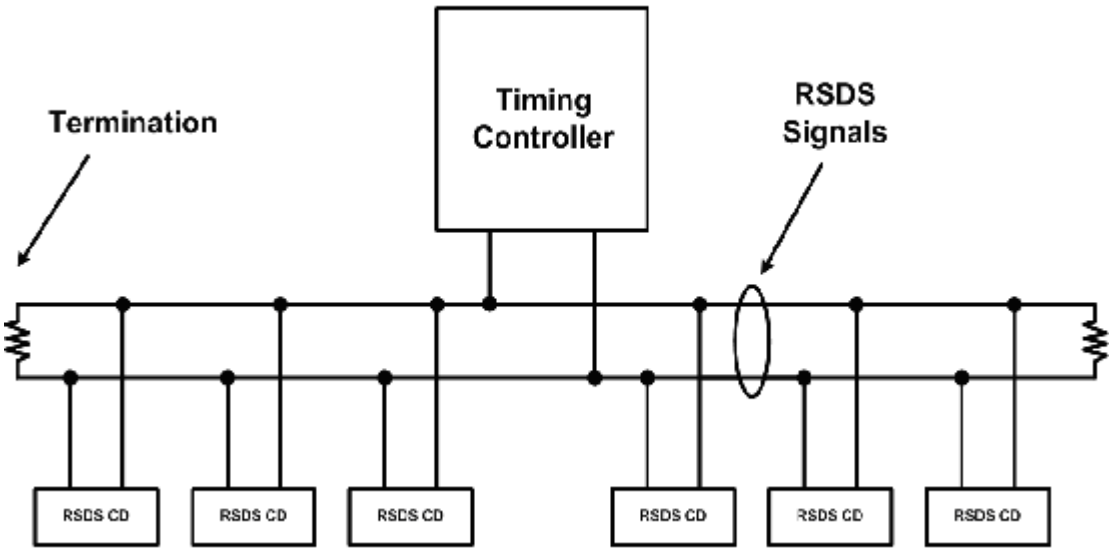


**Fig. 2.5 Type 1 bus configuration of RSDS.**

**In a type 2 configuration**, as shown in **Fig. 2.6**, the source (TCON) is located at one end of the bus. The bus is terminated at the far end with a nominal termination of 100 Ω. The interconnecting medium is a balanced coupled pair with nominal differential impedance of 100 Ω. The bus may be a single or dual bus depending upon the resolution of flat panel displays. The number of RSDS data pairs is 9 or 12

depending upon the color depth supported for a single bus. Or the number of RSDS data pairs is 18 or 24 depending upon the color depth supported for a dual bus.

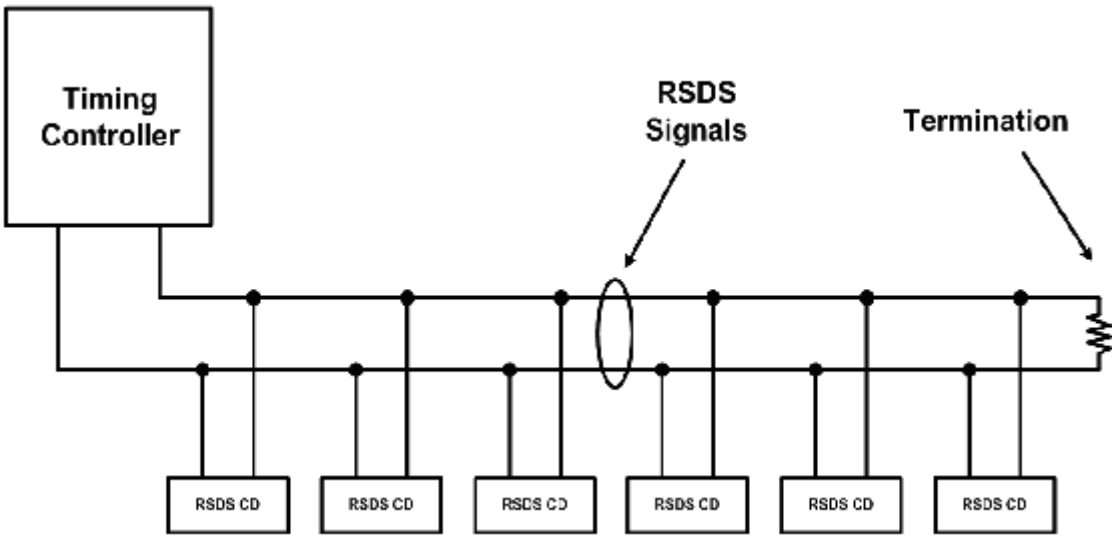


**Fig. 2.6 Type 2 bus configuration of RSDS.**

**In a Type 3** configuration, the source (TCON) is located in the center of the application. There are two buses out of the TCON that run to the right and left respectively. Each bus is terminated at the far end with a nominal termination of 100 Ω. The interconnecting medium is a balanced coupled pair with nominal differential impedance of 100 Ω. The number of RSDS data pairs is 9 or 12 depending upon the color depth supported for a single bus for each bus. The connection of the TCON to the main line is not a stub in this configuration, but rather is part of the main line. This helps to improve signal quality as shown in **Fig. 2.7.**

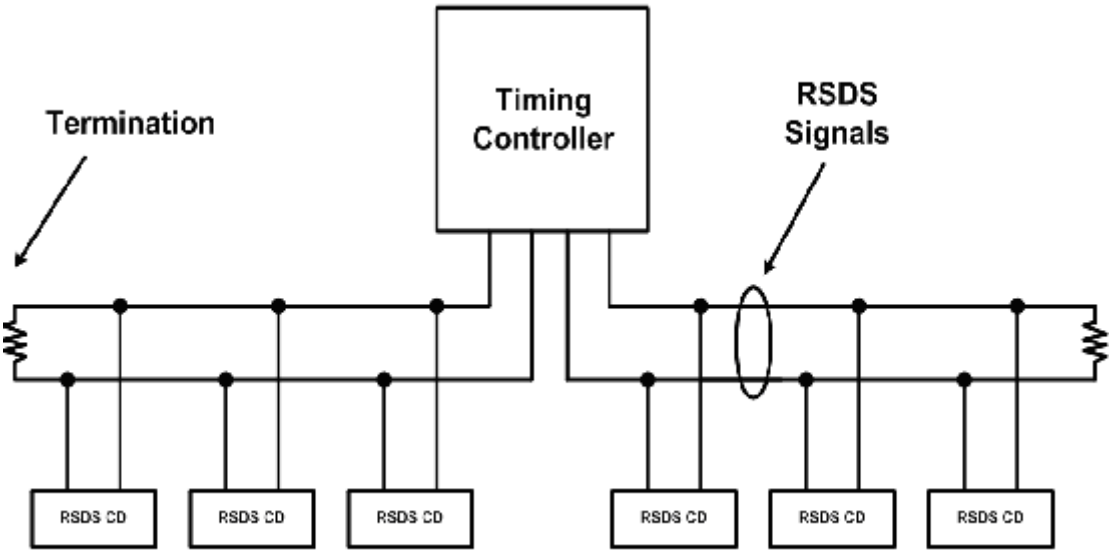


**Fig. 2.7 Type 3 bus configuration of RSDS.**

From **Fig. 2.5** to **Fig. 2.7**, the complete bus is not illustrated, only a single RSDS pair is shown. The number of column drivers on the bus is also application specific and depends upon the resolution of flat panel displays

## 2.3.3 Applications

RSDS like its predecessor LVDS, originated from the unique need of the LCD manufacturers for on glass interface with higher speeds, reduced interconnects, lower power, and lower EMI. As shown in **Fig. 2.8**, the RSDS drivers are embedded at the output of the flat panel timing controller and the RSDS input buffers are at the input of the flat panel column drivers. Since this new technology also uses a low voltage differential swing (+/- 200 mV), lower EMI and lower power consumption can also be realized. Also due to its low voltage swing (versus TTL), faster clock rates can be achieved and thereby enabling higher resolution of FPDs in the future. At present clock rates of 65 MHz have been EMI qualified in pre-production TFT LCD modules

with relative ease when compared to their TTL counter parts. In the near future, higher clock rates in excess of 85 MHz or even 100 MHz plus can be expected. Since this interface is a serial interface, overall bus width is also reduced by half of the conventional TTL bus architecture. In a TTL 6 bit/color dual bus architecture, a total of 36 data lines plus 2 clock signals are required, for a total of 38 conductors. In an equivalent RSDS architecture, only one bus consisting of a total of 9 differential pairs of data lines plus a differential clock pair are required, for a total of 20 conductors. When implementing the same system with RSDS, an overall reduction of 47 % in bus conductors are achieved thereby enabling a small outline PCBs.

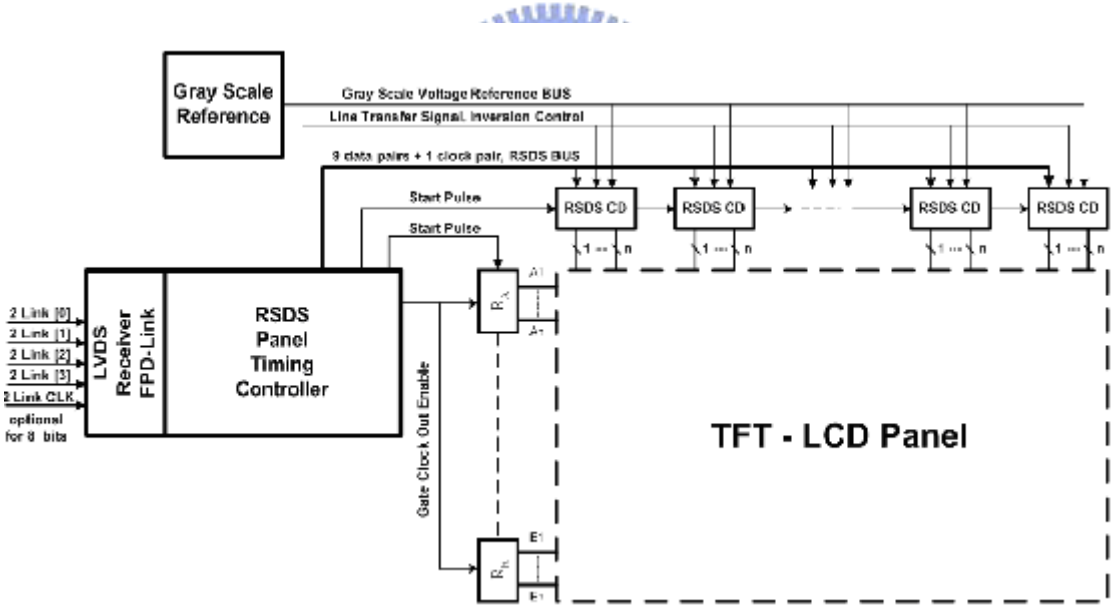


**Fig. 2.8 The RSDS interface utilized in the flat panel display systems.**

## 2.4 Basic Link Design

A general serial link is composed of three primary components：a transmitter, channels, and a receiver, as shown in Fig. 2-7. The data before transmission are usually arranged in parallel form in order to increase the bandwidth of the link. The transmitter has to convert the parallel data into serial stream before the output driver drives signals onto the channels. RSDS$^{TM}$ uses differential data transmission to deliver the serial data stream and the transmitter is configured as a switched-polarity current generator. A differential load resister at the receiver end provides current-to-voltage conversion. For operation in the Gbps range, an additional termination resistor is usually placed at the source (transmitter) end to suppress reflected waves caused by crosstalk or by imperfect termination, due to package parasitic effect and component tolerance. Moreover, RSDS$^{TM}$ uses a lower voltage swing to achieve further advantages in terms of reduced crosstalk and radiated EMI. Therefore, the double termination scheme is used and the termination resistors are integrated in the transmitter ($R_{T-T}$) and in the receiver cell ($R_{T-R}$) [5].

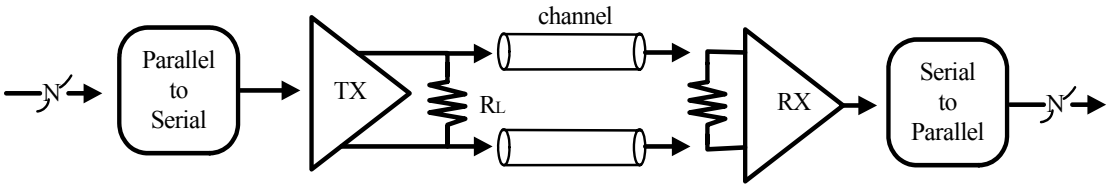


**Fig. 2.9 Block diagram of the basic serial link**

After the data are transmitted onto the channels successfully, the receiver amplifies and samples the received bit stream. The clock recovery circuit restores the clock of transmitter by detecting the transition edge of received data. Eventually, the receiver gets back the correct data by sampling the center point of the received bit stream at each transition edge of the recovered clock.

# Chapter 3
# Phase-Locked Loop

## 3.1 Introduction

Phase-locked loop (PLL) is an analog building block used extensively in many analog, digital and communication systems. PLL causes a particular feedback system to track with another one. More precisely, a PLL is a circuit synchronizing an output signal with a reference or an input signal in frequency as well as in phase. It is undoubted to say that PLL has become an important building block in many electronic systems. This chapter will introduce the architecture of the PLL .It needs a reference input clock signal at 100 MHz, and then produces a output clock signal at 400 MHz. By adopting four differential stages in voltage controlled oscillator, it generates eight clock phases for the use of the multiplexer in transmitter and sampling clock phases for the samplers in receiver.

In the following section, we consider the linear model, the noise and the stability. In order to design a PLL quickly, the design flow and the way to decide the loop parameter are described in the next section. In the end, we show the simulation results as an ending of this chapter.

# 3.2 Architecture of PLL

A phase-locked loop (PLL) is basically an oscillator whose phase and frequency is locked to those of the input signal. This is done by using a negative feedback control loop, as shown in **Fig. 3-1**, which includes a phase/frequency detector (PFD), a charge pump circuit (CP), a loop filter (LF), a voltage controlled oscillator (VCO), and a frequency divider (divided by N). The PFD is used to compare the feedback signal (Fback) from the output signal of divider with the input reference signal (Ref), and generates the Up and Downb signal to the following charge pump circuit. Based on Up and Downb input signals, the charge pump begins to charge or discharge the loop filter to change the input control voltage (Vctrl) of the VCO which varies the frequency of the output signal (Clk). The loop filter is basically a low pass filter used to filter out the high frequency component coming from the PFD and charge pump. In this way, the frequency of the feedback signal can be adjusted to be the same with the reference signal through the feedback control loop. In steady state, the frequency of the output signal will be N-times of the input signal. Moreover, the input reference signal (Ref) and the feedback signal (Fback) are phase-aligned.

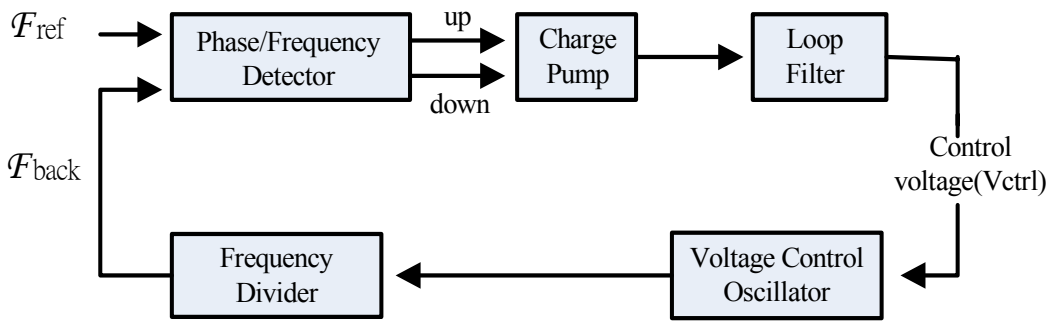


**Fig 3-1 Basic PLL Architecture**

# 3.3 Circuit Implementation

## 3.3.1 Phase-Frequency Detector

The phase frequency detector (PFD) is a digital sequential circuit which employs a tri-state operation. It is triggered by the two positive clock edges of the reference (Ref) and the feedback signals. **Fig 3-2** shows its behavior. If the reference clock leads the feedback clock, the UP signal will be set from low to high. This will in turn increase the frequency of the voltage controlled oscillator output signal. When the feedback signal's rising edge arrives, the reset signal will be high to reset UP signal to the low. In contrast, if there reference clock lags the feedback clock, the Down signal will be set to high, until the reference signal triggers the reset signal. This Down signal, on the contrary, is used to decrease the frequency of the voltage controlled oscillator output signal.

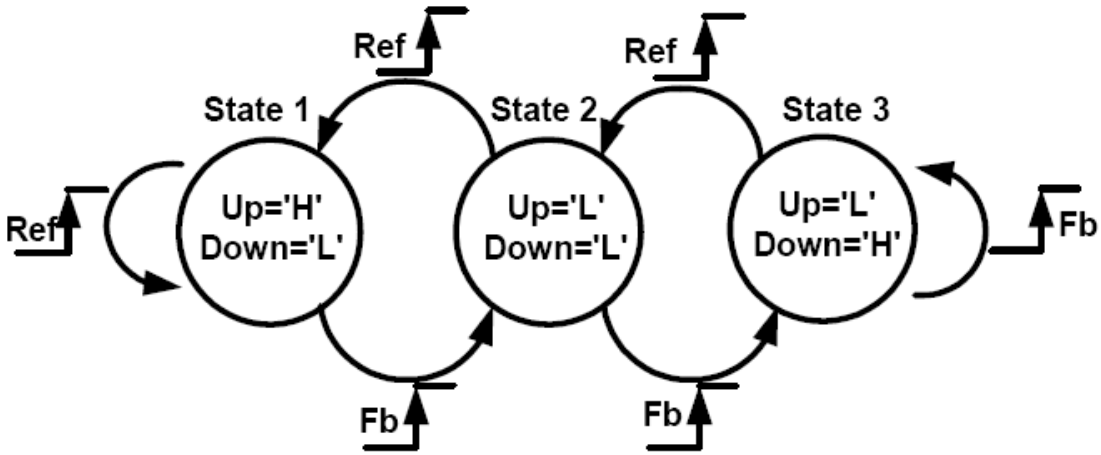


**Fig 3-2 State Machine of PFD**

This three-state operation has a linear range of $\pm 2\pi$ radians and can act as both phase detector and frequency detector. This property will greatly enhance the locking-time. As shown in **Fig. 3-3**, the PFD could be implemented simply by two dynamic D flip-flops and one AND gate. The D flip-flop schematic is shown in **Fig. 3-4.**

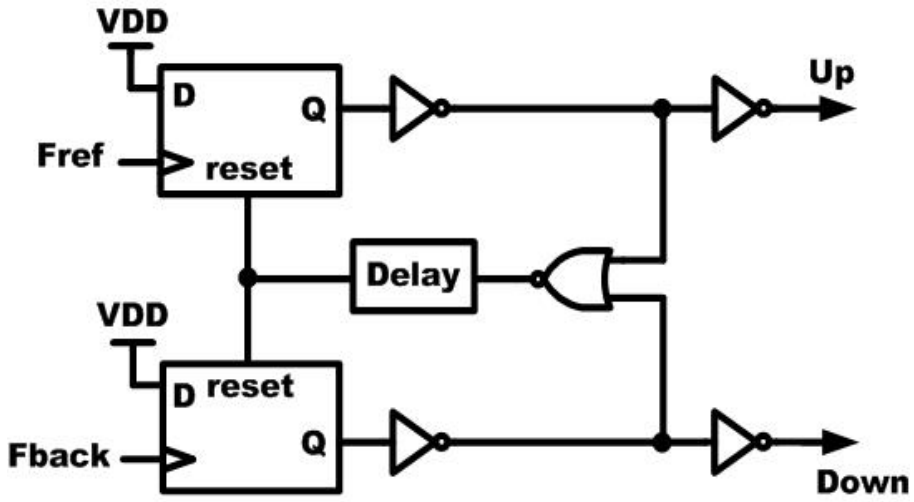


**Fig 3-3 PFD Implementation**

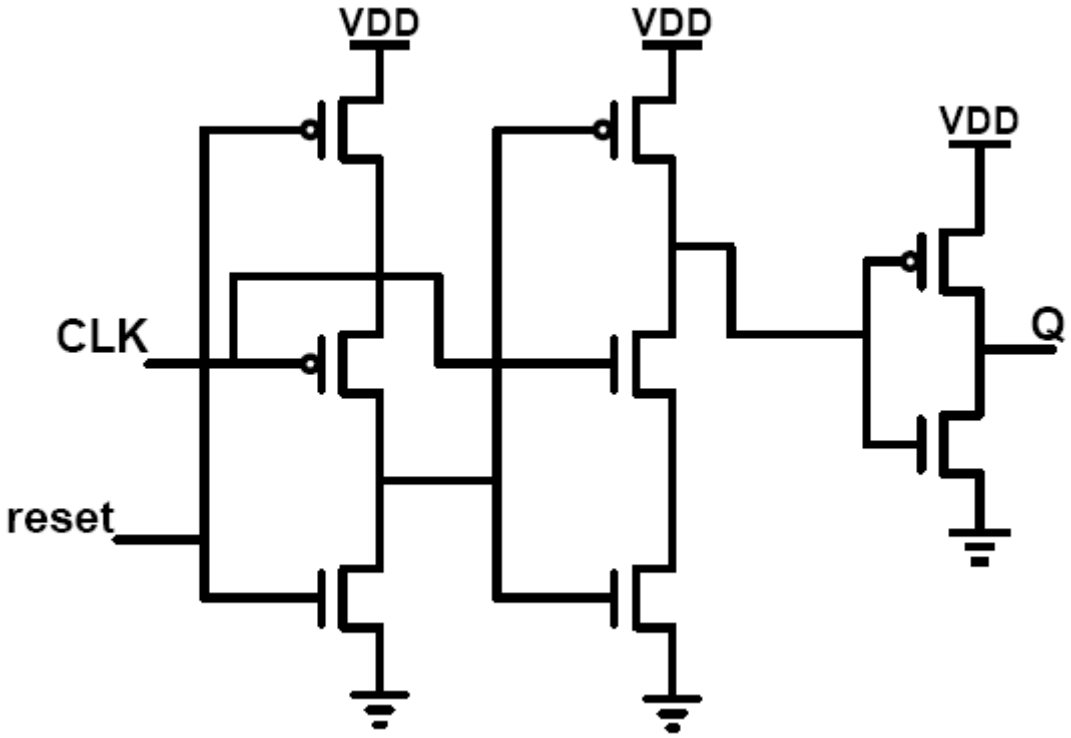


**Fig 3-4 TSPC D-FF in PFD**

Ideally, the PFD should have the ability to distinguish any phase error between reference and feedback signals. In practical, when the phase error is too small, the reset signal is so fast that the following charge pump circuit will not be activated. This will result in dead zone region (undetectable phase difference range). A low precision PFD has a wide dead zone as shown in **Fig. 3-5**, which results in increased jitter. The dead zone is highly undesirable because it allows the VCO to accumulate as much random phase error as the phase difference with respect to the input while receiving no corrective feedback.

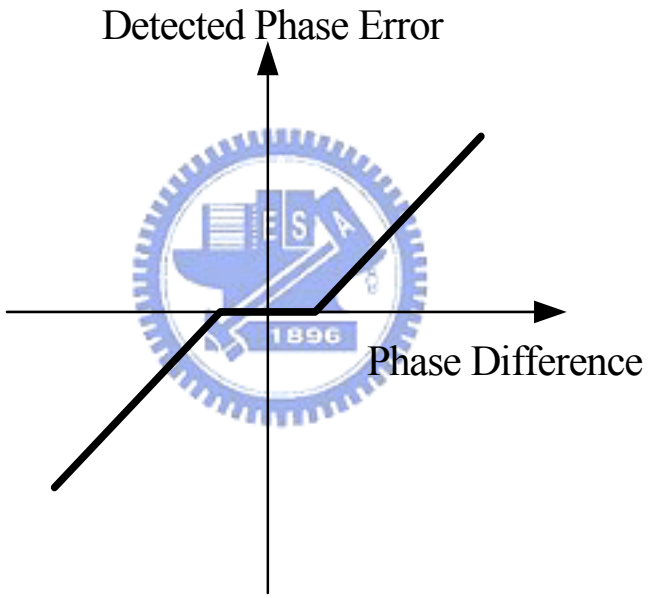


**Fig 3-5 Dead Zone of PFD**

Equal and short duration pulses at the UP and DOWN outputs of the PFD are needed for in-phase inputs in order to eliminate a dead zone region in the PFD as seen by the charge pump. The dead zone region could be eliminated by adding extra delay buffers in the reset path to ensure that when both reference and feedback signals are at the same phase, there would be equal and activated pulses at the output. The elimination of the dead zone region results in overall linear operating characteristics

for the PFD, especially for input signals with small but finite phase difference. However, inserting the delay buffers will limit the maximum operation frequency that is in inverse proportion to the total reset path delay. **Fig 3-6** shows the SPICE simulation result of the proposed PFD circuit.

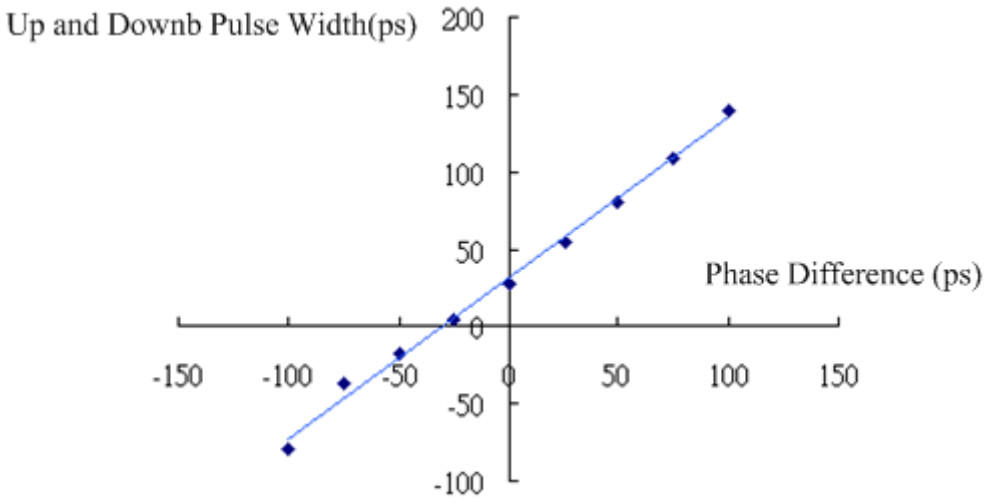


**Fig 3-6 simulation result of PFD without dead zone**

## 3.3.2 Charge Pump

The schematic of the charge pump circuit is shown in **Fig 3-7.** The two switch devices are separated from the output voltage. Therefore, the output voltage is now isolated from the switching noise resulting from the overlap capacitance of the two switch devices. In addition, the intermediate node between the current source and switch devices will charge to the output voltage only by the gate overdrive of the current source devices, Vgs – Vt, an amount independent of the output voltage. Moreover, since both the NMOS and PMOS current sources always turn on in each

cycle, any charge injection will cancel out to first order with equal current source device sizes.

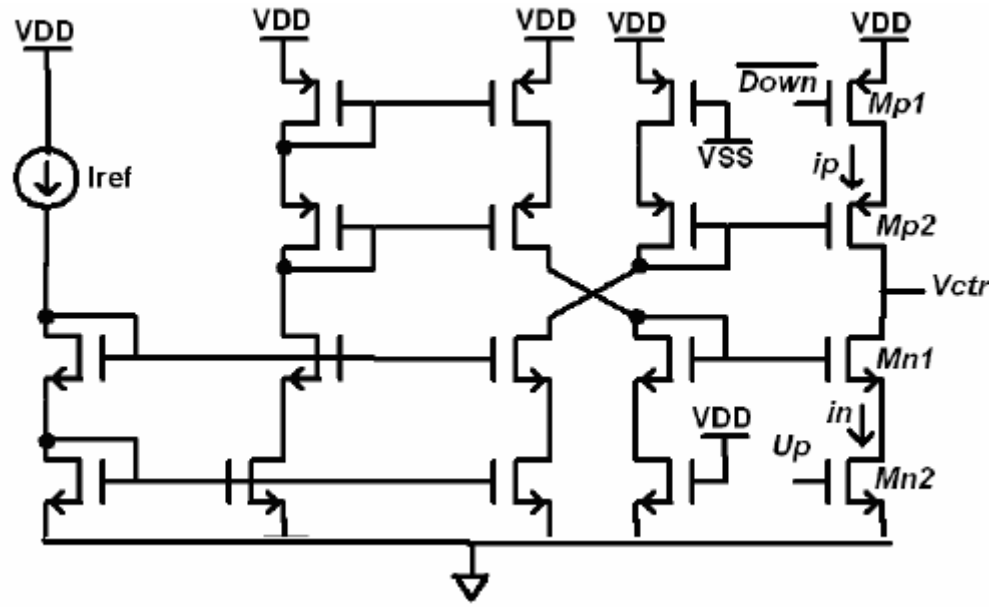


**Fig 3-7 Schematic of the Charge Pump**

## 3.3.3 Loop Filter

The loop filter used in the charge pump PLL is shown in **Fig 3-8**. It has a lead-network consisting of a resistor R1 in series with capacitor C1 and a capacitor C2 in parallel. The lead-network filter provides a pole in the original to provide an infinite DC gain to get the zero static phase error, and a zero in the open loop response in order to improve the phase margin to ensure overall stability of the loop. The transfer function of the filter is given by

$$F(s)=\frac{Kh\times(S+\omega_z)}{S}$$

Where

$$\omega_z = 1/R_1C_1, \quad Kh = R_1$$

Capacitance C2 is used to provide higher-order roll off for reducing the ripple noise to mitigate frequency jump. The total transfer function of the loop filter is

$$F(s) = \frac{Kh \times (S + \omega_z)}{S \times (1 + S/\omega_P)}$$

Where

$$\omega_z = 1/R_1C_1, \quad \omega_P = \omega_z \times (1 + C2/C1), \quad Kh = \frac{R1 \times C1}{C1 + C2}$$

But the adding of the capacitance C2 will make the overall PLL system become third-order one and affect the stability of the loop. In general, by setting C1>20×C2, the third-order can be approximated to second-order loop.

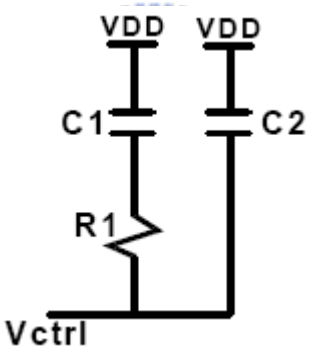


**Fig 3-8 Loop Filter**

## 3.3.4 Voltage Controlled Oscillator

In order to have the low jitter characteristics of the output clock, the delay buffer used in voltage controlled oscillator (VCO) should have low sensitivity and high noise rejection capability of the supply and substrate voltage. The basic building block of the VCO used in this thesis is based on the differential delay stages with symmetric loads and replica-feedback biasing. The building blocks of the VCO include a four stages ring oscillator and a self-biased replica-feedback bias generator. **Fig 3-9** shows

VCO delay cell.

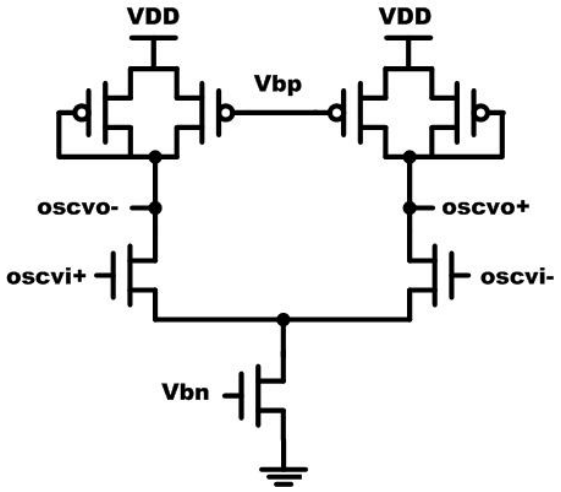


**Fig 3-9 Schematic of the four stages VCO and the delay cell**

As shown in **Fig. 3-9**, the buffer stage contains a source-coupled pair with diode-connected PMOS devices as resistive loads in shunt with an equally sized PMOS device. The control voltage, Vbp, is the bias voltage for the PMOS device. It is also used to generate the bias voltage for the NMOS current source and provides the control over the delay of the buffer stage. In order to provide a bias current that is independent of the supply and substrate noise, the bias voltage of the NMOS current source, Vbn, will be continuously adjusted. **Fig.3-10** shows the I-V characteristics of the symmetric load.

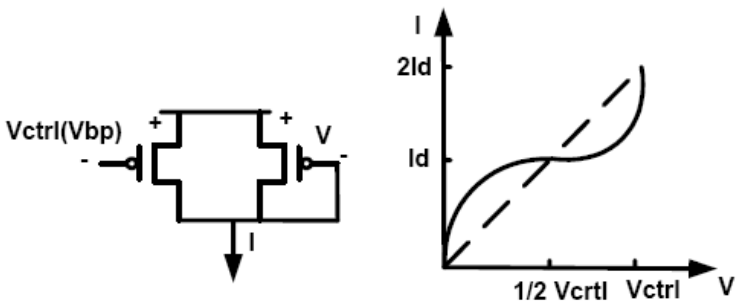


**Fig 3-10 I-V curve of the symmetric load**

Basically, to get the high noise rejection capability over the supply and substrate noise, the load of the differential pair should have a linear I-V characteristic. In practice, this is difficult to use MOS device to achieve it. But the symmetric load can cancel the first order of the common mode voltage noise. Therefore, the symmetric load here, though nonlinear, could be used to have high dynamic supply noise immunity. The control voltage, Vbp, is the bias voltage for the PMOS device. In order to provide a bias current that is independent of the static supply noise, the bias voltage of the NMOS current source, Vbn, will be continuously adjusted. As the supply voltage changes, the drain voltage of the NMOS current source also changes. However, the gate bias is adjusted by the replica-feedback bias generator to keep the output current constant. It seems that it makes the output resistance of the NMOS current source higher. Hence the static supply noise is greatly improved.

Based on the analysis of the I-V curve, it can be shown that the effective resistance of a symmetric load ($R_{eff}$) is directly proportional to the small signal resistance at the ends of the swing range which is just one over the transconductance (gm) for one of the two equally sized PMOS biased at Vctrl. Therefore, the buffer delay is

$$t_d = R_{eff} C_{eff} = \frac{1}{g_m} C_{eff} \tag{3-1}$$

where $C_{eff}$ is the effective buffer output capacitance. The drain current for one of the two equally sized devices biased at Vctrl is

$$I_d = \frac{kp}{2}\left[\left(V_{DD} - V_{ctrl}\right) - \left|Vtp\right|\right]^2 \tag{3-2}$$

Taking derivative with respect to Vctrl, the transconductance gm is given by

$$g_m = kp\left[\left(V_{DD} - V_{ctrl}\right) - \left|Vtp\right|\right] \tag{3-3}$$

The buffer delay is then given by

$$f_{osc} = \frac{1}{2Nt_d} = \frac{kp\left[\left(V_{DD} - V_{ctrl}\right) - \left|Vtp\right|\right]}{2NC_{eff}} \tag{3-4}$$

The gain of the VCO is given by

$$K_{vco} = \frac{df_{osc}}{dV_{ctrl}} = \frac{-kp}{2NC_{eff}} \tag{3-5}$$

As a result, Kvco is independent of the buffer bias current and the VCO has first order tuning linearity.

$$t_d = \frac{C_{eff}}{kp\left[\left(V_{DD} - V_{ctrl}\right) - \left|Vtp\right|\right]} \tag{3-6}$$

The bias generator of the VCO delay cell is shown in **Fig 3-11**. It provides the output bias voltage Vbp and Vbn from input signal Vctrl. The primary function is to continuously adjust the VCO delay buffer bias current to provide the correct lower swing limit Vctrl for the VCO delay buffer stages. As a result, it builds up a current that is held constant and independent of supply voltage. The bias generator consists of a PMOS source coupled differential pair, a half-buffer replica, and a control voltage buffer. The differential amplifier is actually a unity-gain buffer which forces the voltage of node Va in **Fig 3-11** equal to Vctrl, a condition required for correct symmetric load swing limits, and provide the bias voltage Vbn for the NMOS current source. Besides, the bias voltage, Vbn**,**is dynamically adjusted by the differential amplifier to increase the supply noise immunity. With the half-buffer replica, the net result is that the output current of the NMOS current source is established by the load

element and is independent of the supply voltage. If the supply voltage changes, the amplifier will adjust to keep the swing and the bias current constant. Because the differential amplifier utilizes the self-biased architecture, there are two stable states, one of which is unbiased. As a result, an initial circuit is needed to bias the amplifier when power-up.

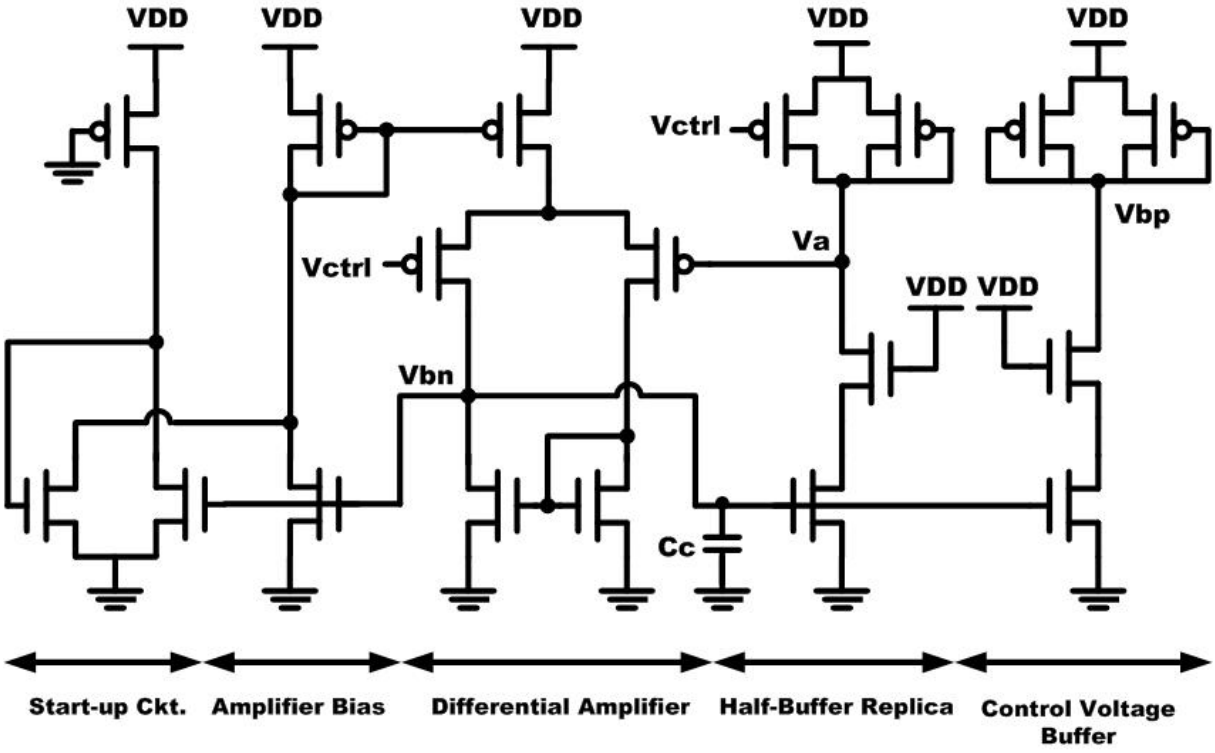


**Fig 3-11 Schematic of self-biased replica-feedback bias generator**

Because the differential amplifier and the half-buffer replica form a two-stage negative feedback loop, frequency response issue must be taken into consideration. Basically, there are two poles in the loop. One is at amplifier output, and the other is at the half-buffer replica output. Since the pole at the amplifier output is the dominant one, it can be moved toward origin to increase the phase margin of the loop by the capacitive load of the NMOS current source gates in the VCO buffer chain. Moreover, in order to track any supply and substrate noise that affect the VCO jitter performance, the bandwidth of the self-biased circuit is usually set equal to the operation frequency

of the VCO. The bias circuit also provides a buffered version of control voltage Vctrl using an extra control voltage buffer. This can isolate the control voltage Vctrl from capacitive coupling in the VCO buffer chain.

The PLL used in this thesis needs to generate four phases for the transmitter multiplexer and for the receiver samplers. Therefore, the VCO uses four delay buffer stages with the output frequency at 400MHz. The transfer curve simulation result of the VCO is shown in **Fig. 3-12**. The supply voltage is 3.3V. For Vctrl between 0.8V to 2.4V, the gain of the VCO is 457MHz.

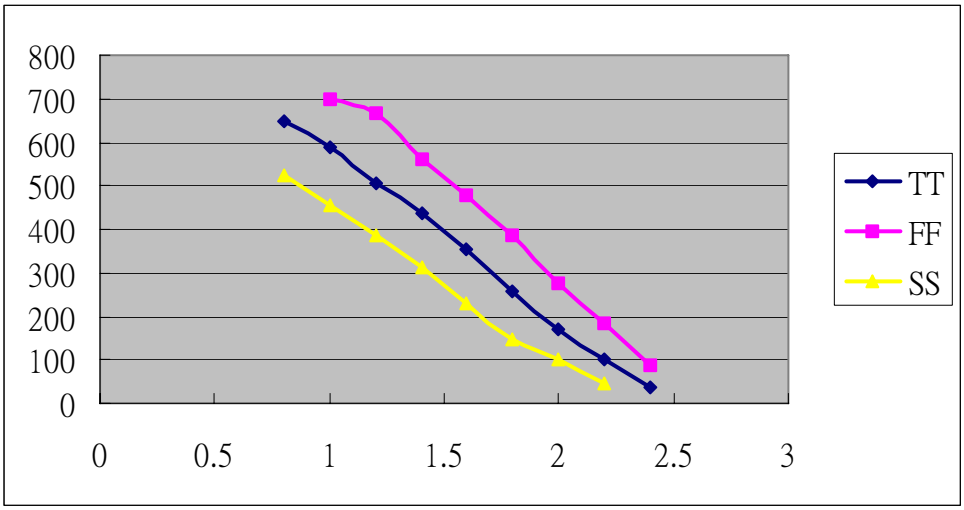


**Fig 3-12 Transfer Curve of the VCO**

The differential oscillator output is converted to the 50% duty cycle single-ended signal used as input to the phase-frequency detector with the differential-to-single-ended converter shown in **Fig. 3-13** and the feed forward type duty-cycle corrector shown in **Fig. 3-14**. The two differential amplifiers of the differential-to-single-ended converter use the same current source bias voltage, Vbn, generated by the self-biased replica-feedback bias generator for the VCO. According to Vbn, the circuit corrects the input common-mode voltage level and provides signal amplification.

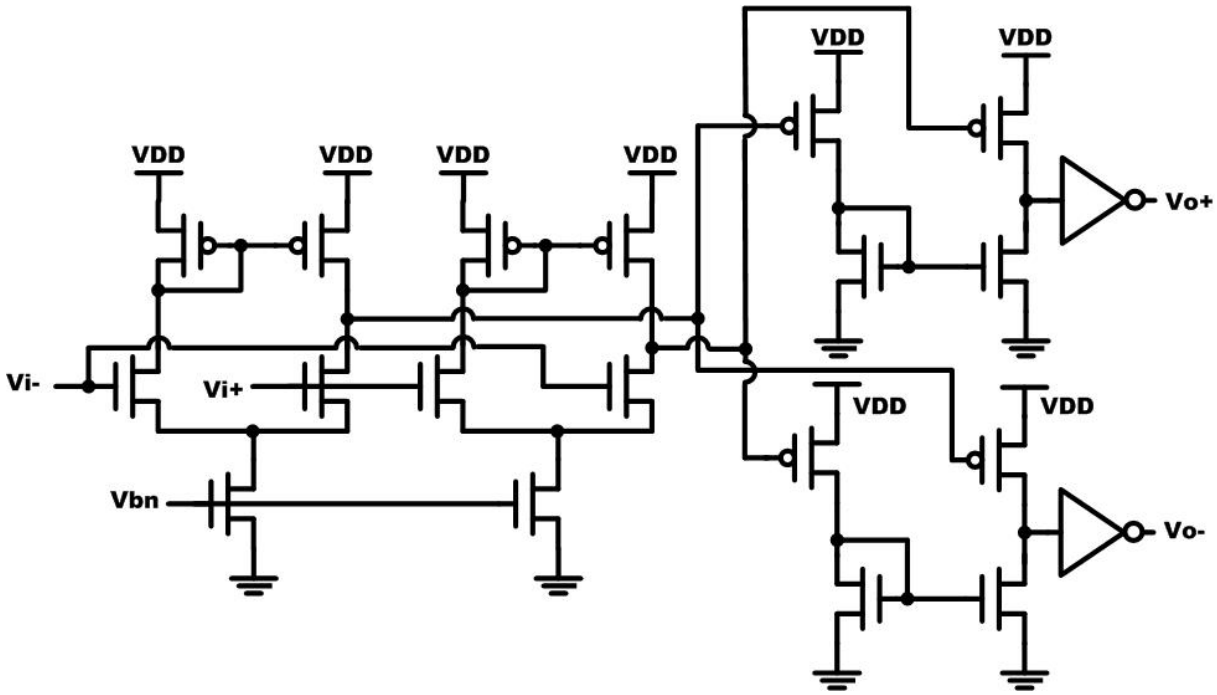


**Fig 3-13 Schematic of differential-to-single-ended converter**

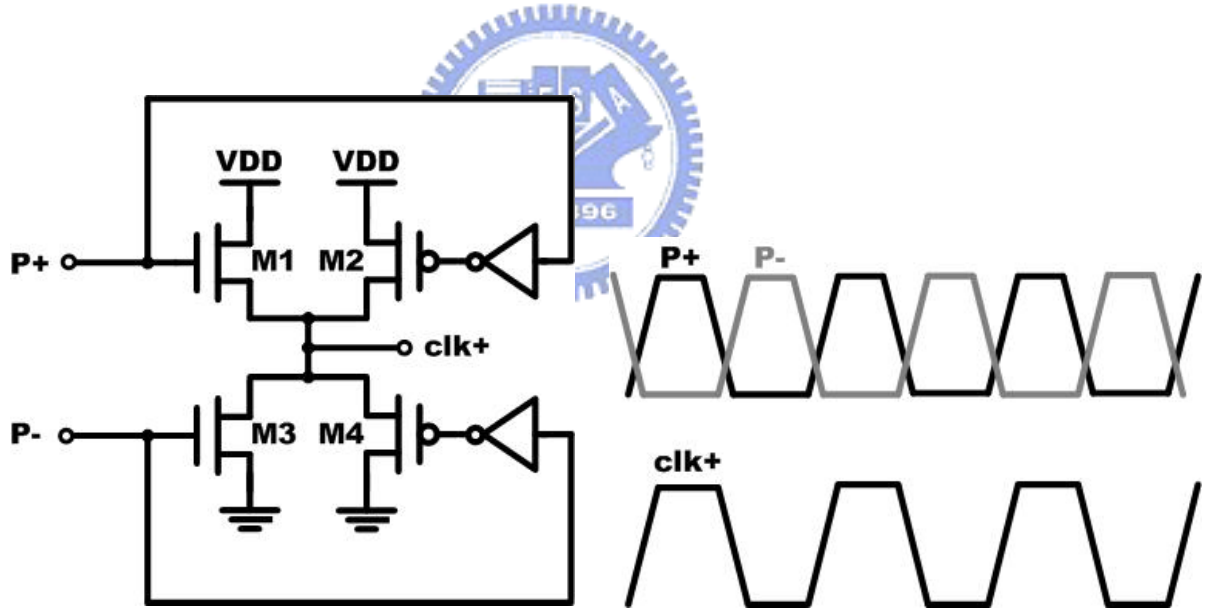


**Fig. 3-14 Schematic of feed forward type duty-cycle corrector and its timing diagram**

The duty-cycle corrector is connected behind the differential-to-single-ended converter to ensure that the duty-cycle of the VCO will be 50%. The signal P+ selected from the multiphase signals turn on M1 and M2, and charges the output node clk+ of the duty-cycle corrector almost instantaneously. Because the discharge path of

the node clk+ is already off due to the signal P-. The signal P-, which is also selected from the multiphase signals, is the one whose rising edge is shifted by 180° in phase from that of P+. Similarly, the signal P- rapidly discharges the node clk+ and delivers the desired 50% duty-cycle signal. Since this duty-cycle correction circuit consists of only two transmission gates and two inverters, the area is minimal and the power consumption is negligible. In order to drive next stages, digital buffers are added at the output to improve the driving ability.

### 3.3.5 Divider

Because the output frequency of the VCO is 400 MHz and the input reference frequency is 100MHz. Hence a divided-by-four circuit is used. The TSPC D Flip-Flop connected its inverted output to D input is used as a divided-by-two circuit, as shown in **Fig. 3-15**. In this circuit we need to check input clock driving capability to assure correct operation. Then, two divided-by-two circuits are cascaded to get a divided-by-four circuit. Unfortunately, asynchronous counter will accumulate jitter stage by stage. A synchronous counter is used at the last stage to re-sample the clock, and it will eliminate the jitter accumulated in asynchronous counter, as shown in **Fig. 3-16.**

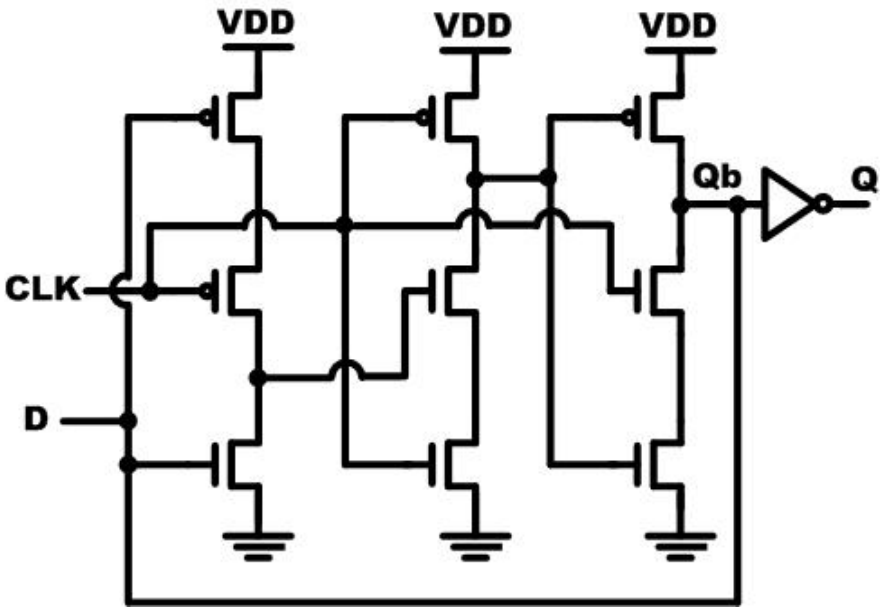


**Fig. 3-15 Schematic of TSPC Asynchronous Divided-by-two circuit**

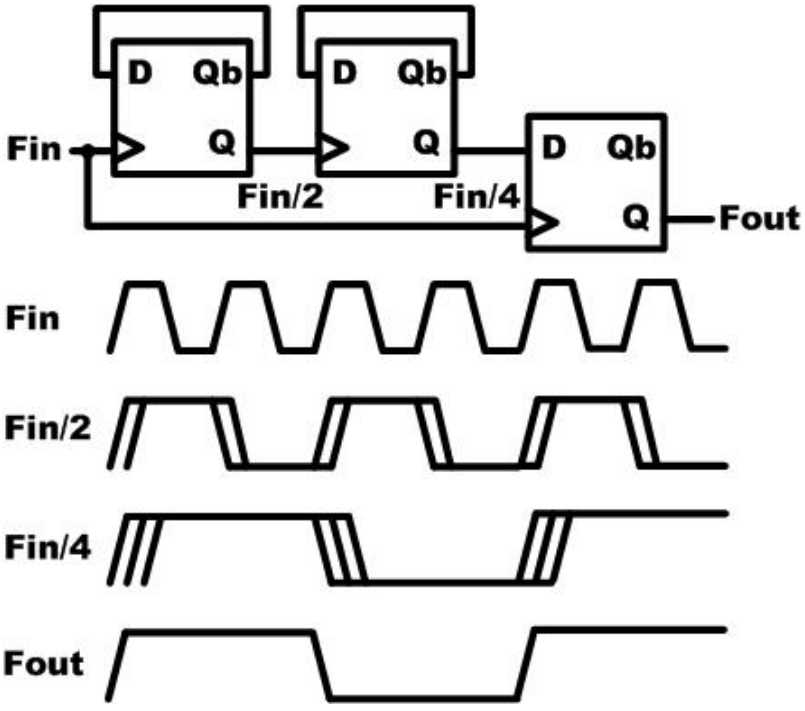


**Fig. 3-16 Divider composed of asynchronous and synchronous counters and its timing diagram**

# 3.4 PLL Parameter Design

Because the charge pump has switching characteristics, the PLL is generally a discrete-time domain operation. It is difficult to use continuous time-domain analysis. However, if under some condition, the s-domain model could also be used to get a thorough understanding of the negative feedback loop. **Fig. 3-17** shows the linear model of the PLL.

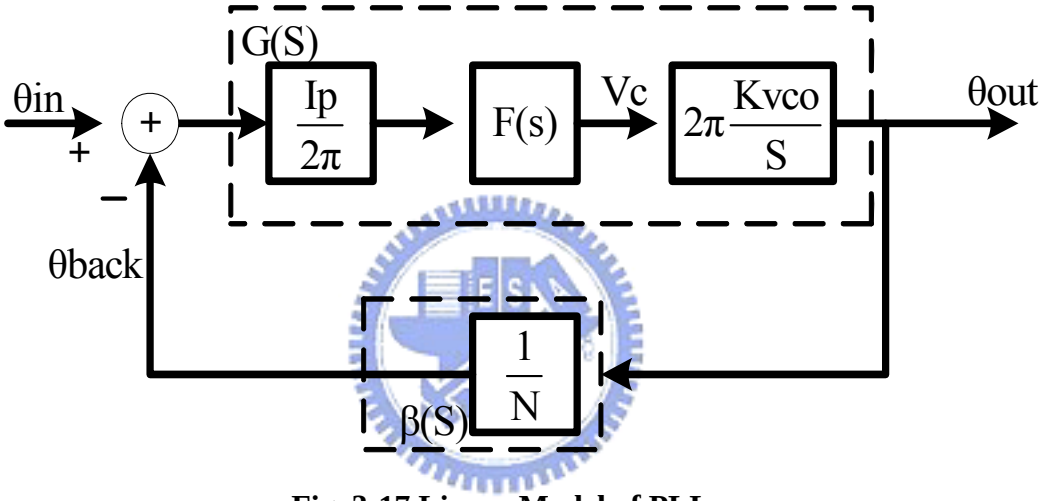


**Fig. 3-17 Linear Model of PLL**

Assume the PLL is in lock state. The PFD and CP have a current change of Ip/2π (A/rad), the LF has a transfer function F(s) (V/A), the VCO has a gain of Kvco (Hz/v), and the feedback factor is 1/N. The conversion gain of the VCO should be changed to 2πKvco/s (rad/sec-V), because phase is the integral of the frequency. Based on the above definitions and PLL linear model, the open loop gain of the PLL can be represented as

$$G(s)\times\beta(s)=\frac{\theta_{back}(s)}{\theta_{in}(s)}=\frac{I_P\times Kvco\times F(s)}{s\times N} \tag{3-7}$$

The closed loop transfer function of the PLL is given by

$$H(s)=\frac{\theta_{out}(s)}{\theta_{in}(s)}=\frac{G(s)}{1+G(s)\times\beta(s)}=\frac{N\times G(s)}{N+G(s)}=\frac{N\times K}{s+K} \tag{3-8}$$

Therefore, the 3-dB bandwidth is

$$\omega_{3dB}=K=\frac{I_P\times Kvco\times F(s)}{N} \tag{3-9}$$

From analysis of LF, we know that the shunt capacitance $C_2$ is typically much smaller than $C_1$. Therefore, we can neglect the capacitor $C_2$ and using classical two-pole system and second-order linear model of PLL to analyze the characteristic of transient response. With $F(s) = R_1 + (1/sC_1)$, the closed loop transfer function can be derived as

$$H(s)=\frac{I_P\times K_{vco}}{C_1}\cdot\frac{(1+SR_1C_1)}{S^2+\frac{I_PK_{vco}R_1}{N}S+\frac{I_PK_{vco}}{NC_1}} \tag{3-10}$$

Equation above can be compared to the classical two-pole system transfer function

$$H(s)=\frac{2\zeta\times\omega_n+{\omega_n}^2}{S^2+2\zeta\times\omega_n\times S+{\omega_n}^2} \tag{3-11}$$

Therefore, the natural frequency $\omega_n$, and damping factor $\zeta$ can be derived as

$$\omega_n=\sqrt{\frac{I_pK_{vco}}{NC_1}} \tag{3-12}$$

$$\zeta=\frac{\omega_n}{2\omega_z} \tag{3-13}$$

In the case of the PLL design, the frequency noise of the VCO could be the dominant noise source to influence the phase noise performance. As will be seen in

later section, the noise of the VCO has the high pass characteristics. Therefore, a large loop bandwidth for the PLL feedback system is better because it can enhance the tracking ability. The choice of the damping factor ζ is a trade off between acquisition time and step response stability. If larger ζ is chosen, the system could have longer acquisition time. On the other hand, if smaller ζ is chosen, the system may be ringing for step response or become unstable.

Then, we use the loop bandwidth and the phase margin to determine the component values of the loop filter. We can get

$$Loop\ BW = \frac{I_P \times Kvco}{N} \cdot \frac{R_1 C_1}{C_1 + C_2} \tag{3-14}$$

The phase term will be determined based on the pole and zero of the loop filter such that the phase margin is calculated as

$$PM = \tan^{-1}\frac{BW}{\omega_z} - \tan^{-1}\frac{BW}{\omega_p} \tag{3-15}$$

By setting the derivative of the phase margin equal to zero, the phase margin is maximum when the loop bandwidth is set to the average of pole and zero.

$$BW = \sqrt{\omega_z \omega_p} \tag{3-16}$$

We can define a new parameter, γ, as

$$\gamma = \frac{BW}{\omega_z} = \frac{\omega_p}{BW} \tag{3-17}$$

The capacitance ration of $C_1$ and $C_2$ can be represented by

$$\frac{C_1}{C_2} = \gamma^2 - 1 \tag{3-18}$$

The loop bandwidth (BW) now can be written as

$$BW = \frac{I_p \times K_{VCO}}{N} \cdot R_1 \left(1 - \frac{1}{\gamma^2}\right) \tag{3-19}$$

The design flow of a third-order PLL can be derived from equations above. The design flow can be summarized as follows:

1. Determine $K_{vco}$ by measuring VCO test keys or simulating a VCO using in the design or referring to the data sheets of the employed commercial VCO.
2. Depending on the desired noise and transient performance, determine the loop bandwidth BW. Usually, the BW is less than 1/10 of the reference clock.
3. If the filter is off-chip, set $I_p$ to be around 100μA to 1mA. If an on-chip filter is employed, decrease the value of $I_p$ so that the reasonable trade off between chip area and charge pump current could be reached.
4. Determine the nominal value of N according to the system to be applied to.
5. Selecting the required PM specification.
6. With BW, $I_p$, PM, N, and $K_{vco}$ determined, $R_1$ can be calculated.
7. Calculate the value of $C_1$ with $C_1=1/R_1\omega_z$.
8. Calculate the value of C2.

The parameters used in the PLL are listed in **Table. 3-1**. **Fig.3-18** shows the curve for the open loop PLL frequency response. This curve gives the phade margin of approximately 70°. **Fig. 3-19** shows the eight even-spaced phases of frequency 400MHz. Fig. 3-20 shows the simulation of the eight output clock signals of the PLL.

| Technology | TSMC 0.35μm 2P4M CMOS |
|---|---|
| Function | PLL |
| Supply voltage | 3.3v |
| Input Frequency | 100 MHz |
| Output Frequency | 400 MHz |
| Charge Pump Current(Icp) | 100 μA |
| Loop Filter -C1 | 59.86 pF |
| -R1 | 3 kO |
| -C2 | 1.92 pF |
| VCOgain(Kvco) | 430 MHz/V |
| Divider (N) | 4 |
| Loop Bandwidth | 5 MHz |
| Phase Margin | 70 degrees |
| Power | 23mW@400MHz |

**Table 3-1 Parameters of the PLL**

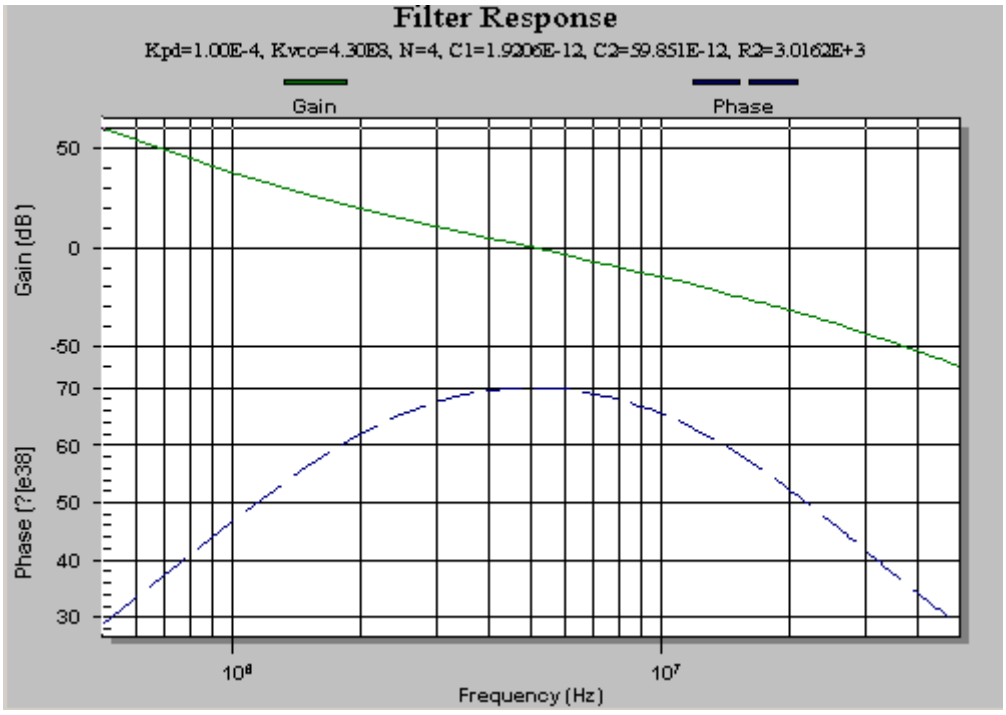


**Fig. 3-18 Open Loop gain simulation of the PLL**

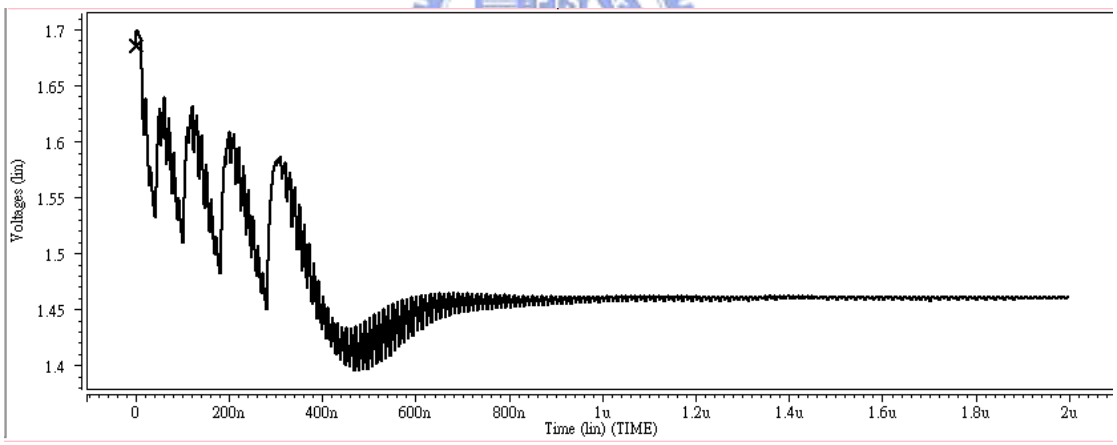


**Fig. 3-19 Simulation of the four output clock signals of the PLL**

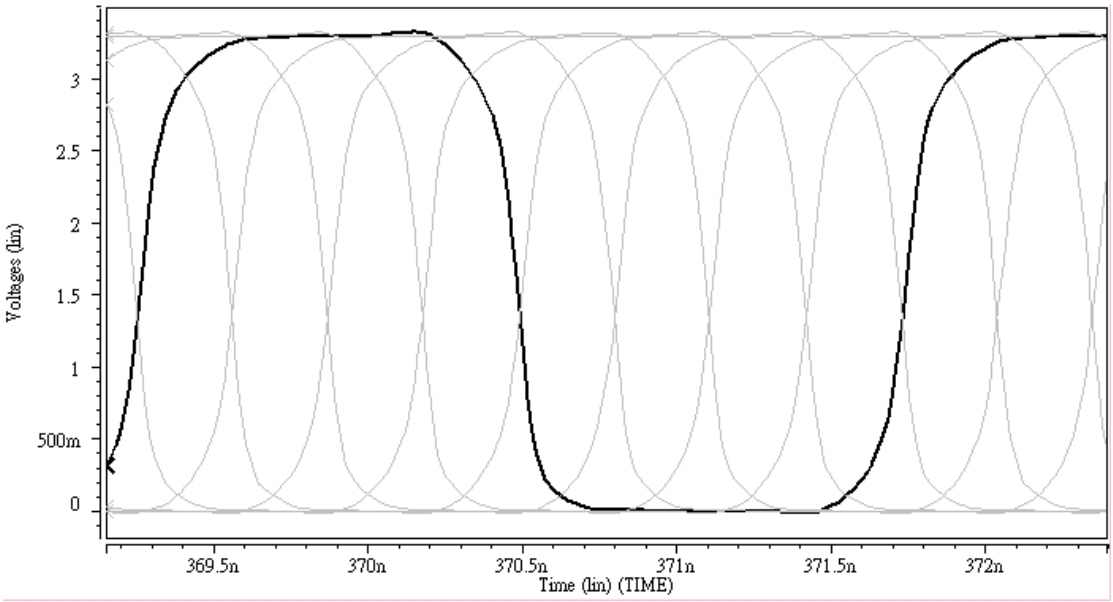


**Fig. 3-20 Simulation of the eight output clock signals of the PLL**

# 3.5 PLL Noise Analysis and Stability

The timing jitter could affect the maximum timing margin of the transmitter and the performance of the high speed serial link. The output jitter of the PLL is contributed by many different noise sources as shown in **Fig. 3-21**, where $\theta_{in}(s)$ is the reference noise, $i_n(s)$ is the PFD and CP noise, $V_n(s)$ is the LF noise and $\theta_n(s)$ is the VCO noise.

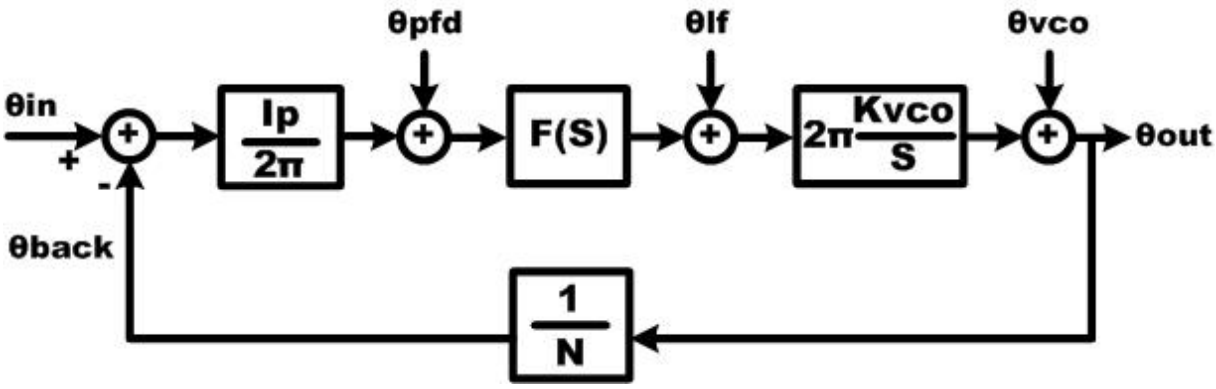


**Fig. 3-21 Linear model of PLL with different noise sources**

These noises introduce the phase fluctuations or timing jitter in time domain. Using closed loop analysis, the transfer functions with different noise sources can be derived as

$$H(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{N \times K}{s + K}$$

$$H_{pfd}(s) = \frac{\theta_{out}(s)}{\theta_{pfd}(s)} = 2\pi \cdot \frac{N}{I_P} \cdot \frac{K}{s + K}$$

$$H_{lf}(s) = \frac{\theta_{out}(s)}{\theta_{lf}(s)} = 2\pi \cdot \frac{K_{vco}}{s + K}$$

$$H_{vco}(s) = \frac{\theta_{out}(s)}{\theta_{vco}(s)} = \frac{s}{s+K} = 1 - \frac{H(s)}{N}$$

where

$$K = \frac{I_p \times K_{vco} \times F(s)}{N} = \frac{I_p K_{vco}}{N} \times \frac{1 + sR_1C_1}{sC_1}$$ (When C2 is neglected)

The noise transfer functions have different characteristics. The $H_{in}(s)$ and $H_{pdf\_cp}(s)$ are low pass functions, the $H_{LF}(s)$ is a band pass function and the $H_{vco}(s)$ is a high pass function. Based on the analysis, the loop bandwidth of the PLL should be maximized to meet the high pass function of the VCO to filter the timing jitter caused by the VCO. The maximum nature frequency $\omega_n$ of the PLL is restricted to the input reference clock frequency $\omega_{in}$. Using the analysis from the PLL, the criteria of the stability limit can be derived as

$$\omega_n^2 < \frac{\omega_{in}^2}{\pi(R_1C_1\omega_{in} + \pi)}$$

As a rule of thumb, stability can be assumed by keeping $\omega_n < 1/10\ \omega_{in}$. Choosing larger loop bandwidth indicates that more phase noise from the input clock will transfer to the output with larger loop bandwidth. However, it does not cause a problem when the input is a clean clock source.

# Chapter 4
# Transmitter

## 4.1 Architectureof Transmitter

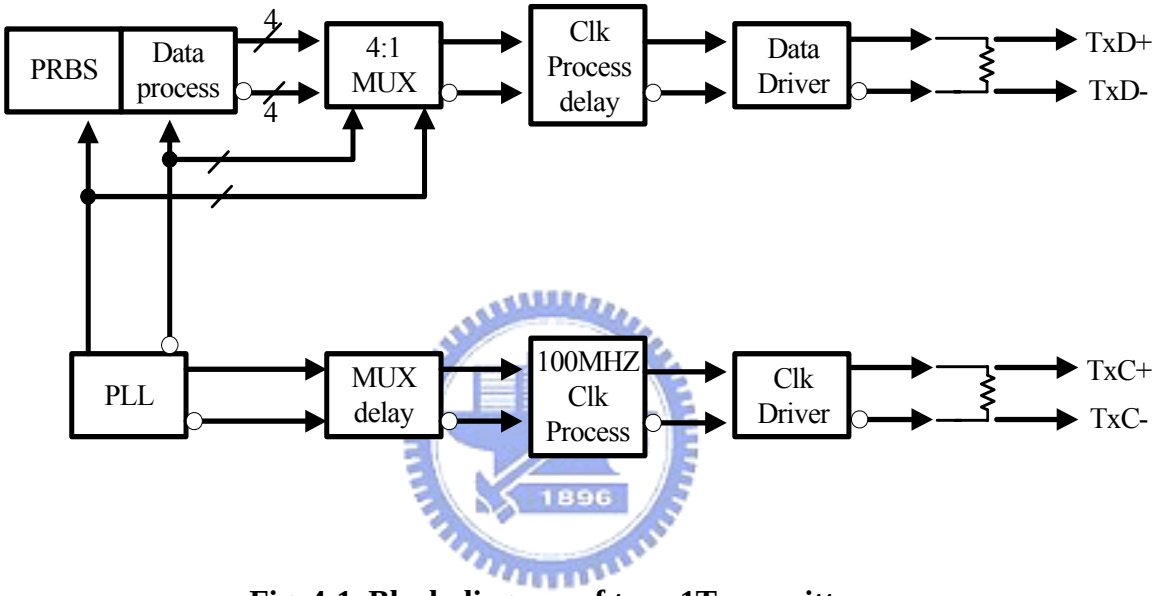


**Fig. 4-1. Block diagram of type 1Transmitter**

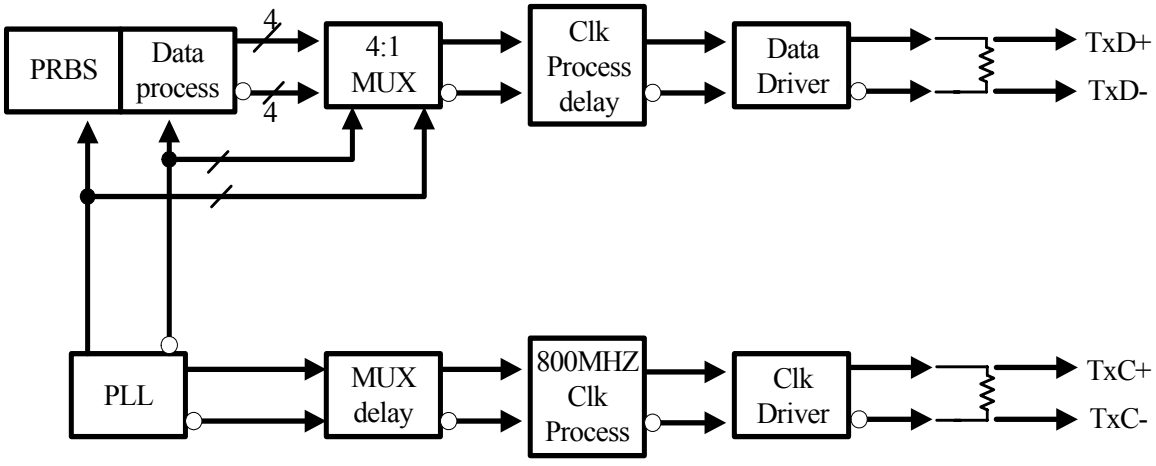


**Fig. 4-2. Block diagram of type 2Transmitter**

The data input is from PRBS (Pseudo Random bit sequence). The data process circuit pre-skew the data before feeding them into the multiplexer. The pre-skew of parallel data are shown in **Fig. 4-3**. **Fig. 4-1** and **Fig. 4-2** show the block diagrams of the transmitter architecture with type 1 and type2. The differences between type 1 and type 2 are clock process circuit and clock process delay circuit. Type 1 transmitter transfer 100MHz clock as **Fig. 4-4** for receiver. Type 2 transmitter transfer 800MHz clock as **Fig. 4-5** for receiver.

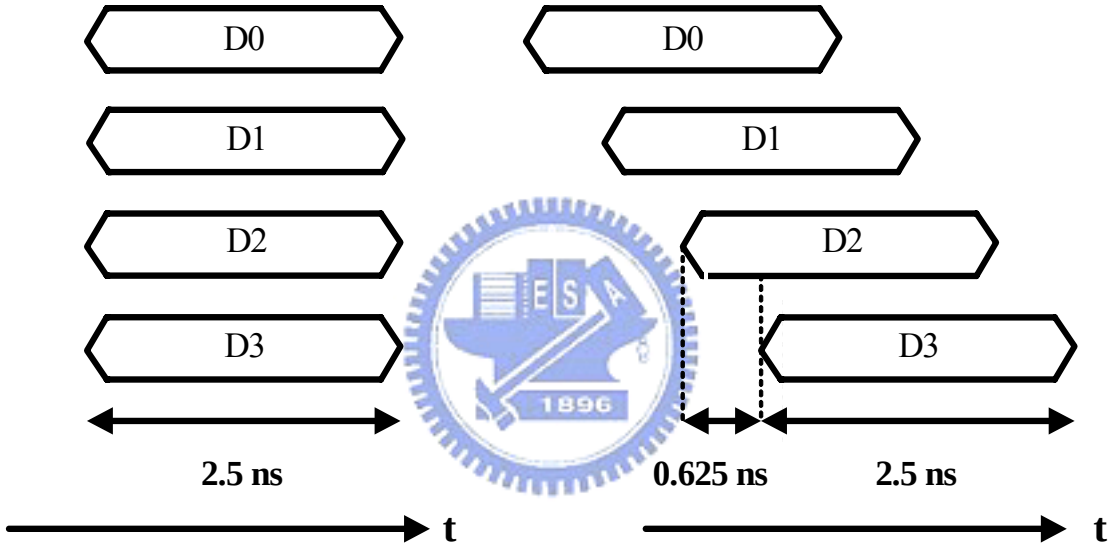


**Fig. 4-3 pre-skew of parallel data**

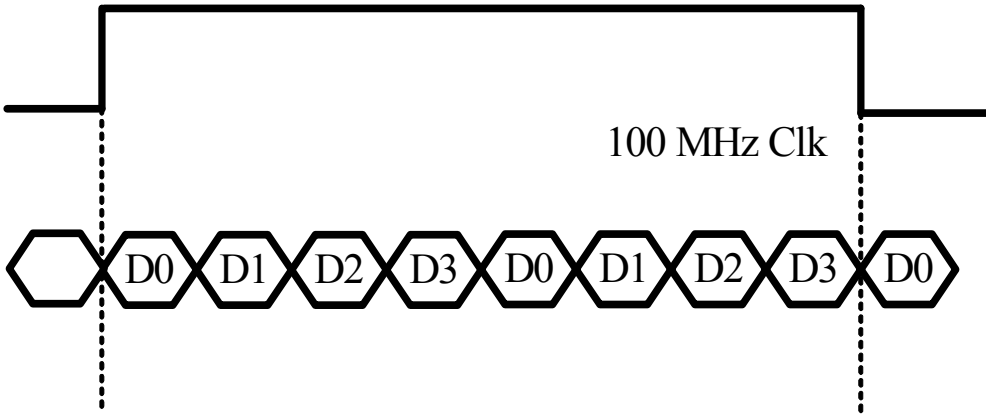


**Fig 4-4 Type 1 clock (100 MHz)**

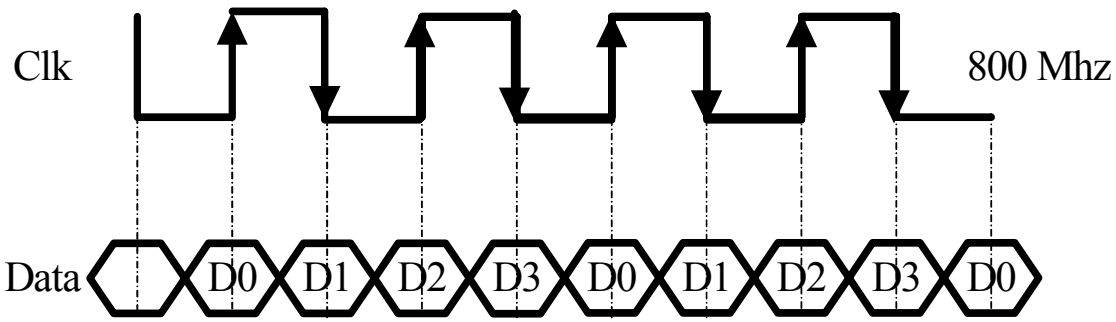


**Fig 4-5 Type 2 clock (800 MHz)**

The transmitter is built up by a PRBS circuit, a PLL, a 4 to 1 multiplexer, clock process circuit, and data and clock circuit. The transmitter consists of a PLL proposed in the chapter 3 to produce the clock signals at 400 MHz with eight even-spaced phases. By using 4:1 input-multiplexer, we can serializes low-speed four channels parallel data on four even-spaced phases of 400MHz which gives a bit rate 1.6Gbps, and we can reduce the frequency requirement of the timing circuits and the digital logic. Only four even-spaced phase is utilized for 4:1 MUX. The other is utilized for transferring 800MHz clock and using data pre-skew.

For testing, the Pseudo Random Bit Sequence (PRBS) is utilized to generate data pattern. Through the data and clock driver, the data stream is transmitted out with a nominal swing of 200mV. In the following section, we will describe the detail circuits of the function blocks in the transmitter architecture.

# 4.2 Pseudo Random Bit Sequence (PRBS)

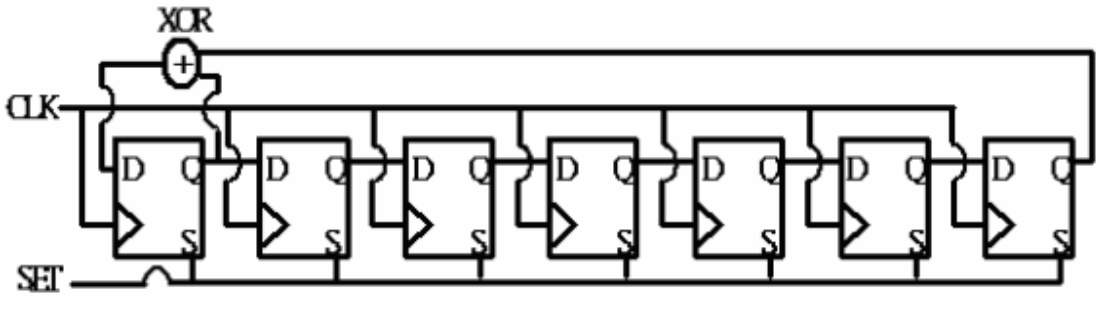


**Fig. 4-6 block diagram of Pseudo Random Bit Sequence (PRBS)**

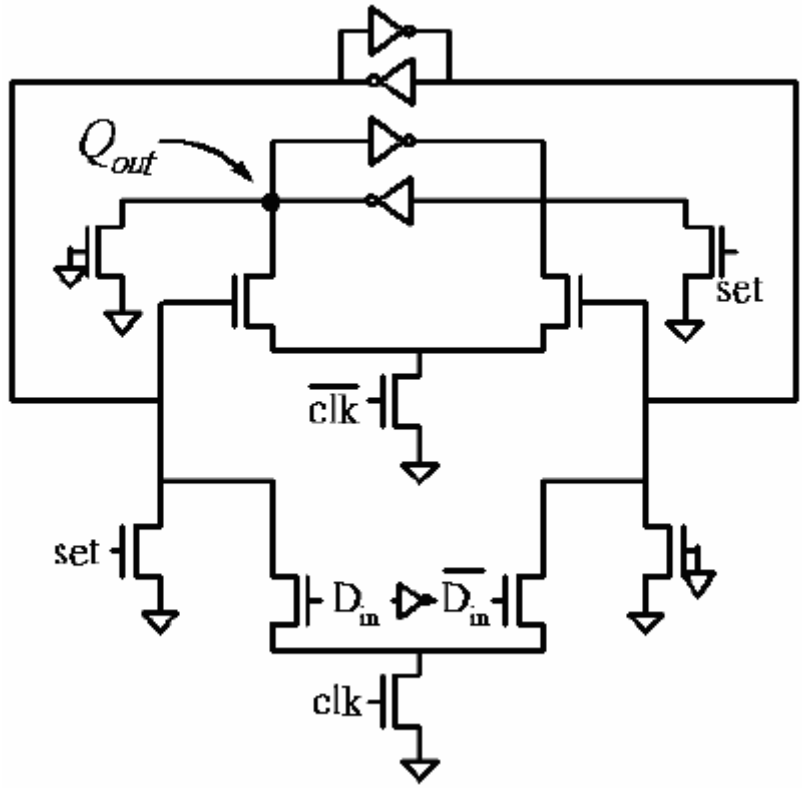


**Fig. 4-7 PRBS delay cell circuit**

As shown in **Fig.4-6**, The Pseudo random bit sequence (PRBS) is widely used for testing communication systems. **Fig. 4-7** shows the circuit implementation of the D-flip flop delay cell used in the PRBS circuit. With a series delay cell, each delay cell can offer a signal for next delay cell. The output of the XOR gate can generate the new data. The pattern repeats every $2^7$-1=127 clock cycles. We also note that if the

initial condition is zero, the delay cells remain in a degenerate state. Therefore, the SET signal must be used to solve this problem. And the XOR logic is the speed-critical part in the circuit. Then, we can use the outputs as 4-parallel data inputs of transmitter.

# 4.3 Four-to-One Multiplexer

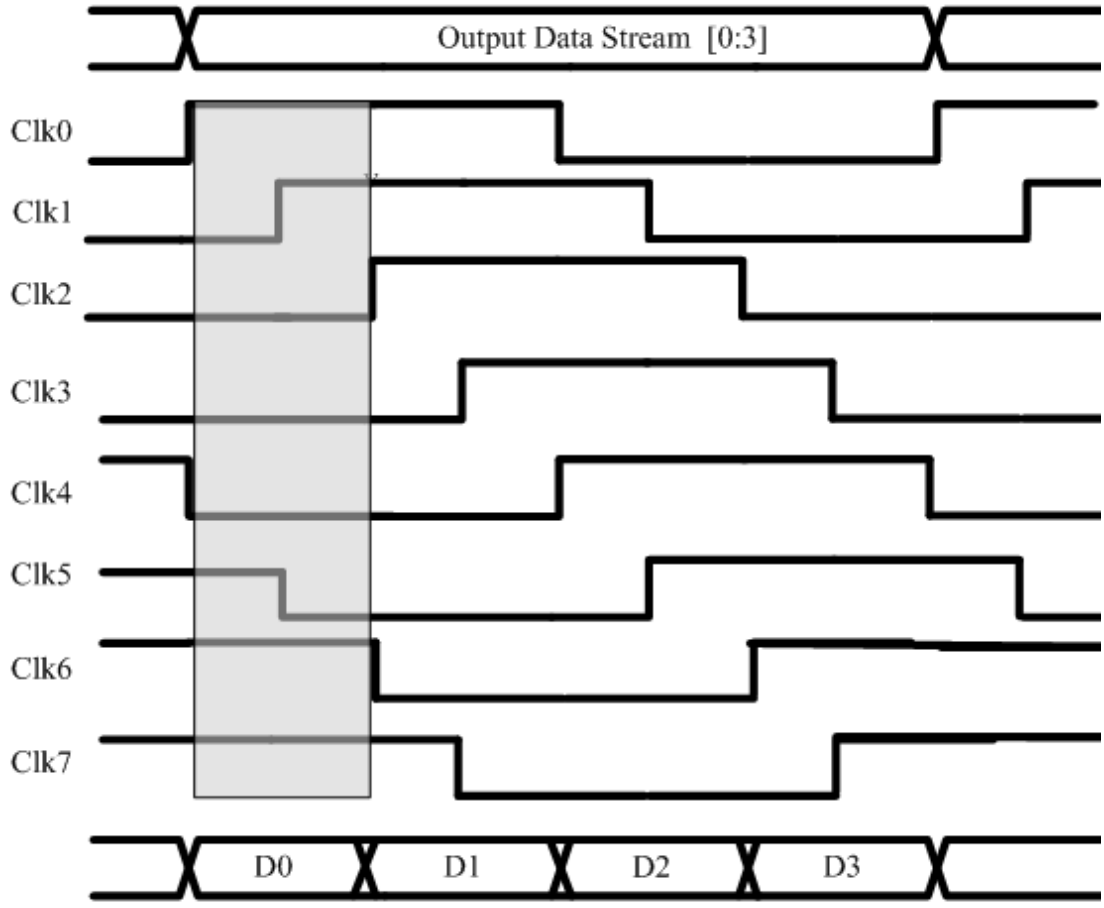


**Fig. 4-8 Timing diagram of 4:1 multiplexer**

The multiplexer is used to serialize the parallel data channels D0~D3.When the transmitter transfers the data stream with 1.6Gbps, the PLL must produce four-phases with 400MHz. It generates the required phases of clk0, clk2, clk4, and clk6. The other phases of clock are utilized to generate 800M Hz clock for TYPE 2 transmitter. The relationship between input data, D0~D3, and clock (clk0, clk2, clk4, andclk6) is shown in **Fig.4-8**. For example, at the timing interval between the rising edge of clk0 and the falling edge of clk6, the input signal D0 starts driving the multiplexer output.

In order to achieve this algorithm, the multiplexer, as shown in **Fig.4-9**, is used to serialize the parallel eight data channel input D0~D3. High multiplexer fan-in may become the bottleneck and the achievable speed gradually decreases. This speed limitation is not an inherent property of the process technology but of the circuit topology. Then 2-1 MUX is utilized, such as **Fig. 4-10** and **Fig. 4-11.** The Mux delay buffer is introduced in **section 4.3.2**.

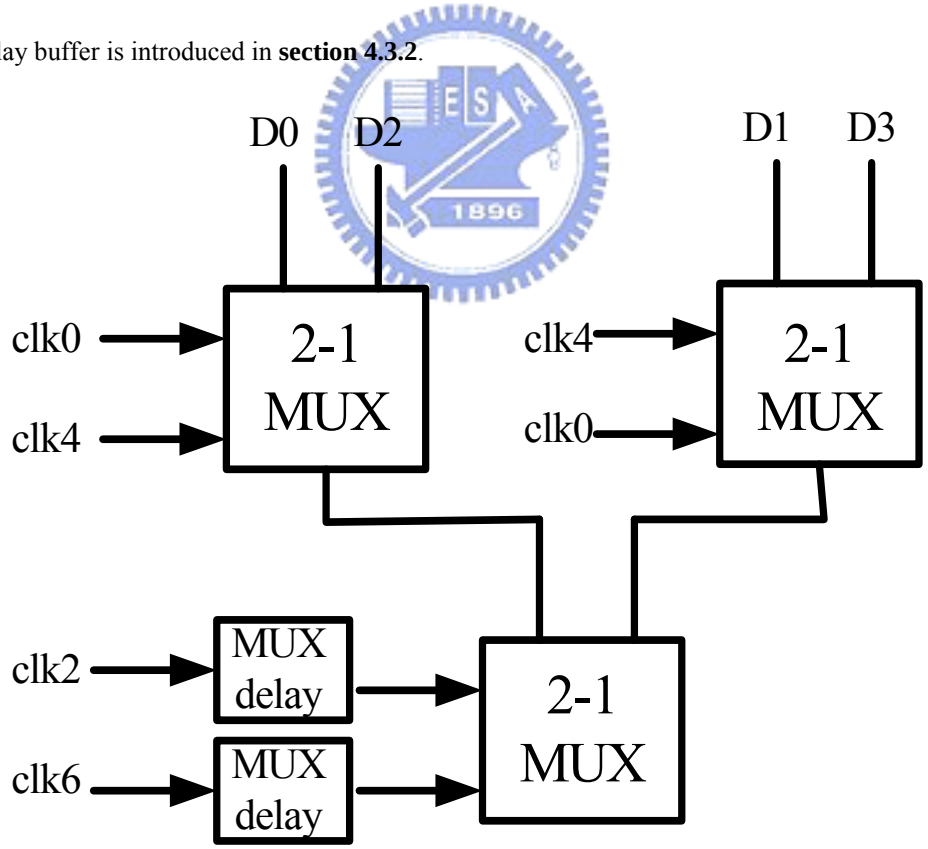


**Fig.4-9 Block Diagram of 4-1 Multiplexer**

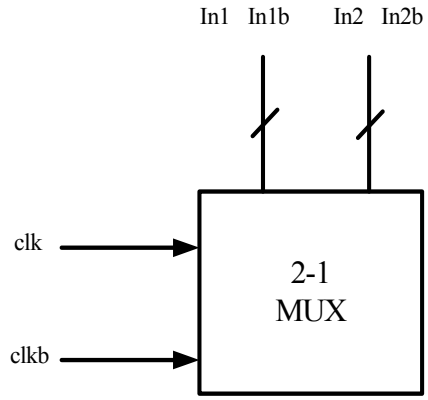


**Fig. 4-10 Block of 2-1 MUX**

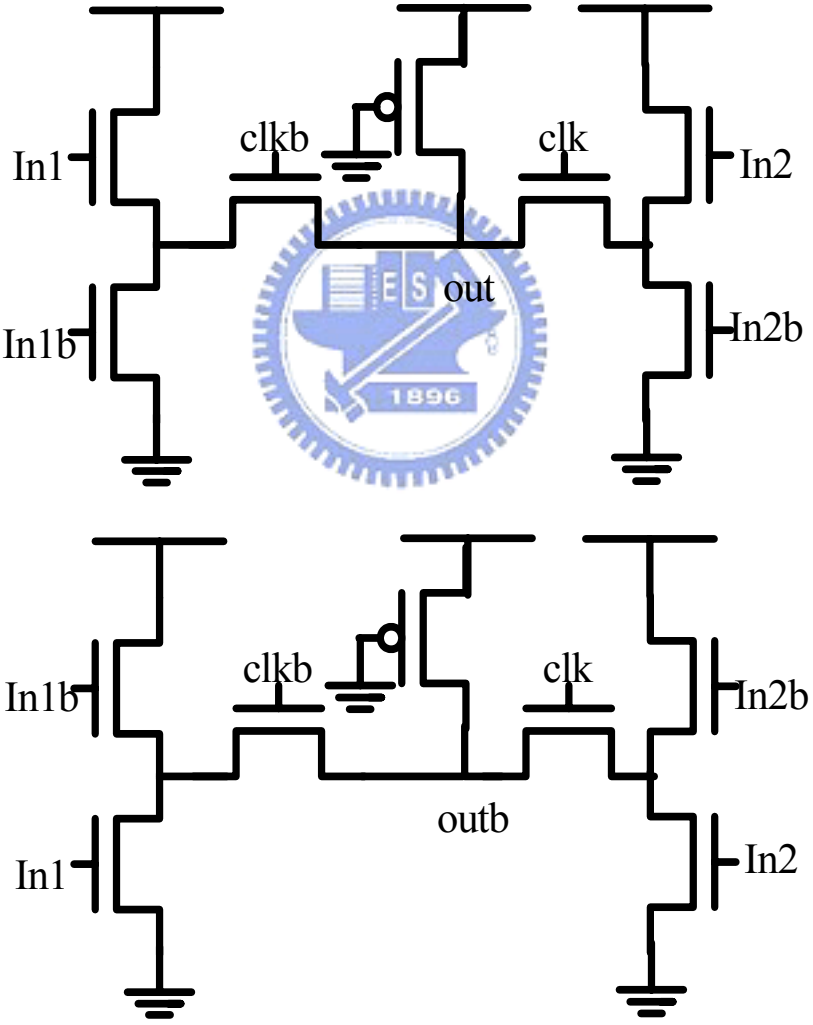


**Fig. 4-11 Schematic of 2-1 MUX**

### 4.3.1 Data Pre- skew to 4:1 Multiplexer

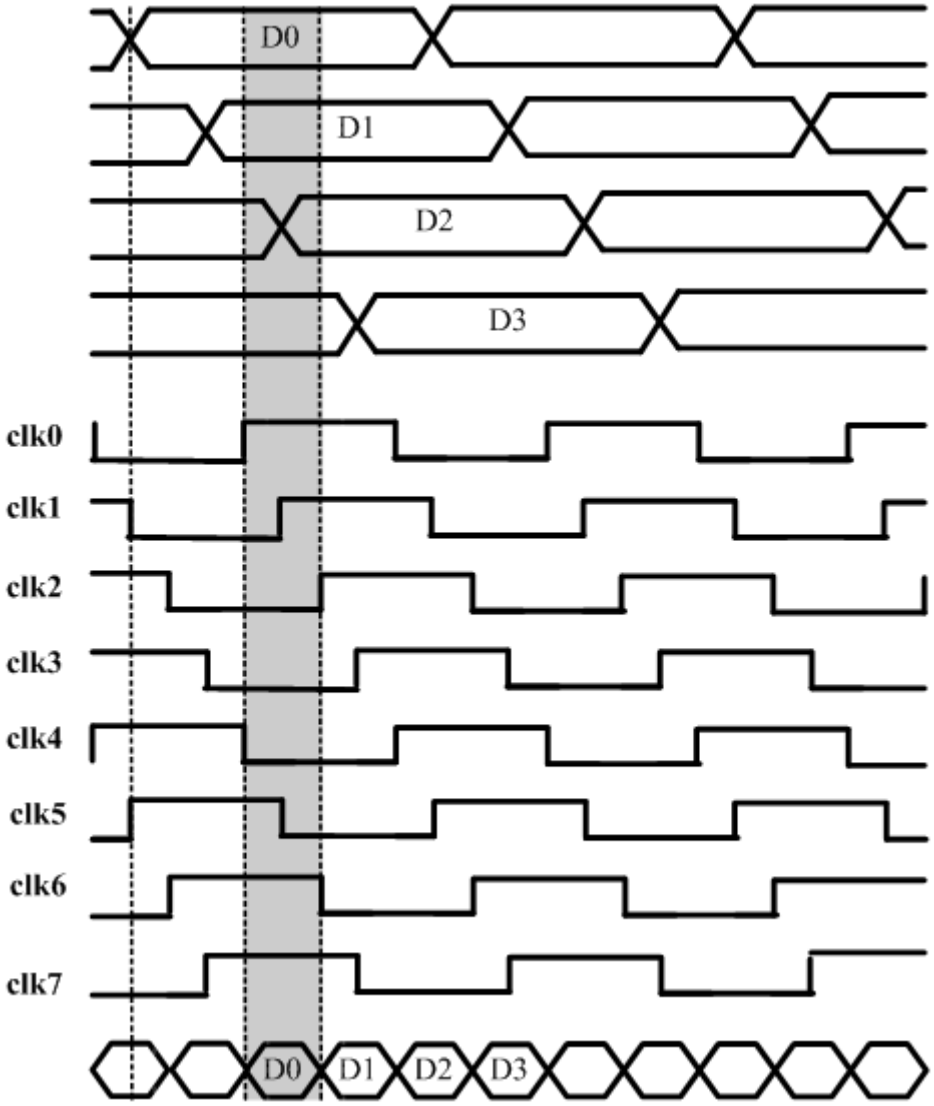


**Fig. 4-12 Timing diagram of Pre-skew**

In order to ensure that each multiplexer of first level can select input data at the stable and correct state, the pre-skew parallel data channel D0~D3 is utilized for the multiplexer. If the transient edges of clock and input data rise approximately at the same time, the selected data is confused and costs some time to be stable. Thus, the output data jitter of the transmitter. **Fig. 4-12** shows the timing diagram of pre-skew. In order to achieve the target, some input data must be shifted before given in 2-level multiplexer.

### 4.3.2 Mux Delay

As showed in **Fig. 4-1** and **Fig. 4-2**, clocks are transferred with data pattern. The delay of data pattern and the clock must be the same and hence the clock is reliable. With the same circuit architecture, the delay of these two circuits are the same. Then the path of clock is designed as long as the path of data pattern. The multiplexer is used to serialize the parallel data channels D0~D3. Data is passed through 2-levels type MUX, and hence two stage of MUX delay buffer is added in clock path, as **Fig. 4-13**.

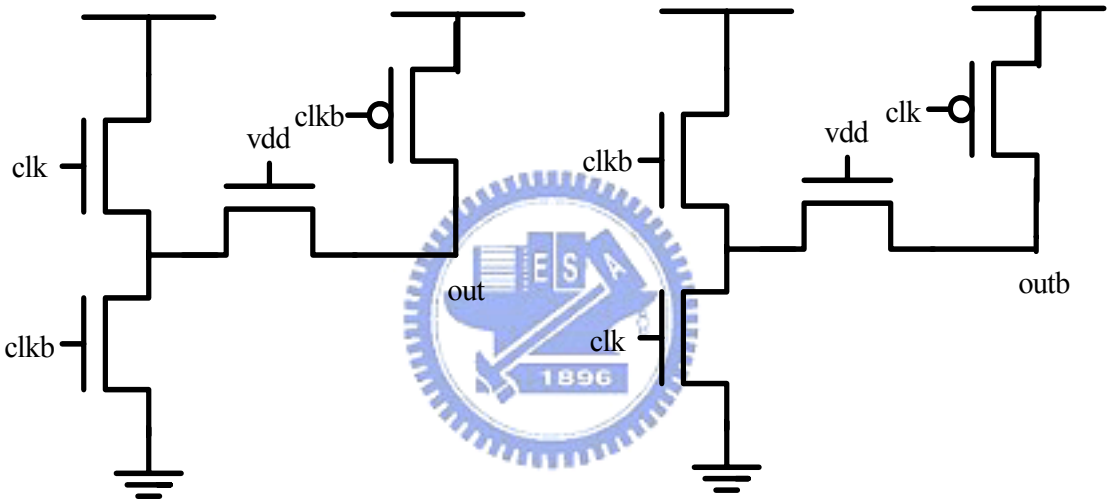


**Fig. 4-13 schematic of MUX delay**

## 4.4 Clock Process Circuit

Because code modulation is usually used for data pattern, we usually don't need such high speed to match spectrum for channel. In TYPE 1 transmitter, 100 MHz clock is transferred, as **Fig. 4-4**. For a critical case, a 1.6Gbps data pattern transfers a one followed by a zero (0 1 0 1 0 1 . . . . ), and it is equal to 800MHZ clock actually. Then 800MHz is the fastest clock to transfer 1.6Gbps data pattern. In TYPE 2 transmitter, 800 MHz clock is transferred, as **Fig. 4-5**.

**TYPE 1 Transmitter:**

In TYPE 1 transmitter, 100MHz clock is utilized to give information about phase between clock and data, as **Fig. 4-4**. Clk0 in **Fig.4-8** is used to generate 100Mhz clock for receiver. Because clk0 is 400MHz and the clock for receiver is 100MHz. Hence a divided-by-four circuit is used. The TSPC D Flip-Flop connected its inverted output to D input is used as a divided-by-two circuit, as shown in **Fig. 3-15**. Two divided-by-two circuits are cascaded to get a divided-by-four circuit. A synchronous counter is used at the last stage to re-sample the clock, and it will eliminate the jitter accumulated in asynchronous counter, as shown in **Fig. 3-16.**

Because clock passed through a divided-by-four circuit suffers delay. In order to ensure the phase between data and the clock is correct. A delay is added to data path. **Fig.4-1** shows the data path which includes clock process delay. **Fig. 4-14** shows the TSPC D Flip-Flop and its delay cell.

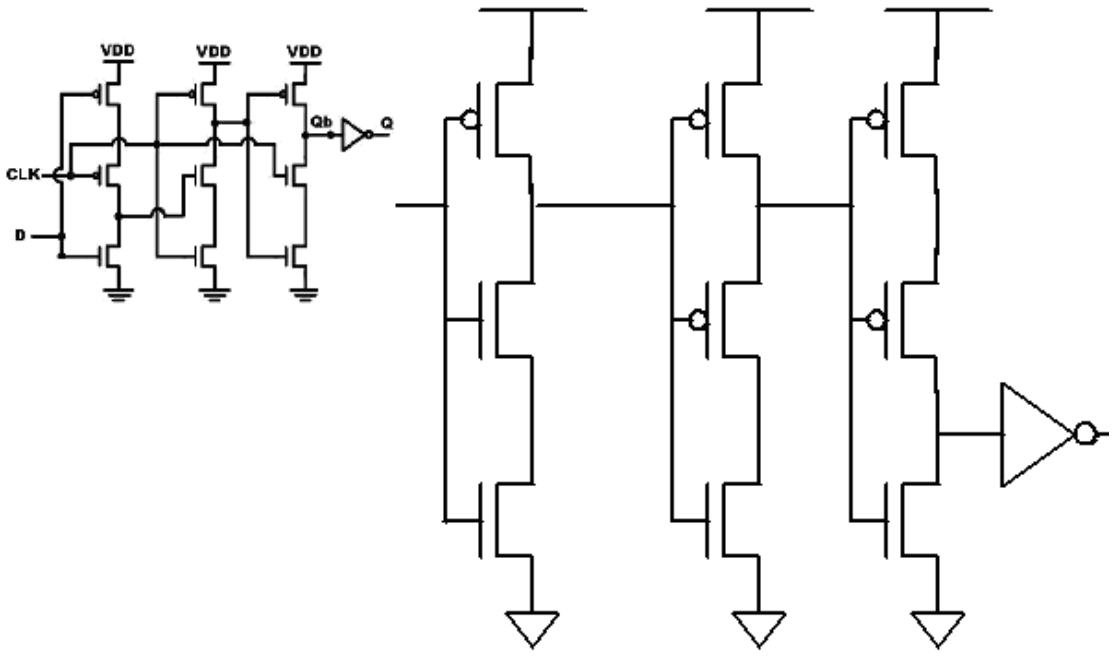


**Fig. 4-14 TSPC delay cell**

**TYPE 2 Transmitter:**

In TYPE 2 transmitter, the edge of 800MHz clock edge will be located at the midpoint of each bit by clock process. It needs clk1 and clk3 in **Fig. 4-8** to generate 800MHz clock for receiver by using XOR, as **Fig. 4-15**.

The receiver overcomes device limitations by using both rising and falling clock edges, as shown in **Fig. 4-5**. The clock is able to operate at half the speed of the data rate.

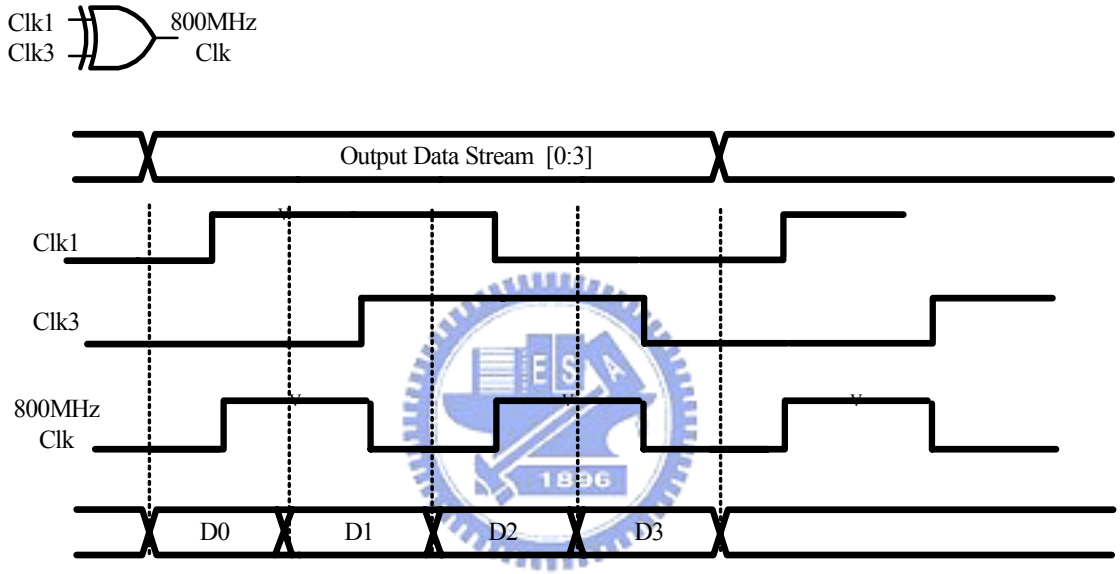


**Fig. 4-15 Timing diagram of clk and data**

Because clock which pass through a XOR gate suffers delay. In order to ensure the phase between data and the clock is correct. A delay is added to data path. **Fig.4-2** shows the data path which includes clock process delay. A XOR gate is added to data path for being clock process delay.

# 4.5 Data driver

The basic receiver has high DC input impedance, the majority of driver current flows across the termination resistor generating about 200mV across the receiver inputs. The simplified RSDS outputs consist of a current source which drives the

differential pair line. When the driver switches, it changes the direction of current flow across the resistor, hence creating a valid “one” or “zero” logic state. A differential load resistor at the receiver end provides current-to-voltage conversion and optimum line matching at the same time. An additional termination resistor is usually placed at the source end to suppress reflected waves caused by crosstalk or by imperfect termination. The implemented transmitter data driver shown in **Fig.4-16** uses the typical configurations with four MOS switches in bridge configuration. In order to obtain the correct output offset voltage of the RSDS$^{TM}$ Spec, a feedback loop across a replica of the transmitter circuit is used, but in this case the effect of component mismatches between the transmitters and replica should be carefully taken into account.

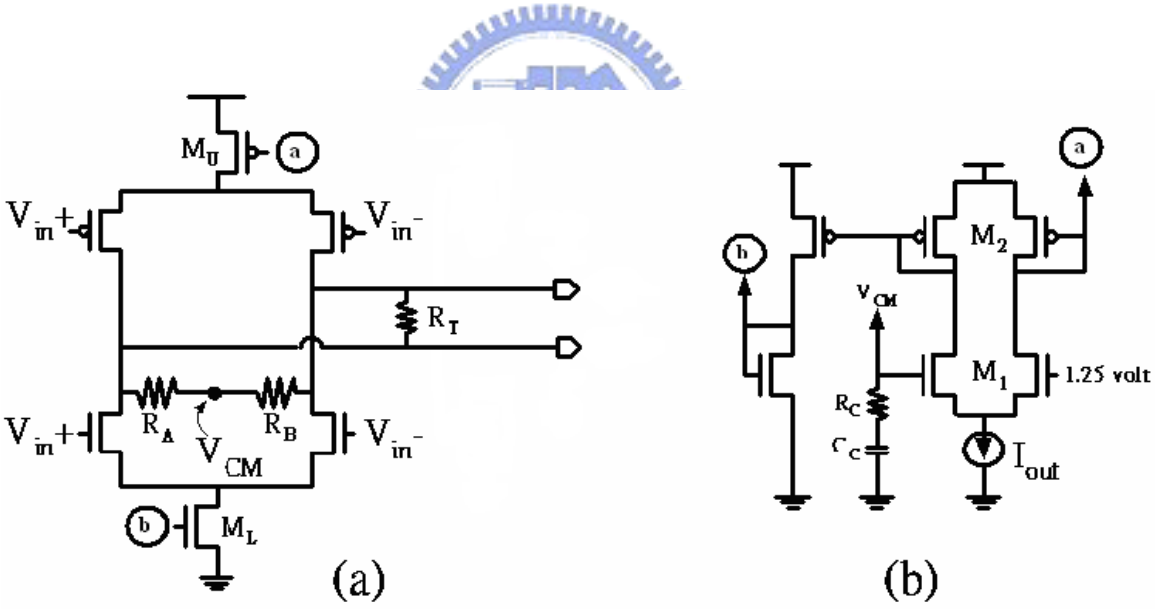


**Fig.4-16 (a) Schematic diagram of the RSDS transmitter data driver. (b) Common mode feedback circuit.**

**Fig.4-16(b)** shows that a simple low-power common-mode feedback control was implemented in the transmitter to achieve higher precision and lower circuit complexity. The common-mode output voltage is sensed by means of a high resistive

divider $R_A$ and $R_B$ (=50kΩ) and compared with a 1.25V reference by the differential amplifier. The fraction of the tail current $I_{out}$ flowing across $M_1$ and $M_2$ is mirrored to $M_U$ and $M_L$, respectively, thus forcing $V_{CM}$≈1.25V. Usually, the large gain of device size $M_U$ and $M_L$ is used in order to make negligible the power consumption of the common-feedback circuit. To develop the correct voltage swing on the 50Ω load resistance ($R_{T\_T}$//$R_{T\_R}$), the amount of current should be designed properly.

## 4.6 Transmitter Simulation Result

### 4.6.1 Simulation Environment

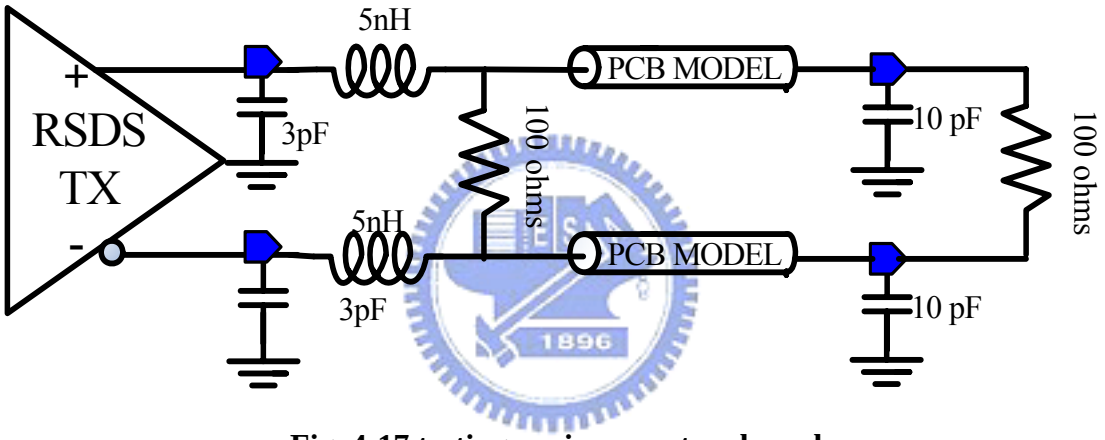


**Fig. 4-17 testing environment on board**

In real IC, the DIE will be packaged and we should take it into consideration. After transmitted from the transmitter data driver, the data output goes through the internal bonding pad, external bonding wire and the PCB circuit. The thin bonding wire can be inductive and the pad is inductive and capacitive. Finally, the output signal arrives at the receiver termination resistor $R_{T\_R}$. During simulation the package effects are added in vdd, gnd, and I/O node. Besides, the output loading of the data driver should be considered. The simulation environment is implemented as shown in **Fig. 4-17**. In the following sections, the simulation results are respectively demonstrated.

## 4.6.2 Simulation Result of PLL

**Fig. 4-18** shows the waveform of eight-phase clock signal with 400MHz clock of the PLL. **Fig. 4-19** shows the eye-diagram of the clock by the PLL. The jitter is about 33 ps.

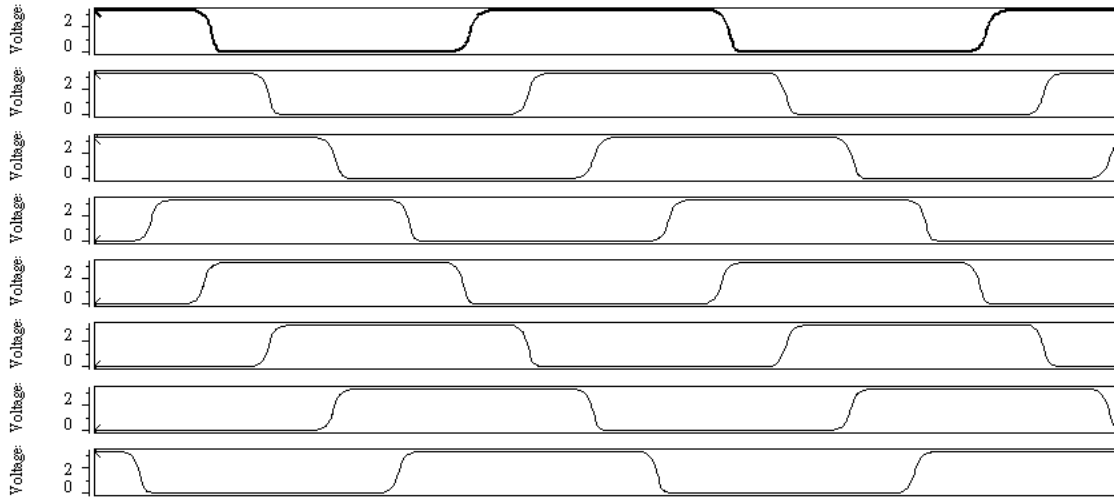


**Fig.4-18 eight-phase VCO clock of PLL**

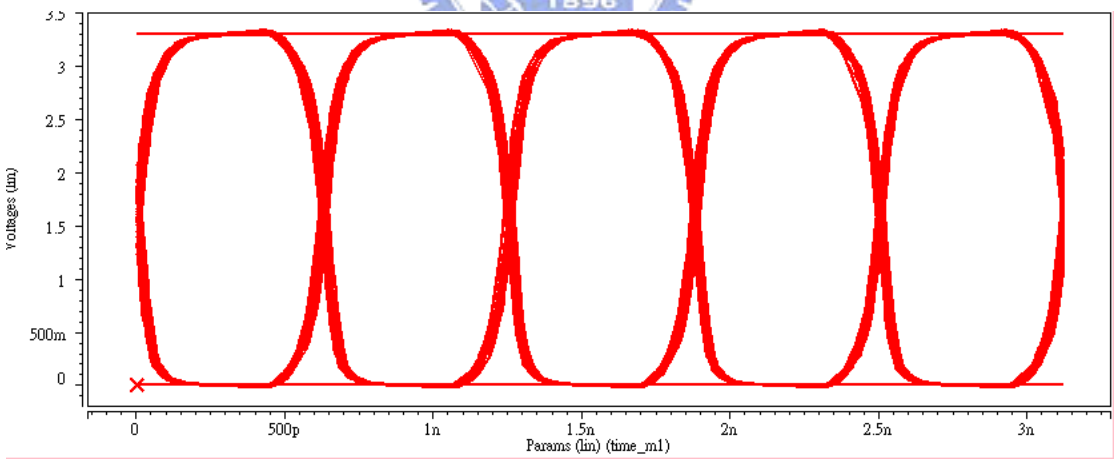


**Fig.4-19 eye diagram of the transmitter output waveform**

## 4.6.3 Simulation Result of Transmitter

- **Without Data Pre-skew**

**Fig. 4-20** shows the simulation result with 2-levels multiplexer. The width of the eye-diagram is about 538 ps with 87 ps jiter.

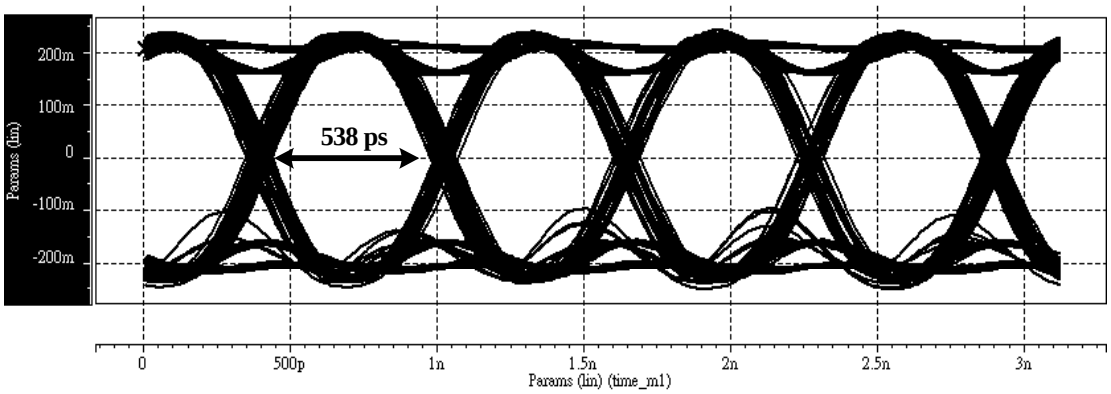


**Fig.4-20 eye diagram of output (Without data preskew)**

- **With Data Pre-skew**

With pre-skew circuit, we can avoid the condition that the clock edge falls on the data transient state. This makes eye-diagram more open. **Fig.4-20** shows the simulation result. The amplitude of data eye-diagram is increased to about 200 mV and the width of the eye-diagram is about 547 ps with 78 ps jitter. **Fig.4-21** shows the waveform of proposed transmitter outputs.

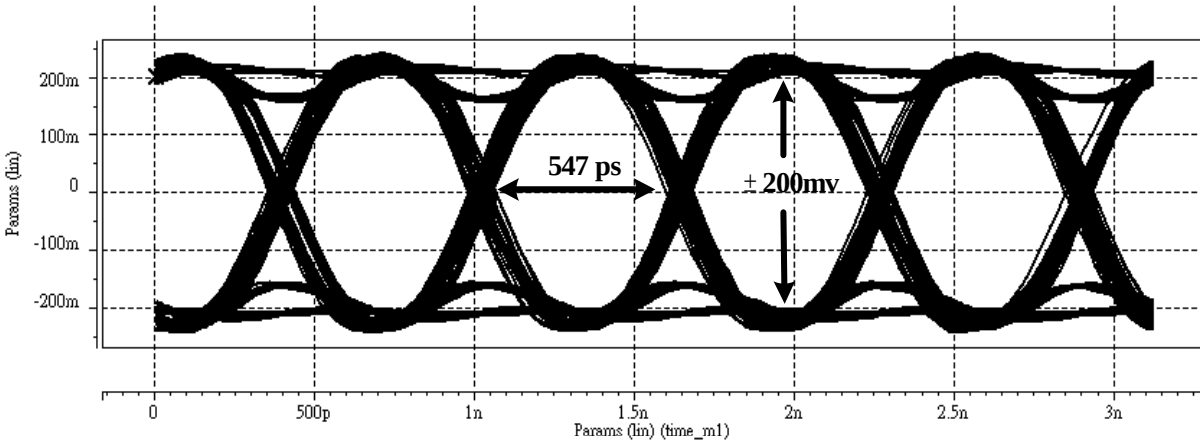


**Fig.4-21 eye diagram of output (Without data preskew)**

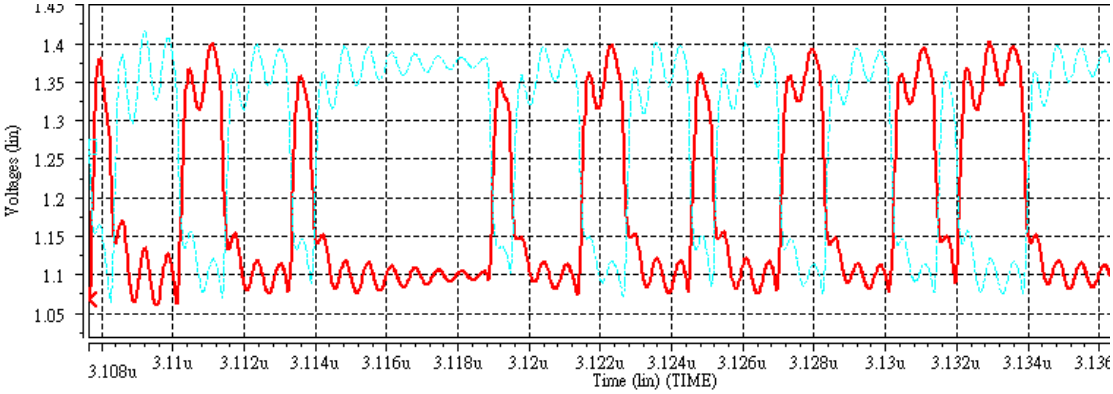


**Fig.4-21 Simulation result of the transmitter output waveform**

# Chapter 5
# Receiver

## 5.1 Architectureof Receiver

This chapter presents the receiver design. **Fig. 5-1** and **Fig. 5-2** show the block diagrams of the receiver architecture with Type 1 and Type2. The purpose of the receiver is to recovery the received signal to the original data by amplifying and sampling the signal. Then, the de-multiplexer makes recovered serial data become four parallel data.

**Fig. 5-1** and **Fig. 5-2** show the block diagrams of the receiver architecture with Type 1 and Type2. Type 1 receiver receives 100MHz clock as **Fig. 4-4** for receiver. Type 2 receiver receives 800MHz clock as **Fig. 4-5** for receiver.

The Type 1 receiver consists of a PLL proposed in the chapter 3 to produce the clock signals at 400 MHz with eight even-spaced phases. By using 4:1 de-multiplexer to parallelize a 1.6Gbps data into low-speed four channels parallel data, we can reduce the frequency requirement of the timing circuits and the digital logic. Only four even-spaced phase is utilized for 4:1 MUX. The other is utilized for transferring 800MHz clock.

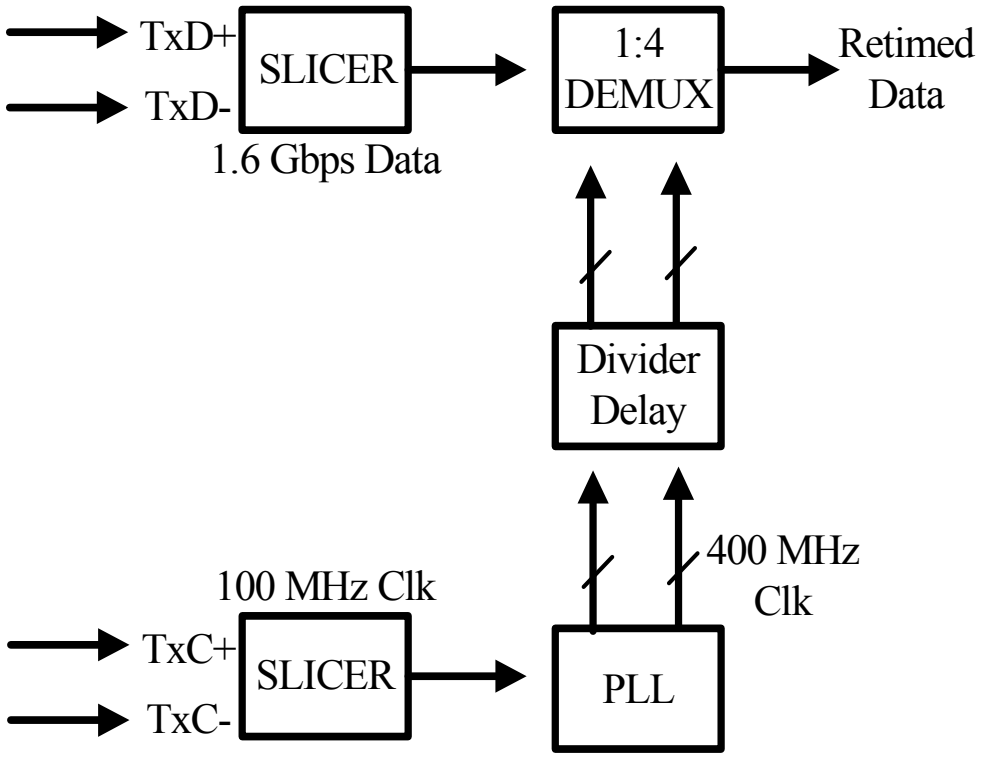


**Fig. 5-1 Block diagram of Type 1 receiver**

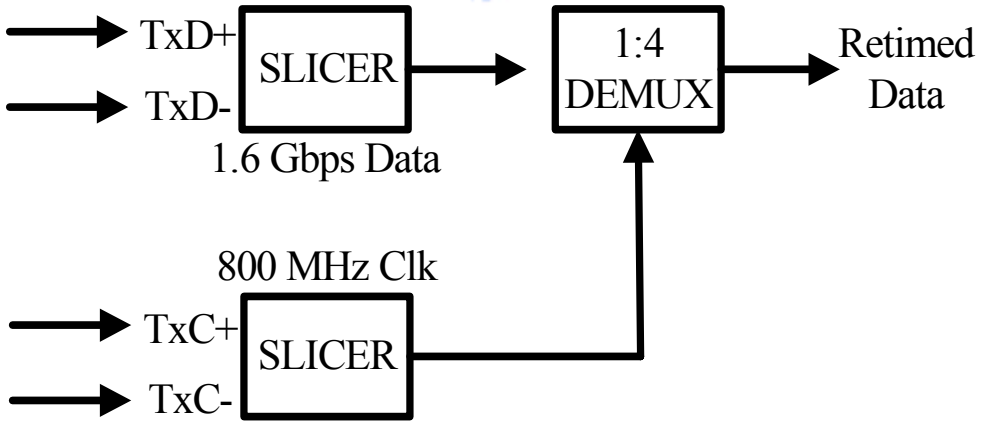


**Fig. 5-2 Block diagram of Type 2 receiver**

# 5.2 Slicer

**Fig. 5-3** shows the schematic of the slicer. The differential data will be distorted because of the inductance and capacitance resonance caused by bonding wire and pad when they enter the receiver chip. It plays a key role to sense received signals, either from system clocks or input data stream, therefore input sensitivity, symmetry and bandwidth are major concerns. It is an open-loop comparator in the receiver circuit. To meet the common mode voltage range, the circuit is implemented with PMOS input differential pairs with a constant current source and using NMOS crossed-coupled pairs as the load.

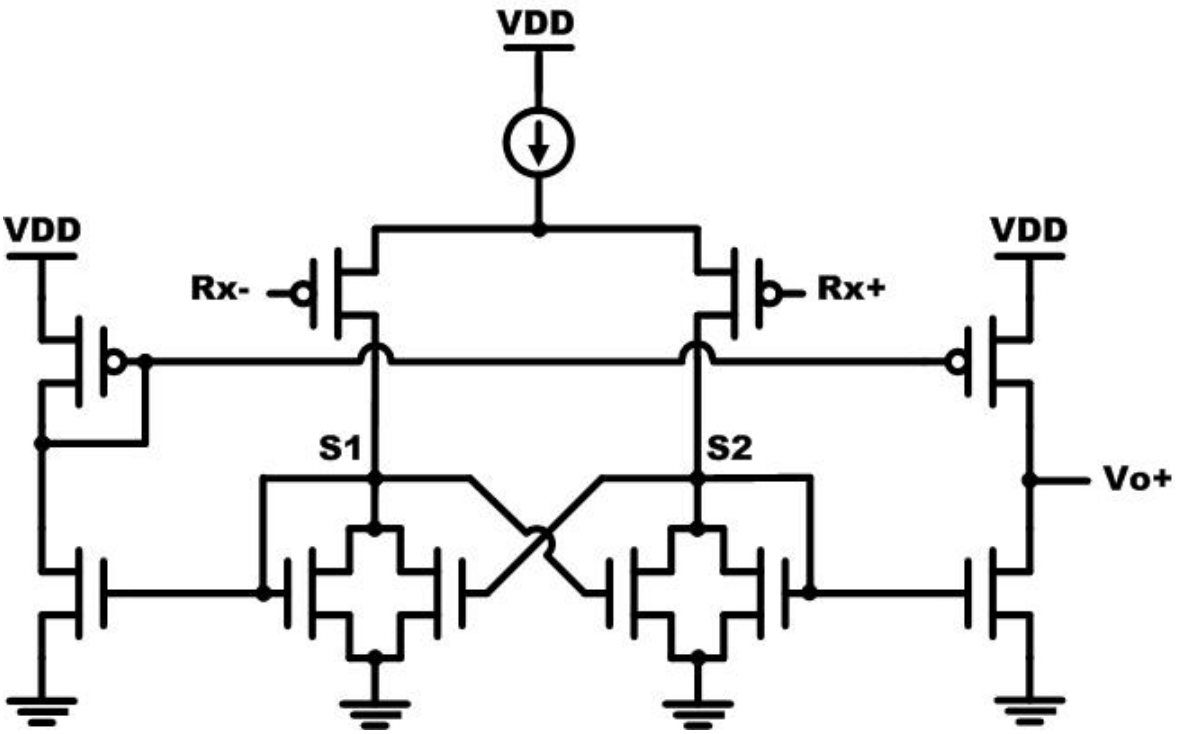


**Fig. 5-3 Schematic of slicer**

The gain and bandwidth of the slicer should be carefully designed to meet the requirement, because the slicer needs to be able to detect the received signals that were noisy and swing limited and amplify the signal to get the nearly full swing CMOS level at the output. Moreover, the offset voltage of the slicer also affects the

correct operation of the receiver. The offset voltage is not only due to the mismatches in the input devices but also mismatches (both device and capacitance mismatch) within the positive-feedback structure. These errors are referred back to the input as the input-offset voltage.

**Fig. 5-4** is the frequency response of the slicer. **Fig. 5-5** shows the hysteresis window of the slicer. The advantage of this hysteresis comparator is noise immunity. The data or clock stream sends to the following PLL or demux to get the data value.

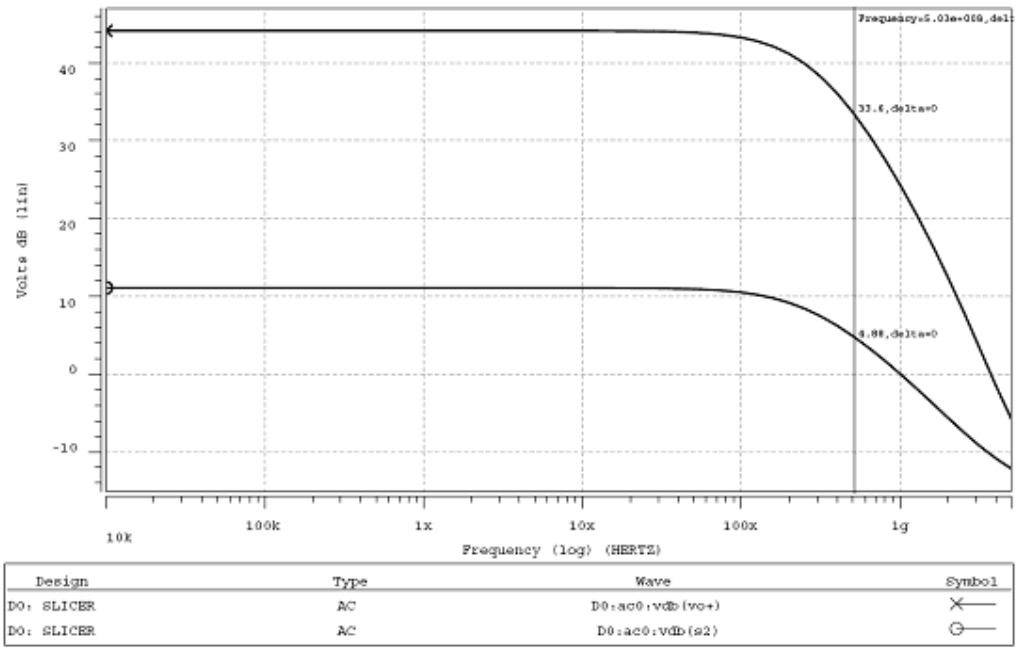


**Fig. 5-4 Frequency response of slicer**

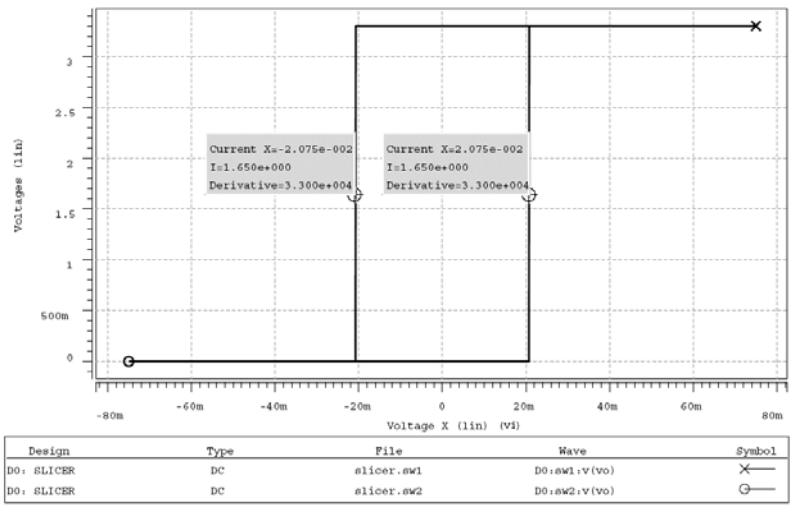


**Fig. 5-5 Hysteresis window of the slicer**

# 5.3 Circuit Implementation

## 5.3.1 Type 1 receiver

**Fig. 5-1** shows the block diagram of Type 1 receiver. When the Type 1 receiver receives the 100MHZ clock by Type 1 transmitter proposed in chapter 4, the PLL proposed in Chapter 3 must produce four-phases with 400MHz. It generates the required phases of clk0, clk1, clk2, and clk3**.** The relationship between output data, D0~D3, and clock (clk0, clk1, clk2, andclk3) is shown in **Fig. 5-7**. For example, at the timing interval between the rising edge of clk0 and the falling edge of clk3, the input signal D0 starts driving the de-multiplexer output.

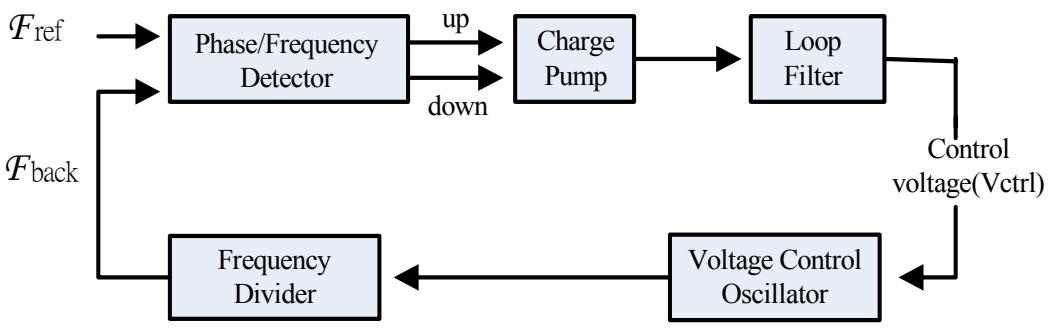


**Fig 5-6 Basic PLL Architecture**

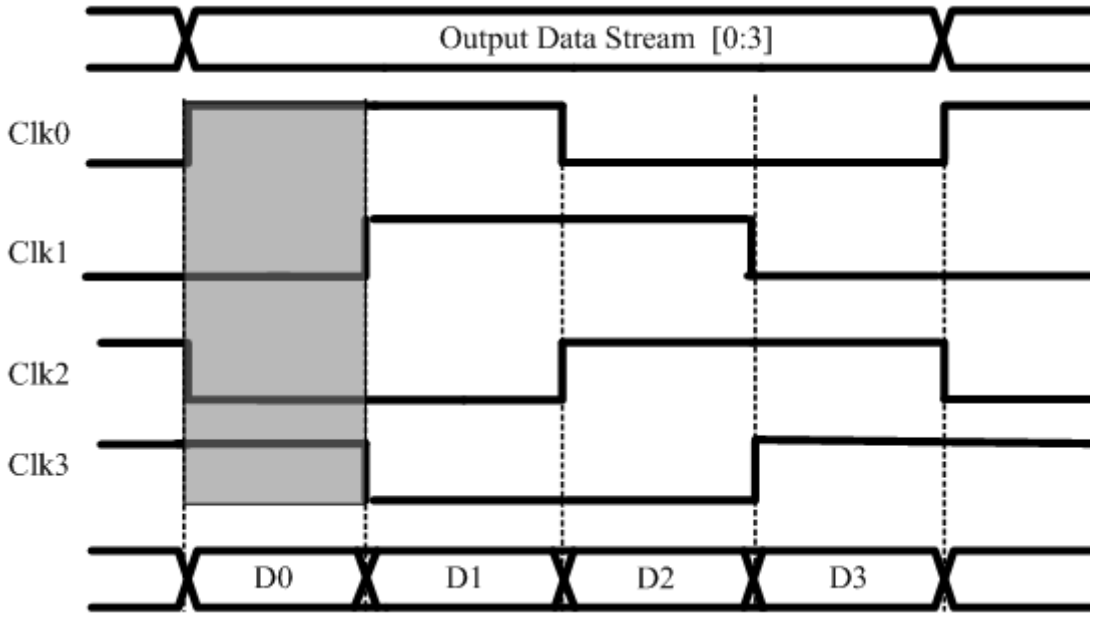


**Fig. 5-7 Timing diagram of data stream and clock**

As showed in **Fig. 5-6,** the clock that VCO generates passed through the divided-by-four divider compares with the reference clock Fref. Hence the phases of the clocks leads the phase of the data. Because the Fref (100MHz clock) form transmitter is utilized to give information about phase between clock and data. In order to ensure the phase between data and the clock is correct. A delay is added to clock path. **Fig.5-1** shows the clock path which includes delay circuit. **Fig. 4-14** shows TSPC D- flip-flop circuit and its delay cell.

In order to achieve this algorithm, the de-multiplexer, as shown in **Fig. 5-8**, is used to parallelize the serial data stream with 1.6Gbps into four parallel data channels D0~D3. High de-multiplexer fan-out may become the bottleneck and the achievable speed gradually decreases.

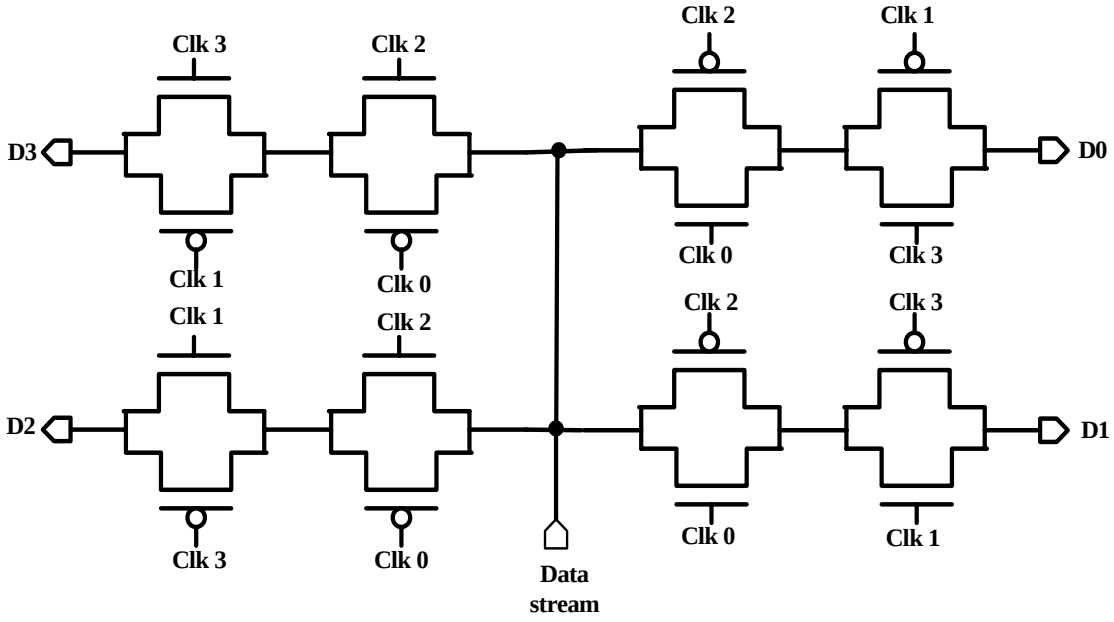


**Fig. 5-8 Block Diagram of 1-4 De-multiplexer**

## 5.3.2 Type 2 receiver

**Fig. 5-2** shows the block diagram of Type 2 receiver. When the Type 2 receiver receives the 800MHZ clock by Type 2 transmitter proposed in chapter 4. The relationship between input data stream and 800 MHz reference clock is shown in **Fig.4-5**. The edge of 800MHz clock edge will be located at the midpoint of each bit by clock process. Then, the de-multiplexer makes recovered serial data become four parallel data.

The asynchronous tree-type de-multiplexer architecture overcomes device limitations by using both rising and falling clock edges, as shown in **Fig. 5-9**. As a result, a tree-type de-multiplexer is able to operate at half the speed of the data rate. The small numbers of high-speed-operated devices in the tree-type architecture do

make it more suitable for high speed operation with low power consumption.

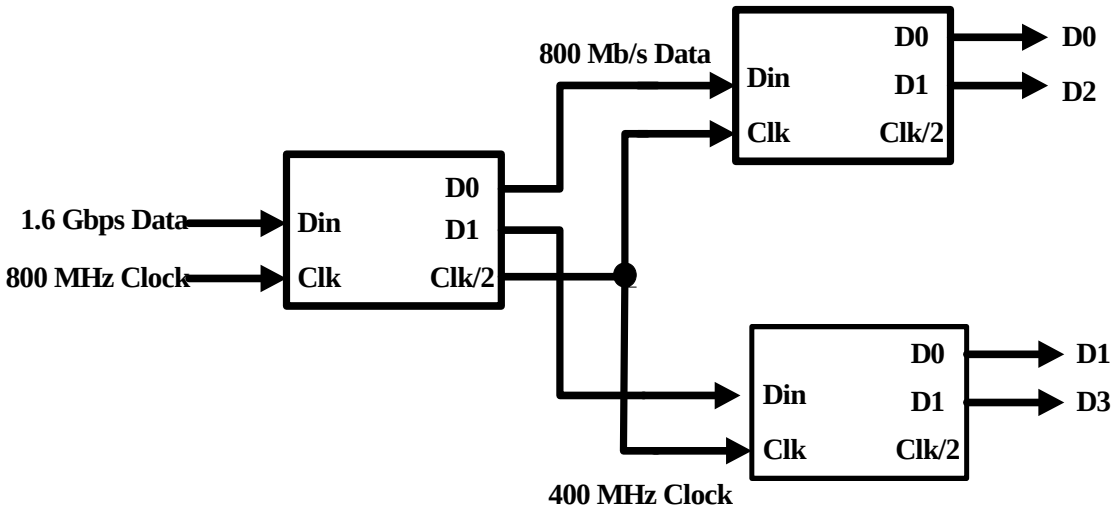


**Fig. 5-9 Asynchronous tree-type 1:4 de-multiplexer**

As shown in **Fig. 5-10 (a)**, a 1:2 DEMUX module does not require precisely controlled clock distribution; **Fig. 5-10 (b)** is its timing diagram. It not only generates the output data but also an optimized clock for the next stage. An asynchronous tree-type 1:4 de-multiplexer is obtained simply by connecting such 1:2 DEMUX modules.

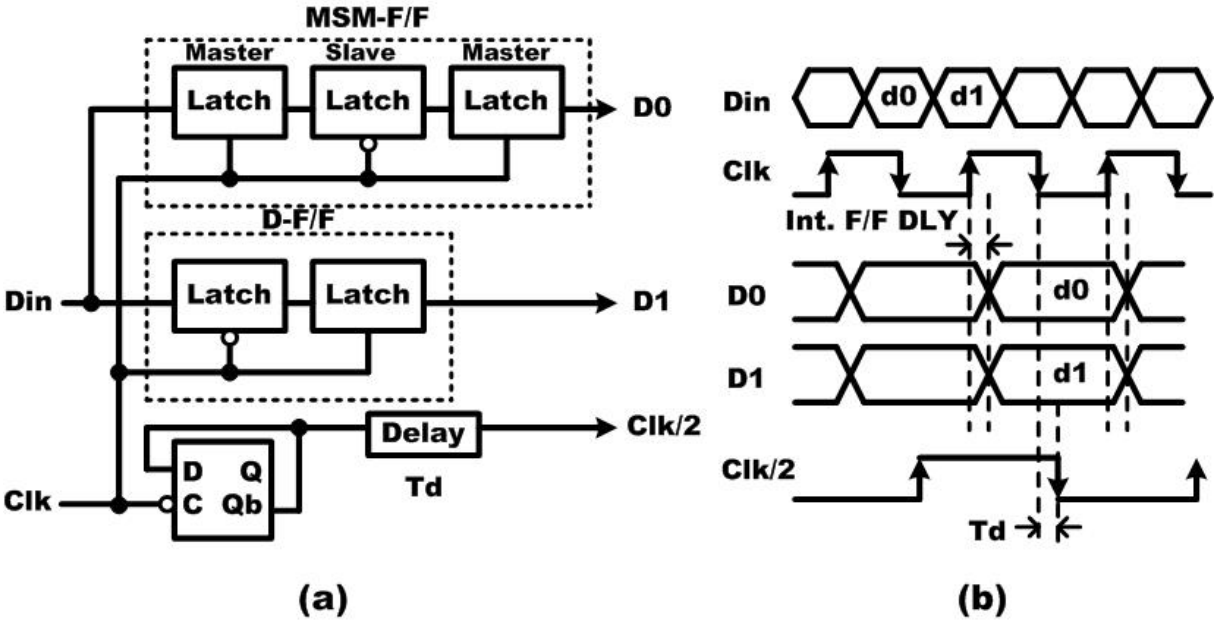


**Fig. 5-10 (a) 1:2 DEMUX module and (b) timing diagram**

The module contains a clock divider for the next stage, as well as a D-flip-flop (D-F/F) and a master-slave-master type flip-flop (MSM-F/F) for data. The module operates at half the clock speed of the input data rate. This is because this module operates using both rising and falling clock edges. **Fig. 5-11** shows Schematic of positive latch. These latched data are output at rising edges of the clock by the second master latch in the MSM-F/F. In this way, two bit output data D0 and D1 are synchronized with the rising edges of the input clock. A divided clock Clk/2 is generated at the falling edges of the input clock. With the delay circuit, which adjusts the timing between D0/D1 and Clk/2, the timing of the Clk/2 for each next stage is set at the precise center of each D0/D1 eye. That is to say, the 1:2 DEMUX module generates optimized timing between the divided clock and the data for the next stage DEMUX modules.

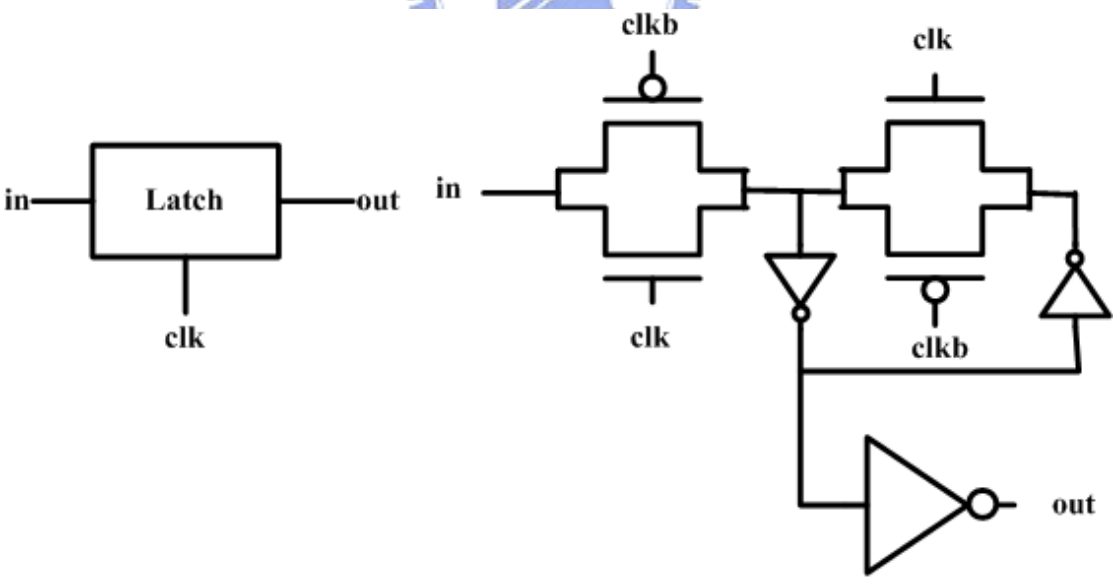


**Fig. 5-11 Schematic of positive latch**

# 5.4 Receiver Simulation Result

The circuit level simulations of the tracking receiver are made in order to ensure

the proper operation under a specified skew amount between data and clock channels. **Fig. 5-12** top graph is the time domain front-end received signal with transmitter and the differential swing is about 400 mV and down graph shows the corresponding output signal of the slicer, the limited received signals are being amplified to the full scale.

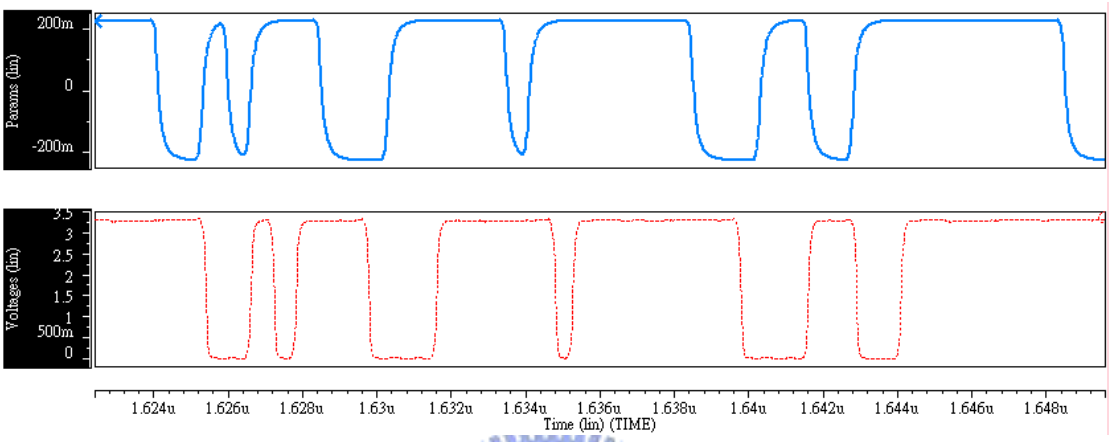


**Fig. 5-12 Time domain of the received signal and output of the slicer**

# 5.4.1 Type 1 receiver

**Fig. 5-13** shows the timing diagram of the received data and clock, and the clock which the PLL generate for de-multiplexer. Since the ripple on the control voltage is the source of the jitter, reducing the amplitude of the control voltage in the lock state is necessary. In this work, the ripple control voltage is about 4mV, as **Fig. 5-14**. After the PLL is locked with the reference 100 MHz clock, the input serial data stream with 1.6 Gbps is divided into four parallel channels with 400 Mbps, as shown in Fig.4-27. It shows the data input (din) and four parallel data outputs of the de-multiplexer (Dout0~Dout3).

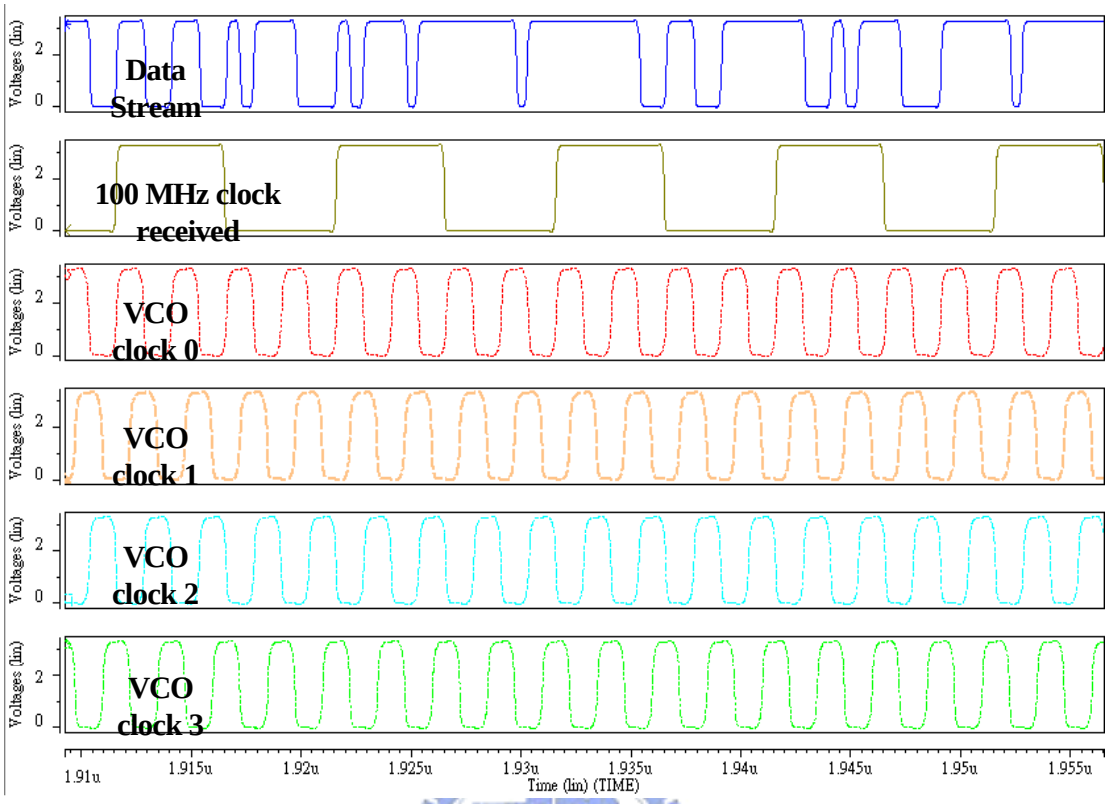


**Fig. 5-13 Timing diagram of the received data and clock, and the clock which PLL generate for de-multiplexer**

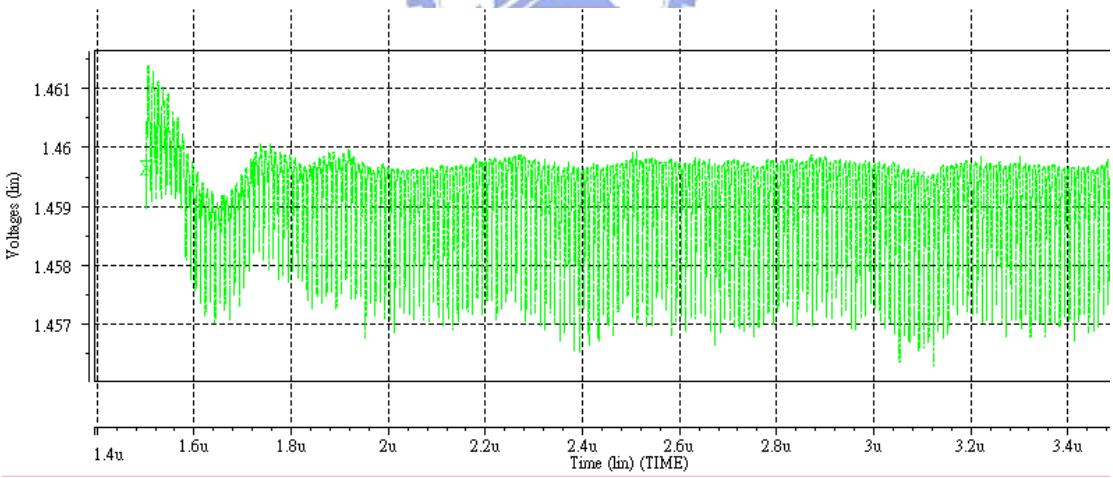


**Fig. 5-14 Control voltage of the PLL in the TYPE 1 receiver**

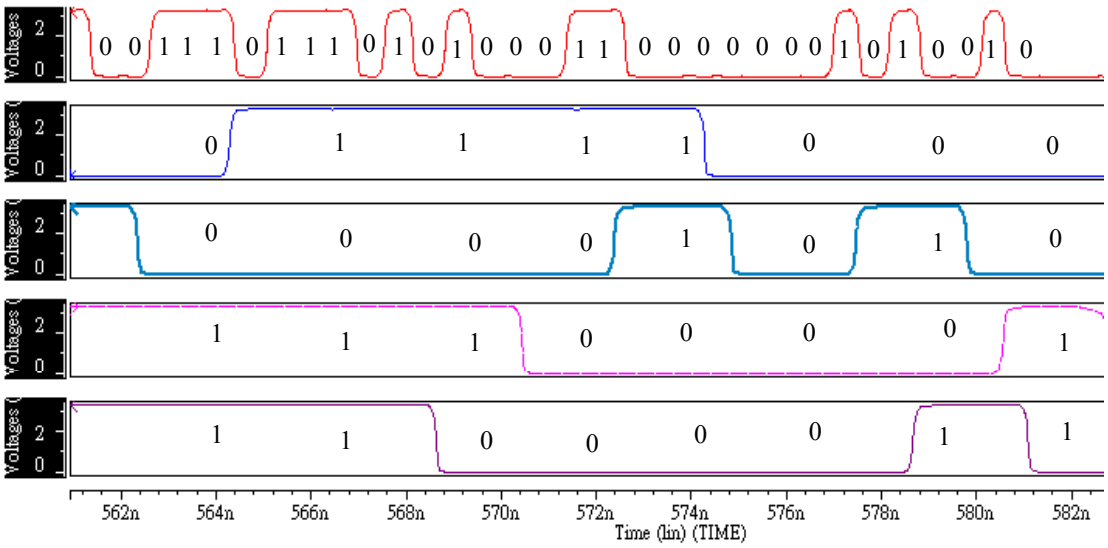


**Fig. 5-15 Four parallel data outputs of the Type 1 receiver**

# 5.4.2 Type 2 receiver

**Fig. 5-15** top graph is received data signal passed through the slicer and down graph shows the corresponding clk signal passed through the slicer. The 800 MHz reference clock is almost located at the midpoint of the input data. **Fig. 5-16** shows the outcome of the receiver. Din is the input data of the receiver and Dout0~Dout3 are the four parallel output.

For testing the tracking ability of the receiver, we change the input data and clock by 90° when the PLL is locked already. As shown in **Fig. 5-17**,the phase of data Is changed at XX, the control voltage ripples and it take the PLL about XX to regain the lock state.

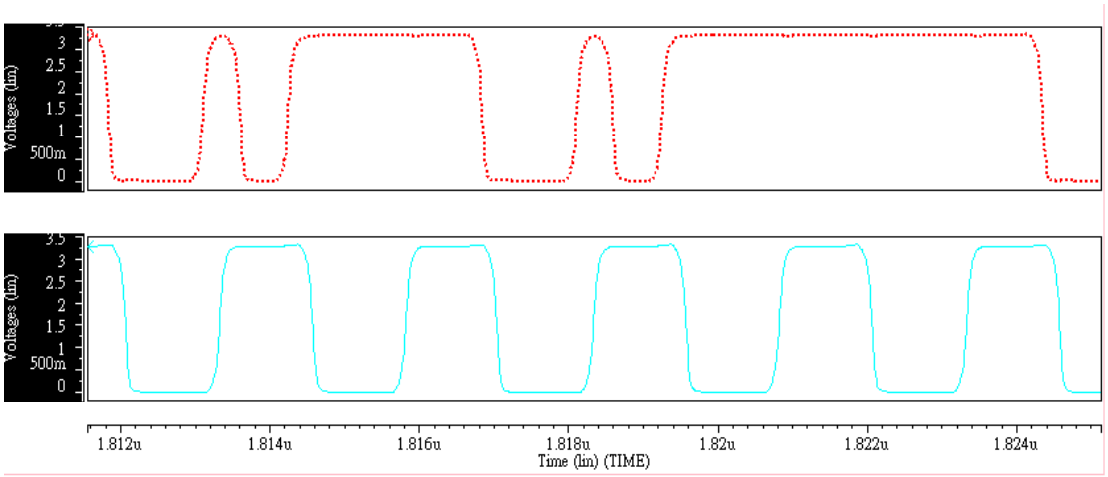


**Fig. 5-16 Timing diagram of the received data and clock**

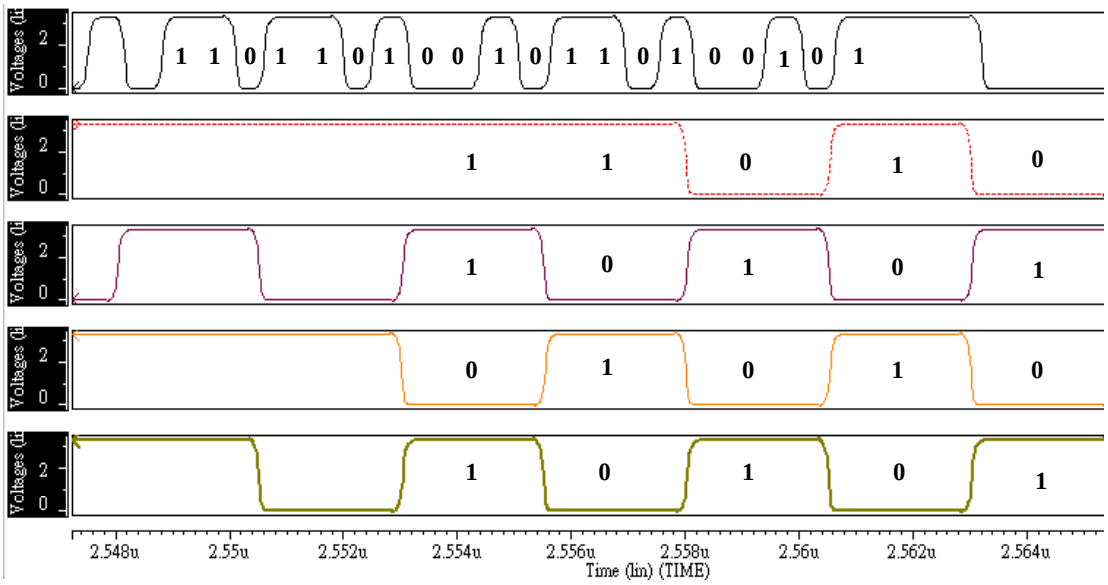


**Fig. 5-17 Four parallel data outputs of the Type 2 receiver**

# Chapter 6

# Conclusion and Future work

## 6.1 Conclusions

In this thesis, we had completed the design of the transceiver based on RSDS interface including two types of transceiver. It is a way to communicate data using a very low voltage swing (about 200mV) differentially over two printed circuit board (PCB) traces or a balanced cable. We have devoted to design two types transceiver with the data rate at 1.6Gbps. And, the transceiver is fabricated in 0.35um 2P4M process. Transmitter is composed of PRBS, eight-phases PLL, 4-to-1 multiplexer, clock process circuit, clock driver and data driver. The first block we discussed is the phase-locked loop (PLL). The main issue of the PLL is to generate the required phases used for the 4:1 multiplexer of the transmitter while making the timing jitter as small as possible. This may be done from system level to circuit level, including parameter design. The input reference of eight phases PLL is 100 MHz; it outputs a uniformly distributed 400 MHz clock. The PLL is composed of Phase Detector, Charge Pump, Loop Filter, Voltage Control Oscillator and a divided-by-two. Eight phases PLL output a uniform distributed clock for multiplexer to convert parallel data to serial data and for clock process circuit to transfer information about data and clock In order to ensure the phase between clock and data, a clock process delay circuit is added to increase the current during the data transition..

The transmitter drives the serial data and clock on to the bus. Receiver is composed of a comparator with hysteresis and a clock recovery system to sample data. It uses the comparator to amplify incoming small signal to full swing, and clock recovery system to sample data correctly. Finally, the receiver converts serial data to four parallel data channel. Whole design issues of the receiver are described in chapter 5.

## 6.2 Future Works

The increasing demand for data bandwidth in networking has driven the development of high-speed and low-cost serial link technology. In order to achieve higher data rate, the serial interfaces must recover clock and data reliably and reduce transmitter jitter and open its data eye, increase receiver jitter tolerance, reduce clock data skew. For the transmitter, to increase even higher data bandwidth, the bandwidth-limited channels effect should be carefully treated. The PLL output jitter must be reduced and multiphase generation can be more uniform by using average resistors. For the receiver, the phase detector of the PLL can use current mode logic to reduce the switching noise and the power consumption. The retimed clock output jitter also must be reduced.

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