Chapter 3 Device fabrication

Base on the design in Chapter 2, the detail fabrication processes for the MUMPs and <111> silicon device are discussed.

3-1 MUMPs fabrication process [21]

The MUMPs is a commercial program that provides a cost-effective, proof of concept MEMS foundry service. MEMSCAP offers three standard processes as part of the MUMPs program: POLYMUMPs、METALMUMPs and SOIMUMPs. POLYMUMPs, a three layer polysilicon surface micromachining process, is used to fabricate the actuator for the reflection type spot scan system.

Fig 3-1 shows the cross-sectional view in POLYMUMPs. Polysilicon is used as the structural layers and phosphosilicate glass (PSG) is used as sacrificial layers.

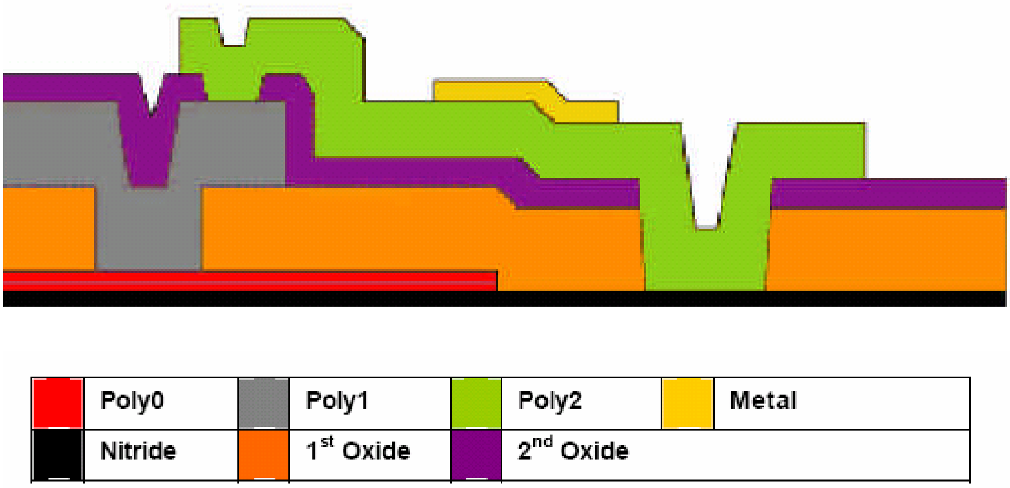


Fig 3-1 Cross section view showing all 7 layers of POLYMUMPs process (not scaled) [21]

The process begins with the deposition of a 600nm low-stress silicon nitride by LPCVD. This is followed directly by the deposition of a 500nm LPCVD polysilicon, POLY0. POLY0 then is patterned by photolithography and etched in a reactive ion etching (RIE) system (Fig 3-2(a)). A 2μm PSG (first oxide) sacrificial layer is then deposited by LPCVD and patterned with photolithography and RIE to define dimples and anchors (Fig 3-2(b)). After the anchor is etched, the first structural layer, POLY1, is deposited and patterned. After POLY1 is etched, the second PSG layer (second oxide) is deposited. Photolithography and RIE in this step (POLY1_POLY2_VIA and ANCHOR) are used to remove the second oxide over the POLY1 layer (Fig 3-2(c)).

The second structural layer, POLY2, is then deposited (1.5μm thick) followed by the deposition of a 200nm PSG. As with the POLY1 process, the PSG acts as etch hard mask and doping source for POLY2 and POLY2 is patterned by photolithography and RIE (Fig 3-2(d)). The final deposited layer is a 0.5μm metal layer by lift-off that provides for reflective mirror surface and electrical wire bonding (Fig 3-2(e)、(f)). The release is performed by immersion the chip in a bath of 49% HF for 4 to 5 minutes and followed by CO_2 drying (Fig 3-2(g)).

3-2 MUMPs fabrication result

A comb actuator with two symmetry triangular mirror in reflective type scan system was fabricated by the MUMPs process

The top and side views of the comb actuator are shown in Fig 3-3 after the final releasing step. In Fig 3-4, the releasing holes are used to increase the releasing speed in the HF solution; the dimples are used to prevent stiction in the drying process.

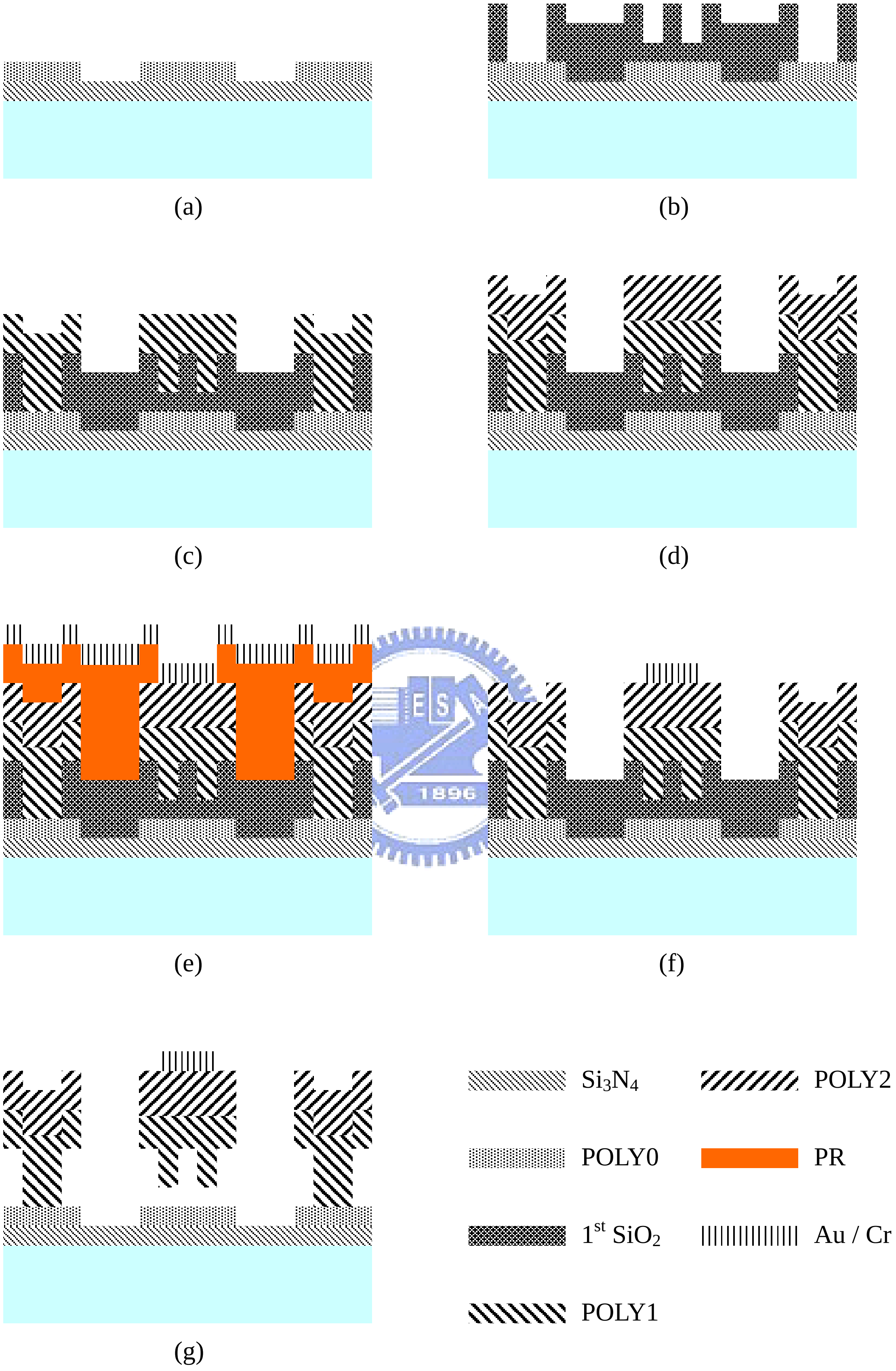
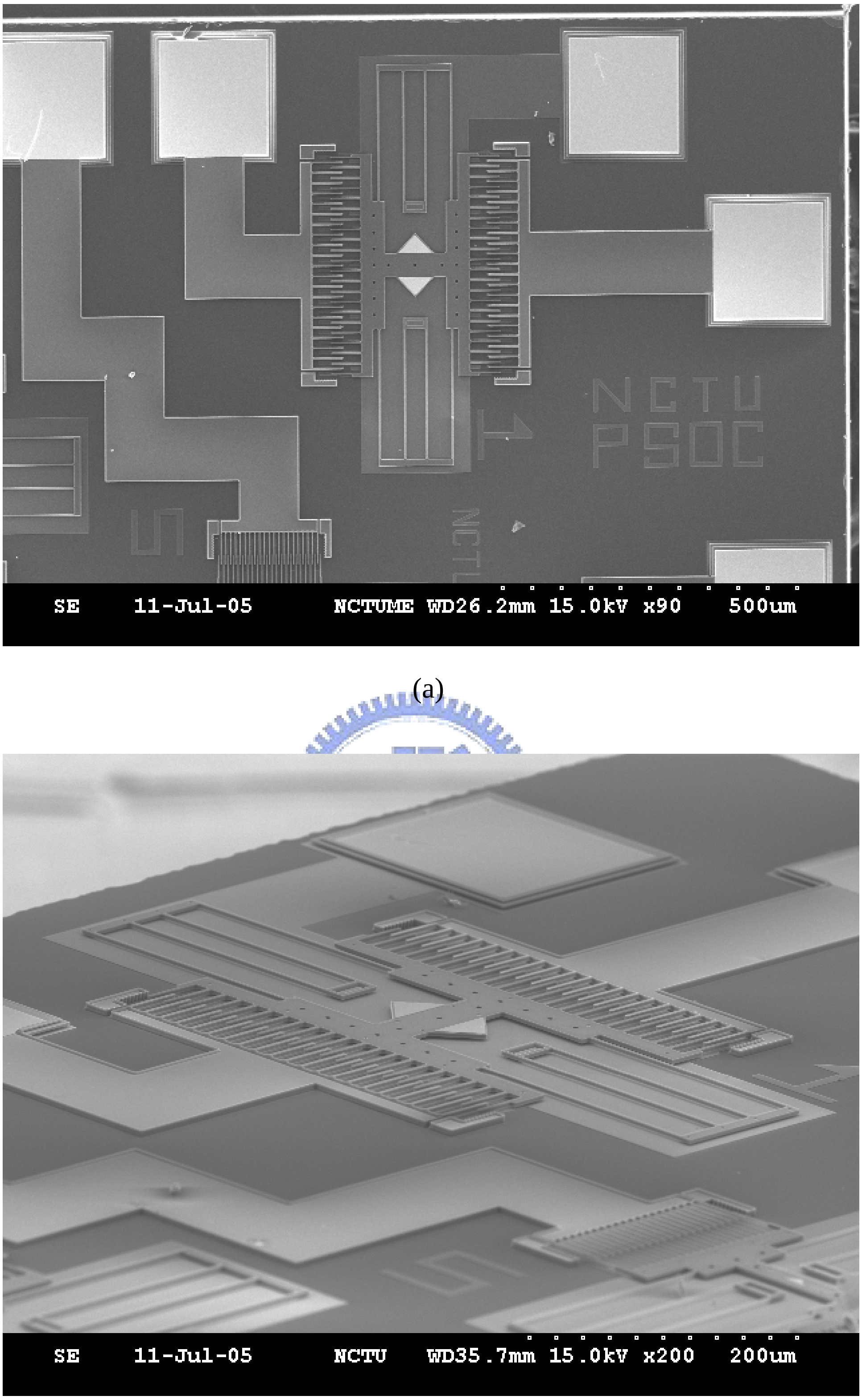

(a) (b) (c) (d) (e) (f) (g)

Fig 3-2 MUMPs process steps



(a)

(b)

Fig 3-3 SEM photographs of the MUMPs comb actuator, (a) top view (b) side view

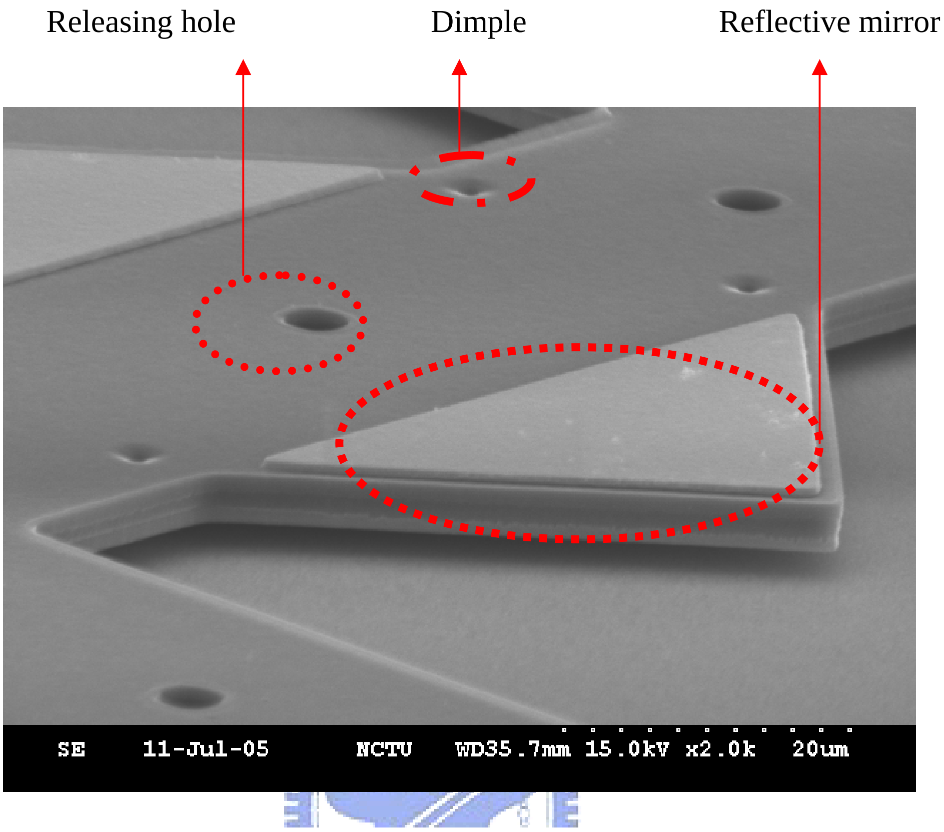


Fig 3-4 Close-up view of the MUMPs comb actuator

3-3 <111> silicon fabrication process

For absorption type devices, single crystalline silicon was used for better photo detector performance. Instead of a reflective mirror, a triangular p-n photo diode was fabricated in the middle of the movable structure and served as the knife edge sensor.

In the process, the features of surface micromachining and bulk micromachining processes are integrated. CVD oxide/nitride are used for etching mask and electrical isolation for sensing and pad interconnection. Inductively coupled plasma (ICP)-RIE is used to define the thickness of comb actuator and the releasing gap. Sidewall passivation technology is adopted to divide the silicon substrate into the structural layer and the sacrificial layer.

Several runs of fabrication had been tried. The first run process begins with a 500μm p-type <111> silicon wafer with 8-12 $\Omega-\mathrm{cm}$ resistivity. A 250nm low-stress silicon nitride is deposited by LPCVD. The layer then is patterned by photolithography (first mask) and etched in a reactive ion etching (RIE) system (Fig 3-5(a)). Next, the wafer is heavily implanted with arsenic in the N^+ region (Fig 3-5(b)). The contact P^+ region is then fabricated by photolithography (second mask) patterning, RIE, and P^+ implantation (Fig 3-5(c)). This planar p-n junction serves as the photo detector as well as the isolation layer for the driving voltage applied to the comb. A 500nm oxide hard mask layer is then deposited by PECVD and patterned with photolithography and RIE (third mask) to define the comb actuator (Fig 3-5(d)). This oxide layer also serves as the isolation layer of aluminum interconnection between the photo detector and the comb actuator driving circuit.

After etching the hard mask oxide, a ICP-RIE process is used to define the single crystalline silicon comb actuator, followed by a lateral sidewall implantation (Fig 3-5(e)). This step forms a p-n junction along the vertical sidewall so that the driving voltage can be applied through the thickness of the comb actuator. This can reduce the required voltage. After the lateral sidewall ion implantation, a thin oxide (300nm) with excellent step coverage is deposited by PECVD (Fig 3-5(f)). The following RIE only etches the top and bottom oxides, but not the sidewall oxide, which serves as the sidewall passivation layer (Fig 3-5(g)).

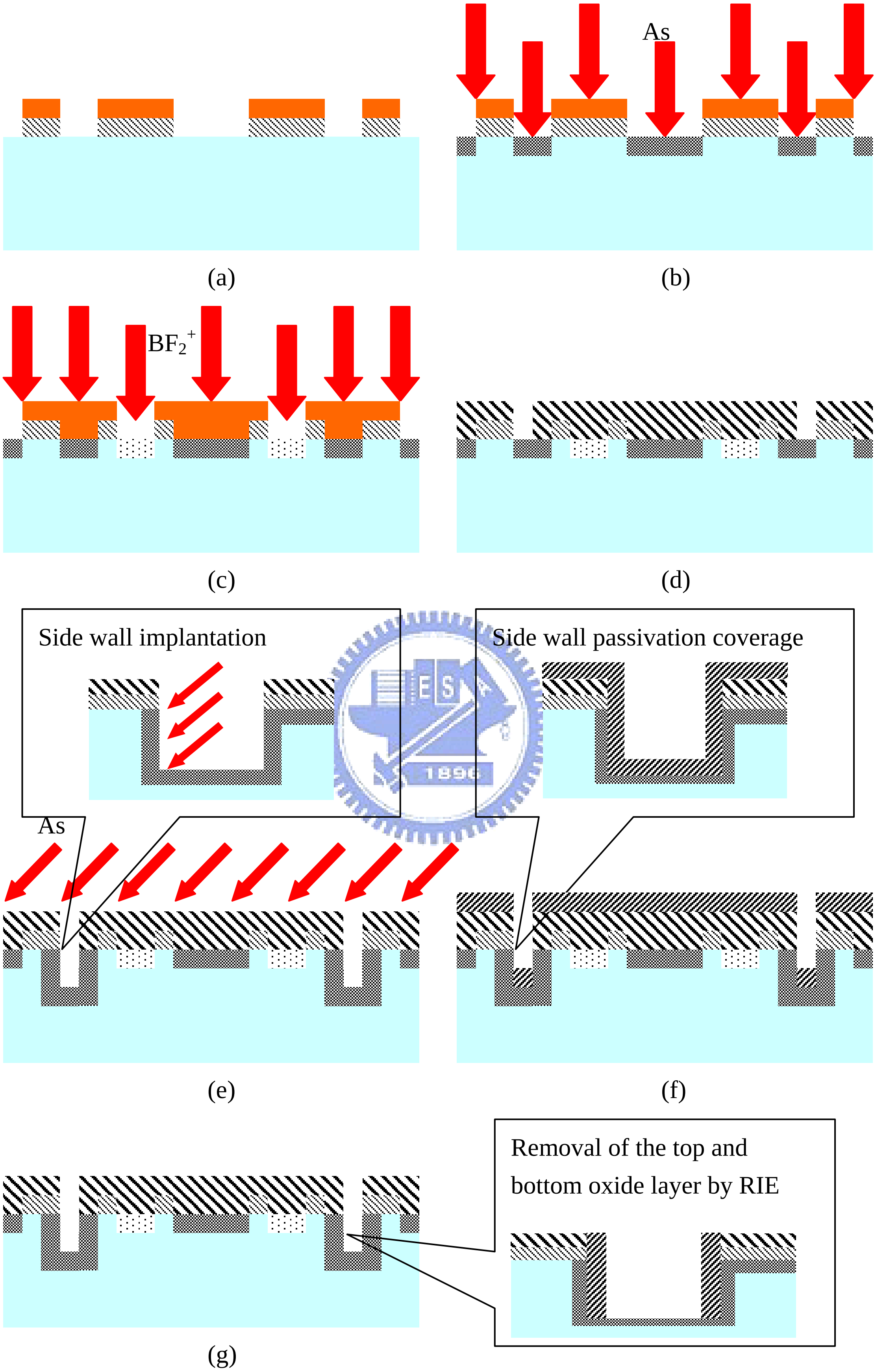
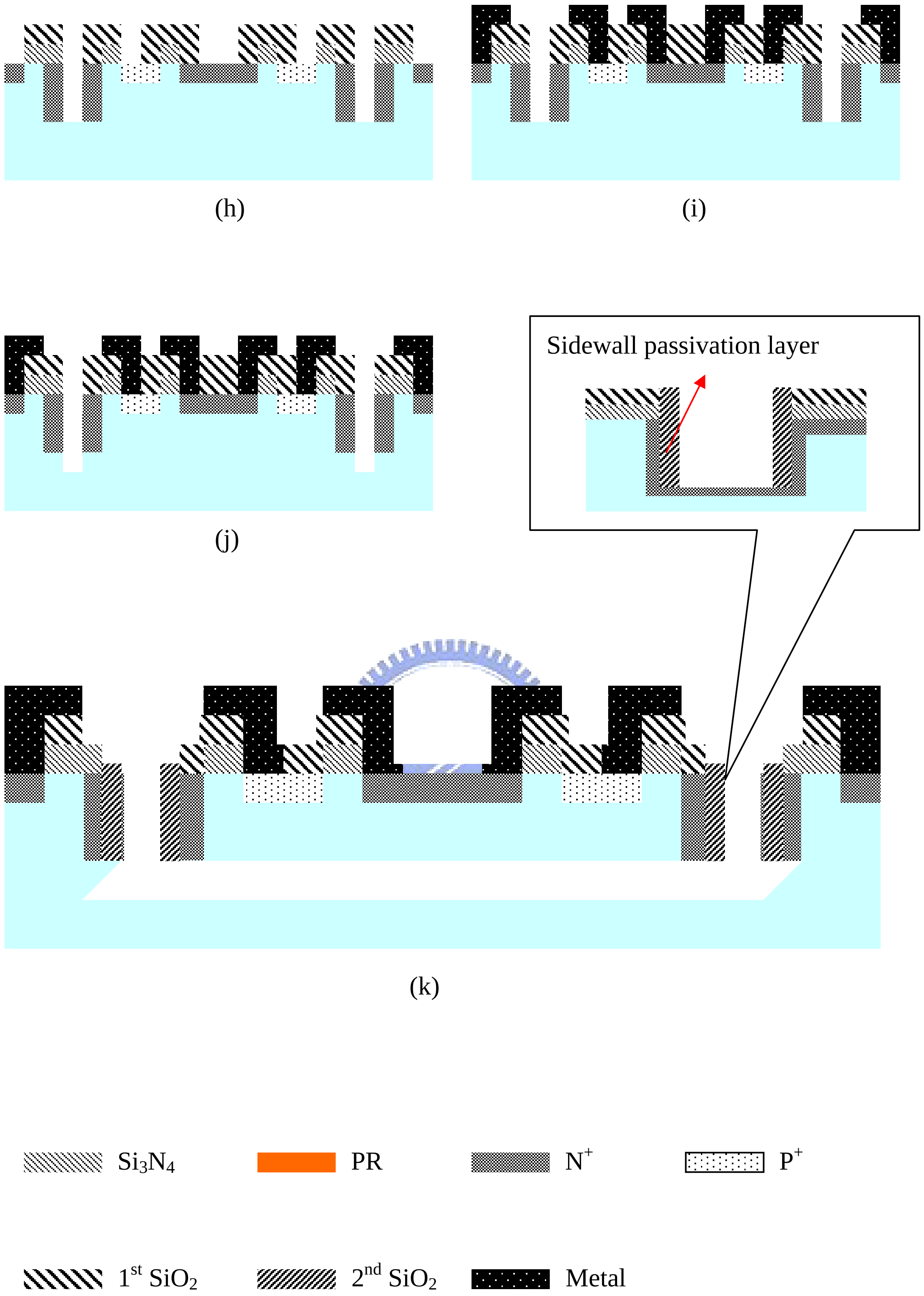


Fig 3-5 <111> silicon device process steps


(h)

(i)

(j)

(k)

Fig 3-5 <111> silicon device process steps (continued)

Next, photolithography (fourth mask) and RIE are used to remove the top oxide and nitride over the contact hole of comb actuator and the photo detector regions (Fig 3-5(h)). The deposited layer is a 0.3μm aluminum metal layer, patterned by lift-off (fifth mask) for reflective surfaces and interconnection for the photo detector (Fig 3-5(i)).

After metallization, the second ICP-RIE process is used to define the releasing gap (Fig 3-5(j)). The release is performed in a bath of 12.5% TMAH solution with 1.5% dissolved silicon and 0.5% $(NH_4)_2S_2O_8$ [22] and followed by several minutes of DI water rinse. Then IPA is used to reduce stiction and followed by at least half hour in an oven at 120°C (Fig 3-5(k)). The detail fabrication parameters are shown in Table 3-1.

Table 3-1 <111> silicon substrate fabrication process

Step	Instruments for process	Parameter	Thickness/Etch depth	Note
1.	p-type <111> silicon with 8-12 Ω-cm wafer RCA cleaning	Standard RCA clean		
2.	LPCVD Si_3N_4	800℃ 180mTorr SiH_2CL_2 / NH_3 =105：35	250nm	Color：blue-purple
3.	1st litho (FH6400)	1st spin 1000 rpm 2nd spin 3000 rpm soft bake 90℃ 2 min exposure 26 sec with filter hard bake 90℃ 25 min	PR TK=1.8 um	

4.	RIE Si_3N_4	50mTorr SF_6 / CHF_3 =30：10 Power=100W	250nm	Etch until the silicon is revealed.
5.	As ion implantation	Dose 3e15 /cm^2 Ion energy 60KeV Tilt 7^0 Twist 22^0		Activate with RTA at 950℃ for 10sec to 15sec
6.	O_2 plasma	10mTorr O_2 =40 ICP=400W Bias=100W		
7.	2nd litho (FH6400)	1st spin 1000 rpm 2nd spin 3000 rpm soft bake 90℃ 2 min exposure 26 sec with filter hard bake 90℃ 25 min	PR TK=1.8 um	
8.	RIE Si_3N_4	50mTorr SF_6 / CHF_3 =30：10 Power=100W	250nm	Etch until the silicon is revealed.
9.	BF_2^+ ion implantation	Dose 3e15 /cm^2 Ion energy 30KeV Tilt 7^0 Twist 22^0		Activate with RTA at 950℃ for 5sec to 10sec
10.	O_2 plasma	10mTorr O_2 =40 ICP=400W Bias=100W		
11.	Hard mask oxide deposited by PECVD	350℃ 150mTorr TEOS / O_2 =10：800 Power=200W	500nm	Color：green
12.	3rd litho (FH6400)	1st spin 1000 rpm 2nd spin 3000 rpm soft bake 90℃ 2 min exposure 26 sec with filter hard bake 90℃ 25 min	PR TK=1.8 um	

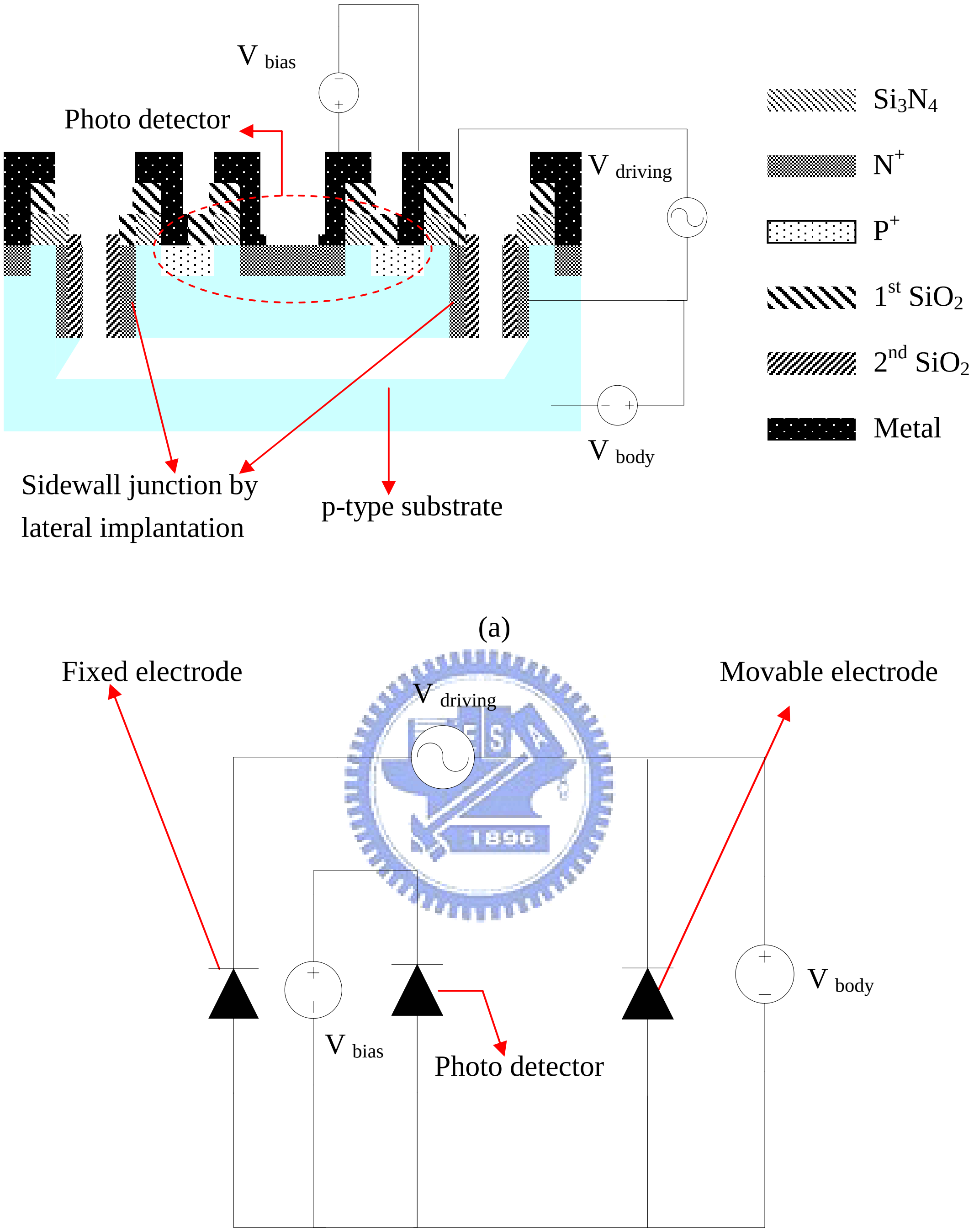
13.	RIE SiO_2 hard mask layer	50mTorr SF_6 / CHF_3 =30：10 Power=100W	500nm	Etch until the silicon is revealed.
14.	Remove PR	Immersion in ACE for 5 min Immersion in H_2SO_4 ： H_2O_2 = 3：1 for 5 min		
15.	1st ICP process	Bosch by ALCTEL (NARC)	6um	Using WYKO to measure the step height
16.	Sidewall As ion implantation	Dose 1e15 /cm^2 Ion energy 60KeV Tilt 45^0 Twist 73^0 Rotation 4 times		The pattern must be orthogonal to the wafer flat edge
17.	O_2 plasma	10mTorr O_2 =40 ICP=400W Bias=100W		
18.	PECVD for sidewall protection layer	1st -1 PECVD run 350℃ 300mTorr TEOS / O_2 =10：800 Power=100W 1st -2 PECVD run 350℃ 150mTorr TEOS / O_2 =10：800 Power=200W 2nd LPCVD run 850℃ 180mTorr SiH_2CL_2 / NH_3 =85：17	1st -1 PECVD run =300nm 1st -2 PECVD run =650nm 2nd LPCVD run =550nm	1st -2 PECVD run => anneal at 600℃ O_2 rich environment for 1hour
19.	RIE SiO_2 / Si_3N_4 sidewall protection	1st -1 run 20mTorr CHF_3 / O_2 =20：4	1st -1 run =300nm	Multiple etch is required to

	layer	Power=120W 1st -2 run 20mTorr CHF_3 / O_2 =20：4 Power=120W 2nd run 50mTorr SF_6 / CHF_3 =30：10 Power=100W	1st -2 run =650nm 2nd run =550nm	exactly control the etching depth and the RIE system must be with high anisotropic character
20.	4th litho (AZ4620)	1st spin 1000 rpm 2nd spin 1500 rpm placing in room temperature for 15 min soft bake 90℃ 15 min exposure 450 sec with filter hard bake 90℃ 25 min	PR TK≒10 um	
21.	RIE SiO_2 contact hole	50mTorr SF_6 / CHF_3 =30：10 Power=100W	TK= =750nm	Etch until the silicon is revealed.
22.	Remove PR	Immersion in ACE for 10 min		
23.	5th litho (AZ4620)	1st spin 1000 rpm 2nd spin 1500 rpm placing in room temperature for 15 min soft bake 90℃ 15 min exposure 450 sec with filter hard bake 90℃ 25 min	PR TK≒10 um	
24.	Metallization	Thermal coating Aluminum	300nm	
25.	Remove PR	Immersion in ACE for 20 min		Immersion in ACE Until the Al on the PR is separated
26.	2nd ICP process	Bosch by ALCTEL (NARC)	1st -1,-2 run =20um	

			2nd run =40um	
27.	Wet etching	Immersion in 12.5% with 1.5% dissolved silicon and 0.5% $(NH_4)_2S_2O_8$ TMAH solution	Etching time > 30 min	Using probe to push the actuator to observe whether the silicon is released complete or not
28.	Baking	DI water 3 min IPA 10 min Placing wafer to an oven at 120 ℃	Backing time > 1hr and 30min	
*	Dry releasing process	Supported by NARC		The process basically similar to the Twins process by University Twenty.

3-4 Junction isolation

However, doping the junction to a depth of several μm needs long diffusion time at high doping temperature and the high temperature will ruin the photo detector. Therefore, the low temperature lateral implantation is used to form the N^+ region along sidewall. Junction isolation using a reverse biased diode is used to isolate different parts in the system. However, doping the junction depth of the integration process to several μm needs long diffusion time at high doping temperature. Therefore, the low temperature lateral implantation is used to form the N^+ region along sidewall.



(a)

(b)

Fig 3-6 The integration process (a) Isolation scheme (b) equivalent circuit

The electrical isolation of the system is shown in Fig 3-6(a). The body bias voltage V_{body} is set to be larger than driving ac voltage $V_{driving}$ of comb actuator to ensure the reverse bias condition of the isolation diode. In equivalent circuit, as shown in Fig

3-6(b), a bias voltage V_{bias} of photo detector is applied to get higher responsivity. The comb actuator and the photo detector are isolated by the three p-n junctions.

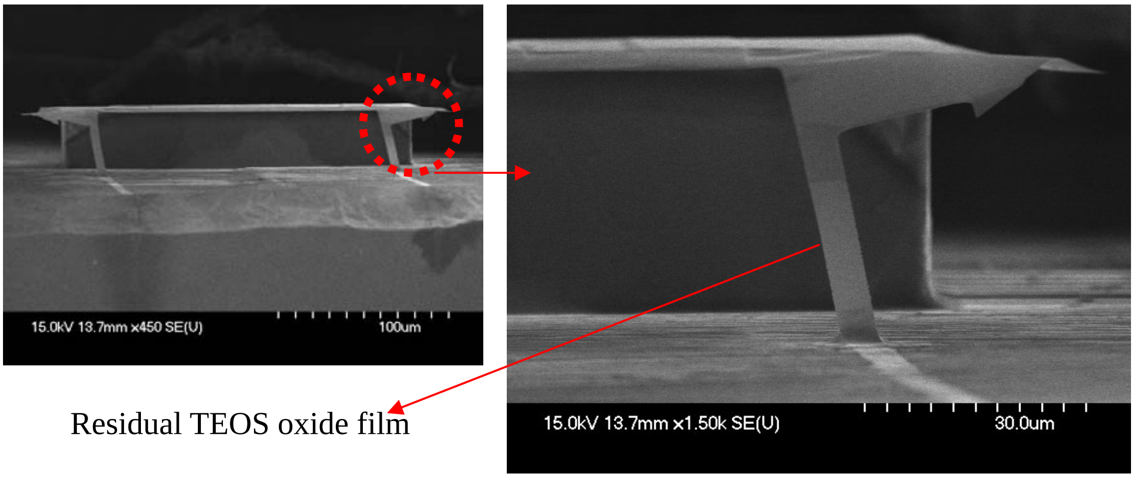
3-5 Issues of the <111> silicon device fabrication

During the progress of the research, the <111> silicon device process had to be modified due to fabrication difficulties. Three runs had been tried. The issues encountered during fabrication and solutions are discussed in the section.

3-5-1 First run

In the first run process, as discussed in the previous section, the hard mask oxide and sidewall passivation layer is deposited by TEOS PECVD with low RF power (100W) and high deposition pressure (300mTorr) without annealing. This step results in bad step coverage of the sidewall passivation film; also the quality of the film is bad and it will be etched by the TMAH solution. Fig 3-7 shows the structure silicon etched by TMAH due to bad step coverage and bad quality of the film.

The step coverage of TEOS based PECVD oxide can be improved by deposition at higher RF power and lower chamber pressure. Therefore, another TEOS source PECVD oxide with RF power 200W and pressure 150mTorr was deposited and annealed in O_2 rich environment at 600℃ for 30 minutes to improve the film quality [23]. This layer can be used as the sidewall passivation layer. The results are as shown in Fig 3-8, where the TEOS oxide film is delaminated from the sidewall structure. The delamination may be due to the porous structure of the oxide layer.



Residual TEOS oxide film

Fig 3-7 Sidewall passivation layer of the first run process after releasing

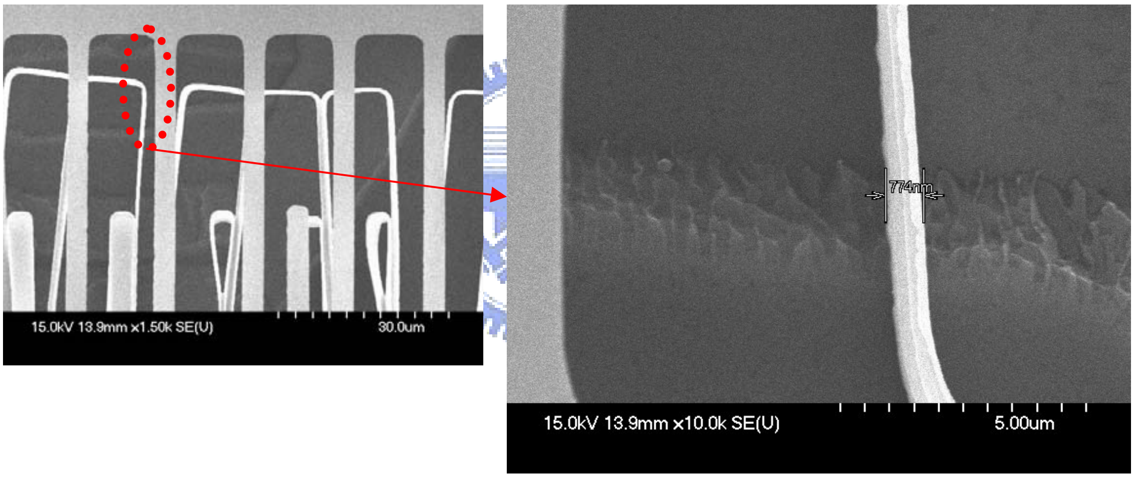
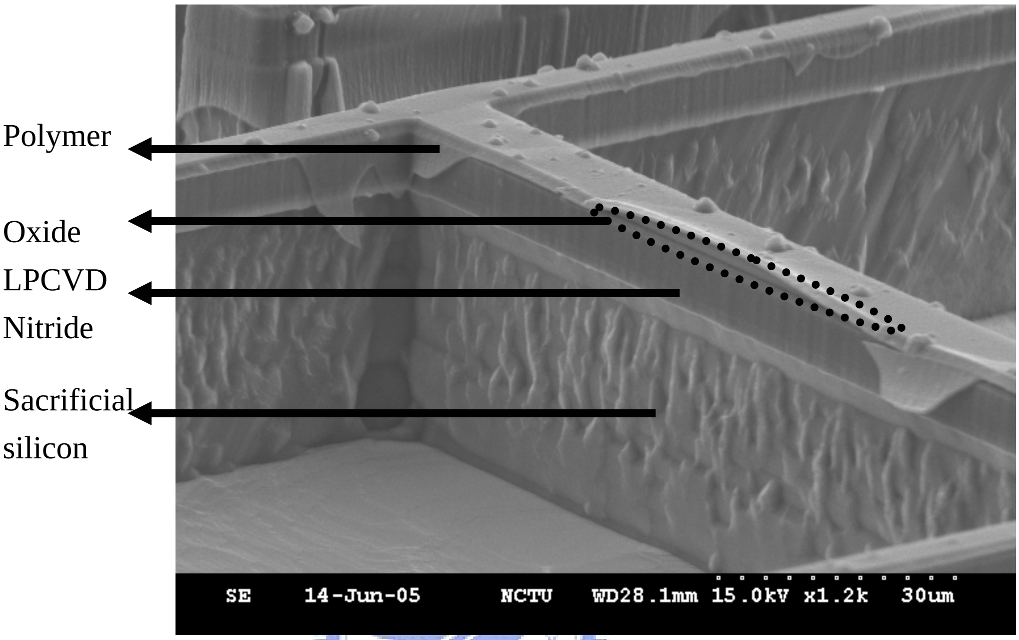


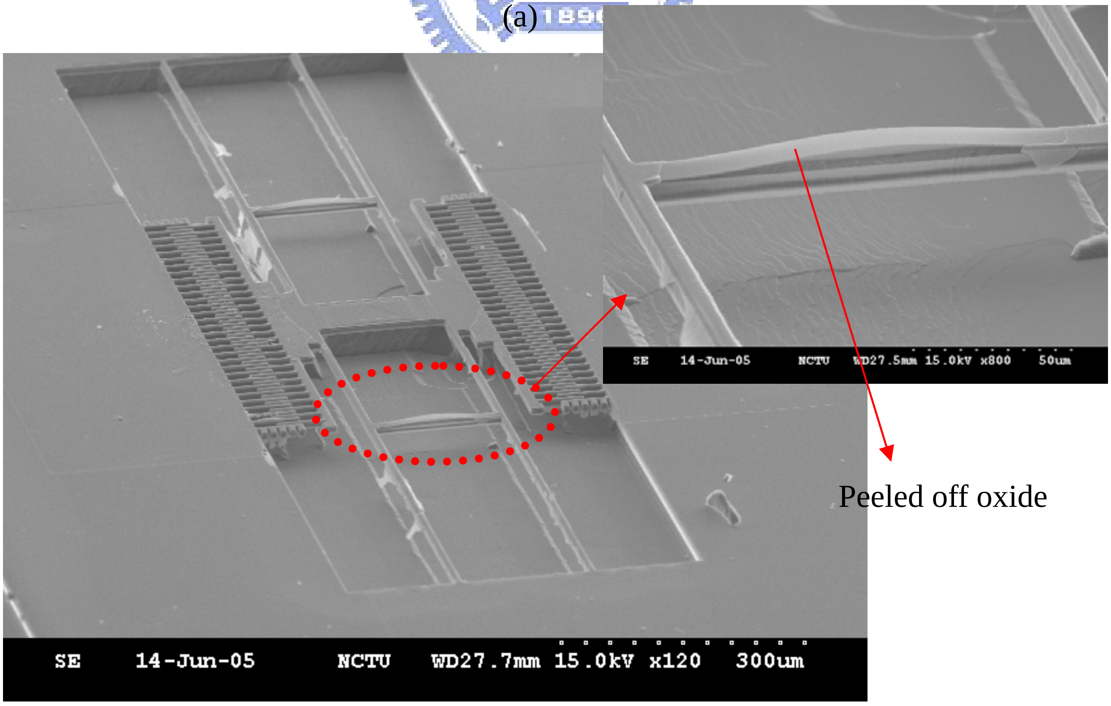
Fig 3-8 Sidewall passivation oxide deposited with RF power of 200W, pressure of 150mTorr, and annealing in O_2 rich environment after releasing

3-5-2 Second run

In the first run process, although the step coverage can be solved by deposition at higher RF power and lower chamber pressure, the porous oxide structures result in the film delamination and failure process. To solve this problem, LPCVD nitride was used in the second run to obtain a sidewall passivation layer with excellent step coverage and film quality.



(a)



(b)

Fig 3-9 Second run device etched for (a) 3 minutes (b) 7 minutes in TMAH solution

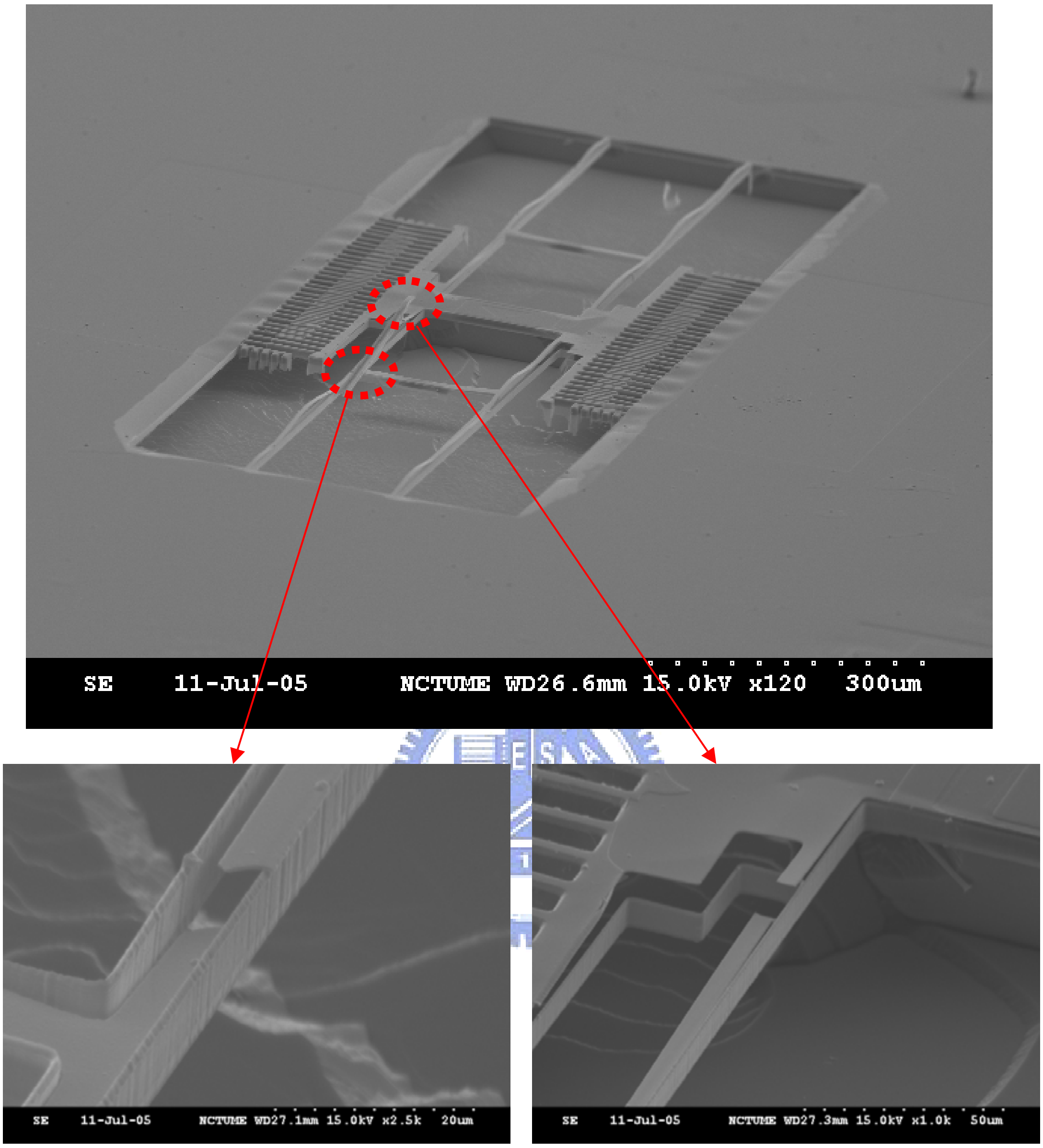


Fig 3-10 Second run device etched for 10 more minutes in TMAH

Fig 3-9(a) shows the device fabricated with this process and then etched in TMAH for 3 minutes. The upper sidewall film was not etched by TMAH and the peeled off film is the residual polymer after the second ICP-RIE. Fig 3-9(b) shows the device etched in TMAH for 7 minutes. The top oxide hard mask layer was separated from silicon top surface. After releasing the device for 10 more minutes, the separation between top oxide and silicon was more obvious, as shown in Fig 3-10. The separation makes the silicon in the corner exposed to the etchant during releasing. Additionally, the break of hard mask oxide layer in the figure may be due to the residual stress.

To explain the separation, an ideal sidewall layer forming process is shown in Fig 3-11(a) [24]. In the ideal case, the dry etching is anisotropic and perpendicular to the surface of the wafer. Hence, the sidewall of the oxide hard mask layer and the oxide/nitride sidewall protection layer are perfectly vertical. In this case, the corner of the silicon structure is preserved and protected during the RIE processes.

However, if the dry etching process is not perfectly anisotropic, the corner of the film or silicon structures can be attacked in the etching process. This may results in the exposure of the silicon structure after the second ICP-RIE to define the releasing gap, as shown in Fig 3-11(b). In Fig 3-12, the trapezoidal oxide and the exposed silicon in the corner can be clearly seen. Possible solutions are discussed in the next section.

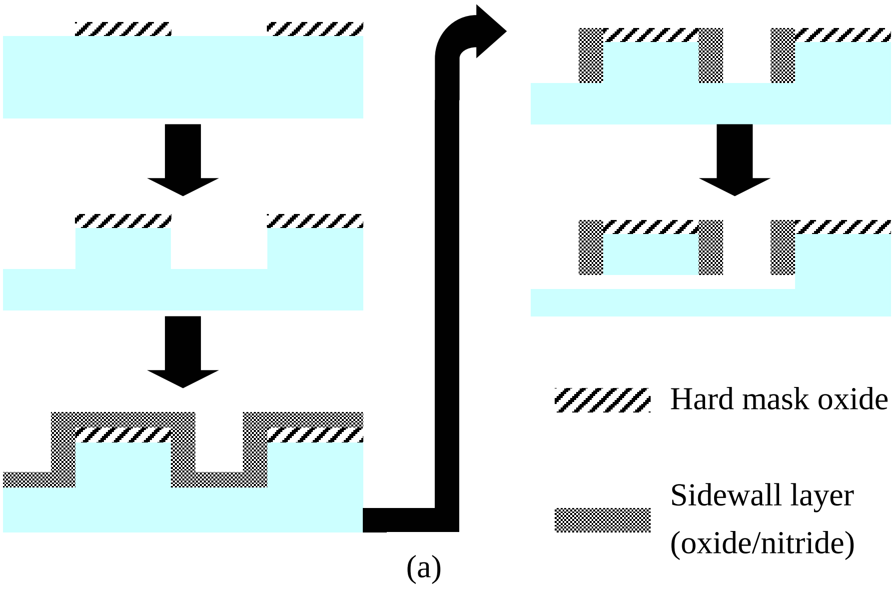
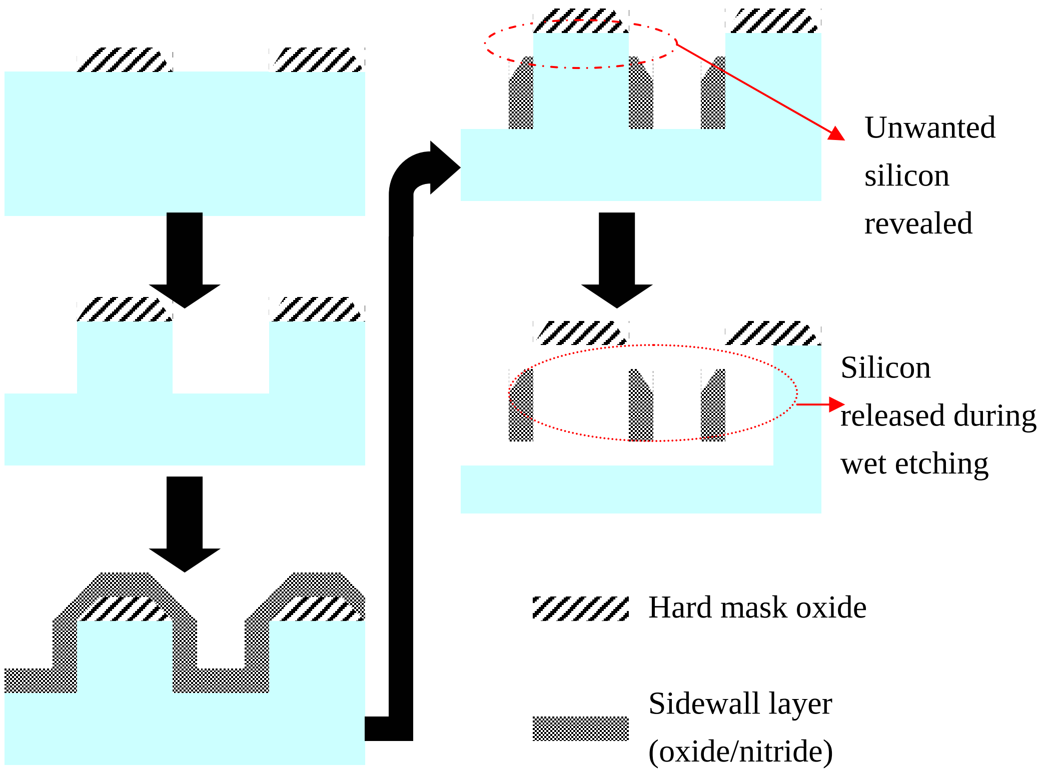


Fig 3-11 <111> silicon fabrication in (a) the ideal case (b) real case with corner bombardment



(b)

Fig 3-11 <111> silicon fabrication in (a) the ideal case (b) real case with corner bombardment (continued)

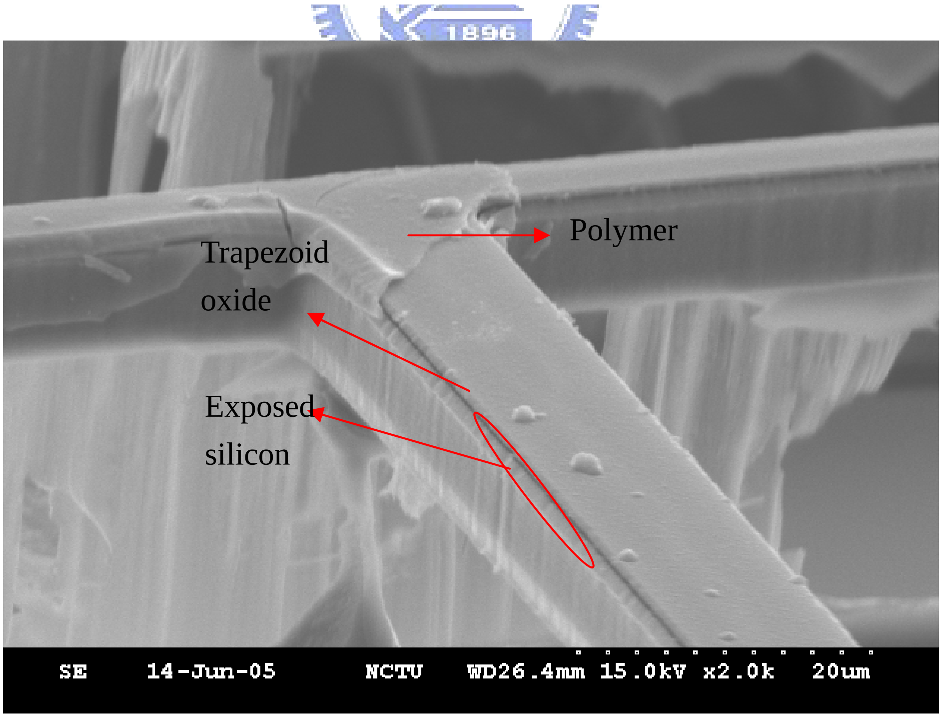


Fig 3-12 SEM photograph of the trapezoidal oxide and exposed silicon in the corner

3-5-3 Third run

To solve the corner attack problem, corner protection using thermal oxide was proposed [24]. Because the top corner has higher growth rate due to its large arriving angle, and the oxide around the corner is thicker. Therefore, the thick corner oxide can withstand the RIE processes longer. The corner silicon may not be exposed to etchant during releasing. However, the high temperature during thermal oxidation will ruin the photo detector.

Therefore, an isotropic dry releasing process (supported by NARC) was used to replace the TMAH wet etching process in the third run. This process is similar to SCREAM process [25]. A passivation polymer layer is first deposited by C_4F_8 after the second ICP-RIE process, as shown in Fig 3-13(a). Next, the top and bottom polymer layers are removed by vertical polymer etching (Fig 3-13(b)). Finally, the isotropic dry releasing is performed with a high flow SF_6 etching, as shown in Fig 3-13(c).

The SEM photograph of the first test run of this process is shown in Fig 3-14(a), in which, all the sacrificial structures have been removed except for the central part. Longer releasing time was used for the second test run and all the structures are released successfully, as shown in Fig 3-14(b).

Compared to the original wet etching process, the dry releasing process results in rough bottom structures and imprecise device thickness, as shown in Fig 3-16. Nevertheless, the requirements on the quality and step coverage of the sidewall passivation films are not as strict as those in wet etching process.

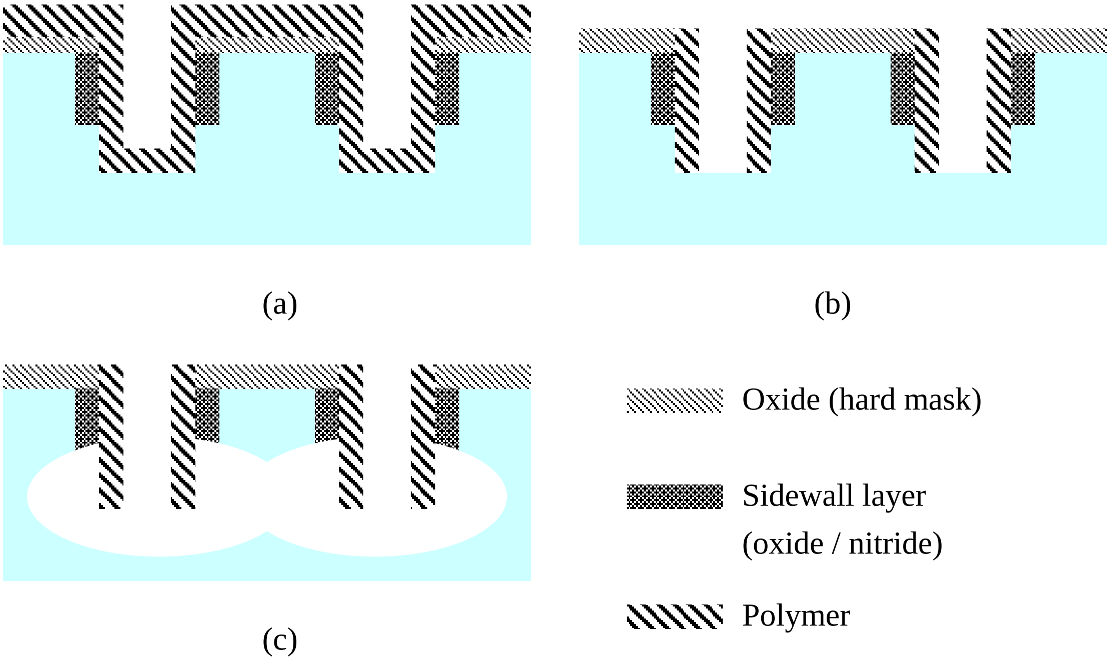
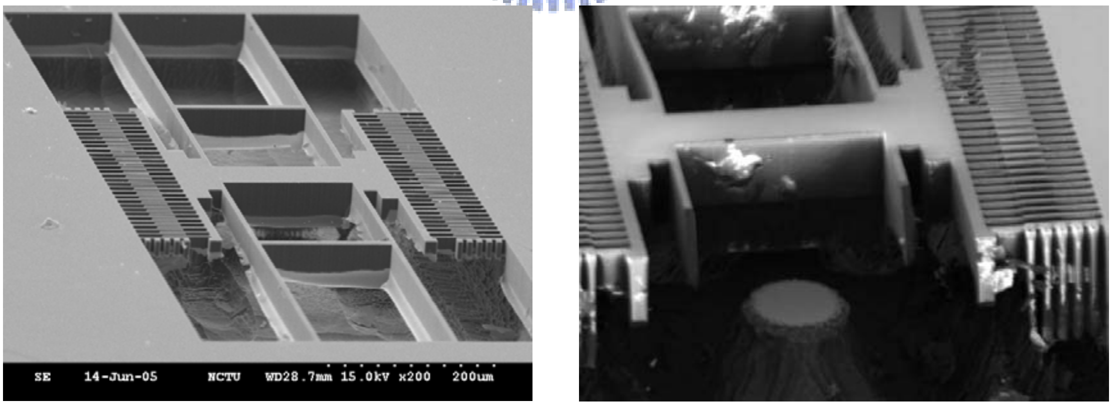


Fig 3-13 Isotropic dry releasing process (a) polymer deposition (b) bottom polymer removal (c) SF_6 dry releasing



(a) (b)

Fig 3-14 SEM photograph of (a) the first test run (b) the second test run

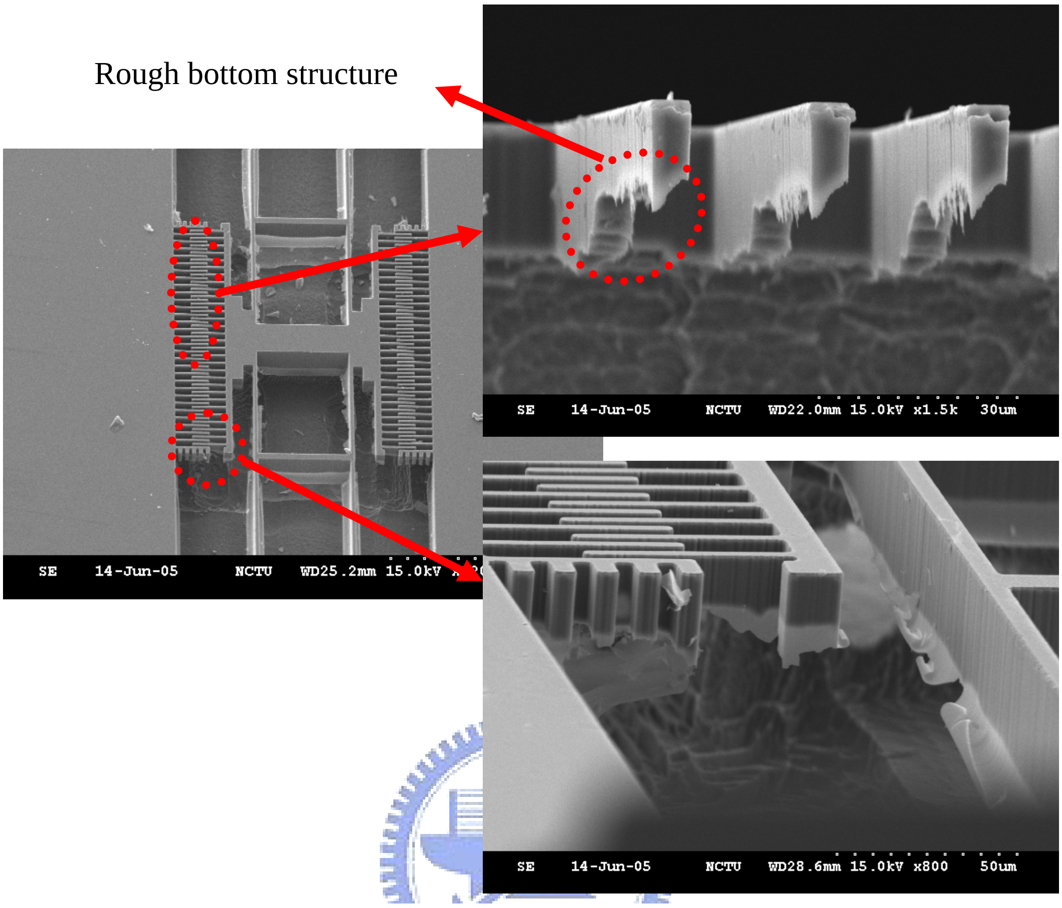


Fig 3-15 SEM photograph of the bottom structure after releasing

3-6 Summary

The comb actuator of the reflection type spot scan system using MUMPs technology has been successfully fabricated.

The integrated process for the absorption type device was proposed. The problems encountered in the process were discussed. A dry releasing process was used to solve the corner attack problems. However, the dry releasing process resulted in rough bottom structure.