# Random-Dopant-Induced Variability in Nano-CMOS Devices and Digital Circuits

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***Abstract*—The impact of the number and position of discrete dopants on device characteristics is crucial in determining the transient behavior of nanoscale circuits. An experimentally validated coupled device-circuit simulation was conducted to investigate the discrete-dopant-induced timing-characteristic fluctuations in 16-nm-gate CMOS circuits. The random-doping effect may induce 18.9% gate-capacitance fluctuation, affecting the intrinsic device gate delay and circuit timing. For a 16-nm-gate CMOS inverter, 0.036-, 0.021-, 0.105-, and 0.108-ps fluctuations in rise time, fall time, low-to-high delay time, and high-to-low delay time are found. The timing fluctuations of NAND and NOR circuits are increased, as the number of transistors increased. Because of the same number of transistors in circuits, the timing fluctuation of NAND and NOR are expected to be similar. However, due to the different function and device operation status of circuit, the timing fluctuation is quite different. The function- and circuit-topology-dependent characteristic fluctuations caused by random nature of discrete dopants are found. This paper provides an insight into random-dopant-induced intrinsic timing fluctuations, which can, in turn, be used to optimize nanoscale MOS field-effect-transistor circuits.**

***Index Terms*—Characteristic fluctuation, modeling and simulation, nanoscale digital IC, random-dopant effect, timing.**

## I. Introduction

SILICON-BASED devices are scaled down continually to increase density and speed. The gate lengths of scaled MOSFETs are under 30 nm in 45-nm-node high-performance circuit design [1]. Devices with sub-10-nm gate lengths have recently been studied [2], [3]. For state-of-the-art nanoscale circuits and systems, the local device variation and uncertainty of signal-propagation time have become crucial in the variation of system timing and the determination of clock speed. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, variations in the process parameters, and other factors are known as indispensable components of the circuit-design procedure [4]–[10].

Manuscript received March 11, 2009; revised April 24, 2009. First published June 26, 2009; current version published July 22, 2009. This work was supported in part by Taiwan National Science Council (NSC) under Contracts NSC-97-2221-E-009-154-MY2 and NSC-96-2221-E-009-210 and in part by a 2007–2009 grant from Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan. The review of this paper was arranged by Editor V. R. Rao.

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Digital Object Identifier 10.1109/TED.2009.2022692

The intrinsic device parameter fluctuations that result from line edge roughness [11], [12], the granularity of the polysilicon gate [13]–[15], and random discrete dopant [15]–[42] effects have substantially affected the device characteristics. With device scaling, various randomness effects resulting from the random nature of manufacturing process have induced significant fluctuations of electrical characteristics in nanoscale MOSFETs. The number of dopants is on the order of tens in the depletion region in a nanoscale MOSFET, whose influence on device characteristic is large enough to be distinct. Various random-dopant effects have been recently studied in both experimental and theoretical approaches [15]–[42]. Fluctuations of characteristics are caused not only by a variation in an average doping density, which is associated with a fluctuation in the number of impurities, but also with a particular random distribution of impurities in the channel region. The randomness of the dopant position and number in device makes the fluctuation of device characteristics difficult to model and mitigate. Diverse approaches have recently been presented to investigate fluctuation-related issues in semiconductor devices [15]–[35] and circuits [36]–[42]. However, less attention has been paid to timing-characteristic fluctuations of active devices caused by random dopants. Additionally, the randomness of dopant positions in devices makes the fluctuation of the gate capacitance of a device nonlinear and difficult to model using present compact models [34].

Thus, this paper presents a large-scale statistically sound coupled device-circuit simulation approach to analyze the random-dopant effect in nanoscale CMOS circuits, concurrently capturing the fluctuations associated with the number and the positions of discrete dopants. Based on the statistically generated large-scale doping profiles, device simulation is performed by solving a set of 3-D drift-diffusion equations with quantum corrections by the density-gradient method [43]–[51], which is performed using a parallel-computing system [52]–[54]. The density-gradient approximation [43]–[51] is used to smooth the singularities of the Coulomb potential [25], [26], [31] by properly introducing the related quantum–mechanical effects. To pursue high accuracy of timing fluctuation [55], a coupled device-circuit simulation [42], [55]–[58] with discrete dopant distribution is conducted to examine the associated timing behavior of the circuit. The characteristic fluctuation of the device was validated with reference to the experimentally measured data [32] to ensure the best accuracy. The results of this paper elucidate the random-dopant fluctuations in circuit timing and discuss the function- and circuit-topology-dependent characteristic fluctuations.

This paper is organized as follows. Section II introduces the simulation technique for studying the effect of random dopant in nanoscale devices and circuits. Section III studies the characteristic fluctuations in 16-nm devices and circuits. Finally, conclusions are drawn and future work is suggested.

## II. Nano-MOSFET Circuit and Simulation Technique

The nominal channel doping concentration of the explored device is $1.48 \times 10^{18}$ cm$^{-3}$. They have a 16-nm gate, a gate oxide thickness of 1.2 nm, and a work function of 4.4 eV. The source/drain and background doping concentrations are $1.1 \times 10^{20}$ and $1 \times 10^{15}$ cm$^{-3}$, respectively. To study the effect of random fluctuations in the number and position of discrete dopants in the channel region, 758 dopants are randomly generated in an $(80\ \text{nm})^3$ cube, yielding an equivalent doping concentration of $1.48 \times 10^{18}$ cm$^{-3}$, as shown in Fig. 1(a). The $(80\ \text{nm})^3$ cube is then partitioned into 125 subcubes of $(16\ \text{nm})^3$. The number of dopants varies from 0 to 14, and the average number is 6, as shown in Fig. 1(b)–(d). These 125 subcubes are then mapped into the channel region of the device for the 3-D "atomistic" device simulation including discrete dopants, as shown in Fig. 1(e). The device is simulated by solving a set of 3-D density-gradient equations coupled with Poisson equation and electron–hole current continuity equations [28]–[30], [32], [33], [42], [49]. A step function $N_A$ is used to define the concentration and positions of dopants

$$N_A = \sum_{i=0}^{k} N_A^{\text{dopant}} \cdot [H(x - x_l, y - y_l, z - z_l) - H(x - x_u, y - y_u, z - z_u)] \quad (1)$$

where

$$H(x, y, z) = \begin{cases} 1, & x \geq 0, y \geq 0, z \geq 0 \\ 0, & \text{otherwise.} \end{cases} \quad (2)$$

$(x_l, y_l, z_l)$ and $(x_u, y_u, z_u)$ are the lower and upper coordinates of a discrete dopant, respectively; $k$ is the number of dopants in the device channel; $N_A^{\text{dopant}}$ is the associated doping concentration for a dopant within a box. Then, $N_A$ is substituted into the source of the Poisson equation and solved with the electron–hole current continuity equations and density-gradient quantum-correction equations simultaneously for device characteristics. In "atomistic" device simulation, the resolution of individual charges within a conventional drift-diffusion simulation using a fine mesh creates problems associated with singularities in the Coulomb potential [25], [26], [31]. The potential becomes too steep with fine mesh, and therefore, the majority carriers are unphysically trapped by ionized impurities, and the mobile carrier density is reduced [25], [26], [31]. Thus, the density-gradient approximation is used to handle discrete charges by properly introducing the related quantum–mechanical effects [43]–[51]. Note that 3-D Monte Carlo device simulations with *ab initio* impurities scattering [27], [35] will provide more rich physical insights and accurate estimations.

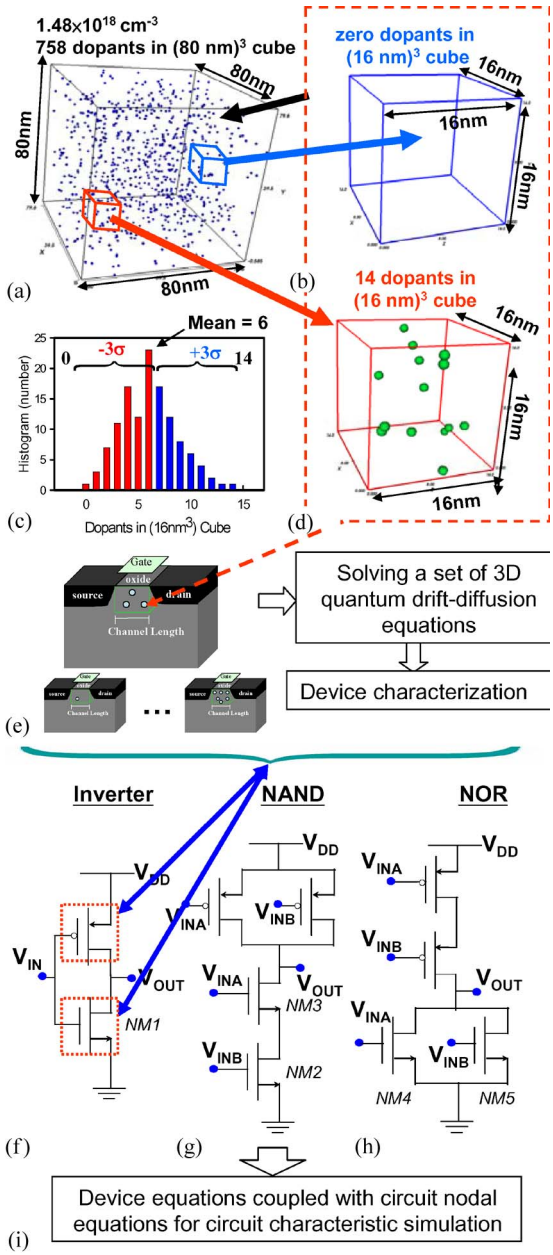


Fig. 1. (a) Discrete dopants randomly distributed in the $(80\ \text{nm})^3$ cube with the average concentration of $1.48 \times 10^{18}$ cm$^{-3}$. (b)–(d) There will be 758 dopants within the cube, but dopants may vary from 0 to 14 (the average number is 6) within its 125 subcubes of $(16\ \text{nm})^3$. The 125 subcubes are equivalently mapped into the channel region for dopant-position/number-sensitive device simulation. The inverter, NAND, and NOR circuits, displayed in (f)–(h), are used as test circuits to study the fluctuation of timing characteristics. (e)–(i) Inverter, NAND, and NOR gates are used as test circuits for timing-variation estimation. A coupled device-circuit simulation is then conducted for circuit characteristic fluctuations.

The inverter, NAND, and NOR circuits, shown in Fig. 1(f)–(h), are used as test circuits to study the fluctuation of timing characteristics. Similarly, 125 cases of PMOSFETs with discrete dopants are generated, as shown in Fig. 1(a)–(d). Then, 125 pairs of NMOSFETs and PMOSFETs are randomly selected and used to study the circuit characteristic fluctuations. To compare fairly the NMOSFET- and PMOSFET-induced

characteristic fluctuation and eliminate the effect of transistor size on fluctuation, the dimensions of the PMOSFET were the same as those of the NMOSFET, and the absolute value of the nominal threshold voltages for both the NMOSFET and PMOSFET were both 140 mV. All statistically generated devices and circuits with discrete dopants, shown in Fig. 1, are incorporated into the large-scale 3-D coupled device-circuit simulation which is performed using a parallel-computing system [52]–[54]. In estimating circuit characteristics, since no well-established compact model of ultrasmall nanoscale devices is available, to capture the discrete-dopant-position-induced fluctuations, a device-circuit coupled simulation approach [42], [55]–[58]. The nodal equations of the test circuit are formulated and then directly coupled to the device transport equations (in the form of a large matrix that contains both circuit and device equations), which are solved simultaneously to obtain the circuit characteristics. The device characteristics, such as potential and current density, obtained by device simulation are input in the circuit simulation through circuit nodal equations. The effect of discrete dopants in the transistor on circuit characteristics is thus properly estimated. The mobility model used in the device simulation, according to Mathiessen's rule [59], [60], can be expressed as

$$\frac{1}{\mu} = \frac{D}{\mu_{\text{surf\_aps}}} + \frac{D}{\mu_{\text{surf\_rs}}} + \frac{1}{\mu_{\text{bulk}}} \tag{3}$$

where $D = \exp(x/l_{\text{crit}})$, $x$ is the distance from the interface, and $l_{\text{crit}}$ is a fitting parameter. The mobility consists of three parts: 1) the surface contribution due to acoustic phonon scattering $\mu_{\text{surf\_aps}} = (B/\mathbf{E}) + [C(N_i/N_0)^{\tau}/\mathbf{E}^{1/3}(T/T_0)^{K}]$, where $N_i = N_A + N_D$, $T_0 = 300$ K, $\mathbf{E}$ is the transverse electric field normal to the interface of semiconductor and insulator, $B$ and $C$ are parameters which are based on physically derived quantities, $N_0$ and $\tau$ are fitting parameters, $T$ is lattice temperature, and $K$ is the temperature dependence of the probability of surface phonon scattering; 2) the contribution attributed to surface roughness scattering is $\mu_{\text{surf\_rs}} = ((E/E_{\text{ref}})^{\chi}/\delta + E^3/\eta)^{-1}$, where $\chi = A + \alpha(n+p)N_{\text{ref}}/(N_i + N_1)^{\nu}$, $\mathbf{E}_{\text{ref}} = 1$ V/cm is a reference electric field to ensure a unitless numerator in $\mu_{\text{surf\_rs}}$, $N_{\text{ref}} = 1$ cm$^{-3}$ is a reference doping concentration to cancel the unit of the term raised to the power $v$ in the denominator of $\chi$, $\delta$ is a constant that depends on the details of the technology, such as oxide growth conditions, $N_1 = 1$ cm$^{-3}$, $A$, $\alpha$, and $\eta$ are fitting parameters; and 3) the bulk mobility is $\mu_{\text{bulk}} = \mu_L(T/T_0)^{-\xi}$, where $\mu_L$ is the mobility due to bulk phonon scattering and $\xi$ is a fitting parameter. The mobility model is quantified with our device measurements for the best accuracy, and the characteristic fluctuation has been validated with the experimentally measured dc baseband data [32].

## III. Results and Discussion

In this section, the device characteristic fluctuations consisting of threshold voltage ($V_{\text{th}}$) and gate capacitance ($C_g$) are investigated. Then, the fluctuation of timing characteristics of the circuit is investigated.

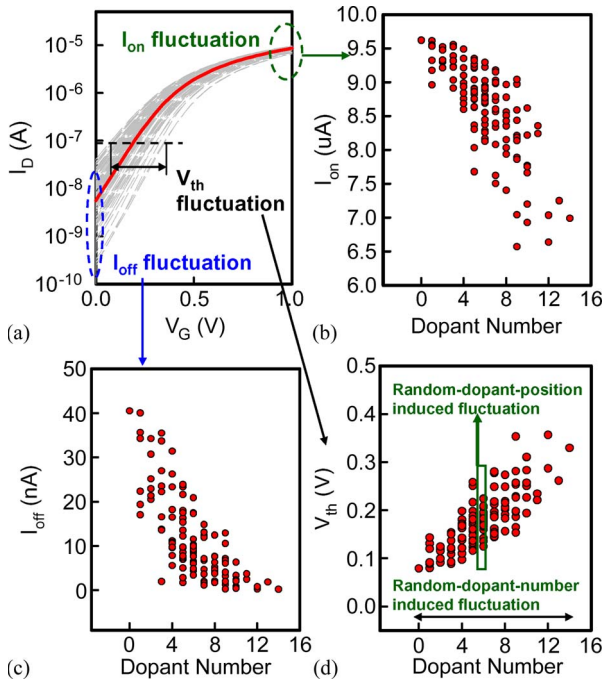


Fig. 2. DC characteristic fluctuations of (a) $I_D$–$V_G$ characteristics, (b) $I_{\text{on}}$, (c) $I_{\text{off}}$, and (d) $V_{\text{th}}$ of the discrete-dopant-fluctuated 16-nm-gate planar MOSFET. The solid line in $I_D$–$V_G$ curves shows the capacitance of the nominal case, and the dashed lines are random-dopant-fluctuated devices.

### A. Intrinsic DC Characteristic Fluctuation in Nanoscale MOSFET

Fig. 2(a) shows the $I_D$–$V_G$ characteristics of 16-nm planar NMOSFETs with discrete dopant fluctuations; the solid line represents the nominal case (continuously doped channel with a doping concentration of $1.48 \times 10^{18}$ cm$^{-3}$), and the dashed lines are random-dopant-fluctuated devices. The ON-state currents ($I_{\text{on}}$), OFF-state currents ($I_{\text{off}}$), and threshold voltage ($V_{\text{th}}$) are shown in Fig. 2(b)–(d), respectively. Each line and symbol shown in Fig. 2(a)–(d) indicates the dc characteristic for each device. The threshold voltage is determined from a current criterion that the drain current larger than $10^{-7}$ (W/L) A. From the random-dopant-number point of view, the equivalent channel doping concentration increases when the dopant number increases; this substantially alters the threshold voltage and the ON- and OFF-state currents. Additionally, the random dopant position induced different fluctuations of characteristics in spite of the same number of dopants, as marked in inset shown in Fig. 2(d). Furthermore, the magnitude of the spread characteristics increases as the number of dopants increases. The detailed physical mechanism is described somewhere else [28]–[30], [32], [33]. Notably, the maximum and minimum $V_{\text{th}}$ are achieved for this specific set of 125 randomized channels and would be different (larger range) if a larger number of samples were taken. Note that, comparing with a simulation of 1000 discrete dopant devices, the difference of the obtained $\sigma V_{\text{th}}$ for the set of 125 randomized channels is about 3 mV.

### B. Gate Capacitance Fluctuation in Nanoscale MOSFET

Fig. 3(a) shows the capacitance–voltage ($C$–$V$) characteristics of the 16-nm planar NMOSFETs with discrete dopant

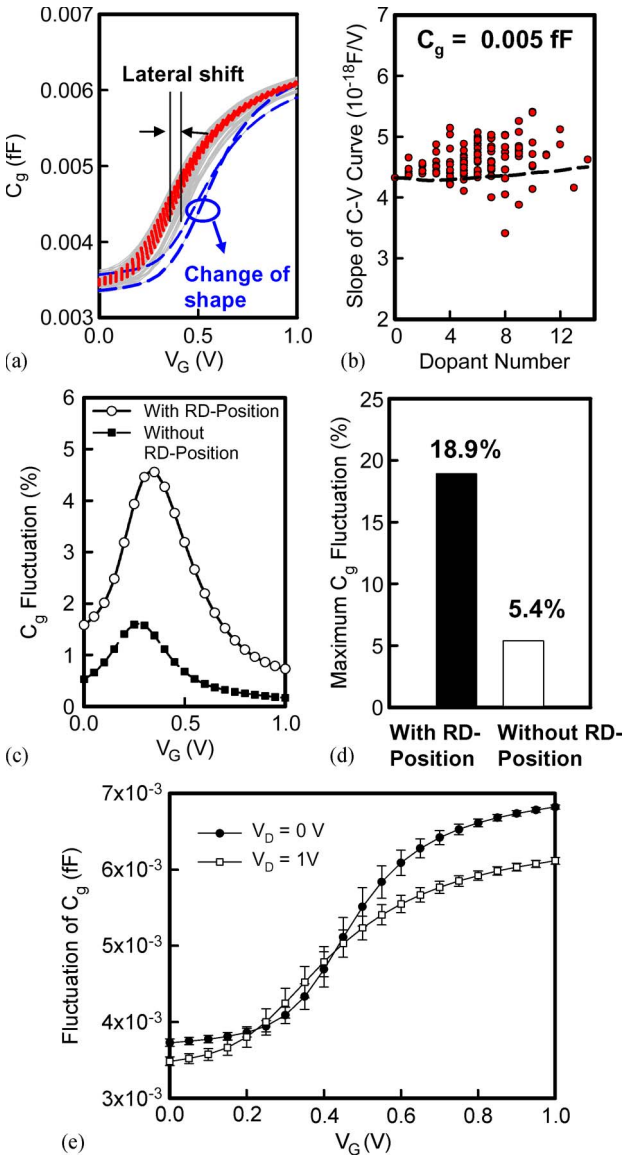


Fig. 3. (a) Capacitance–voltage curves and (b) slope of the $C$–$V$ curves for cases with and without taking random-dopant-position effect into consideration, where the solid line shows the nominal case and the dashed lines are random-dopant-fluctuated devices. The solid and dot lines in (a) are the cases with and without random-dopant-position effect, respectively. The dashed line in (b) indicates the cases without random-dopant-position effect, and the symbols are the cases with random-dopant-position effect. (c) Normalized gate-capacitance fluctuation and (d) maximum gate-capacitance fluctuation are calculated. (e) $C_g$ fluctuation with different drain bias.

fluctuations. The solid and dot lines are the cases with and without random-dopant-position effect, respectively. The cases without random-dopant-position effect are simulated by changing their channel doping concentration continuously from $1.0 \times 10^{15}$ to $3.4 \times 10^{18}$ cm$^{-3}$. Fig. 3(b) shows the slope of the $C$–$V$ curves, in which the gate capacitance $(C_g)$ is fixed to $5 \times 10^{-18}$ F.

The dash line indicates the cases without random-dopant-position effect, and the symbols are the cases with random-dopant-position effect. The slope of $C$–$V$ curve for the cases without random-dopant-position effect is nearly independent of doping concentration, which implies the lateral shift of the

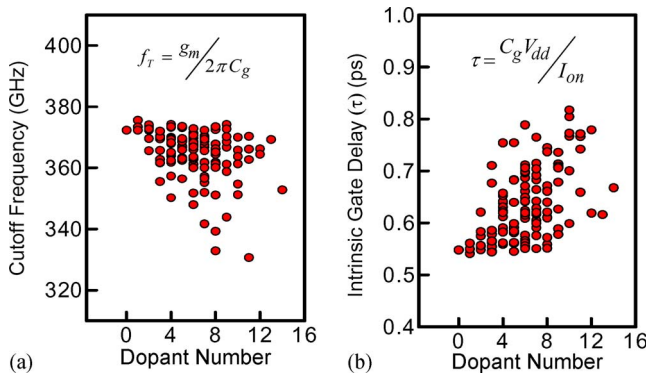


Fig. 4. (a) Cutoff frequency and (b) intrinsic gate delay of transistor for the discrete-dopant-fluctuated 16-nm-gate planar MOSFETs.

$C$–$V$ curves. The lateral shift of gate capacitance is a result of the variation of $V_{\rm th}$ and can be described by the corresponding parameters in compact model. However, the slopes of $C$–$V$ curves are substantially altered as the random-dopant-position effect is taken into consideration, as shown in Fig. 3(b). The variation of the slopes of $C$–$V$ curves indicates the change of shape of $C$–$V$ curves, as shown in Fig. 3(a). The variation of $C$–$V$ curves is a result of the randomness of the dopant position in the depletion region of the channel and, therefore, is hard to describe in the current compact model [34]. To the best of the authors' knowledge, the fluctuation in the gate capacitance $(C_g)$ has not yet been modeled, and a coupled device-circuit simulation must be performed to estimate its impact on circuit characteristics. Fig. 3(c) shows the normalized $C_g$ fluctuation as a function of gate bias. The $C_g$ fluctuations are normalized by the nominal $C_g$. The result implies the importance of random-dopant-position effect. Moreover, the device under subthreshold operation suffers from the largest fluctuation. For the device with high gate voltage $(V_G)$, the screening effect of the inversion layer of the device screens the variation of electrostatic potential and decreases the fluctuation of gate capacitance [34]. The normalized maximum variations of $C_g$ are summarized as shown in Fig. 3(d), in which the normalized maximum variation of $C_g$ is about 18.9%. The neglect of the random-dopant-position effect may underestimate the $C_g$ fluctuation by a factor of five. Fig. 3(e) shows the $C_g$ fluctuation with different drain bias. The device with high drain bias has a less gate capacitance fluctuation due to the pinch-off effect and smaller gate-to-drain capacitance at a high drain bias.

The intrinsic cutoff frequency and intrinsic gate delay of the studied device are shown in Fig. 4(a) and (b), respectively. The insets give the definition of these characteristics. As the number of dopants in the device channel is increased, the depletion width decreases and the gate capacitance increases. With the decreasing transconductance $(g_m)$ and increasing gate capacitance, the intrinsic cutoff frequency of the device decreases with increasing dopant number. The intrinsic gate delay is increased as the dopant number increases due to the decreasing ON-state current and increasing gate capacitance. The fluctuations of cutoff frequency and intrinsic gate delay are 8.2 GHz and 0.069 ps, respectively, and the magnitude of fluctuation is increased as the dopant number increases. The

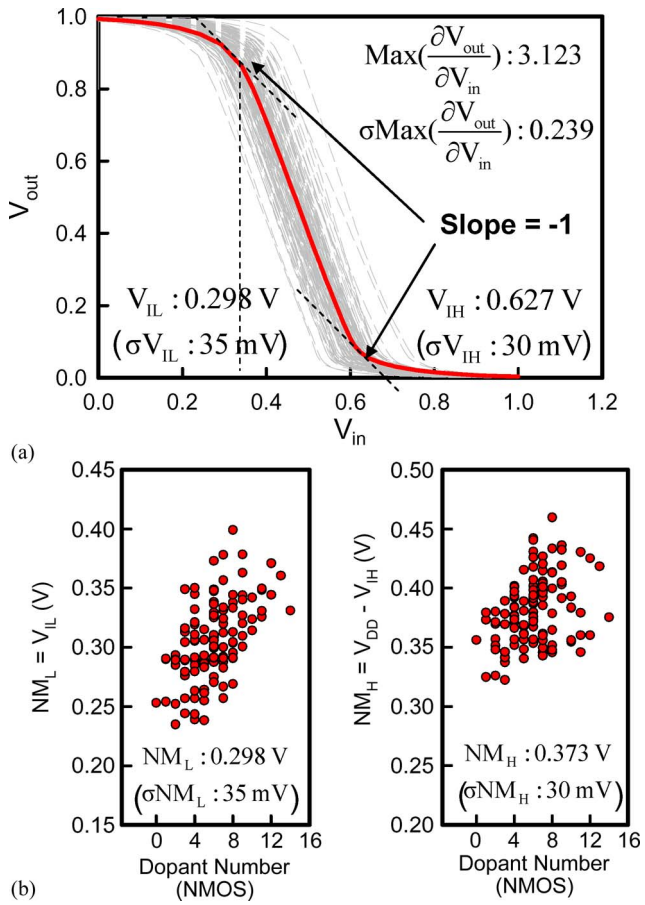


Fig. 5. (a) Voltage transfer curves for the studied 16-nm-gate planar MOSFET circuit. (b) Noise margins, $\mathrm{NM}_L$ and $\mathrm{NM}_H$, as a function of the dopant number in the NMOSFET and PMOSFET.

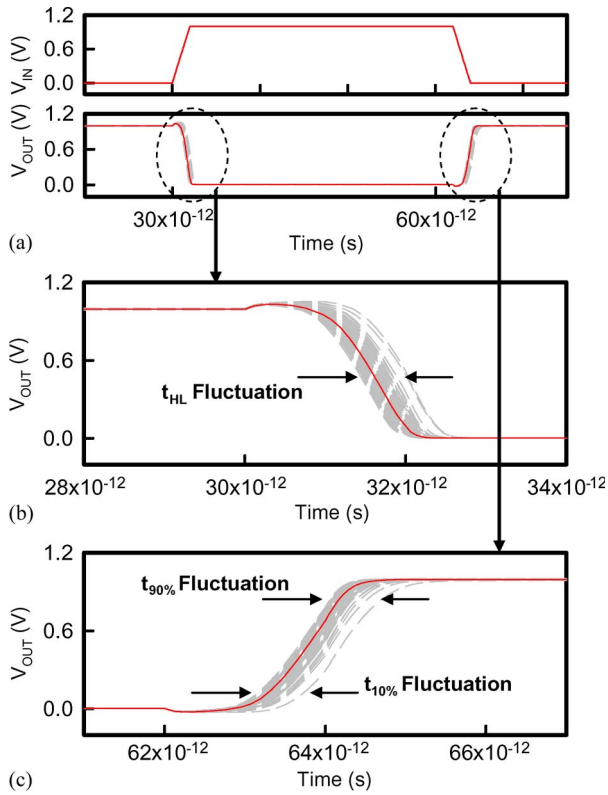


Fig. 6. (a) Input and output signals for the studied discrete-dopant-fluctuated 16-nm-gate inverter circuit. The zoom-in plots of the (b) fall and (c) rise transitions, where the fluctuation of the $t_{\mathrm{HL}}$, $t_{90\%}$, and $t_{10\%}$ are defined.

discrete dopant effect not only causes fluctuations in $V_{\mathrm{th}}$ and current but also affects the gate capacitance of the transistor. Therefore, the transistor's intrinsic gate capacitance is used as a load capacitance in circuit, and the intrinsic timing fluctuations that are induced by discrete dopants are focused.

### C. Device-Variability-Induced Fluctuations in Circuits

Fig. 5(a) shows the voltage transfer curves for the 16-nm-gate CMOS inverters with discrete dopants. Two points on the voltage transfer curve determine the noise margins of the inverter. These are the maximum permitted logic "0" at the input $V_{\mathrm{IL}}$ and the minimum permitted logic "1" at the input $V_{\mathrm{IH}}$. The two points on the voltage transfer curve are defined as those values of $V_{\mathrm{in}}$ where the incremental gain is unity; the slope is $-1$ V/V. The nominal value and fluctuations of $V_{\mathrm{IL}}$ and $V_{\mathrm{IH}}$ are shown in the insets of Fig. 5(a). $\sigma V_{\mathrm{IL}}$ exceeds $V_{\mathrm{IH}}$ because $\sigma V_{\mathrm{th}}$ of NMOSFETs exceeds that of PMOSFETs. The maximum slope of the voltage transfer curve indicates the maximum voltage gain of the inverter. The 7% of normalized voltage gain fluctuation of the inverter is therefore estimated, as shown in the inset of Fig. 5(a). Fig. 5(b) shows the noise margins for the logic "0" and "1," $\mathrm{NM}_H$ and $\mathrm{NM}_L$, respectively, as a function of the dopant number. The $\mathrm{NM}_H$ and $\mathrm{NM}_L$ are defined in insets. The $\mathrm{NM}_L$ is increased with the increasing dopant number in the NMOSFET due to the increased $V_{\mathrm{th}}$ of the device. For the $\mathrm{NM}_H$, as numbers of dopant in the PMOSFET increase, the increased $V_{\mathrm{th}}$ of the device may decrease the $V_{\mathrm{IH}}$ of voltage transfer curve and, thus, increase the $\mathrm{NM}_H$. We notice that, even for cases with the same number of dopants within the device channel, their noise margins are still quite different due to the different distribution of random dopants. The noise margins of the inverter circuit increase as the dopant number increases; however, the fluctuations of the noise margins are also increased due to the more sources of fluctuation in the device channel region.

Fig. 6 shows the input and output transition characteristics for the inverter circuit. Fig. 6(a) shows the input and output signals; the solid line represents the nominal case (continuously doped channel with a channel doping concentration of $1.48 \times 10^{18}$ cm$^{-3}$), and the dashed lines represent cases with discrete dopant fluctuations. The rise time $(t_r)$, fall time $(t_f)$, and hold time of the input signal are 2, 2, and 30 ps, respectively. Fig. 6(b) and (c) shows the zoom-in plots of the falling and rising transitions, respectively. The term $t_r$ is the time required for the output voltage $(V_{\mathrm{OUT}})$ to rise from 10% of the logic "1" level to 90% of the logic "1," and the $t_f$ denotes the time required for the output voltage to fall from 90% of the logic "1" level to 10% of the logic "1" level. The low-to-high delay time $(t_{\mathrm{LH}})$ and high-to-low delay time $(t_{\mathrm{HL}})$ are defined as the difference between the times of the 50% points of the input and output signals during the rising and falling of the output signal, respectively. For the high-to-low transition, the NMOSFET is

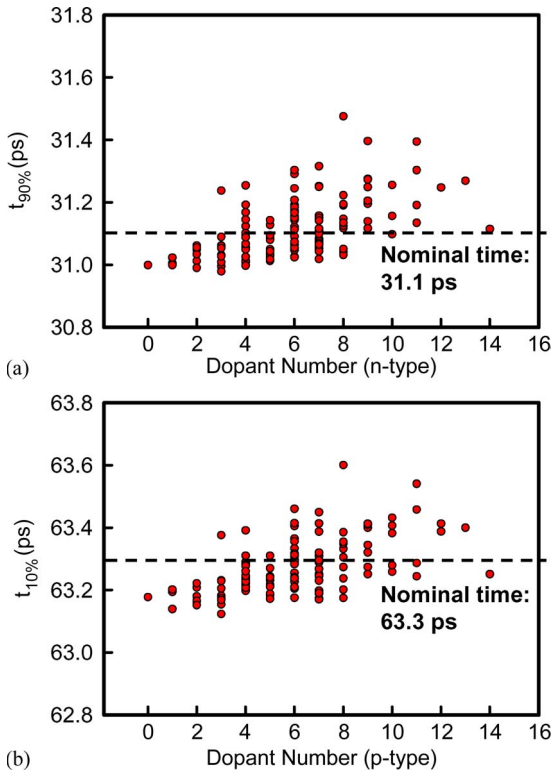


Fig. 7. Fluctuations of (a) fall and (b) rise signal transition points as a function of dopant number in n- and p-type MOSFETs for the discrete-dopant-fluctuated inverter circuits, in which the transition points are defined in Fig. 5(b) and (c), respectively.

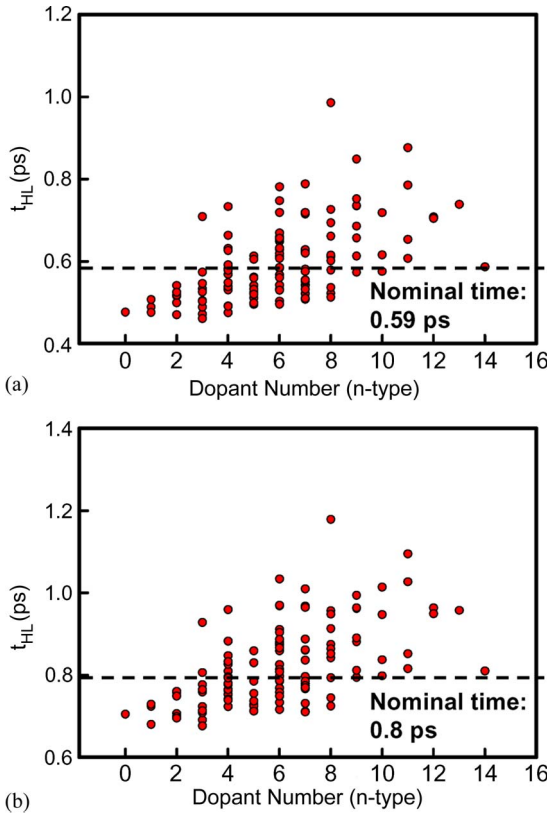


Fig. 8. Fluctuations of (a) high-to-low and (b) low-to-high delay times as a function of dopant number in n- and p-type MOSFETs for the discrete-dopant-fluctuated inverter circuits.

on and starts to discharge load capacitance, causing the output signal to transit from logic "1" to logic "0." Similarly, for the low-to-high transition characteristics, the PMOSFET is turned on and starts to charge the load capacitance, causing the output voltage to transit from logic "0" to logic "1." The 90% $(t_{90\%})$ and 10% $(t_{10\%})$ of the logic "1" level are defined as starting points for the high-to-low and low-to-high transitions and are shown in Fig. 7(a) and (b), respectively. During the high-to-low signal transition, the output signal falls as the NMOSFETs is turned on. Therefore, the fluctuation of the starting points for high-to-low signal transition is determined by the $\sigma V_{\rm th}$ of the NMOSFET. With the increasing number of dopants in NMOSFET, the increased $V_{\rm th}$ delays the starting point of signal transition $(t_{90\%})$ and increases the high-to-low delay time $(t_{\rm HL})$, as shown in Fig. 8(a). Similarly, the starting point of low-to-high transition (the time of 10% of the logic "1" level) is influenced by $V_{\rm th}$ of the PMOSFET and increased as numbers of dopants in the PMOSFET, as shown in Fig. 7(b). Fig. 8(a) and (b) shows the high-to-low delay time $(t_{\rm HL})$ and low-to-high delay time $(t_{\rm LH})$ for the inverter circuits with discrete dopants, respectively. Since the delay time is dependent on the start of the signal transition, the $t_{\rm HL}$ and $t_{\rm LH}$ are increased as the channel dopant number increases. Notably, even with the same dopant number inside the channel, the delay time can still vary significantly. Take the cases of six dopants inside the NMOSFETs as an example; the maximum $t_{\rm HL}$ difference is about 0.3 ps, where the nominal $t_{\rm HL}$ is 0.59 ps. We refer to this effect as discrete-dopant-position-induced fluctuation. The magnitude of discrete-dopant-position-induced fluctuations

TABLE I
SUMMARIZED TRANSITION-TIME VARIATION FOR THE 16-nm-GATE INVERTER CIRCUITS (* NORMALIZED BY THE NOMINAL VALUE)

| (unit: ps) | $t_r$ | $t_f$ | $t_{LH}$ | $t_{HL}$ |
|---|---|---|---|---|
| Nominal | 1.021 | 0.897 | 0.800 | 0.590 |
| Fluctuation | 0.036 | 0.021 | 0.105 | 0.108 |
| Normalized Fluctuation* | 3.5 % | 2.4 % | 13.2 % | 18.3 % |
| Normalized Maximum Fluctuation* | 23.2 % | 12.3 % | 73.5 % | 101.8 % |

increases as the dopant number increases because of the increasing number of fluctuation sources (dopants). Table I summarized the normalized timing-characteristic fluctuations (the standard deviation/nominal value $\times$ 100%). For the 16-nm-gate CMOS inverter, as the number of discrete dopants varies from 0 to 14, fluctuations of $t_r$, $t_f$, $t_{\rm LH}$, and $t_{\rm HL}$ of 0.036, 0.021, 0.105, and 0.108 ps, respectively, may occur. The normalized fluctuation for $t_r$, $t_f$, $t_{\rm LH}$, and $t_{\rm HL}$ are 3.5%, 2.4%, 13.2%, and 18.3%, respectively. The rise/fall-time fluctuations depend on the charge/discharge capability of the PMOSFETs/NMOSFETs. Therefore, $\sigma t_r$ exceeds the $\sigma t_f$ because the driving capability of PMOSFETs is weaker than that of NMOSFETs in the given device dimensions scenario. The device with larger driving capability requires less time to charge and discharge a given load capacitance and so exhibits less fall-time fluctuations. The delay-time fluctuations dominate the timing characteristics. The normalized maximum fluctuations (the maximum variation of time/nominal value $\times$ 100%) of the high-to-low and low-to-high delay times are about 101.8% and 73.5%. Notably, the

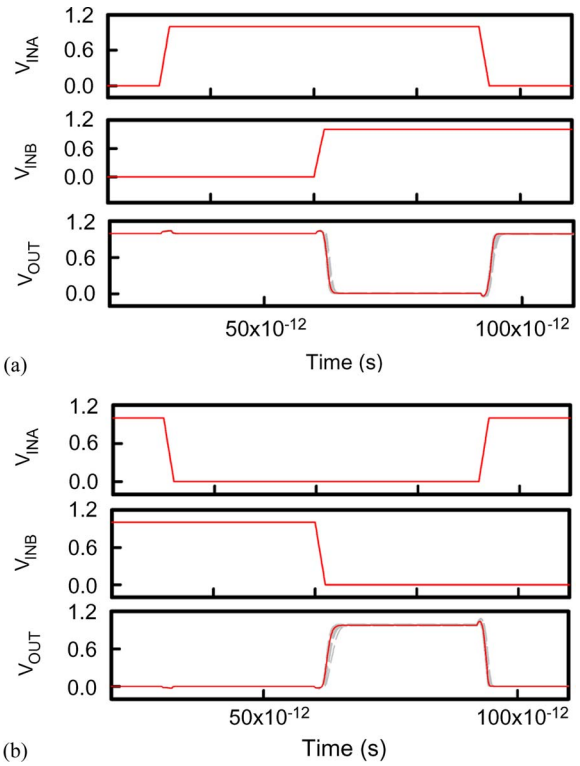


Fig. 9. Input and output signals for the studied discrete-dopant-fluctuated 16-nm-gate (a) two-input NAND and (b) two-input NOR circuits.

maximum and minimum delays associated with this specific set of 125 randomized channels would vary such that their range would increase, as the number of samples increased. For the high-to-low signal transition of the output signal, the delay time is dominated by the starting points of the signal transition and then controlled by the ON/OFF-state of the NMOSFETs in the inverter circuit. Therefore, the fluctuation of the threshold voltage of the NMOSFETs substantially affects the high-to-low delay-time characteristic. Similarly, the low-to-high delay-time fluctuation is strongly influenced by the $\sigma V_{\rm th}$ of PMOSFETs. $\sigma t_{\rm HL}$ exceeds $\sigma t_{\rm LH}$ because the $\sigma V_{\rm th}$ of NMOSFETs exceeds that of PMOSFETs. Notably, the rise- and fall-time fluctuations generally may not be as important as the delay-time fluctuation in circuit timing; however, their maximum variations can exceed 0.237 and 0.110 ps, respectively, which exceed the delay-time fluctuation and should therefore be considered in statistical timing analysis in circuit and system design. Moreover, fluctuations in the rise and fall times can be added to the delay time and increasing the delay-time fluctuations.

Fig. 9(a) and (b) shows the input and output transition characteristics for the two-input NAND, and the two-input NOR circuits, respectively. The solid line represents the nominal case (continuously doped channel with a channel doping concentration of $1.48 \times 10^{18}$ cm$^{-3}$), and the dashed lines represent cases with discrete dopant fluctuations. The timing characteristics are summarized in Table II. As expected, the timing fluctuations of NAND and NOR circuits are increased as the number of transistors is increased. The fluctuation of timing characteristics may suffer from the increase of fluctuation sources in circuit. It is thus reasonable to infer that the NAND

TABLE II
SUMMARIZED TRANSITION-TIME VARIATION FOR THE 16-nm-GATE NAND AND NOR CIRCUITS (* NORMALIZED BY THE NOMINAL VALUE)

| (unit: ps) | $t_r$ | $t_f$ | $t_{LH}$ | $t_{HL}$ |
|---|---|---|---|---|
| NAND | | | | |
| Nominal | 1.248 | 1.197 | 0.987 | 1.254 |
| Fluctuation | 0.070 | 0.056 | 0.107 | 0.129 |
| NOR | | | | |
| Nominal | 1.762 | 0.993 | 1.616 | 0.761 |
| Fluctuation | 0.133 | 0.030 | 0.169 | 0.111 |

and NOR circuits may exhibit larger timing fluctuations than the inverter circuit. In addition, they may have similar timing fluctuations due to the same number of transistors in the circuit. However, the obtained results show that the $\sigma t_r$ and $\sigma t_f$ for the NAND circuit are 0.53 and 1.87 times larger than that of the NOR circuit. The different characteristic of timing fluctuation is resulted from the different operation status of the device with different input signal. For the fall-time transition characteristics of NAND and NOR circuits, their output signal transitions are determined by the devices $NM2$ and $NM4$ in Fig. 1(g) and (h), respectively. The $NM2$ and $NM4$ are operated in the linear and saturation regions, respectively. As aforementioned, the device operated in the saturation region exhibits a better discharge capability to reduce the timing fluctuations. Therefore, the $\sigma t_f$ of the NAND circuit exceeds that of the NOR due to the different operation status of transistors. Moreover, for the NMOSFETs in series ($NM2$ and $NM3$ in the NAND circuit), the $NM2$ may inherit the fluctuations resulted from $NM3$, such as the current fluctuation and intrinsic resistance fluctuation to influence the operation of $NM2$. Similarly, we can infer that $\sigma t_r$ of the NOR circuit is larger than that of the NAND circuit. The fluctuation of timing characteristics is influenced by the different input signal in circuit. In addition, the transistors in series are found to accumulate fluctuations and increase the fluctuations of circuits. Additionally, we can expect that the timing fluctuation can be reduced by the use of shunt transistors. The effect of the shunt transistor is similar to the increase of the device width of the most fluctuation-sensitive element in the circuits. The function- and circuit-topology-dependent characteristic fluctuations resulted from the random nature of the discrete dopants is, for the first time, briefly discussed and worth to be explored for future digital-circuit applications in nano-CMOS era.

## IV. CONCLUSION

In this paper, a 3-D "atomistic" coupled device-circuit simulation approach was adopted to investigate the random-dopant-induced timing-characteristic fluctuations in nanoscale CMOS inverter circuits, concurrently capturing the discrete-dopant-number- and discrete-dopant-position-induced fluctuations. The discrete-dopant-induced fluctuations of the gate capacitance, cutoff frequency, and intrinsic gate delay are investigated. The experimentally calibrated simulation technique predicted that the discrete-dopant-fluctuated 16-nm CMOS inverter circuit may exhibit 0.036-, 0.021-, 0.105-, and 0.108-ps fluctuations in the rise time, fall time, low-to-high

delay time, and high-to-low delay time, respectively. The delay-time fluctuations dominate the timing characteristics. The normalized maximum fluctuations of the high-to-low and low-to-high delay times are about 101.8% and 73.5%. However, the maximum variations of rise- and fall-time fluctuations can exceed 0.237 and 0.110 ps, respectively, which exceed the delay-time fluctuation and should therefore be considered in statistical timing analysis in circuit and system design. For the NAND and NOR circuits, the timing fluctuation is further increased with increasing number of transistors in circuit. Generally, circuits with the same transistors may have a similar variation of characteristics due to the same fluctuation sources. However, due to the device-operation status and circuit topology of circuits, the characteristic fluctuations in NAND and NOR are different. The function- and circuit-topology-dependent characteristic fluctuations resulted from random nature of discrete dopants are discussed. The transistors in series may accumulate fluctuations and increase the fluctuations of circuits. It is considered that links should be established between circuit design and fundamental device technology to allow circuits and systems to accommodate the individual behavior of every transistor on a silicon chip. This paper provides an insight into random-dopant-induced timing-characteristic fluctuations, which may benefit the development of state-of-the-art digital circuits with robust timing characteristics.

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