Low-Threshold-Voltage MoN/HfAlO/SiON p-MOSFETs With 0.85-nm EOT

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***Abstract*—By using HfAlO as a capping layer on SiON, MoN/HfAlO/SiON p-MOSFETs show an effective work function of 5.1 eV, a low threshold voltage of −0.1 V, and a peak hole mobility of 80 $\mathrm{cm^2/(V \cdot s)}$ at small equivalent oxide thickness of 0.85 nm. These self-aligned and gate-first p-MOSFETs processes, with standard ion implantation and 1000 °C rapid thermal annealing, are fully compatible with current very large scale integration fabrication lines.**

***Index Terms*—Capping layer, HfAlO, MoN, p-MOSFETs.**

I. Introduction

HIGH-κ GATE dielectrics and metal gate have been used for CMOSFETs at the 45-nm nodes and beyond [1]–[16], to reduce the dc power consumption from the gate leakage current and continue the gate-oxide scaling. However, the undesired high threshold voltage (V_t) is still one of the major challenges for metal-gate/high-κ CMOSFETs, particularly for the desired low-cost gate-first process. The lack of highly effective work-function $(\phi_{m-\mathrm{eff}})$ gate metal in the periodic table [8]–[10] makes the p-MOSFET very challenging, which is even worse at small equivalent oxide thickness (EOT) by flatband voltage (V_{fb}) roll-off effect [6]–[9]. To address these issues, we previously reported the mechanism of V_{fb} roll-off that was related to interface reaction and interface diffusion of HfO_2 and Si channel during high-temperature rapid thermal annealing (RTA) [8]. To reduce the interface reaction, a low-temperature process was used that led to low V_t metal-gate/high-κ CMOSFET [8], [9] at 1.05–1.2-nm EOT. Alternatively, using Al_2O_3 [10], [11] or AlN [12] as capping layer or Al-content metal gate [13] has been used to modify the $\phi_{m-\mathrm{eff}}$ for p-MOSFET. However, the capping-layer method showed unwanted EOT degradation. In this letter, we report the use of MoN metal gate and thin HfAlO capping layer on SiON to achieve both low V_t and small EOT. After a 1000 °C RTA, the MoN/HfAlO/SiON p-MOSFETs show high $\phi_{m-\mathrm{eff}}$ of 5.1 eV, low V_t of −0.1 V, small 0.85-nm EOT, and good hole mobility of 80 $\mathrm{cm^2/(V \cdot s)}$.

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II. Experimental Procedure

The 12-in n-type Si wafers with 2×10^{15} $\mathrm{cm^{-3}}$ doping concentration and 4.29-eV substrate work function were used in these experiments. No well implant was used in this study. After standard clean, a thin SiON with 1.5- or 2.1-nm physical thickness was first grown on Si wafers. Then, HfAlO [3] of 1-nm thickness was deposited by physical vapor deposition (PVD) and postdeposition annealing at 500 °C in O_2 for 5 min. The composition ratio of Hf and Al in HfAlO is 1 : 1. After that, the metal gate was formed by depositing 50-nm MoN and 200-nm TaN by PVD and patterning. The p^+ source–drain regions were formed by 35-keV and 5×10^{15} $\mathrm{cm^{-2}}$ BF_2^+ implantation, followed by 1000 °C RTA activation for 1 s. Finally, the Al was deposited for source–drain and backside contacts. For comparison, MoN/SiON p-MOSFETs were also formed. The fabricated devices were characterized by capacitance–voltage $(C$–$V)$ and gate-current density–voltage $(J$–$V)$ measurements. The EOT and V_{fb} were extracted from the measured C–V data using a CVC simulator [17] that accounts for the quantum–mechanical effect.

III. Results and Discussion

Fig. 1(a) and (b) shows the C–V and J–V characteristics of MoN/HfAlO/1.5-nm SiON and control MoN/2.1-nm SiON capacitors, respectively. In addition to the positive V_{fb} using MoN gate on SiON, further ∼500-mV V_{fb} shift, smaller EOT of 0.85 nm, and low leakage current of 1.6×10^{-1} $\mathrm{A/cm^2}$ at 1 V of $V_g - V_{\mathrm{fb}}$ were measured for the MoN/HfAlO/1.5-nm SiON device than the control MoN/2.1-nm SiON sample. Such positive V_{fb} shift is needed for low V_t operation. The modulation of V_{fb} is attributed to the interdiffusion and reaction of SiON and HfAlO to form HfAlSiON layer after 1000 °C RTA [13]. The small EOT of 0.85 nm was obtained by considering quantum–mechanical effect [17]. The small EOT is due to optimized interdiffusion of HfAlO/SiON and slight diffusion of MoN gate after 1000 °C RTA, as shown from the SIMS measurements inserted in Fig. 1(b). The $\phi_{m-\mathrm{eff}}$ of 5.1 eV and oxide charge density of 4.5×10^{12} $\mathrm{cm^{-2}}$ were obtained from the V_{fb}–EOT plot inserted in Fig. 1(a). The large $\phi_{m-\mathrm{eff}}$ is suitable for p-MOS applications.

Fig. 2 shows the gate leakage current comparison of MoN/HfAlO/SiON, poly-Si/SiO_2, MoN/2.1-nm SiON, and TaN/HfLaO [8] gate stacks. The small 1.65-nm EOT in the MoN/2.1-nm SiON control device is also due to the slight MoN diffusion. The leakage current of 1.6×10^{-1} $\mathrm{A/cm^2}$ at 1 V above V_{fb} is approximately four orders of magnitude lower than that of SiO_2 at a 0.85-nm EOT. This low leakage

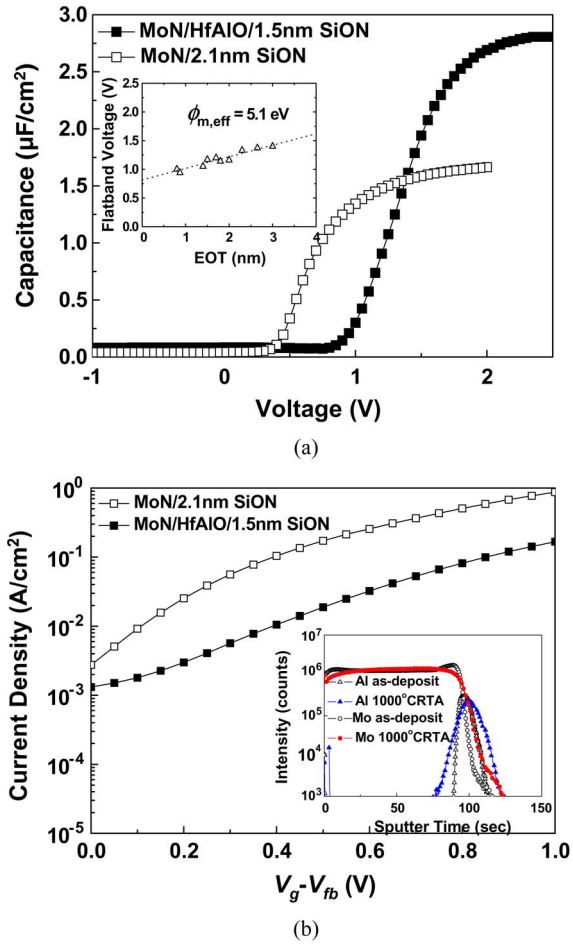

Fig. 1. (a) C–V and (b) J–V characteristics of the MoN/HfAlO/SiON and MoN/SiON p-MOS capacitors after a 1000 °C RTA. The inserted figure in (a) is a $V_{\rm fb}$–EOT plot with different HfAlO thickness on constant 1.5-nm SiON. The inserted figure in (b) is the SIMS profile before and after 1000 °C RTA.

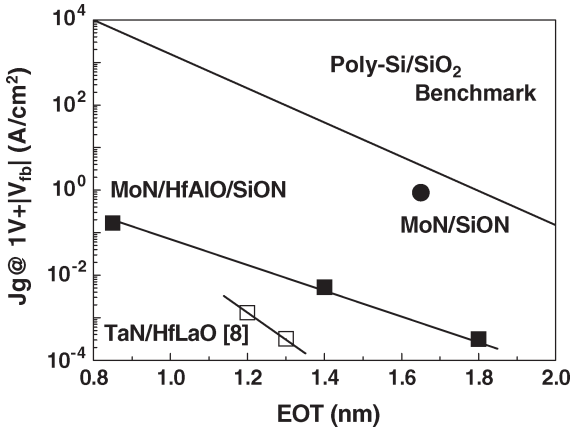

Fig. 2. Gate leakage current density comparison of MoN/HfAlO/SiON, poly-Si/SiO_2 stack, MoN/2.1-nm SiON, and TaN/HfLaO [8] gate stacks.

current is due to the high-κ HfAlO [3]. Thus, both high $\phi_{m-\rm eff}$ and low gate dielectric leakage current can be achieved in MoN/HfAlO/SiON MOS capacitors.

In Fig. 3(a) and (b), we show the I_d–V_d and I_d–V_g characteristics of the 0.85-nm EOT MoN/HfAlO/SiON p-MOSFETs. In addition to the well-behaved transistor characteristics, a small V_t of only -0.10 V was measured from the linear I_d–V_g

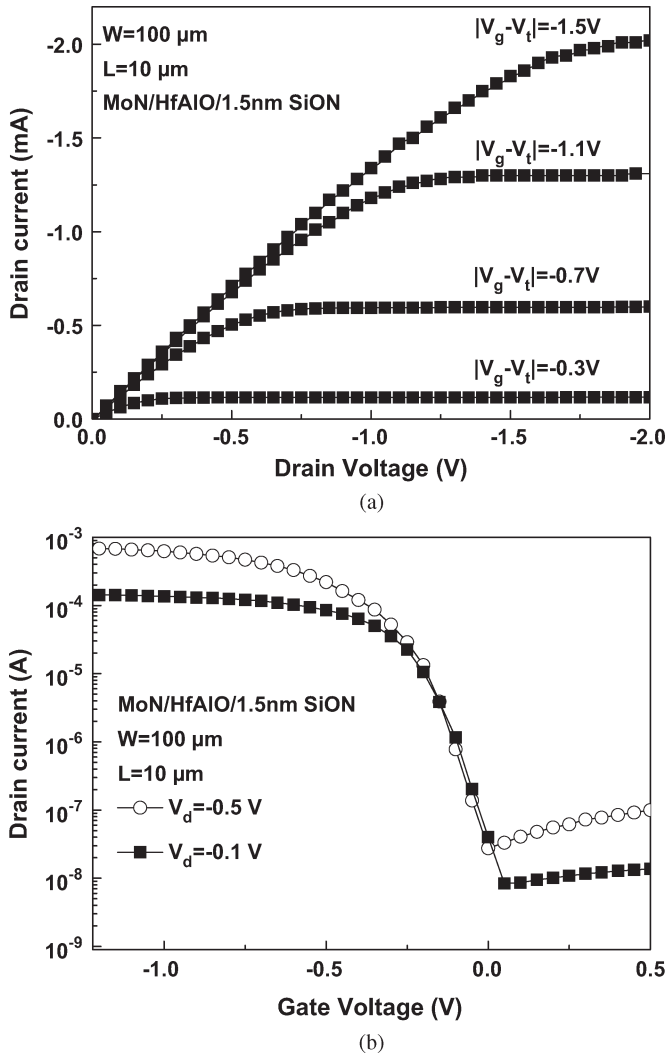

Fig. 3. (a) I_d–V_d and (b) I_d–V_g characteristics of the MoN/HfAlO/SiON p-MOSFETs.

plot—this is due to the high $\phi_{m-\rm eff}$ of 5.1 eV found from the C–V measurements. Such low V_t meets the lowest scalable value of 4 kT/q for MOSFET at the end of *International Technology Roadmap for Semiconductors* [16].

The hole mobility as a function of effective electric field for the MoN/HfAlO/SiON p-MOSFETs is shown in Fig. 4, where the data was extracted directly from the measured I_d–V_g curves at small V_d. For comparison, the MoN/2.1-nm SiON p-MOSFET with 1.65-nm EOT is also shown. Good peak hole mobility of 80 $\rm cm^2/(V \cdot s)$ and 56 $\rm cm^2/(V \cdot s)$ at 0.8 MV/cm were obtained, at a small EOT of 0.85 nm. A slightly degraded mobility is found compared with the MoN/2.1-nm SiON control sample. The reasonably good mobility is due to the optimized SiON between high-κ HfAlO and Si that is critical to prevent mobility degradation [14].

IV. Conclusion

We have demonstrated good performance in terms of V_t and mobility at 0.85-nm EOT for HfAlO-capped SiON p-MOSFETs with a high work-function MoN gate. The self-aligned and gate-first MoN/HfAlO/SiON p-MOSFETs

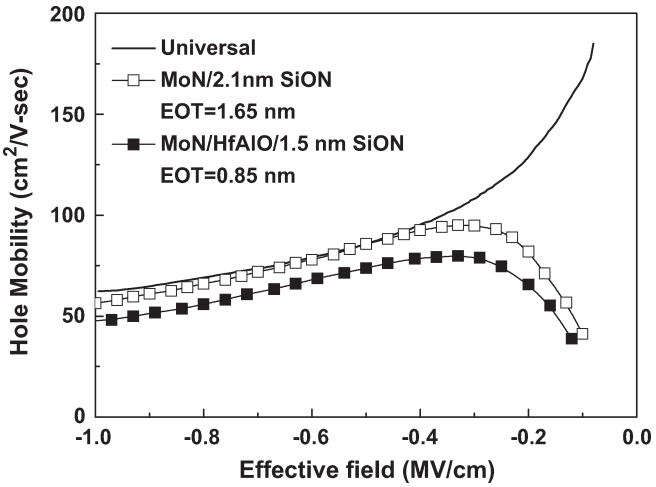

Fig. 4. Hole mobility versus effective electric field for the MoN/HfAlO/SiON p-MOSFETs.

have the advantages of simple high-temperature processing and compatibility with current very large scale integration lines.

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