Low-Threshold-Voltage TaN/Ir/LaTiO p-MOSFETs Incorporating Low-Temperature-Formed Shallow Junctions

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***Abstract*—We demonstrate a low threshold voltage (V_t) of -0.17 V and good hole mobility (54 $\mathrm{cm^2/V \cdot s}$ at 0.8 MV/cm) in TaN/Ir/LaTiO p-MOSFETs at an equivalent oxide thickness of only 0.66 nm. This was achieved by using Ni-induced solid-phase diffusion of SiO_2-covered Ni/Ga which reduced the high-κ dielectric interfacial reactions. This approach, along with its self-aligned and gate-first process, is compatible with current VLSI technology.**

***Index Terms*—LaTiO, low V_t, solid-phase diffusion (SPD).**

I. Introduction

A FUNDAMENTAL challenge for metal-gate/high-κ C-MOSFETs is the undesirable high threshold voltage (V_t) [1]–[14]. This is particularly difficult for high work-function p-MOS, since only Ir and Pt in the periodic table have the required high work function greater than the target 5.2 eV [7]–[13]. However, both Ir and Pt fail for p-MOS devices due to metal diffusion through the high-κ dielectric during the 1000 °C RTA necessary for ion-implanted source–drain activation [7]. Although thermal stability up to 1000 °C can be achieved by using an Ir_3Si gate on HfLaON [10], [11], this yields a V_t of only -0.1 V at 1.6-nm equivalent oxide thickness (EOT). Unfortunately, this value increases at a thinner EOT of 1.2 nm due to the roll-off of the flatband voltage (V_{fb}) as a result of reactions and interdiffusion at the high-κ/Si interface [12]. Although the interfacial reaction can be decreased by inserting a thin SiO_2 layer, this may not work when the EOT is scaled down to $\sim$0.7 nm. This is evident from the limited EOT scaling of 1.0–0.9 nm with downscaling the technology from 45- to 32-nm nodes [15], [16], which is much slower than the EOT proposed by the International Technology Roadmap for Semiconductors. Since the inevitable interfacial reactions follow an Arrhenius temperature dependence, low-temperature processing is essential. This has been verified by the low V_t in metal-gate/high-κ p-MOSFETs when a < 900 °C solid-phase diffusion (SPD) was used to form the ultrashallow junctions [12] and laser annealing of the laser-reflective-gated CMOS [13] with an EOT in the range of 1.05–1.2 nm. Here, we report a low V_t of -0.17 V in a high-κ p-MOSFET at a highly scaled 0.66-nm EOT. Such small EOT and low V_t were achieved by the combined effects of higher κ TiO_2-doped La_2O_3 (LaTiO), high work-function TaN/Ir electrode, and low-temperature Ni-induced SPD to lower the high-κ/Si interfacial reaction.

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II. Experimental Procedure

Standard n-type Si wafers were used in this letter. The self-aligned and gate-first TaN/Ir/LaTiO p-MOSFETs were made by first depositing TiO_2-doped La_2O_3 of $\sim$4.5-nm thickness on a Si substrate using PVD, followed by a postdeposition anneal (PDA). The TiO concentration is $\sim$25% as controlled by the calibrated thickness rate during LaTiO deposition. Then, 100-nm TaN/10-nm Ir was deposited on LaTiO to provide a high work-function gate. The thin thickness of Ir is to decrease the cost. After gate patterning, self-aligned 5-nm Ga and thin Ni were deposited. This was covered with an additional 100-nm SiO_2 and given a 500 °C to 800 °C RTA for the Ni-induced SPD. Detailed p^+/n junction characteristics, sheet resistivity, and SIMS dopant profile of the Ni-induced SPD, and the comparison of B^+ ion implantation can be found elsewhere [12]. The Ni-induced SPD is similar to dopant segregation technique [17], where both cases use the silicidation to drive in the impurities. However, the impurities in the dopant segregation technique [17] were delivered by ion implantation, while in the Ni-induced SPD, a PVD-deposited Ga was used to drive in the impurities. After etching the nonreacted metals, a thick Al contact metal was added on the source–drain regions. The fabricated transistors were characterized by capacitance–voltage (C–V) and current–voltage (I–V) measurements with a typical size of 10 μm $\times$ 100 μm.

III. Results and Discussion

Fig. 1(a) and (b) shows the C–V and J–V characteristics of TaN/Ir/LaTiO p-MOS capacitors fabricated at 650 °C RTA. A high capacitance density of 3.55 μF/cm^2 and a small hysteresis of 16 mV were measured, as well as the required large V_{fb} value, which is vital for low V_t in the p-MOSFETs. By using a quantum-mechanical C–V simulation, we estimated the EOT to be 0.66 nm. The leakage current at such a small EOT was

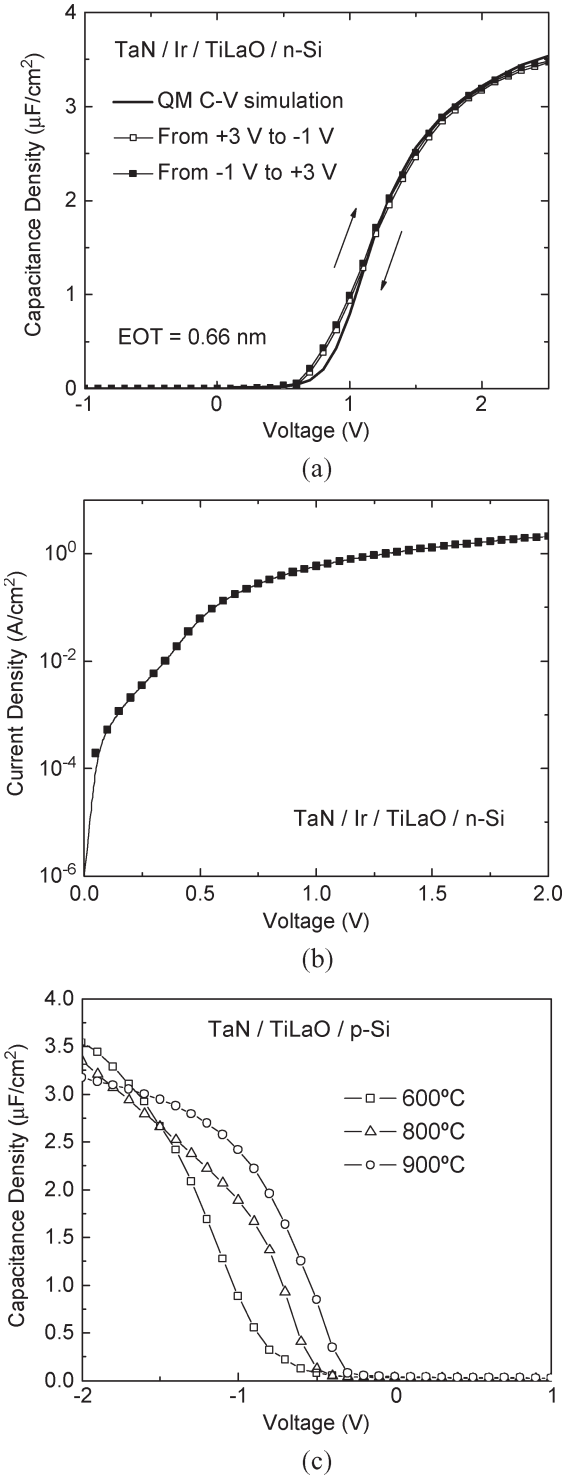

Fig. 1. (a) C–V, (b) J–V, and (c) PDA-temperature-dependent C–V characteristics. The capacitor size is 100 μm $\times$ 100 μm.

low, at 6.1×10^{-1} A/cm^2 at 1 V, which is due to the higher κ value of 29 in the TiLaO gate dielectric. Keeping the PDA temperature low is essential to obtain the proper $V_{\rm fb}$ and a high capacitance density. Fig. 1(c) shows the PDA temperature dependence. The increasing PDA temperature decreases the capacitance density and causes the intolerable $V_{\rm fb}$ roll-off. This is due to the increased interfacial reaction at higher PDA temperature reported previously [12], [13].

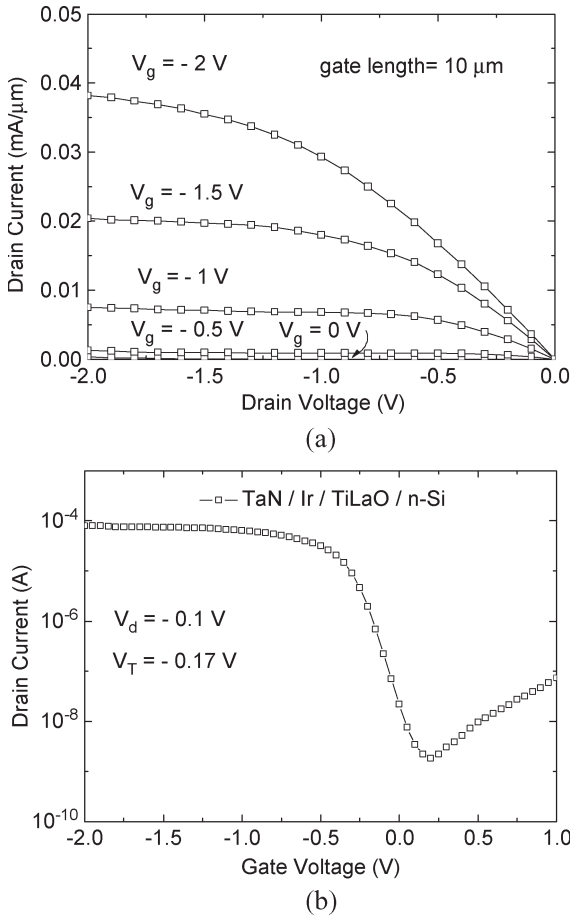

Fig. 2. (a) Drain (I_d–V_d) and (b) transfer (I_d–V_g) characteristics of SiO_2/Ni/Ga SPD-formed TaN/Ir/LaTiO p-MOSFETs.

To prevent the $V_{\rm fb}$ roll-off and limit the interfacial reactions, a low-temperature-formed source–drain shallow junction is required. Fig. 2(a) and (b) shows the I_d–V_d and I_d–V_g characteristics of TaN/Ir/LaTiO p-MOSFETs using low-temperature Ni-induced SPD source–drain junctions [12]. These devices show well-behaved transistor characteristics and a V_t of -0.17 V at a 0.66-nm EOT. The drive current is larger than the previous HfLaO p-MOSFET [12] due to the scaled EOT of only 0.66 nm. The low V_t in TaN/Ir/LaTiO p-MOSFET is due to the high work-function Ir electrode rather than fixed charge traps. This is because the TaN/LaTiO n-MOSFET had a small V_t of 0.l4 V (not shown) due to the negative $V_{\rm fb}$ nature of La_2O_3 [9], [10], [12]. Thus, both low V_t and small EOT p- and n-MOSFETs can be fabricated with a simpler process than poly-Si removal and gate-electrode refill process developed by Intel [15].

Fig. 3 shows the extracted hole mobility as a function of the gate electric field—the data being derived from the measured I_d–V_g characteristics. These data indicate a mobility of 54 cm^2/V $\cdot$ s at a gate electric field of 0.8 MV/cm. It is important to notice that the mobility decreased monotonically with decreasing EOT; electron mobility decreased from 250 cm^2/V $\cdot$ s at 1.3-nm EOT to only $\sim$125 cm^2/V $\cdot$ s at a 0.65-nm EOT [14]. The hole mobility at 0.66-nm EOT is still acceptable and confirms the importance of low-temperature processing.

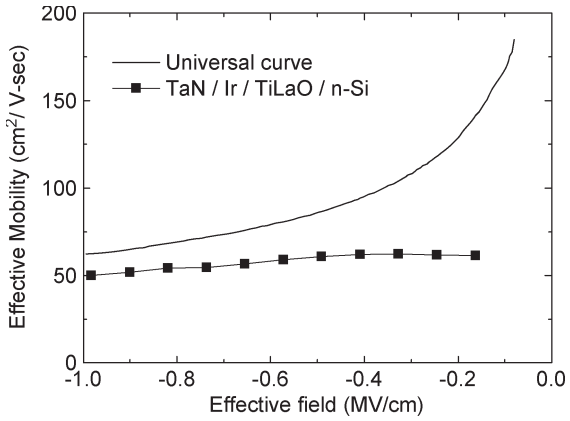

Fig. 3. Hole mobility as a function of effective electric field for SiO_2/Ni/Ga SPD-formed TaN/Ir/LaTiO p-MOSFETs.

IV. Conclusion

We have reported metal-gate/high-κ p-MOS devices which show a low V_t of -0.17 V and a good hole mobility of 54 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ at 0.8 MV/cm at a 0.66-nm EOT. Our shallow-junction TaN/Ir/LaTiO p-MOSFETs have the advantage of a self-aligned gate-first process compatible with current VLSI procedures.

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