IMPROVED HOT CARRIER RELIABILITY IN STRAINED-CHANNEL NMOSFETS WITH TEOS BUFFER LAYER

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INTRODUCTION

Since local tensile strain technology with SiN CESL has emerged as one of the most effective methods to boost the drive current in scaled NMOS devices [1,2], attention should now be focused on the device reliability associated with the strained devices, as the increased substrate current due to the strain and excess hydrogen incorporation from the deposited SiN layer could potentially aggravate the hot-electron effects. Although the physical mechanisms and characteristics of hot electron degradation have been extensively studied [3,4], there seems to be very few works investigating the impact of SiN capping layer and the associated deposition process on the hot carrier reliability of the strained devices. In this work, we investigate this issue and propose the incorporation of a thin TEOS buffer layer to improve the reliability performance.

DEVICE FABRICATION

NMOSFETs characterized in this study have a gate oxide thickness of 3 nm and a 150nm-thick n^+ poly-Si gate electrode. After the gate formation, most wafers were capped with a 300nm-thick LPCVD-SiN layer (denoted as SiN-capped split), while some wafers were deliberately skipped of the SiN deposition step to serve as the controls (denoted as the control split). For some SiN-capped wafers, a thin LPCVD-TEOS buffer layer (10 nm or 20nm) was capped prior to the SiN deposition (denoted as BL-10nmTEOS split and BL-20nmTEOS split, respectively). Yet in some SiN-capped wafers, the SiN layer was deliberately stripped after SiN deposition in order to evaluate the impact of SiN deposition process itself on the device performance (denoted as SiN-removal split).

RESULTS AND DISCUSSION

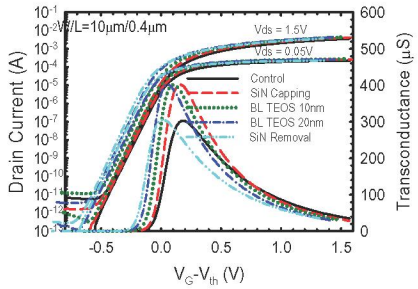

Fig. 1 Subthreshold characteristics and transconductance of NMOSFETs for all splits.

Fig. 1 shows the subthreshold characteristics and transconductance (Gm) of NMOSFETs for all splits, with channel length of 0.4 μm. It can be seen that all splits exhibit similar subthreshold slope. Significant increase in Gm over the control device is observed for all SiN-capped splits with or without the TEOS buffer layer, although similar enhancement is not observed in the SiN-removal split. These results clearly indicate that (a) the performance enhancement arises mainly from the tensile strain induced by the SiN layer, and (b) the insertion of 10nm or 20nm thick TEOS buffer layer does not compromise the device performance. To confirm these findings, output characteristics of NMOSFETs are shown and compared in Fig. 2. Drive current enhancement over the control sample is indeed clearly observed for the SiN-capped and BL-TEOS splits, while SiN-removal samples show negligible improvement.

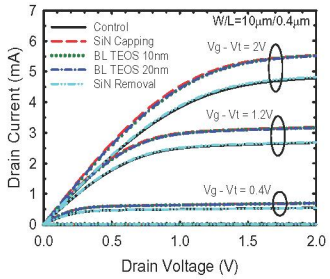

Fig. 2 Output characteristics of NMOSFETs for all splits.

Fig. 3 shows the percentage increase of Gm for the SiN-capped, BL-TEOS, and SiN-removal samples with respect to the control, as a function of channel length. We can see that the Gm enhancement reaches about 33% at a channel length of 0.4 μm in the SiN-capped and BL-TEOS samples. When the SiN capping layer is removed, such enhancement diminishes. These observations demonstrate that the Gm enhancement is truly due to the uniaxial tensile strain induced by the SiN capping which increases with decreasing channel length and the induced tensile strain is not jeopardized by the TEOS buffer layer used in this study. The capacitance-voltage *(C-V)* characteristics of the samples are shown in Fig. 4. Basically all splits show almost identical curves, indicating that the above observations are not caused by the thickness difference among gate oxides.

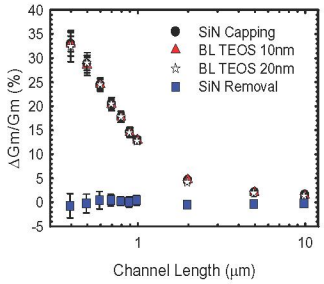

Fig. 3 Percentage increase of transconductance with respect to the control versus channel length. Each datum point represents the mean measurement value from six devices.

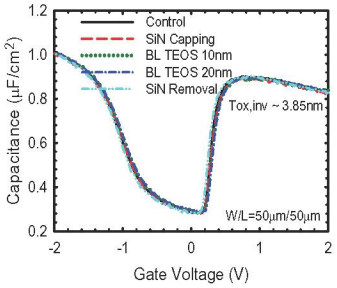

Fig. 4 Capacitance-Voltage *(C-V)* characteristics for all splits.

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IEEE 07CH37867 45th Annual International Reliability Physics Symposium, Phoenix, 2007

Next we focus our attention on the hot-carrier characterization with an aim to clarify whether the use of TEOS buffer layer is beneficial in improving the hot-carrier resistance. Fig. 5 shows substrate current (I_{sub}) versus gate voltage for all splits. It can be seen that the substrate current of the SiN-capped split and the BL-TEOS splits show similar trends, and are larger than that of the control counterpart. This result indicates that the channel strain plays an important role in affecting the generation of channel hot electrons. In addition, a thin 10nm or 20nm TEOS buffer layer does not seem to release the stress by the SiN capping because of the similar maximum substrate current ($I_{sub,max}$). This could be related to the bandgap narrowing effect induced by the channel strain as well as the increased mobility, both tend to enhance the impact ionization rate [5,6], and may potentially worsen the hot-electron degradation in the strained devices [7]. In Fig. 5, it is also interesting to note that I_{sub} in the SiN-removal sample is also larger than that in the control device. This could be explained by the additional hydrogen species by the SiN deposition process that tends to reduce the implant damage located near the drain region.

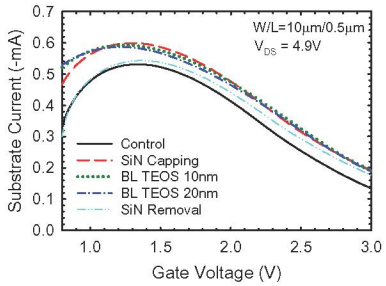

Fig. 5 Substrate current versus gate voltage with channel length of 0.5 μm.

The charge pumping currents of fresh devices with SiN capping are shown in Fig. 6. The sample without the buffer layer shows the smallest charge pumping current (Icp), while the BL-20nmTEOS sample exhibits the largest Icp among the three splits. These results indicate that the TEOS buffer layer can effectively block hydrogen diffusion into the channel region during the SiN deposition process. As a result, the hydrogen incorporation in the gate oxide and at the interface can be suppressed remarkably with the incorporation of TEOS buffer.

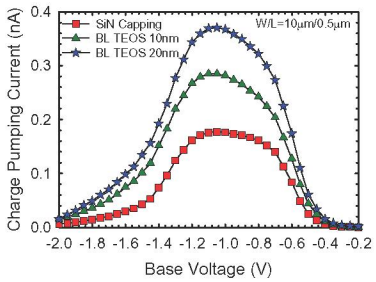

Fig. 6 Charge pumping current for the three SiN capping splits with channel width/length = 10μm /0.5μm.

Fig. 7 shows threshold voltage shift (ΔV_{th}) and increased interface state density (ΔN_{it}) as a function of the stress time. The SiN-capped sample depicts the worst degradation in terms of the largest shifts in these parameters, and the use of TEOS buffer layer apparently improves hot carrier degradation and the BL-20nmTEOS sample shows the smallest degradations. We suspect that the bandgap narrowing effect, the increased carrier mobility, and hydrogen species from the SiN capping process [8] are the primary culprits for the aggravated hot carrier degradations. It is noted that the device with SiN-removal depicts much severe degradation over the control devices and devices with TEOS buffer layers, even though the channel strain has been eliminated by the SiN removal. This phenomenon clearly indicates that the SiN deposition process itself may result in the enhanced damage effect in the short-channel devices. However, the use of TEOS buffer layer can effectively block the diffusion of hydrogen species into the channel region during SiN deposition. Although this results in increased N_{it} in the fresh devices (Fig. 6), significant reduction in broken Si-H bonds and thus less interface states are generated during subsequent stressing as compared with the SiN-capped samples. Consequently, both BL-TEOS splits show much improved resistance to the hot-carrier degradation than the SiN-capped split. The BL-20nmTEOS sample exhibits the best results due to effective suppression of hydrogen diffusion.

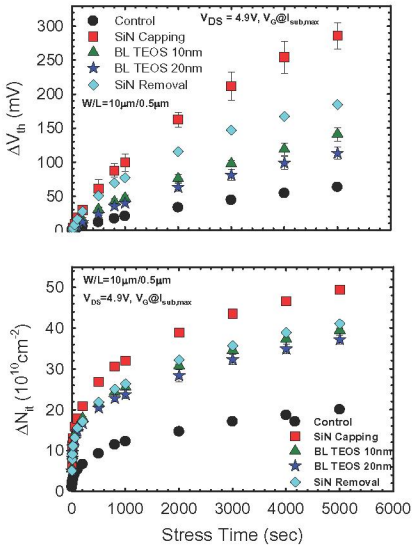

Fig. 7 Results of hot-electron stressing at V_{DS}=4.9V and maximum substrate current performed on all splits with channel width/length = 10μm /0.5μm. (a) Threshold voltage shift; (b) Interface state generation.

CONCLUSION

Both the presence of the SiN capping layer and the deposition process itself exert significant impacts on the device operation and the associated reliability characteristics. The accompanying bandgap narrowing, increased carrier mobility and hydrogen diffusion from the SiN capping process tend to worsen the hot-electron reliability. This work shows that, owing to the use of hydrogen-containing precursors, abundant hydrogen species is presumably incorporated in the oxide and may contribute to the hot-electron degradation, even if the SiN layer is removed later and the channel strain is relieved. Furthermore, by blocking the diffusion of hydrogen species, the devices with 20nm-thick TEOS buffer layer can effectively improve the hot-electron reliability without compromising the performance enhancement by the strain induced by the SiN capping. Optimization of both the thickness of buffer layer and SiN deposition process are thus essential to the implementation of the uniaxial strain in NMOS devices.

ACKNOWLEDGMENTS

This work was supported in part by the National Science Council of the Republic of China under contract No. NSC 95-2221-E-009-297.

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