國立交通大學

電信工程研究所

碩士論文

在鍺通道金氧半場效電晶體上製造閘極介電層二氧化鋯/鍺堆疊結構之研究

Investigation of ZrO_2/Ge Gate Stack Fabricated on Ge-Channel MOSFETs

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摘要

在這篇論文中，首先我們製造了以二氧化鋯為閘極介電層的鍺金氧半電容，再來我們使用了電性和物性分析來研究利用不同溫度的原子層化學沉積以及不同溫度的沉積後退火對鍺基板和二氧化鋯之間介面的影響。我們討論並使用電導方法(conductance method)來萃取介面缺陷電荷密度，也利用准靜態電容量測方法(quasi-static C-V)和貝格朗積分(Berglund integral)萃取出表面電位並探討能帶彎曲的有效程度。我們選擇 250 度的原子層化學沉積以及在 600 度的氮氣環境下進行一分鐘的沉積後退火做為我們製作元件的條件。

其次，我們成功的利用閘極後形成的製程(gate last process)做出了鍺金氧半場效電晶體。我們的 p^{+}/n 接面以及 p 型金氧半場效電晶體的開關比分別為 1.66x10^{4} 和 2.92x10^{3}，次臨界擺幅為 119 mV/dec。我們的 n^{+}/p 接面以及 n 型金氧半場效電晶體的開關比分別為 1.51x10^{5} 和 1.73x10^{4}，次臨界擺幅為 112.5 mV/dec。但是在介電層退火的過程中，我們的摻雜會向外擴散而造成有很大的源極/汲極串連阻抗。為了改善這個缺點，我們改變了製程的先後順序。

再來，我們利用閘極先形成的製程(gate first process)做出了鍺金氧半場效電晶體。們的 p^{+}/n 接面以及 p 型金氧半場效電晶體的開關比分別為 8.61x10^{4} 和 5.32x10^{3}，次臨界擺

幅為 125.8 mV/dec。我們的 n$^+$/p 接面以及 n 型金氧半場效電晶體的開關比分別為 1.66x10^4 和 3.02x10^3，次臨界擺幅為 130.5 mV/dec。

最後，我們比較閘極後形成的鍺金氧半場效電晶體和閘極先形成的鍺金氧半場效電晶體。由於摻雜活化是閘極先形成的製程中最後一個高溫的步驟，所以源極/汲極的串連阻抗被大大的降低。

Investigation of ZrO_2/Ge Gate Stack Fabricated on Ge-Channel MOSFETs

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ABSTRACT

In this thesis, firstly ZrO_2/Ge MOS capacitors are fabricated. ZrO_2 was deposited by atomic layer deposition (ALD) with different conditions such as deposition temperatures and post deposition annealing (PDA) temperatures. We electrically and physically analyze the ZrO_2/Ge MOS capacitors. Conductance method is discussed in detail and utilized to extract the density of interface state of the ZrO_2/Ge MOS capacitors. Also, by using quasi-static C-V curve and Berglund integral, we can estimate the band bending efficiency from the extracted surface potential. We choose ALD at 250°C and PDA at 600°C in N_2 ambient for one minute to be an optimized condition to fabricate the Ge MOSFETs.

Secondly, we successfully fabricate the Ge MOSFETs using a gate last scheme. The on/off ratio of our p^+/n junction and reaches 1.66×10^4 and 2.92×10^3, respectively and the subthreshold swing of p-MOSFET is 119 mV/dec. The on/off ratio of our n^+/p junction and n-MOSFET reaches 1.51×10^5 and 1.73×10^4, respectively and the subthreshold swing of n-MOSFET is 112.5 mV/dec. Even so, we find, however, there is a large source/drain series

resistance in our MOSFET due to the dopant out-diffusion during the high-κ dielectric annealing. In order to improve this drawback, we further change the fabrication from the gate last scheme to the gate first scheme.

Thirdly, we fabricate Ge MOSFETs using a gate first scheme. The on/off ratio of our p^+/n junction and p-MOSFET reaches 8.61×10^4 and 5.32×10^3, respectively and the corresponding subthreshold swing is 125.8 mV/dec. The on/off ratio of our n^+/p junction and n-MOSFET is 1.66×10^4 and 3.02×10^3, respectively while the subthreshold swing is 130.5 mV/dec.

Finally, comparison between the studied gate last and gate first MOSFETs is discussed in detail. The engineering findings of this study indicates that source/drain series resistance can be largely reduced due to more effective dopant activation caused by the last high temperature step in the gate first process.

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政庭學長，不管是實驗的設計、數據的分析及整理、半物、製程上或量測的問題，每次跟你討論都獲益良多，你也都會跟我一一解說，沒有你的幫助，實驗成果是不可能這麼豐富的。能跟你一起做實驗、一起幫 Lamigo 加油真的很開心，祝福你明年能夠順利畢業。哲偉學長，超常拿著蠢問題追著你，不管你怎麼忙也都不厭其煩地替我解惑，也常關心我的進度，希望以後還能有機會一起打球。信淵學長，你的 coding 神技真是令人歎為觀止，在 D_{it} 的萃取上謝謝你的幫忙跟指導，希望你元件能趕快做出來。謝謝宏基學長，因為有你，奈中的機台能夠順利破關，也祝你博士學位能早日破關。謝謝哲鎮、酷奇、小林學長，沒有你們的帶領，實驗沒辦法這麼快的上手，許多實驗上的小撇步，都讓我在實驗上順利不少。再來要感謝實驗室同學的陪伴，主元、邦聖、純敏、周洋平時互相討論研究問題，一起打嘴砲，讓我兩年的研究生生活充滿樂趣。崇浚、弘彬、晨揚、晉宇、俊翰，謝謝你們的幫忙，讓我在實驗的負擔上減輕不小，也祝福你們到時候都能準時畢業。

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Chapter 1

Introduction

1.1 General Background

In 1947, John Bardeen and Walter Brattain observed that when two gold point contacts were applied to germanium, the output signal's power is greater than the input ones. This was the first transistor which was fabricated. Then germanium was the predominant material for solid-state device through the 1950s and 1960s. The first integrated circuit using germanium was fabricated by Jack Kilby at Texas Instrument in 1958. However, the first metal oxide semiconductor field effect transistor (MOSFETs) was invented by Dawon Kahng and Martin Atalla at Bell Laboratory in 1959. Since that, germanium was largely replaced by silicon due to several reasons. The reasons include that silicon exhibits larger bandgap than germanium resulting in lower leakage current. Second, SiO_2 reveals excellent thermal stability and quality for silicon as the gate dielectric compared to water-soluble and thermal unstable GeO_2 for germanium [1.1]. Third, silicon is abundant on the earth's surface. Therefore, silicon has formed the basis of the semiconductor industry almost since its birth.

According to Moore's law [1.2], the number of transistors on integrated circuit doubles approximately every eighteen months. Continue to shrink each component in an integrated circuit can allow more complex circuit in the same area or an equally complex circuit in a smaller area. According to **Table 1.1** [1.3]**,** the scaling parameters are derived based on the constant field scaling, in which the electric field at the semiconductor surface under that gate is kept constant to control the short channel effect.

Recently, it is becoming much difficult to enhance Si complimentary metal-oxide-semiconductor (CMOS) performance through traditional device scaling. In order to maintain Moore's law, MOSFETs with high-mobility channel are attractive for the advanced CMOS devices [1.4]. Germanium has the potential advantage of having carrier mobility high enough to overcome the future scaling limits of Si MOSFET and it is compatible with the conventional Si integration technologies. Therefore, germanium has been identified as the candidate for the channel engineering.

1.2 Motivation

As we know the driving current of a MOSFET can be described as below

$$I_{DS} = \frac{1}{2} C_{ox} \mu \frac{W}{L} (V_{GS} - V_t)^2 \tag{1.1}$$

C_{ox} is the gate oxide capacitance, μ is the mobility for hole or electron, W is the channel width, L is the channel length, V_{GS} is the applied voltage from gate to source and V_t is the threshold voltage. Which we focus on are the mobility and gate oxide capacitance. As shown in **Table1.2** [1.5], germanium reveals better electron (3900 cm^2/V-s v.s. 1500 cm^2/V-s) and hole (1900 cm^2/V-s v.s. 450 cm^2/V-s) mobility than silicon. As we mention above, germanium oxide is water soluble and thermal unstable during fabrication. But there's a significant progress toward the replacement of SiO_2 gate dielectric with high dielectric constant (high-κ) material. Hence, the drawback of germanium oxide becomes less significant.

Recently, effective electrical passivation of germanium for high-κ gate dielectric layers using germanium oxide has been investigated [1.6]. However, GeO_2 gate stack may lead to large equivalent oxide thickness (EOT). In order to scale down EOT, all we want is to develop the gate stack that high-κ material directly on germanium. Employing ZrO_2 high-κ dielectric may be a promising solution. Though the ZrO_2 gate stacks have been investigated [1.7-1.9], the interfaces are still not good enough. Also, they do not use ZrO2 gate stack to realize Ge MOSFET.

1.3 Scope and Organization of the Thesis

The promising high-mobility substrate material, Ge, is investigated in this thesis. In this thesis, we focus on the research of using atomic layer deposition (ALD) to deposit ZrO_2 directly on germanium and then using high-κ rapid thermal anneal (high-κ RTA). The thesis is divided into five chapters and arranged as follows:

Chapter 1, a brief overview of background and motivation is described.

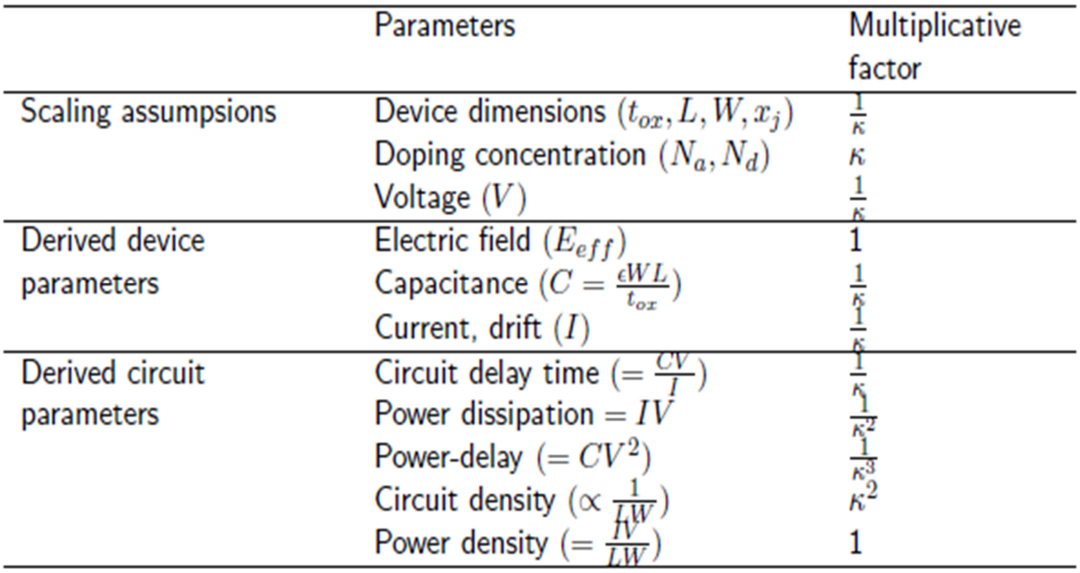
Chapter 2, p-type germanium MOS capacitor is fabricated using ALD ZrO_2. The interface quality of the ZrO_2/Ge system using high-κ RTA at different temperatures is investigated. Theory of conductance method is utilized to the extract density of interface state. Also, by quasi-static C-V curve and Berglund integral, we can estimate the band bending efficiency from the extracted surface potential.

Chapter 3, both n-MOSFETs and p-MOSFETs are fabricated using gate last process. The device electrical characteristics are investigated, including I_D-V_G, I_S-V_G, I_D-V_D, subthreshold swing, series resistance and mobility.

Chapter 4, both n-MOSFETs and p-MOSFETs are fabricated using gate first process. The device electrical characteristics are investigated, including I_D-V_G, I_S-V_G, I_D-V_D, subthreshold swing, series resistance and mobility.

Chapter 5, we summarize the experimental results and give the conclusion in this thesis.

Table 1.1 Scaling parameter in CMOS circuit design.



	Parameters	Multiplicative factor
Scaling assumpsions	Device dimensions (t_{ox}, L, W, x_j)	$\frac{1}{\kappa}$
	Doping concentration (N_a, N_d)	κ
	Voltage (V)	$\frac{1}{\kappa}$
Derived device parameters	Electric field (E_{eff})	1
	Capacitance $(C = \frac{\epsilon WL}{t_{ox}})$	$\frac{1}{\kappa}$
	Current, drift (I)	$\frac{1}{\kappa}$
Derived circuit parameters	Circuit delay time $(= \frac{CV}{I})$	$\frac{1}{\kappa}$
	Power dissipation $= IV$	$\frac{1}{\kappa^2}$
	Power-delay $(= CV^2)$	$\frac{1}{\kappa^3}$
	Circuit density $(\propto \frac{1}{LW})$	κ^2
	Power density $(= \frac{IV}{LW})$	1

Table 1.2 Material properties of bulk Ge, Si, GaAs, and InAs at 300K are compared.

	Ge	**Si**	**GaAs**	**InAs**
Bandgap (eV)	0.66	1.12	1.42	0.35
Hole mobility(cm^2/V-S)	1900	450	400	460
Electron mobility(cm^2/V-S)	3900	1500	8500	33000
Conduction band DOS Nc (cm^{-3})	$1.04x10^{19}$	$2.8x10^{19}$	$4.7x10^{17}$	$8.7x10^{16}$
Valance band DOS Nv (cm^{-3})	$6x10^{18}$	$1.04x10^{19}$	$7x10^{18}$	$6.6x10^{18}$
Lattice constant(Å)	5.646	5.431	5.653	6.058
Dielectric constant	16	11.9	13.1	15.2
Melting point(°C)	937	1412	1240	942
Dopant activation limit (cm^{-3})	P: $(4\text{-}6)x10^{19}$	P: $(1\text{-}2)x10^{20}$	P: $(4\text{-}6)x10^{18}$	P: $(1\text{-}3)x10^{18}$

Chapter 2

ZrO_2/Ge Gate Stack MOS Capacitance

2.1 Introduction

The rapid shrinking of the transistor feature size has forced the channel length and gate dielectric thickness to also decrease rapidly. That is the thickness of SiO_2 must decrease with channel length. However, gate leakage current increase with scaling down the oxide thickness due to direct tunneling. In order to achieve significant suppression of the direct-tunneling gate leakage current and continue scale down the EOT, replacing SiO_2 with high-κ dielectric remarkably demand [2.1].

Development of high-κ/Ge gate stack with high interface quality and small EOT is important for Ge to be used as high mobility channel material. Successful of high-κ/Ge gate stack such as Al_2O_3 and HfO_2 has been studied, recently. As shown in **Table2.1,** Al_2O_3 exhibits wide bandgap energy, large conduction band and valance band offset, thermal stability and the dielectric constant is 2.3 times larger than SiO_2. HfO_2 also exhibits wide bandgap energy, large conduction band and valance band offset, and the dielectric constant is 6.4 times larger than SiO_2. There are several multiple gate stack structures have been investigated, like $Al_2O_3/GeO_x/Ge$ [2.2-2.4] and $HfO_2/Al_2O_3/GeO_x/Ge$ [2.5]. Though, the technique of postoxidation has been developed to reduce the GeO_x thickness and still maintain the good interface quality, the EOT is still restricted due to not enough high dielectric constant of Al_2O_3. To overcome this obstacle, much higher-k HfO_2 is introduced. Nevertheless $HfO_2/GeO_x/Ge$ is not workable since the Ge-Hf bonds which can be produced owing to the Ge atoms diffuse into HfO_2 and, therefore, produce the energy states in the Ge bandgap and leakage pathway [2.6]. So, Al_2O_3 plays an important role in $HfO_2/Al_2O_3/GeO_x/Ge$ gate stack not only serving oxygen diffusion barrier but also suppress Ge diffusion to form leakage path. However, the existence of Al_2O_3 may restrict the EOT to be further scaled down.

In this chapter, p-type germanium MOS capacitors are fabricated with ZrO_2/Ge gate stack by plasma enhanced ALD (PE-ALD) which use Tetrakis(ethylmethylamino)zirconium (**TEMAZr**) as precursor and then followed by oxygen plasma . The reason why we use ZrO_2 is that it exhibits high dielectric constant and also ZrO_2 directly on Ge won't cause leakage path like HfO_2. The effect of different PE-ALD ZrO_2 growth temperatures and different post deposition annealing (PDA) temperatures are investigated. Theory of the conductance method is discussed in detail, and utilized to extract the density of interface state (D_{it}) for the different samples.

2.2 Fabrication of PE-ALD ZrO_2/Ge MOS Capacitors

(100)-oriented p-Ge substrates with resistivity ca. 0.1 Ω·cm ~ 0.6 Ω·cm were used. In order to fabricate Ge MOS capacitors, Ge wafers were cleaned by diluted Hydrofluoric acid (DHF) and deionized water to remove native oxide. Then ZrO_2 film is obtained by PE-ALD growth with an interfacial GeO_x layer on each sample at 200°C and 250°C. Followed, each sample was annealed at 500°C and 600°C in N_2 ambient for 1 minute, respectively. Then, we defined gate electrode area by photolithography and then 1000 Å Ti/Pt was deposited by sputtering. Finally, 4000 Å Al was deposited by thermal coater as backside contact.

The process flow and MOS capacitor structure are shown in **Fig. 2.1** and **Fig. 2.2**. Also the cross-section transmission electron microscopy (TEM) image of the ZrO_2/Ge gate stack MOS capacitor is shown in **Fig. 2.3**.

2.3 Electrical and Physical Characteristics of Ge MOS Capacitors with Various PDA Conditions

The C-V characteristic can be discussed by equivalent circuit in **Fig. 2.4** [2.7]. C_{ox} is oxide capacitance, C_p is accumulation capacitance, C_b is bulk capacitance, C_n is inversion capacitance and C_{it} is interface trap capacitance. We take the p-type substrate as the example. When bias is negative, the surface is accumulated by hole, C_p is very high approaching a short circuit. For small positive bias, the surface is depleted. The space charge in the deletion region dominates and the interface charge will also contribute to the capacitance. For positive bias, C_n dominate. If the electron charge can follow the ac frequency **Fig. 2.5(d)**, C_n is very high approaching a short circuit. If the electron charge can’t follow the ac frequency **Fig. 2.5(e)**, then C_b dominates.

High interface trap density may cause inefficient Fermi level response or even Fermi level pinning, preventing control over the carrier in the channel and the realization of MOSFETs with good sub-threshold swing and high driving current. That is the reason why we want a lower density of interface state. **Fig. 2.5** and **Fig. 2.6** show the multi-frequency C-V of Ge MOS capacitors with different ALD temperatures and different PDA conditions. The more detailed C-V characteristic is shown in **Table2.2**. The hump of C-V curve in the depletion region indicates there are traps at the ZrO_2/Ge interface. We can obviously see that the MOS capacitors with ALD at 200°C reveal much larger hump in the depletion region, which means that the interface between ZrO_2 and Ge reveals higher density of interface state. This phenomenon may be the fact that the oxidation at lower ALD temperature is less complete than higher ALD temperature. Also, we can see that the MOS capacitor with PDA at 600°C which shows even lower hump is much better than the sample with PDA at 500°C. We conclude that using ALD at 250°C to form ZrO_2/Ge gate stack and then annealing at 600°C can result in much better interface quality.

To further investigate the impact of PDA, we analyze the interface by Ge *3d* XPS spectra. **Fig. 2.7** shows the Ge *3d* spectra of ZrO_2/Ge structure that without PDA, PDA at 500°C for 1 minute in N_2 and PDA at 600°C for 1 minute in N_2. We can see that with higher PDA temperature, the sample leads to more germanium suboxide. Because of Ge surface passivated with ZrO_2 are slowly oxidized without causing GeO diffusion. As a result, Ge atoms near MOS interface can be terminated with oxygen atoms or Ge atoms without dangling bonds even under the oxidation condition lower than GeO_2, leading to lower D_{it} with Ge suboxide [2.8]. This suggests that the decrease of density of interface state is attributable to more germanium suboxide.

Also, we use grazing incidence X-ray diffraction (GIXRD) to identify the crystalline phase of ZrO_2. The spectrum is shown in **Fig. 2.8**. All the conditions, such as as-deposited ZrO_2, ZrO_2 annealing at 500°C and 600°C show amorphous phase of gate dielectrics.

2.4 Determine the D_{it} at ZrO_2/Ge Interface

2.4.1 Conductance Method

It is often impractical to fabricate MOSFETs for germanium because the transistor fabrication may introduce other issue. Therefore, MOS capacitor structures are commonly used to investigate the interface of dielectric and substrate. The conductance method, proposed by Nicollian and Goetzberger in 1967, is one of the most sensitive methods to determine D_{it} [2.9-2.10]. The main advantage of conductance method is that D_{it} can be determined directly from the experiment. It is also the most complete method because it yields

D_{it} in depletion and weak inversion portion of the bandgap and the capture cross-sections for majority carriers. The conductance method is based on analyzing the loss due to interface trap capture and emission of carriers. The measurement is applied a dc gate voltage with a small amplitude ac signal (~25 mV) and frequency (typically between 1 MHz and 1 kHz).

The simplified equivalent circuit of MOS capacitor appropriate for the conductance method is shown in **Fig. 2.9 (a)**. It consists of the oxide capacitance C_{ox}, the semiconductor capacitance C_S, and the interface trap capacitance C_{it}. The circuit can be simplified as in **Fig. 2.9 (b),** where C_p and G_p are given by

$$C_p = C_S + \frac{C_{it}}{1+(\omega\tau_{it})^2}, \tag{2.1}$$

and

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2}. \tag{2.2}$$

The interface trap capacitance is related to density of interface state by $C_{it} = q^2 D_{it}$, where q is the elemental charge, ω is the angular frequency, $\omega = 2\pi f$ (f is the measurement frequency).

The trap response time is given by Shockley-Read-Hall statistic of capture and emission rate:

$$\begin{cases} \tau_{it,e} = (\sigma v_{th,e} N_C)^{-1} \exp\left[\dfrac{E_C - E_t}{k_B T}\right] \\ \tau_{it,h} = (\sigma v_{th,h} N_V)^{-1} \exp\left[\dfrac{E_t - E_V}{k_B T}\right] \end{cases}, \tag{2.3}$$

where σ is the capture cross section, v_{th} is the thermal velocity, N is the effective density of state of majority carrier band, E_c and E_v are the conduction band and valence band energy, E_t is the trap energy in bandgap, k_B is the Boltzmann constant and T is the temperature. Eq. (2.1) and (2.2) are for interface trap with a single energy level in bandgap. However, interface traps are continuously distributed in bandgap. For continuum trap energy, the time constant dispersion must be taken into account and the normalized conductance is shown:

$$\frac{G_p}{\omega}=\frac{qD_{it}}{2\omega\tau_{it}}\ln\left[1+(\omega\tau_{it})^2\right]. \tag{2.4}$$

The maximum appears at $\omega \approx 2/\tau_{it}$ and we find

$$D_{it}=\frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{\max}, \tag{2.5}$$

where A is the device area. G_P/ω plots are repeated at different gate voltage to determine D_{it} from the maximum G_P/ω and determine τ_{it} from ω at the peak conductance location on the ω-axis.

For measurement, the equivalent circuit is shown in **Fig.2.9 (c)**, where C_m is measured capacitance, G_m is measured conductance. We can express G_P/ω as

$$\frac{G_p}{\omega}=\frac{\omega G_m C_{ox}{}^2}{G_m{}^2+\omega^2(C_{ox}-C_m)^2}. \tag{2.6}$$

2.4.2 D_{it} Measurement of ZrO_2/Ge Interface

Fig. 2.10 shows trap level position calculated from Eq. (2.3), assuming the capture cross-section σ=1x10^{-16} cm^2. The interface trap response frequency as a function of temperature determines which trap in bandgap can be observable in MOS admittance characteristic. Due to typically measurement frequency (between 1 MHz and 1 KHz), it is unable to extract D_{it} in the whole bandgap at room temperature. Therefore, we vary the temperature to extract D_{it} in the whole bandgap. We can see that traps locate near to midgap can be observed at high temperature and traps locate near to band edge can be observed at low temperature.

Fig. 2.11 shows $G_p/A\omega q$ versus frequency of Ge MOS capacitor with different PDA conditions at 300K. The D_{it} value is estimated by multi peak values of the plot of $G_p/A\omega q$ versus frequency and then multiple a factor: 2.5. Also the frequency can be converted into energy in bandgap by Eq. (2.3). Therefore, the plot of interface state density versus energy in the bandgap can be obtained by repeated different gate voltages.

The capture cross-section is assumed to be 1x10^{-16} cm^2. And the plot of D_{it} versus valance band energy offset is shown in **Fig. 2.11**. We can see that the MOS capacitor with PDA at 600°C reveals about two times smaller interface states than the MOS capacitor with PDA at 500°C. The result matches to what we discuss in chapter 2.3. The lower hump in depletion region indicates lower density of interface states. Also, with higher PDA temperature, the interface between ZrO_2 and germanium contains more Ge suboxide which helps to improve the quality of interface.

The results show more interface state density in the midgap and this phenomenon is called “weak inversion response” [2.11]. Due to small bandgap of germanium, the interface traps will show a communication with majority and minority carrier in measurement frequency when a MOS capacitor is biased in weak inversion. The schematic band diagram is shown in **Fig. 2.13**. The traps can be filled or emptied by minority carrier is due to the proximity of Fermi level to minority carrier band.

The presence of the weak inversion response within the typical 1 KHz to 1 MHz measurement frequency depends on the bandgap energy, the capture cross section and the temperature. For silicon, this phenomenon does not occur in measurement frequency at 300K [2.12]. However, for small bandgap material like germanium, the weak inversion response will occur in measurement frequency at room temperature. As we mention in Eq. (2.3), lower temperature measurement may be a solution to prevent this effect.

Fig. 2.14 shows the relation between gate voltage and surface potential by quasi-static CV and Berglund integral.

$$\phi_S = \int_{V_{FB}}^{V_G} \left(1 - \frac{C_{QS}}{Cox}\right) dV_G \, .$$

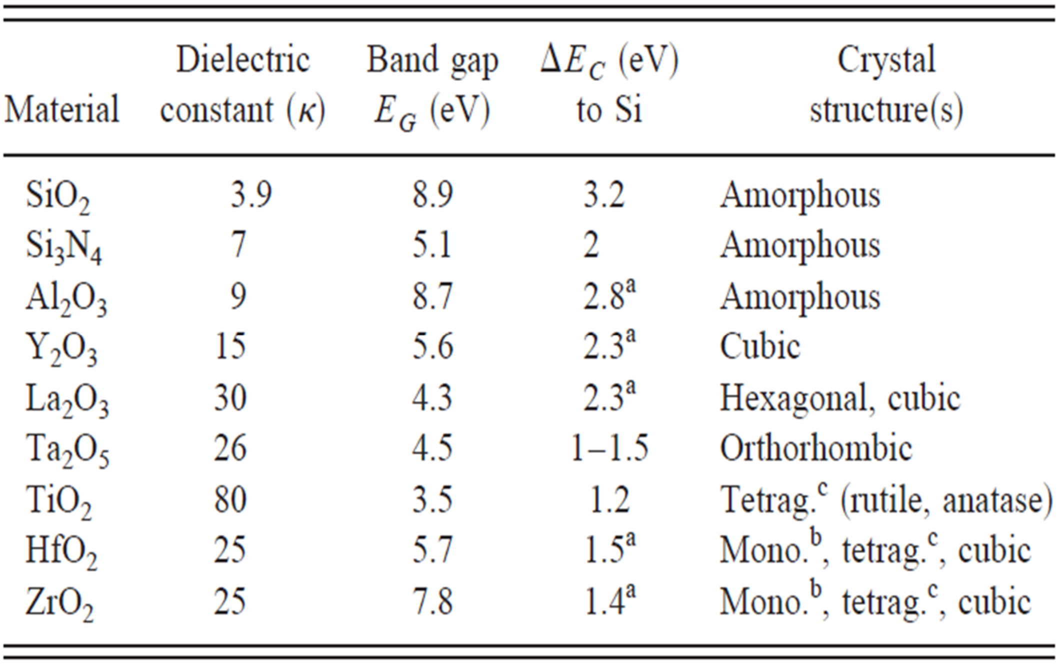
We can see that band bending is much effectively for Ge MOS capacitor with PDA at 600°C than Ge MOS capacitor with PDA at 500°C. Much effective band banding can also confirm that D_{it} for the sample with PDA at 600°C is less than PDA at 500°C.

2.5 Conclusion

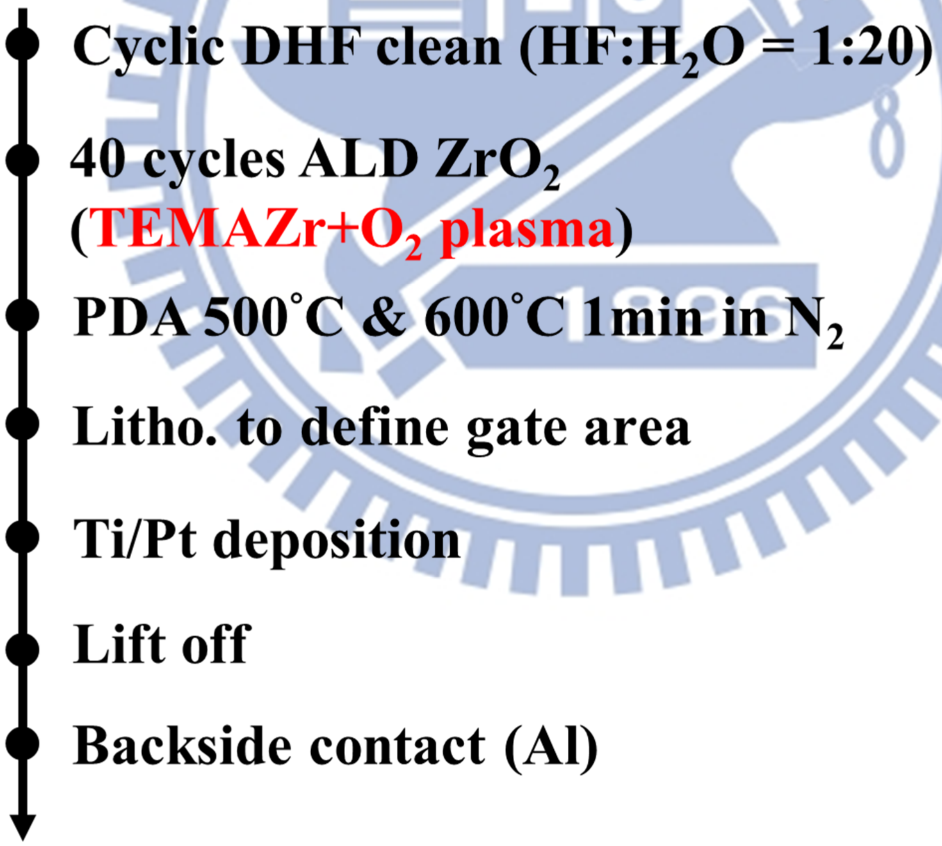
ZrO_2/Ge MOS capacitors are fabricated using PE-ALD. The interface of ZrO_2/Ge is investigated with different ALD temperature and different PDA conditions. The Ge *3d* XPS spectra of different samples such as as-deposited ZrO_2, ZrO_2 with PDA at 500°C and 600°C are shown. The XPS spectra show that with more germanium suboxide, the interface owns lower density of interface states. Conductance method was discussed in detail and utilized to extract D_{it} and confirm what we mention in Chapter 2.3.

The EOT is scaled down to around 1.7 nm and a lower D_{it} value is obtained by PDA at 600°C in N_2 ambient. Finally, we choose ZrO_2/Ge gate stack using PE-ALD at 250°C and then PDA at 600°C in N_2 ambient to be the optimized condition to fabricate germanium MOSFETs.

Table 2.1 Comparison of relevant properties for high-κ candidate.



Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.8[a]	Amorphous
Y_2O_3	15	5.6	2.3[a]	Cubic
La_2O_3	30	4.3	2.3[a]	Hexagonal, cubic
Ta_2O_5	26	4.5	1–1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetrag.[c] (rutile, anatase)
HfO_2	25	5.7	1.5[a]	Mono.[b], tetrag.[c], cubic
ZrO_2	25	7.8	1.4[a]	Mono.[b], tetrag.[c], cubic



Cyclic DHF clean (HF:H_2O = 1:20)

40 cycles ALD ZrO_2 (TEMAZr+O_2 plasma)

PDA 500˚C & 600˚C 1min in N_2

Litho. to define gate area

Ti/Pt deposition

Lift off

Backside contact (Al)

Fig. 2.1 Process flow of (100)-oriented Ge MOSCAPs with different ALD temperature and different PDA conditions.

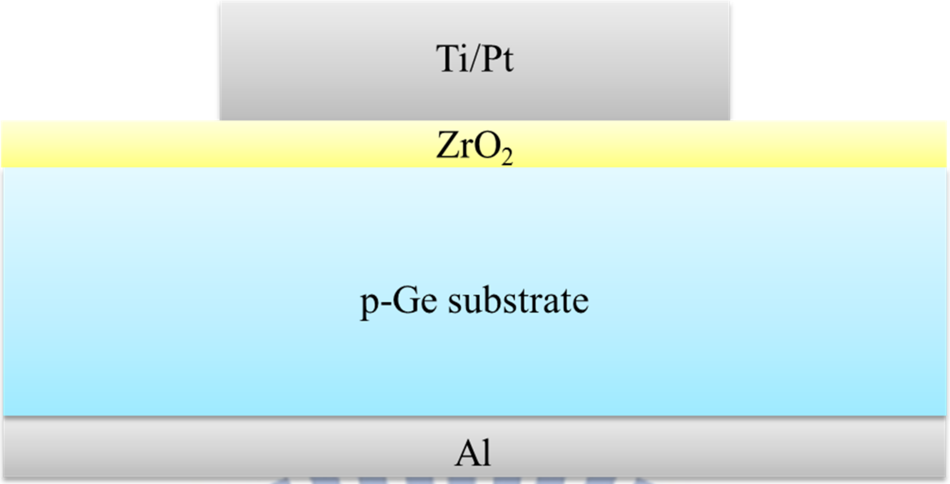


Fig. 2.2 MOSCAP of ZrO_2/Ge gate stack structure.

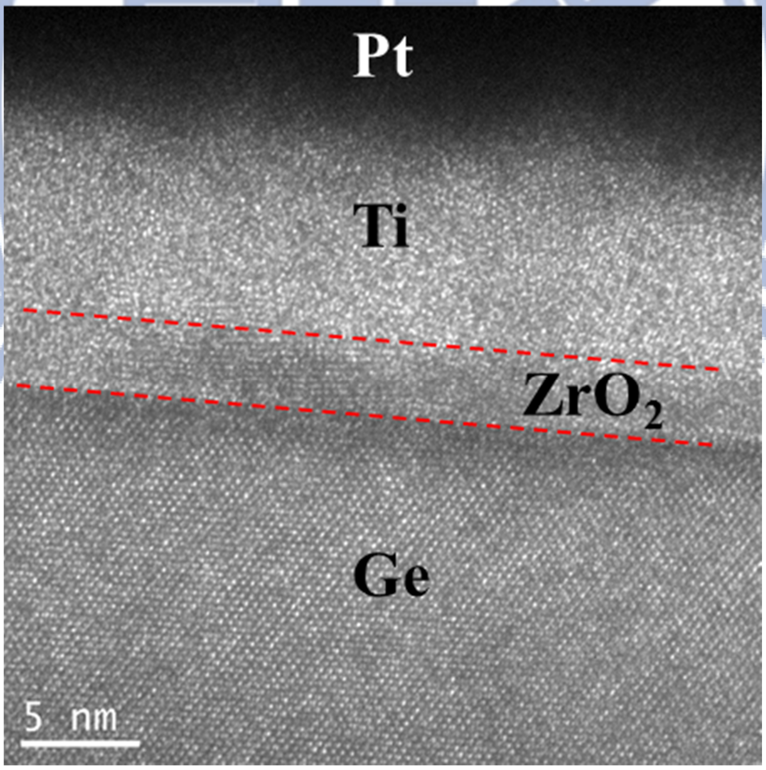
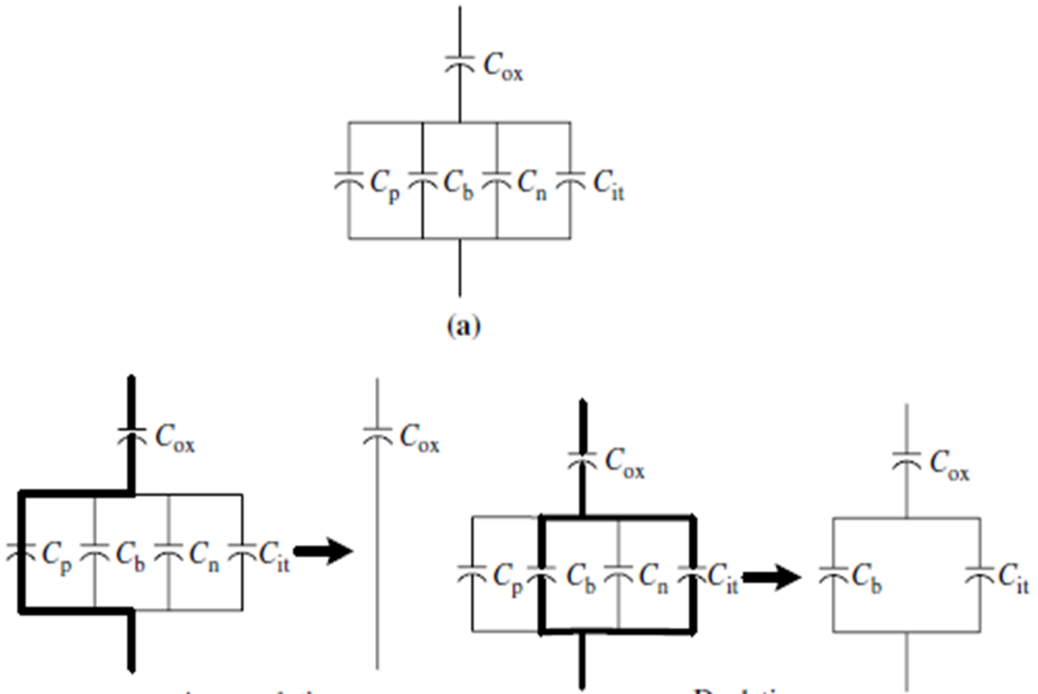
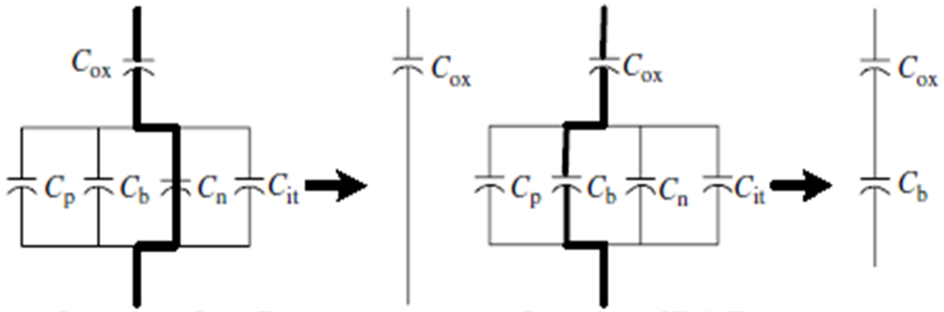


Fig. 2.3 TEM image of PE-ALD ZrO_2/Ge gate stack .



Accumulation
(b)

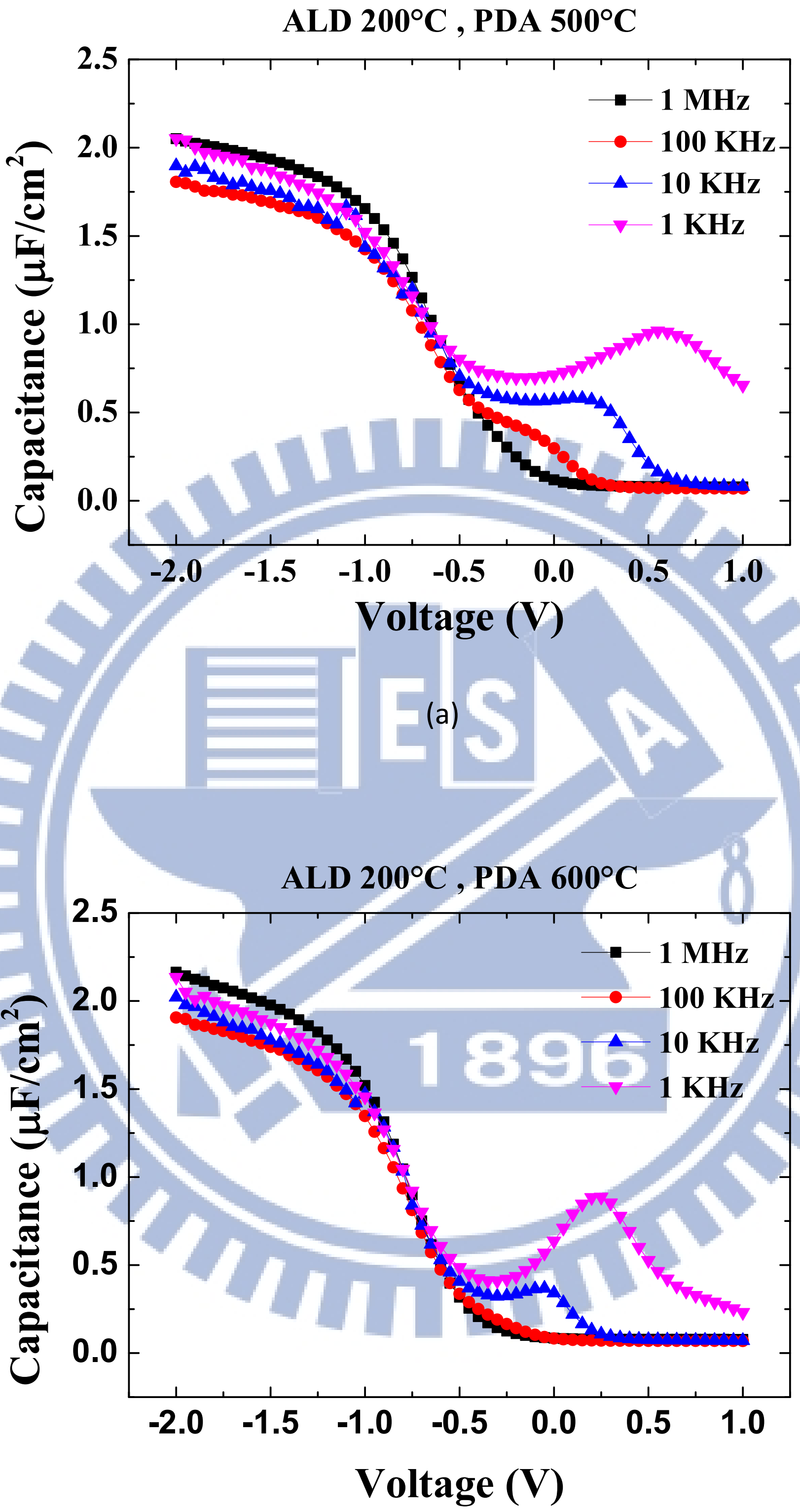
Depletion
(c)



Inversion - Low Frequency
(d)

Inversion - High Frequency
(e)

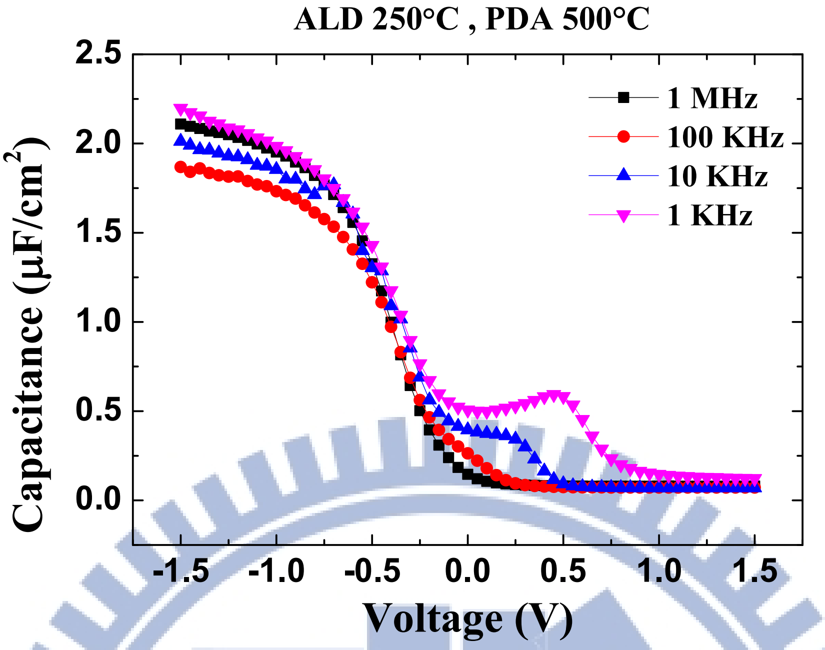
Fig. 2.4 Capacitance of an MOS capacitor for various bias conditions.



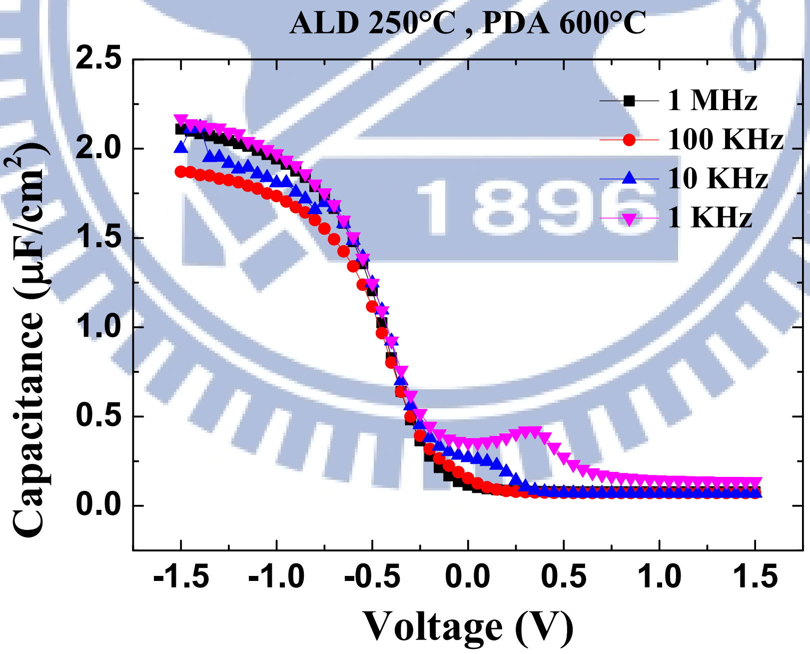
(a)

(b)

Fig. 2.5 Multi-frequency C-V of Ge MOS capacitor with different PDA condition using ALD 200°C; (a) PDA at 500°C for 1 min in N_2, and (b) PDA at 600°C for 1 min in N_2.



(a)



(b)

Fig. 2.6 Multi-frequency C-V of Ge MOS capacitor with different PDA condition using ALD 250°C; (a) PDA at 500°C for 1 min in N_2, and (b) PDA at 600°C for 1 min in N_2.

Table 2.2 C-V characteristic with different PDA temperature; (a) ALD at 200°C, and (b) ALD at 250°C.

ALD at 200°C

PDA temp.	C_{ox} (μF/cm^2)	EOT (nm)	V_{FB} (V)
500°C	1.95	1.77	-0.15
600°C	2.02	1.709	-0.3

(a)

ALD at 250°C

PDA temp.	C_{ox} (μF/cm^2)	EOT (nm)	V_{FB} (V)
500°C	2.01	1.717	-0.1
600°C	2.00	1.726	-0.15

(b)

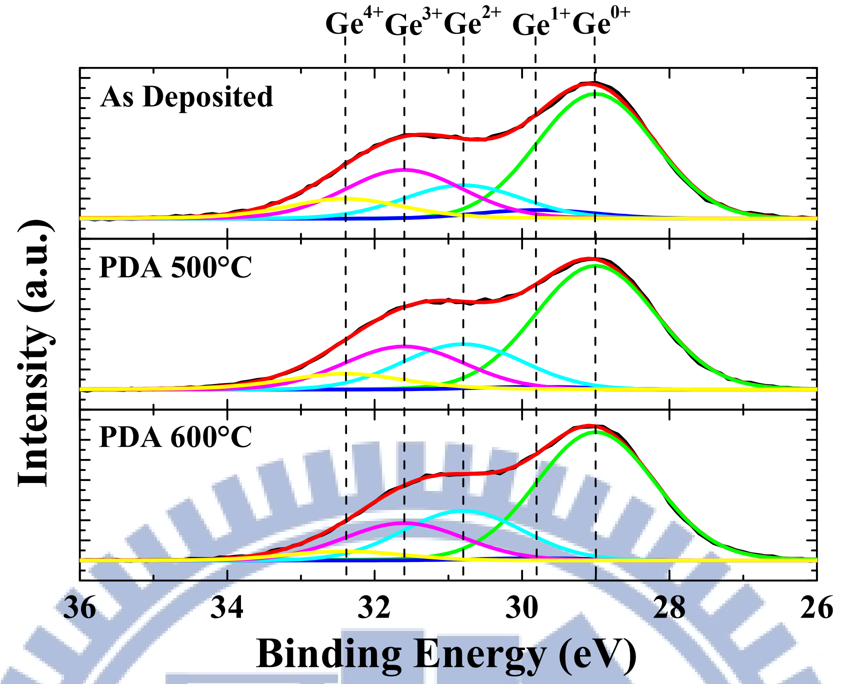


Fig. 2.7 Deconvolution of the XPS spectra of ZrO_2/Ge structure with different PDA conditions.

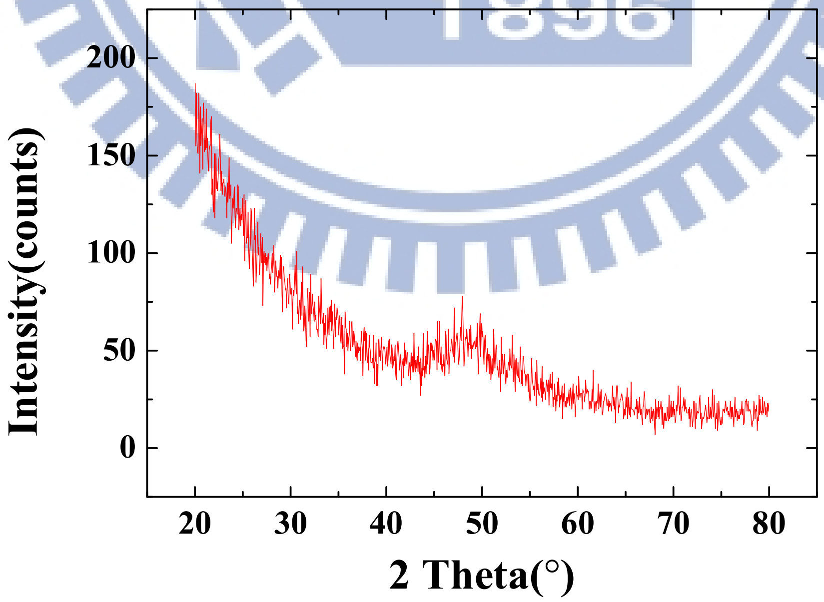


Fig. 2.8 GIXRD spectrum for as-deposited ZrO_2, ZrO_2 with PDA at 500°C and 600°C.

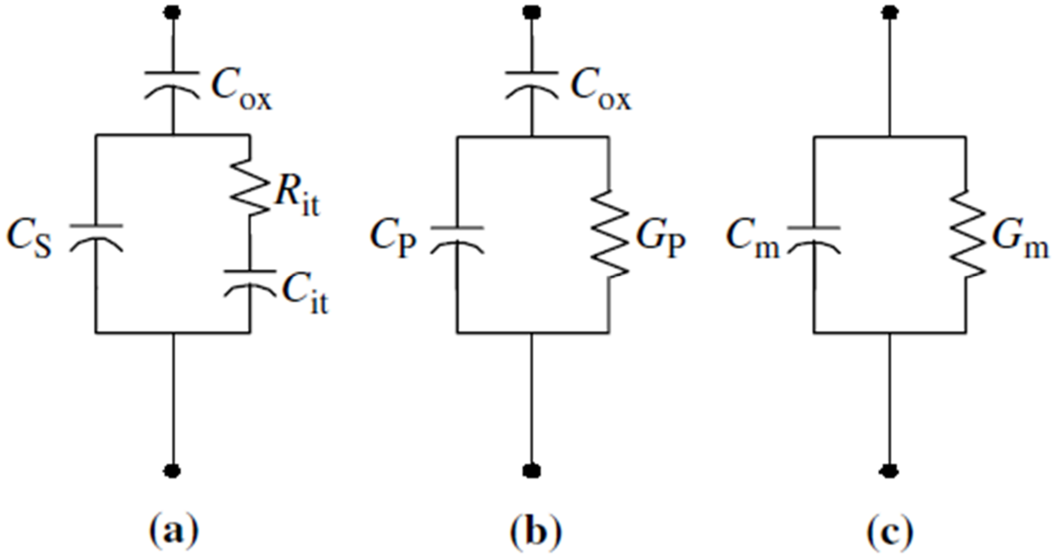


Fig. 2.9 Equivalent circuit for conductance measurement; (a) MOS capacitor with interface trap time constant $\tau_{it} = R_{it}C_{it}$, (b) simplified circuit of (a), and (c) measured circuit.

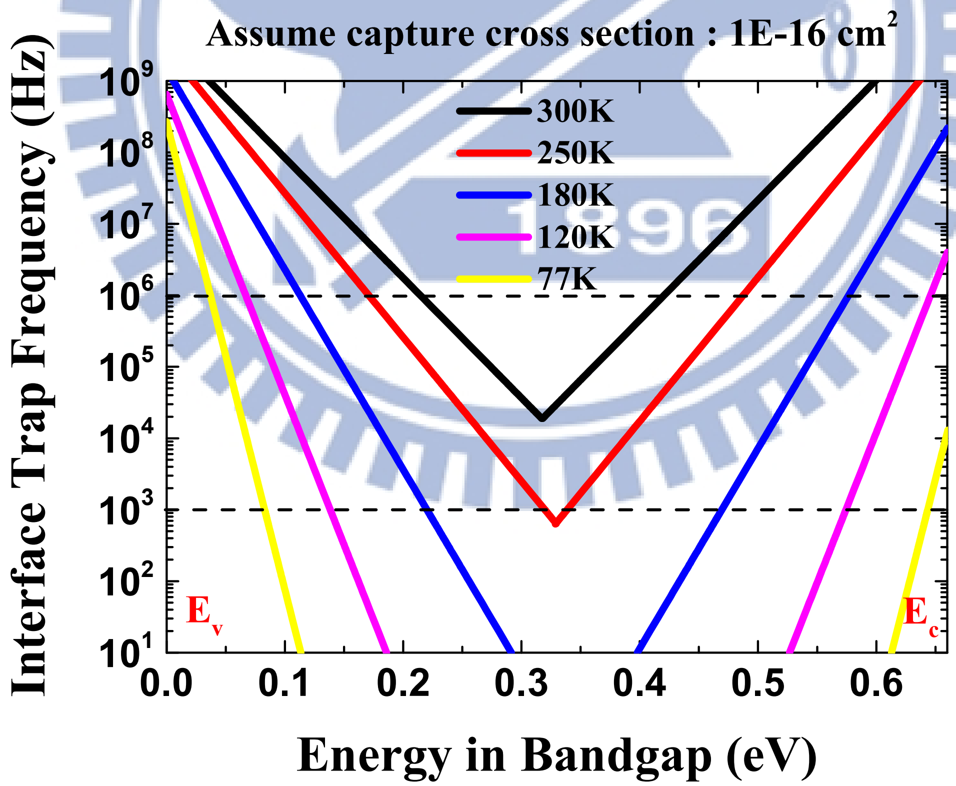
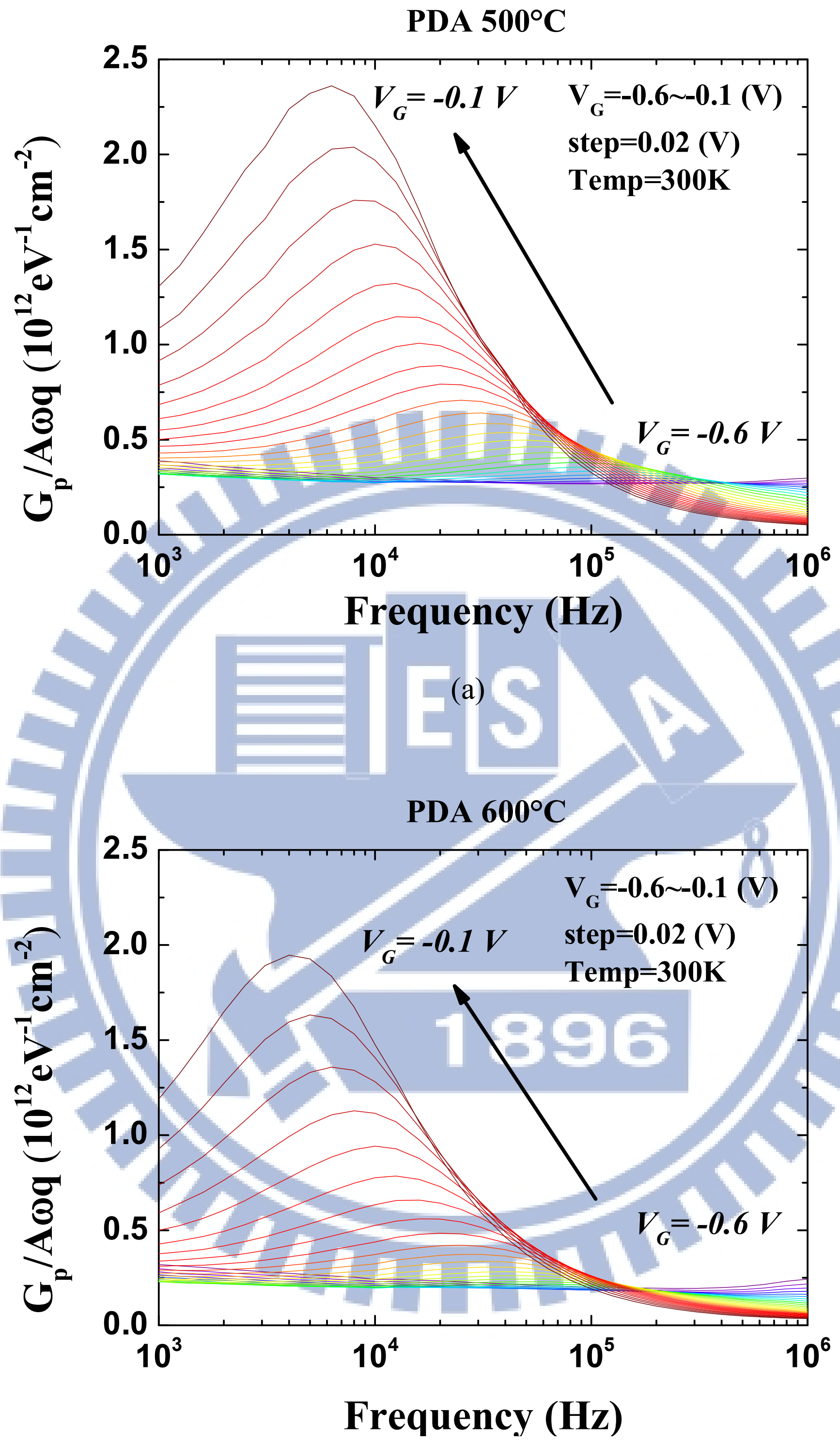


Fig. 2.10 Trap response frequency for germanium under different temperature.



(a)

(b)

Fig. 2.11 $G_p/A\omega q$ versus frequency of Ge MOS capacitor with different PDA conditions; (a) PDA at 500°C, and (b) PDA at 600°C.

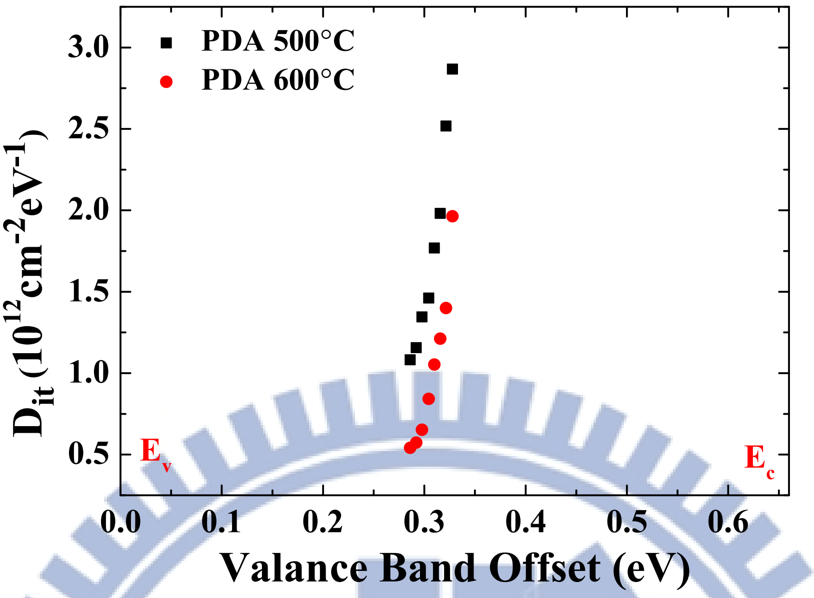


Fig. 2.12 D$_{it}$ measurement of Ge MOS capacitors with different PDA conditions.

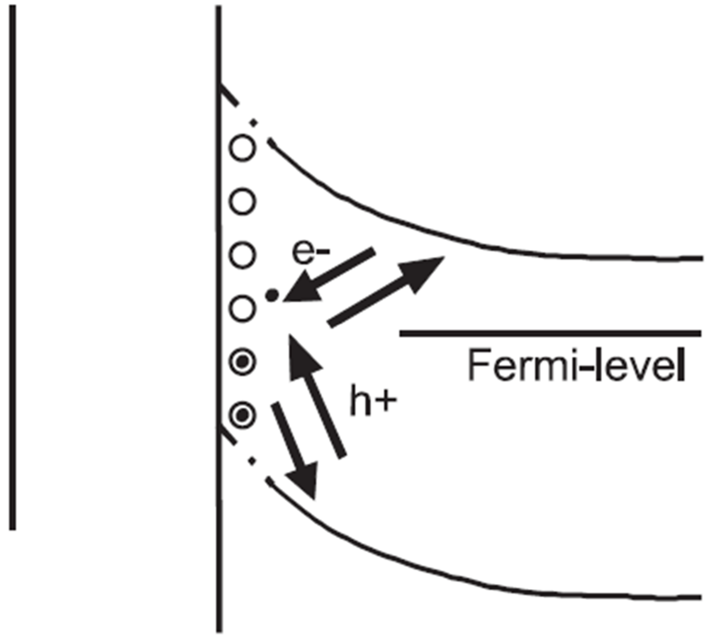
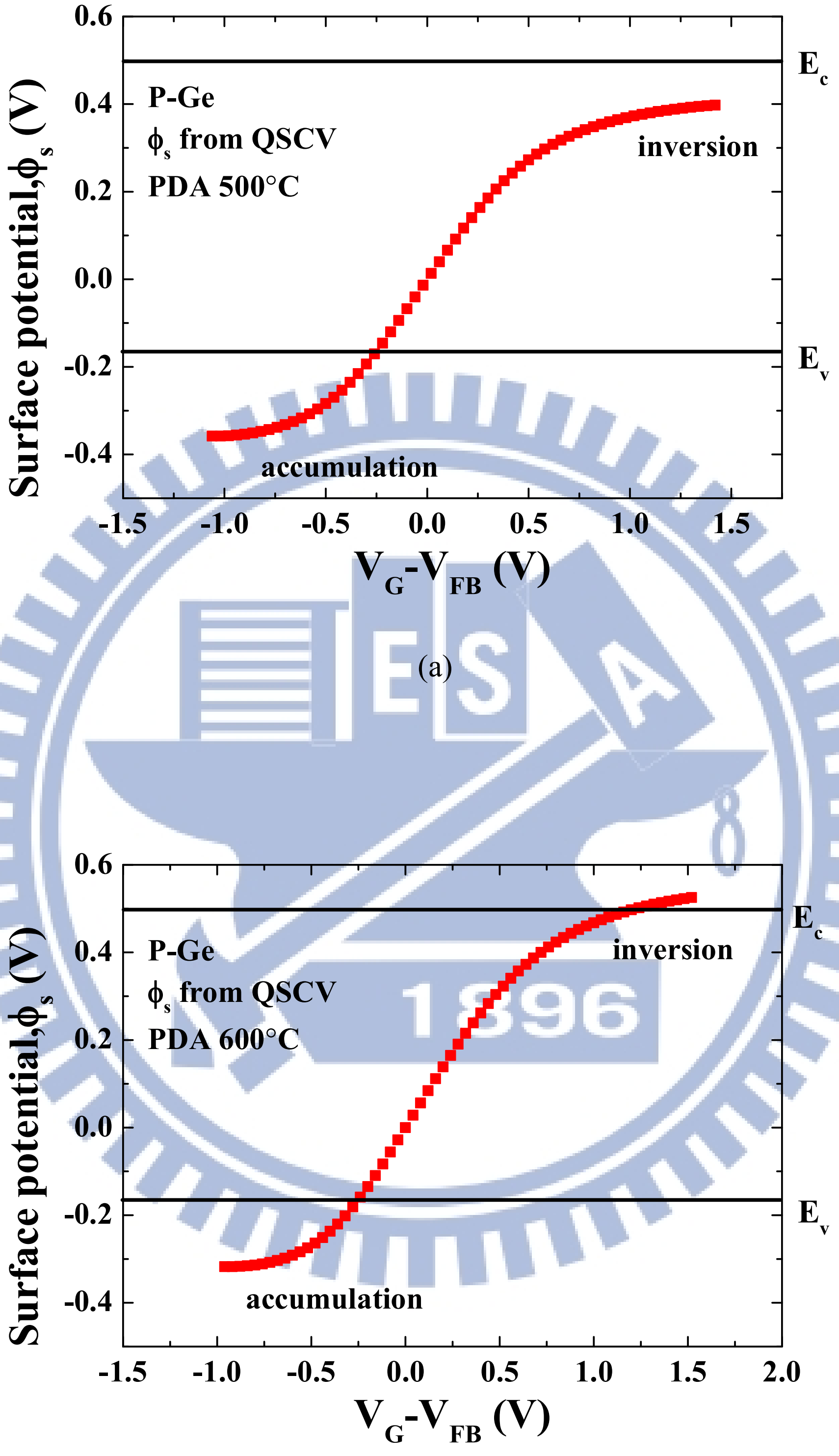


Fig. 2.13 A band diagram showing the weak inversion response.



(a)

(b)

Fig. 2.14 relation between gate voltage and surface potential by integration of quasi-static CV; (a) PDA at 500°C, and (b) PDA at 600°C.

Chapter 3

Germanium MOSFETs with ZrO_2/Ge Gate Stack Using Gate Last Process

3.1 Introduction

Since the technology node of complementary metal-oxide-semiconductor (CMOS) comes to 22 nm, it is becoming much difficult to enhance Si CMOS performance through traditional device scaling [3.1].To further improve the device performance, channel materials with high mobility will be needed for future nodes to meet the ITRS requirements of MOSFETs [3.2]. Germanium is one of potential candidate to replace silicon due to high electron and hole mobility. Also, it is compatible with the conventional silicon integration technologies

Compared to SiO_2, GeO_x is water soluble and reveals poor thermal stability. However, by replacing dielectric with high-κ material, the main drawback of germanium disappears. Recently, high hole and electron mobility have been reported for Ge p-MOSFETs [3.3] and Ge n-MOSFETs [3.4-3.5]. Ge n-MOSFETs always exhibit poor driving currents and mobility lower than universal Si mobility. The reasons are the large source/drain resistance due to low-level activation of n-type dopant. Also, fermi level pinning at the interface between n-Ge and metal leads to the formation of a Schottky barrier which is almost independent on the metal work function [3.6-3.8]. Therefore, the good passivation of the gate oxide/channel interface is needed to improve Ge n-MOSFETs performance.

In this chapter, both germanium n-MOSFET and p-MOSFET were fabricated using gate last process. Junction and device characteristics, series resistance, subthreshold swing and mobility are discussed.

3.2 Fabrication of Gate Last Ge-MOSFETs

(100)-oriented p-Ge substrates and (100)-oriented n-Ge substrates with resistivity ca. 0.1 Ω·cm ~ 0.6 Ω·cm and ca. 0.6 Ω·cm ~ 0.94 Ω·cm were used to fabricate Ge n-MOSFETs and Ge p-MOSFETs, respectively. In order to fabricate Ge MOSFETs, Ge wafers were cleaned by diluted Hydrofluoric acid (DHF) and deionized water to remove native oxide. Then we deposited 4200 Å SiO_2 for field oxide by Plasma-enhanced chemical vapor deposition (PECVD). The source and drain region were defined by first photolithography, followed by implantation of phosphorous for Ge n-MOSFETs and BF_2 for Ge p-MOSFETs. Both phosphorous and BF_2 dopant concentration are 1x15 cm^{-2} and implant energy are 20 keV. After implantation, we deposited 1000 Å SiO_2 for capping layer to prevent dopant out-diffuses during dopant activation. Then we activated dopant by rapid thermal annealing (RTA) system 600°C 30 second for BF_2 and 600°C 10 second for phosphorous, respectively. Next active area (AA) was defined by second photolithography and then 40 cycles PE-ALD ZrO_2 was deposited at 250°C. The samples were annealed using high-κ RTA at 600°C for 60 second in N_2 ambient. After annealing, contact hole was defined by third photolithography, followed dry etching the contact hole on source/drain region. 4000 Å Al was deposited by thermal coater and then defined metal pads through fourth photolithography. Finally, 4000 Å Al was deposited as backside contact. The process flow and device structure are shown in **Fig. 3.1** and **Fig. 3.2**.

3.3 Electrical Characteristic of Ge MOSFETs

Fig. 3.3 shows the junction characteristics of Ge p-MOSFET and Ge n-MOSFET. For p^+/n junction, the current density at forward bias and reverse bias are 6.584×10^1 A/cm^2 at 1 V and 3.93×10^{-3} A/cm^2 at -1 V, respectively while the on/off ratio is about 1.66×10^4. For n^+/p junction, the current density at forward bias and reverse bias are 5.06×10^1 A/cm^2 at -1 V and 3.29×10^{-4} A/cm^2 at 1 V, respectively while the on/off ratio is about 1.51×10^5. The higher current density at reverse bias of germanium device compare to silicon devices is due to smaller bandgap of germanium. To extract junction series resistance, we know that:

$$I \approx I_0 e^{q(V-Ir_s)/nkT},$$

and

$$g_d = \frac{dI}{dV} = \frac{qI(1-r_s g_d)}{nkT}. \tag{3.1}$$

We can write Eq. (3.1) as

$$\frac{I}{g_d} = \frac{nkT}{q} + Ir_s.$$

A plot of I/g$_d$ versus I can determine series resistance (r$_s$) from slope. For p^+/n junction, the series resistance is about 59.4 Ω. For n^+/p junction, the series resistance is about 47.7 Ω.

To extract ideality factor, we know that:

$$I = I_0 e^{qV/nkT}(1-e^{-qV/kT}). \tag{3.2}$$

We can write Eq. (3.2) as

$$\ln\left(\frac{I}{1-e^{-qV/kT}}\right) = \ln I_0 + \frac{q}{nkT}V.$$

A plot of ln[I/(1-exp(-qV/kT))] versus V can determine ideality factor (n) from slope. The ideality factor of p^+/n junction is 1.262 and that of n^+/p junction is 1.512.

Fig. 3.4 shows I_D-V_G and I_S-V_G characteristics of Ge p-MOSFET and Ge n-MOSFET.

For Ge p-MOSFET, the on/off ratio is about $5.62\text{x}10^4$ for I_S and $2.92\text{x}10^3$ for I_D. For Ge n-MOSFET, the on/off ratio is about $1.85\text{x}10^5$ for I_S and $1.73\text{x}10^4$ for I_D. The reason why on/off ratio of I_D is always lower than that of I_S is due to small bandgap energy of germanium causes junction leakage. Our MOSFETs also show serious gated-induce drain leakage current (GIDL) due to large gate to source/drain overlapping area. The subthreshold swing of p-MOSFET is about 119.1 mV/dec, while that of n-MOSFET is about 112.5 mV/dec.

Fig. 3.5 shows I_D-V_D characteristics of Ge p-MOSFET and Ge n-MOSFET. At the same overdrive voltage, we can observe that p-MOSFET reveals much larger driving current than n-MOSFET, due to n-MOSFET reveals much larger source/drain resistance than p-MOSFET. As we know, n-type dopant like phosphorous is much easier lost during subsequent annealing by out-diffusion [3.9-3.10]. During high-κ dielectric annealing, there's only about 3~4 nm ZrO_2 film on source/drain region, such a thin film could not restrict phosphorous out-diffuse. Also, activation of n-type dopant in germanium is a problem which the active level of n-type dopant in germanium is much lower than p-type dopant in germanium [3.11-3.12].

Fig. 3.6 shows the plot of measured resistance versus channel length on mask for Ge p-MOSFET and Ge n-MOSFET. We extract source/drain series resistance (R_{SD}) by Terada and Muta method [3.13].

$$R_m = \frac{V_{DS}}{I_D} = R_{ch} + R_{SD} = \frac{L-\Delta L}{W_{eff}\mu_{eff}C_{ox}(V_{GS}-V_t)} + R_{SD}, \tag{3.3}$$

where R_m is measured resistance, R_{ch} is channel resistance; R_{SD} is source/drain series resistance. Eq. (3.3) gives $R_m=R_{SD}$ while $L=\Delta L$. A plot of R_m versus L for device with different L and varying gate voltage shows lines intersecting at one point giving R_{SD}. If the lines fail to intersect at same point, we can further write Eq. (3.3) as

$$R_m = R_{SD} + AL_{eff} = (R_{SD} - A\Delta L) + AL = B + AL. \tag{3.4}$$

The parameters A and B are determined from slope and intercept of R_m versus L plots for different gate voltages. R_{SD} can be obtained from the intercept of a B versus A plot. By our measurements, the source/drain series resistance is about 365.2 Ω for p-MOSFET and 1965.4 Ω for n-MOSFET. Also ΔL=0.75 μm for p-MOSFET and ΔL=0.15 μm for n-MOSFET.

To extract effective mobility

$$\mu_{eff} = \frac{g_d L}{W Q_{inv}},$$

where the drain conductance g_d is defined as

$$g_d = \frac{\partial I_D}{\partial V_{DS}} | V_{GS} = constant,$$

and Q_{inv} can be measured by split-CV method

$$Q_{inv} = \int_{-\infty}^{V_{GS}} C_{GC} dV_G.$$

The mobile channel charge density is determined from the gate to channel capacitance, C_{GC}. Then C_{GC} is measured using the connection of **Fig. 3.7**, the capacitance meter is connected between the gate and the source/drain and the substrate is grounded. For $V_{GS} < V_T$ the channel region is accumulated and the overlap capacitances $2C_{ov}$ are measured (**Fig. 3.8 (a)**). For $V_{GS} > V_T$, the surface is inverted and $2C_{ov}+C_{ch}$ are measured (**Fig. 3.8 (b)**).

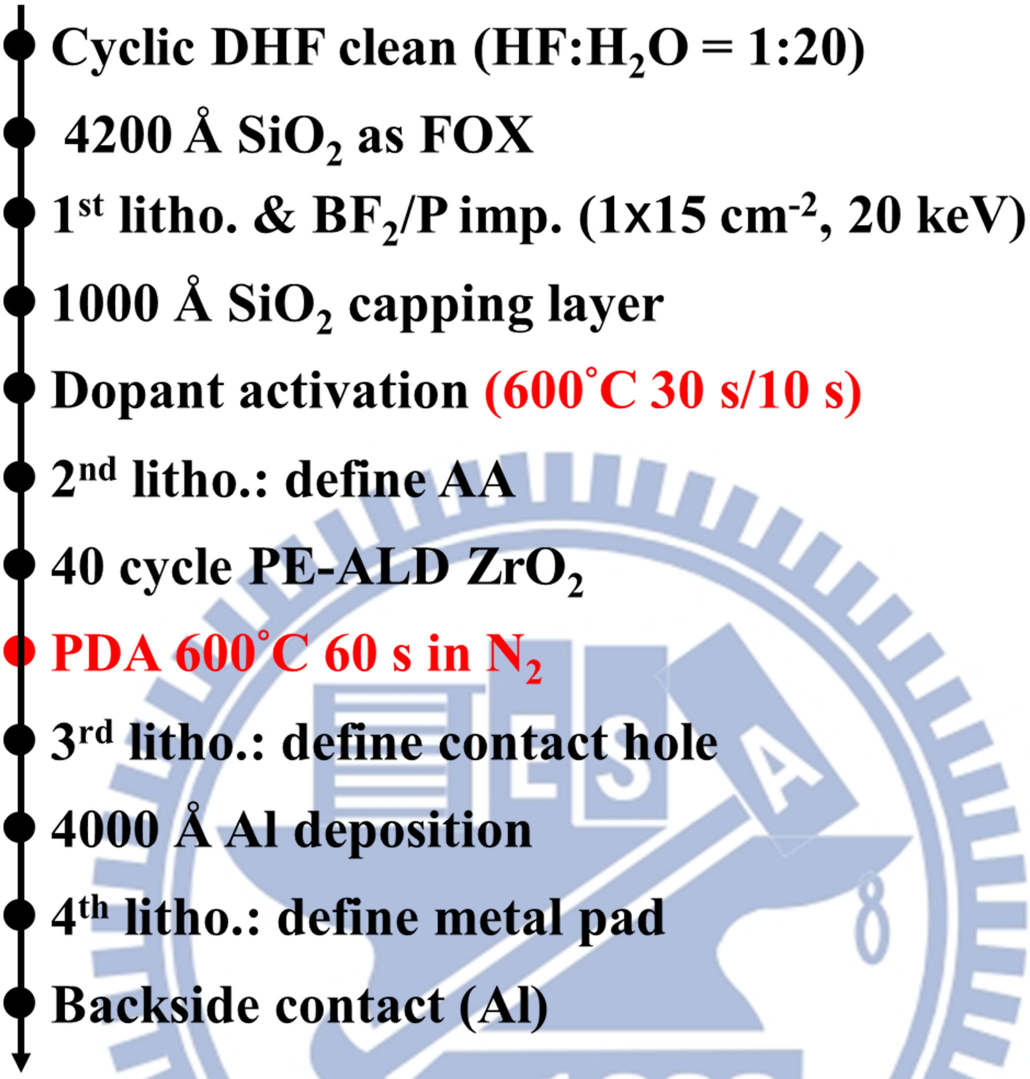
Fig. 3.9 shows hole mobility as a function of inversion charge density for Ge p-MOSFET. The peak hole mobility of p-MOSFET is about 259 cm^2/V-s. Here we do not show the electron mobility of Ge n-MOSFET because of the huge source/drain series drain resistance. The voltage drop across the source/drain resistance $I_D R_{SD}$ causes a reduction in drain current. Hence, the measured mobility by split C-V method appears to be lower than the real value.

3.4 Conclusion

In Chapter 3, we investigate fabrication and electric characteristics of Ge MOSFETs. For Ge p-MOSFET (the channel width is 100 μm, the channel length is 5 μm), the on /off ratio of p^+/n junction, I_D-V_G and I_S-V_G are about 1.66×10^4, 2.92×10^3, and 5.62×10^4, respectively, while the substhreshold swing is about 119.1 mV/dec. For Ge n-MOSFET (the channel width is 100 μm, the channel length is 5 μm), the on /off ratio of n^+/p junction, I_D-V_G and I_S-V_G are about 1.51×10^5, 1.73×10^4, and 1.86×10^5, respectively, while the substhreshold swing is about 112.5 mV/dec.

From I_D-V_D curve we can see that Ge n-MOSFET reveals poor driving current than Ge p-MOSFET at the same overdrive voltage. As we mentioned, n-type dopant in germanium diffuses much easier than p-type dopant in germanium. So n-type dopant will be much easier lost during subsequent thermal process because such a thin high-κ film on source/drain region cannot restrict the dopant out diffuse. Also, the activation level of n-type dopant in germanium is lower than p-type dopant in germanium. Due to these problems, Ge n-MOSFETs always exhibit poor performance than Ge p-MOSFETs.

To solve these problems, changing fabrication scheme may be a solution. In next chapter, Ge MOSFETs using gate first process will be introduced.



- Cyclic DHF clean ($HF:H_2O = 1:20$)
- 4200 Å SiO_2 as FOX
- 1st litho. & BF_2/P imp. (1x15 cm^{-2}, 20 keV)
- 1000 Å SiO_2 capping layer
- Dopant activation (600˚C 30 s/10 s)
- 2nd litho.: define AA
- 40 cycle PE-ALD ZrO_2
- PDA 600˚C 60 s in N_2
- 3rd litho.: define contact hole
- 4000 Å Al deposition
- 4th litho.: define metal pad
- Backside contact (Al)

Fig. 3.1 Process flow of Ge MOSFETs.

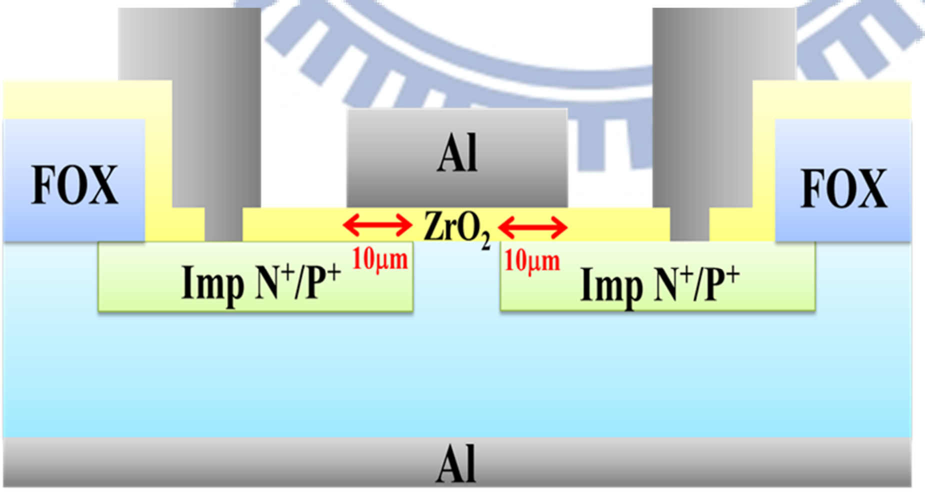
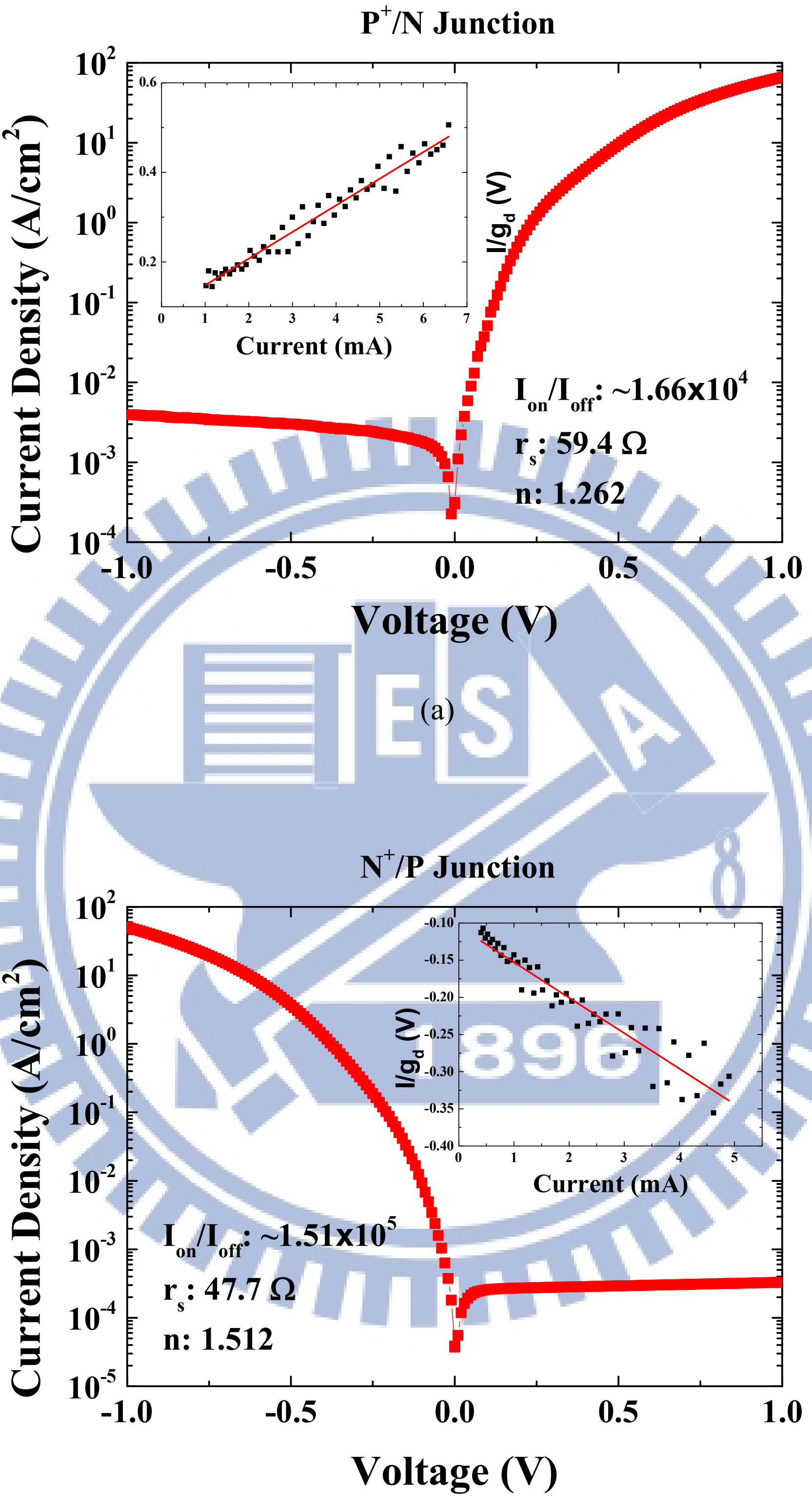


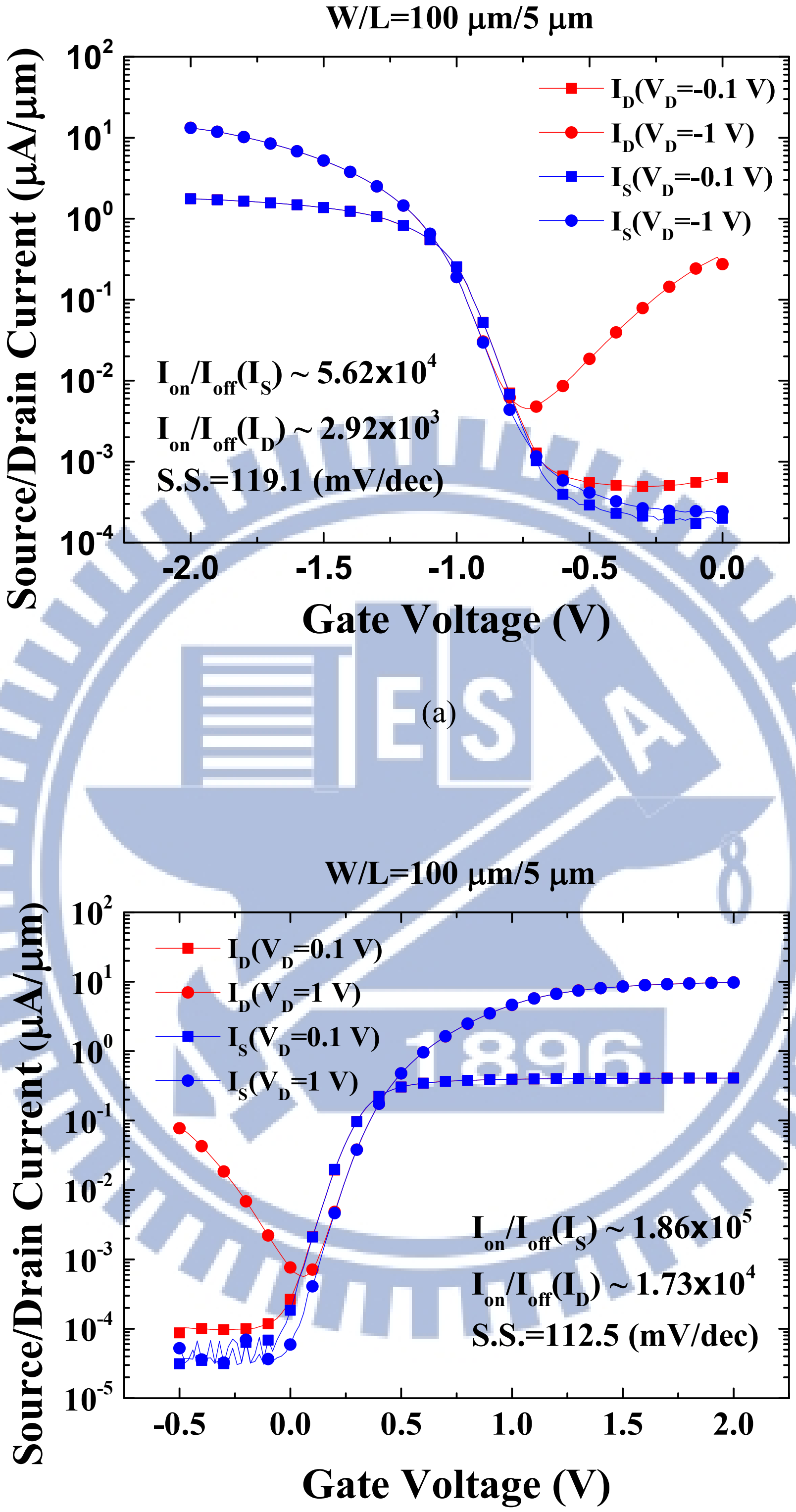
Fig. 3.2 Device structure of Ge MOSFETs.



(a)

(b)

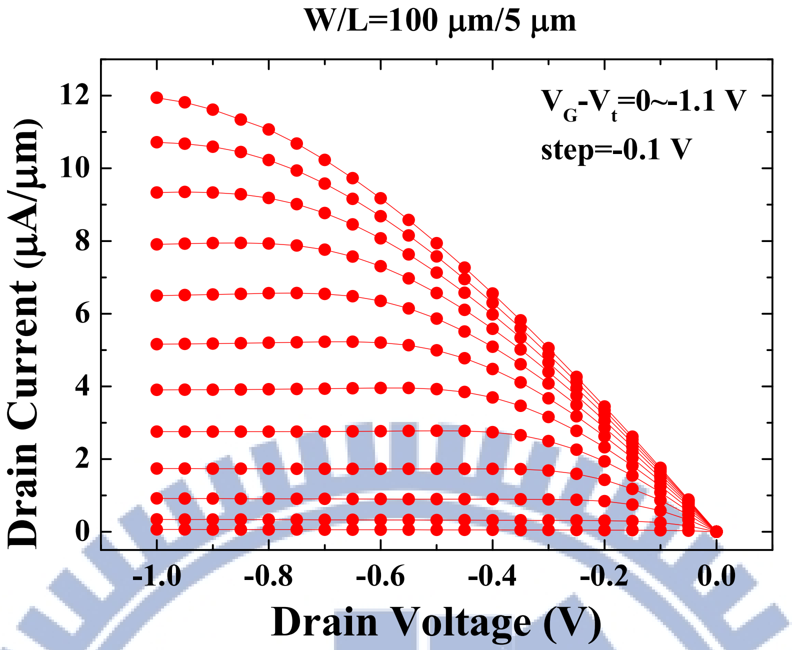
Fig. 3.3 I–V characteristics of $p^{+/}n$ and $n^{+/}p$ junctions; (a) $p^{+/}n$ junction, and (b) $n^{+/}p$ junction.



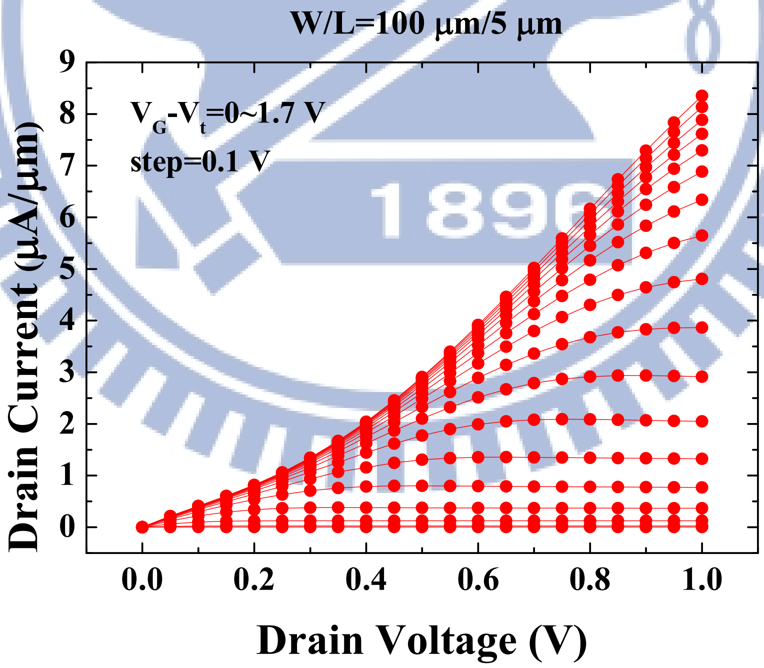
(a)

(b)

Fig. 3.4 I_D-V_G and I_S-V_G characteristics of Ge MOSFETs; (a) Ge p-MOSFET, and (b) Ge n-MOSFET.

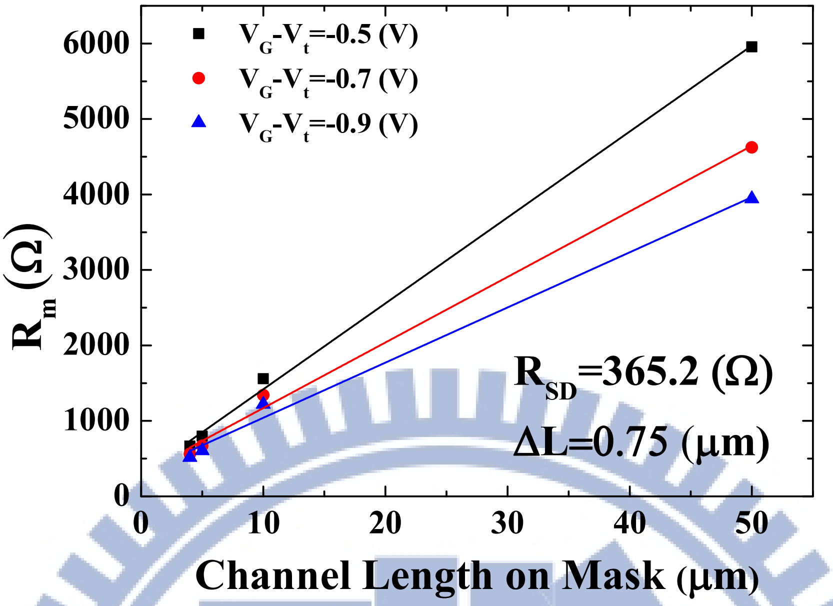


(a)

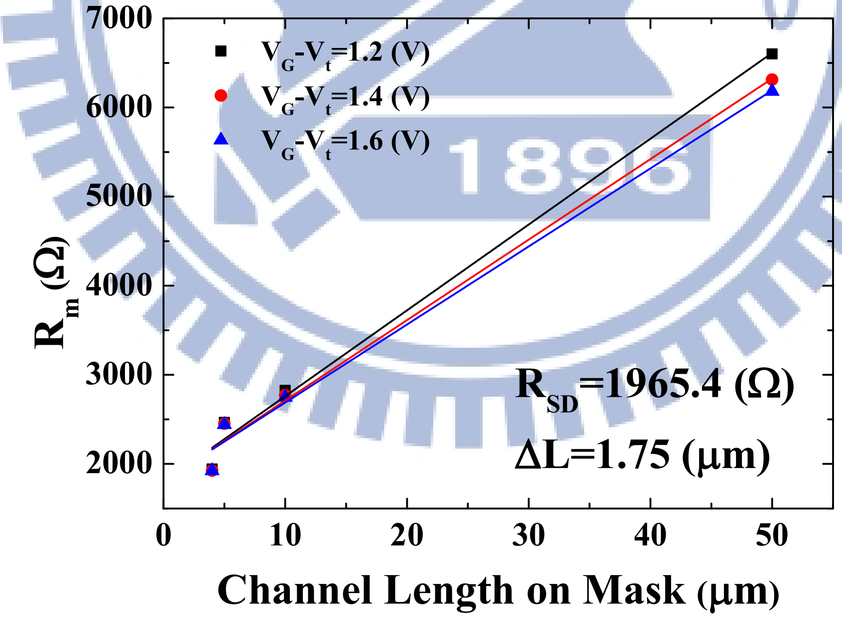


(b)

Fig. 3.5 I_D-V_D characteristic of Ge MOSFETs; (a) Ge p-MOSFET, and (b) Ge n-MOSFET.



(a)



(b)

Fig. 3.6 R_m versus L as a function of gate voltage to extract series resistance; (a) Ge p-MOSFET, and (b) Ge n-MOSFET.

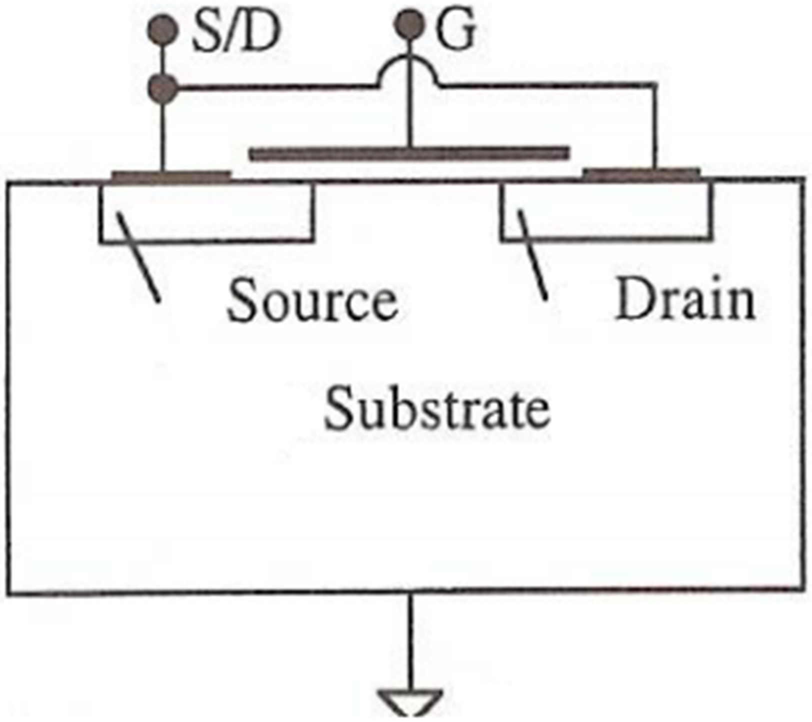
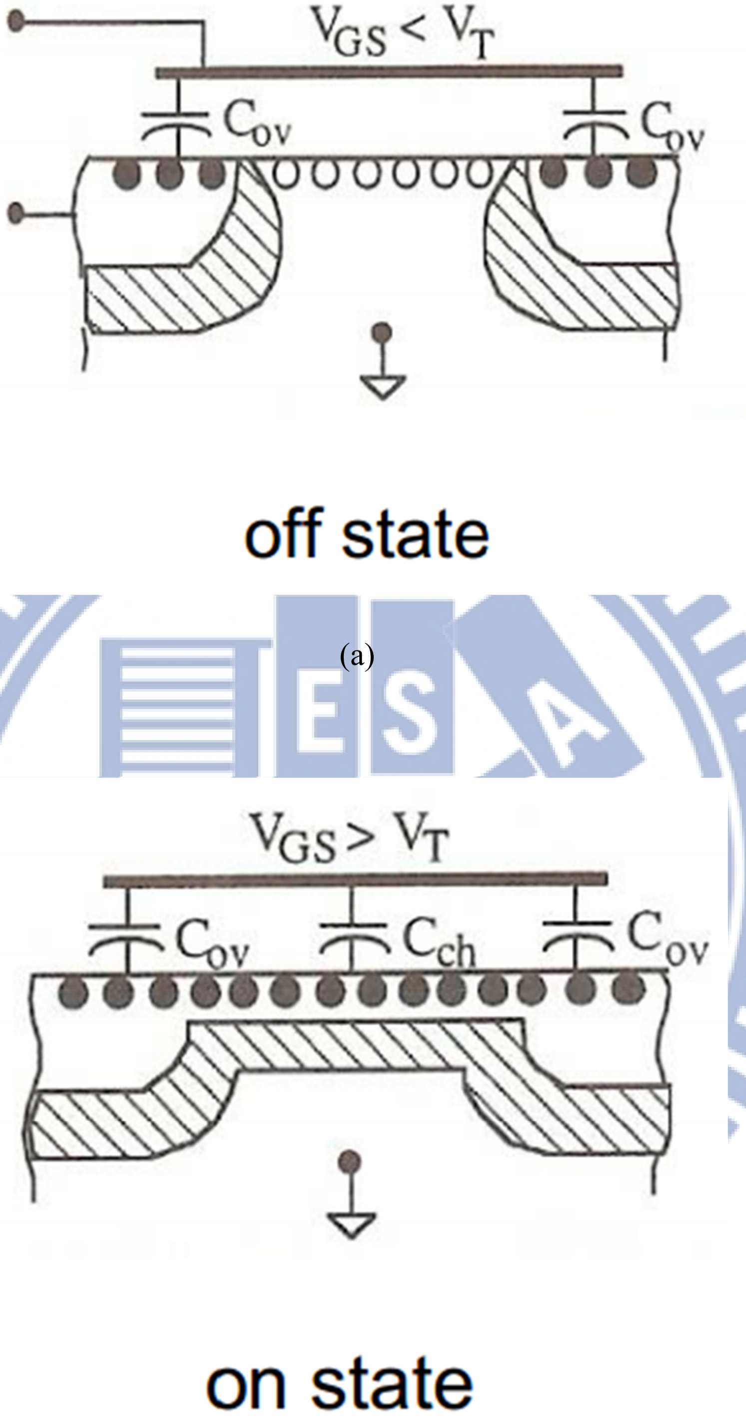


Fig. 3.7 Configuration to measure C_{GC}.



(a)

(b)

Fig. 3.8 Schematic for gate to channel capacitance measurements for (a) $V_{GS} < V_T$, and (b) $V_{GS} > V_T$.

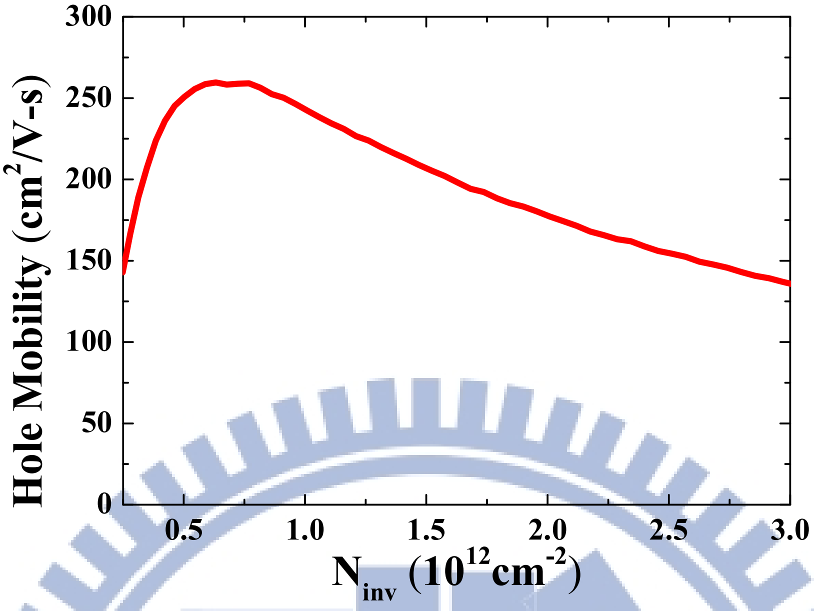


Fig. 3.9 Hole mobility as a function of inversion charge density for Ge p-MOSFET.

Chapter 4

Germanium MOSFETs with ZrO_2/Ge Gate Stack Using Gate First Process

4.1 Introduction

Recently, Ge p-MOSFET with high hole mobility has been reported [4.1-4.2]. But the Ge n-MOSFET is still not good enough due to the high interface density of state (D_{it}) [4.3] and the poor n^+/p junctions. Though, attention has been paid more to GeO_2/Ge gate stack due to its superior interface properties and has been reported with low D_{it} recently [4.4-4.7], the n^+/p junctions still suffer from the low activation and fast diffusion rate of n-type dopants in germanium.

A SiO_2 capping layer has been utilized to prevent dopant out-diffuse [4.8]. In Chapter 3, we have used this method to prevent dopant out-diffuse. However, SiO_2 capping layer will be removed and the dopant will out-diffuse during subsequent process. In order to conquer this drawback, change the fabrication scheme may be a solution. By gate first process, the source/drain will be defined after gate stack formation. Due to this change, more effective dopant activation caused by the last high temperature step in the gate first process can prevent dopant out-diffuse.

In this chapter, both germanium n-MOSFET and p-MOSFET are fabricated using gate first process. Junction and device characteristics, series resistance, subthreshold swing and mobility are discussed.

4.2 Fabrication of Gate First Ge-MOSFETs

(100)-oriented p-Ge substrates and (100)-oriented n-Ge substrates with resistivity ca. 0.1 Ω·cm ~ 0.6 Ω·cm and ca. 0.6 Ω·cm ~ 0.94 Ω·cm were used to fabricate Ge n-MOSFETs and Ge p-MOSFETs. In order to fabricate Ge MOSFETs, Ge wafer were cleaned by diluted Hydrofluoric acid (DHF) and deionized water to remove native oxide. Then we deposited 4200 Å SiO_2 for field oxide by Plasma-enhanced chemical vapor deposition (PECVD). The active area (AA) region was defined by first photolithography. And then 80 cycles ZrO_2 was deposited at 250°C using PE-ALD. After ZrO_2 deposited, the samples were annealed using high-κ RTA at 600°C for 60 second in N_2 ambient. Followed, 500 Å TiN was deposited for gate electrode by sputtering. Next, 500 Å SiO_2 was capping for hard mask and 5000 Å SiO_2 was capped at backside by PECVD. Because of the solution to etch TiN will etch photoresist, so we capped 500 Å SiO_2 on TiN for hard mask. Also, the solution to etch TiN will etch germanium, so we must cap 5000 Å SiO_2 to protect bulk germanium. Then gate was defined by second photolithography. Followed phosphorous for Ge n-MOSFETs and BF_2 for Ge p-MOSFETs were implanted. Both phosphorous and BF_2 dopant concentration are 1x15 cm^{-2} and implant energy are 20 keV. Due to gate first process the source/drain region will be self-align. After implantation, we deposited 1000 Å SiO_2 for capping layer by PECVD to prevent dopant out-diffuses during dopant activation. Then, we activated dopant by rapid thermal annealing (RTA) system 600°C 30 second for both Ge n-MOSFET and Ge p-MOSFET. Next, contact hole was defined by third photolithography, followed dry etching the contact hole on source/drain and gate region. 4000 Å Al was deposited by thermal coater and then defined metal pads through fourth photolithography. Finally, 4000 Å Al was deposited as backside contact. The process flow and device structure are shown in **Fig. 4.1** and **Fig. 4.2**.

4.3 Electrical Characteristic of Ge MOSFETs

Fig. 4.3 shows the junction characteristics of Ge p-MOSFET and Ge n-MOSFET. For p^+/n junction, the current density at forward bias and reverse bias are $3.37\text{x}10^{2}$ A/cm^2 at 1 V and $3.87\text{x}10^{-2}$ A/cm^2 at -1 V, respectively. Also, the on/off ratio is about $8.61\text{x}10^{4}$, the ideality factor is 1.255 and the series resistance is 16.2 Ω for p^+/n junction. For n^+/p junction, the current density at forward bias and reverse bias are $1.64\text{x}10^{2}$ A/cm^2 at -1 V and $1.00\text{x}10^{-2}$ A/cm^2 at 1 V, respectively. Also, the on/off ratio is about $1.66\text{x}10^{4}$, the ideality factor is 1.527 and the series is 21.7 Ω for n^+/p junction. The higher current density at reverse bias of germanium device compare to silicon devices is due to smaller bandgap of germanium.

Fig. 4.4 shows I_D-V_G and I_S-V_G characteristics of Ge p-MOSFET and Ge n-MOSFET. For Ge p-MOSFET, the on/off ratio is about $3.98\text{x}10^{4}$ for I_S and $5.32\text{x}10^{3}$ for I_D. For Ge n-MOSFET, the on/off ratio is about $9.33\text{x}10^{4}$ for I_S and $3.02\text{x}10^{3}$ for I_D. The reason why on/off ratio of I_D is always lower than that of I_S is due to small bandgap energy of germanium causes junction leakage. The subthreshold swing of p-MOSFET and n-MOSFET is about 125.8 mV/dec and 130.5 mV/dec, respectively.

Fig. 4.5 shows I_D-V_D characteristics of Ge p-MOSFET and Ge n-MOSFET. At the same overdrive voltage, we can see that p-MOSFET exhibits much larger driving current than n-MOSFET, due to n-MOSFET reveals much larger source/drain resistance than p-MOSFET. As we know, activation of n-type dopant in germanium is a problem which active level of n-type dopant in germanium is much lower than p-type dopant in germanium.

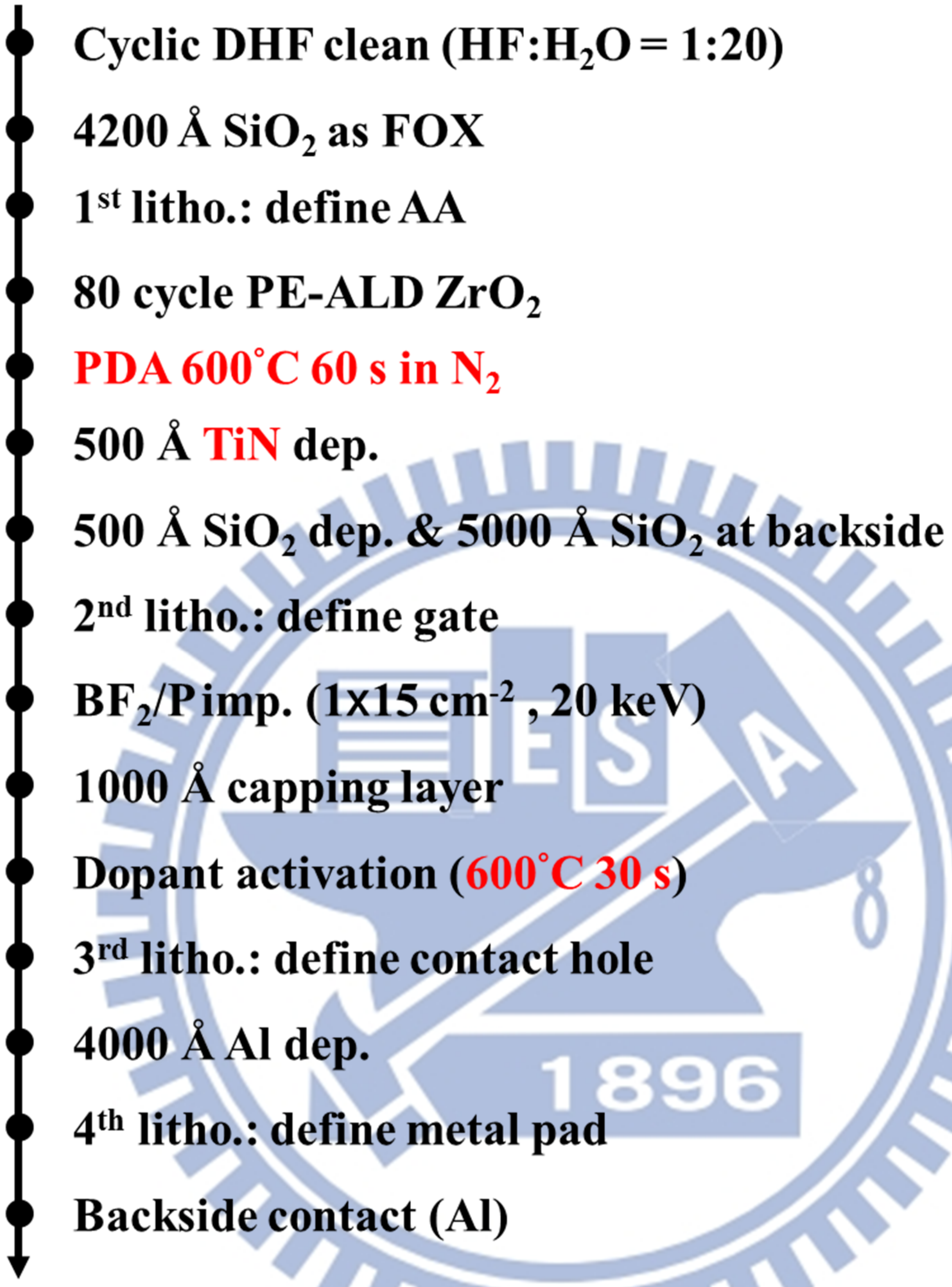
Fig. 4.6 shows the plot of measured resistance versus channel length on mask for Ge p-MOSFET and Ge n-MOSFET. We extract source/drain series resistance (R_{SD}) by Terada and Muta method which we discussed in detail in Chapter 3. By our measurement, the source/drain series resistance is about 50.3 Ω for p-MOSFET and 460.4 Ω for n-MOSFET. Also, $\Delta L=0.52$ μm for p-MOSFET and $\Delta L=0.93$ μm for n-MOSFET.

We use split-CV method which has been discussed in chapter 3 to extract effective mobility. **Fig. 4.7** shows hole mobility as a function inversion charge density for Ge p-MOSFET. The peak hole mobility of p-MOSFET is about 227.4 cm^2/V-s. Here we do not show the electron mobility for Ge n-MOSFET because of the large source/drain series resistance of Ge n-MOSFET. The voltage drop across the source/drain resistance I_DR_{SD} causes a reduction in drain current. Hence, the measured mobility by split C-V method appears to be lower than the real value.

4.4 Conclusion

In Chapter 4, we investigate fabrication and electric characteristics of Ge MOSFETs. For Ge p-MOSFET (the channel width is 200 μm, the channel length is 5 μm), the on /off ratio of p^+/n junction, I_D-V_G and I_S-V_G are about 8.61×10^4, 5.32×10^3, and 3.98×10^4, respectively, while the substhreshold swing is about 125.8 mV/dec. For Ge n-MOSFET (the channel width is 200 μm, the channel length is 5 μm), the on /off ratio of n^+/p junction, I_D-V_G and I_S-V_G are about 1.66×10^4, 3.02×10^3, and 9.33×10^4, respectively, while the substhreshold swing is about 130.5 mV/dec.

From I_D-V_D curve we can see that Ge n-MOSFET reveals poor driving current than Ge p-MOSFET at the same overdrive voltage due to n-type dopant in germanium is much easier diffuse than p-type dopant in germanium. Also, the activation level of n-type dopant in germanium is lower than p-type dopant in germanium. Because of these problems, Ge n-MOSFETs always exhibit poor performance than Ge p-MOSFETs.



- Cyclic DHF clean (HF:H_2O = 1:20)
- 4200 Å SiO_2 as FOX
- 1st litho.: define AA
- 80 cycle PE-ALD ZrO_2
- PDA 600˚C 60 s in N_2
- 500 Å TiN dep.
- 500 Å SiO_2 dep. & 5000 Å SiO_2 at backside
- 2nd litho.: define gate
- BF_2/P imp. (1x15 cm^{-2} , 20 keV)
- 1000 Å capping layer
- Dopant activation (600˚C 30 s)
- 3rd litho.: define contact hole
- 4000 Å Al dep.
- 4th litho.: define metal pad
- Backside contact (Al)

Fig. 4.1 Process flow of Ge MOSFETs.

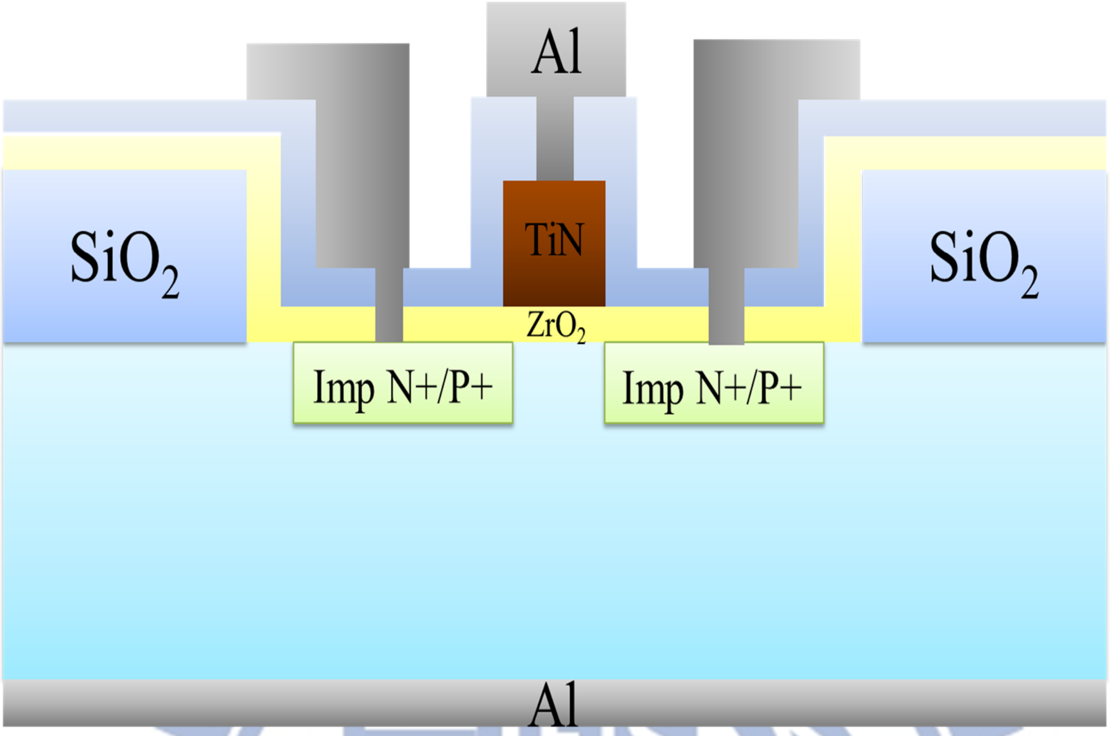
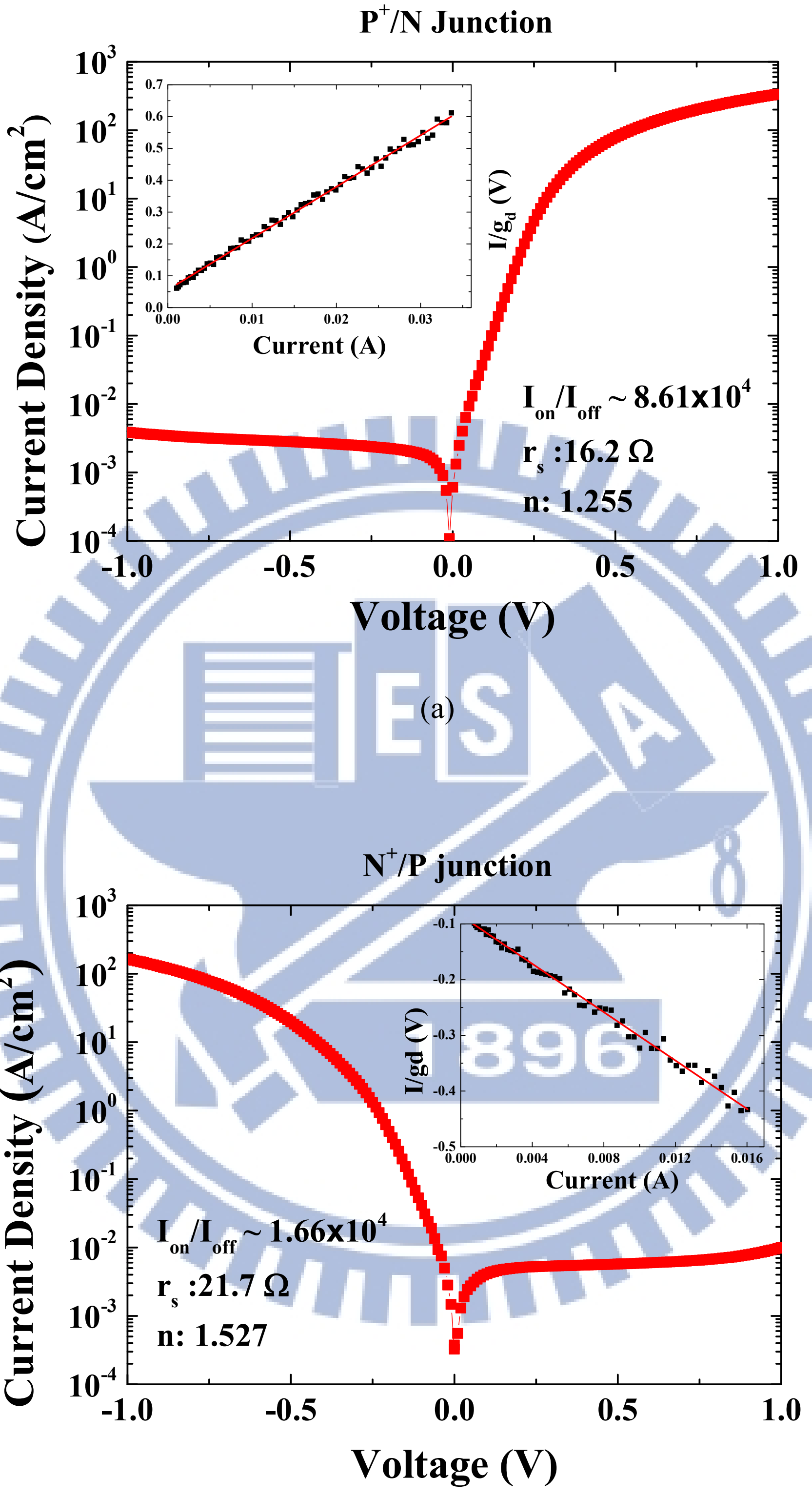


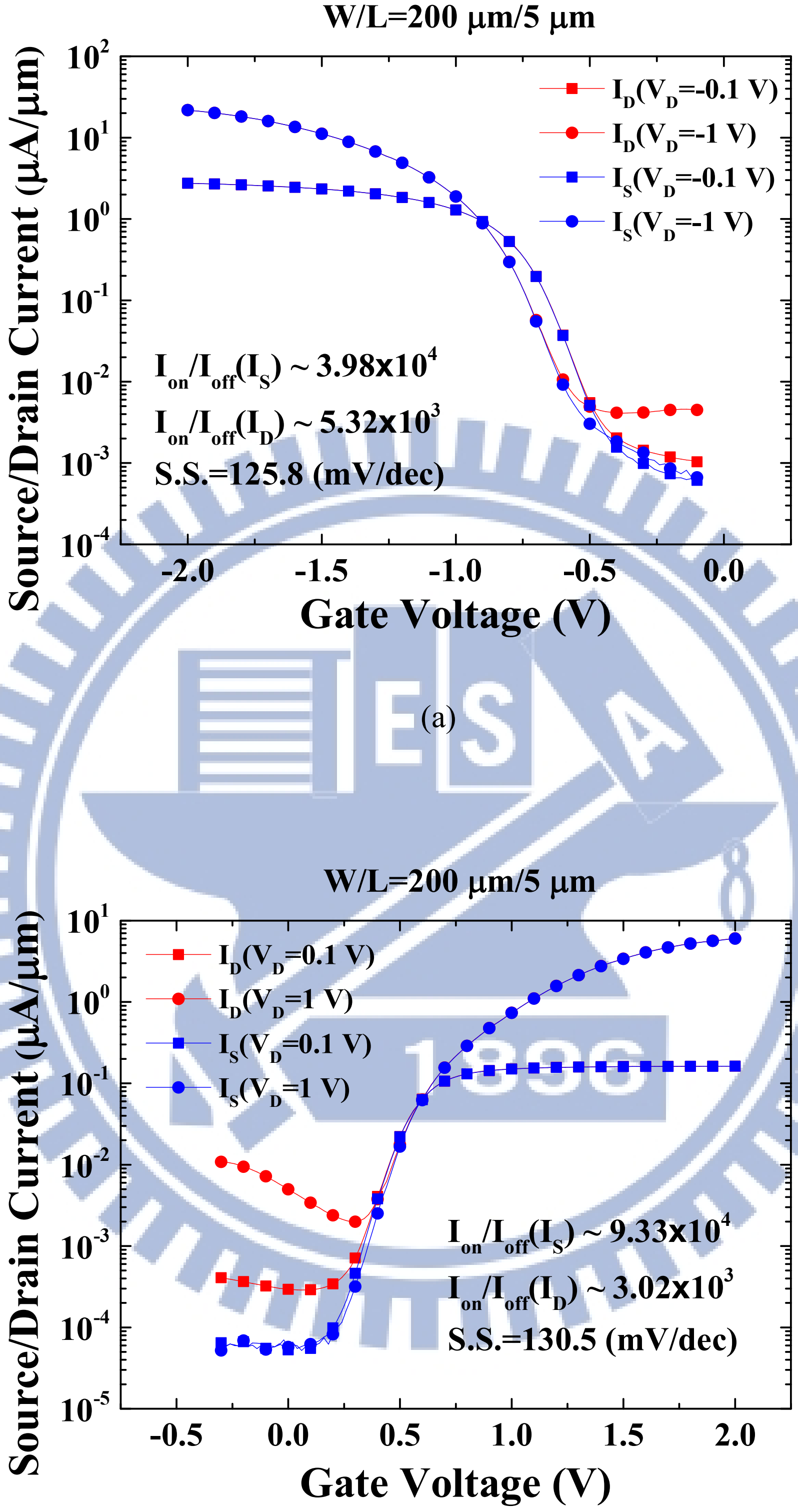
Fig. 4.2 Device structure of Ge MOSFETs.



(a)

(b)

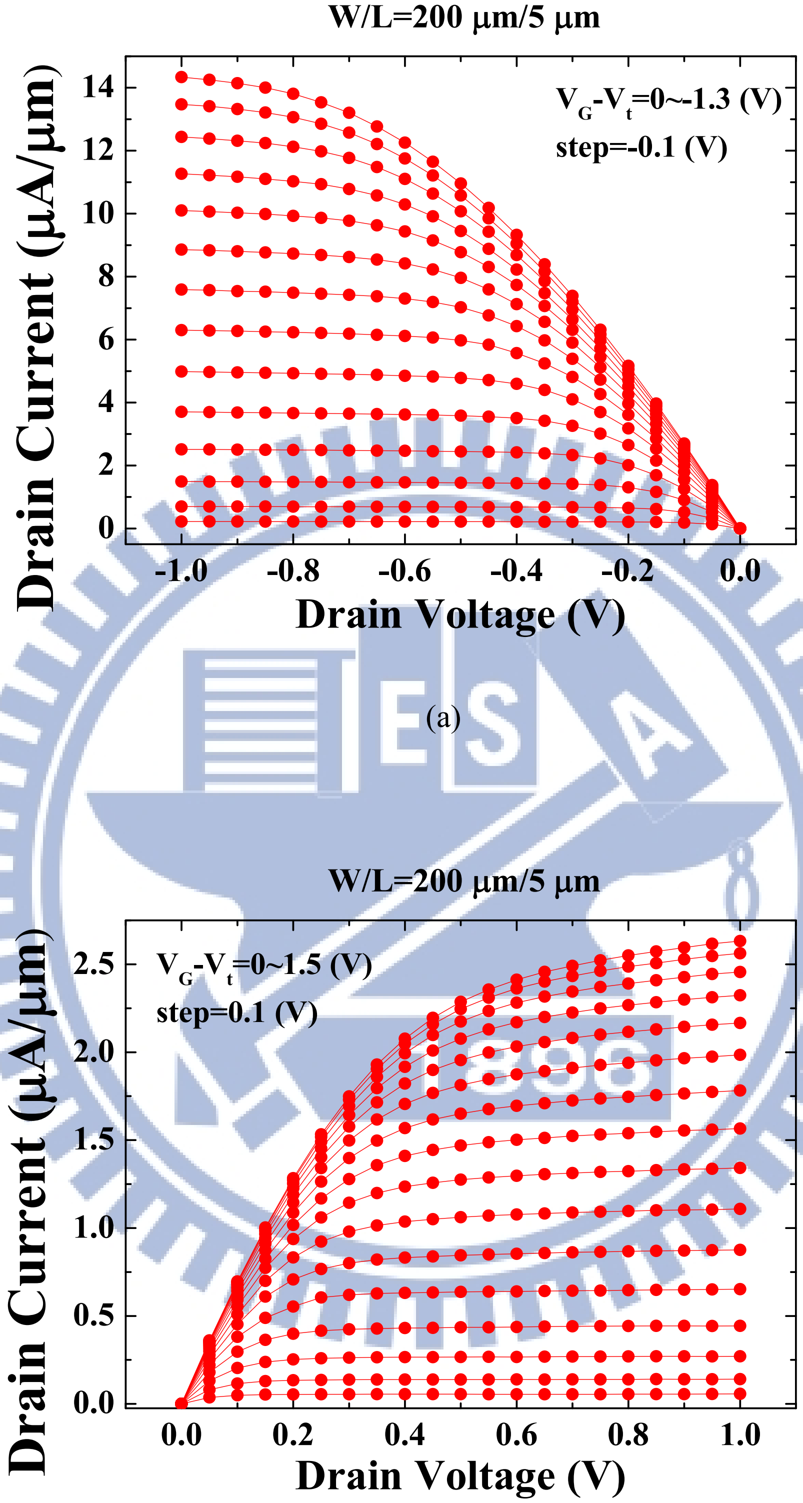
Fig. 4.3 I–V characteristics of $p^{+/}n$ and $n^{+/}p$ junctions; (a) $p^{+/}n$ junction, and (b) $n^{+/}p$ junction.



(a)

(b)

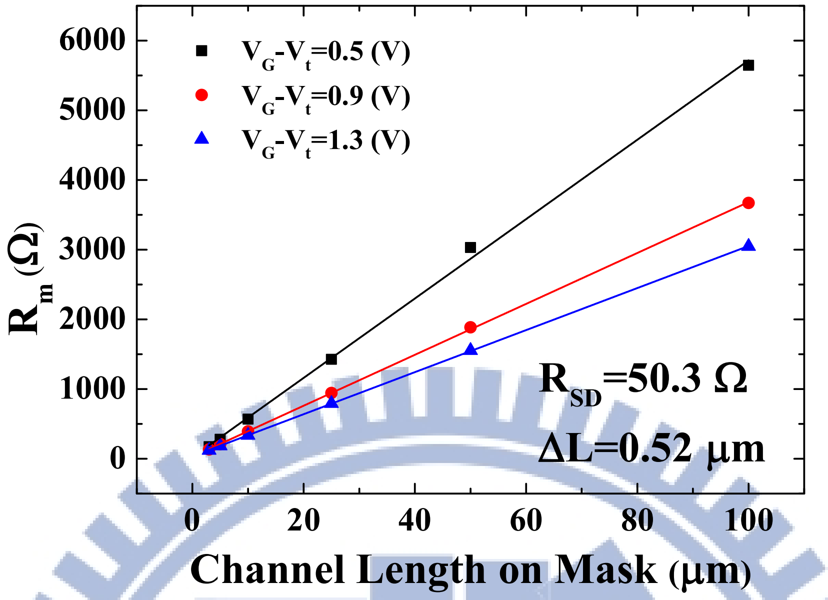
Fig. 4.4 I_D-V_G and I_S-V_G characteristic of Ge MOSFETs; (a) Ge p-MOSFET, and (b) Ge n-MOSFET.



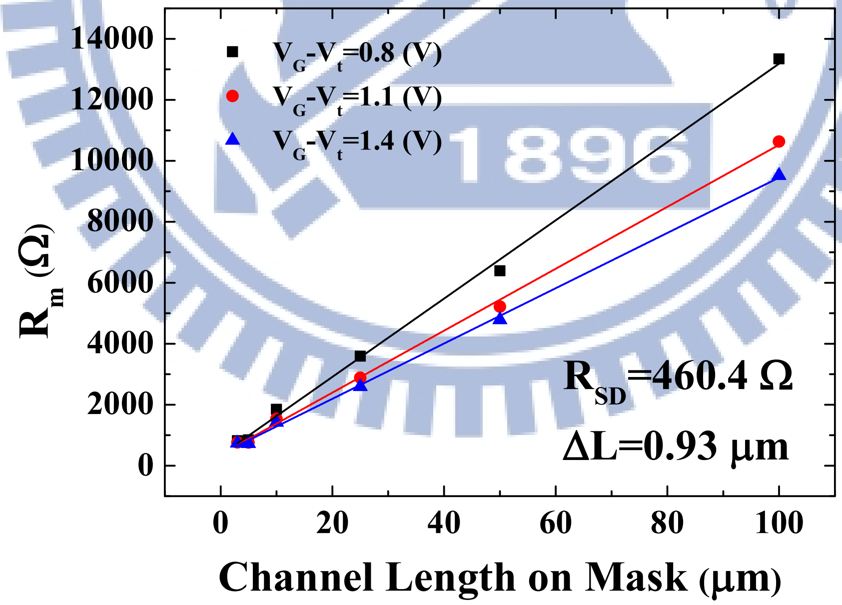
(a)

(b)

Fig. 4.5 I_D-V_D characteristics of Ge MOSFETs; (a) Ge p-MOSFET, and (b) Ge n-MOSFET.



(a)



(b)

Fig. 4.6 R_m versus L as a function of gate voltage to extract series resistance; (a) Ge p-MOSFET, and (b) Ge n-MOSFET.

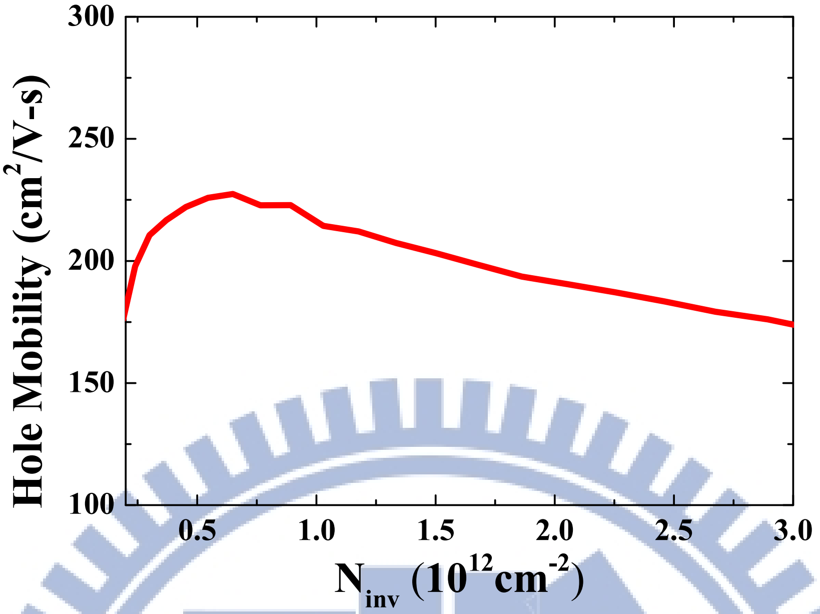


Fig. 4.7 Hole mobility as a function of inversion charge density for Ge p-MOSFET.

Chapter 5

Conclusion

5.1 Comparison between Gate-last and Gate-first MOSFETs

Table 5.1 shows the comparison of Ge p-MOSFETs using gate last process and gate first process. **Table 5.1 (a)** shows junction characteristics of Ge p-MOSFETs. We can see that on current of p^+/n junction using gate first scheme is about 5 times higher than that of p^+/n junction using gate last scheme. Because of dopant activation caused by the last high temperature step in the gate first process, less dopant out-diffuse results in lower junction series resistance. The off current of p^+/n junction using gate first scheme is almost the same compared to that of p^+/n junction using gate last scheme. Therefore, on/off ratio of junction using gate first scheme is higher than that of junction using gate last junction. From **Table 5.1 (b) & (c)**, because of the source/drain resistance of gate first p-MOSFET is 3 times smaller than gate last p-MOSFET (the source/drain resistance has been normalized), we see that driving current for gate first p-MOSFET is a little higher than gate last p-MOSFET. **Fig. 5.1** shows the channel surface of gate last MOSFET and gate first MOSFET. We can see that the channel surface of gate last MOSFET is much rough than gate first MOSFET, so the mobility degrades fast at high electric field for gate last MOSFET compared to gate first MOSFET.

Table 5.2 shows the comparison of Ge n-MOSFETs using gate last process and gate first process. **Table 5.2 (a)** shows junction characteristics of Ge n-MOSFETs. We can see that on current of n^+/p junction using gate first scheme is about 3.2 times higher than that of n^+/p junction using gate last scheme. Because of dopant activation caused by the last high temperature step in the gate first process, less dopant out-diffuse results in lower junction series resistance. The off current of n^+/p junction using gate first scheme is about 30 times higher than that of n^+/p junction using gate last scheme. The reason is that the thermal budget is not enough to activate phosphorous during dopant activation for gate first process. From **Table 5.2 (b) & (c)**, the source/drain resistance of gate first n-MOSFET is 2.1 times smaller than gate last n-MOSFET (the source/drain resistance has been normalized), however, we see that driving current for gate first n-MOSFET is a little lower than gate last n-MOSFET. The reason may be the effective channel length of gate first n-MOSFET is longer than gate last n-MOSFET.

5.2 Conclusion

In this thesis, ZrO_2 film has been obtained by PE-ALD growth with an interfacial GeO_x layer for Ge MOS capacitors. The dependence of ALD ZrO_2 growth temperature and post deposition annealing (PDA) temperature were investigated. D_{it} distribution was also measured by conductance method. The Ge *3d* XPS spectra with different treatment such as as-deposited, annealing at 500°C and annealing at 600°C are shown. With increasing annealing temperature, germanium suboxide will also increase. Therefore, we think more germanium suboxide can improve ZrO_2/Ge interface. We chose PE-ALD ZrO_2 at 250°C and then annealing at 600°C for one minute in N_2 ambient to be the optimized condition to fabricate Ge-MOSFETs.

We have successfully fabricated Ge MOSFETs using gate last process. For Ge p-MOSFET, the on/off ratio of p^+/n junction is 1.66×10^4, on/off ratio of I_D is 2.92×10^3, the subthreshold swing is 119.1 mV/dec, the source/drain resistance is about 365.2 Ω and the peak hole mobility is 259.6 $cm^2/V\text{-}s$. For Ge n-MOSFET, the on/off ratio of n^+/p junction is 1.51×10^5, the on/off ratio of I_D is 1.73×10^4, the subthreshold swing is 112.5 mV/dec and the source/drain resistance is about 1965.4 Ω.

Ge MOSFETs using gate first process were also successfully fabricated. For Ge p-MOSFET, the on/off ratio of p^+/n junction is 8.61×10^4, the on/off ratio of I_D is 5.32×10^3 the subthreshold swing is 125.1 mV/dec, the source/drain resistance is about 50.3 Ω and the peak hole mobility is 227.4 cm^2/V-s. For Ge n-MOSFET, the on/off ratio of n^+/p junction is 1.66×10^4, the on/off ratio of I_D is 3.02×10^3, the subthreshold swing is 130.5 mV/dec and the source/drain resistance is about 460.4 Ω.

Finally, the comparison of gate last MOSFETs and gate first MOSFETs were discussed. We conclude that using gate first scheme can reduce source/drain resistance effectively.

Table 5.1 Comparison of Ge p-MOSFETs between the gate last and the gate first processes.

Ge p-MOSFETs :

Junction	On current (A/cm^2)	Off current (A/cm^2)	On/Off ratio	Series Resistance(Ω)	Ideality factor
Gate last	6.58×10^{1}	3.93×10^{-3}	1.66×10^{4}	59.4	1.262
Gate first	3.37×10^{2}	3.87×10^{-3}	8.61×10^{4}	16.2	1.255

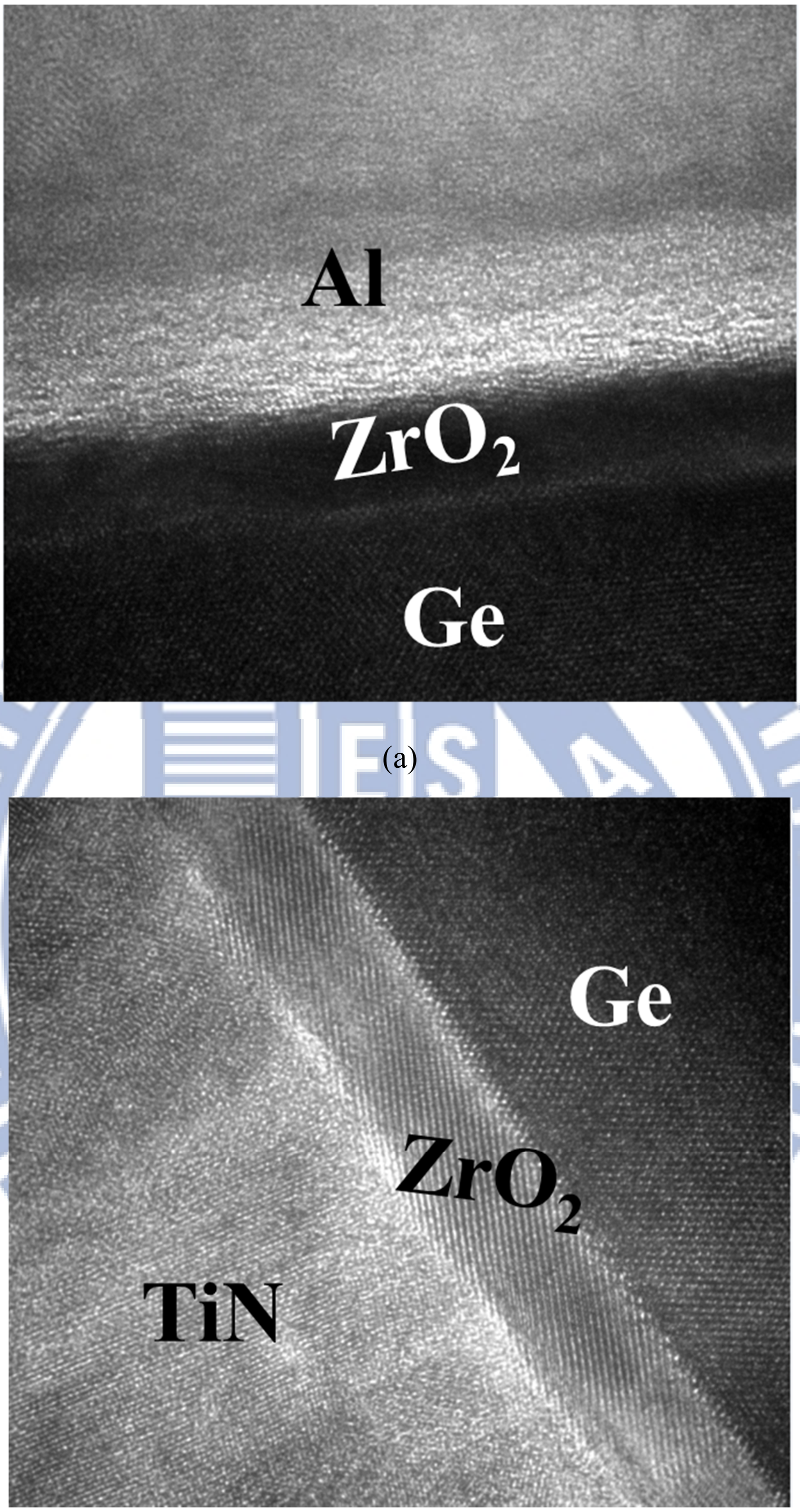
(a)

MOSFET	$I_{D,on}$($\mu A/\mu m$) @V_D= -1 V	$I_{D,off}$($\mu A/\mu m$) @V_D= -1 V	On/off ratio
Gate last	1.32×10^{1}	4.52×10^{-3}	2.92×10^{3}
Gate first	2.18×10^{1}	4.18×10^{-3}	5.32×10^{3}

(b)

MOSFET	S.S(mV/dec)	R_{SD}($\Omega \cdot mm$)	ΔL(μm)
Gate last	119.1	36.52	0.75
Gate first	125.8	10.06	0.52

(c)



(a)

(b)

Fig. 5.1 TEM image of Ge p-MOSFET; (a) gate last MOSFET, and (b) gate first MOSFET.

Table 5.2 Comparison of Ge n-MOSFETs between the gate last and the gate first processes.

Ge n-MOSFETs :

Junction	On current (A/cm^2)	Off current (A/cm^2)	On/Off ratio	Series Resistance(Ω)	Ideality factor
Gate last	$5.06x10^1$	$3.29x10^{-4}$	$1.51x10^5$	47.7	1.512
Gate first	$1.64x10^2$	$1.00x10^{-2}$	$1.66x10^4$	21.7	1.527

(a)

MOSFET	$I_{D,on}$(μA/μm) @V_D= 1 V	$I_{D,off}$(μA/μm) @V_D= 1 V	On/off ratio
Gate last	9.74	$5.63x10^{-4}$	$1.73x10^4$
Gate first	6.01	$2.06x10^{-3}$	$2.92x10^3$

(b)

MOSFET	S.S(mV/dec)	R_{SD}(Ω·mm)	ΔL(μm)
Gate last	112.5	196.54	1.75
Gate first	130.5	92.08	0.93

(c)

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Chapter 4:

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碩士論文題目:

在鍺通道金氧半場效電晶體上製造閘極介電層二氧化鋯/鍺堆疊結構之研究

Investigation of of ZrO$_2$/Ge Gate Stack Fabricated on Ge-Channel MOSFETs