國立交通大學

材料科學與工程學系

碩士論文

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元件能隙工程與遲滯效應

Advanced InAs Quantum Well MOSFET:
Device Bandgap Engineering and Hysteresis Effect

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摘 要

本研究著重於兩個關於砷化銦金氧半場效電晶體的重要議題:砷化銦複合通道 (InGaAs/ InAs/ InGaAs) 之能隙工程與介面能態所引致的遲滯現象之研究。

關於元件能隙工程,吾人首先藉數值模擬以探究元件磊晶結構對載子侷限能力和遷移率的影響。吾人亦探討幾種用於元件製作及量測的磊晶結構。透過實驗結果之驗證,吾人發現複合通道厚度及次通道銦含量之極佳化有益於元件電流之提升與短通道效應之抑制。

關於遲滯效應，吾人探究遲滯現象之物理原因及其對偏壓變化之相依性。吾人提出一個物理機制以解釋遲滯現象中的閥值電壓偏移,此機制亦可藉實驗結果驗證。吾人藉著推導出之方程式，研究遲滯現象對不同的偏壓變化之相依性。另外,吾人亦提出一種萃取電晶體介面能態的方法。此法免如傳統方法般使用 MOS 電容，可評估電晶體閘極堆疊結構之介面性質。

此外，吾人推導幾個關於砷化銦量子井場效電晶體的物理模型，如閥值電壓及閘極電容，以對元件電性有綜覽性之理解。

關鍵詞：　先進金氧半場效電晶體、砷化銦量子井金氧半場效電晶體、
元件能隙工程、遲滯效應、高介電常數閘極介電質/金屬閘極、
閥值電壓不穩定性

Advanced InAs Quantum Well MOSFET:
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ABSTRACT

This thesis focuses on two important issues in InAs quantum well MOSFETs: the bandgap engineering of the InGaAs/InAs/InGaAs composite channel as well as the hysteresis phenomena incurred by the interface states at the high-*k*/semiconductor interface.

With respect to the device bandgap engineering, the influence of device epitaxial structures on carrier confinement and apparent mobility was firstly investigated by numerical simulations. The epitaxial structures used for the fabrication and characterization of the devices were introduced and reviewed. Through experimental verification, we found that optimized composite channel thickness and sub-channel indium (In) composition are beneficial to the drive current and the suppression of short channel effects.

With respect to the hysteresis effect, we explored the physics origin and the bias dependences of hysteresis phenomena. A mechanism was proposed to explain the threshold voltage shift in hysteresis phenomena, and it was verified by experimental results. Various bias dependences were also studied and emphasized by using the derived equations. In addition, we also proposed a new method to extract the interface state density of the transistor without using MOS capacitor like conventional methods. The proposed method was able to evaluate the interface properties of the gate stack of MOS transistors.

In addition, the physical models for the threshold voltage and gate capacitance of InAs quantum well MOSFETs were developed in order to have a understanding of the electrical behaviors of devices.

Keywords: Advanced MOSFET, InAs Quantum Well MOSFET,
Bandgap Engineering, Hysteresis Effect,
High-*k* Gate Dielectric/Metal Gate, Threshold Voltage Instability

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韶光荏苒，匆匆又過了幾個寒暑。回顧在新竹的日子，平庸如我，無非是憑著貴人相助和好運氣方能一步步走到這裡的。

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LIST OF SYMBOLS

C	capacitance/area in MOS (F/cm^2)
C_G	gate capacitance/area (F/cm^2)
C_{OX}	gate oxide capacitance/ area (F/cm^2)
C_d	depletion capacitance/ area (F/cm^2)
C_{ins}	insulator capacitance/ area (F/cm^2)
C_{it},	interface-state capacitance/ area (F/cm^2)
$C_{centroid}$	centroid capacitance/ area (F/cm^2)
C_Q	quantum capacitance/ area (F/cm^2)
D	electrical flux density (C/m^2)
D_{it}	interface-state density (cm^{-2}eV^{-1})
D, G, S	drain, gate, source of an FET
E_c, E_v	conduction band, valence band edge (J, eV)
E_F	equilibrium Fermi level (J, eV)
E_0	charge neutral level (J, eV)
f(E)	Fermi-Dirac distribution function
g_m	mutual transconductance in an FET (S)
I_D	channel current in an FET, direction from drain to source (A)
I_G	gate current in an FET (A)
k	Boltzmann constant (J/K, eV/K)
k	wave vector (cm^{-1})
L_g	gate length in an FET (m)
m_n*, m_p*	effective mass for electrons, holes (kg)
m_0	rest mass of electrons (kg)
N_{it}	effective (net) charge density/area (/cm^2)
q	magnitude of the electronic charge (C)
Q_+, Q_-	total positive, negative charge (C)
Q_f	oxide fixed charge/area (C/cm^2)
Q_{it}	interface trap charge/area (C/cm^2)
Q_m	mobile ionic charge/area (C/cm^2)
R	resistance (ohm)
SS	subthreshold swing/slope (mV/decade)
T	temperature (K)
V	voltage (V)
V_D, V_G	voltage from drain to source, gate to source in an FET (V)

V_T	threshold voltage (V)
V_{th}	thermal voltage (V)
W_g	gate width in an FET (m)
$Z_{centroid}$	centroid distance (m)

Chapter 1
Introduction

1.1 General Background

Semiconductor quantum heterostructures have drawn a great deal of attention of scientists and engineers in the fields of solid-state physics, materials science, and electronics. Engineered heterostructures not only incorporate new transport properties and device operation principles into the emerging transistor technologies, but also pave the way for future low-power and high-performance complementary metal-oxide-semiconductor (CMOS) technology through this approach: III-V MOSFET.

Driven by the Moore's law, Si MOSFETs have dominated the CMOS technology for over three decades with the advance of lithography technology. However, scaling of deep submicron MOS transistors encountered difficulties in device engineering, including short channel effects (SCEs) [1], degraded mobility [2], random dopant fluctuation (RDF) [3], and random telegraph noise (RTN) [4]. Improved electrostatic control had been realized though device body engineering and new device architectures, such as ultra-shallow junction [5], retrograde doping [6], raised source-drain [7], FinFET [8] and ultra-thin body silicon-on insulator (UTB-SOI) [9]. Moreover, partially/fully depleted devices [10] with lightly-doped/no-dopant channel are expected to be a feasible solution to get rid of the RDF. Regarding the mobility degradation, strained Si technology has been demonstrated in industrial products. However, stress engineering approaches its limit since the injection velocity of Si is insufficient to meet the requirements of sub-10 nm MOS transistors. Advanced MOSFET technology utilizing III-Vs and/or Ge channels emerges as the promising candidates for nano-scale low-power and high-performance MOSFETs. The strength of III-V-based channel comes not only from their superior transport properties that strained-Si cannot achieve, but also from the art of device bandgap engineering.

III-V materials' low effective mass and hence high carrier velocity enable the transistors to perform high drain current (I_D), impressive transconductance (g_m), and short gate delay at low supply voltage (V_{DD}). Scaling V_{DD} without the expense of device performance is essential to the present and future CMOS technology. The V_{DD} scaling is beneficial to the hot carrier effects and the power consumption, since the power consumption of a MOSFET is given by $P = 0.5\ C_i \times V_{DD}^2$, where C_i is the gate capacitance. Lower V_{DD} represents less power consumption and prevents the devices from some reliability issues. There are two momentums that accelerate the pursuing of high-mobility channel materials. The first one is: the ballistic transport and velocity saturation phenomena in nano-scale MOSFETs make the I_D and g_m depend on carrier velocity instead of gate length (L_g) as the L_g below 100 nm [1]. The second one is: the surface-channel Si MOSFETs suffer from severe surface scattering at oxide/semiconductor interface during device scaling, due to large transverse electrical field. In the perspective of the improvement in mobility and injection velocity, $In_xGa_{1-x}As$ with In composition of 53% and above as well as InAs were taken into consideration by the International Roadmap Committee [11]. Even though low effective mass leads to high carrier velocity, but its drawback — low density of state (DOS) has to be taken into considerations. Low DOS leads to the lower sheet electron concentration in channel, so the transistor requires more gate overdrive (V_G - V_T) to sustain available carriers. Fig. 1.1 shows the electron injection velocity at virtual source in InAs and InGaAs quantum well field effect transistors (QW-FETs) as a function of L_g at supply voltage V_{DD} = 0.5V [12]. It is apparent that III-V-based materials are suitable candidates for n-channel MOSFETs.

In addition to high carrier velocity, the flexibility of bandgap engineering has been proven in various heterostructure transistors, such as high electron mobility transistor (HEMT) (i.e., QW-FET) [13], III-V FinFET [14], III-V UTB MOSFET [15] and III-V tunneling FET (TFET) [16]. The essence of bandgap engineering is, according to the specific application, one can design and adjust the materials, composition, and thickness of each layer in the heterostructure, so as to optimize the required device performance. Take HEMT as an example, composite channel [17] has been used to enhance the carrier mobility and the carrier confinement, leading to improved g_m as well as current gain cut-off frequency (f_T). Furthermore, the HEMT with thin composite channel [18] have demonstrated record f_T of ~710 GHz by National Chiao Tung University, Taiwan in 2013. Another example is the vertical heterostructure TFET [19] proposed and fabricated by Intel Corporation in 2011. The inserted thin $In_{0.7}Ga_{0.3}As$ layer served as a smaller tunneling barrier, which drastically increased the drive current. These two examples illustrated the physics and technology of the bandgap engineering in III-V FETs.

Indeed, III-V MOSFET requires both pertinent gate dielectrics and good gate-dielectric/semiconductor interface. Unlike Si, III-Vs are lack of high-quality native oxide, which makes Si as the mainstream ULSI technology. In recent years, atomic layer deposition (ALD) realizes the deposition of high-*k* dielectrics on III-V materials along with the capability of ultra-thin interfacial layer to reduce interface state density (D_{it}) and gate leakage. Associated with the study of interfacial layer, various surface treatments are also proposed to passivate the interface states. Even though the researches on passivation techniques are under development, ALD technology has opened up a frontier field in III-V FET researches.

Regarding the device engineering, a controversial issue lies in the device architecture of III-V MOSFET: surface channel or buried channel. Surface channel devices provide better gate modulation through the reduced gate-to-channel distance and higher gate capacitance, but III-V's relatively higher D_{it} will make the device suffer from scattering and degraded subthreshold behaviors. In contrast, buried channel ensures better high-*k*/semiconductor interface by using appropriate gate stack (e.g., Al_2O_3/InP and $TaSiO_x$/InP), in which drastically reduced D_{it} preserves the high mobility essence of III-V materials. However, the corresponding side effect is the increased gate-to-channel distance, which makes the buried channel device prone to the short channel effects. In short, the choosing of surface channel or buried channel is a trade-off between gate modulation and mobility.

To sum up, the combination of III-V nMOS and Ge pMOS on Si platform is the ultimate scenario in the foreseeable future, if the following difficulties can be overcomed: 1) optimized logic performance through device bandgap engineering, 2) good high-*k* dielectric/semiconductor interface with D_{it} in the order of 10^{11} $cm^{-2}eV^{-1}$, 3) low resistive, refractory, and gold-free source/drain (S/D) contact, and 4) III-Vs/Ge on Si epitaxy technology, which is the corner stone of heterogeneous integration.

1.2 Motivations

Although many works had used $In_xGa_{1-x}As/InAs/In_xGa_{1-x}As$ composite channel structure in HEMTs/QW-FETs and QW-MOSFETs, there is no complete research on the bandgap engineering of InAs composite channels. Based on the flexibility of composite channel, device performance can be optimized for different applications. In this work, the logic characteristics of composite channel QW-MOSFETs are emphasized because of the emerging of III-V MOS transistors in sub-10 nm regime. Furthermore, InAs composite channel QW-MOSFETs requires appropriate physical models to describe the fundamental electrical properties, such as threshold voltage (V_T) and gate capacitance (C_G). The derived equations help us to look into the basic electrical behaviors, and to have an in-depth understanding on hysteresis phenomena.

1.3 Thesis Outline

The objective of this dissertation is two-fold: 1) to deliver a comprehensive study on the bandgap engineering of composite channel for future low-power and high-performance logic application and 2) to examine the physical origin and bias dependence of the hysteresis effect based on the derived models.

In Chapter 2, the literature review starts from the InAs composite channel and its applications in HEMTs. Then the disadvantages of HEMT are discussed. Finally, the InAs FETs with insulated gate are introduced and reviewed.

In Chapter 3, the process and characterization of InAs composite channel QW-MOSFETs are introduced. The metrology methods for DC and RF characterization are also briefly described. This chapter serves as the research methodology of this work.

In Chapter 4, the investigation of bandgap engineering of InAs composite channel is conducted through both theoretical and experimental approaches. In the beginning, the influence of epitaxial structures on device performance is examined by numerical device simulations. The experimental studies were also performed. InAs QW-MOSFETs with three kinds of epitaxial structures were fabricated and characterized. It was found that the devices with inverted thin channel structure exhibit the best logic and microwave characteristics under low-power operation conditions.

In Chapter 5, the mechanism of the hysteresis phenomena and the bias dependence are explored. The trapping/de-trapping of the acceptor-like interface states at high-*k*/semiconductor interface has proven to be directly related to the hysteresis effect through electrical analysis. Moreover, a new extraction method is proposed to evaluate the D_{it} of MOS transistors.

In Chapter 6, the conclusions of this dissertation are drawn.

In the Appendix, analytical models developed to describe the threshold voltage (V_T) and gate capacitance (C_G) are presented. Based on the V_T and C_G models, the current-voltage (I-V) characteristics are then derived in an analog fashion to the well-developed MOSFET equations. The derived models provide a fundamental understanding on the electrical behaviors of devices. Moreover, the V_T model can also be used to analyze the hysteresis effect.

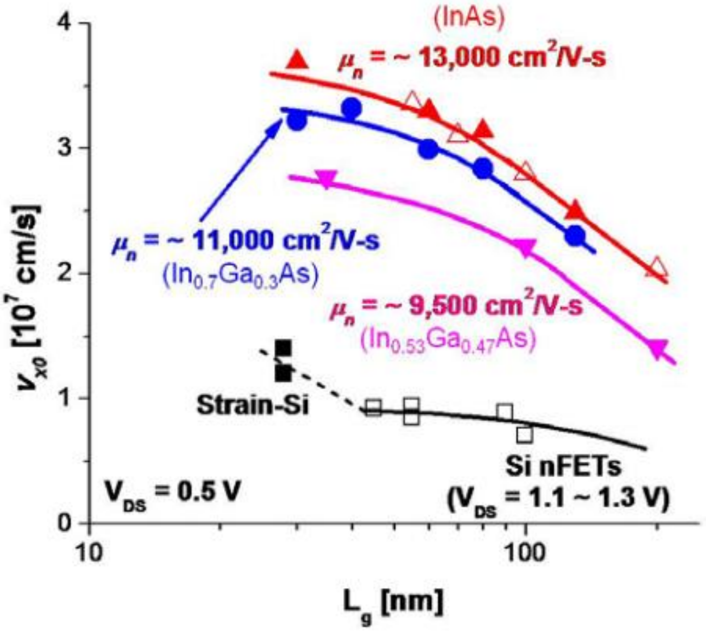

Fig. 1.1 The electron injection velocity at virtual source in InAs and InGaAs HEMTs/QW-FETs as a function of gate length at supply voltage V_{DD} = 0.5 V. (Figure taken from Alamo *et al.* [12])

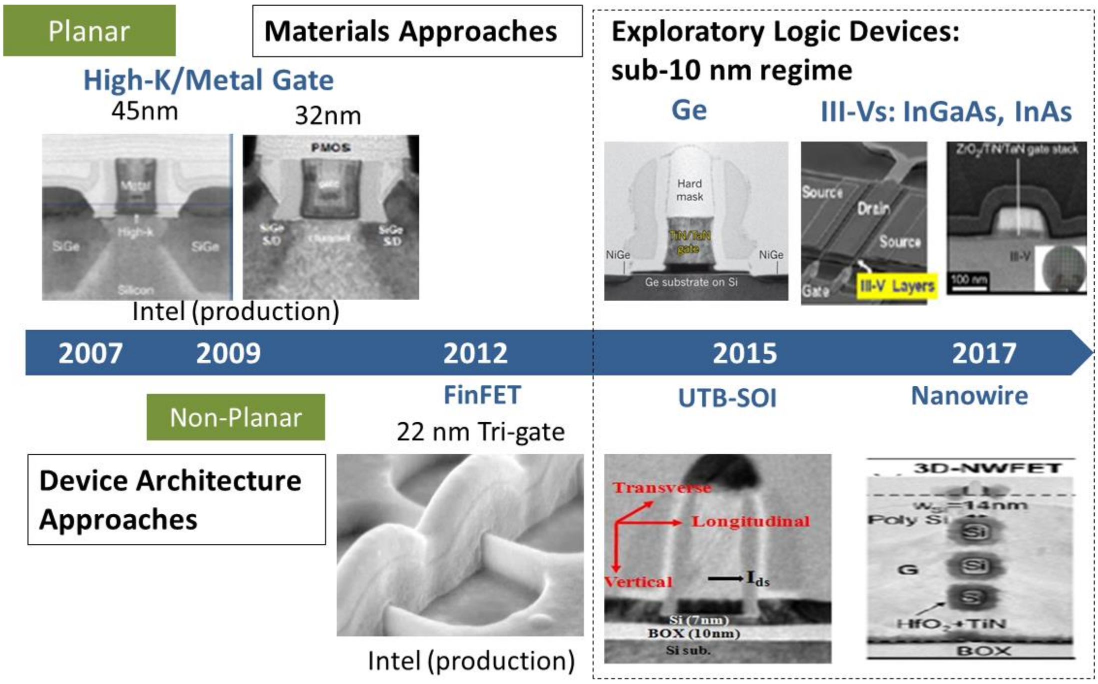

Fig. 1.2 Advanced and emerging device technology. The paradigm shift of transistor technology comes from the combination of new materials and new device architectures.

Chapter 2

Literature Review

2.1 $In_xGa_{1-x}As/InAs/In_xGa_{1-x}As$ Composite Channel and Its Applications in High Electron Mobility Transistors

Applying InAs channel to FETs is not a new technology. InAs FETs are often accompanied with composite channel, in which InAs channel is sandwiched by upper and lower cladding InGaAs sub-channels. The main purposes include: 1) the accommodation of lattice mismatch; 2) lowered interface free energy, which yields smoother interface and prevents the formation of defects such as misfit dislocations; 3) better carrier confinement, which is obtained through the $In_xGa_{1-x}As/InAs/In_xGa_{1-x}As$ heterostructure.

Due to the excellent transport properties and enhanced carrier confinement of InAs composite channel, Nakayama *et al.* [17] demonstrated extraordinary electron mobility of 18,300 $cm^2V^{-1}s^{-1}$ by using 1-nm $In_{0.53}Ga_{0.47}As$/ 2-nm $In_{0.8}Ga_{0.2}As$/ 4-nm InAs/ 4-nm $In_{0.8}Ga_{0.2}As$/ 9-nm $In_{0.53}Ga_{0.47}As$ configuration, as shown in Fig. 2.1. The inserted $In_{0.8}Ga_{0.2}As$ layer between InAs and $In_{0.53}Ga_{0.47}As$ reduces the interface free energy since the surface energy for $In_{0.53}Ga_{0.47}As$/InAs is higher than $In_{0.8}Ga_{0.2}As$/InAs. The streak RHEED pattern confirms the smoother interface.

With respect to the design of InAs composite channel, the key parameters that determine device performance can be categorized into two subjects: 1) the thickness of the InAs-core and InGaAs sub-channels; 2) the In composition of the cladding InGaAs sub-channels.

Regarding the thickness optimization of the upper sub-channel, Akazaki *et al.* [20] optimized the thickness of the upper cladding $In_{0.53}Ga_{0.47}As$ and the InAs-core at fixed total composite channel thickness of 30 nm. An optimized configuration was achieved by using 2.5-nm $In_{0.53}Ga_{0.47}As$/ 4-nm InAs/ 23.5-nm $In_{0.53}Ga_{0.47}As$ composite channel, which leads to the electron mobility of 12,800 $cm^2V^{-1}s^{-1}$. The HEMT using this configuration with 0.6×150 μm^2 gate exhibits f_T of 58.1 GHz.

Regarding the thickness of upper and lower InGaAs layers, Lange *et al.* [21]

made comparisons of $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ with two kinds of sub-channel configurations at fixed upper sub-channel thickness: t_{InGaAs}(upper) = t_{InGaAs}(lower) and t_{InGaAs}(upper) < t_{InGaAs}(lower), where the t_{InGaAs}(upper) and t_{InGaAs}(lower) stand for the upper and lower sub-channels, respectively. The electron mobility for the structure with thinner lower-clad is 14,800 $cm^2V^{-1}s^{-1}$, while for the thicker one is 15,400 $cm^2V^{-1}s^{-1}$. The HEMT with thicker lower-clad exhibits better DC and RF performance. However, the device with thinner lower-clad has less impact ionization phenomena and suppressed SCEs.

Regarding the optimization of the In composition of lower sub-channel, Xu *et al.* [22] compared the In composition of the lower cladding layer at fixed $In_{0.53}Ga_{0.47}As/InAs/In_xGa_{1-x}As$ thickness of 2/3/7 nm, in which the compared In composition are 0.3 and 0.7. The performance of the device with $In_{0.3}Ga_{0.7}As$ lower sub-channel was better than the $In_{0.7}Ga_{0.3}As$ one. The performance improvement was attributed to the improved carrier confinement caused by the higher potential of $In_{0.3}Ga_{0.7}As$ layer. Moreover, the tensile $In_{0.3}Ga_{0.7}As$ layer is believed to compensate the strong compressive strain in the InAs layer, resulting in a better epitaxial quality of InAs layer.

The optimized composite channel has demonstrated impressive microwave characteristics in HEMTs. In Kim and Alamo's work [23], the heterostructure with 2-nm $In_{0.53}Ga_{0.47}As$/ 5-nm InAs/ 3-nm $In_{0.53}Ga_{0.47}As$ has the electron mobility of 13,200 $cm^2V^{-1}s^{-1}$; and their HEMT exhibits the f_T of 491 GHz. On the other hand, Fatah *et al.* [24] also used the same composite channel configuration to achieve the f_T of 615 GHz. Furthermore, Chang *et al.* [18] demonstrated the record f_T of 710 GHz by incorporating 1-nm $In_{0.7}Ga_{0.3}As$/ 2-nm InAs/ 1-nm $In_{0.7}Ga_{0.3}As$ ultra-thin composite channel and low-resistive $In_{0.65}Ga_{0.35}As$/ $In_{0.53}Ga_{0.47}As$ /$In_{0.52}Al_{0.48}As$ multi-cap, as shown in Fig. 2.2.

Even though those researches on the composite channel in HEMTs demonstrated good result on the RF performance, yet they paid less attention on the logic characteristics such as subthreshold swing (SS) and drain-induced barrier lowering (DIBL). Moreover, a trade-off between device performance and gate leakage exists in the Schottky-gated InAs HEMTs: although device with thin-barrier-layer structure are able to improve both logic and RF performance, the gate leakage is relatively high. This trade-off comes from the Schottky gate, since the gate leakage for Schottky-gated devices is several orders higher than the devices with insulated gate (i.e., Insulated Gate FET, IGFET). Therefore, the InAs transistors with insulated gate are preferred and had been extensively studied in recent years, in order to evaluate its performance and feasibility in ULSI applications.

2.2 InAs Quantum Well MOSFET

Above-mentioned works are HEMTs, which employ Schottky gate instead of the insulated gate. InAs FETs with high-*k* dielectric gate stack is essential to low-power CMOS, since it reduces the static power consumption of the transistors and the entire ICs. As a result, InAs IGFET with engineered quantum heterostructure has attracted much attention in several device-related journals and conferences such as International Electron Device Meeting (IEDM) and Symposium on VLSI Technology (VLSIT).

The primary concern on the InAs MOS transistors is the high-*k*/semiconductor heterointerface. Intel Corporation [25] reported two gate stacks with good interface quality: Al_2O_3/InP and $TaSiO_x$/InP. Both of them represent low frequency dispersion (7%/decade) compared to conventional $Al_2O_3/In_{0.52}Al_{0.48}As$ (27%/decade) gate stack. This result indicates that InP is an ideal material for the high-*k*/III-Vs integration. Moreover, this research may also terminate the debate among surface channel and buried channel. Although surface channel device like [26] are able to achieve high I_D and g_m due to its higher C_G, the poor subthreshold behaviors and frequency dispersion due to high D_{it} is unacceptable for digital applications. Furthermore, the InP layer can also be used as the etch stop layer during the selective removal of heavily-doped cap layer, giving rise to better process control and V_T uniformity [27]. Therefore, using high-*k*/InP as the gate stack is beneficial to ULSI applications.

Finally, three impressive researches on InAs MOS transistors will be reviewed in the following paragraphs.

SEMATECH VLSIT 2012

Kim *et al.* [28] demonstrated the InAs QW-MOSFET with thin InP layer, low D_{it} Al_2O_3/InP gate stack, and optimized modulation doping concentration. The device exhibited peak g_m of 1730 μS/μm, f_T of 245 GHz, and SS of 105 mV/decade at V_D = 0.5 V. The optimized δ-doping concentration of 1×10^{12} cm^{-2} leads to high g_m and good SS since higher concentration limits the charge modulation (Fig. 2.3). The immunity to SCEs is also attributed to the gate stack with minimum D_{it} of 4×10^{12} $cm^{-2}eV^{-1}$.

MIT IEDM 2012

The InAs QW-MOSFETs with L_g = 30 nm and L_g = 22 nm [29] were realized through the CMOS-compatible and self-aligned process, which gives rise to the scaled gate-to-contact distance of 20-30 nm. The device employed the 3-nm $In_{0.7}Ga_{0.3}As$/ 2-nm InAs/ 5-nm $In_{0.7}Ga_{0.3}As$ composite channel, low-resistive Mo contact, and the 2-nm HfO_2 gate dielectric with the EOT less than 1nm. The 30-nm and 22-nm devices exhibit peak g_m of 1420 μS/μm and 1050μS/μm, respectively. The SS of 30-nm device is 114 mV/decade at V_D = 0.5 V.

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Lee *et al.* [30] reported the InAs QW-MOSFET with record extrinsic peak g_m of 2450 μS/μm and excellent I_D of 1950 μA/μm at V_D = 0.5 V. The device consists of regrown S/D, digital etching process, inverted-modulation-doped 5-nm InAs/ 3-nm $In_{0.53}Ga_{0.47}As$ composite channel, and substitution gate process. The device architecture is shown in Fig. 2.4. We can see that the 0.5-nm interfacial layer/ 3.6-nm HfO_2/Ni/Au gate scheme is directly stacked on the InAs composite channel instead of InP layer. As a result, the SS for the 40-nm device is about 400 mV/decade. The epitaxial S/D gives rise to the reduction of parasitic resistance, achieving low on-resistance R_{on} of 214 Ω-μm. The digital etching was conducted to remove the damaged semiconductor surface, which is introduced in the process of epitaxial S/D. As a whole, although this device architecture provided very high I_D and g_m, the poor subthreshold behaviors and low I_{ON}/I_{OFF} still prevents this architecture from CMOS applications.

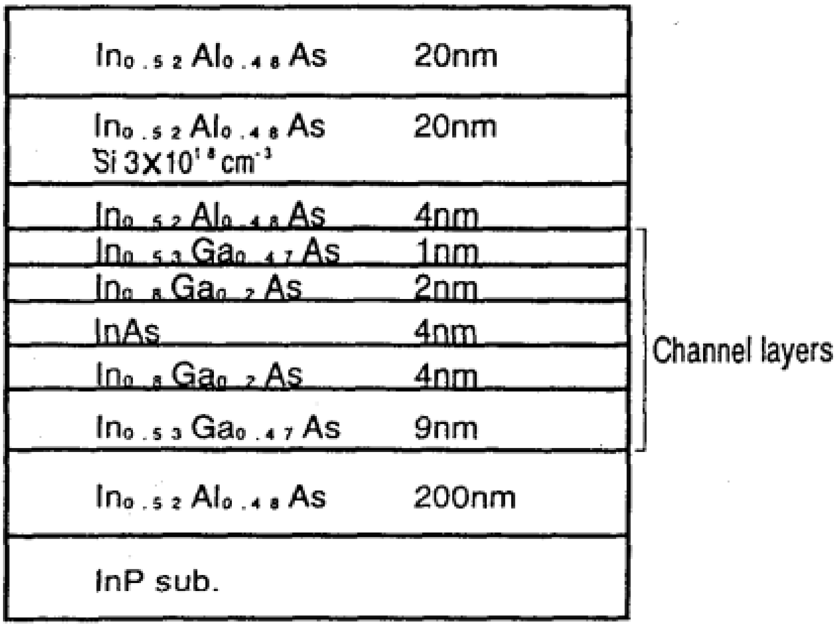


Fig. 2.1 The epitaxial structure consists of $In_{0.53}Ga_{0.47}As$/ $In_{0.8}Ga_{0.2}As$/ InAs/ $In_{0.8}Ga_{0.2}As$/ $In_{0.53}Ga_{0.47}As$ configuration, yielding electron mobility of 18,300 $cm^2V^{-1}s^{-1}$. (Figure taken from Nakayama *et al.* [17])

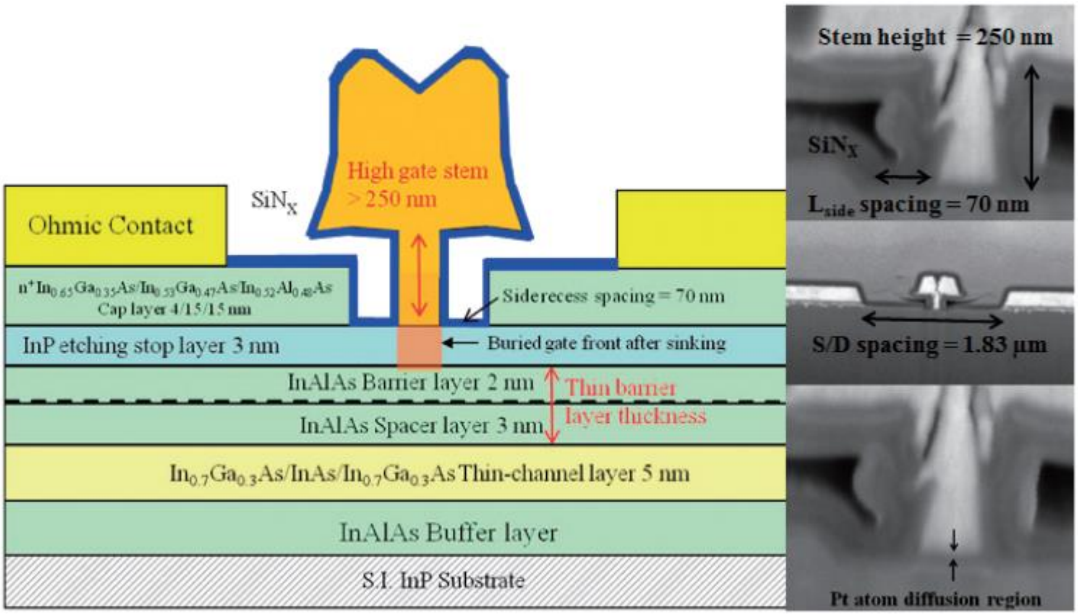


Fig. 2.2 Schematic view of the ultra-thin-channel InAs HEMT structure, which incorporates ultra-thin $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ composite channel. (Figure taken from Chang *et al.* [18])

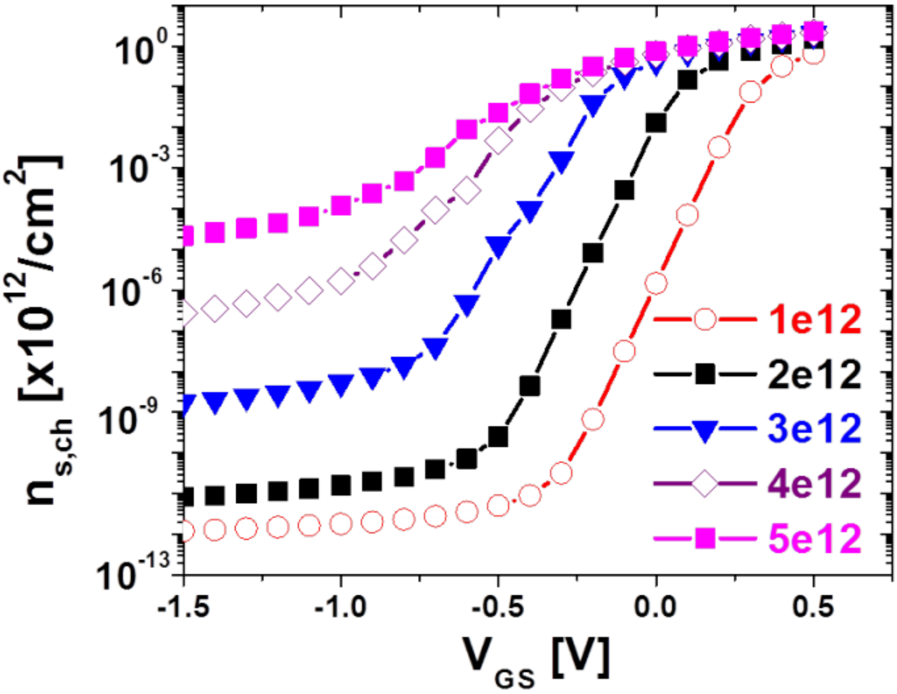


Fig. 2.3 1D Poisson-Schrödinger simulations of channel electron density as a function of gate bias. (Figure taken from Kim *et al.* [28])

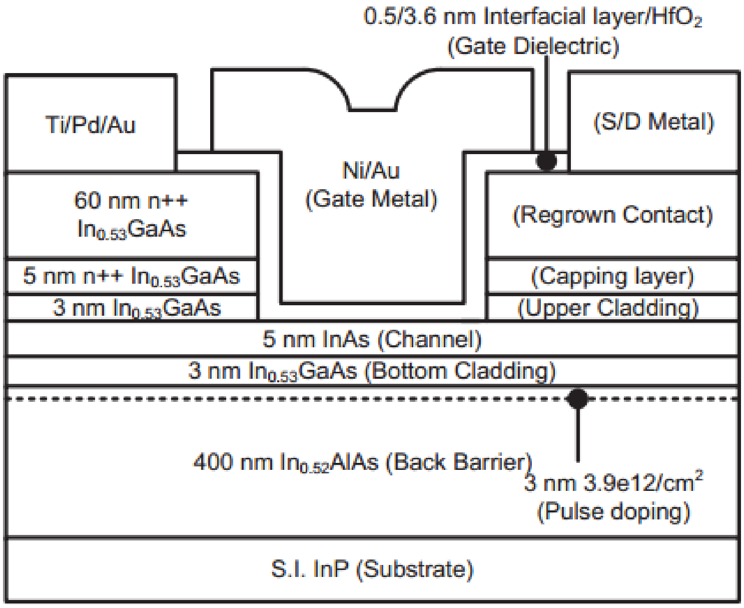


Fig. 2.4 Schematic view of InAs MOSFET with InAs/$In_{0.53}Ga_{0.47}As$ channel, regrown S/D, and surface recess etching. (Figure taken from Lee *et al.* [30])

Chapter 3
Fabrication and Characterization of Quantum Well MOSFET

3.1 Device Fabrication

The process flow for the InAs QW-MOSFETs of this work is shown in Fig. 3.1, and the details of the fabrication steps are summarized in Table 3.1. There are 9 major steps:

1) Device isolation,
2) Formation of the alignment marks for e-beam lithography (EBL),
3) Definition of cap-recess region by EBL,
4) Removal of the cap layer in the EBL defined area,
5) Deposition of high-*k* gate dielectrics by ALD,
6) Definition of contacts and the removal of dielectrics,
7) Metallization of S/D contacts and pads,
8) Gate definition by EBL, and
9) Gate metallization.

The details and purpose of each step are elaborated individually as the follows. The last paragraph evaluates the pros and cons of this gate-last process, and summarizes the critical steps and their effect on device performance.

Device isolation was performed using phosphoric-based mixture and hydrochloric-based solution; the former selectively etches InGaAs and InAlAs layers, and the latter selectively removes InP etch stop layer. The area outside the defined region was etched down to the buffer layer in order to achieve good electrical isolation. Finally, the etch depth was measured by surface profiler after the removal of photo resist (PR). Through mesa formation, the electrically conductive slice, called “active” region, is isolated from the contact pads. Isolation not only restricts the current flows within the active region, but also reduces parasitic resistance and capacitance. The parasitic resistance comes from the current flow between source and drain that does not pass under the gate, degrading device RF performance. Minimum parasitic capacitance was achieved by placing gate stripe on the semi-insulating substrate, since the capacitance is associated with the doping concentration in depletion region underneath the gate stripe.

The e-beam alignment mark was formed by lift-off process, in which the image reversal technique realized the reverse-tapered PR (i.e., AZ 5214-E) profile that enabled the lift-off process. This metallization step only served the purpose of EBL alignment and the process control monitoring (PCM) pattern for the digital etching in the cap-recess process. The design consideration of separating e-beam alignment marks and contact pads in two different steps is that: high post-deposition-annealing (PDA) temperature (400~500℃) after high-*k* deposition degrades ohmic contacts if S/D contacts are formed before the dielectric deposition. Therefore the thermally stable metal scheme, Ti/Au, is employed to prevent metallurgical reaction that might deform the alignment mark and hence degrade the accuracy of EBL.

The EBL of cap-recess region was performed by using typical e-beam resist (ZEP-520A) and the EBL system (JEOL JBX-6000FS). The cross-section of cap recess EBL was shown in Fig. 3.2. Length of the opened area is about 150 nm with resist thickness about 280 nm. Thinner resist profile is advantageous to the scaling of cap-recessed region, which is critical to improve the device performance, since shorter cap-recessed length reduces the parasitic resistance.

Cap-recess was conducted by the selective etching of the InGaAs cap layer over the InP etch stop layer. Citric-based and succinic-based mixtures were used for the selective etching of the native oxide on the surface and the InGaAs cap layer, respectively. We monitored the current of PCM pattern during wet etching, not only to make sure the cap layer within the opened area was removed clearly, but also to optimize the lateral etching, which determines the parasitic resistance and capacitance. The optimized digital recess condition led to a clear removal of cap layer without long lateral etching.

High-*k* gate dielectric was deposited by ALD (Cambridge NanoTech Fiji-202 DCS). In this work, 5-nm Al_2O_3 were used as gate dielectric. Before Al_2O_3 deposition, the sample was passivated by *in-situ* trimethylaluminum (TMA) pre-treatment, which has been proven to be able to reduce D_{it} [31]. In fact, other thinner high-*k* materials with higher dielectric constant such as HfO_2 and La_2O_3 can also be employed in order to decrease effective oxide thickness (EOT), which is helpful to boost device performance including I_D, g_m, on-off current ratio (I_{ON}/I_{OFF}), and SS. However, because this research focuses on device bandgap engineering, other high-*k* stacks and the surface treatments were not used for convenience.

After the photolithography for contacts and pads, the dielectric within the opened area was removed by dilute hydrogen fluoride (DHF) solution, and a treatment using dilute hydrochloric acid was performed before ohmic metallization. The contacts and pads were formed by alloyed Au/Ge/Ni/Au stack. The purposes of this conventional ohmic metal scheme are two-fold: 1) Au/Ge alloy improves adhesion between semiconductor and metal; 2) Ge diffuses into the InGaAs cap layer during the annealing after metallization, and drastically increase the doping concentration few nm underneath the metal. After the lift-off process, excellent specific contact resistance of 1.27×10^{-7} Ω-cm^2 was extracted by transmission line measurement (TLM). Although the extracted value is below the measurement limit of TLM, the result still suggested a good ohmic contact.

Finally, gate EBL and the corresponding metallization were performed. The gate width (W_g) and L_g of the InAs QW-MOSFETs are 40 μm and 250 nm, respectively. The cross-sectional SEM image of the gate stripe is shown in Fig. 3.3. The gate metal scheme used in this work was Ti/Au. After e-beam evaporation, typical e-beam resist stripper, ZDMAC, was used in this lift-off process. The device structure is shown in Fig 3.4.

Finally, the device was passivated by the SiN_x grown by plasma enhanced chemical vapor deposition (PECVD). The via was formed after device passivation.

The key process steps can be divided into several categories according to their effects on device: 1) cap recess EBL, cap etching, and source-drain spacing; 2) surface treatment and PDA condition; 3) gate dielectric materials and thickness; 4) gate EBL; 5) gate stack (which includes the materials for gate metal and gate oxide). They determine parasitic resistance, D_{it}, EOT, L_g, and V_T respectively.

In a nutshell, the devices employed a “gate-last” process. However, as we know, the devices undergone “gate-first” process have better metal-gate/high-*k* and high-*k*/semiconductor interfaces. This is attributed to the fact that the interfaces in gate-first process are kept way from the chemicals and deleterious processing environments that introduce interface states during device fabrication steps. However, because we only have contact aligner to define the S/D contacts and pads, if the gate is formed before contacts, the gate might break during the photolithography using contact aligner. Therefore, we have to choose gate-last process, even though its relatively higher D_{it} may degrade the subthreshold behaviors.

3.2 Device Characterization [1]

3.2.1 DC Measurement

The I-V behaviors of the transistors were characterized in terms of the output and the transfer characteristics. The figures of merit (FOMs) representing device logic performance can be extracted and evaluated by DC measurement. The principles and operational definitions of the extracted FOMs are briefly described in the following paragraphs.

Threshold Voltage (V_T)

The V_T is a fundamental parameter for MOSFET modeling and characterization. This parameter, which stands for the onset of significant drain current flow, has been given several operational definitions. Most of the proposed procedures are based on the measurement of the drain current versus gate voltage (I_D-V_G) characteristics of the transistor. Typical extraction methods bias the transistor at low drain voltage, so that the device operates in the linear region.

There are three commonly used methods that bias device in the linear region: 1) constant current (CC) method, which defines V_T as the gate voltage corresponding to the constant drain current, I_D of 1mA/mm; 2) transconductance linear extrapolation (TLE) method, which defines V_T as the gate voltage axis intercept of the linear extrapolation of the g_m-V_G curve at its maximum first derivative point; 3) extrapolation in the linear region (ELR) method, which defines V_T as the gate voltage axis intercept of the linear extrapolation of the I_D–V_G curves at its maximum transconductance point.

It is obvious that CC method determines V_T in a simple manner, but the CC method has the severe disadvantage of being totally dependent of the arbitrarily chosen value of the I_D level. On the other hand, the assumptions behind TLE method are that: 1) in weak inversion region, g_m increases exponentially with V_G; 2) in the transition region between weak and strong inversion, g_m increases linearly with V_G; 3) in the strong inversion region, g_m decreases with V_G due to the series resistance and mobility. In this work, we choose the most popular one — ELR method to extract device V_T.

Subthreshold Swing (SS)

The SS is the FOM reflects the electrostatic control of the transistor. The SS is defined as:

$$SS = \left(\frac{d \log I_D}{d V_G} \right)^{-1} \tag{3.1}$$

The SS of surface channel MOSFETs can be expressed as:

$$SS = (\ln 10) \frac{kT}{q} \left[1 + \frac{C_{it} + C_d}{C_{OX}} \right] \tag{3.2}$$

The theoretical limitation of SS is about 60 mV/decade, which is also called the thermionic limit of MOSFETs. However, for nowadays nano-scale logic MOSFETs, the SS increases with the scaled gate length due to SCEs. Moreover, the SS degradation is also attributed to the interface states between gate oxide and semiconductor. The introduction of high-*k* gate stack makes the SS degradation more significant, since the interface is poorer than Si/SiO_2 system. This issue is even worse for III-V MOSFETs with high-*k* gate stack, because of the large amount of interface states on the III-V surface. Note that the SS of QW-MOSFETs is different from surface channel MOSFETs. The equation and the details of derivation are presented in the Appendix (A.3).

Drain-induced Barrier Lowering (DIBL)

The DIBL is also a parameter monitoring the short channel effects. The DIBL is defined as:

$$DIBL = \frac{d V_T}{d V_D} \tag{3.3}$$

The DIBL leads to a source-drain leakage and the loss of gate control. The phenomenon can be understood from Fig. 3.5, in which the surface potential of long channel and short channel MOSFETs are plotted. As the V_D increases, the conduction band edge near the drain side is pulled down. For long channel devices, this phenomenon does not have strong influence on the leakage, since the pulled-down region does not reach the source side. However, for short channel devices, the surface potential near the source side is pulled down by the V_D, resulting in a significant drain leakage and a lowering in device V_T.

In practice, we prefer to use two drain biases, 0.5 V and 50 mV, to extract the value of DIBL, since the devices studied in this work is for low-power logic application, the V_D is expected to be lower than 1 V.

3.2.2 RF Measurement

The microwave characteristics are usually characterized by using vector network analyzer (VNA) to obtain the scattering parameters. Typical FOMs, such as f_T and maximum oscillation frequency (f_{max}), can be extracted by interpreting the scattering parameters. The principles and operational definitions of scattering parameters and the extracted FOMs are introduced as the follows.

Two-port Scattering Parameters

The scattering parameters, or called S-parameters, are the fundamental to microwave characteristics of a linear network. It is difficult to measure Z-, Y-, or H-parameters since the device are unstable at open/short conditions. S-parameters measurement uses the matched load (50Ω) instead of open/short circuit conditions, so it is easier to be obtained at high operation frequency. Therefore, the FOMs of device RF characteristics can be extracted by S-parameters, such as gain, return loss, voltage standing wave ratio (VSWR), and reflection coefficient and amplifier stability.

The relationship between the reflected, incident power waves and the S-parameter matrix is expressed as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.4}$$

The electrical field of the signal going into and leaving the ports are denoted as a and b, respectively. And the subscripts, 1 and 2, represents the input port and the output port respectively.

Therefore, s_{11} is the input voltage reflection coefficient, defined as b_1/a_1 at $a_2 = 0$; s_{12} is the reverse voltage gain, defined as b_1/a_2 at $a_1 = 0$; s_{21} is the forward voltage gain, defined as b_2/a_1 at $a_2 = 0$; s_{22} is the output port voltage reflection coefficient, defined as b_2/a_2 at $a_1 = 0$.Therefore, the properties of two-port network are then given by:

scalar logarithmic gain, g = $20\log_{10}|s_{21}|$ dB
input return loss, $RL_{in} = |20\log_{10}|s_{11}||$ dB
output return loss, $RL_{out}= |20\log_{10}|s_{22}||$ dB
input VSWR = $(1+|s_{11}|)/(1-|s_{11}|)$
output VSWR = $(1+|s_{22}|)/(1-|s_{22}|)$

Current gain cut-off frequency (f_T)

The f_T is a more appropriate FOM for digital circuits, in which speed is the primary concern. The operational definition of f_T is the frequency corresponding to the current gain (h_{21}) becomes unity (0 dB), where h_{21} is given by:

$$h_{21} = \frac{2\, s_{21}}{(1-s_{11})(1-s_{22})+s_{12}s_{21}} \tag{3.5}$$

For surface channel MOSFET, the f_T can be approximated as:

$$f_T = \frac{g_m}{2\pi(C'_G + C'_{par})} \tag{3.6}$$

where C'_{par} is the total input parasitic capacitance.

Maximum oscillation frequency (f_{max})

The f_{max} is more relevant for analog applications, since it is defined as the frequency corresponding to the power gain/ unilateral gain becomes unity (0 dB). The unilateral gain, U, is given by

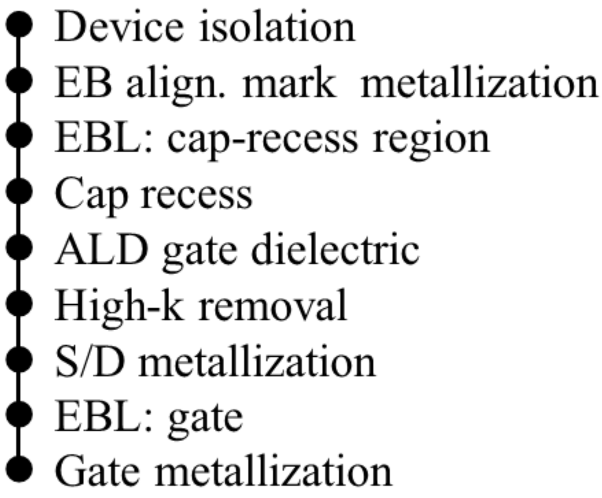
$$U = \frac{|s_{21}|^2}{(1-|s_{11}|^2)(1-|s_{22}|^2)} \tag{3.7}$$

For surface channel MOSFET, the f_{max} can be approximated as:

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_G C'_{GD}}} \tag{3.8}$$

Table 3.1 The fabrication process of InAs QW-MOSFET.

Modules	**Steps**	**Remarks**
1. Device isolation	Photolithography	
	Mesa isolation	◆ InGaAs/InAlAs etching H_3PO_4: H_2O_2: H_2O =1:1:80 ◆ InP etching HCl: H_3PO_4: H_2O = 1:1:1
	PR strip	
	AEI	Etch depth: 220 nm (to buffer layer)
2. EBL alignment mark formation	Photolithography	
	Metallization	◆ Native oxide etching HCl: H_2O =1:10 ◆ Ti/Au = 50/150 nm ◆ 250℃ annealing for 30 sec
3. Cap-recess	E-beam lithography	Resist: ZEP-520A
	Cap etching	◆ Critic acid-based solution ◆ Succinic acid-based solution
	PR strip	ZDMAC
4. ALD high-k gate dielectric	Pre-deposition TMA treatment	
	ALD gate dielectric	5nm Al_2O_3
5. S/D contact formation	Photolithography	
	Dielectric etching	HF: H_2O =1:100
	Metallization	◆ Au/Ge/Ni/Au=20/40/140/250 nm ◆ Lift-off process
6. Gate formation	E-beam lithography	Resist: PMGI/ZEP-520A
	Metallization	◆ Ti/Au = 50/250 nm ◆ Lift-off process
7. Passivation	Device passivation	PECVD 100-nm Si_3N_4
	Photolithography	
	Via etching	
	PR strip	



- Device isolation
- EB align. mark metallization
- EBL: cap-recess region
- Cap recess
- ALD gate dielectric
- High-k removal
- S/D metallization
- EBL: gate
- Gate metallization

Fig. 3.1 Process flow of buried-channel gate-last QW-MOSFET.

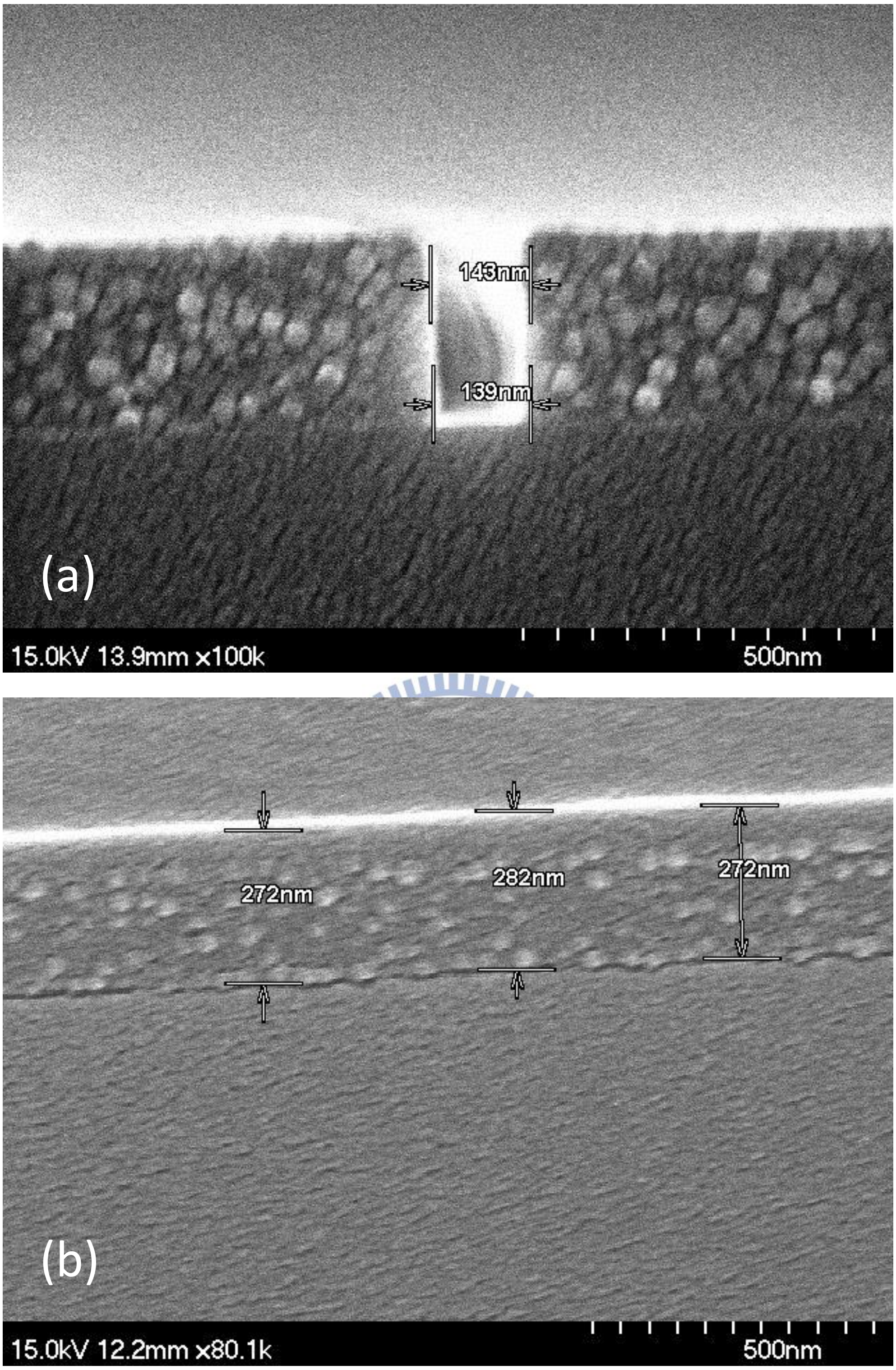


Fig. 3.2 Cross-sectional SEM image of cap-recess EBL (a) resist profile (b) resist thickness. The resist used in this EBL is ZEP-520A.

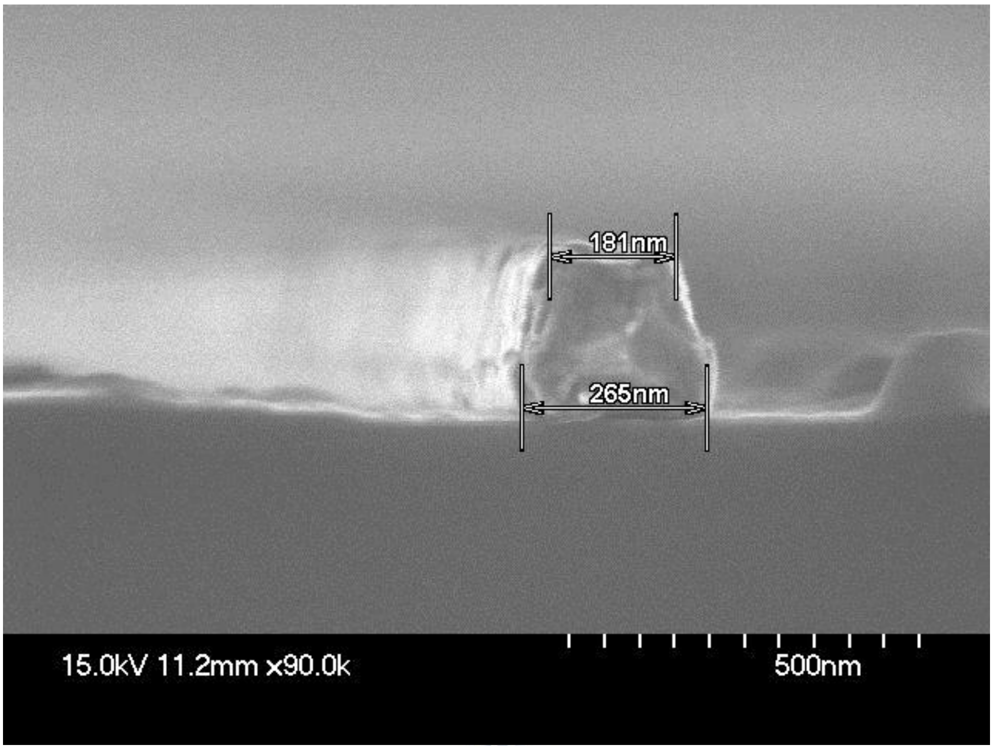


Fig. 3.3 SEM image of the gate stripe. The gate length of the fabricated QW-MOSFETs in this work is about 250 nm.

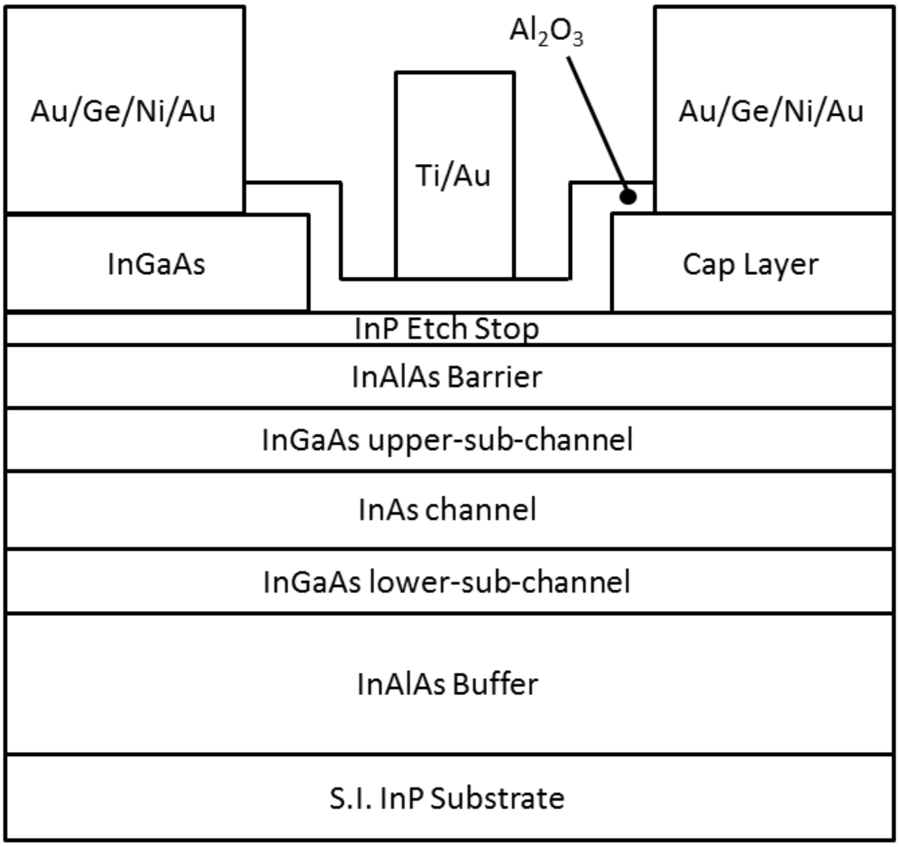


Fig. 3.4 Schematic device structure of the InAs QW-MOSFETs in this work.

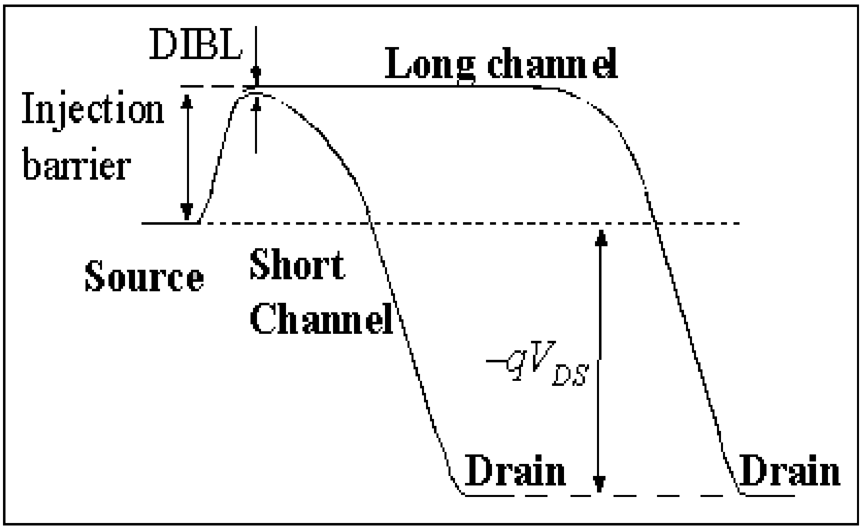


Fig. 3.5 Effect of DIBL on the threshold voltage of short channel devices.

Chapter 4
Device Bandgap Engineering

In order to investigate the bandgap engineering of composite channel, we used both theoretical and experimental approaches. For the theoretical analysis, a technology computer aided design (TCAD) tool, nextnano, was used to capture and visualize the theoretical analysis. For the experimental study, three kinds of QW-MOSFETs with different epitaxial structures were fabricated and characterized. Through DC and RF measurements, the experimental analysis was also conducted in order to examine the effect of epitaxial structure on the performance of InAs QW-MOSFETs.

4.1 Effect of Epitaxial Structure on Carrier Confinement and Mobility

4.1.1 Thickness of InAs-core and InGaAs Sub-channels

In order to study the influence of InAs-core thickness on the carrier confinement in the InAs-core and the apparent mobility of the entire epitaxial structure, two $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ structures with different composite channel thickness (i.e., InGaAs/InAs/InGaAs of 5/5/5 and 5/2/5 nm) were simulated. The band diagrams, the eigenvalues of sub-bands, and the wavefunction (i.e., $|\varphi|^2$) in each sub-band of these two quantum well (QW) systems were solved by Poisson-Schrödinger solver. The numerical results are shown in Fig. 4.1 and Fig. 4.2.

In Fig. 4.1, we can see that the first sub-band "height", which is defined as the difference between first sub-band and the condition band of InAs, of thin-core structure is higher than the thick one (i.e., 112 mV vs. 74 mV). Obviously, this result is due to the thickness of center InAs layer. The InAlAs/InGaAs/InAs/InGaAs/InAlAs structure is essentially a QW system, in which the thickness of composite channel determines the "width" of this QW. The thinner InAs-core corresponds to higher and more discrete eigenvalues (i.e., larger energy separation between sub-bands).

In Fig. 4.2, the electron distribution of the structures with thin-core (blue) and thick-core (black) are shown. We can see that the thin-core structure has higher peak in the center. However, it does not lead to more electrons dwell in the InAs layer, since the total number of the electrons in the core is the area under the probability curve within the InAs layer. In this case, the thin-core structure has fewer electrons in the high-mobility InAs layer due to the scaled InAs thickness. Therefore, the apparent mobility of the simulated thin-InAs structure is lower than the thick one in this case. This result suggests that the scaling of the InGaAs/InAs/InGaAs structure should employ the scaling of both InAs and InGaAs layer; otherwise the reduced area in the InAs region will slightly degrade the apparent mobility of the entire structure.

This suggestion can be verified by the experimental result. Three epitaxial structures (shown in Tables 4.1, 4.2, and 4.3) with InGaAs/InAs/InGaAs of 4/5/4, 3/2/3, and 1/2/1 nm are grown by molecular beam epitaxy (MBE), and their Hall mobility are characterized to examine the effect of the composite channel thickness on the apparent mobility. It is shown that the measured Hall mobility of 4/5/4-structure is 13,500 $cm^2V^{-1}s^{-1}$, which is higher than 3/2/3-strucuture (11,500 $cm^2V^{-1}s^{-1}$) and 1/2/1-structure (11,100 $cm^2V^{-1}s^{-1}$). We can see that although the 3/2/3-structure and 1/2/1-sturcture has the same InAs-core thickness, thinner InGaAs sub-channel leads to lower Hall mobility since more carriers dwells outside the high-mobility InGaAs/InAs/InGaAs composite channel. The previous deduction can also be verified by simulations. The $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As/ In_{0.52}Al_{0.48}As$ QW systems with two kinds of InGaAs/InAs/InGaAs thicknesses, 3/2/3 and 1/2/1 nm, are shown in Fig. 4.3. Even though the peak population of in InAs region for 1/2/1-structure is higher than 3/2/3-structure, the 1/2/1-strcucture has more electrons outside the composite channel, leading to the small mobility degradation. The result of Hall measurements also manifested the fact that the thickness ratio (TR) of InGaAs sub-channel to InAs-core, TR = t_{InGaAs}/t_{InAs}, should be scaled during the optimization of composite channel.

4.1.2 Indium Composition of InGaAs Sub-channels

In order to study the influence of InGaAs sub-channel In composition on the carrier confinement in the InAs-core and the apparent mobility of the entire epitaxial structure, two $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As/InAs/In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ structures with different $In_xGa_{1-x}As$ sub-channel In composition (70% vs. 30%) were simulated. The purpose of choosing the large difference in In composition in the simulation is to easily visualize and address the effect of sub-channel In composition. The band diagrams, the eigenvalues of sub-bands, and the wavefunctions of these two QW systems are shown in Fig. 4.4.

In Fig. 4.4, the black line denotes the conduction band edge of the QW system with higher In composition (high-In%), and the blue line is for lower In composition (low-In%); the wavefunction in the first sub-band for low-In% and high-In% are in pink and red, respectively. We can see that there is no significant difference in the first sub-band “height” (i.e., 0.19 V for low-In% and 0.18 V for high-In%), since the thickness of every layers are the same.

In Fig. 4.5, the electron distribution of the structures with low-In% (blue) and thick-core (black) are shown. We can see that the low-In% structure has higher peak in the center. Because the InAs-thickness of low-In% and high-In% is the same, the higher peak probability corresponds to the higher apparent mobility. This result suggests that we are able to improve the carrier confinement in the InAs-core and the apparent mobility by using the sub-channel with slightly lower In composition. However, the In composition cannot be too low; otherwise it will degrade the apparent mobility since some portion of electrons travel through the lower-mobility InGaAs sub-channel.

To sum up, not only the thickness of InAs and InGaAs layers but also the In composition of InGaAs sub-channels should be optimized to achieve good electrostatic control and carrier mobility. Although the buried channel QW-MOSFET prevents the electrons from surface scattering and preserves the high-mobility-essence of InAs channel, buried channel MOSFETs usually has poor subthreshold behaviors due to the increased gate-to-channel distance. Hence the immunity to SCEs is also an important issue to QW-MOSFET.

The improvements in controlling SCEs can be obtained by the scaling of gate-to-channel distance (i.e., gate-to-2DEG distance, more precisely for the case of

QW-MOSFETs). This goal can be realized by reducing the thickness of InP etch stop layer, InAlAs barrier layer, and InGaAs/InAs/InGaAs composite channel. The epitaxial structures used for the fabrication of QW-MOSFETs with different optimization strategies will be presented in the next section.

4.2 Experimental Epitaxial Structures

Three kinds of structures for the experimental study of the impact of epitaxial structures on the performance of QW-MOSFETs will be shown and disused in this section. According to the thickness of composite channel and the modulation doping type, they are named regular channel (RC), thin channel (TC), and inverted thin channel (ITC), as shown in Tables 4.1, 4.2, and 4.4, respectively. The Hall mobility and sheet carrier density of all the experimental structures are summarized in Table 4.5.

The thickness of each layer of InGaAs/InAs/InGaAs composite channel structure are (unit: nm), 4/5/4 for RC, 3/2/3 for TC, and 2/3/4 for ITC. Note that the total thickness of RC is 13 nm, which is comparable to the “thin channel” works done by Kim *et al* [28]. In ITC structure, the In composition of two InGaAs sub-channels is slightly lower than RC and TC (65% vs. 70%). The purpose of this design is the formation of deeper QW that confines more carriers in the high-mobility InAs core.

Compared to RC, TC structure features scaled gate-to-channel distance, reduced composite channel thickness, and smaller potential drop in the barrier layer. The band diagram of the RC and TC structures is shown in Fig. 4.6. The scaled gate-to-channel distance was obtained by reducing the thickness of barrier layer and composite channel. This factor is expected to have better electrostatic control. However, the un-optimized scaling of composite channel resulted in a small degradation in the carrier mobility as mentioned in Section 4.1.1.

Compared to RC, ITC structure features ultra-scaled gate-to-channel distance, lower-In-composition sub-channel, and inverted-type modulation doping. The band diagram of RC and ITC structures is shown in Fig.4.7. The ultra-scaled gate-to-channel distance is also attributed to the inverted δ-doping. The elimination of upper InAlAs barrier layer not only reduced the gate-to-channel distance, but also reduced the S/D resistance R_{SD}, since the intrinsic InAlAs layer is resistive. Moreover, the inverted modulation doping slightly makes the 2DEG away from the gate. On the other hand, the InGaAs sub-channel with lower In composition is expected to have better carrier confinement compared to the structure with higher In composition (i.e., if the thickness of each layer in the structures are the same) as discussed in Section 4.1.2. An observable difference near the InP layer is also shown in Fig. 4.7. This difference is due to the different band alignment of heterojunctions. For RC structure, the InP/InAlAs heterojunciton belongs to type II, the staggered gap. For ITC structure, the InP/InGaAs heterojunctions belongs to type I, the straddling gap. This difference affects the V_T of QW-MOSFETs. The comprehensive V_T calculation will be discussed in the Appendix.

4.3 Result and Discussion

The QW-MOSFETs with RC, TC, and ITC epitaxial structures were fabricated and characterized in terms of DC and RF performance. The L_g and W_g of the QW-MOSFETs are 0.25 μm and 40 μm, respectively, and the EOT of all devices is about 2 nm. The output and transfer characteristics for RC/TC/ITC QW-MOSFETs and RC HEMT are shown in Figures 4.8, 4.9, 4.10, and 4.11. Summary of all device performances is presented in Table 4.6, in which the DC performance of Schottky-gated RC HEMT with gate length of 60 nm is also shown for the comparison of insulated-gate and Schottky-gate InAs FETs. Favorable current saturations at low V_D of 0.5 V with good pinch-off behaviors are observed in all typical devices.

RC QW-MOSFETs represents comparable I_D to 60-nm-gate RC HEMT (257 μA/μm vs. 208 μA/μm, respectively) with suppressed gate leakage current, as shown in Fig. 4.12. The gate current of QW-MOSFET is about 2.5 orders lower than HEMT, since the wide-bandgap of gate dielectric prevents gate leakage. The reason why we compare HEMT with QW-MOSFET instead of MOS capacitor is due to the difference in the high-*k*/semiconductor interface. The high-*k*/semiconductor interface of transistors is worse than MOS capacitor, since the process of transistors is more complicated than the capacitor. So the comparison among HEMT and QW-MOSFET reflects the “real” difference in gate leakage. On the other hand, the g_m of RC QW-MOSFET is much smaller than that of RC HEMT due to the difference in gate length. Regarding the subthreshold behavior, the SS of QW-MOSFET is 684 mV/decade, while the SS of HEMT is only 110 mV/decade. The SS degradation is due to the poor III-V/high-k interface. Those interface states not only affect the subthreshold behavior, but also give rise to severe hysteresis phenomena, so the surface treatment before gate dielectric deposition should be optimized.

Compared to RC device, TC QW-MOSFET exhibits 6% lower I_D and 11% lower peak g_m at the same bias condition, as shown in Fig. 4.13. This slight degradation can be explained by the difference in mobility. The Hall mobility of RC structure is slightly higher than TC structure since the RC structure has better carrier confinement in InAs channel as mentioned in Section 4.1.1. However, the TC device has much better electrostatic control (SS of 187 mV/decade) due to the scaling of barrier layer and composite channel. The experimental results indicate that, even though thinner composite channel is beneficial to suppress SCEs, interface states still play an important role in the SS degradation. Furthermore, the TC device has higher V_T. The reason should be examined by the derived V_T models in the Appendix. For normal-type QW-MOSFETs (i.e, not inverted modulation doping), the V_T is given by[1]:

$$V_T \sim \phi_B - \frac{(\Delta E_{C,HK/InP} - \Delta E_{C,InP/InAlAs} + \Delta E_{C,InAlAs/InGaAs} + \frac{\Delta E_g}{2})}{q} - \phi_P + (\phi_{1sb} - \phi_{ch})$$
$$- \frac{qN_{ox,bulk}}{C_{ox}} - \frac{qN_{it}(E_F)}{C_{ox}} \qquad (4.1)$$

where, $\Delta E_{C,HK/InP}$: the conduction band discontinuity of high-*k*/InP interface;

$\Delta E_{C,InP/InAlAs}$: the conduction band discontinuity of InP/InAlAs interface;

$\Delta E_{C,InAlAs/InGaAs}$: the conduction band discontinuity of InAlAs/InGaAs interface;

ΔE_g: $\Delta E_g = E_g(\mathrm{In_xGa_{1-x}As}) - E_g(\mathrm{InAs})$;

ϕ_P: the potential change in the barrier layer,

for delta-doping, $\phi_p = q\, n_{sh}\, t_{barrier} / \varepsilon_{barrier}$;

N_{it} : the *effective* charge density (/cm^2) of the high-k /InP interface traps;

$N_{ox,bulk}$: the fixed oxide charge density (/cm^2).

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[1] The full derivation of V_T is shown in the Appendix. (A.1)

Because the other materials-related parameters for TC and RC structures are the same and the ϕ_p for TC is smaller than RC due to thinner barrier layer (i.e., smaller $t_{barrier}$), the V_T of TC device is expected to be higher than RC device. The experimental result also verifies our deduction: the V_T of TC QW-MOSFET is -0.09 V, and the V_T of RC device is -1.12 V.

ITC QW-MOSFET demonstrates the best output and transfer characteristics (Fig. 4.14) among the three device structures: I_D of 505 μA/μm, peak g_m of 412 μS/μm. The I_D is about twice larger than RC device and the peak g_m also has over 50% improvement. The great improvement over RC and TC devices is based on the reduced parasitic resistance and increased gate capacitance. The equivalent circuits near the S/D side in term of resistance for normal-type and inverted-type QW-MOSFETs are shown in Fig. 4.15. The total parasitic source (or drain) resistance of normal-type device is given by: R_S (norm.) = $r_c+r_{cap}+r_{etch\ stop}+r_{barrier}$; and the parasitic resistance of inverted-type device is expressed as: R_S (inv.) = $r_c+r_{cap}+r_{etch\ stop}$, where r_C is the contact resistance, and the other subscripts stands for the resistance component in that layer. Clearly, the inverted-type device possesses smaller parasitic resistance by the elimination of upper InAlAs layer, which is known to be the largest resistance component. One the other hand, the equivalent circuits of composite channel QW-MOSFETs' gate stack in term of capacitance is shown in Fig. 4.16. The gate capacitance, C_G, can be expressed as[2]:

$$C_G = \frac{1}{\dfrac{1}{C_{OX}} + \left[C_{it} + \dfrac{1}{\dfrac{1}{C_{ins}} + \dfrac{1}{C_Q} + \dfrac{1}{C_{centroid}}}\right]^{-1}} \tag{4.2}$$

where the subscripts *ox*, *it*, *ins*, *Q*, *centroid* stand for the capacitance component of gate dielectric, interface states, insulator layer (i.e., InP and InAlAs), quantum capacitance, and centroid capacitance. The insulator capacitance (C_{ins}) of normal-type device is the series combination of two capacitance components (i.e., $C_{ins}(\text{norm.})^{-1}=C_{InP}^{-1} + C_{InAlAs}^{-1}$). However, for inverted-type device, C_{ins} has only the InP component. Thus the inverted-type device has higher C_{ins} and hence higher C_G. Furthermore, ITC device exhibits SS of 312 mV/decade, which is better than RC device. This improvement in SS is attributed to the ultra-scaled gate-to-channel

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[2] The full derivation of C_G is shown in the Appendix. (A.2)

distance achieved by inverted modulation doping. However, the SS of TC device is still better than ITC. Moreover, the I_{ON}/I_{OFF} of ITC devices is in the order of 10^2, which is far below the requirement for logic application (~10^5). This poor ratio is caused by higher modulation doping concentration, as mentioned in Section 2.2 (cf. Fig. 2.3). The improvement in I_{ON}/I_{OFF} can be realized by lowering the concentration of δ-doping or replacing the ohmic metal stack with Schottky metal scheme to suppress off-state leakage (I_{OFF}). But the latter method is not preferred, since Schottky S/D not only reduces I_{OFF}, but also reduces I_{ON}. However, the overall evaluation in terms of I_D and g_m still indicates that ITC structure is a more suitable design for future low-power and high-performance logic applications.

The on-wafer RF measurement of RC QW-MOSFET and ITC QW-MOSFET are also conducted to evaluate their potential in high frequency applications. The microwave characteristics of RC and ITC devices without de-embedding are shown in Fig. 4.17. The extrinsic f_T and f_{max} are extracted by extrapolation with theoretical -20 dB/decade slope and the devices are biased at low V_D of 0.5 V. For RC device, the extrinsic f_T and f_{max} are 32 GHz and 53 GHz. The extrinsic f_T and f_{max} of ITC device are 70 GHz and 82 GHz. It is shown that ITC device exhibits better microwave performance and the ITC structure is also a preferable design for the RF and microwave applications.

Finally, the ITC device is also benchmarked with the similar works done by other research groups. The current drive at V_D of 0.5 V as a function of gate length of the benchmarked devices is presented in Fig. 4.18. The ITC QW-MOSFET in this work has good current drive and RF performance without using sub-100-nm-gate like other works.

4.4 Summary

A thoroughgoing investigation into the bandgap engineering of InAs composite channel is obtained. The conclusions of this chapter are drawn and listed as follows:

- The structure with lower-In-composition sub-channel improves carrier confinement in the InAs-core. The better carrier confinement results in the improved transport properties. However, the In composition of sub-channel cannot be too low; otherwise the decreased mobility in sub-channel will degrade the apparent mobility of the entire structure.
- The device with thinner composite channel structure effectively suppresses SCEs by reducing gate-to-channel distance. The TR should be optimized during the scaling of entire composite channel. Moreover, the interface states still play an important role in SS degradation, which is hard to be compensated by simply using thin composite channel structure.
- The device with ITC structure exhibits good I_D and g_m, but mediate SS. The improvement in I_D and g_m is due to the reduced parasitic resistance and higher gate capacitance caused by the elimination of upper InAlAs layer. The improved immunity to SCEs is attributed to the thinner composite channel and ultra-thin InP layer.
- The experimental results shows that ITC InAs QW-MOSFET is a promising candidate for future low-power high-performance logic and microwave applications if the optimized surface treatment, scaled L_g, and reduced EOT are realized.

Table 4.1 Experimental epitaxial structure 1: regular channel (RC).

	Materials	In %	Thickness (A)	Dopant & Concentration
Cap	n^{+}-InGaAs	53	450	Si, 5×10^{19} cm^{-3}
Etch Stop	i-InP	100	50	
Barrier	i-InAlAs	52	80	
δ-doping	Si	-	-	Si, 4×10^{12} cm^{-2}
Spacer	i-InAlAs	52	50	
Channel	i-InGaAs	70	40	
	i-InAs	100	50	
	i-InGaAs	70	40	
Buffer	i-InAlAs	52	5000	
3” semi-insulating InP substrate				

Table 4.2 Experimental epitaxial structure 2: thin channel (TC).

	Materials	In %	Thickness (A)	Dopant & Concentration
Cap	n^+-InGaAs	53	450	Si, 5×10^{19} cm^{-3}
Etch Stop	i-InP	100	50	
Barrier	i-InAlAs	52	50	
δ-doping	Si	-	-	Si, 4×10^{12} cm^{-2}
Spacer	i-InAlAs	52	30	
Channel	i-InGaAs	70	30	
	i-InAs	100	20	
	i-InGaAs	70	30	
Buffer	i-InAlAs	52	5000	
3” semi-insulating InP substrate				

Table 4.3 Experimental epitaxial structure 3: ultra-thin channel (UTC).

	Materials	In %	Thickness (A)	Dopant & Concentration
Cap	n^+-InGaAs	65	40	Si, 2×10^{19} cm^{-3}
	n^+-InGaAs	53	150	Si, 2×10^{19} cm^{-3}
	n^+-InAlAs	52	150	Si, 2×10^{19} cm^{-3}
Etch Stop	i-InP	100	30	
Barrier	i-InAlAs	52	20	
δ-doping	Si	-	-	Si, 4×10^{12} cm^{-2}
Spacer	i-InAlAs	52	30	
Channel	i-InGaAs	70	10	
	i-InAs	100	20	
	i-InGaAs	70	10	
Buffer	i-InAlAs	52	6000	
3” semi-insulating InP substrate				

Table 4.4 Experimental epitaxial structure 4: inverted thin channel (ITC).

	Materials	In %	Thickness (A)	Dopant & Concentration
Cap	n^+-InGaAs	53	250	Si, 2×10^{19} cm^{-3}
Etch Stop	i-InP	100	30	
Channel	i-InGaAs	65	20	
	i-InAs	100	30	
	i-InGaAs	65	40	
Spacer	i-InAlAs	52	30	
δ-doping	Si	-	-	Si, 3×10^{12} cm^{-2}
Buffer	i-InAlAs	52	5000	
3” semi-insulating InP substrate				

Table 4.5 Summary of the Hall measurement.

Epitaxial Structure	RC	TC	UTC	ITC
Composite Channel Structure $In_XGa_{1-X}As/InAs/In_XGa_{1-X}As$ (unit: nm)	4/5/4	3/2/3	1/2/1	2/3/4
Sub-channel In %	70	70	70	65
Hall Mobility ($cm^2V^{-1}s^{-1}$)	13,400	11,500	11,100	12,400
Sheet Carrier Concentration ($\times 10^{12}$ cm^{-2})	2.95	3.24	3.02	2.81

Table 4.6 Summary of the DC and RF performance of QW-MOSFETs and HEMT fabricated in this work.

	QW-MOSFET			HEMT
channel type	RC	TC	ITC	RC
gate length	250	250	250	60
I_D (μA/μm) @ V_D = 0.5V	257	242	505	208
peak g_m (μS/μm) @ V_D = 0.5V	270	241	412	584
SS (mV/decade)	684	187	312	110
DIBL (mV/V)	198	170	183	137
V_T (V)	-1.12	-0.09	-0.85	-0.35
I_{ON}/I_{OFF}	1.27×10^2	9.6×10^3	5.73×10^2	8.53×10^3
f_T (GHz)	32	N/A	70	N/A
f_{max} (GHz)	53	N/A	82	N/A

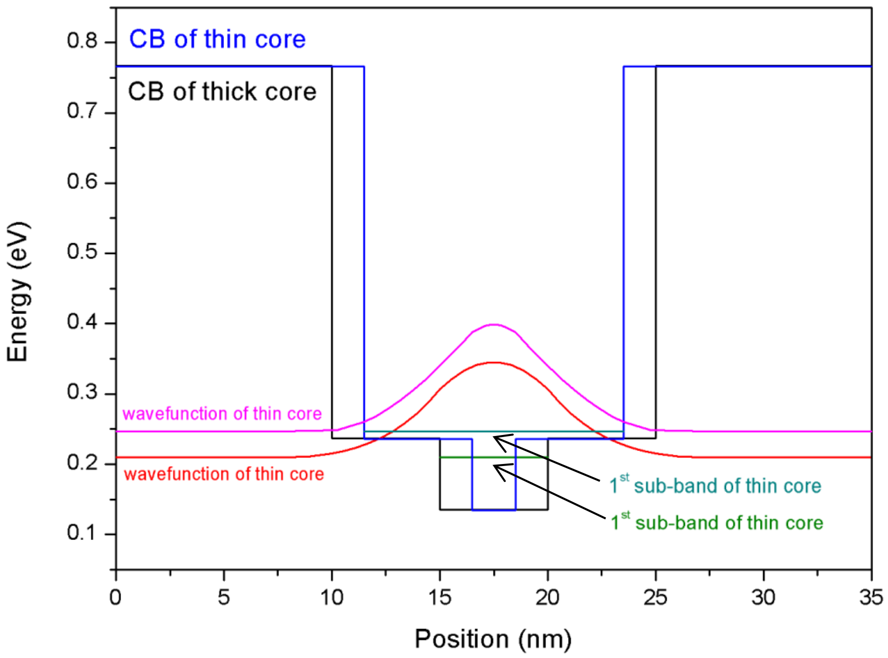


Fig. 4.1 The conduction band edge profiles of the QWs with different InAs-core thickness in the composite channels. The simulated QW structures consist of $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ /$In_{0.52}Al_{0.48}As$ with InGaAs/InAs/InGaAs thicknesses of 5/5/5 and 5/2/5 nm.

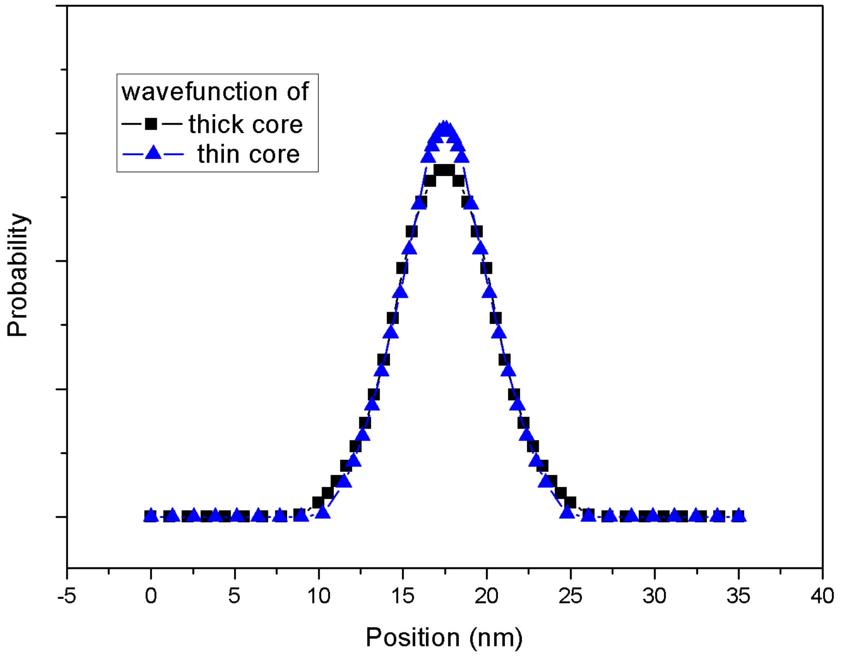


Fig. 4.2 The wavefunction in first sub-band of the QWs with different InAs-core thickness in the composite channels. The simulated QW structures consist of $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ /$In_{0.52}Al_{0.48}As$ with InGaAs/InAs/InGaAs thicknesses of 5/5/5 and 5/2/5 nm.

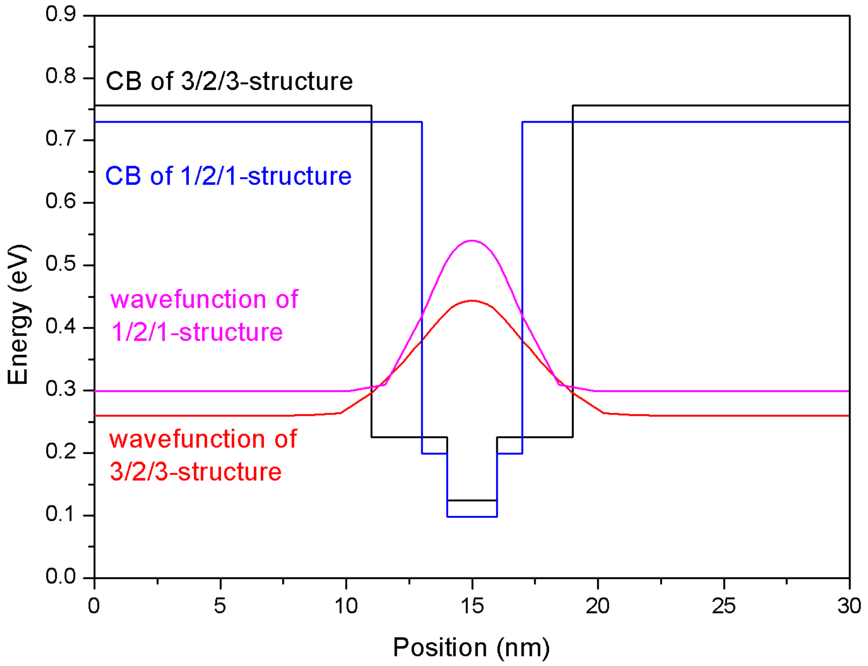


Fig. 4.3 The $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ QW systems with two kinds of InGaAs/InAs/InGaAs thicknesses, 3/2/3 and 1/2/1 nm.

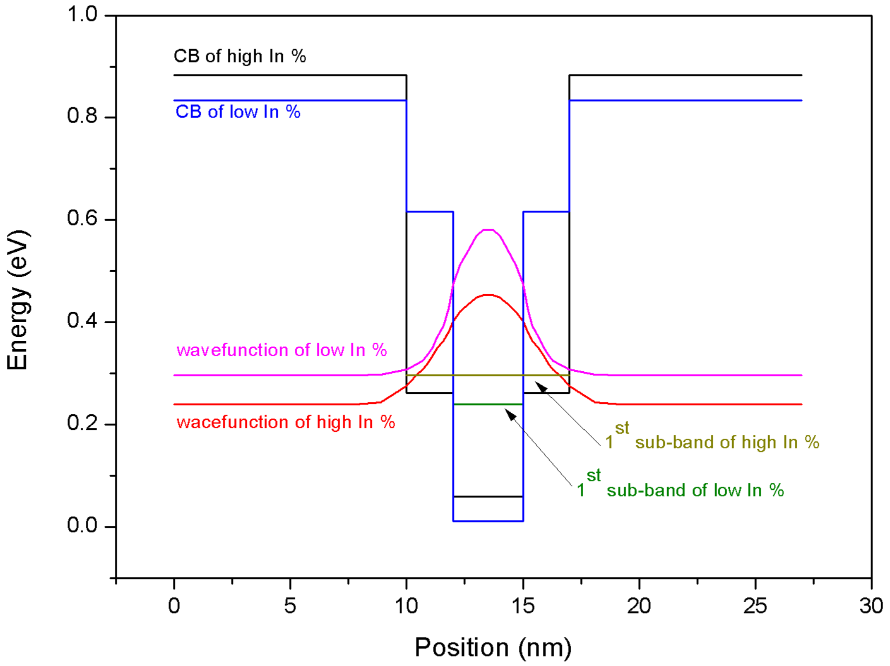


Fig. 4.4 The conduction band profiles of two QW systems with different In composition in the InGaAs sub-channels. Two kinds of In composition, $In_{0.7}Ga_{0.3}As$ and $In_{0.3}Ga_{0.7}As$, are used to emphasize the difference in In composition.

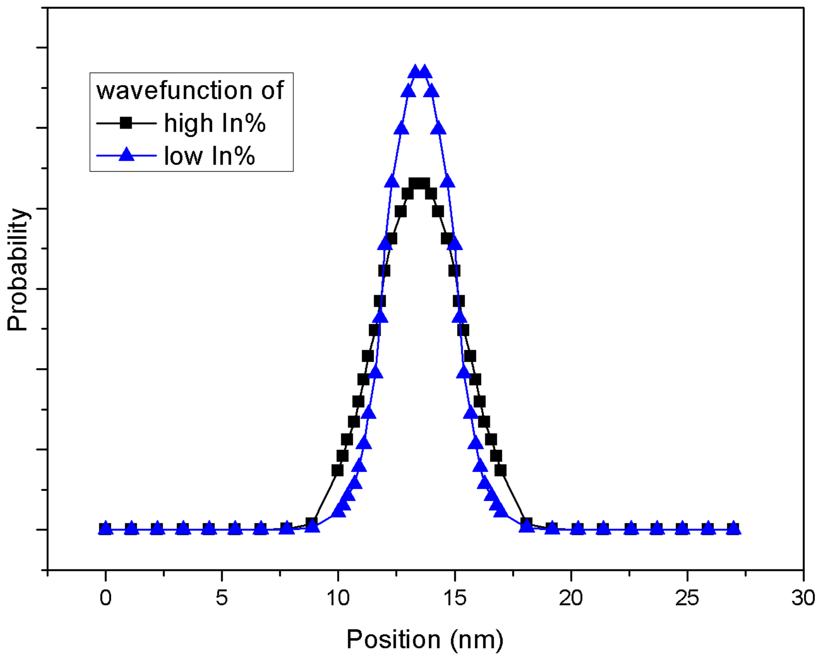


Fig. 4.5 The wavefunction in first sub-band of the QWs with different sub-channel In composition of 70% and 30%.

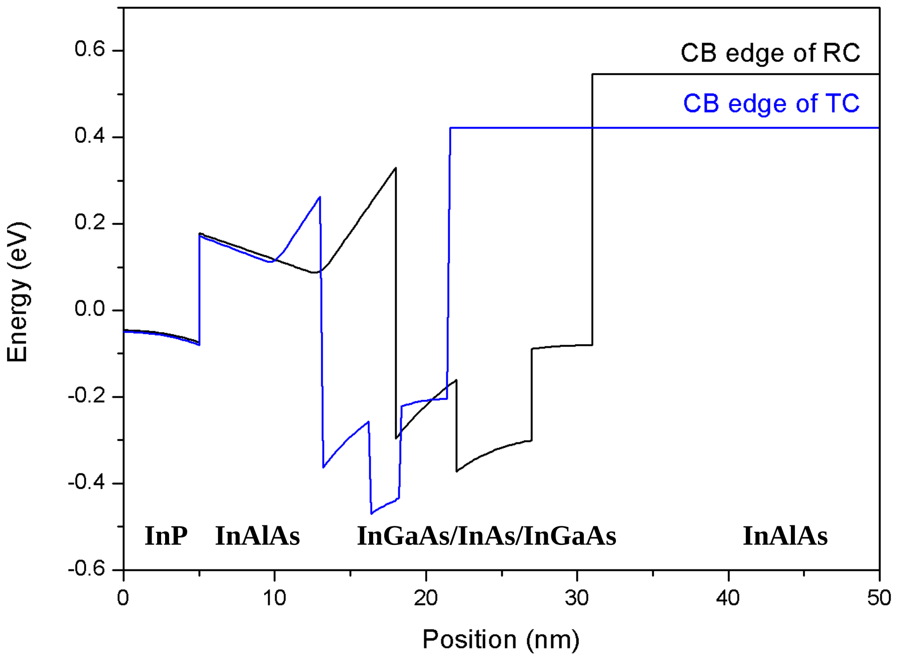


Fig. 4.6 The band diagrams of the RC and TC structures.

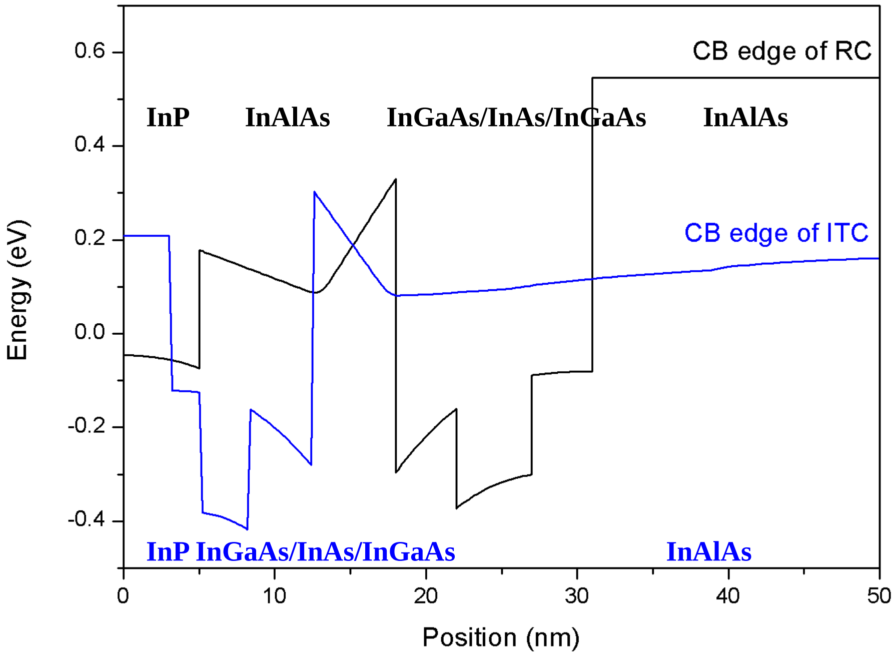


Fig. 4.7 The band diagrams of the RC and ITC structures.

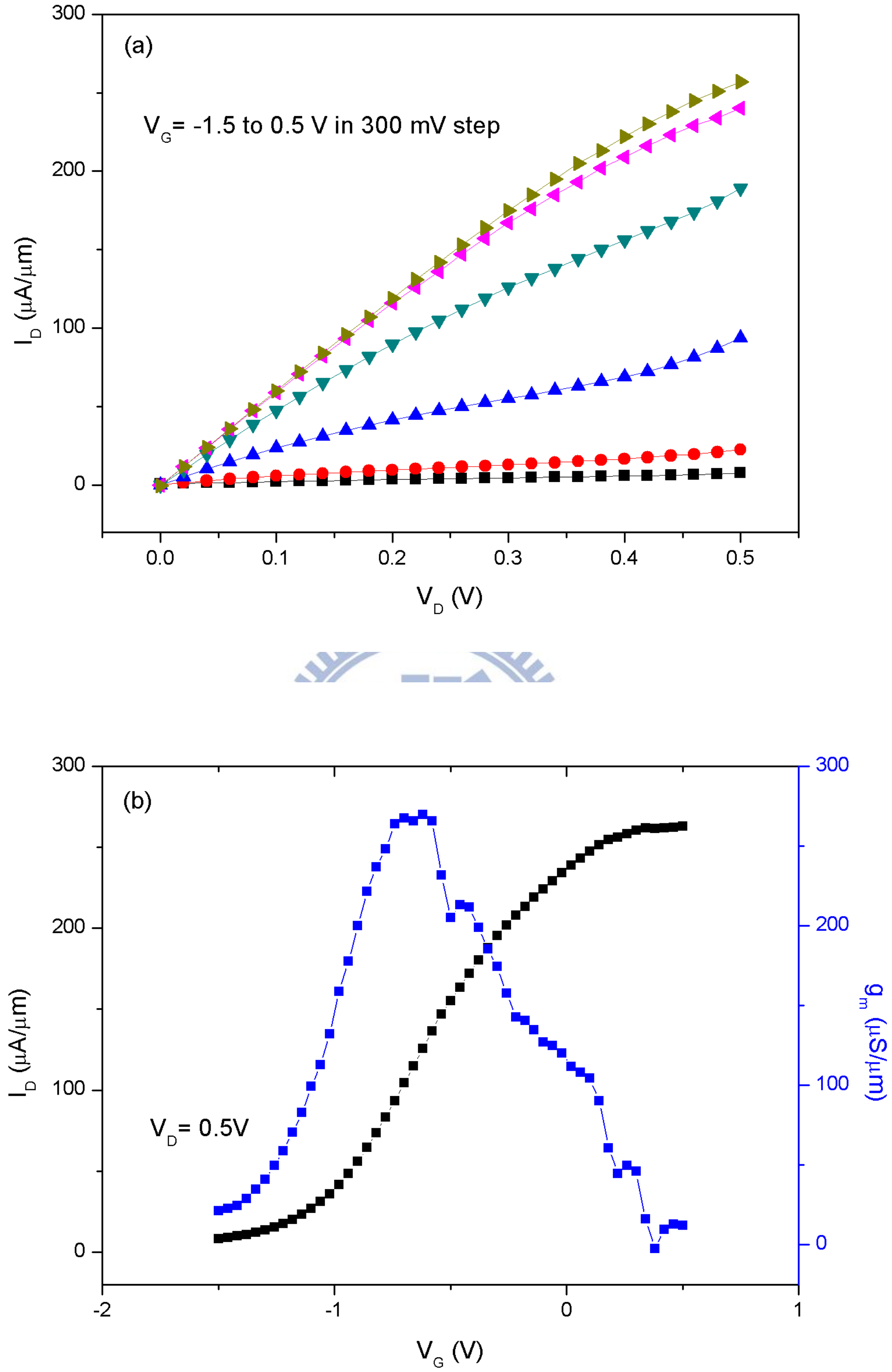


Fig. 4.8 (a) output characteristics and (b) transfer characteristics of RC QW-MOSFET.

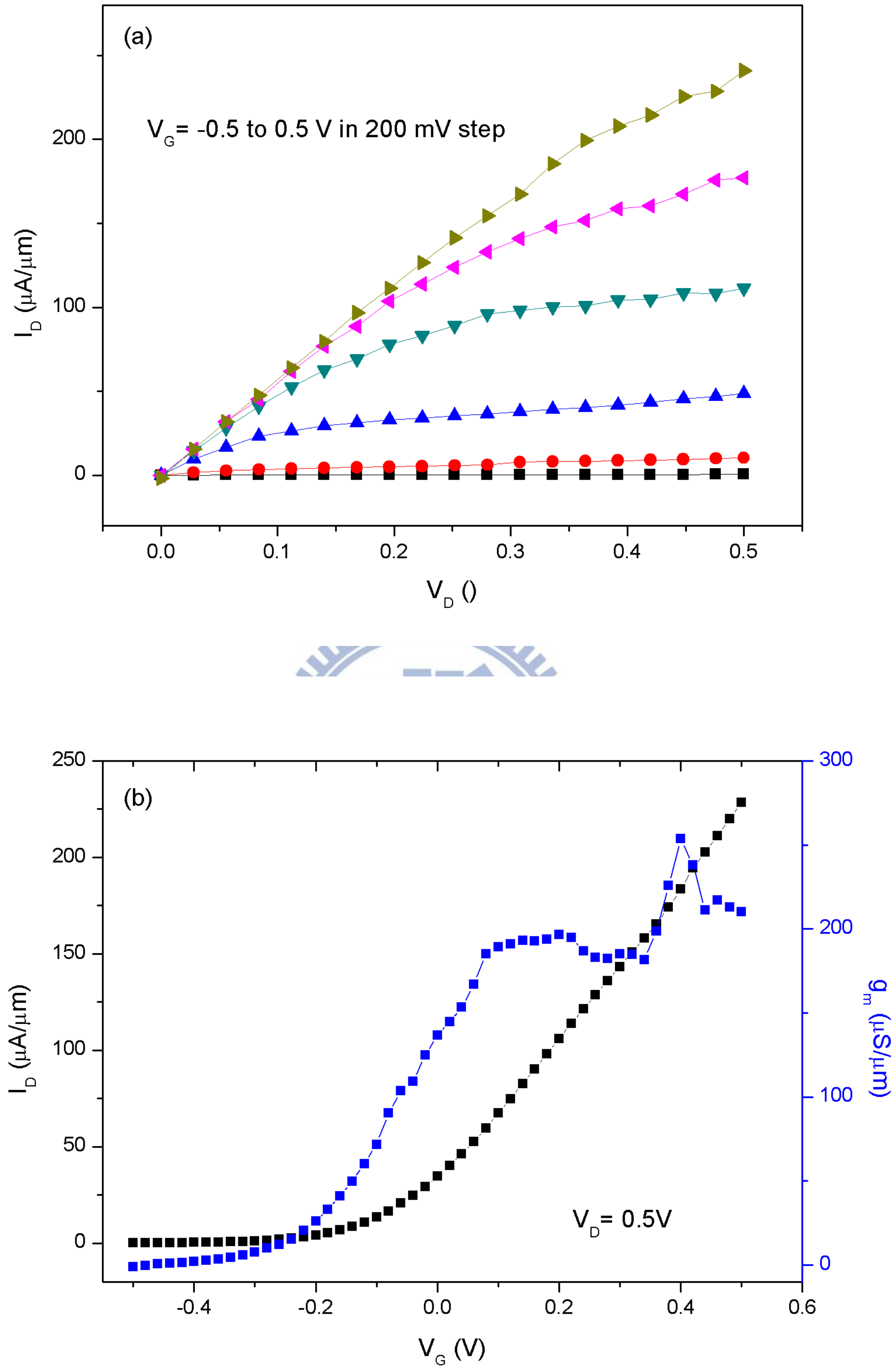


Fig. 4.9 (a) output characteristics and (b) transfer characteristics of TC QW-MOSFET.

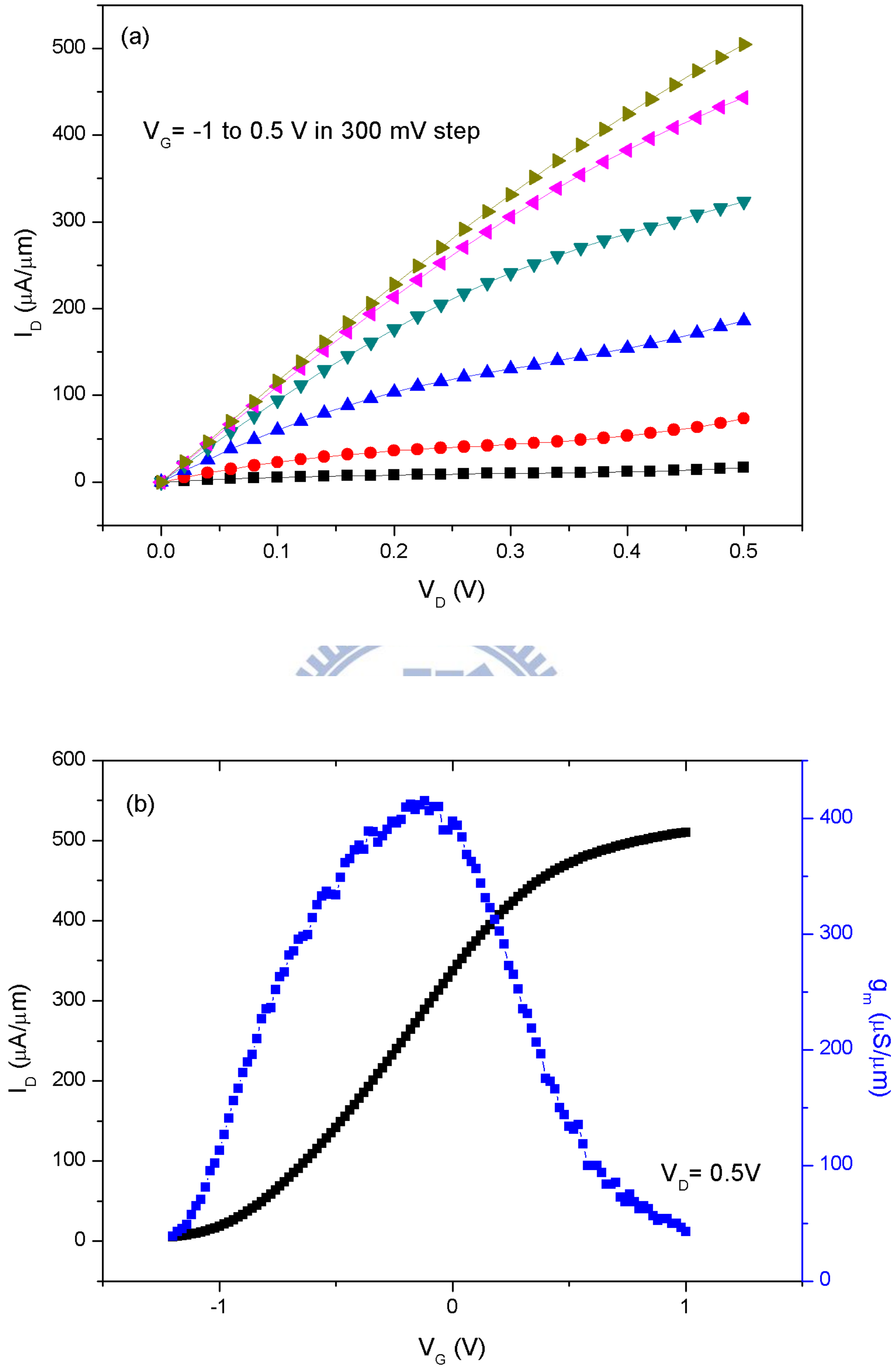


Fig. 4.10 (a) output characteristics and (b) transfer characteristics of ITC QW-MOSFET.

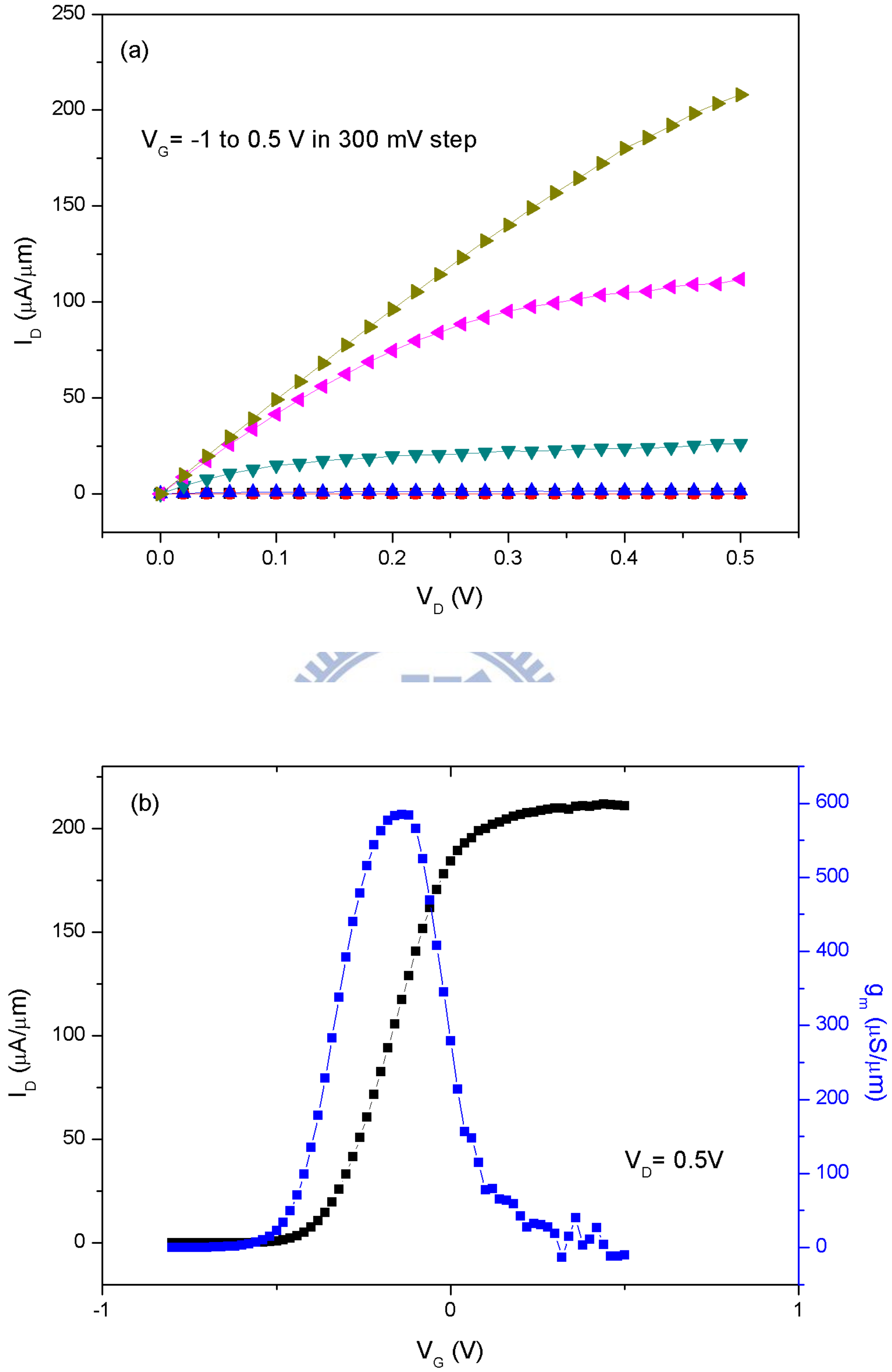


Fig. 4.11 (a) output characteristics and (b) transfer characteristics of RC HEMT.

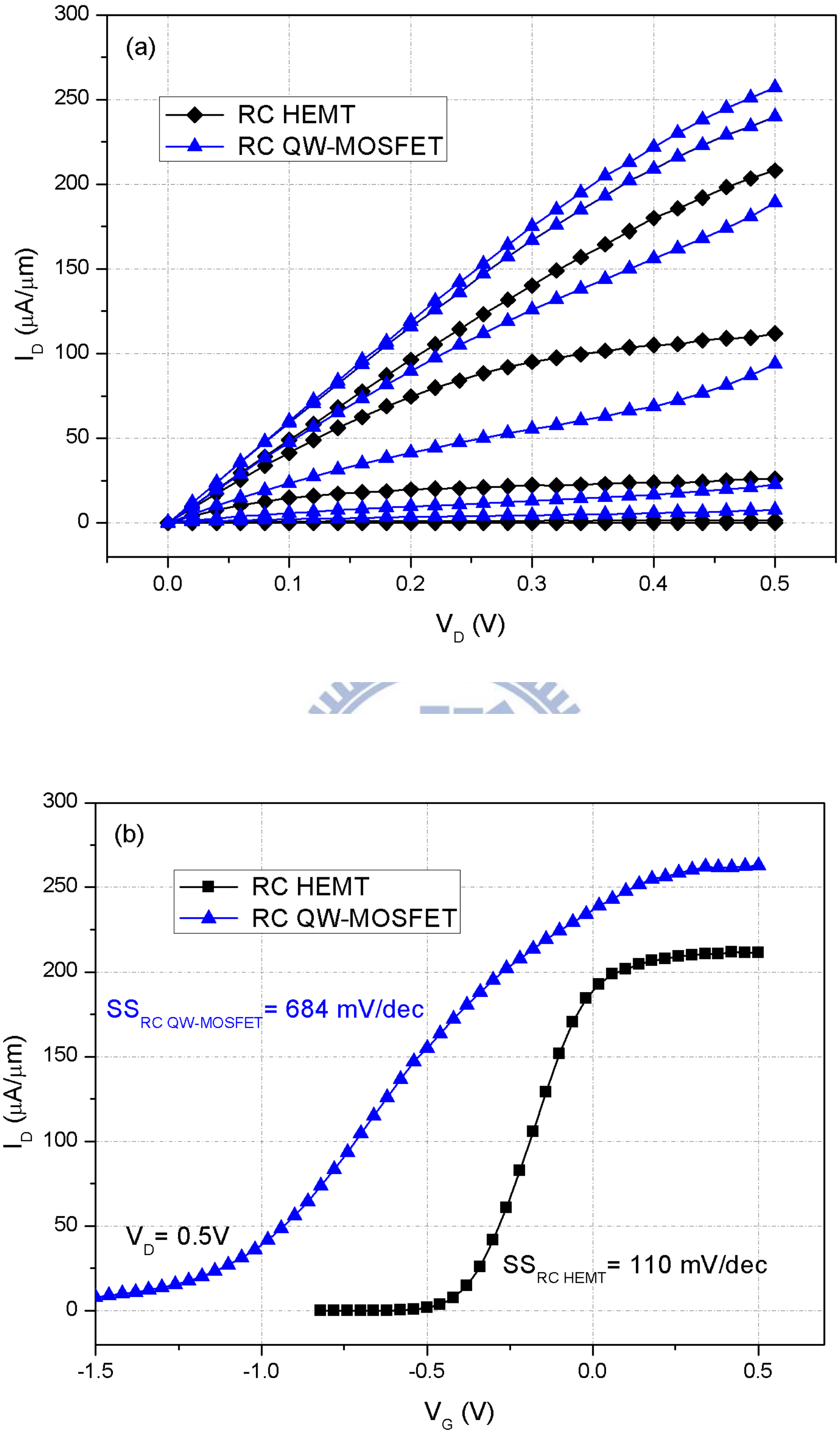


Fig. 4.12 RC QW-MOSFET vs. RC HEMT (a) I_D-V_D (b) I_D-V_G.

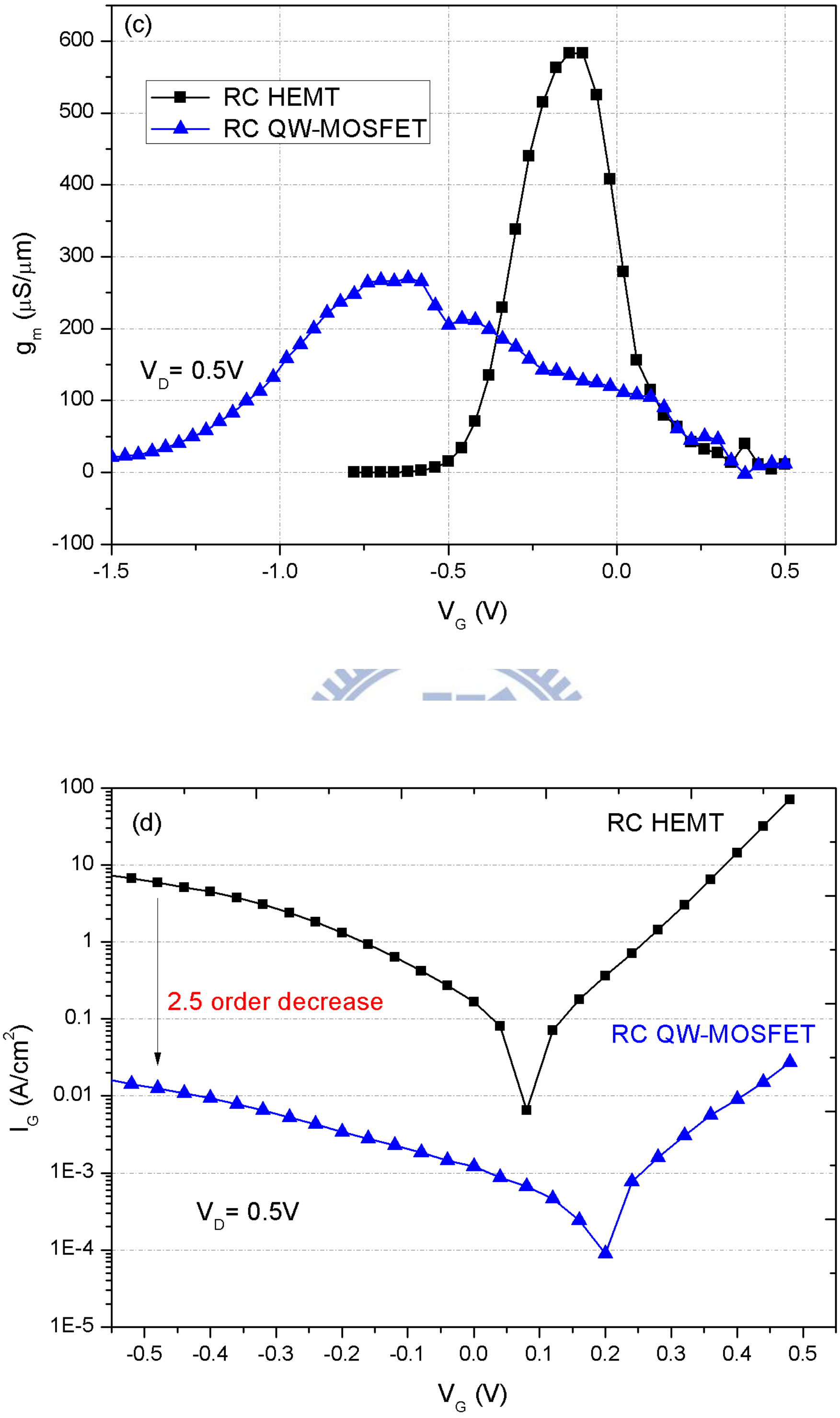


Fig. 4.12 (cont.) RC QW-MOSFET vs. RC HEMT (c) g_m-V_G (d) I_G-V_G.

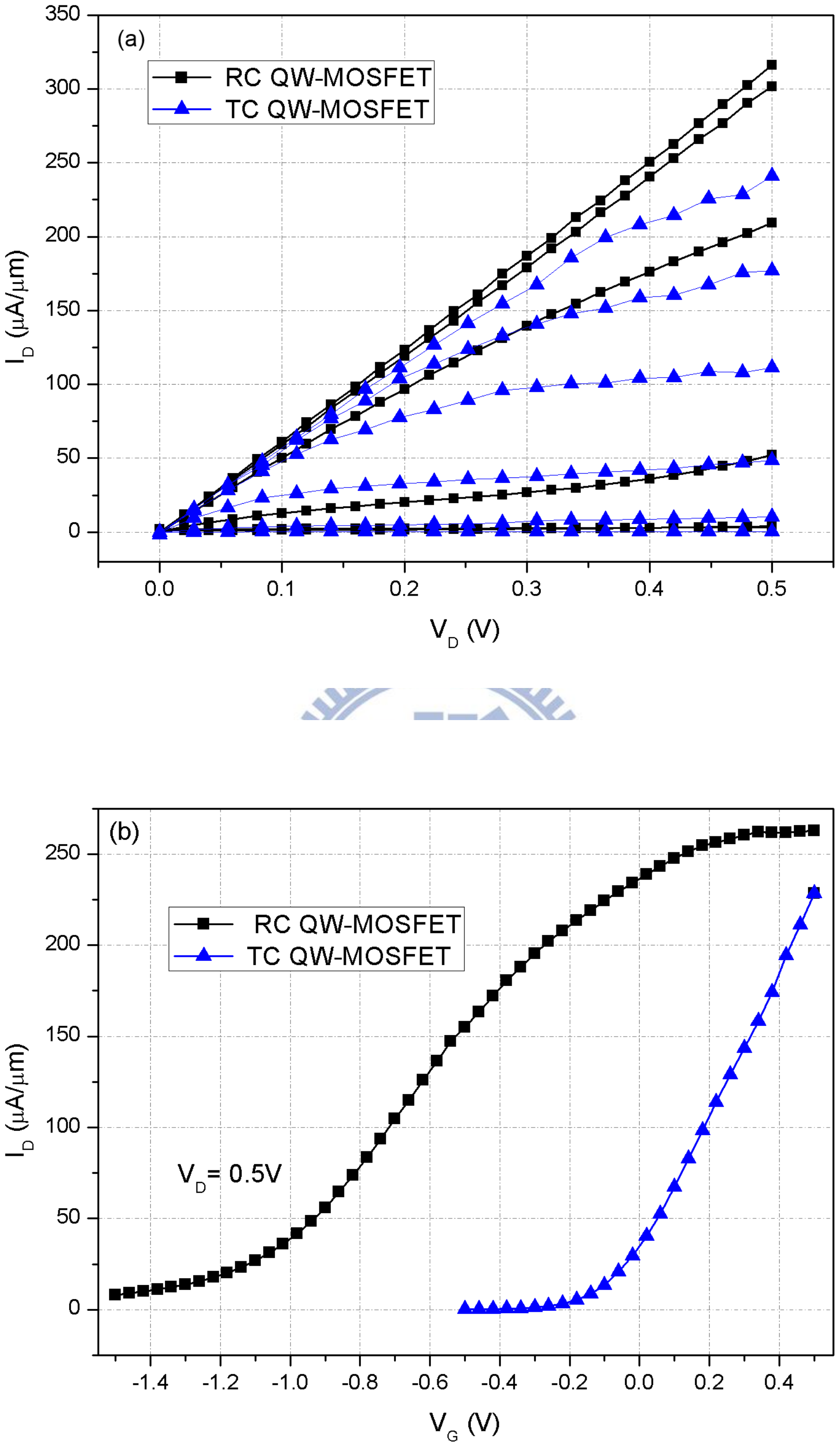


Fig. 4.13 TC QW-MOSFET vs. RC QW-MOSFET (a) I_D-V_D (b) I_D-V_G.

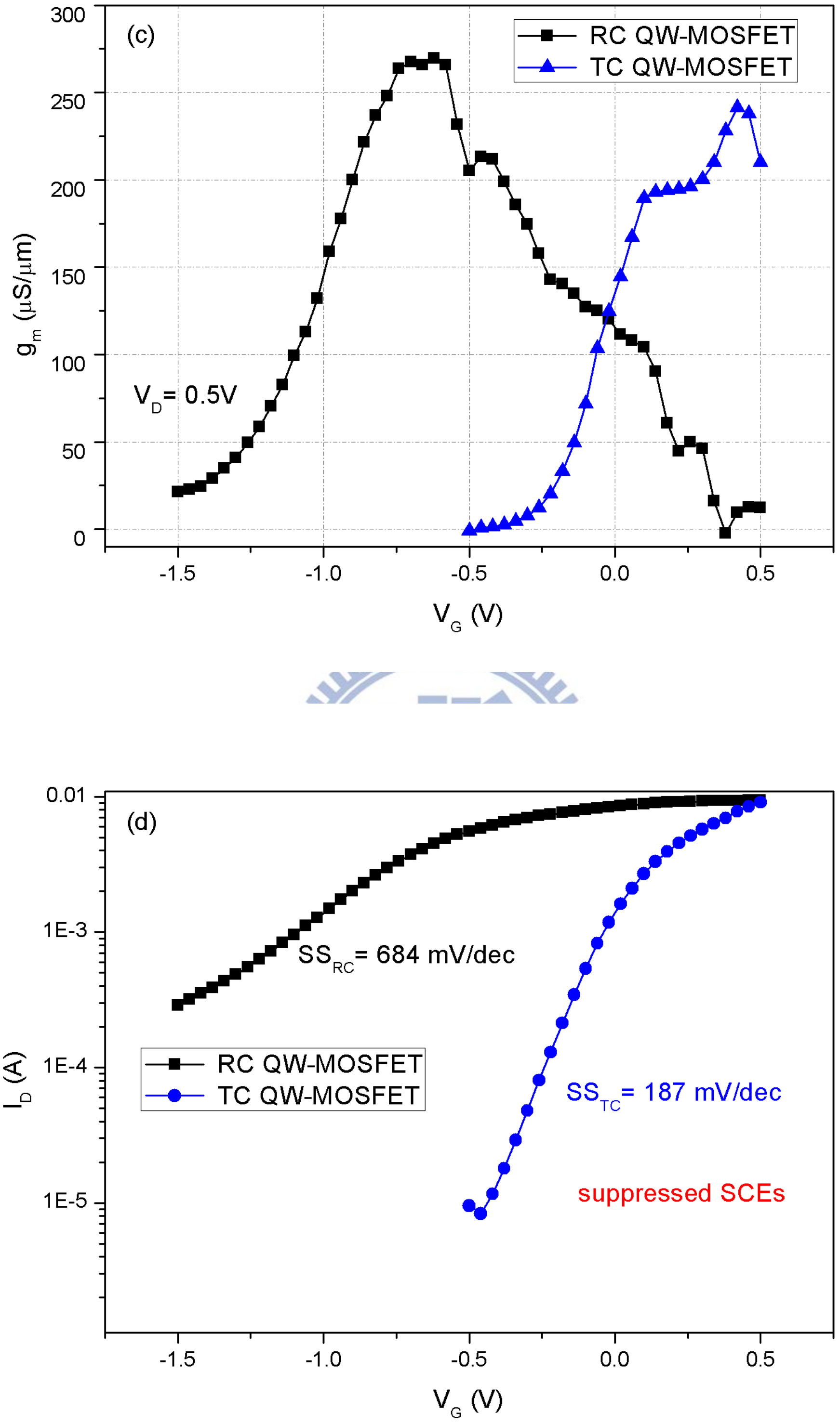


Fig. 4.13 (cont.) TC QW-MOSFET vs. RC QW-MOSFET (c) g_m-V_G (d) semi-log I_G-V_G.

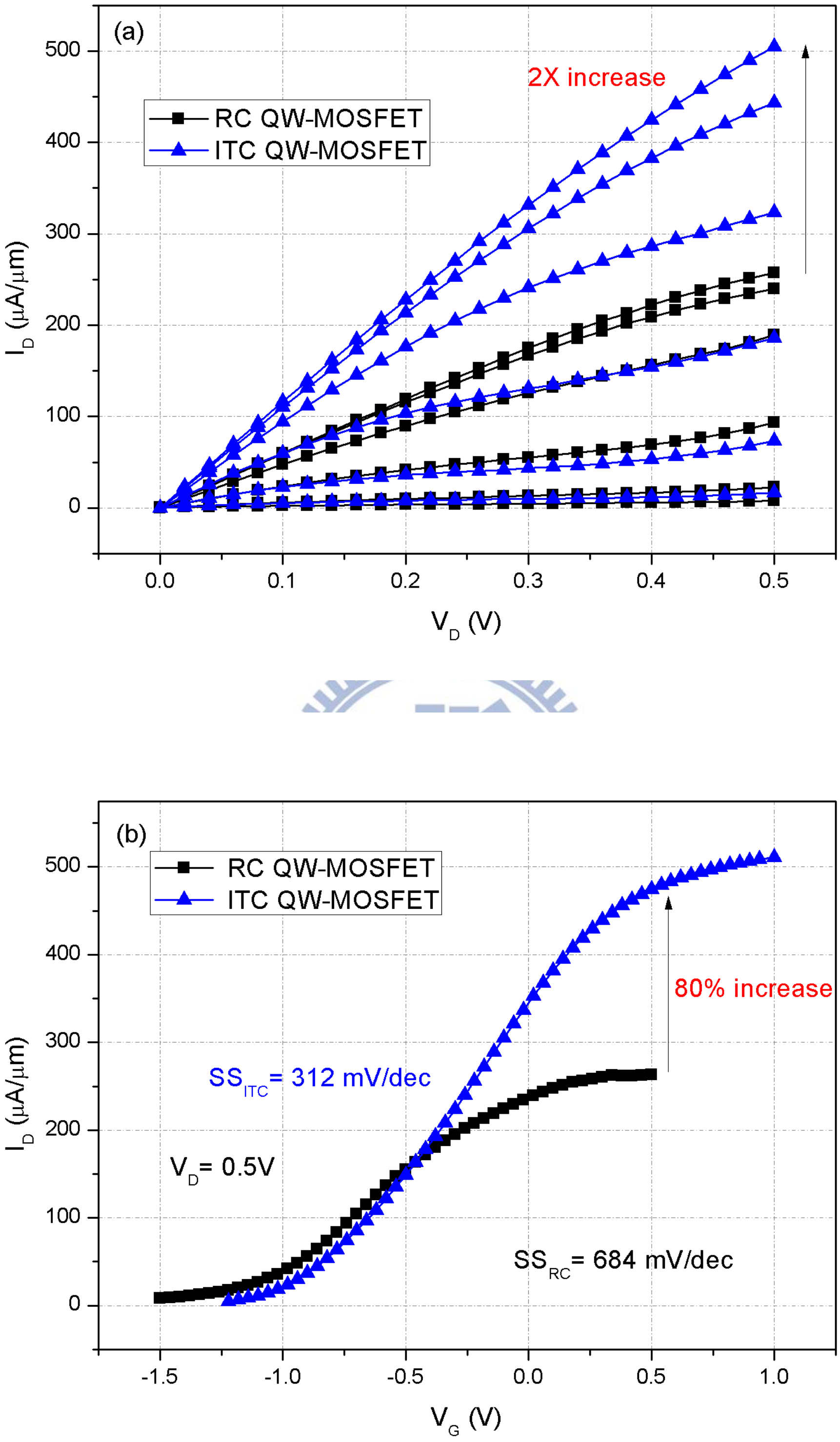


Fig. 4.14 ITC QW-MOSFET vs. RC QW-MOSFET (a) I_D-V_D (b) I_D-V_G.

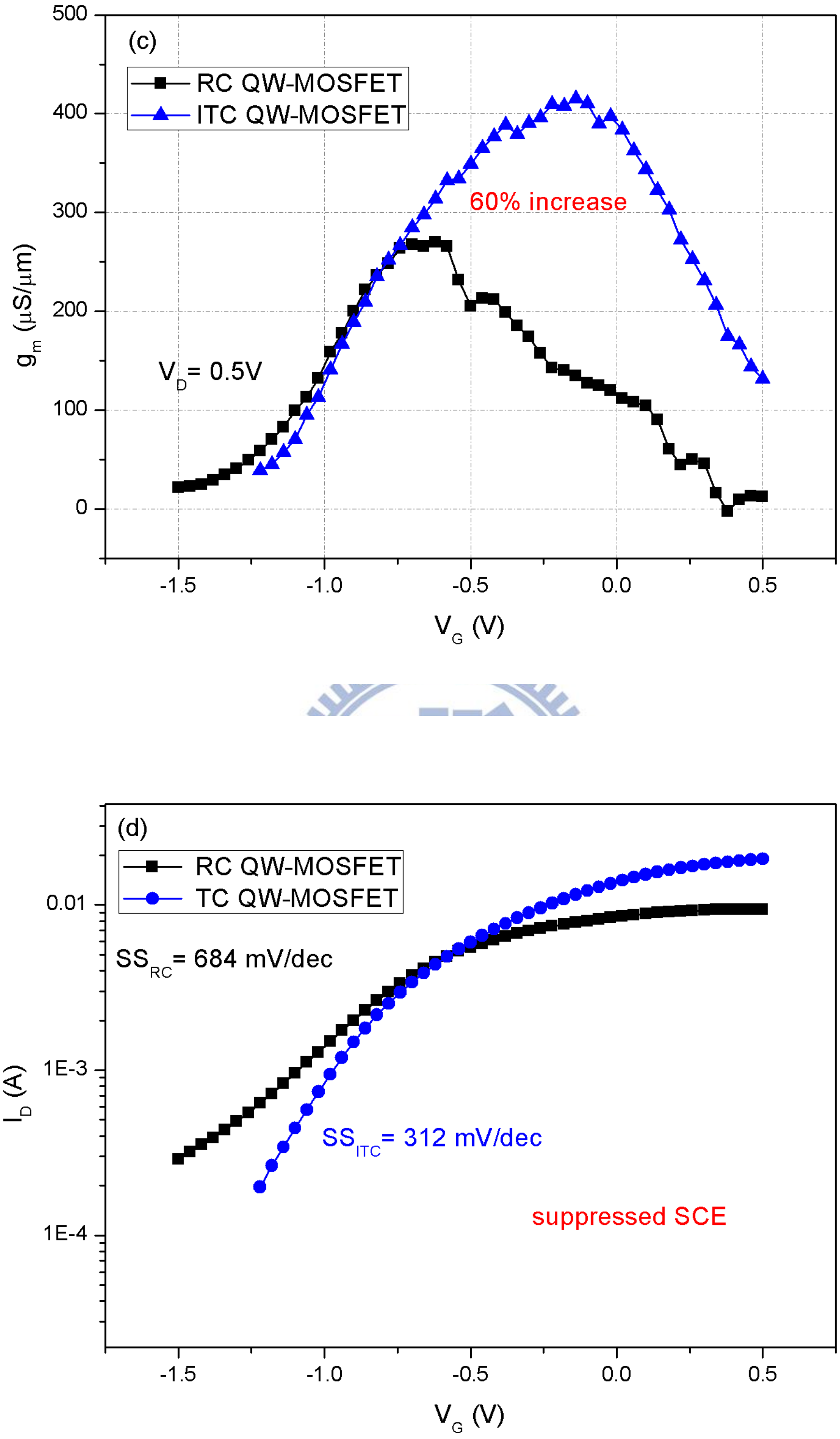
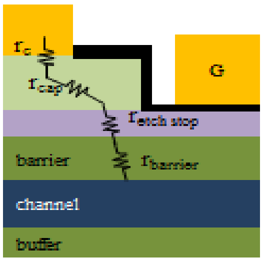


Fig. 4.14 (cont.) ITC QW-MOSFET vs. RC QW-MOSFET (c) g_m-V_G (d) semi-log I_G-V_G.

Normal-type QW-MOSFET



Inverted-type QW-MOSFET

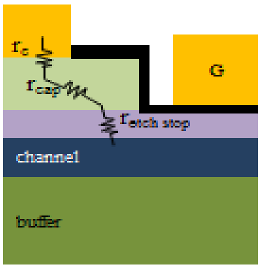


Fig. 4.15 The equivalent circuits near the S/D side in term of resistance for normal-type and inverted-type QW-MOSFETs.

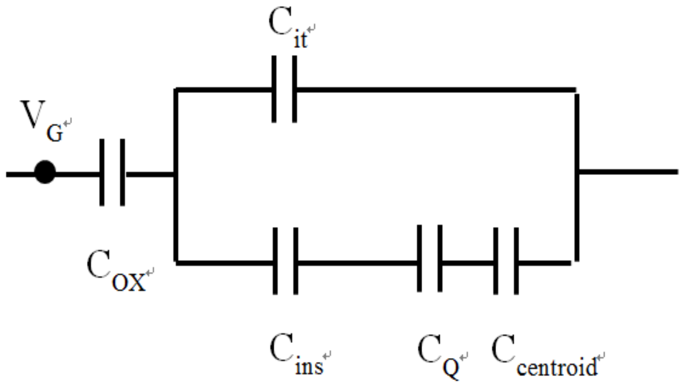


Fig. 4.16 The equivalent circuits of composite channel QW-MOSFETs' gate stack in term of capacitance, where the subscripts *ox*, *it*, *ins*, *Q*, *centroid* stand for the capacitance component of gate dielectric, interface states, insulator layer (i.e., InP and InAlAs), quantum capacitance, and centroid capacitance.

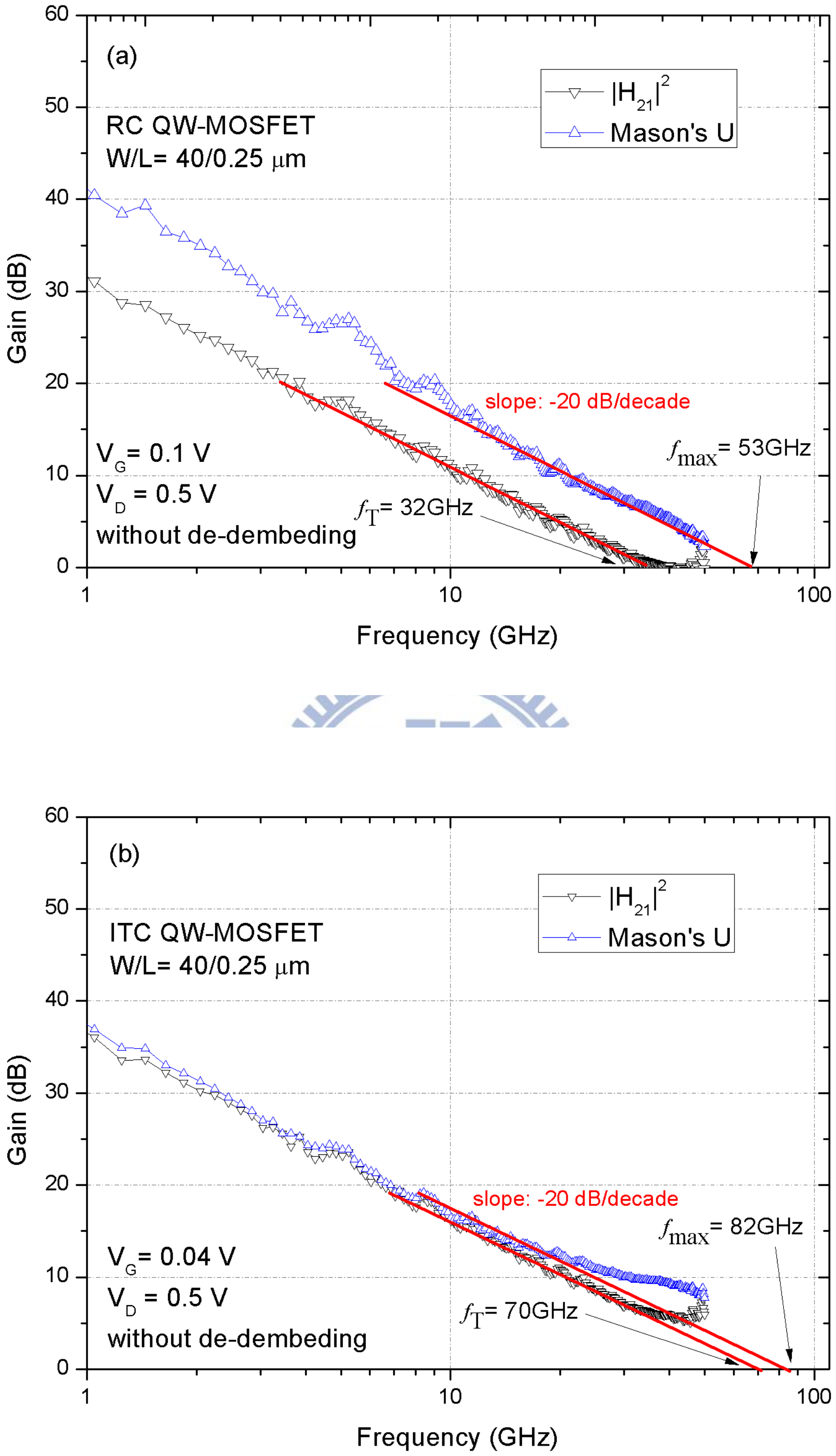


Fig. 4.17 Microwave characteristics of (a) RC QW-MOSFET (b) ITC QW-MOSFET.

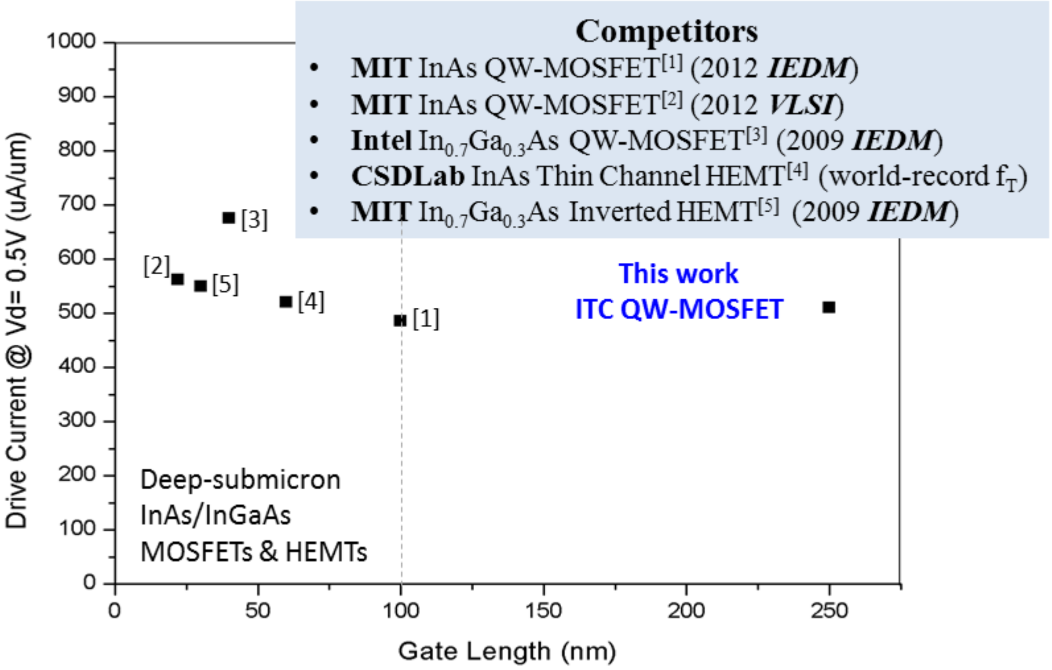


Fig. 4.18 Benchmarking of the InAs/InGaAs MOSFETs and HEMTs. The ITC QWMOSFET is benchmarked to the similar works using InAs and high-In InGaAs channels. The benchmarked devices are made by [29], [28], [25], [18], and [13], respectively.

Chapter 5
Hysteresis Effect

5.1 Hysteresis Phenomena

The hysteresis phenomena were observed in the transfer characteristics of the InAs QW-MOSFETs by sweeping the gate voltage forth and back, as shown in Fig. 5.1 where the forward-sweep is defined as the gate biasing starts from negative value to positive value. The hysteresis phenomena can be categorized into two facts: 1) in the linear scale I_D-V_G curve (Fig. 5.1 (a)), the I_D in the reverse-sweep is higher than forward-sweep; 2) in the semi-log scale I_D-V_G curve (Fig. 5.1 (b)), the SS of forward-sweep is worse than reverse-sweep. Generally speaking, the V_T shift and the SS degradation were found in the hysteresis phenomena.

There are several mechanisms that cause V_T shift [32-35], such as the fixed oxide charge and the interface state generation. The former comes from the hot-carrier injection, and the latter is also due to the hot-carriers. The hot-carrier injection causes positive V_T shift for n-channel MOSFETs since negatively-charged carriers are accelerated by the high electrical field and are injected from the channel to the gate dielectric. The hot-carrier injection not only introduces a positive V_T shift, but also degrades the quality of gate dielectric, causing a higher gate leakage by creating a percolation leakage path. On the other hand, the impact ionization near drain side leads to the generation of electron-hole pairs (EHP), and the electrons possessing high energy are able to generate interface states at the high-*k*/semiconductor interface. Once the generated-states are filled with carriers, the charged states manifest itself as a cause of Columbic scattering, leading to the mobility degradation and hence the degradation in device performance.

However, both V_T shift and SS degradation were observed in our experiment (Fig. 5.1). This result suggested that the V_T shift is not due to the fixed oxide charge, since the fixed oxide charge only gives rise to the V_T shift instead of the SS degradation. Moreover, the gate leakage currents of the forward-sweep and reverse-sweeps were the same (Fig. 5.2.) No observable change in I_G indicated that no percolation path is generated in the gate dielectric during gate bias sweeps, so the hot-carrier-injection is not responsible for our hysteresis phenomena. Besides, even though the interface-state generation is able to cause SS degradation, the generated interface-states are impossible to recover by simply sweeping the gate voltage forth and back. Therefore, neither the fixed oxide charge nor the interface-states generation is the cause of our hysteresis phenomena in the transfer characteristics.

5.2 Physics Origin and Proposed Models

The physics origin of those phenomena is proposed to be based on the trapping and de-trapping of the interface states, which modulate the V_T during gate bias sweeping and hence affect the I-V characteristics.

The mechanism of the charging and discharging of the acceptor-like interface states is depicted by Fig. 5.3. The acceptor-like states lay between the Fermi level of semiconductor (E_{Fs}) and the charge neutral level (E_{CNL}). At equilibrium, those states are filled with electrons and are negatively-charged. The *net* density of the acceptor-like interface states, N_{it} (/cm^2), can be expressed as:

$$N_{it} = \int_{E_{F,CNL}}^{E_F} D_{it}(E)\, dE \tag{5.1}$$

which is negatively-charged and corresponds to the area under the $D_{it}(E)$ vs. energy curve shown in Fig. 5.3. The charged states manifest itself as the virtual negative gate bias and hence increase the V_T by qN_{it}/C_{OX}, according to Eq. (A.6). It implies that the ΔV_T caused by the charged states is proportional to the number of the *charged* interface states. It is noticeable that N_{it} is a function of E_F, and E_F can be modulated by V_G. As the gate is biased at positive value (Fig. 5.3 (c)), the difference between E_{Fs} and E_{CNL} increases compared to the condition of $V_G = 0$ V (Fig. 5.3 (b)); thus more acceptor-like states are charged, resulting in a higher V_T. On the other hand, as the gate is biased at negative value (Fig. 5.3 (a)), the difference between E_{Fs} and E_{CNL} decreases. Hence less interface states are filled with electrons, resulting in a lower V_T compared to the V_T at $V_G = 0$ V. Therefore, in the forward sweep, where V_G sweeps from $V_G < 0$ to $V_G > 0$, the V_T increases dynamically as the gate bias moving toward positive direction. In the reverse sweep, where V_G sweeps from $V_G > 0$ to $V_G < 0$, the V_T decreases dynamically as the gate bias moving toward negative direction.

Consequently, the dynamics of V_T instability emerges: the filling process of acceptor-like states occurs in the forward sweep, while the emission process takes place in the reverse sweep.

The variation in V_T during V_G sweep results in the change in drain current. The I_D of long-channel MOSFET operated in the linear region can be expressed as:

$$I_D(lin.) = \frac{W_g C_G \mu}{L_g}[(V_G - V_T)V_D - \frac{V_D^2}{2}] \tag{5.2}$$

where W_g, L_g, μ, and C_G stand for the gate width, the gate length, the effective mobility of carriers, and the gate capacitance, respectively. The detail of the derivation of Eq. (5.2) and C_G is presented in the Appendix. Based on Eq. (5.2), the increase in V_T , which is caused by the charging of interface states in the forward-sweep, leads to a reduction in gate overdrive V_G - V_T, and hence decreased I_D (compared to the situation without the charging of acceptor-like interface states). Conversely, in the reverse-sweep, an increase in I_D is observed due to the reduction in V_T. If the difference in V_T between the forward-sweep and reverse-sweep is denoted as ΔV_T, (i.e., $\Delta V_T = V_{T,\text{ forward}} - V_{T,\text{ reverse}}$), then the change in I_D, $\Delta I_D = I_{D,\text{ forward}} - I_{D,\text{ reverse}}$, can be expressed as[3]:

$$\Delta I_D(lin.) = -\frac{W_g C_G \mu V_D}{L_g}\Delta V_T \tag{5.3}$$

In addition, the reduction/increase in I_D can be reviewed from the other perspective: the reduction/increase in I_D corresponds to the charging/dis-charging of acceptor-like states, which act as a parasitic capacitor. In the forward-sweep, a portion of the drain current is used for the charging of the parasitic capacitor. And the emission of electrons (i.e., the dis-charging of parasitic capacitors) in the reverse-sweep gives rise to the increase in I_D, since the Fermi level is lowered by V_G in the reverse-sweep.

Because ΔV_T is caused by the trapping/de-trapping of acceptor-like states, the relation between ΔV_T and ΔN_{it} , the difference in the quantity of the negatively-charged interface states between forward-sweep and reverse-sweep (i.e., $\Delta N_{it} = N_{it}$ (forward)- N_{it} (reverse)), can be simply deduced by using Eq. (A.6) and expressed as:

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[3] $\Delta I_D = I_{D,\text{ forward}} - I_{D,\text{ reverse}} = I_D(V_T = V_{T,\text{reverse}} + \Delta V_T) - I_D(V_T = V_{T,\text{reverse}})$

$$\Delta V_T = \frac{q\Delta N_{it}}{C_{OX}} \tag{5.4}$$

It is noticeable that the ΔN_{it} is not caused by the interface-states generation; ΔN_{it} is caused by the incomplete charging/dis-charging during V_G sweeps, since the deep level states possess longer emission time and cannot respond to quick V_G sweeps. Moreover, the forward-sweep SS degradation is attributed to the localized charge storage, which is also the cause of SS degradation for the charge-trapping SONOS devices [36-37].

To sum up, two physical parameters that monitor the hysteresis phenomena, ΔI_D and ΔV_T, are quantitatively described and their dependence on the charged interface states is also discussed in this section. The bias dependence will be investigated by examining these two physical parameters in the next section.

5.3 Bias Dependence

The investigations of the bias dependence of hysteresis phenomena were conducted on the InAs QW-MOSFET with ITC structure. Through the study of the dependence of: 1) ΔI_D-V_D; 2) ΔV_T-V_D; 3) ΔI_D-V_G sweep range; 4) ΔV_T-V_G, the bias dependences were not only studied, but also were consistent with our proposed mechanism for hysteresis phenomena.

5.3.1 ΔI_D -V_D Dependence

In order to examine the influence of the biased V_D on ΔI_D in the transfer characteristics, the ΔI_D of various V_D conditions as a function of V_G was measured and presented in Fig. 5.4. It shows that the hysteresis effect has more influence as the device V_G is in the “linear” region of the I_D-V_G curves. According to Eq. (5.3), it is not surprising that the ΔI_D increase with biased V_D. However, it should be noted that the effective mobility, the gate capacitance, and the ΔV_T are a function of V_G. Thus Eq. (5.3) should be rewritten in a more precise manner to address the bias dependence of every parameter.

$$\Delta I_D(lin.) = \frac{W_g C_G(V_G)\mu(V_G)\,V_D}{L_g}\Delta V_T(V_G) \tag{5.5}$$

Clearly, we cannot simply divide ΔI_D by a factor, $W_g C_G \mu V_D / L_g$, to extract the ΔV_T-V_G dependence, since both the mobility and the gate capacitance depend on V_G. Therefore we must use another method to extract the ΔV_T-V_G dependence. The dependence of ΔV_T -V_G and the proposed method will be discussed in Section 5.3.4.

The maximum $|\Delta I_D|$ as a function of biased V_D in the transfer curves is shown in Fig. 5.5. The adjusted R^2 of the linear fitting line is 0.98. It shows that the maximum ΔI_D is almost proportional to the biased V_D. The small deviation from the linear relationship demonstrates that the ΔV_T is still a function of V_D.

5.3.2 ΔV_T-V_D Dependence

The ΔV_T as a function of the biased V_D is shown in Fig. 5.6, where the V_T in the forward/reverse-sweeps is simply extracted by the linear extrapolation of I_D-V_G transfer curves. In the regime of lower V_D (V_D = 0.05 and 0.1 V), the ΔV_T is about 0.12 V. However, in the regime of "higher" V_D (V_D > 0.3 V), the ΔV_T is about 0.3 V. The ΔV_T increases with V_D and then "saturates" at specific value. This result shows that the V_D-accelerated channel electrons assist the charging process. Moreover, the specific V_D corresponds to the onset of faster increase in ΔV_T is about 0.3 V. This critical V_D corresponds to the required energy for electrons moving from the channel to the high-*k*/InP interface, so the ΔV_T saturates as the biased V_D larger than the critical V_D.

5.3.3 ΔI_D - V_G Sweep Range Dependence

To investigate the reversibility of the I_D-V_G curves in forward/reverse-sweeps, the transfer curves were measured with increasing $V_{G,max}$. All the curves were swept at V_D of 0.5 V, with V_G starting from the same negative bias (-1 V) to different $V_{G,max}$ and then reverse. The I_D-V_G curves with different sweep range were measured and presented in Fig. 5.7. The overlapped forward and reverse curves shown in the Fig 5.7 (a) not only manifest that the ΔV_T is recoverable upon V_G sweep, but also are the direct evidence that ΔV_T is caused by the charging/discharging of interface states, since the generated-interface-states and the fixed oxide charge are impossible to recover by sweeping V_G forth and back. Fig 5.7 (b) shows that the maximum ΔI_D

increases with V_G sweep range since more interface states are charged as the $V_{G,max}$ increases.

5.3.4 ΔV_T-V_G Dependence

In Section 5.3.1, we mentioned that the difficulties in the extraction of ΔV_T-V_G dependence, since both the mobility and the gate capacitance depend on V_G. Furthermore, the ΔV_T extraction method used in Section 5.3.2 (linear extrapolation of I_D-V_G) discards the V_G dependence; hence that method is inappropriate to explore the ΔV_T-V_G dependence. Thus we must use a method to cancel out the term $W_g C_G \mu V_D / L_g$ without losing the V_G dependence.

A simple method is used to evaluate ΔV_T-V_G dependence, which is considered to be related to ΔN_{it}. It is noticeable that the term we want to eliminate is exactly the g_m, which is given by:

$$g_m = \frac{dI_D}{dV_G} = \frac{W_g C_G(V_G)\mu(V_G)V_D}{L_g} \qquad (5.6)$$

Therefore, the ΔV_T preserving the V_G dependence can be extracted by dividing Eq. (5.5) by Eq. (5.6). This method features the simplicy of the extraction process. It does not have to extract the C_G-V_G and μ-V_G dependence; the former are usually characterized by typically capacitance-voltage (C-V) measurement, and the latter are usually extracted by split C-V method.

The ΔV_T-V_G dependence is shown in Fig. 5.8. The ΔV_T increases with V_G, and the adjusted R^2 of the linear fitting line is 0.97. This result suggests that the ΔV_T is almost proportional to V_G. This result is also the strong and direct evidence that the ΔV_T is caused by the charging/dis-charging of acceptor-like states.

The quantity of charged interface states of two V_G biases, V_{G1} and V_{G2}, as a function of energy is presented in Fig. 5.9 where the E_{F1} and E_{F2} correspond to the Fermi level at the gate bias of V_{G1} and V_{G2}, respectively. The difference in N_{it} between two gate biases, (i.e., $\delta N_{it} = N_{it}(E_{F2}) - N_{it}(E_{F1})$) can be approximated as:

$$\delta N_{it} \approx D_{it} \times \left(E_{F2} - E_{F1}\right) \qquad (5.7)$$

Furthermore, the difference in Fermi level between two gate biases (E_{F2}-E_{F1}) is proportional to V_{G2}-V_{G1}, since $(E_{F2} - E_{F1}) = q\,(V_{G2} - V_{G1})$. Therefore, based on Eq. (5.4) and Eq. (5.7), the ΔV_T is expected to linearly increase with V_G if the variation in

D_{it} is small. Our experimental result is consistent with the theoretical analysis. Therefore, the high linearity verifies the proposed physics origin of hysteresis phenomena.

On the other hand, the ΔV_T vs. V_G curves of various biased V_D are presented in Fig. 5.10. The slopes of all fitting curves are almost the same (Fig. 5.11). Then we must ask ourselves a question: what is the physical meaning behind this slope?

In order to answer this question, we start from the derivation of ΔV_T with respect to V_G:

$$\frac{d\Delta V_T}{dV_G} = \frac{q}{C_{OX}}\frac{d\Delta N_{it}}{dV_G} = \frac{1}{C_{OX}}\frac{d\Delta Q_{it}}{dV_G} = \frac{\Delta C_{it}}{C_{OX}}$$
$$= \frac{q^2}{C_{OX}} D_{it} \qquad (5.8)$$

From Eq. (5.8), we can see that the slope ($d\Delta V_T$ /dV_G) is proportional to D_{it}, since C_{OX} is constant for specific device. The reason why all V_D biases has the same slope is revealed: the slope corresponds to the D_{it} of the MOS transistor. Therefore, we find out a new method to extract the D_{it} value in the gate stack of transistor.

$$D_{it} = \frac{C_{OX}}{q^2}\frac{d\Delta V_T}{dV_G}(unit : cm^{-2}J^{-1}) \qquad (5.9)$$
$$= \frac{C_{OX}}{q}\frac{d\Delta V_T}{dV_G}(unit : cm^{-2}eV^{-1}) \qquad (5.10)$$

In this case, the extracted D_{it} value is 1.86×10^{12} $cm^{-2}eV^{-1}$. Since the proposed extraction method is based on the measurement of hysteresis effect, in which the value of ΔI_D depends on the speed of V_G sweep, the extracted D_{it} value in this case[4] only corresponds to the deep level states which has emission time longer than the measurement speed (about 30 ms). Therefore, pulse I-V measurement is required for the detection of fast interface states. The key feature of the proposed method is: it evaluates D_{it} without using MOS capacitor; hence it directly reflects the D_{it} value in a MOS transistor.

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[4] In our DC measurement, the sweep rate and step are 0.6 V/s and 0.02 V.

5.4 Summary

An understanding regarding the hysteresis effect is obtained in terms of the exploration of its mechanism and bias dependence. Moreover, a new method to evaluate transistor D_{it} is proposed. The conclusions of this chapter are drawn and listed as follows:

- The origin of hysteresis phenomena is proposed to be based on the trapping and de-trapping of acceptor-like states. The charging/dis-charging process dynamically modulates the V_T so that the changes in I_D and SS occur in the I_D-V_G transfer curves.
- The change in drain current is due to the variation in V_T upon V_G sweeps, in which the forward-sweep possess higher V_T and the reverse-sweep has lower V_T. Moreover, the change in SS is due to the localized charge storage in the interface states instead of the interface-states generation. The mechanism of SS degradation is similar to charge-trapping memory devices, like SONOS.
- Various bias dependences are characterized and explained. The reversibility of different V_G sweep range and the linear relationship between ΔV_T and V_G confirms the proposed mechanism. It is shown that the ΔI_D increases with biased V_D and V_G sweep range, and the ΔV_T increases with biased V_D and V_G.
- A new D_{it} extraction methodology is proposed. The proposed method is able to extract the D_{it} value of a transistor, so it can be used to directly evaluate the interface properties of the gate stack of transistors.

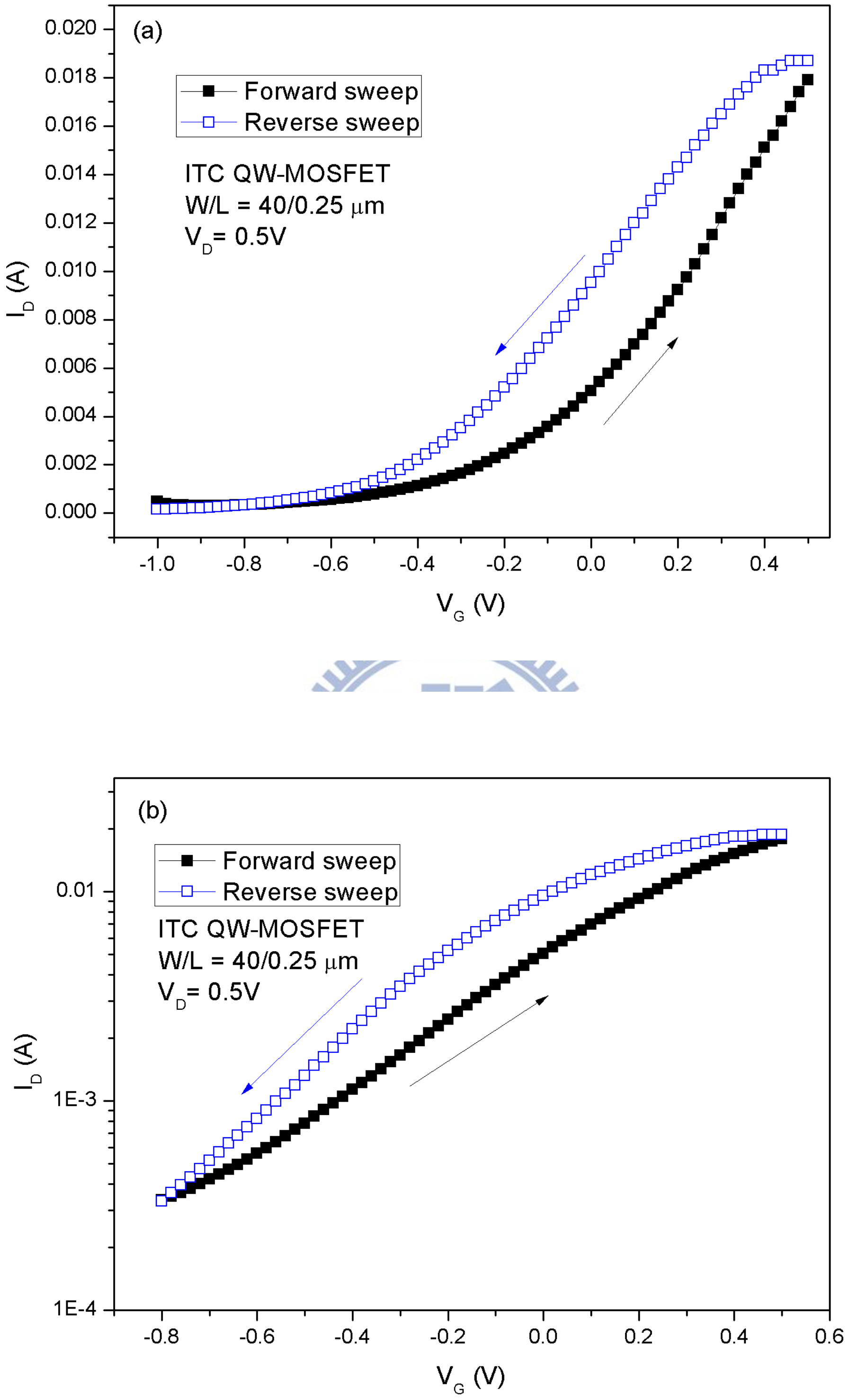

Fig. 5.1 The hysteresis phenomena in I_D-V_G transfer characteristics: (a) linear scale (b) semi-log scale.

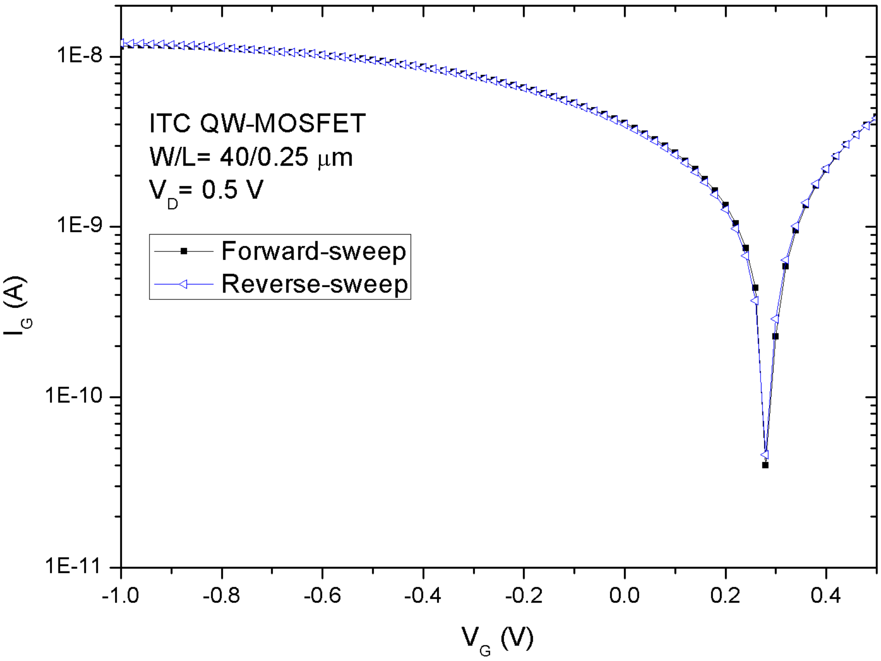

Fig. 5.2 The gate leakage current of the forward-/reverse-sweeps.

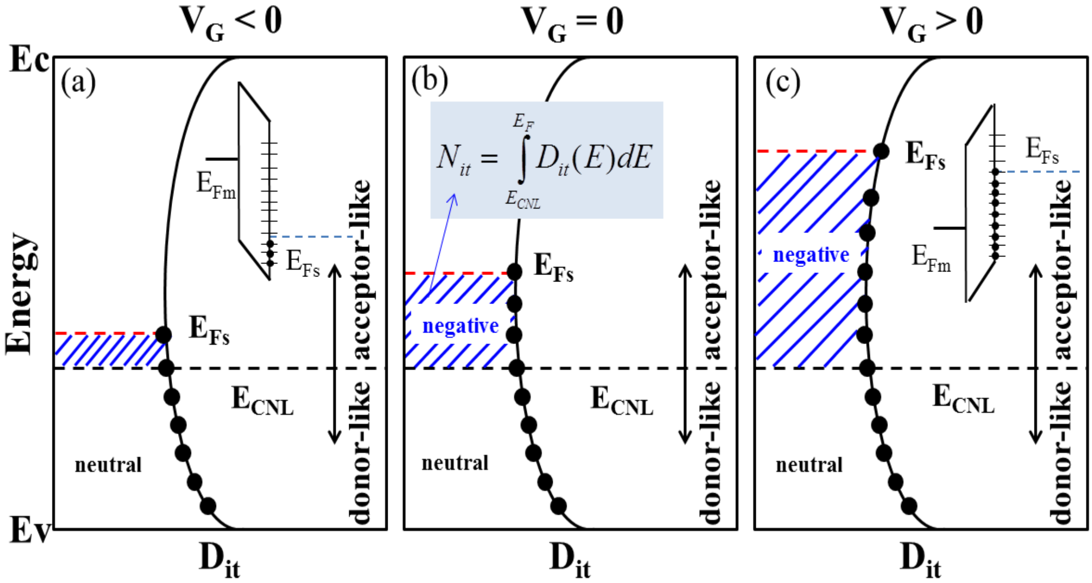

Fig. 5.3 The mechanism of how V_G modulates the amount of charged acceptor-like interface states. (a) $V_G > 0$ (b) $V_G = 0$ (c) $V_G < 0$.

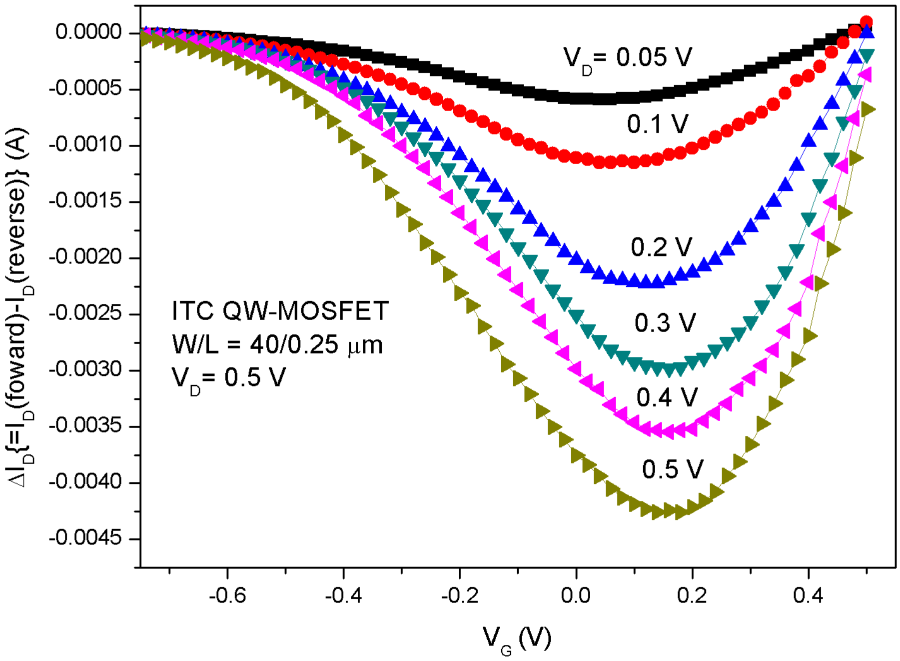

Fig. 5.4 ΔI_D -V_D Dependence: the ΔI_D of various drain bias conditions as a function of V_G, where the ΔI_D is defined as: ΔI_D = I_D (forward) - I_D (reverse) in the transfer characteristics.

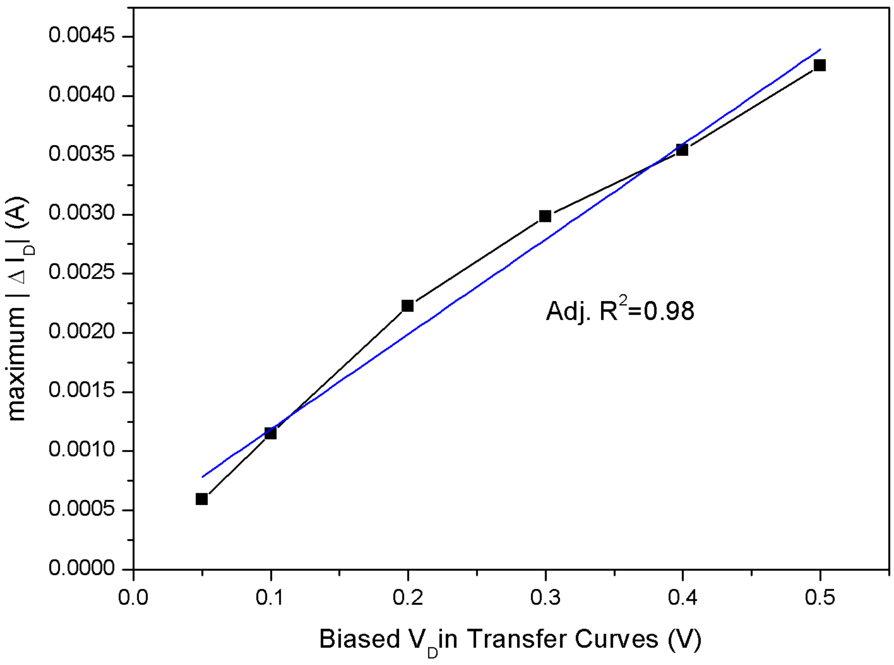

Fig. 5.5 The maximum $|\Delta I_D|$ as a function of biased V_D in the transfer curves. The adjusted R^2 of the linear fitting line is 0.98.

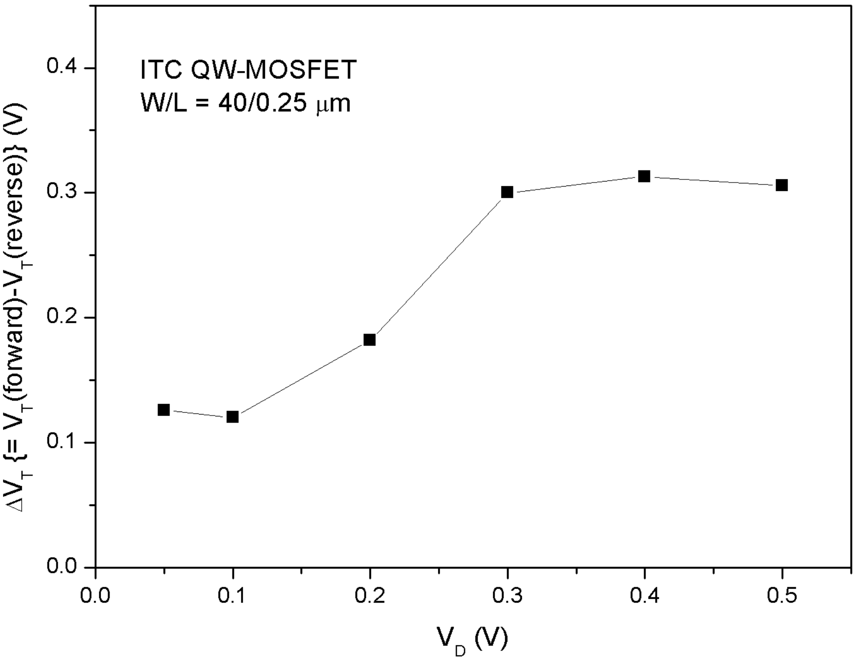

Fig. 5.6 The ΔV_T as a function of the biased V_D, where the V_T in the forward and reverse-sweeps is simply extracted by the linear extrapolation of I_D-V_G transfer curves.

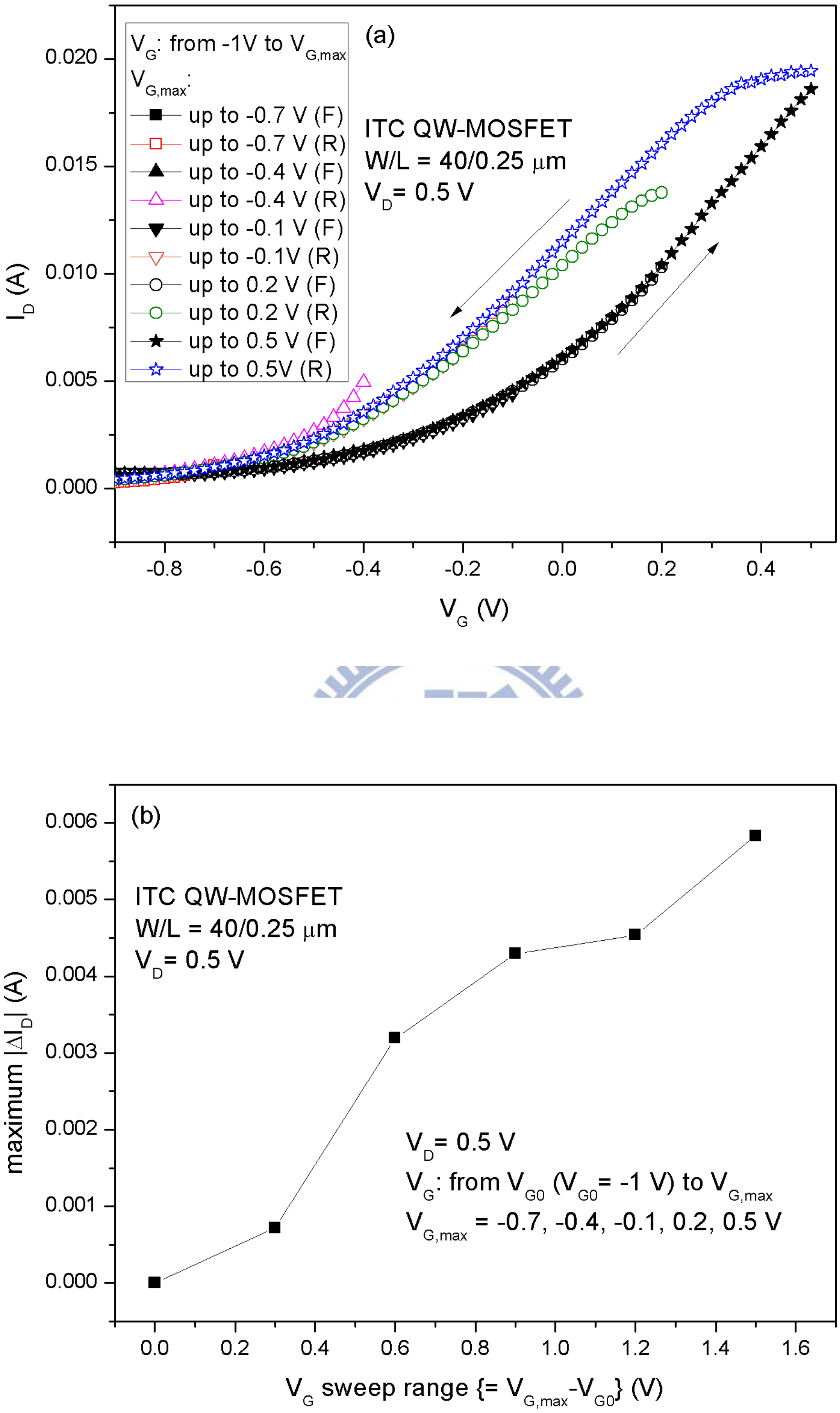

Fig. 5.7 ΔI_D - V_G Sweep Range Dependence: (a) the I_D-V_G curves with different sweep range (b) the maximum ΔI_D as a function of V_G sweep range, which is defined as: V_G sweep range = $V_{G,max}$ - V_{G0}.

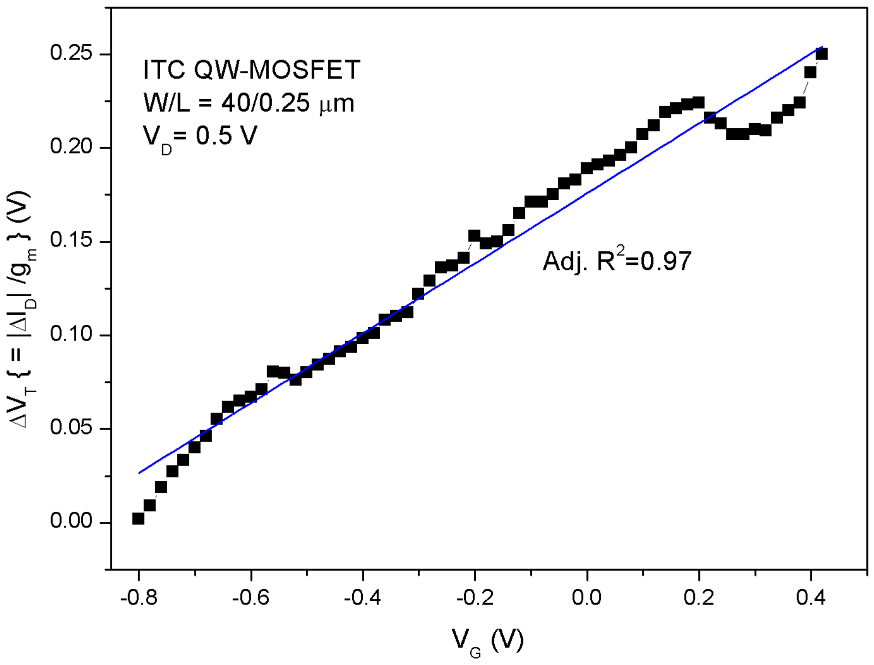

Fig. 5.8 The ΔV_T-V_G dependence, where the ΔV_T is extracted by the proposed method shown in Section 5.3.4.

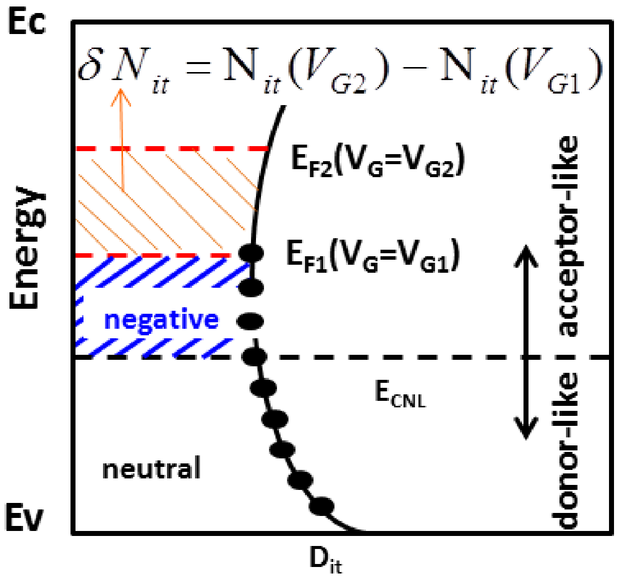

Fig. 5.9 The quantity of charged interface states of two V_G biases, V_{G1} and V_{G2}, as a function of energy, where the E_{F1} and E_{F2} correspond to the Fermi level at the gate bias of V_{G1} and V_{G2}, respectively. The difference in N_{it} between two gate biases is denoted as δN_{it}.

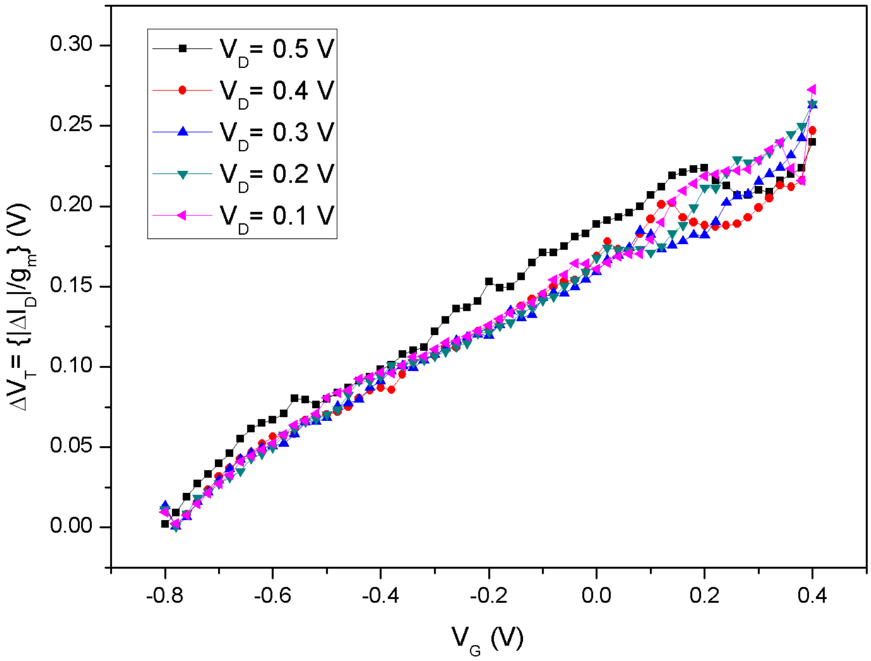

Fig. 5.10 The ΔV_T vs. V_G curves of various biased V_D.

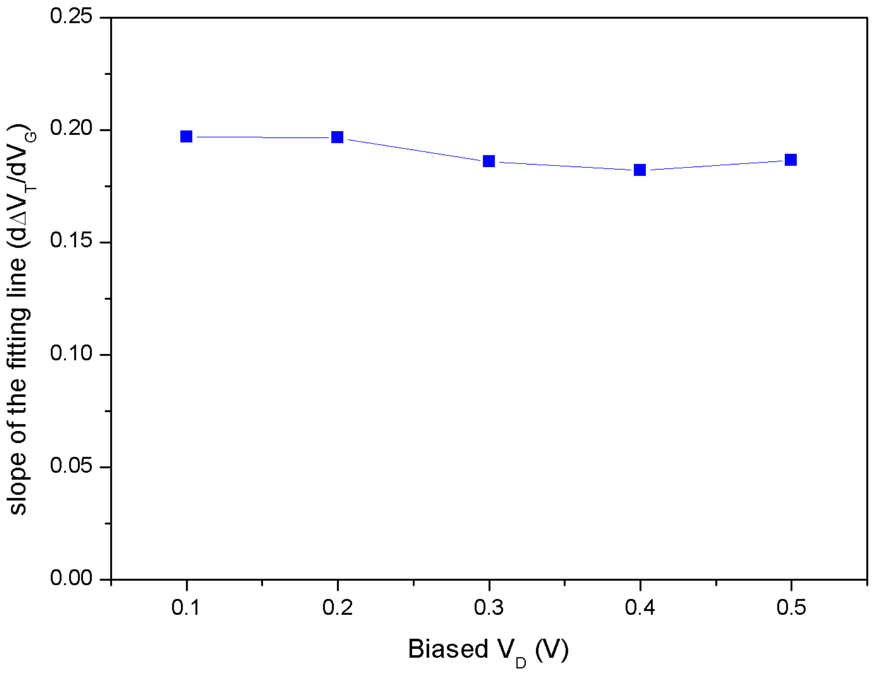

Fig. 5.11 The slope of the fitting line as a function of biased V_D.

Chapter 6
Conclusions

This dissertation investigated two major issues in InAs QW-MOSFETs. A gate-last process for buried channel InAs MOS transistors was developed, serving as the foundation of the study of bandgap engineering of composite channel and the investigation of the hysteresis effect. Contributions of each subject in this work are summarized as follows.

Regarding the bandgap engineering in the composite channel, the simulation is firstly conducted to explore the impact of epitaxial structures (in terms of the thickness of InGaAs/InAs/InGaAs layers and the In composition of InGaAs sub-channel) on the carrier confinement and apparent mobility. The simulation showed that optimized sub-channel In composition and thickness ratio may improve the carrier confinement and hence transport properties. Next, InAs QW-MOSFETs with three kinds of epitaxial structures were fabricated and characterized. The experimental results show that: 1) the device with thinner composite channel structure effectively suppresses SCEs by reducing gate-to-channel distance; 2) the ITC device demonstrates good DC and RF performance: I_D of 505 μA/μm, peak g_m of 412 μS/μm, extrinsic f_T of 70 GHz, and extrinsic f_{max} of 82 GHz. Consequently, the ITC InAs QW-MOSFET is a promising candidate for future low-power high-performance logic and microwave applications if the optimized surface treatment, scaled gate length, and reduced EOT are realized.

About the hysteresis effect, a mechanism is proposed to describe the hysteresis effect. The charging/dis-charging process of interface states is responsible for the hysteresis phenomena. Furthermore, several bias dependences were discussed through the electrical analysis. Besides, based on the measurement of hysteresis effect, a new method that can directly monitor the high-*k*/semiconductor interface in the gate stack of transistor is proposed.

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Appendix
Physically-based Models for Quantum Well MOSFET

A.1 Threshold Voltage Calculation

For the convenience of derivation, the device is assumed to be biased at flat band condition. The schematic band diagram of normal-type InAs QW-MOSFET at flat band condition is show in Fig. A.1, where $\Delta E_{c,HK/InP}$, $\Delta E_{c,InP/InAlAs}$, and $\Delta E_{c,InAlAs/InGaAs}$, are the conduction band discontinuity in high-*k*/InP, InP/InAlAs, and InAlAs/InGaAs interfaces. The half of the difference in band gap ΔE_g corresponds to the "depth" of the $In_xGa_{1-x}As/InAs/In_xGa_{1-x}As$ sub-QW. The value of ΔE_g can be calculated according to the alloy composition of $In_xGa_{1-x}As$.

$$\Delta E_g = (1-x)[E_g(GaAs) - E_g(InAs)] \qquad (A.1)$$

The difference between the eigenvalue of first sub-band and the conduction band edge of InAs is denoted as ϕ_{1sb}.

$$\phi_{1sb} = \mathrm{E}\,(1^{st}\ \text{sub-band}) - \mathrm{E_c}\,(\text{InAs}) \qquad (A.2)$$

And the difference between the conduction band edge of InAs and Fermi level is denoted as ϕ_{ch}.

$$\phi_{ch} = \mathrm{E_c}(\text{InAs}) - \mathrm{E_F} \qquad (A.3)$$

The V_T of QW-MOSFETs is the applied voltage that makes the E_F and the energy level of first sub-band exactly at the same level. Once the Fermi level is over the 1st sub-band, electrons accumulate in the $In_xGa_{1-x}As/InAs/In_xGa_{1-x}As$ sub-QW. And the sheet carrier density (n_s) in the QW is a function of the degree of Fermi level over the first sub-band. Thus, the V_T is temporarily given by:

$$V_T - V_{FB} = \phi_B - \frac{(\Delta E_{C,HK/InP} - \Delta E_{c,InP/InAlAs} + \Delta E_{C,InAlAs/InGaAs} + \frac{\Delta E_g}{2})}{q} + (\phi_{1sb} - \phi_{ch}) \qquad (A.4)$$

However, for III-V MOS transistors, it is not reasonable to neglect the effect of the fixed oxide charge and interface states. If we assume the fixed oxide charge is uniformly distributed within the high-*k* dielectric with charge density $N_{OX,bulk}$ (cm^{-2}), the amount of change in threshold voltage is given by:

$$\Delta V_{T,\,fixed\ oxide} = -\frac{qN_{ox,bulk}}{C_{ox}} \qquad (A.5)$$

Moreover, the change in V_T caused by interface states can be expressed as:

$$\Delta V_{T,acceptor\text{-}like\ \ states} = -\frac{qN_{it}(E_F)}{C_{ox}} \qquad (A.6)$$

where N_{it} is the net charge density of the interface states. It should be noticed that, because the acceptor-like states are negatively-charged as long as it traps electrons (i.e., N_{it} (E_F) is negative value, as shown in Fig. 5.3), the charged acceptor-like states results in a positive shift in V_T. Moreover, N_{it} is a function of E_F. It means that the V_T fluctuates with the gate biasing. This phenomenon suggests that the dynamics of interface states (i.e. trapping and de-trapping mechanism when the device operating in transient state) affects the electrical behaviors through the variation in V_T. The effect of interface states on the transfer characteristics has been discussed in Chapter 5.

Therefore, based on (A.4), (A.5), and (A.6), the modified expression for V_T is given by:

$$V_T - V_{FB} = \phi_B - \frac{(\Delta E_{C,HK/InP} - \Delta E_{c,InP/InAlAs} + \Delta E_{C,InAlAs/InGaAs} + \frac{\Delta E_g}{2})}{q} + (\phi_{1sb} - \phi_{ch}) - \frac{qN_{ox,bulk}}{C_{ox}} - \frac{qN_{it}(E_F)}{C_{ox}} \qquad (A.7)$$

On the other hand, the V_T of inverted-type QW-MOSFET can be deduced from its band diagram (i.e., following the similar procedure), shown in Fig. A.2:

$$V_T - V_{FB} = \phi_B - \frac{(\Delta E_{C,\mathrm{HK}/InP} + \Delta E_{c,InP/InGaAs} + \Delta E_g/2)}{q} + (\phi_{1sb} - \phi_{ch}) - \frac{qN_{ox,bulk}}{C_{ox}} - \frac{qN_{it}(E_F)}{C_{ox}} \qquad (A.8)$$

A.2 Gate Capacitance Calculation

The C_G of surface channel MOSFET in strong inversion can be modeled by the capacitance components due to gate oxide (C_{OX}), depletion layer in the channel (C_d), and interface states (C_{it}), as shown in Fig. A.3 (a). But the C_G of QW-MOSFETs is more complex. In this section, we will discuss its model in the sequence of the multiple layers between gate oxide and composite channel, quantum capacitance, and centroid capacitance ($C_{centroid}$).

For normal type devices, the equivalent capacitance of the InP etch stop layer and InAlAs barrier layer can be modeled as insulator capacitance (C_{ins}). The C_{ins} consists of two kinds of dielectrics (InP and InAlAs) within the capacitor, shown in Fig. A.4 (a). The electric flux density *D*, within the capacitor is given by:

$$D = \varepsilon E = \rho_S = \frac{Q}{A} \tag{A.9}$$

where ρ_s is the sheet charge density, *Q* is the stored charge, and *A* is the area of the capacitor. Thus the electrical field in each dielectric is given by:

$$E_{InP} = \frac{D}{\varepsilon_1} = \frac{Q}{\varepsilon_1 A} \tag{A.10}$$

$$E_{InAlAs} = \frac{D}{\varepsilon_2} = \frac{Q}{\varepsilon_2 A} \tag{A.11}$$

Hence the electrical potential is expressed as:

$$\begin{aligned} V &= -\int_{y=0}^{y=(t_1+t_2)} E\, dl = -\int_{y=t_2}^{y=(t_2+t_1)} E_1\, dl - \int_{y=0}^{y=t_2} E_2\, dl \\ &= \frac{Q\,t_1}{\varepsilon_1 A} + \frac{Q\,t_2}{\varepsilon_2 A} = Q\left(\frac{t_1}{\varepsilon_1 A} + \frac{t_2}{\varepsilon_2 A}\right) = Q\left(\frac{1}{C_{InP}} + \frac{1}{C_{InAlAs}}\right) \end{aligned} \tag{A.12}$$

Therefore, the C_{ins} is the series combination of the capacitance component of InP and InAlAs, shown in Fig. A.4 (b).

$$C_{ins} = \frac{Q}{V} = \frac{1}{\left(\dfrac{1}{C_{InP}} + \dfrac{1}{C_{InAlAs}}\right)} \tag{A.13}$$

Eq. (A.13) can be extended to the general form.

$$C_{ins}^{\;-1} = \sum_i \frac{1}{C_i} \tag{A.14}$$

The concept and calculations of the quantum capacitance was introduced by Serge Luryi [38]. The 2DEG in a QW does not completely screen an applied transverse electric filed, and act as a capacitor in series. In other words, quantum capacitance corresponds to the extra energy, $Q/2C_Q$, to form a highly conducting 2DEG in the discrete energy levels in a QW with finite DOS. The quantum capacitance is known as:

$$C_Q = \frac{g_v m_\perp e^2}{\pi \hbar^2} \qquad (A.15)$$

where $m_\perp$ is the effective mass in the direction perpendicular to the plane of QW, and g_v is the valley degeneracy factor. For Si MOSFETs on (100) surface, the quantum capacitance is much larger than the capacitance of gate oxide, so that the C_Q term in the series combination can be neglect. Nevertheless, it is important to consider C_Q in III-V FETs, since III-Vs exhibit low effective mass and DOS. Thereby it requires more energy for filling the QW with electrons.

The centroid capacitance $C_{centroid}$, which is in series to quantum capacitance, is a consequence of the bell-shaped electron distribution in the QW. The distance from barrier interface to each charge is different. Similar to the modeling of Si MOSFET's inversion capacitance C_{inv} [39], the bell-shaped electron distribution can be modeled by an average distance $Z_{centroid}$, and $C_{centroid}$ is thereby modeled as the parallel plate capacitance:

$$C_{centroid} = \frac{k_{ch}\varepsilon_0}{Z_{centroid}} \qquad (A.16)$$

, where k_{ch} is the dielectric constant of the channel materials. It is difficult to extract precise $Z_{centroid}$, so some works employ the derivation of electron charge with respect to the energy difference between E_i and E_c. However, this method introduces more complexity upon extracting the sheet charge density as a function of $E_i - E_c$.

The equivalent circuit of total C_G is shown in Fig. A.3 (b). The C_G of InAs QW-MOSFET can be expressed by:

$$C_G = \frac{1}{\frac{1}{C_{OX}} + \left[C_{it} + \frac{1}{\frac{1}{C_{ins}} + \frac{1}{C_Q} + \frac{1}{C_{centroid}}}\right]^{-1}} \qquad (A.17)$$

where C_{OX} is the gate oxide capacitance, $C_{OX} = \varepsilon / t_{OX}$.

Rearrange Eq. (A.17), we have

$$C_G = C_{OX} \times \left\{ \frac{1}{1+[\frac{C_{it}}{C_{OX}} + \frac{1}{C_{OX}\left(\frac{1}{C_{ins}} + \frac{1}{C_Q} + \frac{1}{C_{centroid}}\right)}]^{-1}} \right\} \qquad (A.18)$$

From Eq. (A.18), we can clearly look into the effects of every capacitance component on the total C_G. The terms within the square bracket of Eq. (A.18) manifest itself as a reduction factor of C_G. The introduction of C_{it}, C_{ins}, C_Q, and $C_{centroid}$ inevitably reduces C_G. However, the weighting of the first term and the second term in the square bracket of Eq. (A.18) should be evaluated through the actual physical parameters of the devices. Moreover, Eq. (A.18) also suggests the direction of bandgap engineering and is consistent with the experimental results in Section 4.3: 1) The thinner etch stop layer and barrier layer give rise to higher C_{ins} and C_G; 2) The thinner channel layer results in a higher $C_{centroid}$; 3) The higher EOT increases C_{OX}; 4) The better interface quality reduces C_{it} since C_{it} is proportional to D_{it}.

A.3 Current-Voltage Characteristics and Subthreshold Behaviors

Based on Eq. (A.7) and Eq. (A.17), we are able to derive the I-V behaviors and its related properties such as g_m and SS by using charge control model and gradual channel approximation in an analog fashion to the well-developed Si MOSFET equations [1].

$$I_D(lin.) = \frac{W_g C_G \mu}{L_g}[(V_G - V_T)V_D - \frac{V_D^2}{2}] \qquad (A.19)$$

And the I_D in the saturation region, where $V_D \geqq V_G - V_T$, is given by

$$I_D(sat.) = \frac{W_g C_G \mu}{2\, L_g}(V_G - V_T)^2 \qquad (A.20)$$

Note that Eq. (A.19) and Eq. (A.20) are very similar to the equations for Si MOSFET, since they are under the same assumptions and approximations. The differences between QW-MOSFET and Si MOSFET in the I_D equation are the V_T and C_G terms. For Si surface channel MOSFET, the C_G term includes C_{OX}, C_{it}, and C_d only.

For InAs composite channel QW-MOSFET, the C_G incorporates C_{OX}, C_{it}, C_{ins}, $C_{centroid}$, and C_Q. Eq. (A.19) also includes the description of the effect of the quantity of charged acceptor-like interface states on the drain current.

By differentiating Eq. (A.19) with respect to V_G, we can obtain the g_m of QW-MOSFET under constant mobility approximation.

$$g_m(lin.) = \frac{dI_D}{dV_G} = \frac{W_g C_G \mu V_D}{L_g}(1 - \frac{dV_T}{dV_G}) \qquad (A.21)$$

In the expression of g_m in Eq. (A.21), we not only neglect the fact that the C_G is a function of V_G, but also emphasis the fact that the V_T is a function of V_G, since the charged acceptor-like interface states modulates V_T and hence affect I_D and g_m. Based on Eq. (A.21), we can see that the g_m of the reverse-sweep is higher than forward-sweep, since the dV_T/dV_G is positive in forward-sweep, while dV_T/dV_G is negative in reverse-sweep. If we neglect the term dV_T/dV_G, the g_m is reduced to the well-known form.

$$g_m(lin.) = \frac{W_g C_G \mu V_D}{L_g} \qquad (A.22)$$

However, for the analysis in this work, we prefer Eq. (A.21) instead of Eq. (A.22) since it captures more details about how the charged interface state modulates V_T and hence g_m.

The SS describes how sharply the I_D rises with V_G, and is defined as the V_G change needed to induce a I_D change of one order of magnitude. For Si MOSFET, the I_D in subthreshold region is given by [1]:

$$I_D(subth.) = \mu \frac{W_g}{L_g}(\frac{kT}{q})^2 (C_d + C_{it})(1 - e^{\frac{-qV_D}{kT}}) e^{\frac{q(V_G - V_T)}{C_r kT}} \qquad (A.23)$$

$$where\, C_r = 1 + \frac{C_d + C_{it}}{C_{OX}} \qquad (A.24)$$

And the SS is given by:

$$SS = \left[\frac{d(\log I_D)}{dV_G}\right]^{-1} = (\ln 10)\frac{kT}{q}\left[1 + \frac{C_d + C_{it}}{C_{OX}}\right] = (\ln 10) V_{th}\, C_r \qquad (A.25)$$

where V_{th} is the thermal voltage given by kT/q. Eq. (A.24) can be understood by the equivalent circuit of the MOSFET in terms of the capacitors (Fig. A.3 (a)). The expression of C_r is the capacitor divider ratio. Eq. (A.25) also suggests a minimum SS of the MOSFET at room temperature (300K): 60 mV/decade which is also called the thermionic limit. The subthreshold current and SS for the InAs QW-MOSFET can be expressed as follows by considering the capacitor divider ratio of InAs QW-MOSFET (Fig. A.3 (b)).

$$I_D(subth.) = \mu \frac{W_g}{L_g} \left(\frac{kT}{q}\right)^2 (C_{it} + C_K)\left(1 - e^{\frac{-qV_D}{kT}}\right) e^{\frac{q(V_G - V_T)}{C_\lambda kT}} \qquad (A.26)$$

$$SS = (\ln 10)\frac{kT}{q}\left[1 + \frac{C_{it} + C_K}{C_{OX}}\right] = (\ln 10)\, V_{th}\left[1 + \frac{C_{it} + C_K}{C_{OX}}\right] = (\ln 10)\, V_{th} C_\lambda \qquad (A.27)$$

$$where \;\; C_K = \left(\frac{1}{C_{ins}} + \frac{1}{C_{centroid}} + \frac{1}{C_Q}\right)^{-1} \qquad (A.28)$$

$$C_\lambda = 1 + \frac{C_{it} + C_K}{C_{OX}} \qquad (A.29)$$

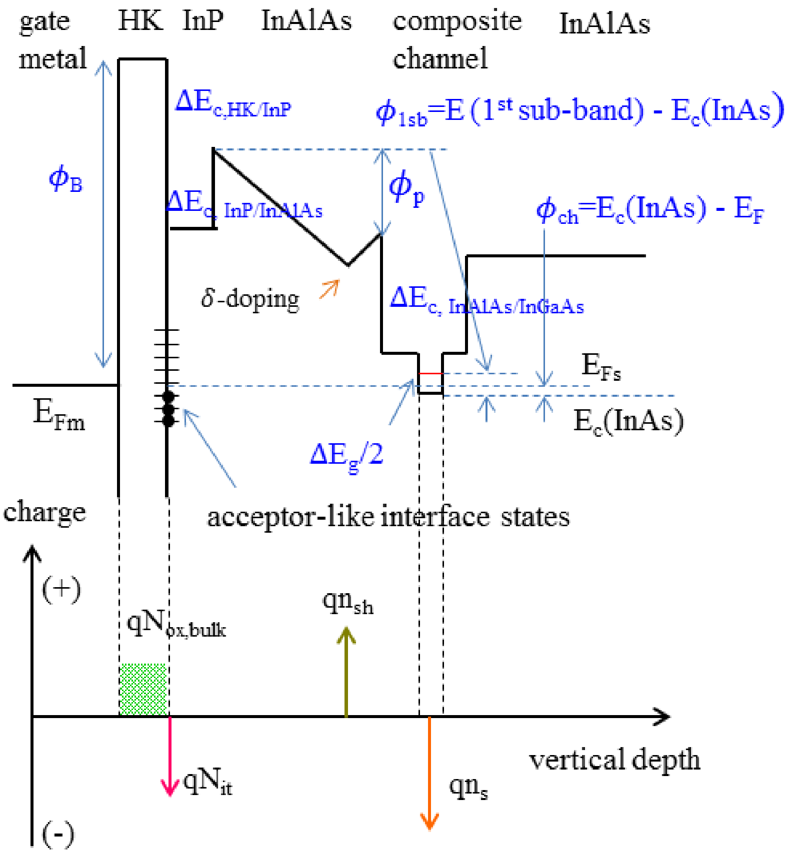

Fig. A.1 Schematic band diagram and the charge density vs. position of normal type InAs composite channel QW-MOSFET at flat band condition.

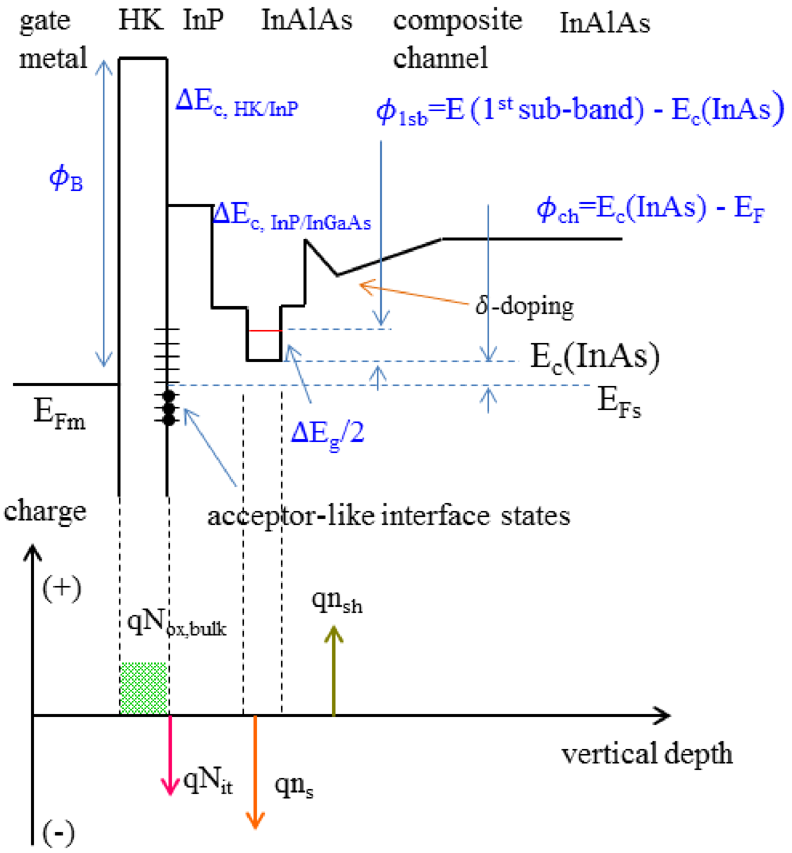

Fig. A.2 Schematic band diagram and the charge density vs. position of inverted type InAs composite channel QW-MOSFET at flat band condition.

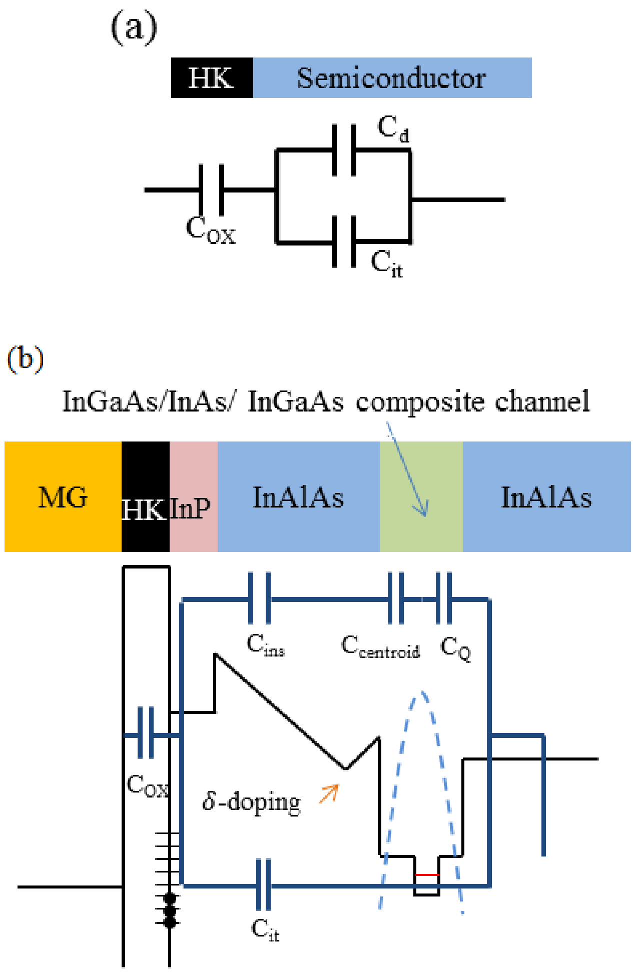

Fig. A.3 Equivalent circuit of the gate capacitance of (a) surface channel MOSFET (b) InAs composite channel QW-MOSFET.

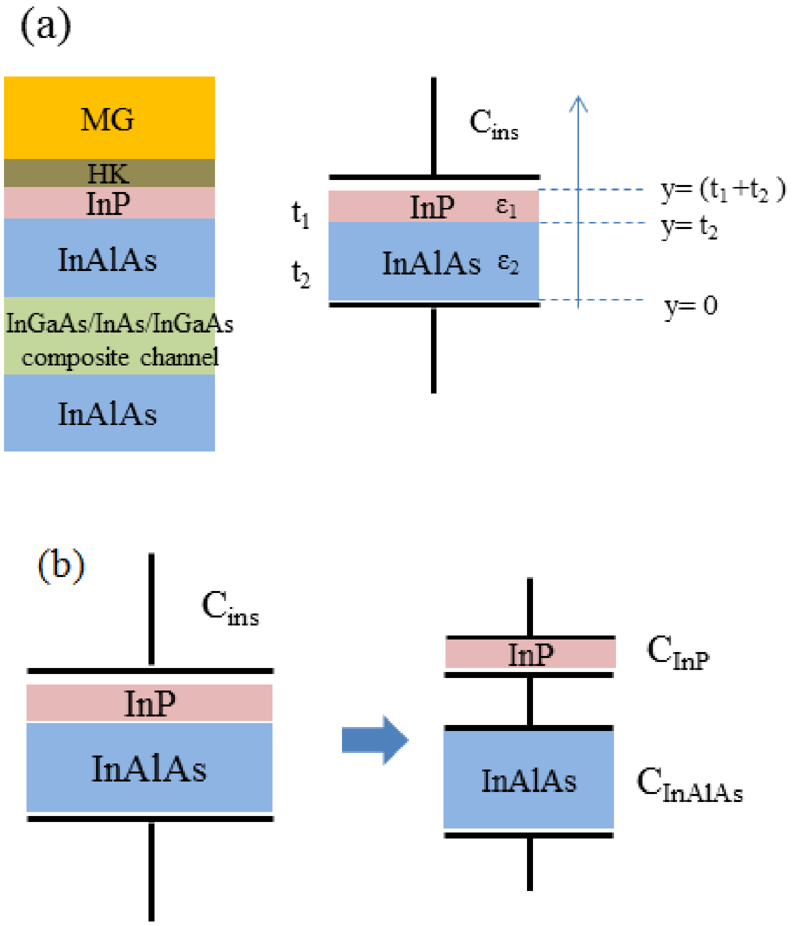

Fig. A.4 The insulator capacitance.

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