Design of Sub-90 nm Low-Power and Variation Tolerant PD/SOI SRAM Cell Based on Dynamic Stability Metrics

Rajiv V. Joshi, *Fellow, IEEE*, Saibal Mukhopadhyay, *Member, IEEE*, Donald W. Plass, Yuen H. Chan, Ching-Te Chuang, *Fellow, IEEE*, and Yue Tan

***Abstract*—In this paper we have studied the impacts of floating body effect, device leakage, and gate oxide tunneling leakage on the read and write-ability of a PD/SOI CMOS SRAM cell under Vt, L and W variations in sub-100 nm technology for the first time. The floating body effect is shown to degrade the read stability while improving the write-ability. On the other hand, the gate-to-body tunneling current improves the read stability while degrading the write-ability. It is also shown that the use of high-Vt and thick oxide cell transistors can improve leakage, read and write-ability without causing significant performance degradation. The test-chip is fabricated in sub-90 nm SOI technology to show the effectiveness of high-Vt and thick-oxide devices in improving stability of SRAM cells.**

***Index Terms*—Dynamic stability, high-Vt, process variation, SRAM, thick oxide, write-ability.**

I. Introduction

With technology scaling, inter-die and intra-die variations in process parameters (channel length (L), width (W), threshold voltage (Vt) etc) have become serious problems in circuit design [1], [2]. The device-to-device (intra-die) variations in L, W or Vt between the neighboring transistors in an SRAM cell can significantly degrade the stability of the cell. The static stability of a cell is measured by the static noise margin (SNM) [3]. In [3] authors have analyzed the impact of device-to-device Vt fluctuations on the SNM of a bulk CMOS SRAM cell. However, in a PD/SOI SRAM cell, due to the floating body effect, the strength of the different transistors in the cell varies during read and write operations [4]. Even if the static stability of the cell is high, device-to-device fluctuations may result in instability during the read and write operations. In addition, the initial states of cell transistors as well as gate-to-body tunneling current are very critical in cell stability. Hence, a thorough understanding of the dynamic stability under parameter variations is crucial to maintain/exploit the performance advantage of PD/SOI technology. We have also analyzed the impact of using high Vt and thick oxide transistors on the performance and stability of the cell. It has been observed that, use of high Vt and thick oxide cell transistors can significantly reduce the cell leakage, improve the cell stability without causing significant performance degradation. Notice that in this study, parameters are treated as independent and variations are applied in the worst case directions, thus representing the worst case scenario. Test-chip is fabricated in sub-90 nm PD/SOI technology and measured to demonstrate the effectiveness of the high-Vt and thick-oxide devices. The measurement results verifies the simulation based predictions and demonstrate that, use of higher-Vt and thicker-oxide devices can significantly improve the cell stability and hence, SRAM yield.

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II. Dynamic Cell Stability

In this section, we present the concept and the methods for analyzing dynamic stability of SRAM cell.

A. Dynamic Stability

The strengths of the PMOS and NMOS transistors in an SRAM cell (Fig. 1) control the read stability and write-ability (collectively known as cell stability) of the SRAM cell. The strength is defined by the threshold voltage (Vt), channel length (L), and channel width (W) of transistors. The conventional static stability analysis focuses on the beta ratio (which is determined by the L and W ratios) and Vts of pass-gates and cross-coupled PFET/NFET. The Vt used in such analysis is normally the Vt measured at a particular terminal (i.e., Vds and Vgs) voltages (e.g., at Vds-V_{DD}). However, due to short channel effects, such as Drain Induced Barrier Lowering (DIBL), the Vt of a device depends on its terminal voltages and hence, changes dynamically for different voltages at cell terminals (e.g., wordline, bitlines, cell supply) as well as cell nodes (i.e., V_{DD} or 0 at a given node) [9]. Further, for PD/SOI devices, the operating conditions (i.e., V_{ds} and V_{gs} values) of a device also modify the threshold voltage due to floating body effect. Moreover, the read/write operation of a cell also depends on the capacitances at the cell nodes, which can only be captured through transient analysis. Therefore, for a true analysis of the cell stability, static analysis considering parameters such as L, W, and Vt, as well as transient analysis considering dynamic changes in the bias conditions and corresponding effects

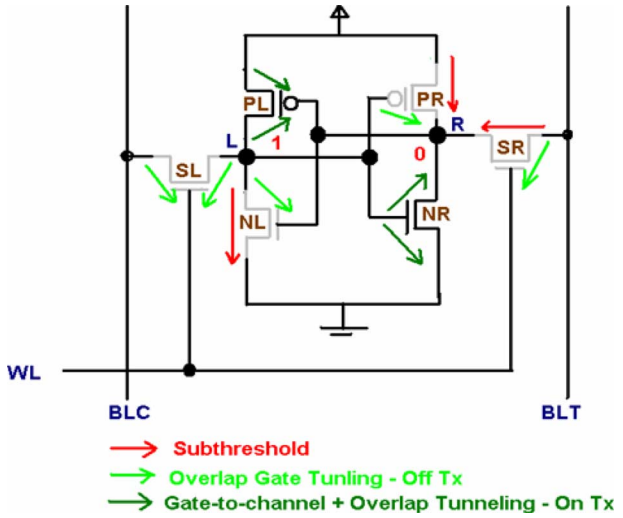

Fig. 1. A SRAM cell storing "1".

in device parameters need to be considered. The 'dynamic stability analysis' evaluates cell stability considering both the static and bias-dependent transient effects, and hence provides a more accurate measure of stability of SRAM cell in operation. In dynamic analysis instead of performing a DC analysis of SRAM cell, a transient analysis is performed considering dynamic voltage waveforms at wordline and bitlines. In a true sense dynamic stability can be defined as the critical noise level required in the cell to prevent the upset or corruption under dynamically stressing the transistors. In this work, for read stability or write-ability analysis considering random Vt mismatch, we consider the 'noise' as the worst case Vth variation (the read and write operations have different worst case conditions as explained in following sections). To estimate dynamic stability for read or write operations, we first apply certain worst-case Vth mismatch. Next, we consider different $\mathrm{V_{DD}}$ values defining cell, bitline, and wordline voltage levels, and perform transient analysis for read or write operations. *In the* transient analysis wordline slew rate is varied from low to high to explore the worst case condition for the cell. The SRAM cell as well as the peripherals is considered in the analysis to obtain a comprehensive picture. The effect of array organization, such as the impact of other cells on the same column and/or same row, is also considered. The considerations of array organization and peripherals provide a more accurate measure of stability compared to static/DC analysis (such as Static Noise Margin for read stability) which considers '*a cell in isolation*'. The transient simulations (with standard waveforms for read/write operations) provide an indication of correct (stable) or faulty (unstable) operation of the cell at a given $\mathrm{V_{DD}}$ level. The range of $\mathrm{V_{DD}}$ which provides correct (stable) operations is used as an indicator of the dynamic read stability or write-ability. Note, that $\mathrm{V_{DD}}$ level is just one option, one can also perform dynamic stability analysis by modifying the operating frequency, wordline pulse width, etc.

In summary, the dynamic stability of the cell is a measure of the robustness of the cell against parameter variations during the read (read stability) and write (write stability, or "write-ability") operation. The dynamic stability measures the ac characteristics of the cell and provides more detail information regarding the cell functionality compared to the static noise margin. Since dynamic stability captures the cell behavior in the ac mode (e.g., frequency response of the cell, the effect of node capacitances, floating body effect in SOI as discussed later) it is a better indicator of the actual product behavior.

In the following sections, we discuss the dynamic stability analysis for read and write operation in an SRAM cell. In this analysis, sub-90nm PD/SOI SRAM cell is used. Further, the analysis consider a PD/SOI SRAM cell which stores '1' (i.e., $V_L = $ '1′ and $V_R = $ '0′) (Fig. 1). The analysis is same for a cell storing '0' (i.e., $V_L = $ '0′ and $V_R = $ '1′), which is not repeated for brevity. To explain the effects of Vt variation on read stability and write-ability we have used simplified equations considering square-law transistor model. However, the results are obtained using circuit simulations for the sub-90nm PD/SOI cell.

B. Read Stability

During the read operation, the access transistor S_R and the NMOS transistor N_R form a resistor-voltage-divider between node *BLT* and node R. This increases V_R to an intermediate voltage (V_{READ}) which subsequently increases the subthreshold leakage through N_L , thereby discharging V_L from '1'. A reduction in V_L further reduces the strength of $\mathrm{N_R}$ (since $V_{gs}(N_R) = V_L < V_{DD}$) and hence cause V_R to rise more [5], [7]. If V_{READ} is higher than the trip point of the inverter P_L-N_L, the state of the cell gets flipped (i.e., $V_L = $ '0′ and $V_R = $ '1′ after reading). This is known as 'destructive read' or 'unstable read'. A simple static condition for read stability can be defined as [7], [8]:

$$V_{TRIP}(P_L - N_L) > V_{READ}. \tag{1}$$

The intermediate voltage can be obtained by solving V_{READ}:

$$\begin{aligned} &I_{ds(SR)}(V_{DD} - V_{READ}, V_{DD} - V_{READ}) \\ &\quad + I_{ds(PR)}(V_L - V_{DD}, V_{READ} - V_{DD}) \\ &\quad = I_{ds(NR)}(V_L \approx V_{DD}, V_{READ}) \end{aligned} \tag{2}$$

where, $\mathrm{I_{ds}}$ (gate-source, drain-source) represents the drain-to-source current. For the sake of simplicity, in the above formulation we have neglected the gate leakage contributions to node R.

1) Worst-Case Condition for Read-Stability: From (1) we can observe that, if the relative strength of P_R and S_R increases while that of N_R reduces, V_{READ} increases thereby increasing the possibilities of the read failure. Hence, the worst-case for read stability occurs if due to process variation, S_R and P_R becomes strong (Vt & L reduces, W increases) whereas N_R becomes weak (Vt & L increases, W reduces).

2) Impact of Floating Body Effect in PD/SOI: In PD/SOI various effects such as gate-to-body coupling (which causes kink effect), drain-to-body, body-to-source coupling can affect the body voltages. In PD/SOI SRAM before the start of the read operation, the $\mathrm{V_{ds}}$ of $\mathrm{S_R}$ is $\mathrm{V_{DD}}$ which increases the body-voltage of $\mathrm{S_R}$. The body-voltage of $\mathrm{N_R}$ is much lower as $\mathrm{V_{ds}}$ $[V_{BODY}(N_R) = 0]$. This is evident from the waveform shown in Fig. 2 which shows the body voltage of different transistors before and during read operations. Further, since node L is at '1', body voltage of both $\mathrm{N_R}$ and $\mathrm{P_R}$ are also higher. Since a higher

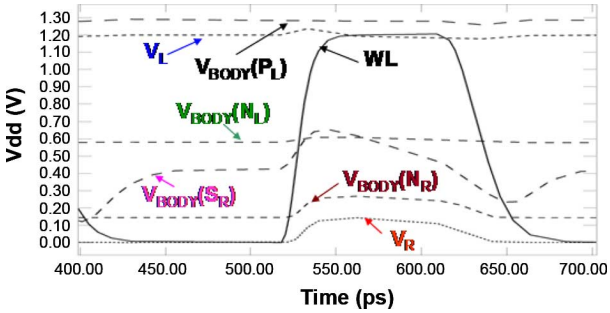

Fig. 2. Waveform for read operation showing body voltage of different transistors.

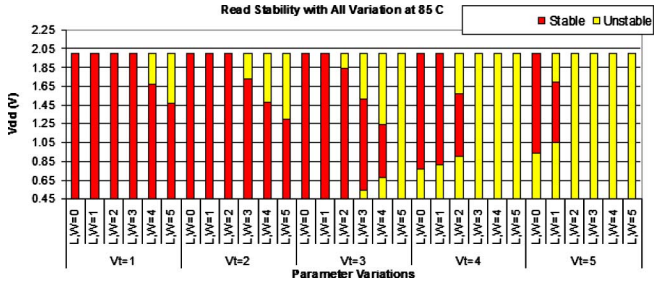

Fig. 3. Variation of read-stability at $\mathrm{T} = 85°\mathrm{C}$ for different L, W and Vt variation (normalized unit for variation) .

body voltage for NMOS indicates a stronger device (i.e., lower Vth) while a higher body voltage for PMOS indicates a weaker device (i.e., higher $\mathrm{V_{th}}$), the floating body effect results in (1) stronger $\mathrm{S_R}$ and weaker $\mathrm{N_R}$ (higher $\mathrm{V_{READ}}$); and (2) stronger $\mathrm{N_L}$ and weaker $\mathrm{P_L}$ [lower $\mathrm{V_{TRIP}}$ ($\mathrm{P_L}$-$\mathrm{N_L}$)]. Therefore, floating body-effect tends to marginally degrade the read stability.

3) Impact of Leakage on Read Stability: The high leakage in the nano-scaled transistors plays an important role in determining the read-stability. A larger subthreshold leakage of the transistor N_L reduces the voltage V_L during read operation and thereby affects read-stability. A larger subthreshold leakage of $\mathrm{P_R}$ also negatively affects read stability by increasing $\mathrm{V_{READ}}$. Also in the presence of large number of cells on the same bit column having opposite state as that of the selected cell can increase leakage on bitlines which slows down the bitline discharge. Due to back to back body diodes in PD SOI (reverse diode from drain to body and forward diode from body to source) the other leakage component (parasitic bipolar current) exists from drain-to-body-to-source. This has a similar effect on the cell stability as that of sub-threshold leakages. A slower bit-line discharge indicates a higher $\mathrm{V_{ds}}$ stress for $\mathrm{S_R}$ thereby affecting read stability. Similarly, as shown in Fig. 1, the gate-to-channel and the overlap tunneling leakage from the transistors N_R, N_L, P_R and P_L entering into the node R, cause V_R to rise more during read operation and hence degrade the read stability. While the gate-to-body tunneling leakage is much smaller than the other leakage components, it has interesting implications for PD/SOI SRAM cell. For PD/SOI devices, however, the gate-to-body tunneling current charges/discharges the floating body, thus changing the body voltage and Vt. When the gate of a transistor at "VDD" and source and drain are at "0", initially the body sits at "0". The gate-to-body tunneling current charges the transistor body. Similarly, when gate is at '0' the gate-to-body tunneling current tends to discharge the body-voltage. Therefore, gate-to-body tunneling current reduces the body-voltage of $\mathrm{S_R}$ and $\mathrm{N_L}$ (gate at $\mathrm{V_{DD}}$) thereby weakening them. It also reduces body-voltage of $\mathrm{P_L}$ which makes it stronger. On the other hand, gate-to-body tunneling increases the body-voltage of $\mathrm{N_R}$ (gate at $\mathrm{V_{DD}}$) thereby making it stronger [6]. This helps to reduce $\mathrm{V_{READ}}$ (stronger $\mathrm{N_R}$ and weaker $\mathrm{S_R}$) and increase $\mathrm{V_{TRIP}}$ (stronger $\mathrm{P_L}$ and weaker $\mathrm{N_L}$), thereby improving read stability. Hence, the presence of gate-to-body tunneling current helps to improve the read stability of PD/SOI SRAM cell.

4) Circuit Simulation Results for Read Stability: To measure the read stability, we have applied the Vt, L and W variations in the worst-case direction and varied the V_{DD} from a low to a high value. We have measured the V_{DD} region in which the cell is stable for each unit of variation in Vt, L and W. A larger stable region indicates a better robustness against read failure due to process variation. Fig. 3 shows the read stability of the cell at $\mathrm{T} = 85°\mathrm{C}$ with application of different parameter variation. Note, that the figure shows two different unstable regions. This is due to the counter-acting effects of $\mathrm{V_{DD}}$ on the cell characteristics. As mentioned earlier, in this simulation, we consider same $\mathrm{V_{DD}}$ value for cell supply, wordline voltage, and bitline voltage. A lower wordline $\mathrm{V_{DD}}$ implies a lower gate voltage for the pass-gates and a lower bitline $\mathrm{V_{DD}}$ implies a lower Vds stress across the pass-gate. Both of these reduces the pass-gate strength and helps to reduce $\mathrm{V_{READ}}$. However, a lower cell $\mathrm{V_{DD}}$ reduces the trip-point and the strength of the pull-down device (NR) in the read path. Both of these negatively impact the read stability. At very low voltage, the negative effect of lower cell $\mathrm{V_{DD}}$ results in unstable read operations. On the other hand, at very high $\mathrm{V_{DD}}$, the increased strength of the access device results in unstable read. Note, that during read operation the pass-gate $\mathrm{S_R}$ is in saturation while $\mathrm{N_R}$ is in linear. Since saturation current is a stronger function of $\mathrm{V_{GS}}$ (e.g., quadratic) compared to linear current, a higher wordline $\mathrm{V_{DD}}$ increases $\mathrm{V_{READ}}$ resulting in unstable read operation. This explains the origin of two unstable regions related to read operations. Further, a higher $\mathrm{V_{DD}}$ also increases the Vth mismatch between $\mathrm{S_R}$ and $\mathrm{N_R}$ due to DIBL effect [as Vds for $\mathrm{S_R}$ $(= \mathrm{V_{DD}} - \mathrm{V_{READ}}) >$ Vds for $\mathrm{N_R(VREAD)}$ $\Rightarrow$ due to DIBL $\mathrm{Vt(S_R)} < \mathrm{Vt(N_R)}$] which negatively impacts read stability [9]. Moreover, as explained in the following section, for PD/SOI the floating body effect results in a lower $\mathrm{V_{th}}$ for $\mathrm{S_R}$ from $\mathrm{N_R}$ at the start of read operation. At a higher $\mathrm{V_{DD}}$ the body-voltage difference between $\mathrm{S_R}$ and $\mathrm{N_R}$ is higher which also degrades read stability. It can be observed that, the impact of Vt variation is very significant. The impact of the L & W variation becomes significant when coupled with Vt variation. The stronger effect of Vth variation originates from the stronger-than-linear dependence of saturation current on Vt which results in a stronger sensitivity of $\mathrm{V_{READ}}$ and $\mathrm{V_{TRIP}}$ to Vt compared to L and W (both linear and saturation current depends linearly on L and W). Considering a given Vt variation and different amount of L and W variation it was observed that, read stability marginally degrades at a higher

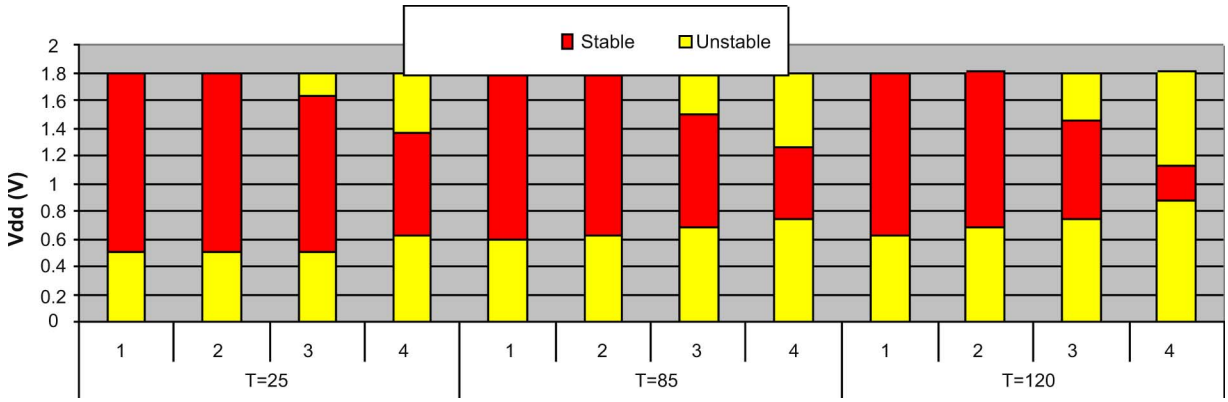

Fig. 4. Effect of temperature on read stability: L and W variation along with Vt variation of 3 unit.

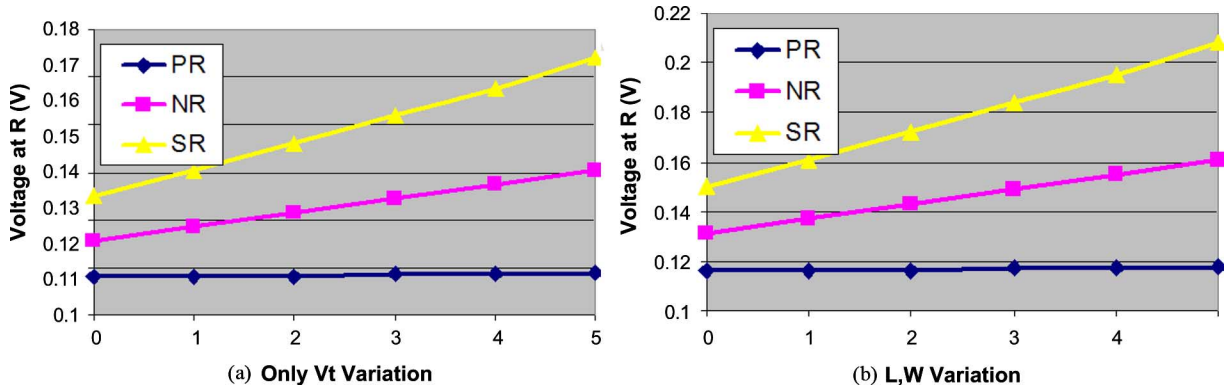

Fig. 5. Impact of variation of different transistor on the read stability. (a) Vt variation (b) L, W variation (with 3 units of Vt variation). A higher voltage at node R indicates a worse read-stability (normalized unit for variation).

temperature (Fig. 4). This is mainly because; at a higher temperature mobility degrades. Further, linear current depends more strongly on mobility compared to saturation current (velocity saturation effect in short-channel devices makes saturation current less sensitive to mobility). Hence, at a higher temperature due to lower mobility, linear current reduces more than saturation current resulting in a higher $\mathrm{V_{READ}}$ and degraded read stability. The temperature sensitivity increases if L & W variation increases as sensitivity of β-ratio [where, $\beta = \mu_{\mathrm{eff}}\mathrm{C_{ox}(W/L)}$] to L, W mismatch depends on mobility which in turn depends on mobility. At a higher temperature, the leakage current contributed by $\mathrm{P_R}$ [see (2)] increases. This leakage contribution also increases when L mismatch is considered (as worst-case L mismatch means lower L for $\mathrm{P_R}$). The higher temperature coupled with Vt and L mismatch can significantly increase the leakage current contribution resulting in a higher $\mathrm{V_{READ}}$ and lower read stability. Fig. 5 shows V_{READ} at different Vt, L and W variation, by applying the variations to transistors S_R, N_R and P_R one at a time. It can be observed that, application of variation in S_R cause maximum rise in V_{READ}. This indicates that S_R is most critical for read stability. This is because of the stronger-than-linear dependence of saturation current of $\mathrm{S_R}$ on device $\mathrm{V_{th}}$. The impact of P_R is minimum since it is in the subthreshold region. From Fig. 4, it can be concluded that to optimize the cell for best read stability we need a weak access transistor while a strong pull-down NMOS. The effect of gate-to-body tunneling current on the read stability is shown in Fig. 6. It can be clearly observed that, the presence of gate-to-body tunneling current improves the read stability of PD/SOI SRAM cell.

C. Write-Ability

While writing a '0' to the cell shown in Fig. 1 (i.e., changing the state of the cell from (V_L = '1' and V_R = '0') to (V_L = '0' and V_R = '1')), the low going bit-line *BLC* forms a voltage divider between the PMOS P_L and the access transistor S_L. If due to this voltage division the voltage at node $\mathrm{L}(V_{WRITE})$ is reduced below the trip point of the inverter $\mathrm{P_R}$-$\mathrm{N_R}$ within the time-interval when WL is high $(\mathrm{T_{WL}})$ then a successful write occurs [4]–[8]. Hence, the stability conditions for write operations can be formulated as [5], [7], [8]:

$$T_{WRITE} < T_{WL} \tag{3}$$

where T_{WRITE} is the time required to reduce the voltage $\mathrm{V_L}$ from $\mathrm{V_{DD}}$ to the trip-point of $\mathrm{P_R}$-$\mathrm{N_R}$. $\mathrm{T_{WRITE}}$ can be obtained by:

$$T_{WRITE} = \int_{V_{TRIP}(P_R-N_R)}^{V_{DD}} \frac{C_L}{I_{ds(SL)} + I_{ds(NL)} - I_{ds(PL)}} dV_L \tag{4}$$

Note, a stronger $\mathrm{P_L}$ and weaker $\mathrm{S_L}$ increases write time and degrades write-ability.

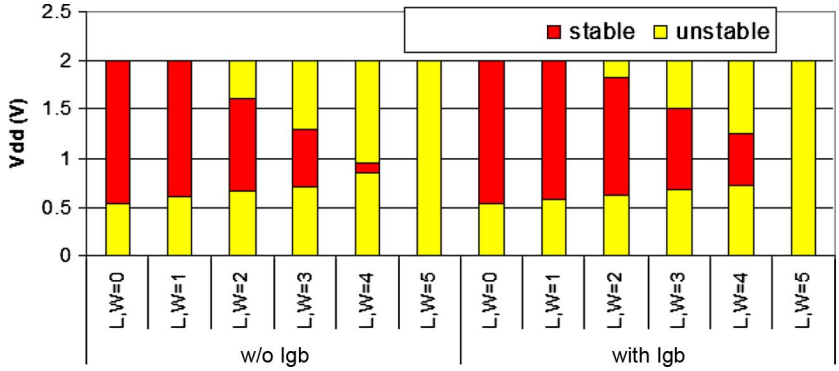

Fig. 6. Impact of gate-to-body tunneling current on read-stability (normalized unit for variation).

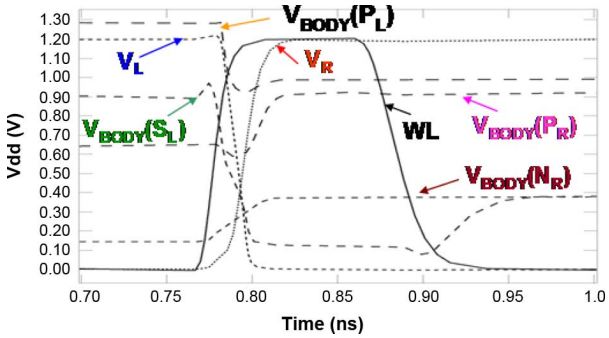

Fig. 7. Waveform showing body voltages during write operation.

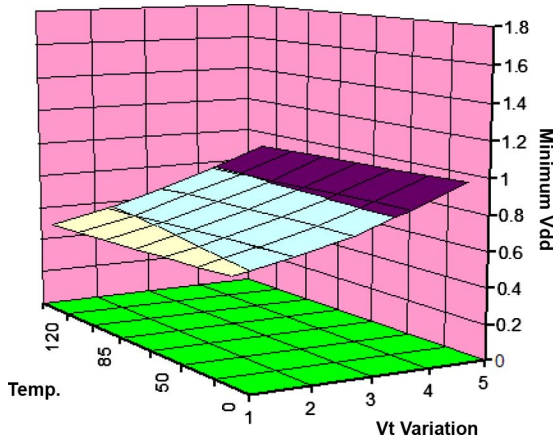

Fig. 8. Write-ability at with Vt and Temperature variation.

1) Worst-Case Condition for Write-Ability: From (3)–(4) we can observe that, if the relative strength of P_L increases while that of S_L and N_L reduces the net discharging current for node 'L'[$= \mathrm{I_{ds(SL)}} + \mathrm{I_{ds(NL)}} - \mathrm{I_{ds(PL)}}$] becomes lower thereby increasing T_{WRITE}. Further, a weaker $\mathrm{S_R}$ and $\mathrm{P_R}$ and a stronger $\mathrm{N_R}$ reduce the trip-point of $\mathrm{P_R}$-$\mathrm{N_R}$ which also increases $\mathrm{T_{WRITE}}$. Hence, the worst-case condition for write-ability occurs if due to process variation, (a) P_L becomes strong (Vt and L reduces, W increases) whereas S_L and N_L become weak (Vt & L increases, W reduces) resulting in lower discharging current; and (b) $\mathrm{S_R}$ and $\mathrm{P_R}$ become weak (higher Vt & L, lower W) and $\mathrm{N_R}$ becomes strong (lower Vt and L, higher W) resulting in lower trip-point of $\mathrm{P_R}$-NR.

2) Impact of Floating Body Effect in PD/SOI: In PD/SOI SRAM before the start of the write operation, body voltage of $S_L[V_{BODY}(S_L)]$ and $\mathrm{P_L}[V_{BODY}(P_L)]$ are high (since drain and source at V_{DD}). This is shown Fig. 7 which shows the body-voltages of different transistors before and during a typical write operation. This results in a stronger S_L and weaker P_L and thus improves the write-ability. Further, since node R is at '0', $\mathrm{V_{BODY}(N_R)}$ is low ($\mathrm{V_{drain}} = \mathrm{V_{source}} = 0$) while $\mathrm{V_{BODY}(S_R)}$ is high ($\mathrm{V_{ds}} \sim \mathrm{V_{DD}}$), resulting in a weaker $\mathrm{N_R}$ and stronger $\mathrm{S_R}$. The body voltage of $\mathrm{P_R}$ is also less (as $\mathrm{V_{drain}} = 0$) resulting in a stronger $\mathrm{P_R}$. Stronger $\mathrm{S_R}$ and $\mathrm{P_R}$ and weaker $\mathrm{N_R}$ improves write-ability. Therefore, floating body effect tends to improve the write-ability.

3) Impact of Leakage on Write-Ability: A large subthreshold leakage of the transistor N_L helps to discharge V_L. The gate-to-channel and overlap-tunneling leakage of the transistors N_R, N_L, P_R and P_L also helps to discharge V_L and hence improves write-ability. On the other hand, gate-to-body tunneling reduces the body voltages of N_L, S_L, $\mathrm{S_R}$, $\mathrm{P_L}$ (gate at '0'). This weakens N_L, S_L, and $\mathrm{S_R}$ while strengthens $\mathrm{P_L}$ thereby degrading write-ability [5]. For the worst case write operation all the unselected cells have same polarity as that of the selected cell. When the node holding "1" needs to be written to "0", parasitic bipolar currents induced in pass gates can reduce the currents to discharge the bitline degrading the "write-ability". Similarly, gate-to-body tunneling increases body voltages of $\mathrm{N_R}$ (makes it stronger) and $\mathrm{P_R}$ (makes it weaker) as both of them have gate at $\mathrm{V_{DD}}$. This lowers the $\mathrm{V_{TRIP}}$ of ($\mathrm{P_R}$-$\mathrm{N_R}$). Therefore, gate-to-body tunneling current degrades the write-ability of PD/SOI SRAM cell. It is interesting to note that, for PD/SOI devices floating body effect degrades read stability while improves write-ability. On the other hand, gate-to-body tunneling improves read stability while degrades write-ability.

4) Circuit Simulation Results for Write-Ability: To measure the write-ability, we have applied the Vt, L and W variations in the worst-case direction and varied the V_{DD} from a low to a high value. As V_{DD} increases, the strength of S_L increases, thereby increasing the write-ability. We have measured the minimum $V_{DD}(V_{DD\,\mathrm{min}})$ at which the cell remains writable. A lower value of $V_{DD\,\mathrm{min}}$ indicates a better write-ability. Fig. 8 shows the variation of the $V_{DD\,\mathrm{min}}$ with application of only Vt variation at different temperature. It can be observed that,

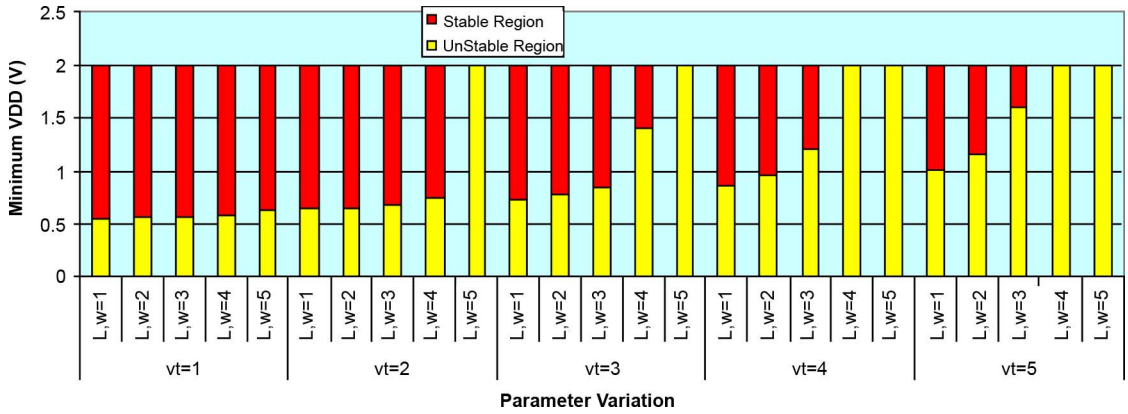

Fig. 9. Write-ability with all variation at $\mathrm{T} = 85°\mathrm{C}$ (normalized unit for variation).

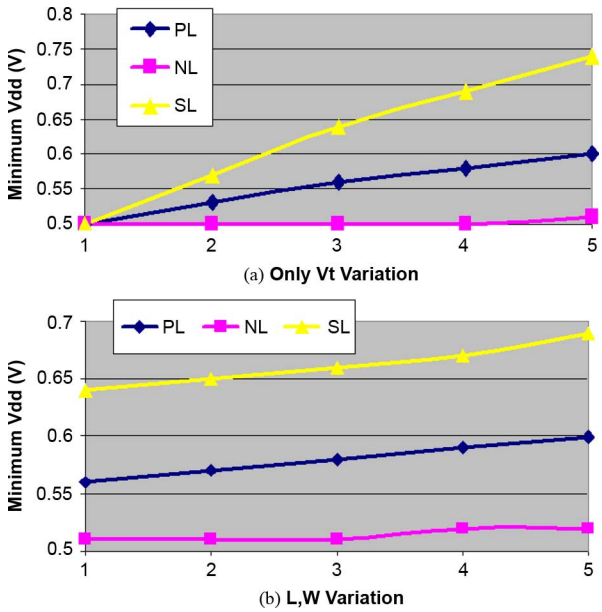

Fig. 10. Impact of variation of different transistor on the write-ability. (a) Vt variation (b) L, W variation. A lower VDDmin indicates better write-stability (normalized unit for variation).

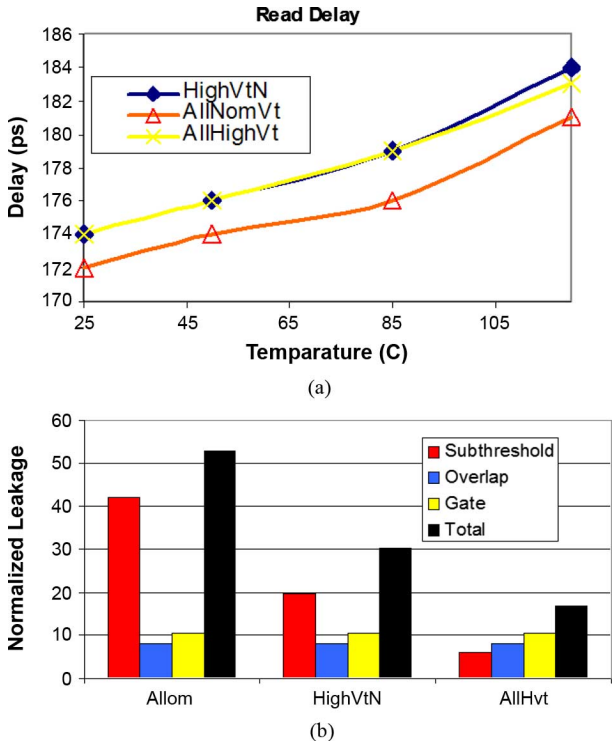

Fig. 11. Impact of using high Vt transistor on the performance and leakage of an SRAM cell: (a) Read delay vs. temperature, (b) Leakage components in stand-bv mode. Notice that, significant leakage reduction is possible with small performance degradation by using high Vt transistors.

$V_{DD\,\min} > V_{DD}\ (= 0.9\,\mathrm{V})$ if Vt variation is high. It can also be observed that, the sensitivity with temperature is not very high. The sensitivity of the $V_{DD\,\min}$ with respect to L and W variation alone is very low (figure not shown). However, if L and W variation is coupled with Vt variation, it has a strong impact (Fig. 9). The effect of temperature variation was observed to be small. Fig. 9 shows $V_{DD\,\min}$ with application of Vt (Fig. 10(a)) and $\langle$L and W$\rangle$ (Fig. 10(b)) variations to transistors S_L, P_L and N_L alone. It can be observed that, the access transistor S_L is most critical whereas N_L has little impact (since it is in subthreshold region). Hence, a weaker PMOS pull-up and a stronger NMOS access transistor are required for better write-ability.

III. Stability With High-Vt Transistors

In order to reduce the subthrehold leakage in the cell, scaled SRAM cells are often designed with high Vt transistors. It has been observed that the performance degradation associated with the use of high Vt transistors are not very significant. Fig. 11 shows the read delay (Fig. 11(a)) and the leakage (Fig. 11(b)) of the SRAM cell designed with all nominal Vt (*AllNomVT*), high Vt NMOS (*HighVtN*) and all high Vt transistors (*AllHVT*). It can be observed that, leakage improves significantly from *AllNomVt* to *AllHVT* $(> 4\mathrm{X})$ and the associated performance degradation is quite small $(< 2\%)$. The subthreshold leakage shows maximum reduction with higher-Vt transistors. The leakage reduction obtained with high-Vt increases at a higher temperature as the current contribution from the subthreshold leakage is much higher. In the following sections we will describe the impact of using high-Vt transistors on the stability of the cell.

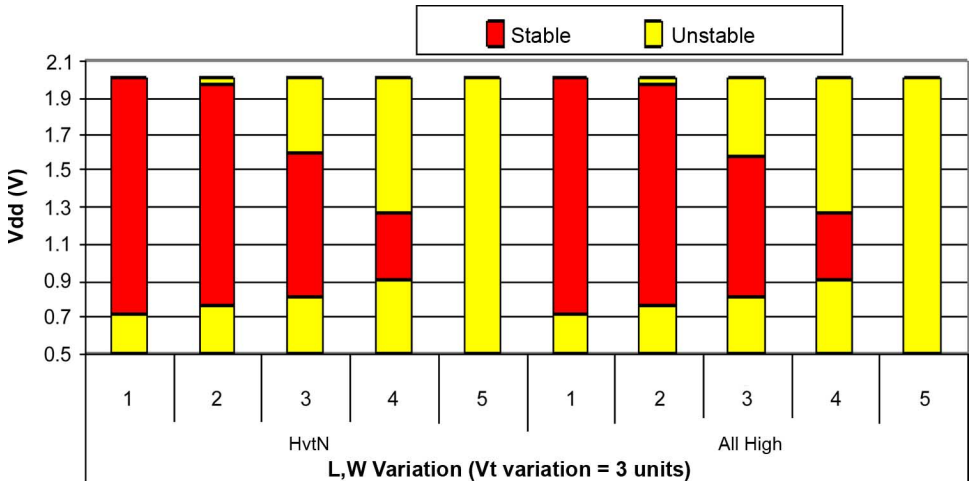

Fig. 12. Impact of using High Vt transistors on read-stability. X axis represents normalized units of L, W variations along with 3 units of Vt variations.

A. Read Stability With High Vt

In order to analyze the impact of high Vt transistors, let us assume a simplified square-law transistor characteristics. Under this assumption, the trip point of the inverter P_L-N_L can be given by

$$V_{TRIP} = \frac{V_{DD} - Vt_{p0} - \Delta Vtp + (Vt_{n0} + \Delta Vtn)\sqrt{\left(\frac{\beta_{NL}}{\beta_{PL}}\right)}}{1 + \sqrt{\left(\frac{\beta_{NL}}{\beta_{PL}}\right)}}$$

or

$$V_{TRIP} = V_{TRIP0} + \frac{\Delta Vtn\sqrt{\left(\frac{\beta_{NL}}{\beta_{PL}}\right)} - \Delta Vtp}{1 + \sqrt{\left(\frac{\beta_{NL}}{\beta_{PL}}\right)}} \quad (5)$$

where β for each transistor is given by

$$\beta = \left(\frac{\mu_{eff}\varepsilon}{T_{ox}}\right)\left(\frac{W}{L}\right) \quad (6)$$

Vt_{p0} and Vt_{n0} represents the nominal PMOS and NMOS Vt, V_{TRIP0} represents the trip point with nominal Vt and ΔVtp and ΔVtn represents the difference between high and nominal Vt. From (6) it can be observed that, use of higher Vt for NMOS increases the trip point whereas increasing the PMOS Vt lowers the trip point. Since in SRAM $\beta_{NL} > \beta_{PL}$ (because $(W/L)_{PMOS} < (W/L)_{NMOS}$ and $\mu_P < \mu_N$), increasing Vt of NMOS has a stronger impact (assuming $\Delta Vtp \approx \Delta Vtn$) on the trip point of the inverter. Similarly, V_{READ} can be given by (assuming $Vtn_{SR} \approx Vtn_{NR} = Vtn$) [5]:

$$V_{READ} = \frac{(V_{DD} - Vt_{n0} - \Delta Vtn)\left(1 + \sqrt{\left(\frac{\beta_{NR}}{\beta_{SR}}\right)} \pm \sqrt{\left(\frac{\beta_{NR}}{\beta_{SR}}\right) + \left(\frac{\beta_{NR}}{\beta_{SR}}\right)}\right)}{1 + \sqrt{\left(\frac{\beta_{NR}}{\beta_{SR}}\right)}} \quad (7)$$

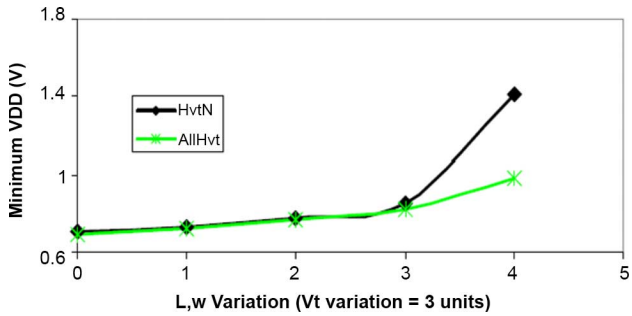

Fig. 13. Impact of using high Vt transistors on write-ability. X-axis represents different units of L, W variation along with 3 units of Vt variation.

The use of high Vt NMOS $\mathrm{N_R}$ increases the on resistance of the pull-down path and thus results in a higher V_{READ}. However, high Vt NMOS $\mathrm{S_R}$ lowers the current into the node R and hence lowers $\mathrm{V_{READ}}$. It can be observed from Fig. 5 that S_R is more critical than N_R in increasing V_{READ} due to parameter variation. Hence, using high Vt NMOS decreases the $\mathrm{V_{READ}}$ (see (7)) and helps to improve read-stability. Simultaneously, high Vt NMOS increases the trip point of the inverter $\mathrm{P_L}$-$\mathrm{N_L}$ and reduces the subthreshold leakage of $\mathrm{N_L}$, thereby improving the read stability. Moreover, the improvement primarily comes from the use of higher Vt NMOS transistors. Hence, improvement in stability from *HighVtN* to *AllHVT* is not very significant (Fig. 12).

B. Write-Ability With High Vt

As explained in Section III-A, use of high Vt transistors increases the trip point of the inverter $\mathrm{P_R}$-$\mathrm{N_R}$, thereby helping to improve the write-ability (see (3)). Using high Vt NMOS $(\mathrm{S_L})$ reduces the discharging current (degrading write-ability) but using high Vt PMOS transistor $(\mathrm{P_L})$ increases the discharging current for node 'L' (improving write-ability). Hence, it can be concluded that, migrating from *AllNomVt* to *HighVtN* does not improve the write-ability. However, use of *AllHVT* cell improves the write-ability (Fig. 13). A larger improvement is achieved at higher variation of the process parameters.

IV. Stability With Thick-Oxide Transistors

The use of high-Vt transistors in a cell reduces the subthreshold leakage of an SRAM cell. However, in nano-scale transistors gate leakage is a major contributor to the total leakage. Hence, to reduce the total leakage of the cell it is necessary to reduce the gate leakage of the cell transistors. Fig. 1 shows the different transistors that contribute to the gate leakage. Fig. 14(a) shows the different leakage component of an SRAM cell for different Vt and Tox assignment (ThickN1.5 $\equiv$ High Vt & Thick Oxide (by 1.5 A°) NMOS and Nominal Vt Nominal Oxide PMOS; ThickN1.5HvtP $\equiv$ High Vt & Thick Oxide (by 1.5 A°) NMOS and High Vt Nominal oxide PMOS; ThickN3.0HvtP $\equiv$ High Vt & Thick Oxide (by 3 A°) NMOS and High Vt Nominal oxide PMOS). It can be observed that, use of AllHighVt cell reduces the subthreshold leakage of the cell. However, in AllHighVt cell gate leakage is the dominant leakage mechanism (at T = 25 C). Hence, using thick oxide NMOS devices significantly reduces the total leakage from the AllHighVt case. It should be noted that, thick oxide PMOS does not have a strong impact as the gate leakage in PMOS is much lower than that in NMOS. It can be noted that, use of thick oxide NMOS and all high Vt devices results in 11X reduction in total cell leakage compared to the cell with all nominal Vt and all nominal Tox. The improvement increases at a higher temperature. The performance degradation associated with the 11X leakage reduction from AllNomVt to ThickN3.0HvtP is negligible ($\sim 5\%$) (Fig. 14(b)). Hence, use of thicker oxide (and higher Vt) devices is efficient in reducing cell leakage with negligible performance penalty. In the following section we will analyze the effect of thicker oxide devices on read stability and write-ability.

A. Read Stability With Thick-Oxide Devices

Increasing the oxide thickness of the NMOS transistors increases the trip point of the inverter $\mathrm{P_L}$-$\mathrm{N_L}$. To understand that let us consider the expression of $\mathrm{V_{TRIP}}$ from (5):

$$\begin{aligned} V_{TRIP} &= \frac{V_{DD} - Vt_p + Vt_{n0}\sqrt{\left(\frac{\beta_{NL}}{\beta_{PL}}\right)}}{1+\sqrt{\left(\frac{\beta_{NL}}{\beta_{PL}}\right)}} \\ &= \frac{V_{DD} - Vt_p + Vt_{n0} r}{1+r}; \text{ where,} \\ r &= \sqrt{\left(\frac{\beta_{NL}}{\beta_{PL}}\right)} \Rightarrow \frac{\partial V_{TRIP}}{\partial r} \\ &= \frac{Vt_{n0}(1+r) - (V_{DD} - Vt_p + Vt_{n0} r)}{(1+r)^2} \\ &= -\frac{(V_{DD} - Vt_p + Vt_{n0})}{(1+r)^2} < 0 \end{aligned} \tag{8}$$

Increasing the T_{ox} of the NMOS alone reduces β_{NL} thereby reducing r $(= \sqrt{\beta_{NL}/\beta_{PL}})$. Hence, from (8) it can be observed that increasing the oxide thickness of NMOS increases the trip-point thereby improving the read stability. Moreover, increasing oxide thickness of NMOS reduces the strength of both $\mathrm{N_R}$ (NMOS transistor) and $\mathrm{S_R}$ (access transistor). Since the access transistor has a stronger impact on read stability (see Fig. 5), increasing the NMOS oxide thickness helps to reduce $\mathrm{NV_{READ}}$ thereby further improving the read stability. From Fig. 15(a) use of thicker oxide NMOS devices shows a large improvement in read stability (Fig. 15(a)). First, compared to *HvtN* case increasing NMOS oxide thickness (ThickN1.5) results in a significant improvement in read stability. The similar improvement is also observed from *AllHigh* to *ThickN1.5HvtP*. However, increasing NMOS oxide thickness from 1.5 A° to 3.0 A° does not result in significant additional improvement. It is also interesting to note that, the minimum stable $\mathrm{V_{DD}}$ for ThickN1.5 is marginally higher than ThickN1.5HvtP. This is due to the fact that, a higher Vt PFET reduces the trip-point and hence degrades stability for low VDD as explained in Section II.

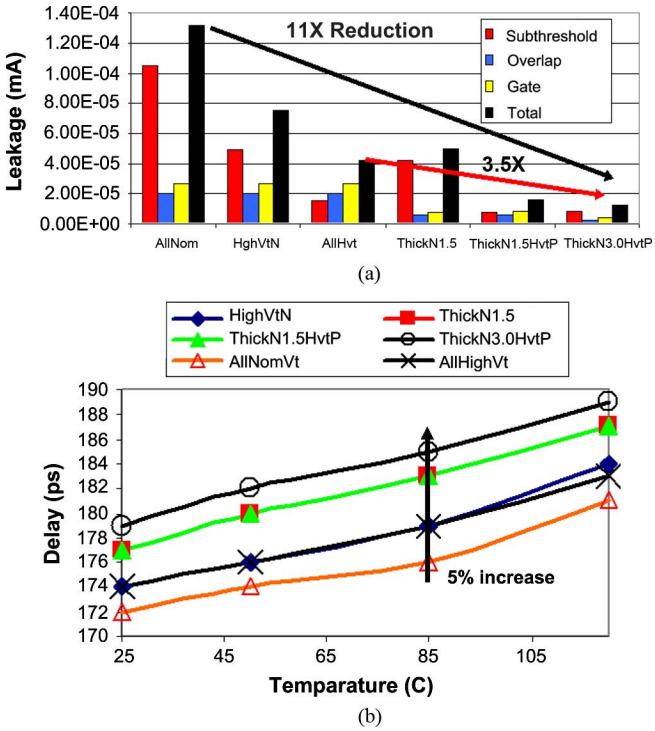

Fig. 14. Effect of Vt and oxide thickness of different devices on SRAM cell: (a) Leakage components for different Vt and $\mathrm{T_{ox}}$ assignment, and (b) Cell performance (read delay) for different Vt and Tox assignment.

B. Write-Ability With Thick-Oxide Devices

As explained in Section IV-A, use of thick-oxide NMOS transistors increases the trip point of the inverter $\mathrm{P_R}$-$\mathrm{N_R}$, thereby helping to improve the write-ability. On the other hand, higher oxide thickness of S_L reduces its strength. Consequently, the rate of discharge of node L (storing "1") reduces. However, it should be noted that, increasing the Tox of S_L marginally improves its mobility (lower vertical electric field implies lower scattering). Hence, the overall impact in the discharge rate of node "L" is marginal ($\sim 1\%$). This is evident from the negligible (1%) increase in the write delay associated with the thick oxide cells. Hence, the overall impact of thick oxide cells on write-ability is marginal. Fig. 15(b) shows that, the write-ability of the AllHvt cell is much better compared

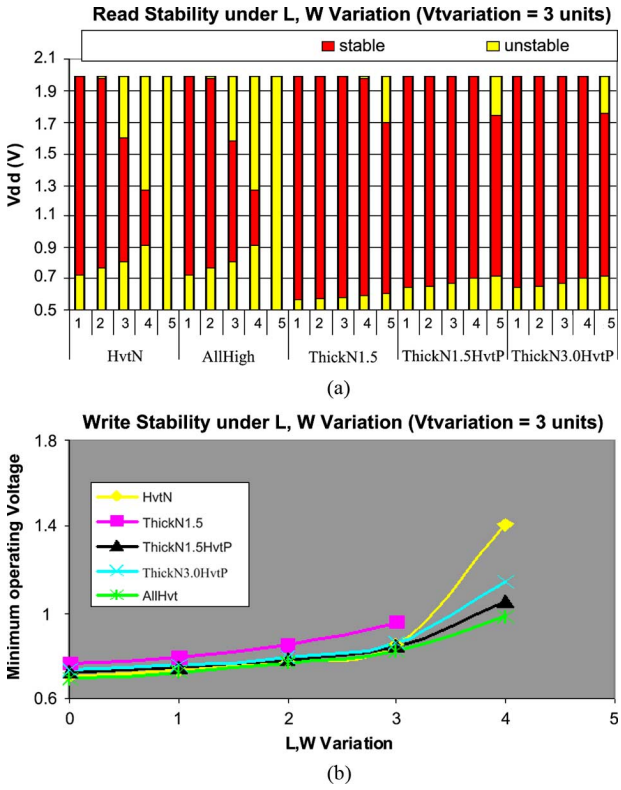

Fig. 15. Impact of using high-Vt and thick-oxide transistors on (a) Read-stability, and (b) Write-ability. X-axis represents different units L, W variations along with 3 units of Vt variations.

to the other cases. Increasing the thickness of NMOS devices with nominal Vt PMOS *ThickN1.5* significantly worsens write-ability. With a high-Vt PMOS, increasing NMOS oxide thickness results in marginal degradation of write-ability. From Figs. 15(a) and 15(b) it can be observed that, all highVt devices with thick-oxide NMOS device can result in significantly lower leakage and better read stability, with marginally lower performance and write-ability. Use of thick-oxide PMOS along with thick-oxide NMOS can result in further leakage saving and better-write-ability with a minimal impact on read stability. This is verified through hardware measurement as shown later.

V. Test-Chip Design and Measurement Results

A test-chip is designed in sub-90nm PD/SOI technology to evaluate the effects of threshold voltage and gate oxide thickness on SRAM cell stability. The die photo for the SRAM cell stability characterization macro is shown in Fig. 16(a) and the detail layout is shown in Fig. 17(a). The designed the SRAM fly cell macro uses a 25-pad-set to characterize the dense SRAM cell device DC parametrics for a 36 Kbit SRAM array. The SRAM devices cells are wired out using metal layer. Two inverters in the cell are disconnected to accurately characterize the devices and cell stability. The device threshold voltage of each of the six transistors is measured in-line at room temperature and nominal supply voltage (1.0 V for this technology). The saturation threshold voltage (Vtsat) is defined by the gate-source voltage (Vgs) at which the drain is connected to supply voltage

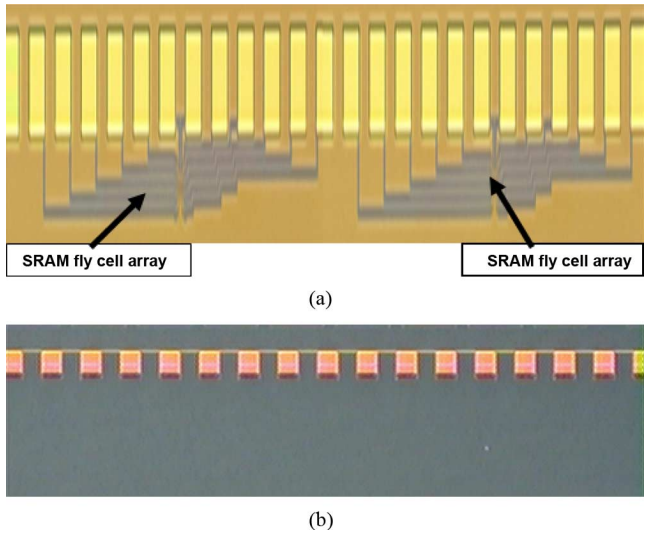

Fig. 16. Die-photo of the SRAM array showing (a) The fly cells for stability characterization, and (b) SRAM yield monitor.

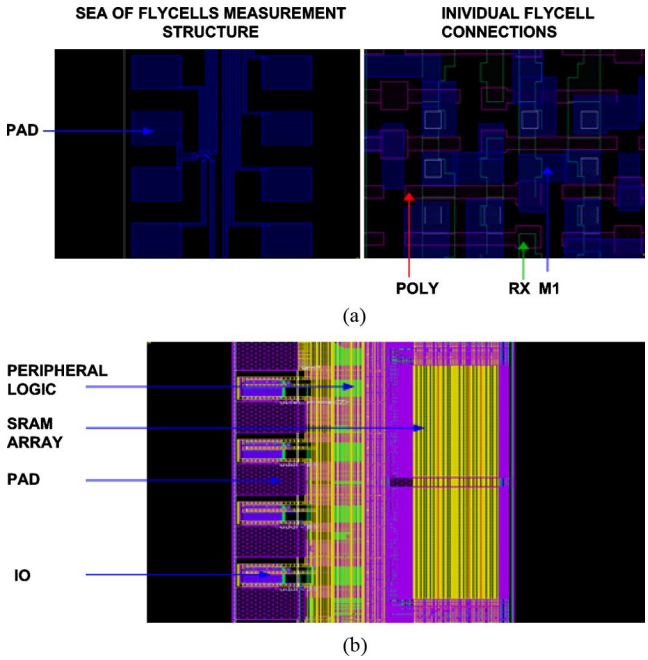

Fig. 17. Layout of the SRAM array showing (a) The fly cells for stability characterization, and (b) SRAM yield monitor (layouts are also shown as actual photomicrographs are obscured by metal fill).

and the source-drain current reaches 300 nA/um, and 70 nA/um, for N-type and P-type, respectively. The yield of SRAM is based on 1 Mbit arrays. Fig. 16(b) shows the die-photo of the SRAM yield monitor and Fig. 17(b) shows the layout. Onchip yield monitor circuits are used to measure the yield.

Fig. 18 shows the effect of device threshold voltage on read and write-ability of SRAM cells (normalized stability values are shown). The Vth value for all cell devices are increased in the fabricated cells. As predicted in Section III, use of higher Vt improves both read and write-ability, whether lower Vt degrades both of them. The high-Vt NMOS improves the read-stability while high-Vt PMOS results in better write-ability. Moreover,

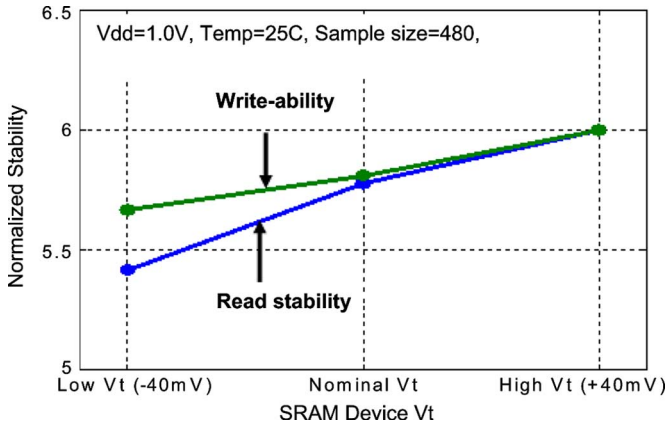

Fig. 18. Stability improvement with higher Vt devices.

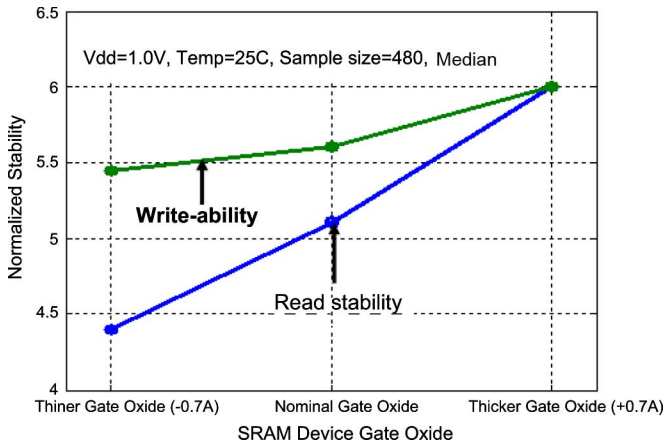

Fig. 19. Stability improvement with thicker oxide devices.

it can be observed that, the use of high-Vt improves read-stability more strongly. This is because, as explained in Section III, higher Vt simultaneously increases trip voltage and reduces read voltage. The improvement is less for write-ability. This is because, with a higher Vt the pass transistors becomes weaker and negatively impacts write-ability and reduces the overall improvement of write-ability. Fig. 19 shows the effects of oxide thickness on read and write-ability. The oxide-thickness for both NMOS and PMOS are increased in the fabricated cells. As predicted in Section IV, use of thicker oxide NMOS improves read-stability and thicker-oxide PMOS improves and write-ability. Therefore, thicker-oxide cells have both read stability and write-ability. Further, improvement of read stability is more compared to the write-ability. Fig. 20 shows the yield improvement of a 1Mbit array with the use of higher Vt pass gate devices. It can be observed that, significant yield improvement can be achieved with the use of higher Vt. Further, this shows that proper design/optimization of the device Vt may be helpful for yield improvement.

VI. Conclusions

With increasing variation in the process parameters, the dynamic stability of the SRAM cell during read and write

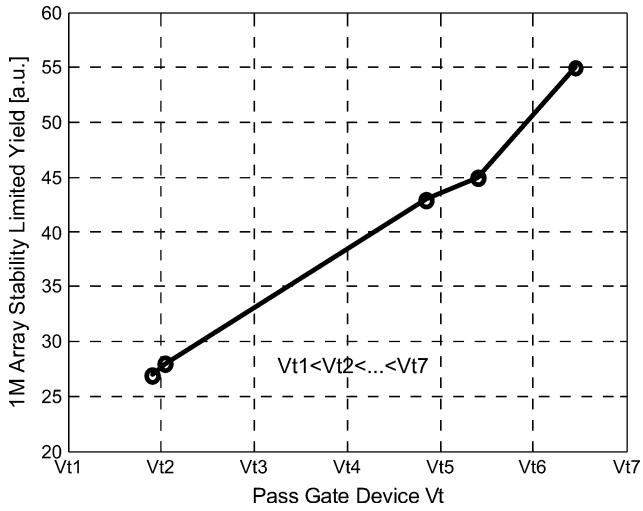

Fig. 20. Yield improvement with optimization of Vt value of higher-Vt devices.

operations has emerged as a serious design challenge. In this work we have presented a detailed study of the read and the write-ability for a sub-100 nm PD/SOI SRAM cell under parameter variations. PD/SOI specific aspects such as floating body effect and gate-to-body tunneling current were considered. The floating body effect was shown to degrade the read stability while improving the write-ability. On the other hand, the gate-to-body tunneling current improved the read stability while degrading the write-ability. The impact of using high Vt and thick oxide transistors in the cell on the cell stability has been evaluated and it has been shown that, high Vt and thick oxide cells offer improvement in leakage, read and write-ability without causing significant performance degradation. The study provided the basic understanding for maintaining/exploiting PD/SOI SRAM performance advantage and is corroborated with the SRAM hardware data.

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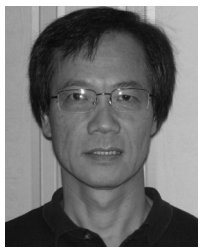

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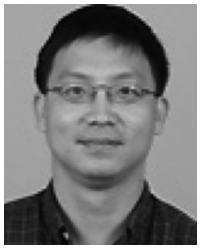
Dr. Chuang has received an Outstanding Technical Achievement Award, a Research Division Outstanding Contribution Award, five Research Division Awards, and 12 Invention Achievement Awards from IBM. He took early retirement from IBM to join National Chiao-Tung University, Hsinchu, Taiwan, as a Chair Professor in the Department of Electronic Engineering in February 2008. He has received the Outstanding Scholar Award from Taiwan's Foundation for the Advancement of Outstanding Scholarship for 2008 to 2013.

Dr. Chuang served on the Device Technology Program Committee for IEDM in 1986 and 1987, and the Program Committee for Symposium on VLSI Circuits from 1992 to 2006. He was the Publication/Publicity Chairman for Symposium on VLSI Technology and Symposium on VLSI Circuits in 1993 and 1994, and the Best Student Paper Award Sub-Committee Chairman for Symposium on VLSI Circuits from 2004 to 2006. He was elected an IEEE Fellow in 1994 "for contributions to high-performance bipolar devices, circuits, and technology". He has authored many invited papers in international journals including *International Journal of High Speed Electronics*, *Proceedings of the IEEE*, *IEEE Circuits and Devices Magazine*, and *Microelectronics Journal*. He has presented numerous plenary, invited or tutorial papers/talks at international conferences such as International SOI Conference, DAC, VLSI-TSA, ISSCC Microprocessor Design Workshop, VLSI Circuit Symposium Short Course, ISQED, ICCAD, APMC, VLSI-DAT, ISCAS, MTDT, and WSEAS. He was a corecipient of the Best Paper Award at the 2000 IEEE International SOI Conference. He holds 27 U.S. patents with 14 pending. He has authored or coauthored over 260 papers.



Yue Tan received the B.S. and M.S. degrees in electronic engineering from Southeast University, China, in 1991 and 1995, respectively, and the Ph.D. degree in electrical and electronic engineering from the Hong Kong University of Science and Technology (HKUST), where he designed and implemented a fully integrated SOI RF power amplifier for 900 MHz wireless applications. Meanwhile, he also developed a high voltage (100 V) CMOS technology for Plasma Display Panel application in a 0.6 μm technology.

In 2001, he joined IBM Microelectronics Division. He began work on SOI RF devices and integrated circuits design at IBM Semiconductor Research and Development Center in Hopewell Junction, NY, as a means of supporting early SOI device, technology, and electronic design automation learning for foundry business and product in 130 nm and 90 nm technology nodes. Since 2003, he has applied his interest in developing traditional 6-T SRAM for leading-edge technologies for bulk and SOI. Currently, Dr. Tan is taking SRAM cell ownership responsibility for IBM SOI technology. He is developing the highest performance SRAM cell for a given area with robust manufacturing process window and optimized for product yield and minimum array operating voltage from 90 nm to 22 nm technology nodes. Focusing predominantly on SOI device, circuit design, electronic design automation, and technology integration, He has authored or coauthored more than 30 papers in technical journals and referred conferences. He holds many published and pending U.S. patents.