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Current-mode design techniques in low-voltage 24-GHz RF CMOS receiver front-end

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Abstract A new high frequency CMOS current-mode receiver front-end composed of a current-mode low noise amplifier (LNA) and a current-mode down-conversion mixer has been proposed in the frequency band of 24 GHz and fabricated in 0.13-μm 1P8M CMOS technology. The measurement of the current-mode receiver front-end exhibits a conversion gain of 11.3 dB, a noise figure (NF) of 14.2 dB, the input-referred 1-dB compression point ($P_{-1\,\mathrm{dB}}$) of −13.5 dBm and the input-referred third-order intercept point (P_{IIP3}) of −1 dBm. The receiver dissipates 27.8 mW where the supply of LNA is 0.8 V and the supply of mixer is 1.2 V. The power consumption of output buffer is not included. The receiver front-end occupies the active area of $1.45 \times 0.72\ \mathrm{mm}^2$ including testing pads. The measured results show that the proposed current-mode approach can be applied to a high-frequency receiver front-end and is capable of low-voltage applications in the advanced CMOS technologies.

Keywords 24-GHz · CMOS · Current-mode · Receiver front-end

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1 Introduction

Over the last two decades, the frequency spectra below 10 GHz have gradually become crowded because of massive requirements of data transmission from the modern wireless applications such as Bluetooth, wireless local area network (WLAN) and ultra-wideband (UWB), etc. Consequently, many researchers start to investigate RF transceiver front-end circuits in much higher frequency bands like 24 and 60 GHz for example because higher operating frequency can provide more bandwidth. In addition to the original industrial-science-medical (ISM) band within 24–24.25 GHz, the FCC has opened the 22–29-GHz frequency band in 2002 for short-range automotive radar systems, autonomous cruise control (ACC) for example [1]. In the 24-GHz frequency range, some applications such as radars, wireless local area networks, point-to-point wireless communications, local multipoint distribution services (LMDS) and other ISM band applications are implemented by CMOS, SiGe BiCMOS and III-V compound semiconductor [2–6].

Table 1 shows the pros and cons of different technologies which are used for the implementation of 24-GHz systems. Although III–V compound semiconductor and SiGe BiCMOS have good performance in higher frequency RF circuits, the cost of these technologies is relatively higher than CMOS technologies. In addition, these technologies suffer from the difficulties to integrate with complex digital systems which are usually realized by CMOS technologies for low cost and low power. With the fast advancement of CMOS technologies, the nanometer CMOS technologies have already become a candidate to realize 24-GHz or even 60-GHz RF systems. Consequently, nanometer CMOS technologies are recommended to realize 24-GHz systems because of their advantages of

Table 1 The pros and cons of different technologies

	GaAs	BiCMOS	CMOS
g_m	High	High	Low
f_T	High	Moderate	Moderate
RF performance	High	High	Moderate
Yield	Low	Moderate	High
Integration	Low	Moderate	High
Cost	High	Moderate	Low
Technology improvement	Slow	Moderate	Fast

higher integration level, smaller chip area, lower power consumption and lower cost.

As the CMOS technology is scaled down to nanometer nodes, the supply voltage is gradually reduced to around or even below 1 V. The lower the supply voltage, the smaller the voltage headroom is left in the design of CMOS RF circuits. In voltage-mode circuits, the impedances of internal nodes are usually large so that the signal information can be mostly carried with the time-varying voltage signals. Since large enough voltage swing is required to keep signal information, it is difficult for voltage-mode circuits to use reduced voltage headroom under low supply voltage.

In current-mode circuits, however, the impedances of internal nodes are smaller than those in voltage-mode circuits and voltage swings at internal nodes become smaller. But the signal information is mainly carried with the time-varying current signals. Consequently, current-mode circuits can be designed under small voltage headroom. Furthermore, when dealing with signal processing, it is easy to perform the function of summation by simply connecting the signal paths together without additional amplifiers. Thus power consumption can be further reduced. With the above advantages, current-mode RF circuits are capable of operating in low supply voltage and dissipating smaller power. The current-mode design techniques can have great potential in the design of CMOS RF front-end in the advanced nanometer CMOS technologies.

Two current-mode CMOS RF front-end circuits have been published by the present authors [7, 8]. A 24-GHz current-mode power amplifier (PA) was designed in 0.13-μm bulk CMOS technology [7]. This CMOS current-mode PA can achieve large output power with high power added efficiency (PAE) in the 24-GHz frequency range. The proposed PA is capable of operating in the low supply voltage of 1.2 V. In [8], a 24-GHz transmitter using current-mode approach in 0.13-μm CMOS technology is proposed. The transmitter is operated in low supply voltage of 1 V, and it consumes very small power. So far, no current-mode CMOS receiver circuit is proposed.

The first 24-GHz receiver front-end using current-mode design techniques in 130-nm CMOS technology is proposed, analyzed, and measured. The proposed current-mode receiver front-end is of single-balance structure and integrated with a current-mode LNA and a current-mode down-conversion mixer. In the proposed current-mode LNA, two cascaded current-mirror amplifiers are adopted to realize the amplification of current signals. Following the LNA is the current summing circuit to perform the summation of RF and LO signals. The summed signal is sent to the current squaring circuit to perform the function of current mixing of RF and LO signals. The measurement results have shown that the proposed current-mode CMOS receiver achieves the conversion gain of 11.3 dB, the $P_{1\,dB}$ of −13.5 dBm, and the P_{IIP3} of −1 dBm. The measured total NF is 14.2 dB at RF frequency of 24 GHz and LO frequency of 19 GHz. The current-mode receiver front-end dissipates 27.8 mW under the condition that the supply of the LNA is 0.8 V and the supply of the mixer is 1.2 V. Compared to other implementations for 24-GHz receiver front-ends in [2] and [5], the proposed 24-GHz current-mode receiver front-end has the advantage of low-voltage operation and low-power dissipation with comparable performances.

In Sect. 2, the architecture, operational principles, and circuit realizations of CMOS current-mode RF receiver front-end are described. The experimental chip is designed and fabricated in 130-nm 1P8M CMOS technology. The measurement results are presented in Sect. 3 to verify the circuit performances. Finally, the conclusion is given in Sect. 4.

2 Operational principles and circuit realizations

The block diagram of the designed 24-GHz receiver front-end is shown in Fig. 1. It is composed of a LNA and a mixer. The off-chip signal generator provides the local oscillator (LO) signal for the receiver. With the LO signal at 19 GHz, the received RF signal at 24 GHz is

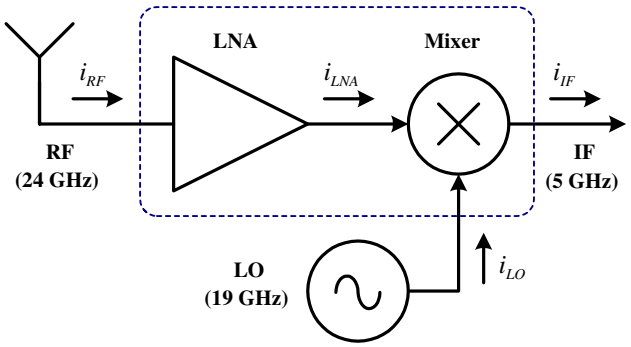

Fig. 1 Block diagram of the 24-GHz current-mode receiver front-end

down-converted to the intermediate frequency (IF) which is at the frequency band of 5 GHz by the Mixer. The IF is chosen at 5 GHz so that the mature RF receiver front-end circuits at 5 GHz can be adopted to realize the second-step down-conversion from the IF to the baseband.

In the design of CMOS LNA, the CMOS current-mirror structure is adopted as the current amplifier and two stages of current-mirror amplifiers are cascaded to provide sufficient gain. As for the current-mode down-conversion mixer, the high frequency analog current multiplier is proposed. It consists of a current summing circuit and a current squaring circuit. The detailed circuit designs and analyses are presented in the following.

2.1 Current-mode LNA

The circuit diagram of the proposed current-mode LNA is shown in Fig. 2(a) where M_1 and M_2 form the first-stage current-mirror amplifier and M_3 and M_4 form the second stage cascaded with the first stage. All MOS are operated in the saturation region. The aspect ratio of M_2 is designed M times of that of M_1 whereas the aspect ratio of M_4 is designed N times of that of M_3. Therefore, the gate-source capacitances of $M_2(M_4)$, $C_{GS,M_2}(C_{GS,M_4})$, is about $M(N)$ times of C_{GS,M_1} (C_{GS,M_3}). M_6-M_8 with gate shorted to drain are used to reduce the supply voltage to the amplifiers so that the LNA can be biased well and operated at low dc power dissipation. The bypass capacitors C_1-C_3 are used at the nodes A_1-A_3, respectively, to make them ac ground and bypass the supply noise. If V_{DD} is low enough, M_6-M_8 and C_1-C_3 is not required as shown in Fig. 2(b). To reduce the signal losses at the operating frequency, the inductors L_1-L_3 are chosen as the loads of the current-mode LNA to resonate out the parasitic capacitances C_{T_1}, C_{T_2}, and C_{T_3} at the nodes A_4, A_5, and A_6, respectively, where $C_{T_1} = (1+M)C_{GS,M_1} + C_{DS,M_1}$, $C_{T_2} = (1+N)C_{GS,M_3} + C_{DS,M_2} + C_{DS,M_3}$ and $C_{T_3} = C_{DS,M_4}$.

The input ac coupling capacitor C_{IN} and the input pad with the capacitance of C_{PAD1} form the input matching network of the current-mode LNA. C_{OUT} is the capacitor that blocks dc between LNA and the following current-mode mixer. Only ac current signals can pass to the next stage. L_{GD} is designed to resonate out the gate-drain capacitor C_{GD2} of M_2 at the operating frequency ω_0 in order to enhance the reverse isolation of the LNA. After resonating out the parasitic capacitances of the transistor between its gate and drain, the transistor becomes more unilateral so that the stability can be improved. In addition, the input matching network is easier to design because of good isolation of the LNA.

At the operating frequency ω_0, inductors L_1-L_3 and the respective parasitic capacitors $C_{T_1}-C_{T_3}$ are resonated. The small-signal equivalent circuits of the current-mode

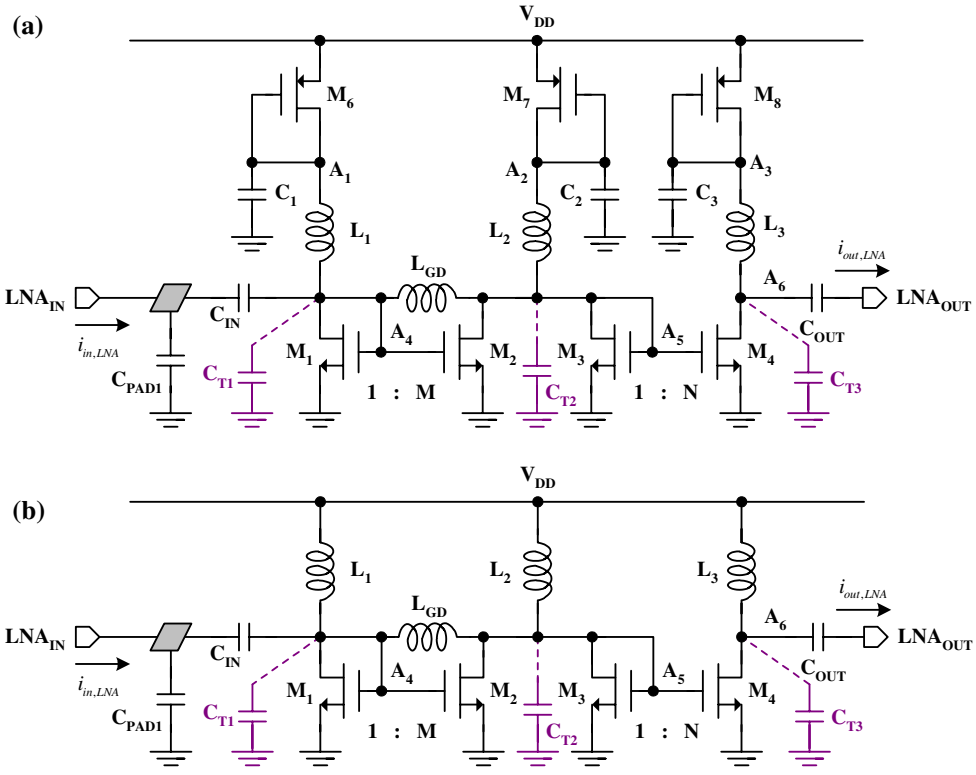

Fig. 2 (**a**) Circuit diagram of the current-mode LNA and (**b**) circuit diagram of the current-mode LNA of low-voltage version

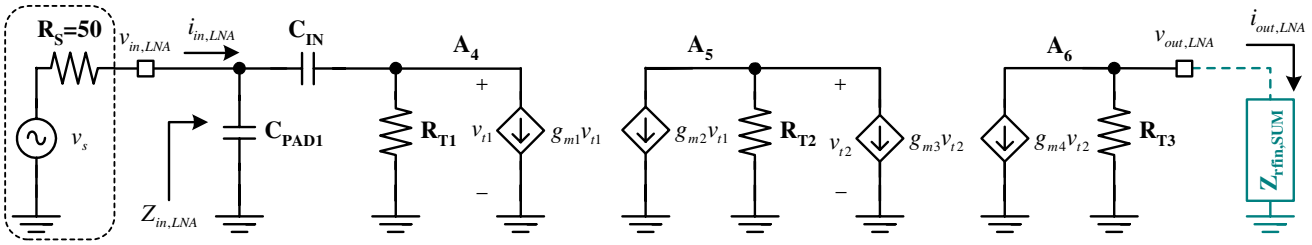

Fig. 3 Small-signal equivalent circuit of the current-mode LNA at the operating frequency ω_0

LNA of Fig. 2(a) and 2(b) at the operation frequency ω_0 are the same and can be depicted in Fig. 3 where $R_{T_1} = (R_{p,L_1} // r_{o,M_1})$, $R_{T_2} = (R_{p,L_2} // r_{o,M_2} // r_{o,M_3})$ and $R_{T_3} = (R_{p,L_3} // r_{o,M_4})$. $R_{p,L_1}-R_{p,L_3}$ are the equivalent parallel resistances of the inductors L_1-L_3. $r_{o,M_1}-r_{o,M_4}$ and $g_{m_1}-g_{m_4}$ are the output impedance and transconductance of the transistors M_1-M_4, respectively. Because the circuit dimensions are much smaller than the wavelengths involved, the distributed effect of circuits is negligible. Thus the lumped small-signal equivalent circuit is adopted.

From Fig. 3, the input impedance $Z_{\text{in,LNA}}$ in s-domain can be expressed as

$$Z_{\text{in,LNA}}(s) = \frac{1}{sC_{\text{PAD1}}} \parallel \left[\frac{1}{sC_{\text{IN}}} + \left(R_{T_1} \parallel \frac{1}{g_{m_1}}\right)\right] = \frac{(1+g_{m_1}R_{T_1}) + sR_{T_1}C_{\text{IN}}}{s(C_{\text{PAD1}}+C_{\text{IN}}) + s^2 C_{\text{PAD1}}C_{\text{IN}}R_{T_1}}. \quad (1)$$

Let $s = j\omega$ and the input impedance of the LNA can be calculated as

$$Z_{\text{in,LNA}}(j\omega) = \frac{\omega R_{T_1}C_{\text{IN}}[(C_{\text{PAD1}}+C_{\text{IN}}) - (1+g_{m_1}R_{T_1})C_{\text{PAD1}}]}{\omega\left[(C_{\text{PAD1}}+C_{\text{IN}})^2 + (\omega R_{T_1}C_{\text{PAD1}}C_{\text{IN}})^2\right]} - j\frac{\left[(1+g_{m_1}R_{T_1})(C_{\text{PAD1}}+C_{\text{IN}}) - \omega^2 R_{T_1}^2 C_{\text{IN}}^2 C_{\text{PAD1}}\right]}{\omega\left[(C_{\text{PAD1}}+C_{\text{IN}})^2 + (\omega R_{T_1}C_{\text{PAD1}}C_{\text{IN}})^2\right]}. \quad (2)$$

In order to achieve maximum power transfer, $Z_{\text{in,LNA}}$ should be equal to 50 Ω at the operation frequency ω_0. The imaginary part of the $Z_{\text{in,LNA}}$ can be eliminated at ω_0 if the following equation is satisfied.

$$(1+g_{m_1}R_{T_1})(C_{\text{PAD1}}+C_{\text{IN}}) - \omega_0^2 R_{T_1}^2 C_{\text{IN}}^2 C_{\text{PAD1}} = 0. \quad (3)$$

Thus the relation among $C_{\text{IN}}, C_{\text{PAD1}}, R_{T_1}$, g_{m_1}, and ω_0 can be designed according to the following equation

$$\omega_0 = \frac{1}{R_{T_1}C_{\text{IN}}}\sqrt{(1+g_{m_1}R_{T_1})\left(1+\frac{C_{\text{IN}}}{C_{\text{PAD1}}}\right)}. \quad (4)$$

Substituting (4) into (2), the input impedance at the operation frequency ω_0 can be expressed as

$$Z_{\text{in,LNA}}|_{\omega=\omega_0} = \frac{R_{T_1}C_{\text{IN}}[(C_{\text{PAD1}}+C_{\text{IN}}) - (1+g_{m_1}R_{T_1})C_{\text{PAD1}}]}{\left[(C_{\text{PAD1}}+C_{\text{IN}})^2 + (\omega_0 R_{T_1}C_{\text{PAD1}}C_{\text{IN}})^2\right]}. \quad (5)$$

To calculate the current gain A_i and the voltage gain A_v of the LNA, the input impedance $Z_{\text{rfin,SUM}}$ of the following current mixer should be taken into considerations. From Fig. 3, the current gain A_i at the operating frequency ω_0 can be calculated and expressed as

$$A_i|_{\omega=\omega_0} \equiv \left.\frac{i_{\text{out,LNA}}}{i_{\text{in,LNA}}}\right|_{\omega=\omega_0} = \frac{g_{m_2}g_{m_4}R_{T_1}R_{T_2}}{(1+g_{m_3}R_{T_2})\sqrt{(1+g_{m_1}R_{T_1})^2(1+C_{\text{PAD1}}/C_{\text{IN}})^2 + \omega_0^2 R_{T_1}^2 C_{\text{PAD1}}^2}} \cdot \left(\frac{R_{T_3}}{Z_{\text{rfin,SUM}}+R_{T_3}}\right). \quad (6)$$

The simulated gain, NF, and input matching characteristics of the current-mode LNA in Fig. 2(b) are shown in Fig. 4. The LNA can achieve the maximum gain of 17 dB at the operating frequency of 24 GHz. It can reach the NF of 3.4 dB at 24 GHz. The linearity performance of the LNA is verified by harmonic balance (HB) simulation. With the signals at 23.9 and 24.1 GHz, the simulated linearity curves shown in Fig. 5 depicts a $P_{-1\,\text{dB,LNA}}$ of −18.5 dBm and a $P_{\text{IIP3,LNA}}$ of −10.8 dBm. The LNA in Fig. 2(b) drains 20.4 mA from the supply voltage of 0.8 V and drains 34.82 mA from the supply voltage of

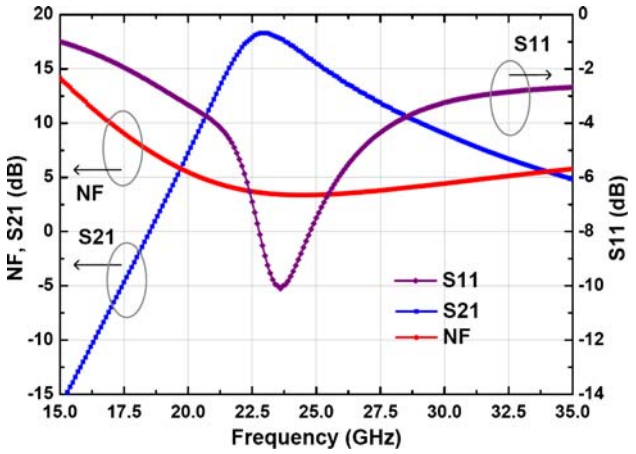

Fig. 4 Simulated gain, NF, and input matching characteristics of the current-mode LNA

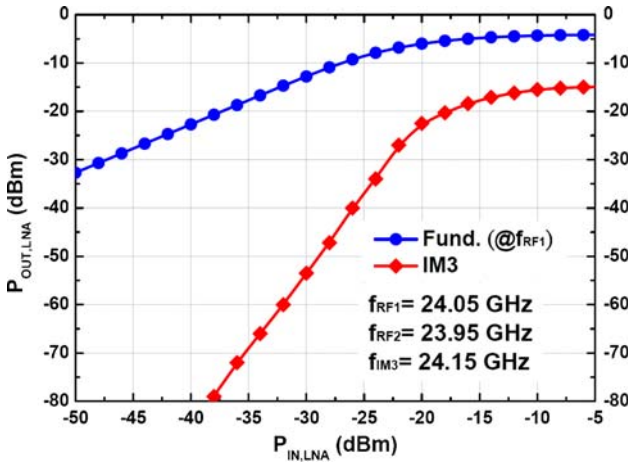

Fig. 5 Simulated linearity performance of the current-mode LNA

1.2 V. The increase in simulated current consumption from 20.4 to 34.82 mA is because the overdrive voltage of LNA is changed from 0.8 to 1.2 V as the supply voltage is increased from 0.8 to 1.2 V.

The accuracy of the gain (S_{21}) of the LNA over different process corners including FF, FS, TT, SF, SS are depicted in Fig. 6(a) and (b). The S_{21} is varied from around 17.6 to 13.8 dB at the supply voltage of 0.8 V and is varied from about 18.1 to 16.9 dB at the supply voltage of 1.2 V.

2.2 Current-mode down-conversion mixer

The conceptual block diagram of the proposed current-mode down-conversion mixer is depicted in Fig. 7. This mixer is composed of a current summing circuit, a current squaring circuit, and a band-pass filter (BPF). The RF input

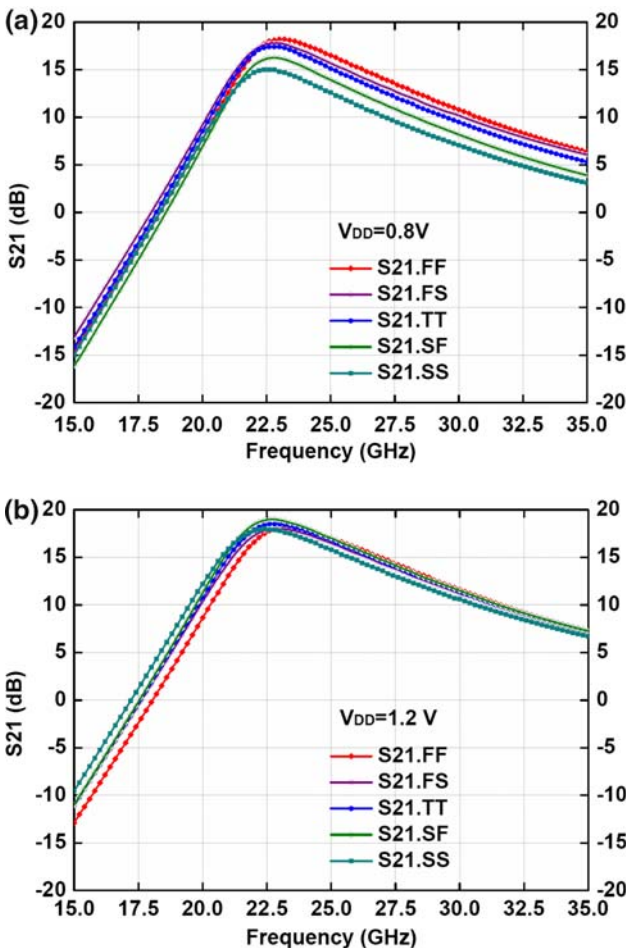

Fig. 6 S_{21} of the LNA in different process corners (**a**) at the supply voltage of 0.8 V and (**b**) at the supply voltage of 1.2 V

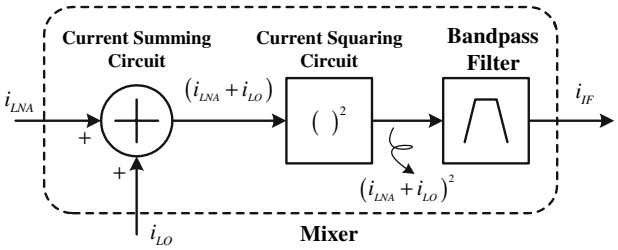

Fig. 7 Conceptual block diagram of the current-mode down-conversion mixer

current signal $i_{\mathrm{LNA}} = I_{\mathrm{LNA}} \cos \omega_{\mathrm{RF}} t$ from the current-mode LNA and the LO input current signal $i_{\mathrm{LO}} = I_{\mathrm{LO}} \cos \omega_{\mathrm{LO}} t$ from the off-chip LO signal generator are summed in advance through the current summing circuit. The summed current signal $i_{\mathrm{SUM}} = (i_{\mathrm{LNA}} + i_{\mathrm{LO}}) = (I_{\mathrm{LNA}} \cos \omega_{\mathrm{RF}} t + I_{\mathrm{LO}} \cos \omega_{\mathrm{LO}} t)$ are sent to the following current squaring circuit which results in the square components of i^2_{LNA} and i^2_{LO} and the multiplication component $i_{\mathrm{LNA}} \times i_{\mathrm{LO}}$. The

multiplication component of two current input signals provides the function of double sideband mixing.

Through the double sideband mixing, the received 24-GHz signal is converted to 5 GHz which is the lower sideband (LSB) and 43 GHz which is the upper sideband (USB) with the LO signal at 19 GHz. Following the current squaring circuit is the BPF which is capable of frequency selectivity. In this receiver design, the center frequency of the BPF is designed at 5 GHz so that the targeted LSB can be obtained and the unwanted USB can be attenuated. The detailed operational principles of the current squaring circuit and the current summing circuit are described in the following subsections.

2.2.1 Current squaring circuit and band-pass filter

The conceptual circuit of the current squaring circuit as modified from [9] is shown in Fig. 8 where M_{SQ_1} and M_{SQ_2} are current mirror circuit. The bulk and source of M_{SQ_3} are connected together to eliminate the body effect. Assume that both short-channel effect and channel-length modulation effect are negligible, and the MOS transistors $M_{SQ_1}-M_{SQ_3}$ are well matched with the same channel width/length W/L. If all MOS devices are in the saturation region, the relation between $v_{GS,MSQ_1}, v_{GS,MSQ_3}$, and the input current i_{in} can be expressed as

$$v_{GS,MSQ_1} = \frac{V_B}{2} + \frac{i_{in}}{k_n \frac{W}{L}(V_B - 2V_{th})}, \tag{7}$$

$$v_{GS,MSQ_3} = \frac{V_B}{2} - \frac{i_{in}}{k_n \frac{W}{L}(V_B - 2V_{th})}, \tag{8}$$

where $k_n = \mu_n C_{OX}$ is the mobility μ_n times the oxide capacitance per unit area C_{OX}, V_{th} is the threshold voltage, v_{GS} is gate-to-source voltage, and V_B is the dc bias voltage of the current squaring circuit and equal to $(v_{GS,MSQ_1} + v_{GS,MSQ_2})$. From (7) and (8), the drain currents i_1 and i_3 of M_{SQ_1} and M_{SQ_3}, respectively, can be calculated. Since $i_1 = i_2$, the output current i_{OUT} can be written as

$$i_{OUT} = i_1 + i_3 = I_B + \frac{i_{in}^2}{4I_B}, \tag{9}$$

where

$$I_B = \frac{1}{4} k_n \frac{W}{L}(V_B - 2V_{th})^2. \tag{10}$$

Suppose the input current i_{in} of the current squaring circuit equals $(I_{RF}\cos\omega_{RF}t + I_{LO}\cos\omega_{LO}t)$, the output current signal of the current squaring circuit from (9) can be expressed as

$$\begin{aligned} i_{OUT}(t) = &\left(I_B + \frac{I_{RF}^2 + I_{LO}^2}{8I_B}\right) \\ &+ \frac{1}{8I_B}\left(I_{RF}^2\cos 2\omega_{RF}t + I_{LO}^2\cos 2\omega_{LO}t\right) \\ &+ \frac{I_{RF}I_{LO}}{4I_B}[\cos(\omega_{RF}+\omega_{LO})t + \cos(\omega_{RF}-\omega_{LO})t]. \end{aligned} \tag{11}$$

From the last term in (11), the double sideband mixing is achieved and the RF signal at the frequency ω_{RF} is mixed with the LO signal at the frequency of ω_{LO}. The signal at ω_{RF} is converted into the signals at $(\omega_{RF}+\omega_{LO})$ and at $(\omega_{RF}-\omega_{LO})$. The ω_{IF} in this design is set to $(\omega_{RF}-\omega_{LO})$. The current conversion gain of the current squaring circuit can be defined as

$$\begin{aligned} \text{Currnet conversion gain} &= \frac{i_{OUT}|_{\omega=(\omega_{RF}-\omega_{LO})}}{i_{RF}} = \frac{I_{LO}}{4I_B} \\ &= \frac{I_{LO}}{k_n \frac{W}{L}(V_B - 2V_{th})^2}. \end{aligned} \tag{12}$$

From (12), the current conversion gain can be controlled by the magnitude of LO signal and the biasing voltage V_B.

The load of the current squaring circuit can be designed by a LC tank which is resonated at IF and serves as a BPF. Because of its bandpass characteristics, both harmonic and inter-modulation components with frequencies far away

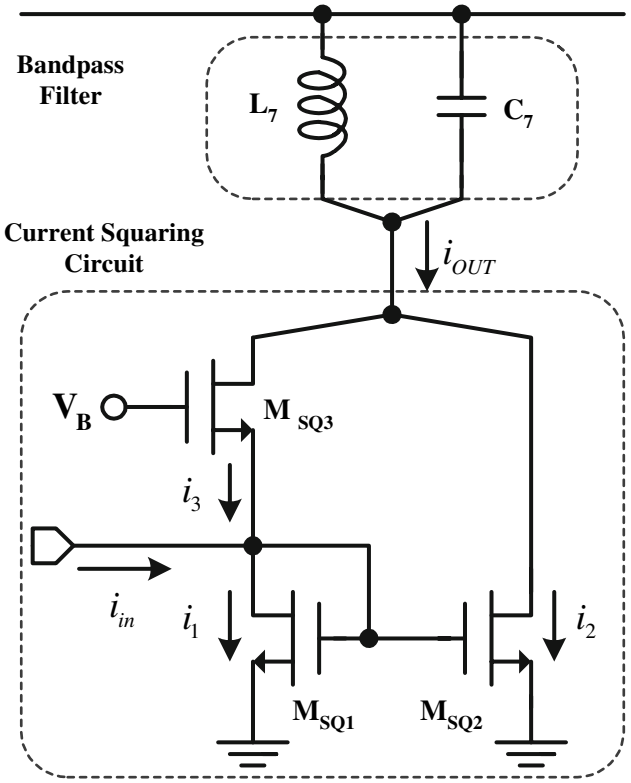

Fig. 8 Circuit diagram of the current squaring circuit and bandpass filter

from the IF can be suppressed. Only the IF signal can be selected and sent to the output.

With the advanced of the CMOS technology, the device current is not of the square characteristic. Due to the short-channel effect, the relation among drain current i_{DS}, overdrive voltage v_{OV} and drain to source voltage v_{DS} can be written as

$$i_{DS} = \frac{1}{2}k\frac{W}{L}(v_{OV})^m(1+\lambda v_{DS}), \tag{13}$$

where $1 \le m < 2$, $v_{OV} = v_{GS} - V_{th}$, and the coefficient λ models the effect of the channel length modulation which is related to v_{DS}. Besides, the parameter m is roughly equal 2 if the overdrive voltage of the MOS is small. Because the drain to source voltage v_{DS} between M_{SQ_1} and M_{SQ_3} are not exactly the same when the biasing voltage V_B is slightly varied, the channel-length modulation effect should be considered as in (13).

Because V_B is usually designed a little higher than two times threshold voltage of M_{SQ_1} and M_{SQ_3} from the consideration of the current conversion gain as shown in (12), the overdrive voltage voltages of both M_{SQ_1} and M_{SQ_3} are not high. Consequently, the coefficient m in (13) can be approximated as 2. If $\delta = (v_{DS,MSQ_3} - v_{DS,MSQ_1})/2$ and $\sigma = (v_{DS,MSQ_3} + v_{DS,MSQ_1})/2$ is assumed, the expression i_{OUT} in (9) can be modified as

$$i_{OUT} = i_{in}^2\frac{(1-\chi)}{4I_B} + i_{in}(V_B - 2V_{th})^2 \times \frac{\lambda}{(1+\lambda\sigma)^2}\cdot\left\{\begin{array}{l}\frac{\delta}{2I_B} + \left[\sigma + \lambda\sigma^2 - \delta\frac{\left(2+2\lambda\sigma-27\lambda^2\sigma^2\right)}{(2+3\lambda\sigma)}\right] \\ -\delta\lambda\sigma\left[\frac{\left(3+10\lambda\sigma+11\lambda^2\sigma^2+4\lambda^3\sigma^3\right)}{(2+3\lambda\sigma)}\right]\end{array}\right\} + I_B\left[\frac{(1+2\lambda\sigma+2\delta\lambda)(2+3\lambda\sigma)^2}{2(2+3\lambda\sigma)(1+\lambda\sigma)^2+2\lambda\left(3\delta+7\delta\lambda\sigma+4\lambda^2\sigma^2\right)}\right], \tag{14}$$

where

$$\chi = \frac{\lambda}{2(1+\lambda\sigma)^4}\cdot\left[\sigma(1+\lambda\sigma)^2(1+2\lambda\sigma) - \delta(1-\lambda\sigma)\right]. \tag{15}$$

If the effect of channel length modulation effect is neglected as $\lambda = 0$, χ is equal 0 and (14) can be simplified to (9). The factor of the i_{in}^2 in (14) reveals that the conversion gain of the squaring circuit with the channel-length modulation becomes $(1-\chi)$ times smaller than that without channel-length modulation.

Moreover, even if the drain to source voltage differences of M_{SQ_1} and M_{SQ_3} are the same, we have $\delta = 0$. But the channel length modulation effect makes the coefficient χ not equal 0. In this case, (14) can be simplified to

$$i_{OUT} = i_{in}^2\frac{(1-\gamma)}{4I_B} + i_{in}(V_B - 2V_{th})^2\left(\frac{\lambda\sigma}{1+\lambda\sigma}\right) + \frac{I_B}{2}\left[\frac{(1+2\lambda\sigma)(2+3\lambda\sigma)^2}{(2+3\lambda\sigma)(1+\lambda\sigma)^2+4\lambda^3\sigma^2}\right], \tag{16}$$

where

$$\gamma = \frac{\lambda\sigma(1+2\lambda\sigma)}{2(1+\lambda\sigma)^2}. \tag{17}$$

From the above derivations, channel length modulation effect degrades the conversion gain of the current squaring circuit which is $(1-\chi)$ smaller in (14) or $(1-\gamma)$ smaller in (16). Besides, this effect also results in the leakage of the fundamental signal of LO and RF signals. The simulation results in Fig. 9 show that the conversion gain approaches maximum when the biasing voltage V_B equals V_{DD} which is 1.2 V in this design. Meanwhile, the minimum value of drain to source voltage difference of M_{SQ_1} and M_{SQ_3} can be achieved under this condition.

2.2.2 *Current summing circuit*

Figure 10 shows the current summing circuit. Two common-gate transistors M_9 and M_{10} operated in the saturation region function as current buffers. The bulks of M_9 and M_{10} are connected to ground. Although M_9 and M_{10} suffer from the body effect resulting in slightly increase of their threshold voltage, the isolation among the input port of RF, the input port of LO, and the output port can be improved. Besides, the voltage headroom of this circuit is sufficient because the inductor L_4 is tied to V_{DD} and L_5–L_6 are tied to

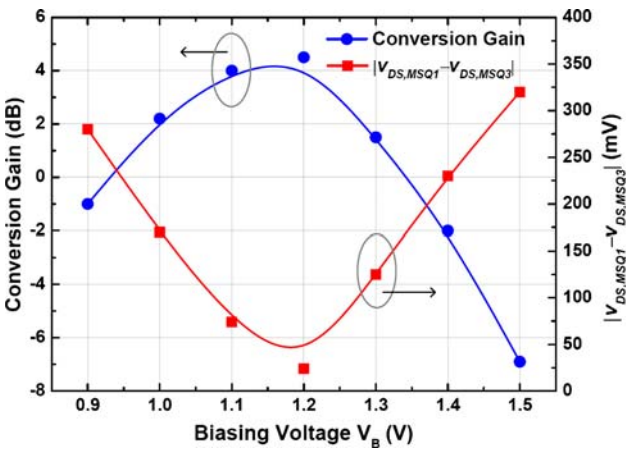

Fig. 9 Simulated conversion gain and $|v_{DS,MSQ_1} - v_{DS,MSQ_3}|$ versus V_B.

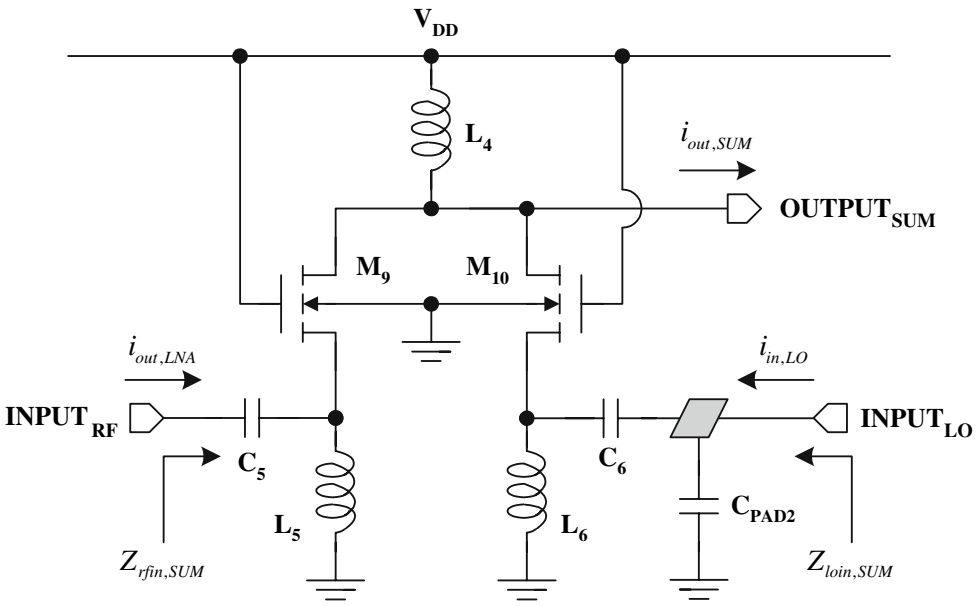

Fig. 10 Circuit diagram of the current summing circuit

ground. This current summing circuit can be operated at very low supply voltage.

Due to the advantage of current-mode signal processing, the current signals $i_{\mathrm{out,LNA}}$ from LNA circuit and $i_{\mathrm{in,LO}}$ from off-chip LO signal generator are summed by connecting the drains of M_9 and M_{10} together. L_4 is designed to provide high impedance at the output so that the summed current signal $(i_{\mathrm{out,LNA}} + i_{\mathrm{in,LO}})$ can be fed into the following current squaring circuit. C_5 is the dc blocking capacitor to prevent from disturbing the biasing point of the LNA. At the frequency of RF, L_5 is resonated with the parasitic gate-to-source capacitance $C_{\mathrm{GS},M9}$ of M_9 and source-to-bulk capacitance C_{SB,M_9} of M_9 to provide high impedance to ac ground so that the input RF current signal from the LNA circuit can flow into M_9. L_6, C_6 and C_{PAD2} form the matching network for LO input port. The parasitic gate-to-source capacitance $C_{\mathrm{GS},M_{10}}$ of M_{10} and source-to-bulk capacitance $C_{\mathrm{SB},M_{10}}$ of M_{10} are also considered in this matching network.

2.3 Current-mode receiver front-end

The detailed connections of the current-mode receiver front-end circuits under a single supply voltage of V_{DD} are shown in Fig. 11. The circuits include a two-stage current-mode LNA of low-voltage version, a current summing circuit, and a current squaring circuit. The input signal at ω_{RF} is firstly amplified by LNA, and then is mixed with the LO signal at ω_{LO} by the current-mode mixer formed by a current summing circuit and a current squaring circuit. The down-converted signal at ω_{IF} is finally sent to output buffer which is a current-mirror amplifier formed by M_{14}, M_{15}, and L_8. The output matching network is designed by L_8, C_9, and C_{PAD3} so that the output impedance of the measuring buffer equals 50 Ω and the maximum power transfer can be achieved. Table 2 shows the design parameters of the two-stage current-mode LNA of low-voltage version. Table 3 shows the design parameters of current-mode down-conversion mixer and output buffer.

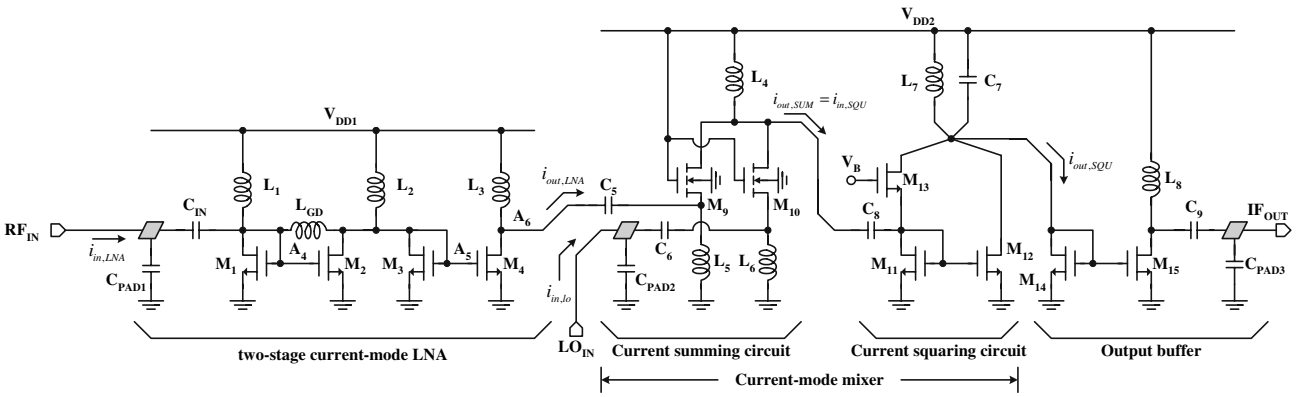

Fig. 11 Detailed connections of the 24-GHz current-mode receiver front-end with output buffer

Table 2 Device parameters of 24-GHz CMOS LNA

Current-mode LNA of low-voltage version		
M_1	$L = 0.13$ μm	$W = 1.2$ μm
M_2	$L = 0.13$ μm	$W = 52.8$ μm
M_3	$L = 0.13$ μm	$W = 1.2$ μm
M_4	$L = 0.13$ μm	$W = 31.2$ μm
C_{PAD1}	20 fF	
C_{IN}	89 fF	
L_{GD}	506 pH	Rad = 32.5 μm, $w = 3$ μm, nr = 3
L_1	298 pH	Rad = 15 μm, $w = 9$ μm, nr = 1.5
L_2	315 pH	Rad = 15 m, $w = 3$ μm, nr = 1.5
L_3	315 pH	Rad = 15 m, $w = 3$ μm, nr = 1.5

In this work, the RF input frequency is set at 24 GHz, the LO frequency is set at 19 GHz, and accordingly the IF output frequency is at 5 GHz. The image frequency is at 14 GHz. According to Fig. 4, the image rejection of the proposed receiver front-end is more than 30 dB before the first down-conversion mixer due to the large IF frequency of 5 GHz is selected. This performance is achieved due to the multistage nature of bandpass LNA. If much higher image rejection is required, the off-chip band-select filter before the LNA can be used to enhance the performance of image rejection.

Table 3 Device parameters of 24-GHz CMOS down-conversion mixer and output buffer

Current-mode down-conversion mixer		
Current summing circuit		
M_9	$L = 0.13$ μm	$W = 38.4$ μm
M_{10}	$L = 0.13$ μm	$W = 38.4$ μm
C_{CPAD2}	20 fF	
C_5	63 fF	
C_6	274 fF	
L_4	443 pH	Rad = 27 μm, $w = 3$ μm, nr = 1.5
L_5	945 pH	Rad = 20 m, $w = 3$ μm, nr = 3.25
L_6	916 pH	Rad = 26 μm, $w = 3$ μm, nr = 2.75
Current squaring circuit		
M_{11}	$L = 0.13$ μm	$W = 14.4$ μm
M_{12}	$L = 0.13$ μm	$W = 14.4$ μm
M_{13}	$L = 0.13$ μm	$W = 14.4$ μm
L_7	884 pH	Rad = 15.5 μm, $w = 3$ μm, nr = 3.5
C_7	1 pF	
C_8	132 fF	
Output buffer		
M_{14}	$L = 0.13$ μm	$W = 1.2$ μm
M_{15}	$L = 0.13$ μm	$W = 150$ μm
L_8	1.69 nH	Rad = 20 μm, $w = 3$ μm, nr = 4.5
C_9	583 fF	
C_{PAD3}	20 fF	

For testing consideration, the three ports are also designed to match with 50 Ω. If multiple power supplies can be used in the receiver front-end, the simulated power consumption of the current-mode receiver is 29.94 mW where the two-stage current-mode LNA of low-voltage version drains 20.4 mA from the supply voltage of 0.8 V, and the current summing circuit and current squaring circuit drain 8.8 and 2.55 mA, respectively, from the supply voltage of 1.2 V. Under this condition, the two-tone analyses by HB simulation with two RF input signals at 23.95 and 24.05 GHz and the LO signal at 19 GHz with the power level of −3 dBm are depicted in Fig. 12. It reveals that the receiver has a simulated conversion gain of 21.5 dB, a $P_{-1\,dB,RX}$ of −29 dBm, and a $P_{IIP3,RX}$ of −18.2 dBm. The simulated total NF is 4.2 dB with the RF at 24 GHz and LO at 19 GHz.

Moreover, if the receiver front-end is restricted to use single power supply, it consumes 55.4 mW from the supply voltage of 1.2 V. The excess power consumption is from the LNA because higher voltage is adopted to bias the LNA of the low-voltage version, and the LNA drains 34.82 mA from the supply voltage of 1.2 V.

The use of multiple supply voltage of 0.8 and 1.2 V complicates the design. In this design, the supply voltages are from different off-chip power supplies. Therefore, the smaller supply voltage can be easily supported. If the receiver is restricted to use a single supply voltage of 1.2 V, the LNA is recommended to use the circuit in Fig. 2(a) where M_6−M_8 provide a simple way to have the voltage drop of around 400 mV for the LNA such that the voltages of A_1−A_3 are around 0.8 V and M_1−M_4 can be well biased.

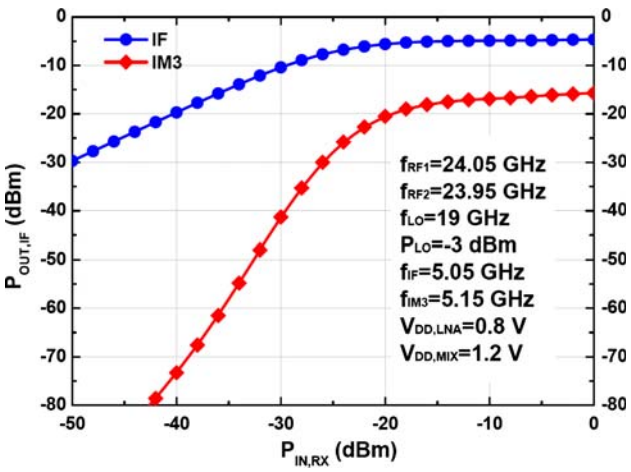

Fig. 12 Simulated linearity performance of the 24-GHz current-mode receiver by two-tone HB analyses

3 Experimental results

The designed 24-GHz current-mode receiver front-end circuit was fabricated in 0.13-μm 1P8M CMOS technology. The top metal of this process is with the thickness of 3.35 μm. The equivalent relative dielectric constant ε_{eff} is about 4.2. Based on the technology information of the backend process, the electromagnetic (EM) tool HFSS is used to evaluate and extract the characteristics of the on-chip octagonal spiral inductors and the interconnections within the circuits.

The floor plans of the proposed receiver front-end are depicted in Fig. 13. Nine on-chip octagonal spiral inductors are used. The distances of each inductor are more than 100 μm to mitigate the magnetic coupling between on-chip inductors. In addition, the distances of the active devices of current-mode LNA, current summing circuit, current-squaring circuit and output buffer are arranged far, the noise influence between these circuits are kept small. The signal path between input pad and the input of the LNA is drawn as short as possible to avoid additional signal losses and increase of NF. Besides, large on-chip decoupling capacitors are used between the biases and ground, such that high frequency noises can be bypassed to ground and consequently stable biases and supplies of the receiver can be achieved. All dc pads are protected by ESD diodes to enhance the reliability of the proposed receiver. The performance of each circuit block in this 24-GHz current-mode receiver is over-designed to overcome process variations. This chip occupies the active region of 1.45×0.72 mm^2 including testing pads.

The measurement setups of this fabricated receiver are described as follows. The on-wafer probing measurement is adopted to verify the performance of the receiver front-end. Three GSG RF probes with the pitch of 150 μm and a 6-pin dc probe with the pitch of 150 μm are applied to probe the testing pads. The *S* parameters are measured to analyze both the input and output matching characteristics by the network analyzer, Agilent E8364B, which can characterize the *S*-parameter performance from 10 MHz to 50 GHz. To measure conversion gain and linearity, three signal generators Agilent E8257D are used to provide two RF and one LO signals for the device under test (DUT). The spectrum analyzer Agilent E4448A is used to monitor the spectrum to verify the linearity and conversion gain of the receiver. The NF analyzer Agilent N8975A with a broadband noise source HP 346C is used to measure the performance of NF of the receiver.

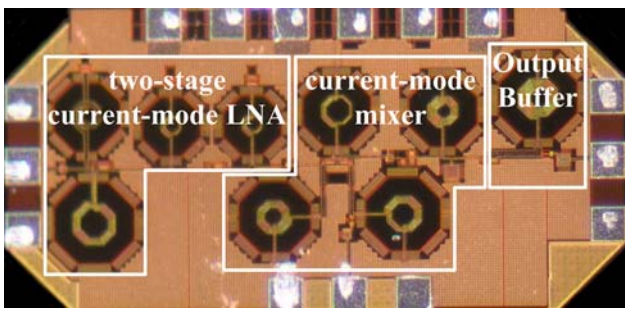

Fig. 13 Chip micrograph of the fabricated current-mode receiver front-end

Owing to the layout mistake of the fabricated chip, the focused ion beam (FIB) post-process is used to modify the metal connections of the current-mode LNA. The FIB metal lines connect the LNA circuit to the power supply. Under the condition that multiple power supplies can be used so that the power supply of LNA is 0.8 V and the power supply of the current-mode mixer is 1.2 V, the measured total power consumption is 27.8 mW. Moreover, if the single power supply of 1.2 V is applied to the receiver front-end, the measured power dissipation is increased to about 49.8 mW. The reason why the increase in measured power dissipation from 27.8 mW for the multiple supply voltages to 49.8 mW for the single supply voltage is the supply voltage of LNA is increased from 0.8 to 1.2 V. This results in increasing more overdrive voltage of 400 mV of the LNA, and consequently the measured power dissipation of LNA itself is increased. The measured current consumption of the LNA is 19.45 mA from the supply voltage of 0.8 V and is 31.3 mA from the supply voltage of 1.2 V.

Figure 14 presents the measured and revise-simulated conversion gain versus RF input frequency. The losses from cables, probes and adaptors are compensated. Moreover, the parasitic resistances resulting from FIB post-process are considered in the revise-simulated results. The tested RF input power is −30 dBm. The LO is set to the frequency which is 5 GHz lower than the RF, $f_{\text{LO}} = f_{\text{RF}} - 5$ GHz, and the tested LO input power is −3 dBm. The output is observed at the fixed IF frequency of 5 GHz. The measured conversion gain of the RF frequency at 24 GHz is 11.3 dB under the condition that the power supplies of the LNA and Mixer are 0.8 and 1.2 V, respectively. In addition, the conversion gain is 12 dB under the condition that the power supply of both LNA and Mixer is 1.2 V. Because the parasitic resistances from FIB post-process are in series with the inductive loads of the current-mode LNA, the quality factor of the loads of the LNA is decreased. This makes the gain of the LNA decrease, and consequently the conversion gain of the receiver is decreased.

The two-tone test results are shown in Fig. 15. Two RF inputs with 100 MHz frequency spacing are at the frequency of 24.05 and 23.95 GHz and the LO is at 19 GHz with the power of −3 dBm. Because of the conversion gain

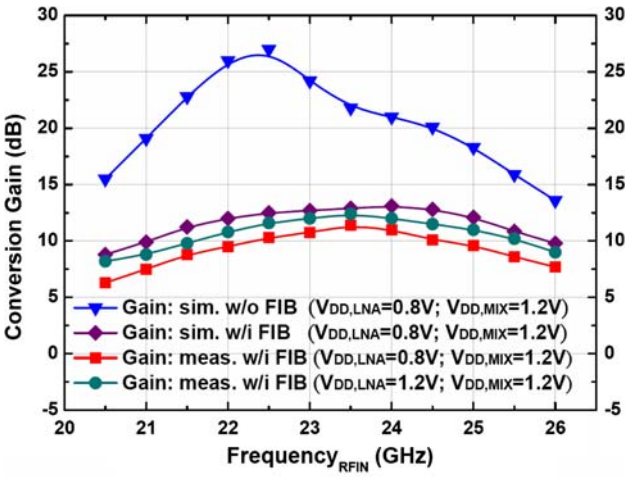

Fig. 14 The measured and simulated conversion gain of the receiver versus RF input frequency

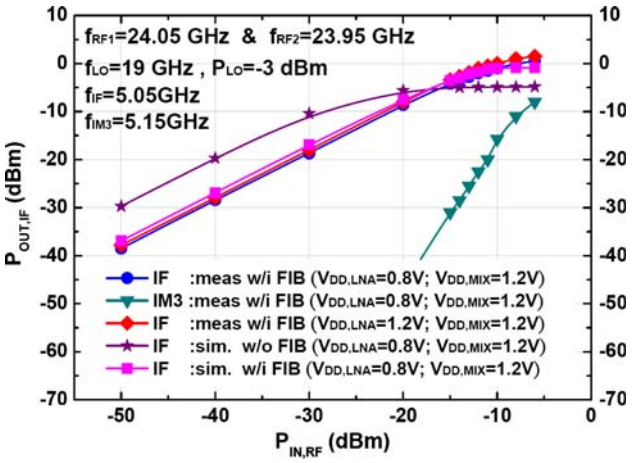

Fig. 15 The measured linearity performance of the receiver by two-tone testing

reduction of the receiver, the measured $P_{-1\,\mathrm{dB}}$ and P_{IIP3} are raised to −13.5 dBm and −1 dBm, respectively, under the condition that the power supplies of LNA and Mixer are 0.8 and 1.2 V, respectively. Besides, the measured $P_{-1\,\mathrm{dB}}$ and P_{IIP3} are about −12 and −1.5 dBm, respectively, under the condition that the single power supply of 1.2 V for LNA and mixer is adopted. At the RF frequency of 24 GHz and the LO frequency of 19 GHz, the measured total NF of the receiver is 14.2 and 13.3 dB if the power supply of LNA is 0.8 and 1.2 V, respectively.

Table 4 summaries the performance of the proposed current-mode receiver front-end. In addition, some comparison results of published 24-GHz receiver front-end circuits are also provided. Compared to the works published in [2] and [5], the proposed 24-GHz CMOS current-mode receiver front-end has the advantage of smaller power dissipations and can be operated in low supply voltage. This current-mode receiver front-end also has better linearity performance.

The layout mistake has been corrected and the modified design is under fabrication now. Therefore, the new test results are unavailable at present.

4 Conclusion

In this work, the current-mode design techniques of CMOS RF circuits are developed and are applied to realize the first 24-GHz CMOS current-mode receiver front-end. The receiver integrated with a current-mode LNA and a

Table 4 The measured performances and comparisons results of published 24-GHz receiver front-end circuits

	This work		[2]	[5]
Technology	0.13 μm CMOS		0.18 μm CMOS	0.8 pm SiGe HBT f_T = 80 GHz
Receiver architecture	Direct-conversion (2-stage LNA + Mixer)		Direct-conversion (3-stage LNA + single-balanced Gilbert Mixer)	Direct-conversion (3-stage differential LNA + *I*/*Q* differential Gilbert Mixer)
Topology	Current mode		Voltage mode	Voltage mode
$\mathrm{Freq_{RF}}$ (GHz)	24		21.8	24.1
$\mathrm{Freq_{LO}}$ (GHz)	19		16.9	23.9
$\mathrm{Freq_{IF}}$ (GHz)	5		4.9	0.2
$\mathrm{Gain_{RX}}$ (dB)	12	11.3	27.5	31
$\mathrm{NF_{RX}}$ (dB)	13.3	14.2	7.7	8.8
$\mathrm{P_{IIP3,\ RX}}$ (dBm)	−1.5	−1	–	–
$\mathrm{P_{1\ dB,\ RX}}$ (dBm)	−12	−13.5	−23	−27
Power (mW)	49.8	27.8	64.5	640
Supply (V)	1.2	0.8/1.2	1.5	4
Chip area ($\mathrm{mm^2}$)	1.45 × 0.72		0.4 × 0.5	1.48 × 1.15

current-mode down-conversion mixer is designed, fabricated in 0.13-μm CMOS technology and measured. Two-stage current-mirror amplifiers cascaded are used to realize the current-mode LNA. The LNA has the capability of low voltage operation. The current summing circuit and current squaring circuits are adopted to perform the mixing of the current signals. The measured results demonstrate that the proposed current-mode receiver front-end can operate well in the 24-GHz frequency band. Although the receiver does not achieve the expected performance because of the layout mistake, after the FIB post-process to remedy for the layout mistake, the designed 24-GHz CMOS current-mode receiver front-end still can exhibit the conversion gain of 11.3 dB, the NF of 14.2 dB, and the P_{IIP3} of -1 dBm under the condition that power supply of the current-mode LNA is 0.8 V and the power supply of the current-mode mixer is 1.2 V. The total power dissipation of the current-mode receiver front-end under this condition is 27.8 mW. The current-mode design techniques have the capability of designing low-voltage RF circuits in the advanced nanometer CMOS technologies. Future research on the applications of short range automotive radar systems or point-to-point wireless communication systems will be explored and discussed by the proposed current-mode approaches.

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