國 立 交 通 大 學

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博 士 論 文

以二氧化鉿為基底之高介電常數閘極介電層中的電荷捕捉與逃逸之電特性分析

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中華民國 九十五 年 十一 月

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摘要

本論文主要探討的是，以二氧化鉿為基底之高介電常數閘極介電層中的電荷捕捉與逃逸之各種不同的電特性分析。與傳統的二氧化矽(SiO_2)或氮氧化矽(SiON)閘極氧化層不同的是，以二氧化鉿為基底之高介電常數閘極介電層具有相當嚴重的可靠度問題—臨界電壓的不穩定性，起因於早已存在的主體缺陷中的快速與緩慢的電荷捕捉與逃逸現象，特別是對於處在矽基底電子注射狀態下的 N 型金氧半場效電晶體而言。我們發現，在偏壓高溫不穩定性(bias-temperature instability, BTI)應力測試的應力/量測循環之中，這些被捕捉的電荷載子將導致半導體元件中臨界電壓的偏移、汲極電流的衰減，以及通道載子移動率的變異；而且能夠被偵測到的被捕捉電荷載子數目與切換和量測的時間延遲長短有著相當密切的關係，這是因為一旦閘極應力偏壓被移開的時候，將導致快速的瞬間電荷逃逸現象發生。因此，我們必須使用適當的電特性分析方法，以瞭解在以二氧化鉿為基底的高介電常數閘極介電層中之快速與緩慢的電荷捕捉與逃逸現象的物理機制，以及這些現象對於效能評估所造成的衝擊，無論是在個別元件或整體電路的層級而言。

第一章簡介了一般性的背景知識與研究動機，並從材料與電特性等方面來說

明為什麼我們要用以二氧化鉿為基底的高介電常數閘極介電層來取代傳統的二氧化矽閘極氧化層。接著說明因電荷捕捉與逃逸現象所造成的臨界電壓不穩定性，此一議題已被廣泛認定是高介電常數閘極介電層中嚴苛的可靠度問題之一，其中包含了快速與緩慢的高介電常數閘極介電層缺陷。最後，簡單說明本論文的組織架構，以提供此一學術研究之綱要概述。

第二章描述了在正偏壓高溫不穩定性(positive bias temperature instability, PBTI)應力測試下，N 型金氧半場效電晶體中之鉿矽酸鹽(HfSiO)/二氧化矽(SiO_2)高介電常數雙層閘極堆疊的臨界電壓不穩定性。我們廣泛探討了在正偏壓高溫不穩定性應力測試下的各項基本元件特性的劣化行為以及電荷捕捉時的載子傳輸機制，並採用一具有離散捕捉時間常數的電荷捕捉物理模型(延伸的指數成長模型)來描述並預測此一電荷捕捉行為。此外，我們也一併探討了應力測試電壓、溫度，以及閘極堆疊結構對於電荷捕捉行為的相關性，以瞭解在鉿矽酸鹽/二氧化矽高介電常數雙層閘極堆疊中之電荷捕捉的物理特性。第三章描述了處在靜態與動態正偏壓應力測試下，二氧化鉿(HfO_2)/二氧化矽(SiO_2)高介電常數雙層閘極堆疊中的電荷捕捉與逃逸行為。我們發現，如果反向的復甦偏壓強到足以將之前捕捉的電荷載子清除乾淨的話，相似的電荷捕捉與逃逸行為將不斷地重覆出現在連續施加的靜態應力/復甦循環之中。根據這些發現，我們可以推論，這些高介電常數介電層缺陷應是早已存在於二氧化鉿高介電常數介電層中的主體缺陷，而且在這些應力測試循環之中應該沒有新的高介電常數介電層缺陷產生。接著，我們驗證了，假使逃逸的電荷載子數目遠小於注入的總電荷載子數目，靜態與動態的正偏壓應力測試將呈現相似的電荷捕捉基本特性。此外，我們可以藉由改變在特定頻率下之應力脈衝波形的責任週期大小，來觀察及分析動態正偏壓應力測試下的瞬間充電行

為，並證實一以有效應力時間為參數的通用電荷捕捉模型。

第四章說明了一採用五元素電路模型的雙頻電容—電壓校正方法，此方法可廣泛應用於高介電常數閘極介電層與超薄氧化層。此一通用的五元素電路模型同時考量了靜態與動態的介電層能量損耗，以及半導體電容常有的寄生元件，譬如來自於基底/井區的串聯電阻與來自於傳輸線/量測系統的串聯電感。再者，這一個五元素電路模型可依據閘極漏電流之大小，轉變為其他兩種不同的四元素電路模型，以簡化其計算與分析。我們發現，使用此一雙頻電容—電壓校正方法，可有效修正低漏電之高介電常數閘極介電層中的箝制與擴大電容—電壓圖形，並可解釋各寄生元件的面積效應及其物理起源。此外，此一雙頻電容—電壓校正方法亦可有效抑制超薄氧化層中因量子穿隧漏電流而引起的嚴重電容值墜落現象，並可另外搭配適當的電容—電壓模擬軟體(已考慮多晶矽空乏效應與量子效應)，以求取超薄氧化層的等效氧化層厚度。第五章闡釋了如何使用低頻電容—電壓量測方法，來決定在二氧化鉿/二氧化矽高介電常數雙層閘極堆疊中的邊界缺陷之空間與能階分佈。邊界缺陷，在此代表的是那些能夠被偵測到的快速高介電常數介電層缺陷，一般都座落在高介電常數介電層/二氧化矽氧化層的介面附近，而這些邊界缺陷能夠和底部的矽基板經由量子直接穿隧效應作即時的電荷載子交換。我們發現，假使這些邊界缺陷的瞬間充電與放電行為能夠跟得上電容量測的小訊號頻率，則在低頻所量測到之增加的電容值大小，可視為一與理想介電層電容值並聯的邊界缺陷電容值。如同物理模型所預測的，此一邊界缺陷電容值已被證實與待測元件的閘極面積成線性相關，而且此一邊界缺陷電容值的大小也與鉿矽酸鹽薄膜中的矽成分高低有著相當密切的關係。此外，此一邊界缺陷電容值與量測頻率和閘極偏壓之間的關係式，也可經由適當的轉換，成為自矽基底表面的穿隧距離

和自二氧化鉿導帶邊緣的缺陷能階深度。以一穿透梯形位能障礙的彈性直接穿隧物理模型為理論基礎，我們能夠藉由一平滑的三維網線，來描述在二氧化鉿/二氧化矽高介電常數雙層閘極堆疊中的邊界缺陷之空間與能階分佈。此外，根據這些物理模型萃取的結果，我們可以推論絕大部分、早已存在的高介電常數介電層缺陷均分佈在二氧化鉿的主體介電層之中，而且有相當可觀的部分是座落在低能階之位置。

第六章闡明了如何使用低頻電荷泵浦(charge pumping)方法，來分析在二氧化鉿/二氧化矽高介電常數雙層閘極堆疊中的邊界缺陷之瞬間充電與放電行為。如同在低頻電容—電壓圖形中的邊界缺陷電容值一般，在低頻電荷泵浦方法中所量測到的額外每單位循環再結合電荷載子數目，皆可歸因於反覆的多數與少數載子再結合，而此一現象主要發生於高介電常數介電層/二氧化矽氧化層介面附近的邊界缺陷。藉由改變輸入脈衝波形的上升/下降時間、峰值與基值水平電壓，以及責任週期，我們可以對邊界缺陷之瞬間充電與放電行為的穿隧路徑及物理機制有更深入的瞭解，我們並發現瞬間充電與放電現象可能發生在僅僅 50 至 100 奈秒之間。以一具有對稱的前向與反向穿隧時間常數之彈性直接穿隧物理模型為理論基礎，我們同樣能夠得到邊界缺陷的空間與能階分佈，並以一平滑的三維網線來作描述。同時，我們比較了低頻電容—電壓量測與低頻電荷泵浦這兩種適用於邊界缺陷的分析方法，並對邊界缺陷的空間與能階分佈得到一致的結論。

最後，第七章總結本論文的各項發現與貢獻，並指出本論文中尚未被清楚理解或尚未有強烈證據支持的研究主題。這些延伸的研究主題能夠幫助我們指引出未來的技術發展方向，並值得投入大量的研究活動去深入探討。

Electrical Characterization of Charge Trapping and De-trapping in Hf-Based High-k Gate Dielectrics

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ABSTRACT

This dissertation studies the charge trapping and de-trapping in Hf-based high-k gate dielectrics through various electrical characterizations. Unlike the conventional SiO_2 or SiON gate oxides, Hf-based high-k gate dielectrics are known to suffer from the serious reliability concern of threshold voltage instability due to the fast and slow charge trapping and de-trapping in the pre-existing bulk traps in Hf-based high-k gate dielectrics, especially under the substrate electron injection conditions in high-k nMOSFETs. These trapped charge carriers are believed to cause the threshold voltage shift, drain current degradation, and channel mobility variation during the stress/measure cycles of bias temperature instability (BTI) stress, and the number of trapped charge carriers which can be detected depends greatly on the switching and measurement time delays due to fast transient charge de-trapping when the stress bias voltage is removed. Therefore, appropriate electrical characterization methods should be employed to understand the physical mechanisms of fast and slow charge trapping and de-trapping in Hf-based high-k gate dielectrics and their impacts on the performance evaluation whether in the device or circuit level.

Chapter 1 introduces the general background and motivations about why should we use the Hf-based high-k gate dielectrics to replace the conventional SiO_2 gate oxides in

terms of the electrical and material properties. The threshold voltage instability induced by charge trapping and de-trapping has been identified as one of the most critical reliability issues in Hf-based high-k gate dielectrics, including the charge trapping and de-trapping in fast and slow high-k traps. Moreover, the organization of this dissertation will be briefly described and explained to give the outline of this academic study.

Chapter 2 describes the threshold voltage instability in nMOSFETs with dual- layer HfSiO/ SiO_2 high-k gate stack under static positive bias temperature instability (PBTI) stress. The fundamental characteristics and carrier transport mechanism of charge trapping under static PBTI stress are investigated extensively, and a physical model of charge trapping with dispersive capture time constants (stretched exponential growth model) has been employed to describe and to predict the charge trapping behavior. In addition, the dependences of stress voltage, temperature, and gate stack structure are studied to further understand the physical nature of charge trapping process in the dual-layer HfSiO/SiO_2 high-k gate stack. Chapter 3 depicts the charge trapping and de-trapping behaviors in the dual-layer HfO_2/SiO_2 high-k gate stack under static and dynamic positive bias stress. Similar charge trapping and de-trapping behaviors could be observed and repeated during the consecutive static stress/recovery cycles if the recovery bias voltage is strong enough to clean up the previously trapped charge carriers. Based on these findings, we may conclude that these high-k traps are the pre-existing bulk traps in the HfO_2 high-k dielectric and that no additional high-k traps are generated during the stress cycles. Then the fundamental characteristics of charge trapping under dynamic positive bias stress has been demonstrated to be identical with those under static positive bias stress if the de-trapped charge carriers could be neglected as compared to the total injected charge carriers. The transient charging behavior under dynamic positive bias stress could be observed and analyzed by varying

the duty cycles of stress pulse waveform at a specific frequency, and a universal charge trapping model has been proved in terms of the effective stress time.

Chapter 4 explains the two-frequency capacitance-voltage (C-V) correction method using a five-element circuit model for high-k gate dielectrics and ultrathin oxides. This general circuit model of five elements considers both the static and dynamic dielectric energy losses and parasitic components such as the substrate/well resistance and cable/system inductance, and this five-element circuit model could be modified as another two four-element circuit models to simply the calculations, depending on the gate leakage current. The clamped and amplified C-V curves of low-leakage high-k gate dielectrics could be effectively eliminated by using this two-frequency C-V correction method, and the area dependence and physical origin of parasitic components have also been clarified in detail. Also, the severe capacitance drop in the C-V curves of ultrathin oxides could be effectively suppressed and then simulated to obtain the equivalent oxide thickness (EOT) of ultrathin oxides by using the C-V simulation program which has already taken the poly depletion and quantum size effects into account.

Chapter 5 illustrates the space and energy distribution of border traps in the dual-layer HfO_2/SiO_2 high-k gate stack by the low-frequency capacitance-voltage (C-V) measurements. Border traps here represent the detected fast high-k traps located near the high-k/oxide interface which can instantly exchange the charge carriers with the underlying Si substrate through direct tunneling. The capacitance increase at low frequencies could be regarded as the border trap capacitance which is in parallel with the ideal dielectric capacitance if the transient charging and discharging of these border traps could follow the small-signal measurement frequency immediately. Border trap capacitance has been proved to be linearly proportional to the gate area as expected and

highly associated with the Si composition in HfSiO films, and its frequency and gate bias voltage dependences could also be transformed into the relationships of the tunneling distance from Si substrate surface and the trap energy depth from HfO_2 conduction band edge. Based on a physical model of elastic direct tunneling through trapezoidal potential barriers, the space and energy distribution of border traps in the dual-layer HfO_2/SiO_2 high-k gate stack could be smoothly profiled as a 3D-mesh. According to the model-extracted results, we may conclude that most of the pre-existing high-k traps are located in the HfO_2 bulk layer and that considerable parts of these traps are positioned at the shallow energy levels.

Chapter 6 clarifies the transient charging and discharging of border traps in the dual-layer HfO_2/SiO_2 high-k gate stack by low-frequency charge pumping method. Similar to the border trap capacitance at low-frequency C-V curves, additional recombined charge per cycle at low-frequency charge pumping measurements could be attributed to the repetitive recombination of majority and minority carriers which instantly tunnel into and out of the border traps located near the high-k/oxide interface. The tunneling path and physical mechanism of transient charging and discharging behaviors of these border traps could be further understood by varying the rise time and fall time, peak and base level voltages, and duty cycles of input pulse waveform, and the transient charging and discharging behaviors may occur within only 50-100 ns. Based on an elastic direct tunneling model with symmetric forward and reverse tunneling time constants, the space and energy distribution of border traps could also be obtained as a smoothed 3D-mesh. A comparison of analysis results was made between the low-frequency C-V measurement and low-frequency charge pumping method, and identical conclusions were drawn from these two different methods.

Finally, chapter 7 summarizes the findings and contributions of this dissertation,

and also indicates the topics that have not yet been understood clearly nor verified with strong evidence supports. These topics could help us direct the development of future technologies and deserve to be studied with great activities.

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我把這本論文，獻給他們。

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Fig. 6-11 Space and energy distribution of border trap volume density ρ_{bt} in the dual-layer HfO_2/SiO_2 high-k gate stack. Symbols are model-extracted data points, and 3D-mesh is the smoothed surface profiling of these points.

Chapter 1: Introduction

1.1 Why Use Hf-Based High-k Gate Dielectrics

As the Moore's law continues to drive the continuous scaling of gate dielectric thickness, it is becoming increasingly clear that we are approaching the materials limit of conventional SiO_2-based ultrathin oxides. The aggressive scaling of CMOS device technology in recent years has reduced the equivalent oxide thickness (EOT) of silicon oxynitirde SiON below 2.0 nm, thus leading to the serious concerns of gate dielectric integrity, reliability issues, and stand-by power consumption. Moreover, the rapidly-increasing tunneling gate leakage current has been identified as one of the major challenges to fulfill the specific EOT requirements in sub-65nm technology nodes as projected by the international technology roadmap for semiconductors (ITRS) in Table 1-I [1.1].

In order to avoid the intolerable tunneling leakage and power consumption in the ultrathin oxides, high dielectric permittivity (high-k) gate dielectric has been proposed to offer thicker dielectric physical thickness while maintaining the same equivalent oxide thickness (EOT) in electrical properties [1.2]. An analysis method for predicting the scaling limits of different high-k gate dielectrics has been proposed by Yeo *et al.*, and the selection guidelines for appropriate alternative high-k gate dielectrics (Fig. 1-1) were provided in terms of three logic technology applications, including the high performance (HP), low operating power (LOP), and low stand-by power (LSTP) logic technologies [1.3]. Table 1-II shows the summarized material and electrical properties of various high-k gate dielectrics such as Si_3N_4, Al_2O_3, Ta_2O_5, La_2O_3, Gd_2O_3, Y_2O_3, HfO_2, ZrO_2, $SrTiO_3$, $HfSiO_4$, and $ZrSiO_4$ [1.4], and Fig. 1-2 illustrates the bandgap and band alignment of these high-k gate dielectrics with respect to Si [1.5]. The

dashed lines represent 1eV above/below the conduction/valence bands, which indicate the minimum barrier height for electrons and holes to reduce the gate leakage current. Fig. 1-3 shows the ternary phase transition diagrams for (a) Ta-Si-O, (b) Ti-Si-O, and (c) Zr-Si-O compounds [1.6]. As compared to the unstable Ta_2O_5 and TiO_2, ZrO_2 high-k dielectric is thermo-dynamically stable with SiO_2 and Si, and no phase separation would occur into the M_xO_y and M_xSi_y phases [1.7]. Thus, ZrO_2:SiO_2 and HfO_2:SiO_2 silicates within an appropriate composition range could be obtained with very low gate leakage current, moderate dielectric constant, and excellent thermal stability. Among these investigated high-k gate dielectrics, Hf-based high-k gate dielectrics (including HfO_2, HfSiO, and HfSiON) have been recognized as the most promising candidates due to their moderate dielectric constant (~20-25), large energy bandgap (~5.7-6.0 eV), high conduction band offset (~1.5-1.9 eV), excellent thermal stability on the Si substrate (~950°C), and stable amorphous crystalline structure by incorporating the Si or N atoms. However, it has been reported that there is plenty of pre-existing bulk traps in the HfO_2 high-k gate dielectrics, thus leading to the critical reliability issue of threshold voltage instability induced by charge trapping and de-trapping.

1.2 Threshold Voltage Instability in the Hf-Based High-k Gate Dielectrics

Unlike the conventional SiO_2 or SiON, there is a large number of pre-existing bulk traps in the Hf-based high-k gate dielectrics, and this is believed to be an intrinsic problem related to the specific properties or crystal structure of high-k gate dielectrics, regardless of the deposition technique or process conditions. Charge trapping in these pre-existing high-k bulk defects would cause the continued threshold

voltage shift and drain current degradation with the operation time, especially the fast electron trapping in high-k nMOSFETs. In general, a defect band filled with plenty of pre-existing bulk traps is assumed to be positioned just above the Si conduction band edge as shown in Fig. 1-4 [1.8]. As can be seen, the position of trapped charge carriers in the energy levels would change rapidly with the applied gate bias voltage due to the asymmetric band structures in SiO_2 and HfO_2. For positive gate bias, the pre-existing bulk traps in the HfO_2 layer would be charged by the injected electrons through the interfacial oxide. For negative gate bias, these trapped electrons would be discharged in the reverse direction into the Si conduction band. Moreover, these high-k bulk traps could be divided into the slow and fast traps, depending on their de-trapping time constants when the gate bias voltage is removed.

First, the hysteresis of Capacitance-voltage curves and the threshold voltage shift determined by static I_d-V_g characteristics have been widely used to study the slow high-k traps from which the trapped charge carriers could not de-trap immediately [1.9], [1.10]. Then, the pulse I_d-V_g technique and charge pumping method have been proposed and employed to investigate the fast high-k traps which could instantly capture and emit the charge carriers by tunneling through the thin interfacial oxide [1.8], [1.11]-[1.13]. The tunneling model through the thin interfacial oxide is similar to that of tunneling into near-interface oxide traps in the heavily-irradiated SiO_2 that has already been studied and proposed [1.14]-[1.19]. These near-interface oxide traps are defined as the oxide traps located near the interface that can instantly exchange charge carriers with the underlying Si substrate through direct tunneling [1.20], [1.21] and are suggested to be named as “border traps” to be distinguished from the conventional interface states and oxide traps [1.22]. Fig. 1-5 shows the schematic illustration of the interface states, fixed oxide traps, and border traps in terms of (a)

the spatial location of defects, and (b) their electrical response. Border traps are the near-interface oxide traps which can be detected within the time scale of electrical measurements being performed. Similarly, the detected fast high-k traps by the C-V measurement or charge pumping method at low frequencies could also be defined as the pre-existing high-k traps located near the high-k/SiO_2 interface that can instantly exchange charge carriers with the underlying Si substrate through direct tunneling, and are called the border traps in the high-k dielectrics to be distinguished from other fast high-k traps (which have not been detected, depending on the measurement frequency).

Compared to the negative bias temperature instability (NBTI) in ultrathin oxide pMOSFETs, threshold voltage instability induced by charge trapping and de-trapping is believed to be the limiting reliability factor in high-k devices. Therefore, this dissertation will concentrate on using various electrical characterization methods to better understand the fundamental characteristics and physical mechanism of charge trapping and de-trapping in Hf-based high-k gate dielectrics.

1.3 Dissertation Organization

The organization of this dissertation is briefly described below. Chapter 2 studies the characteristics and physical model of charge trapping in the pre-existing high-k traps under positive bias temperature instability (PBTI) stress. The dependences of gate bias voltage, temperature, and gate stack structure have also been investigated. Chapter 3 discusses the charge trapping and de-trapping behaviors under static and dynamic positive bias stress, and a universal charge trapping model has been proved in terms of the effective stress time. These two chapters could help us realize the threshold voltage instability in high-k devices and predict the long-term reliability

lifetime. Chapter 4 illustrates the two-frequency C-V correction method using a five-element circuit model for high-k gate dielectrics and ultrathin oxides. The physical origin of dynamic energy loss and the area dependences of parasitic components are also explained in detail. This C-V correction technique could be used later to eliminate the impact of parasitic components on the dielectric capacitance at high frequencies. Chapter 5 indicates the border trap capacitance determined by low-frequency C-V measurement as a specific characteristic of the transient charging and discharging of border traps in high-k dielectrics. Moreover, the space and energy distribution of border traps could be transformed from the frequency and voltage dependences of border trap capacitance. Chapter 6 explains the transient charging and discharging behaviors observed by low-frequency charge pumping method, and an elastic direct tunneling model with symmetric forward and reverse tunneling time constants has been proposed to extract the space and energy distribution of border traps in high-k dielectrics. Also, a comparison between the low-frequency C-V and charge pumping methods has been made to clarify the differences. Finally, chapter 7 summarizes the findings and contributions of this dissertation, and provides the suggested directions for future studies.

Table 1-I Equivalent oxide thickness (EOT) requirements for three logic technology applications projected by the 2005 ITRS roadmap [1.1].

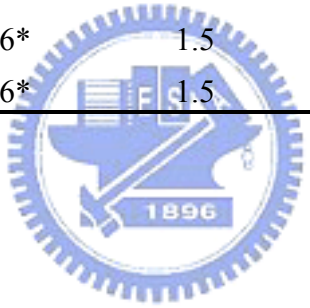
Year of Production	2005	2007	2010	2013	2016
DRAM 1/2 Pitch (nm)	80	65	45	32	22
High-Performance Logic Technology EOT Requirements					
Extended Planar Bulk (Å)	12	11	6.5		
UTB FD (Å)			7	5	
DG (Å)				6	5
Low Operating Power Logic Technology EOT Requirements					
Extended Planar Bulk (Å)	14	12	9		
UTB FD (Å)				8	7
DG (Å)				8	7
Low Stand-by Power Logic Technology EOT Requirements					
Extended Planar Bulk (Å)	21	19	14	12	
UTB FD (Å)				11	8
DG (Å)				12	11

*UTB FD: ultra-thin body fully-depleted SOI, DG: double-gate MOSFET.
: manufacturable solutions are NOT known.

Table 1-II Summarized material and electrical properties of various selected high-k gate dielectrics [1.4].

Dielectric	Dielectric constant	Bandgap (eV)	Conduction band offset (eV)	Leakage reduction	Thermal stability on Si substrate
SiO_2	3.9	9	3.5	N/A	>1050°C
Si_3N_4	7	5.3	2.4		>1050°C
Al_2O_3	~10	8.8	2.8	10^2-10^3x	~1000°C
Ta_2O_5	25	4.4	0.36		Not stable
La_2O_3	~21	6*	2.3		
Gd_2O_3	~12				
Y_2O_3	~15	6	2.3	10^4-10^5x	**Silicate formation**
HfO_2	~20	6	1.5	10^4-10^5x	~950°C
ZrO_2	~23	5.8	1.4	10^4-10^5x	~900°C
$SrTiO_3$		3.3	~0.1		
$ZrSiO_4$		6*	1.5		
$HfSiO_4$		6*	1.5		

*Estimated value



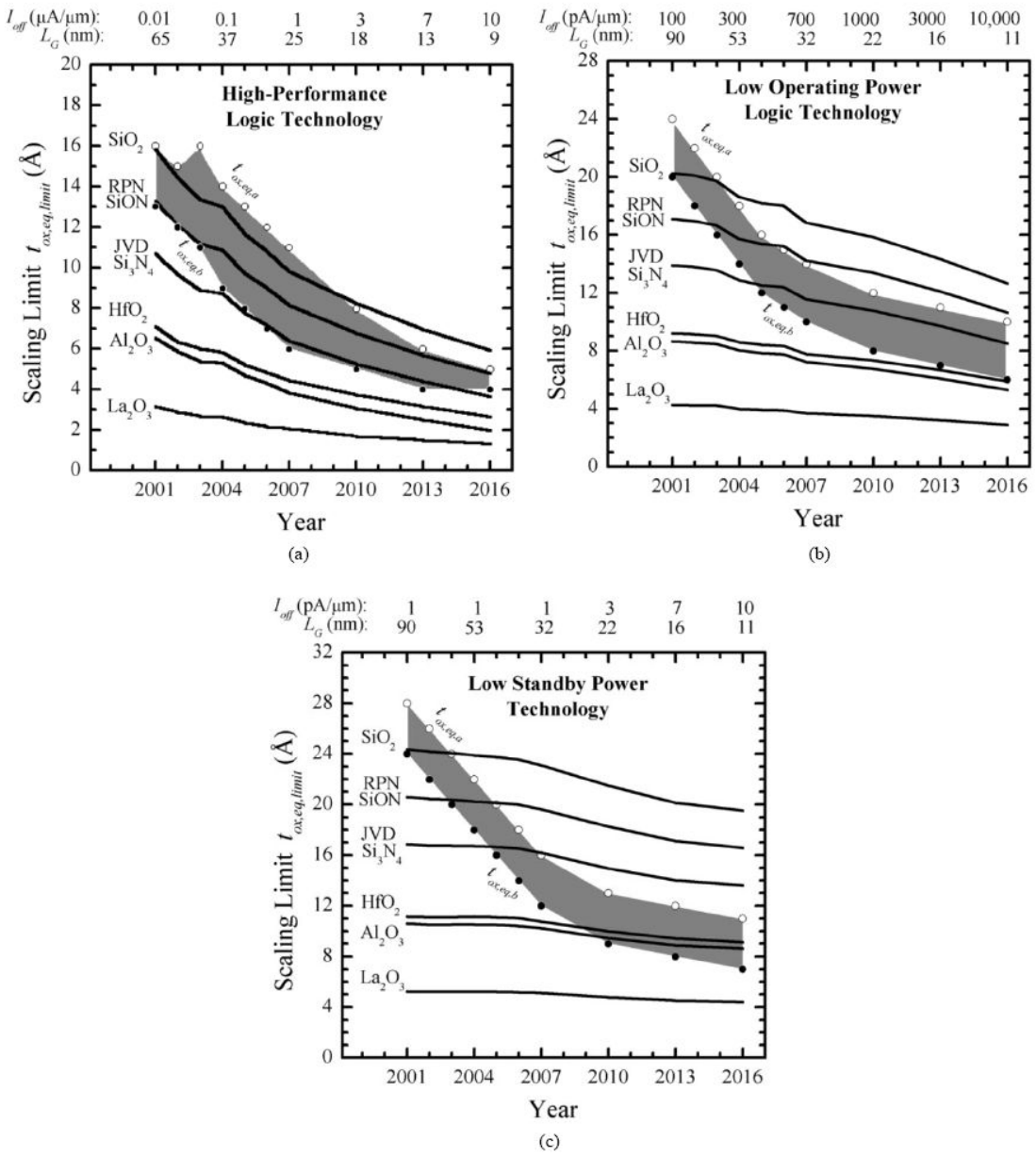


Fig. 1-1 Scaling limits (solid lines) of many different gate dielectrics as a function of the specifications for (a) high-performance, (b) low operating-power, and (c) low stand-by power logic technologies. The gray area represents the recommended $T_{ox,eq}$ values [1.3].

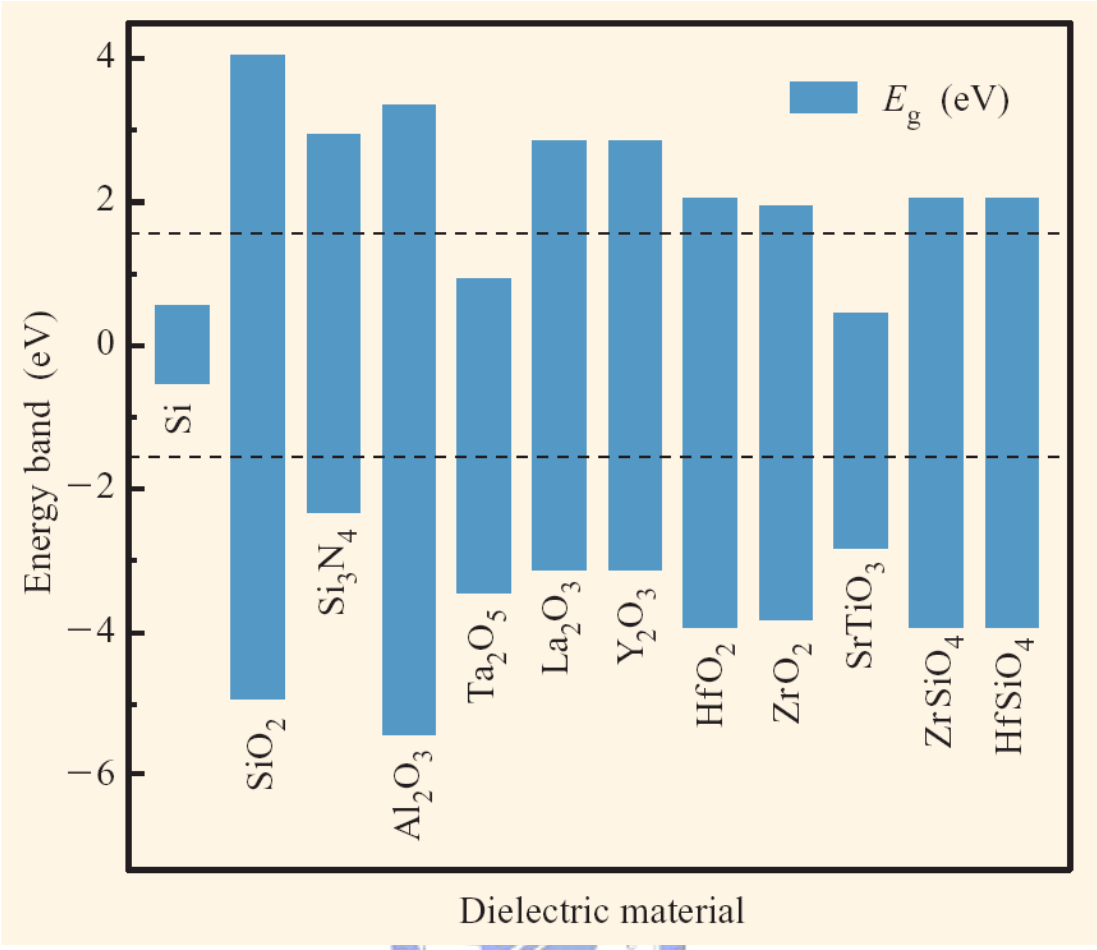


Fig. 1-2 Bandgap and band alignment of various high-k gate dielectrics with respect to silicon. The dashed lines represent 1eV above/below the conduction/ valence bands, which indicate the minimum barrier height to suppress the gate leakage current [1.5].

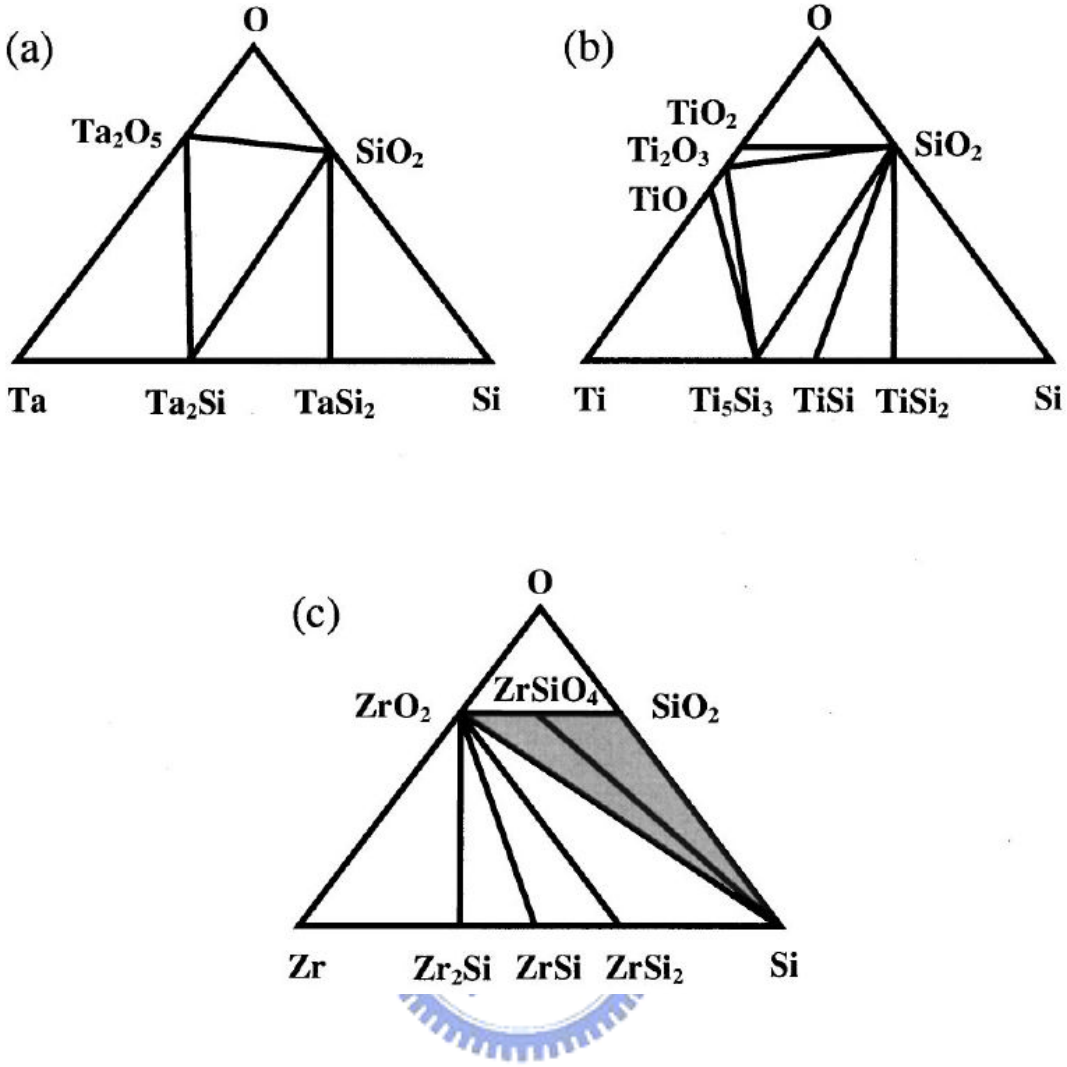


Fig. 1-3 Ternary phase diagrams for (a) Ta-Si-O, (b) Ti-Si-O, and (c) Zr-Si-O compounds. As compared to Ta_2O_5 and TiO_2, ZrO_2 is thermo-dynamically stable with SiO_2 and Si, and no phase separation would occur into the M_xO_y and M_xSi_y phases [1.6], [1.7].

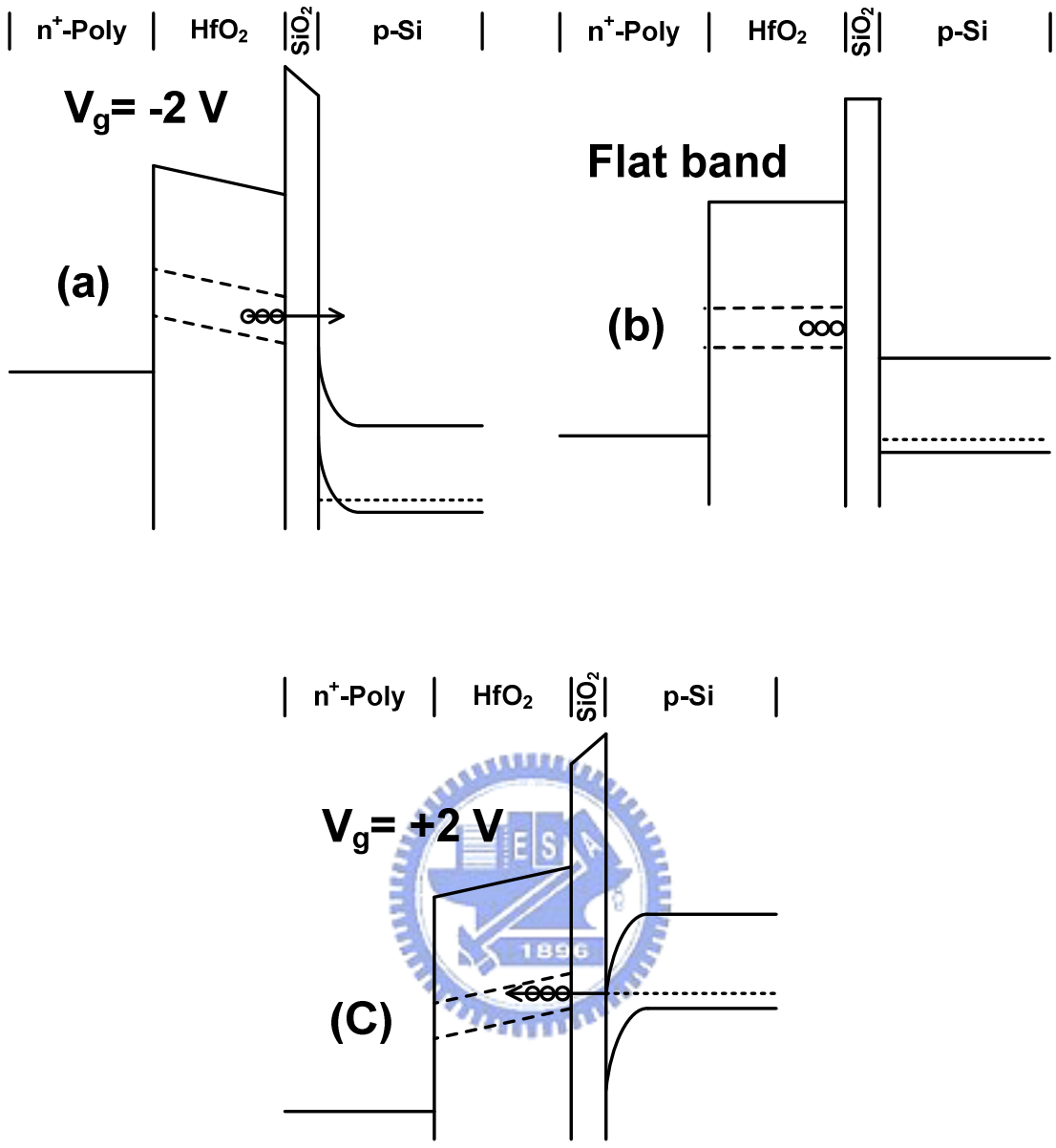


Fig. 1-4 Schematic band diagram of the dual-layer HfO_2/SiO_2 high-k gate stack biased with (a) negative gate bias, (b) flatband condition, and (c) positive gate bias. A defect band in the HfO_2 layer is positioned just above the Si conduction band edge [1.8].

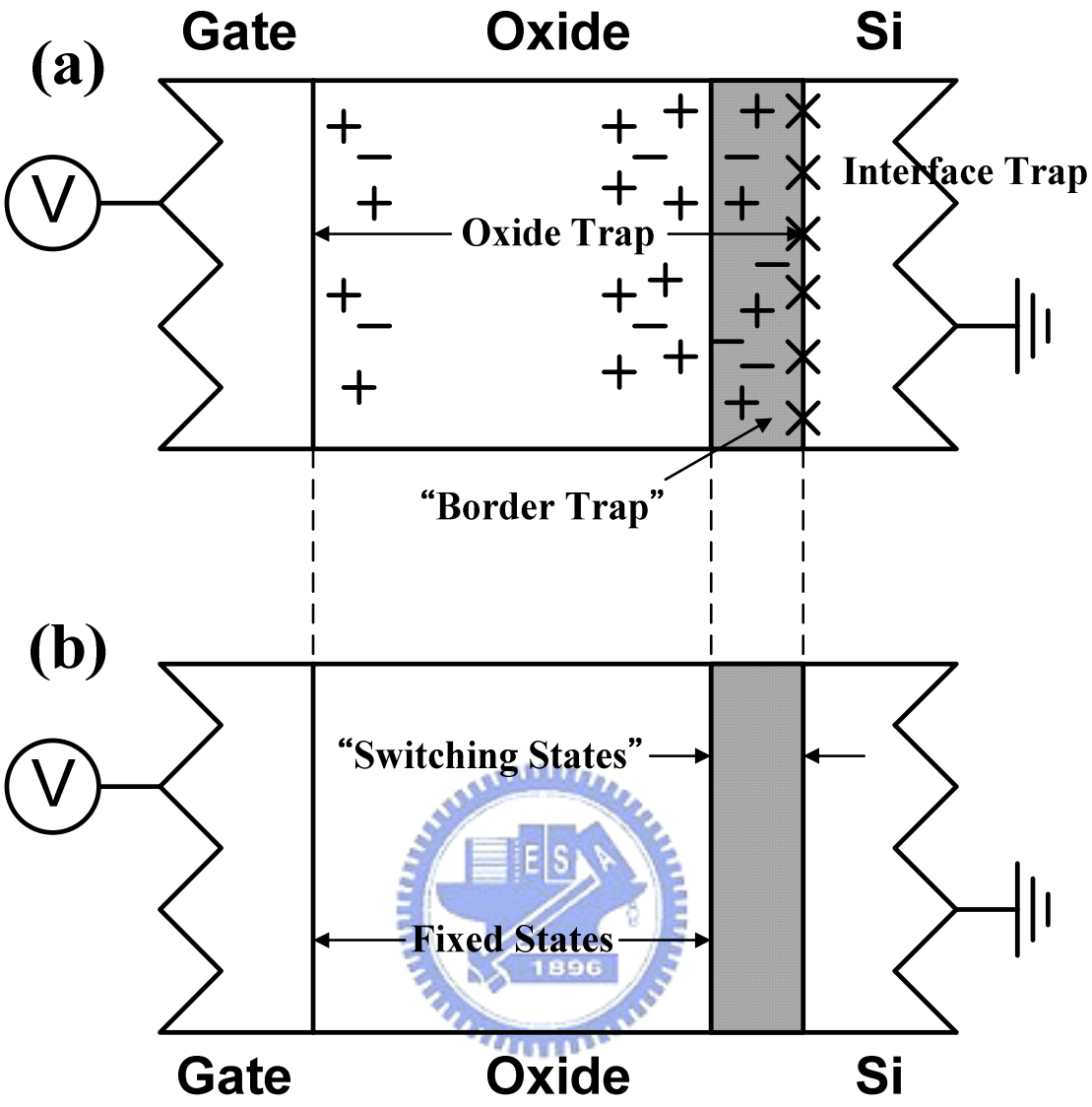


Fig. 1-5 Schematic illustration of the interface states, fixed oxide traps, and border traps in terms of (a) the spatial location of defects, and (b) their electrical response. Border traps are the near-interface oxide traps which could be detected within the time scale of electrical measurements being performed [1.22].

Chapter 2: Threshold Voltage Instability in nMOSFETs with $HfSiO/SiO_2$ High-k Gate Stack under Static PBTI Stress

2.1 Introduction

Threshold voltage (V_t) instability induced by charge trapping has been recognized as one of the critical reliability issues in Hf-based high-k gate dielectrics, especially for the nMOSFETs under substrate electron injection conditions (positive bias stress) [2.1]. The channel electrons are injected into the HfO_2 high-k gate dielectric with pre-existing bulk trap density of $3\text{-}6\text{x}10^{12}$ cm^{-2} by tunneling through the thin base oxide. In general, a defect band filled with plenty of pre-existing high-k traps is positioned above the Si conduction band edge in energy and in the HfO_2 bulk layer in space [2.2]. In other words, these pre-existing high-k traps are distributed in a wide range of space and energy, thus making the charge trapping model different from that of conventional SiO_2 or SiON. The high-k traps located at deep energy levels are believed to be responsible for the C-V hysteresis or V_t instability determined by static I_d-V_g characteristics [2.3], [2.4], and the high-k traps located at shallow energy levels are indicated as the physical origins of stress-induced leakage current (SILC) in HfO_2/SiO_2 high-k gate stacks [2.5]. In addition, the initial high-k bulk trap density has been demonstrated to be highly associated with the event of dielectric breakdown in HfO_2 high-k gate dielectrics, thus influencing the device reliability and yield [2.6].

As reported in the literature, Si atoms could be incorporated into the HfO_2 high-k gate dielectrics to suppress the dielectric re-crystallization during high temperature rapid thermal annealing (RTA) and to reduce the high-k bulk trap density [2.7], [2.8]. Moreover, the thickness of base oxide SiO_2 plays a significant role in the charging and

discharging dynamics of threshold voltage instability in the HfO_2/SiO_2 high-k gate stacks, and the tunneling time constant decreases exponentially with the decrease of base oxide thickness [2.9]. Although thin base oxide thickness is preferred for the continuous scaling of equivalent oxide thickness (EOT) below 1.0nm, this may further degrade the problem of threshold voltage instability due to fast charge trapping. Both the composition of high-k bulk layer and base oxide thickness are being modified to obtain the appropriate high-k gate stack structure with required EOT value and reduced threshold voltage instability.

This chapter will first study the fundamental characteristics of charge trapping in the $HfSiO/SiO_2$ high-k gate stack under positive bias temperature instability (PBTI) stress in section 2.3, including the carrier transport mechanism, threshold voltage shift, drain current degradation, and transconductance variation. Then, a charge trapping model with dispersive capture time constants will be used to describe and to predict the charge trapping behavior in section 2.4. Finally, section 2.5 will investigate the temperature dependence of charge trapping and the appropriate $HfSiO/SiO_2$ high-k gate stack structure for future CMOS technology nodes.

2.2 Device Fabrication and Analysis Method

MOSFET devices with the $HfSiO/SiO_2$ high-k gate stacks and poly-Si gate electrodes were fabricated using the standard CMOS process technology. After the definition of shallow trench isolation (STI) and active areas, dual gate oxide (DGO) process was employed to grow both core and I/O oxides on a single chip. For the core devices, base oxides SiO_2 ranging from 0.8 to 1.2 nm were thermally grown, followed by the deposition of metal-organic chemical vapor deposition (MOCVD) HfSiO high-k dielectrics with 50, 60 or 75% Si composition, which is defined as the atomic

ratio of Si/(Hf+Si) in the HfSiO films. Then the poly-Si gate electrodes were deposited and patterned, followed by the source/drain extension ion implantation and spacer formation. After the deep S/D ion implantation, spike rapid thermal annealing (RTA) was applied to fully activate the implanted dopants while reducing the thermal budget. Finally, cobalt salicide ($CoSi_2$), inter-metal dielectric (IMD), tungsten (W) plug, and single-damascene Cu metallization were used to complete the devices and facilitate the electrical characterization. Fig. 2-1 shows the high-resolution Rutherford backscattering spectrometry (RBS) depth profile of the HfSiO(2.0 nm)/SiO_2(1.2 nm) high-k gate stack with 50% Si composition in the HfSiO film. The optical thickness of the HfSiO and SiO_2 layers is determined by transmission electron microscopy (TEM, not shown here). A homogeneous HfSiO bulk layer with 50% Si composition has been demonstrated using the MOCVD deposition technique.

The use of base oxide is intended to improve the interface quality and provide better device performance. The HfSiO/SiO_2 high-k gate stacks with various combinations of base oxide thickness and Si composition in the HfSiO film were elaborately fabricated to produce an equivalent oxide thickness (EOT) of about 2 nm for the purpose of comparison. In addition, a 1.96-nm oxynitride gate dielectric was also prepared to serve as the control sample. In order to study the various charge trapping characteristics in the HfSiO/SiO_2 high-k gate stacks, the static PBTI stress was widely used in this study to examine the charge trapping in the nMOSFETs with various high-k gate stacks as mentioned above. In this stressing scheme, a positive bias voltage ranging from 1.2 to 1.6 V was applied to the gate at 125°C for a defined period of time, while the S/D and substrate were grounded. Positive gate bias voltage can inject inversion electrons from the channel region into the HfSiO bulk layer, and parts of these injected electrons might be trapped by the pre-existing HfSiO bulk

defects and become oxide-trapped charge. Then static I_d-V_g characteristics[1] were immediately measured at linear and saturation regions to determine the threshold voltage (V_t) and saturation drain current ($I_{d,sat}$ at V_g=V_d=1.2 V) at that moment. This procedure was consecutively repeated to extract the V_t shift and $I_{d,sat}$ degradation ($\Delta I_{d,sat}/I_{d,sat}$) until the end of the static PBTI stress, which are used as indicators to quantify the extent of charge trapping in the HfSiO/SiO_2 high-k gate stacks.

2.3 Static Positive Bias Temperature Instability (PBTI) Stress

In order to investigate the carrier transport mechanism in the HfSiO/SiO_2 high-k gate stacks under static PBTI stress (substrate electron injection conditions), the $\ln(J_g/E_{HfSiO})$ versus $E_{HfSiO}^{1/2}$ at temperatures ranging from 25 to 200°C are plotted in Fig. 2-2. If the dielectric constant κ and physical thickness d of the base oxide and HfSiO high-k dielectric are known, the electric field in each layer could be determined by the following equations:

$$D = \varepsilon_0 \kappa_{SiO2} E_{SiO2} = \varepsilon_0 \kappa_{HfSiO} E_{HfSiO,} \tag{2.1}$$

$$V_g - V_{fb} = d_{SiO2} E_{SiO2} + d_{HfSiO} E_{HfSiO}, \tag{2.2}$$

where D is the electric displacement which is supposed to be kept constant throughout this dual-layer HfSiO/SiO_2 high-k gate stack, and ε_0 is the permittivity of free space. At low fields and high temperatures, the thermally-excited electrons hopping from one isolated state to the other yield the ohmic characteristic, which is represented by the horizontal lines and is exponentially dependent on the temperature. At high fields and low temperatures, however, the field-enhanced thermal excitation of trapped

[1] Since the threshold voltage shift and drain current degradation were determined by static I_d-V_g characteristics, not by pulse I_d-V_g technique, the possible concern of transient charge de-trapping may arise. However, the focused physical entities in this chapter and chapter 3 are slow high-k traps from which the trapped charge carriers can not be de-trapped immediately when the stress bias voltage is removed. Also, the behaviors and model fitting are mainly concerning about the slow high-k traps.

electrons into the conduction band produces the Frenkel-Poole emission, which is represented by the slash lines and whose barrier height (Φ_B ~1.05 eV from F-P model fitting) for carrier re-emission is the depth of the trap potential well [2.10]. Both the ohmic and Frenkel-Poole emission are generally recognized as the trap-assisted conduction mechanisms, thus suggesting that there is a large number of trapping centers in the HfSiO bulk layer.

Fig. 2-3 shows the time evolution of (a) I_d-V_g and (b) transconductance G_m-V_g curves under static PBTI stress with V_g= +1.6 V. As can be seen, the I_d-V_g and G_m-V_g curves exhibited continuous positive voltage shifts under the static PBTI stress, presumably due to the threshold voltage shift induced by electron trapping in the HfSiO bulk layer. Moreover, the parallel shifts of the I_d-V_g and G_m-V_g curves indicate that both the subthreshold slope and maximum transconductance $G_{m,max}$ remained unchanged under the static PBTI stress even if a great amount of channel electrons had been injected into and trapped in the HfSiO bulk layer. From these observations, it appears that no degradation of the interface quality occurred due to the carrier injection, whereas the amount of trapped charge in the HfSiO bulk layer continued to grow and eventually became saturated.

2.4 Modeling of Static PBTI Stress Behavior

Fig. 2-4 shows (a) the threshold voltage (V_t) shift and (b) the saturation drain current ($I_{d,sat}$) degradation as a function of stress time for nMOSFETs under static PBTI stress at various gate bias voltages. The symbols are measurement data, while the solid lines are the curve fitting results using the physical model proposed by Zafar et al., which depicts the phenomena of charge trapping in HfO_2 and Al_2O_3 high-k gate dielectrics [2.11]. This model assumes that the injected charge carriers are captured in

the pre-existing bulk traps in the high-k gate dielectrics with dispersive capture time constants and that no additional new traps are generated during the static PBTI stress. The V_t shift induced by charge trapping is formulated as a function of stress time:

$$\Delta V_t(t) = \Delta V_{t,\max} \times (1 - \exp(-(t/\tau)^{\beta})), \tag{2.3}$$

where $\Delta V_{t,max}$ is the maximum threshold voltage shift if all the high-k bulk traps are filled with trapped charge, t is the PBTI stress time, τ is the characteristic capture time constant, and β is the distribution factor of the capture time constants (If β=1, this model would be the same as the charge trapping model in SiO_2 with discrete capture time constant). This three-parameter fitting model can well describe the behavior of charge trapping in the HfSiO high-k dielectrics under various gate bias voltages. According to the results of curve fitting shown in Table 2-I, the fitting parameters $\Delta V_{t,max}$ and τ vary with the gate bias voltage, but β remains constant at about 0.32. This is consistent with Zafar's previous work, and it suggests that charge trapping is a field-enhanced process and that the distribution of bulk traps with different capture time constant is independent of V_g and might be a materials issue. As can be seen in Fig. 2-4, both V_t shift and $I_{d,sat}$ degradation increased with the stress time in a power law relation when the stress time is much less than the capture time constant τ, and they may eventually become saturated after prolonged charge injection. These findings can also be explained by the above physical model.

Fig. 2-5 shows a linear relation between the V_t shift and $I_{d,sat}$ degradation (V_t shift= 4.3(mV/%) x $I_{d,sat}$ degradation), and this linear relation can be equally applied to various gate bias voltages ranging from +1.2 to +1.6 V. Since the subthreshold swing and maximum transconductance $G_{m,max}$ remain unchanged during the PBT stress, the increase of the threshold voltage is mainly responsible for the saturation drain current degradation.

2.5 Dependences of Temperature and Gate Stack Structure

Fig. 2-6 shows the V_t shift as a function of stress time at temperatures ranging from 25 to 160°C. The V_t shift induced by charge trapping increased exponentially with temperature and followed the Arrhenius equation with activation energy E_a of 0.0357 eV under V_g= +2.0 V (the inset), which is a function of the applied electric field and process conditions. These findings can be explained by considering the carrier transport process from inversion channel to poly-Si gate under positive gate bias voltages. At first the channel electrons tunnel through the ultrathin base oxide and penetrate into the HfSiO bulk traps. Then these injected charge carriers may hop from trap to trap due to the thermal excitation (ohmic conduction) or they may directly jump into the conduction band due to the field enhancement during the hopping process (Frenkel-Poole emission), depending on the applied gate bias voltage. Since quantum direct tunneling is essentially independent of temperature, the temperature dependence of the V_t shift should result largely from the trap-assisted tunneling process. Moreover, the number of the trapped charge carriers that possess enough kinetic energy to overcome the trap potential barrier and to emit into the conduction band per unit time would increase exponentially due to the thermal excitation. In fact, the activation energy E_a= 0.0354 eV for the gate current density under the same gate bias voltage (V_g= +2.0 V) is almost identical to that of the V_t shift in Fig. 2-6. Thus, the temperature dependence of the V_t shift is mainly attributed to the increase of the charging current density at high temperatures.

The effects of the base oxide thickness and Si composition in the HfSiO films on $I_{d,sat}$ degradation are illustrated in Fig. 2-7. The extent of charge trapping in the HfSiO/SiO_2 high-k gate stacks increased with the decrease of base oxide thickness as

well as the Si composition in the HfSiO films, whereas the oxynitride SiON gate dielectric exhibited negligible charge trapping under the static PBTI stress. These findings can be explained by considering the channel-to-bulk tunneling time constant and the amount of neutral Hf-OH trapping centers in the HfSiO bulk layer [2.1], [2.9]. The tunneling time constant decreases exponentially with decreasing base oxide thickness, and the typical tunneling time constants are calculated to be 0.1 and 100 μs for 1- and 2-nm base oxides, respectively [2.12]. Since the Si composition in the HfSiO films (the ratio of Si/(Hf+Si) atoms) represents the percentage of Hf atoms in the HfO_2 high-k dielectrics replaced by Si atoms, the higher the Si composition is, the lower the number of neutral Hf-OH trapping centers is in the HfSiO bulk layer. Consequently, the extent of charge trapping decreases with the increase of Si composition in the HfSiO films. Fig. 2-8 shows that the $I_{d,sat}$ degradation at a specific stress time (3000 sec) increased rapidly in a power law relationship with the gate bias voltage for various combinations of base oxide thickness and Si composition in the HfSiO film. The exponent of the power law relationships declined with the decrease of base oxide thickness and Si composition, which follows the same trend in Fig. 2-7, thus implying that there should be more significant charge trapping in the further scaled Hf-based high-k gate stacks. Therefore, the $HfSiO/SiO_2$ high-k gate stack with appropriate base oxide thickness and Si composition in the HfSiO film should be employed to minimize the charge trapping while achieving the requirements of EOT scaling and gate leakage current.

2.6 Summary

In this chapter, charge trapping characteristics in the $HfSiO/SiO_2$ high-k gate stacks are investigated with regard to the base oxide thickness and Si composition in

the HfSiO film. It was found that ohmic and Frenkel-Poole emission are the major carrier transport mechanisms in the HfSiO/SiO_2 high-k gate stacks under static PBTI stress conditions. During the PBTI stress, V_t shift and $I_{d,sat}$ degradation continue to grow and eventually become saturated, whereas the subthreshold swing and maximum transconductance remain unchanged. Positive gate bias voltage can introduce a great number of channel electrons into the pre-existing HfSiO bulk defects without degrading the interface quality. The V_t shift induced by charge trapping is mainly responsible for the $I_{d,sat}$ degradation, and there exists a linear relation between the V_t shift and $I_{d,sat}$ degradation, which can be equally applied to various gate bias voltages (+1.2 to +1.6 V in this study). The gate bias and temperature dependence reveals that the V_t shift induced by charge trapping is field-enhanced and thermally–activated, presumably due to the physical nature of trap-assisted tunneling process. Moreover, the extent of charge trapping increases with decreasing base oxide thickness and Si composition in the HfSiO film, and the channel-to-bulk tunneling time constant and the amount of neutral Hf-OH trapping centers are believed to be the determining factors for these observed phenomena. Finally, the decreasing exponent of the power law relation of saturation drain current degradation indicates that charge trapping would become more significant if thin base oxide and low Si composition were employed in the further scaled HfSiO/SiO_2 high-k gate stacks.

Table 2-I Gate bias voltage dependence of the three fitting parameters, $\Delta V_{t,max}$, τ and β, in the physical model of charge trapping in high-k gate dielectrics.

Parameter	***Unit***	***Gate Bias Voltage Dependence***
$\Delta V_{t,max}$	V	$\Delta V_{t,\max} \sim 358.53 \times \ln(V_g) + 5.96$, logarithmic
τ	s	$\tau \sim 3.55 \times 10^5 \times \exp(-3.79 \times V_g)$, exponential decay
β	-	β~0.32, independent of gate bias voltage

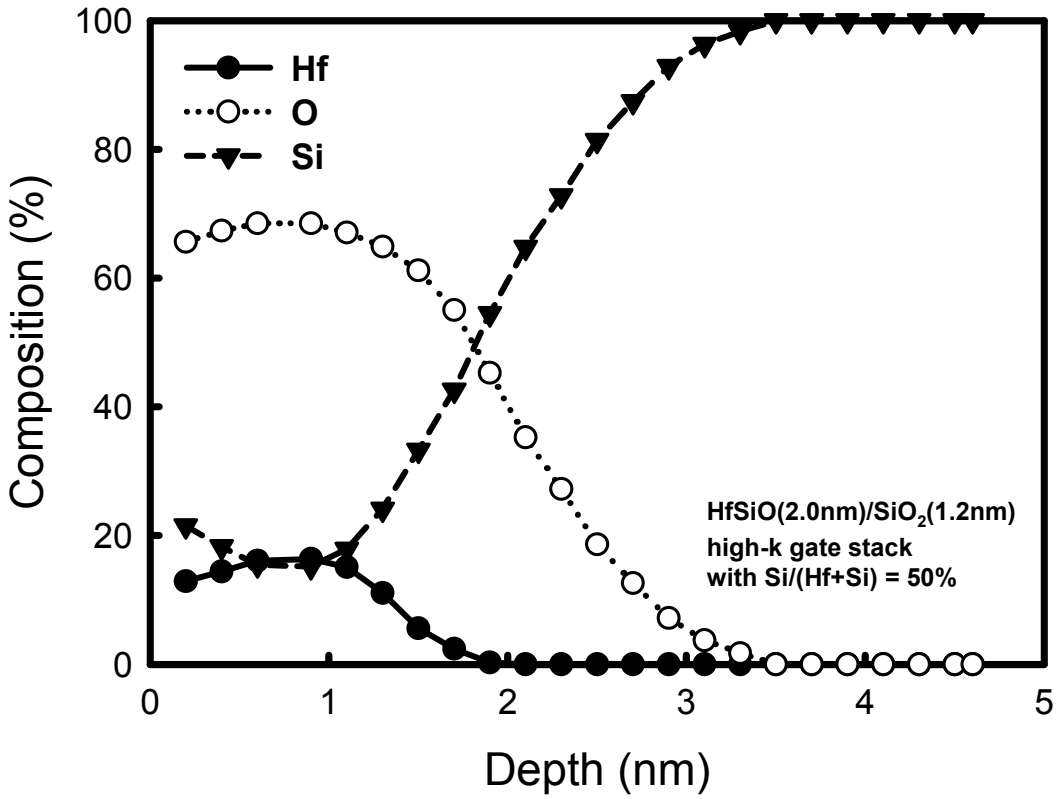


Fig. 2-1 High-resolution Rutherford backscattering spectrometry (RBS) depth profile of the HfSiO(2.0 nm)/SiO_2(1.2 nm) high-k gate stack with 50% Si composition in the HfSiO film.

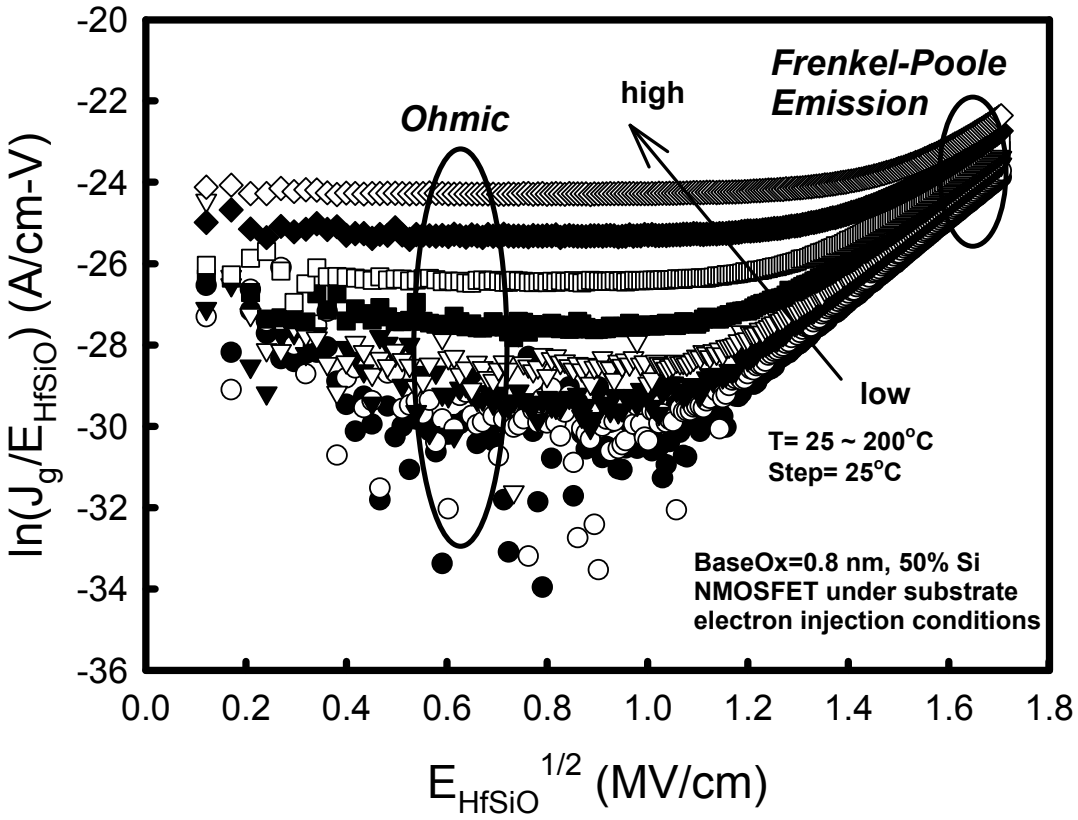
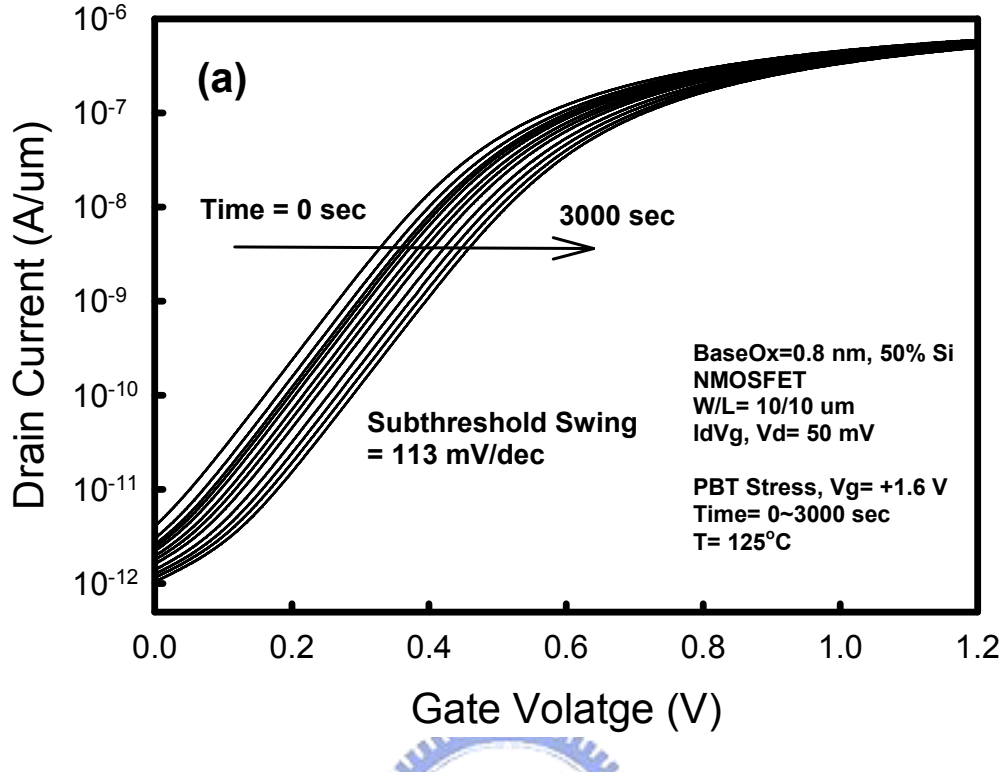


Fig. 2-2 Carrier transport mechanism in the $HfSiO/SiO_2$ high-k gate stack under substrate electron injection conditions at temperatures ranging from 25 to 200°C.



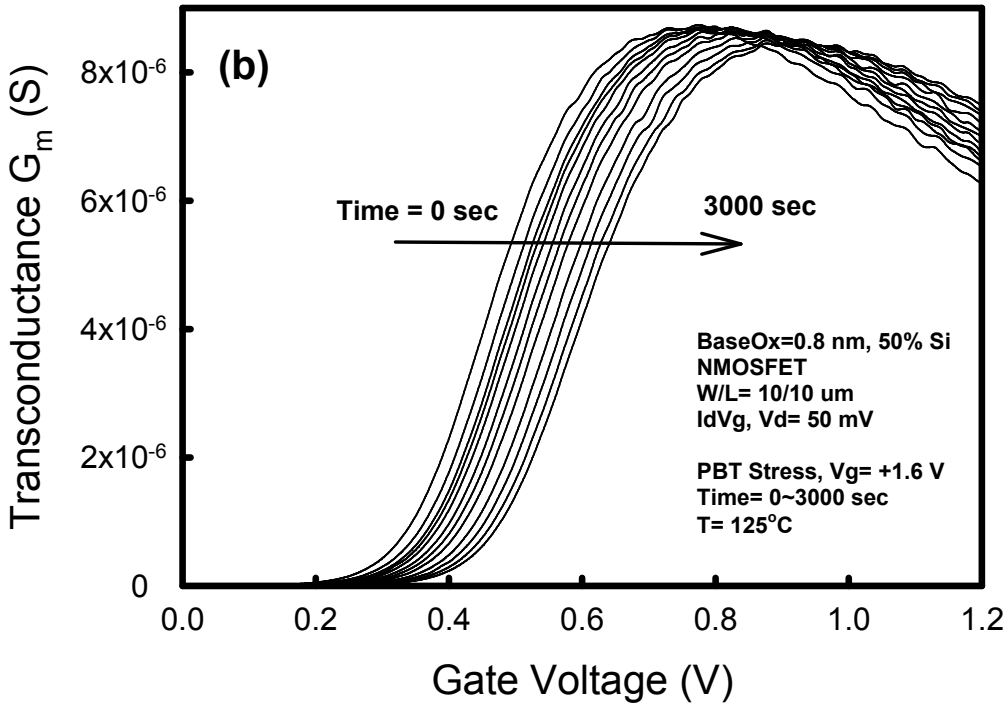
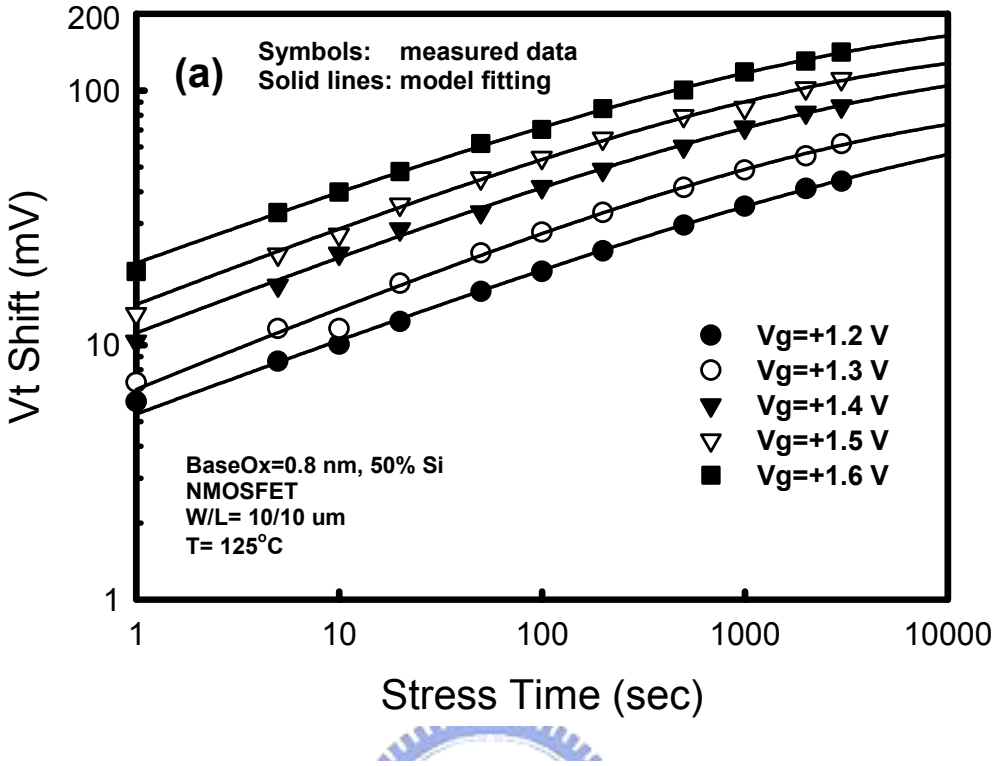


Fig. 2-3 Time evolution of (a) I_d-V_g and (b) G_m-V_g curves of the nMOSFETs with HfSiO/SiO_2 high-k gate stacks under static PBTI stress.



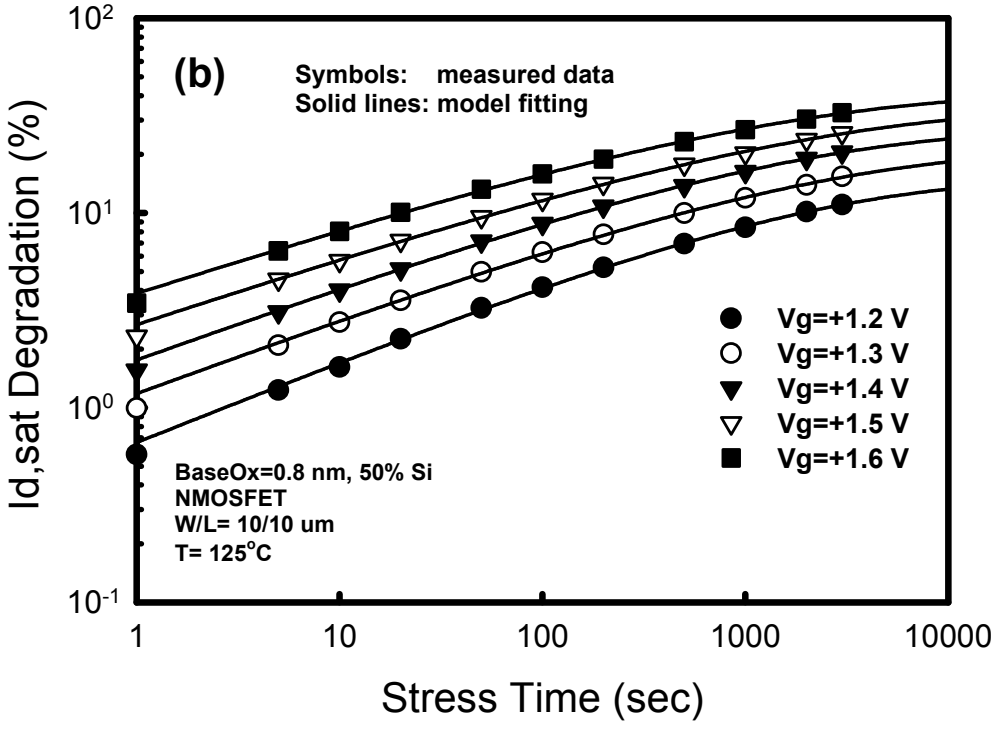


Fig. 2-4 (a) Threshold voltage shift and (b) saturation drain current degradation of the nMOSFETs under various positive gate bias voltages as a function of stress time

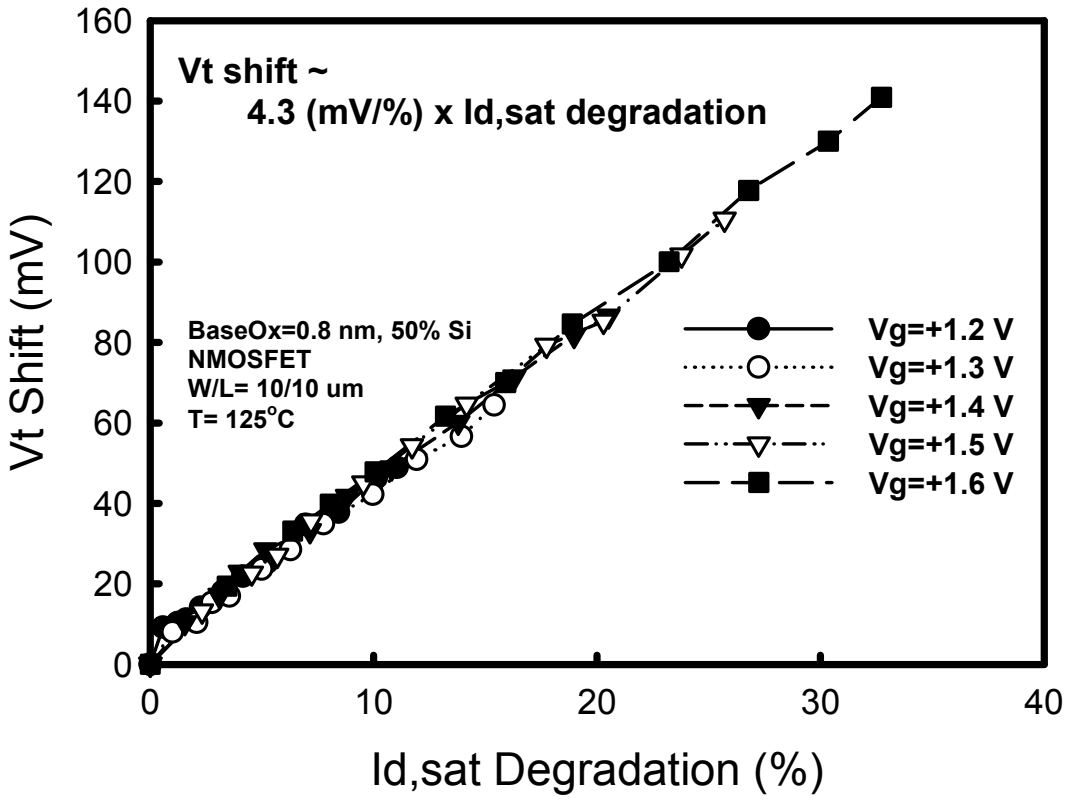


Fig. 2-5 Linear relation between the threshold voltage shift and saturation drain current degradation under static PBTI stress, which can be equally applied to various gate bias voltages.

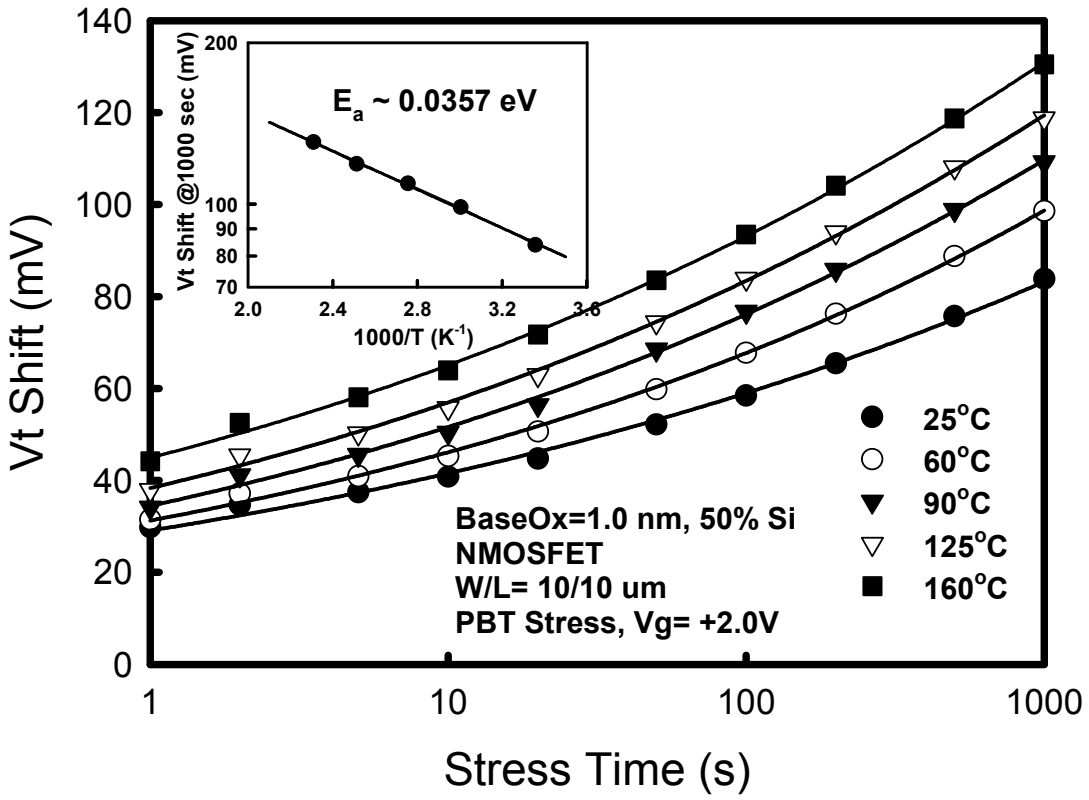


Fig. 2-6 Threshold voltage shift as a function of stress time under +2.0 V gate bias voltage at various temperatures. The inset indicates that the V_t shift follows the Arrhenius equation with the activation energy of 0.0357 eV under V_g= +2.0 V.

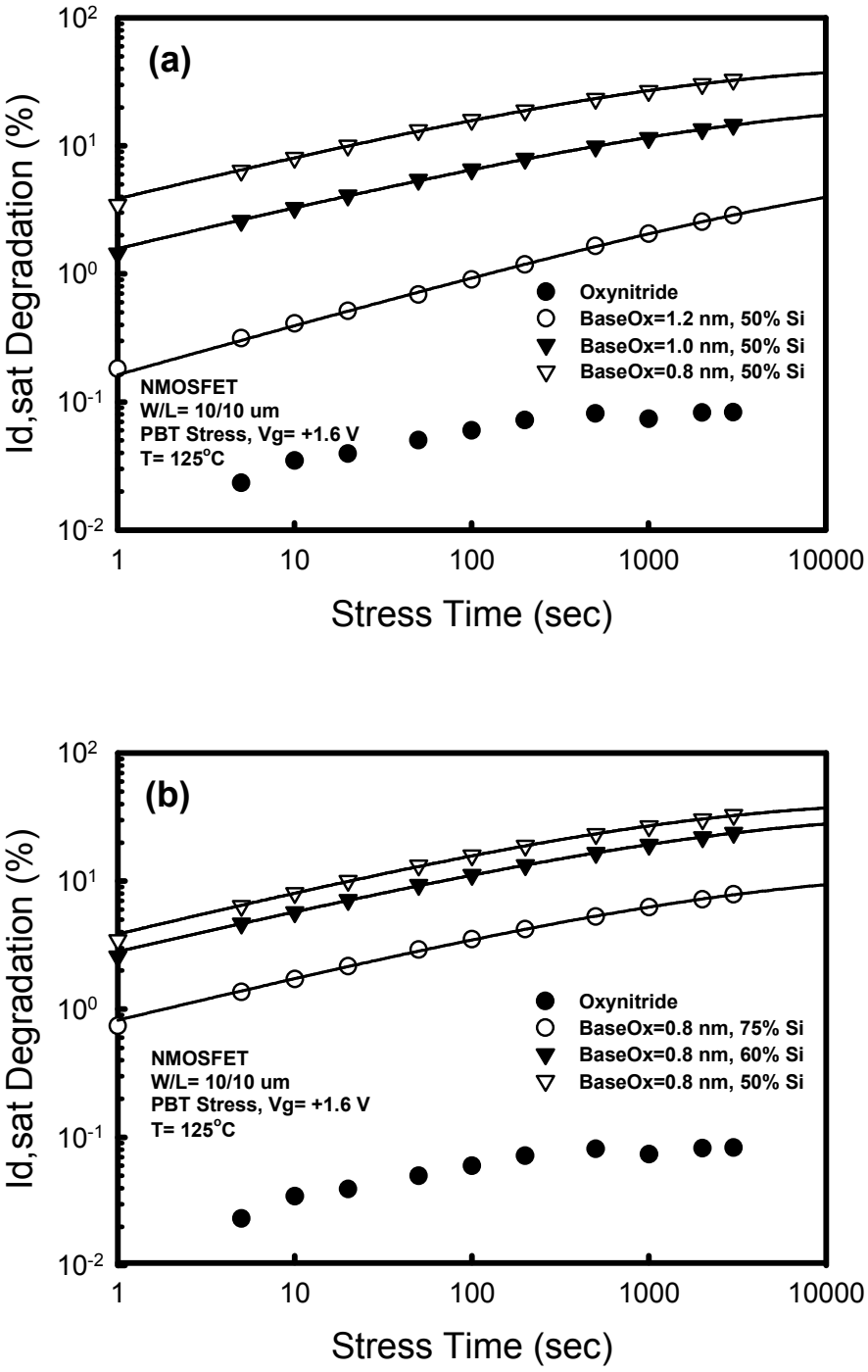


Fig. 2-7 Saturation drain current degradation under +1.6 V gate bias voltage as a function of stress time for the $HfSiO/SiO_2$ high-k gate stacks with different (a) base oxide thickness and (b) Si composition in the HfSiO film. Base oxide thickness of 1.2 nm and Si composition of 75% are preferred for the reduction of charge trapping.

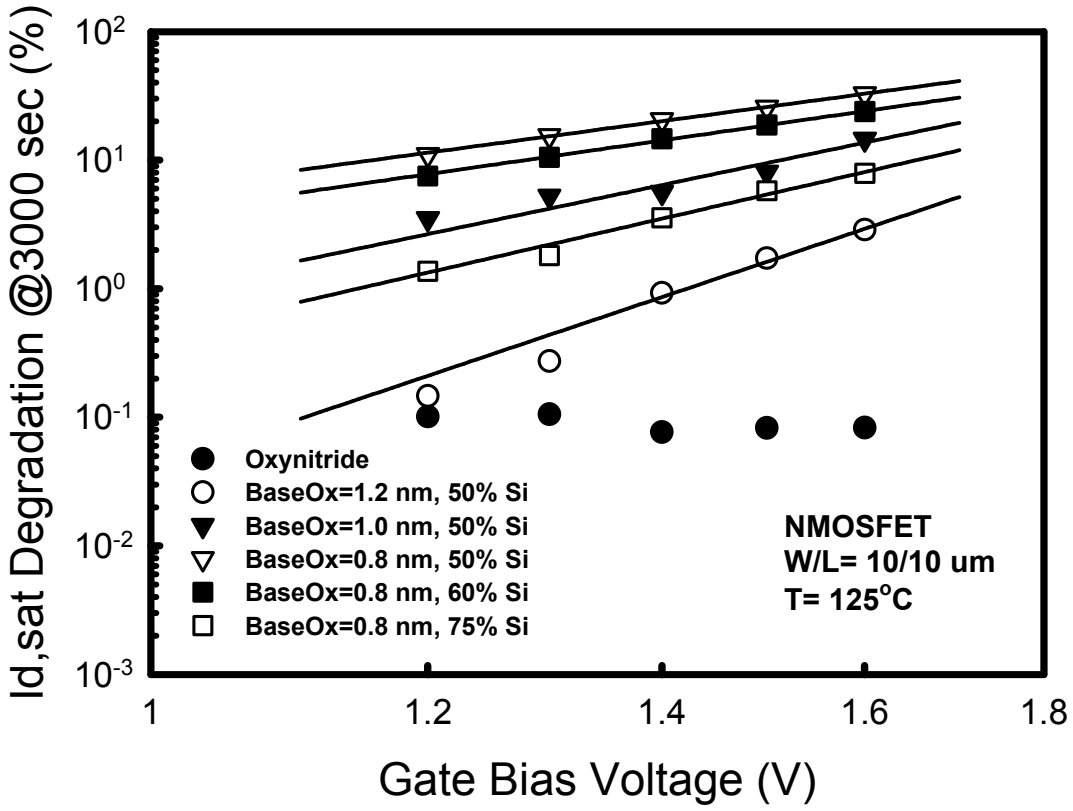


Fig. 2-8 Power law dependence of saturation drain current degradation on the gate bias voltage for the $HfSiO/SiO_2$ high-k gate stacks with various combinations of base oxide thickness and Si composition in the HfSiO film.

Chapter 3: Charge Trapping and De-trapping Behaviors in the Dual-Layer HfO_2/SiO_2 High-k Gate Stack under Static and Dynamic Positive Bias Stress

3.1 Introduction

Unlike the negative bias temperature instability (NBTI) in PMOS devices with conventional ultrathin oxide, threshold voltage instability in Hf-based high-k gate dielectrics has been recognized as the most critical reliability issue that needs to be solved urgently, especially the positive bias temperature instability (PBTI) in high-k NMOS devices even stressed at moderate temperatures [3.1]-[3.3]. This is attributed to the fast charge trapping and de-trapping in pre-existing bulk traps in the HfO_2 high-k gate dielectric [3.4]-[3.6]. Since these charge carriers could be quickly and easily trapped/de-trapped by applying a forward/reverse bias voltage, this may lead to the underestimate of charge trapping in high-k gate dielectrics due to the switching and measurement delays within the stress/measure cycles [3.7]. Also, it is found that the trapped charge carriers could recover to the pre-stress condition after prolonged recovery time, and the recovery rate depends more on the recovery voltage and recovery time rather than the amount of injected charge carriers in high-k gate dielectrics. However, the trapping rate within the stress/recovery cycles would become gradually saturated and follow the initial stress time dependence (pre-recovery) due to the repelling build-in potential of trapped charge carriers [3.8], [3.9]. In other words, these reversible charge trapping and de-trapping behaviors are highly related to the stress history of previously trapped charge carriers, thus implying these high-k traps are pre-existing bulk traps in the Hf-based high-k gate dielectrics.

In this chapter, the charge trapping and de-trapping behaviors under various static stress and recovery voltages will be first studied in detail to understand the charging and discharging physical model during the consecutive static stress/recovery cycles in section 3.3. Then in section 3.4, the fundamental characteristics of charge trapping will be studied under dynamic positive bias stress at a specific frequency (f= 100 kHz) so as to realize the differences between the static and dynamic positive bias stresses. Finally, the transient charging behavior will be analyzed by changing the effective stress time within one cycle to realize the dynamics of charge trapping model in section 3.5.

3.2 Device Fabrication and Analysis Method

NMOS devices with the poly-Si/TaC/HfO_2/SiO_2 high-k gate stack were fabricated using the conventional CMOS process technology. Interfacial oxide (~0.8 nm) was thermally grown, followed by the deposition of HfO_2 (~3.2 nm) high-k gate dielectric using atomic layer deposition (ALD) technique. Then n-type metal gate electrode TaC (Φ_m~ 4.3 eV on HfO_2 [3.10]) was deposited using physical vapor deposition (PVD) method, and the poly-Si gate served as the capping layer to ensure the process compatibility. The equivalent oxide thickness (EOT) of the above mentioned high-k gate stack was extracted to be 1.48 nm by using the C-V simulation program which has taken the quantum effect into account [3.11]. The dynamic stress was performed by applying a series of pulse trains to the gate. The typical pulse waveforms are illustrated as follows unless specified otherwise: the frequency is 100k Hz, duty cycle is 50%, rise time and fall time are both 10 ns, and peak and base level voltages are +2.0 and 0 V, respectively.

3.3 Charge Trapping and De-trapping Behaviors during the Stress/ Recovery Cycles under Static Positive Bias Stress

Fig. 3-1 shows the threshold voltage shift of the dual-layer HfO_2/SiO_2 high-k gate stack as a function of the static stress/recovery time with a fixed stress voltage V_g= +2.0 V and various recovery voltages V_g= 0 ~ -2.0 V. The threshold voltage shift in this study is determined from the static I_d-V_g characteristics. Basically, the recovery voltage plays a significant role to clean up the trapped charge carriers before the next stress cycle. Under strong recovery voltage V_g= -2.0 V, almost all the trapped electrons in the HfO_2 high-k traps could be de-trapped immediately, and similar charge trapping/de-trapping behaviors could be observed and repeated during the three consecutive stress/recovery cycles of static positive bias stress. However, the charge trapping/de-trapping behaviors changed under weak recovery voltages since the trapped charge carriers had not been completely removed during the previous recovery cycles. Fig. 3-2 shows the threshold voltage shift as a function of the static stress/recovery time with various stress voltages V_g= +1.6 ~ +2.8 V and a fixed recovery voltage V_g= -1.6 V. Similar charge trapping/de-trapping behaviors could also be observed and repeated during the three stress/recovery cycles even under strong stress voltages. Here a moderate recovery bias voltage V_g= -1.6 V has been used to avoid the hole trapping under strong negative bias voltages. These findings suggest that these high-k traps are the pre-existing bulk traps in the HfO_2 high-k dielectrics and that no additional high-k bulk traps have been generated during the stress cycles [3.4], [3.6].

3.4 Threshold Voltage Instability under Dynamic Positive Bias Stress

Fig. 3-3 shows the time evolution of (a) I_d-V_g and (b) G_m-V_g curves of the

nMOSFET with dual-layer HfO_2/SiO_2 high-k gate stack under dynamic positive bias stress (stress V_g= +2.0 V, recovery V_g= 0 V, frequency= 100k Hz, and duty cycle= 50%). The I_d-V_g and G_m-V_g curves also exhibited continuous positive shifts with stress time under dynamic positive bias stress, presumably due to the threshold voltage instability induced by charge trapping in the HfO_2 bulk layer. Moreover, the parallel shifts of these I_d-V_g and G_m-V_g curves indicate that both the subthreshold swing and maximum transconductance remained constant under dynamic positive bias stress even if a great number of charge carriers had been trapped and de-trapped in the HfO_2 bulk layer. These findings are consistent with those under static positive bias stress. Fig. 3-4 shows the threshold voltage shift of the dual-layer HfO_2/SiO_2 high-k gate stack as a function of the stress time under dynamic positive bias stress with various stress voltages V_g= +1.2 ~ +2.8 V. As can be seen, the V_t shift follows the power law relation $\Delta V_t \sim t^{0.18}$ under various stress voltages[2], and the V_t shift would eventually become saturated under high stress voltages or after prolonged stress time. These findings are consistent with those under static positive bias stress, thus suggesting charge trapping in the pre-existing traps in HfO_2 high-k dielectrics [3.12]. Fig. 3-5 shows the linear relationship between the V_t shift and $I_{d,lin}$ degradation ($I_{d,lin}$ degradation = 0.3(%/mV) x V_t shift), and this linear relationship can be equally applied to various stress bias voltages ranging from +1.2 to +2.8 V. Since the subthreshold swing and maximum transconductance remain constant during the dynamic positive bias stress, the threshold voltage shift is mainly responsible for the drain current degradation biased in the linear region. It appears that the trapped charge

[2] The time dependence of power law here could be regarded as another function form of the previous charge filling model with dispersive capture time constants (stretched exponential growth model). If the term $(t/\tau)^{\beta}$ is much smaller than 1, the Taylor series expansion of stretched exponential growth model could be transformed into this power law model $\sim t^{\beta}$. In addition, this model could also be transformed into the logarithmic time dependence log(t) when $0<(t/\tau)^{\beta}<1$. In other words, we may observe different time dependence under different situations due to the change of $(t/\tau)^{\beta}$ value.

carriers in the HfO_2 high-k dielectric follow the same physical rules whether under dynamic or static positive bias stress.

3.5 Charge Trapping and De-trapping Behaviors during the Stress/ Recovery Cycles under Dynamic Positive Bias Stress

Fig. 3-6 shows the threshold voltage shift as a function of stress time under the bipolar dynamic stress at f= 100k Hz with a fixed peak level voltage V_{peak}= +2.0 V and various base level voltages V_{base}=0 ~ -2.0 V. As can be seen, the amount of trapped charge carriers decreased drastically with the increasing negative base level voltage. Similar to the charge de-trapping during the static recovery cycles, the negative V_{base} bias voltage is also significant to instantly pull out the trapped electrons from the pre-existing HfO_2 high-k traps even within the short recovery time period of the bipolar dynamic stress.

Fig. 3-7 shows the threshold voltage shift of the dual-layer HfO_2/SiO_2 high-k gate stack as a function of the stress time under dynamic positive bias stress with various duty cycles ranging from 0.1 to 90%. As can be seen, V_t shift is highly associated with the duty cycle, and V_t shift is not linearly proportional to the duty cycle. Negligible V_t shift could be observed at very small duty cycles ~0.1-0.2%, thus implying the transition time for the charge carriers to be injected. Fig. 3-8 shows the threshold voltage shift as a function of the pulse width of stress pulse waveform under dynamic positive bias stress at various stress times ranging from 1 to 1000 sec, where the pulse width is the pulse period multiplied by duty cycles. By changing the pulse width of stress pulse waveform, the charge trapping behavior could be analyzed over a wide range of stress time period. It was found that the number of trapped charge carriers is not linearly proportional to the stress time period within one pulse cycle and that the

transient charge trapping might occur within only 10-50 ns. The kink near 1μs pulse width implies that some slower high-k traps may have trapping/de-trapping time constants longer than 1μs. Fig. 3-9 shows the threshold voltage shift as a function of effective stress time under dynamic positive bias stress, where the effective stress time is transformed from the stress time multiplied by duty cycles in Fig. 3-8. It has been demonstrated that a universal charge trapping model should be followed in terms of the effective stress time even under the dynamic positive bias stress with different duty cycles if the amount of de-trapped charge carriers is negligible during the short recovery time period as compared to the total injected charge carriers. These findings could also explain and support the frequency dependence of threshold voltage instability in the previous studies about dynamic positive bias stress, where the amount of trapped charge carriers decreased with the increasing frequency due to the shorter stress time period within one pulse cycle [3.13]-[3.15].

3.6 Summary

The charge trapping and de-trapping behaviors in the dual-layer HfO_2/SiO_2 high-k gate stack have been extensively studied under the static and dynamic positive bias stress with various stress and recovery voltages. Similar charge trapping and de-trapping behaviors could be observed and repeated during the consecutive static stress/recovery cycles if the recovery bias voltage is strong enough to remove most of the trapped charge carriers, thus suggesting that these high-k traps are the pre-existing bulk traps in the HfO_2 high-k dielectric and that no additional high-k bulk traps have been generated during the stress cycles. Moreover, the charge trapping behavior at different stress times could be analyzed over a wide range of stress time period within one pulse cycle by changing the pulse width of stress pulse waveform at a specific

frequency. Transient charge trapping phenomenon could be observed within only 10-50 ns, and a universal charge trapping model has also been demonstrated in terms of the effective stress time.

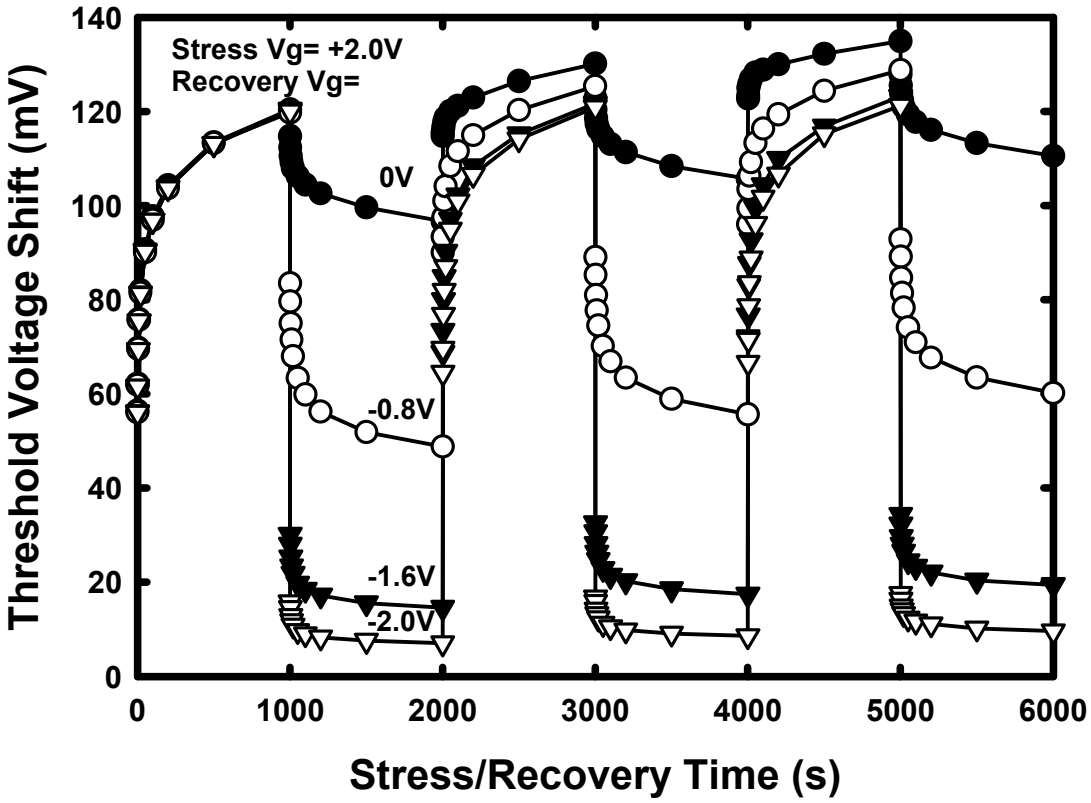


Fig. 3-1 Threshold voltage shift of the dual-layer HfO_2/SiO_2 high-k gate stack as a function of the static stress/recovery time with fixed stress voltage V_g= +2.0 V and various recovery voltages V_g= 0 ~ -2.0 V.

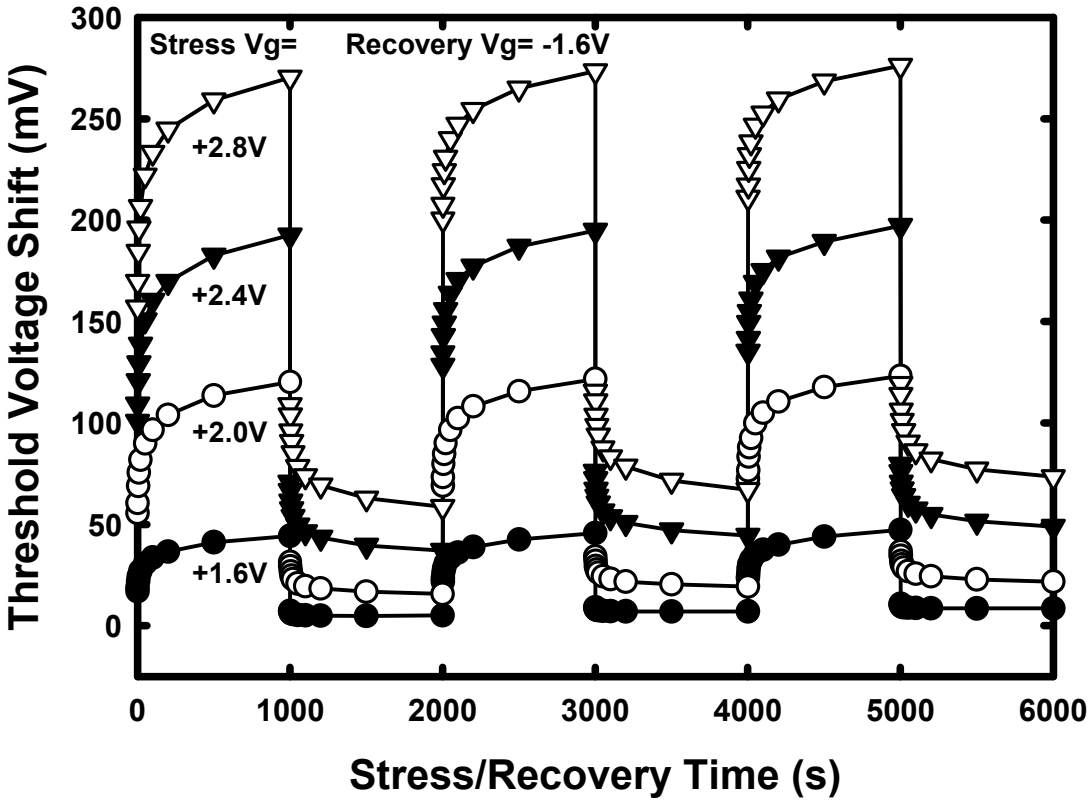


Fig. 3-2 Threshold voltage shift of the dual-layer HfO_2/SiO_2 high-k gate stack as a function of the static stress/recovery time with various stress voltages V_g= +1.6 ~ +2.8 V and fixed recovery voltage V_g= -1.6 V.

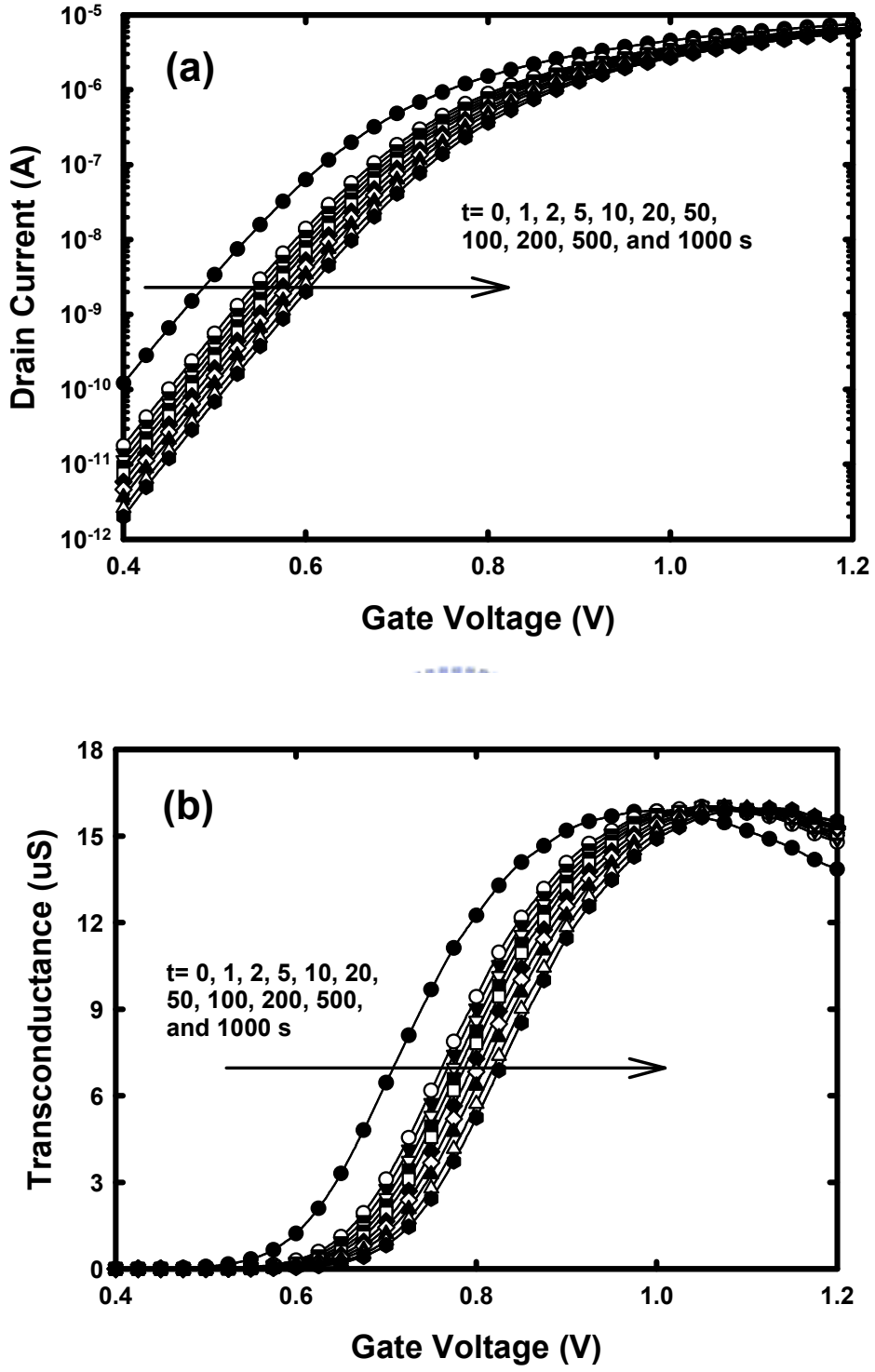


Fig. 3-3 Time evolution of (a) I_d-V_g and (b) G_m-V_g curves of the nMOSFET with dual-layer HfO_2/SiO_2 high-k gate stack under dynamic positive bias stress (stress V_g= +2.0 V, recovery V_g= 0 V, frequency= 100k Hz, and duty cycle= 50%).

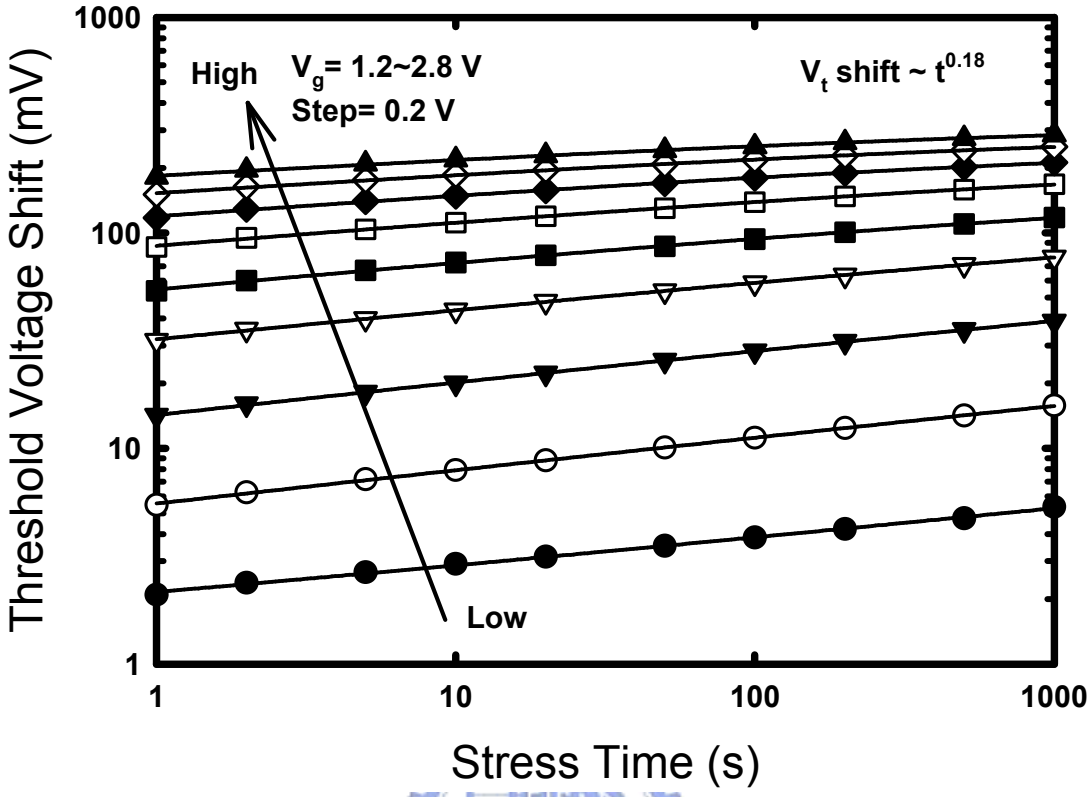


Fig. 3-4 Threshold voltage shift of the dual-layer HfO_2/SiO_2 high-k gate stack as a function of the stress time under dynamic positive bias stress with various stress voltages V_g= +1.2 ~ +2.8 V. As can be seen, the V_t shift follows the power law relation ~$t^{0.18}$ as that under static positive bias stress.

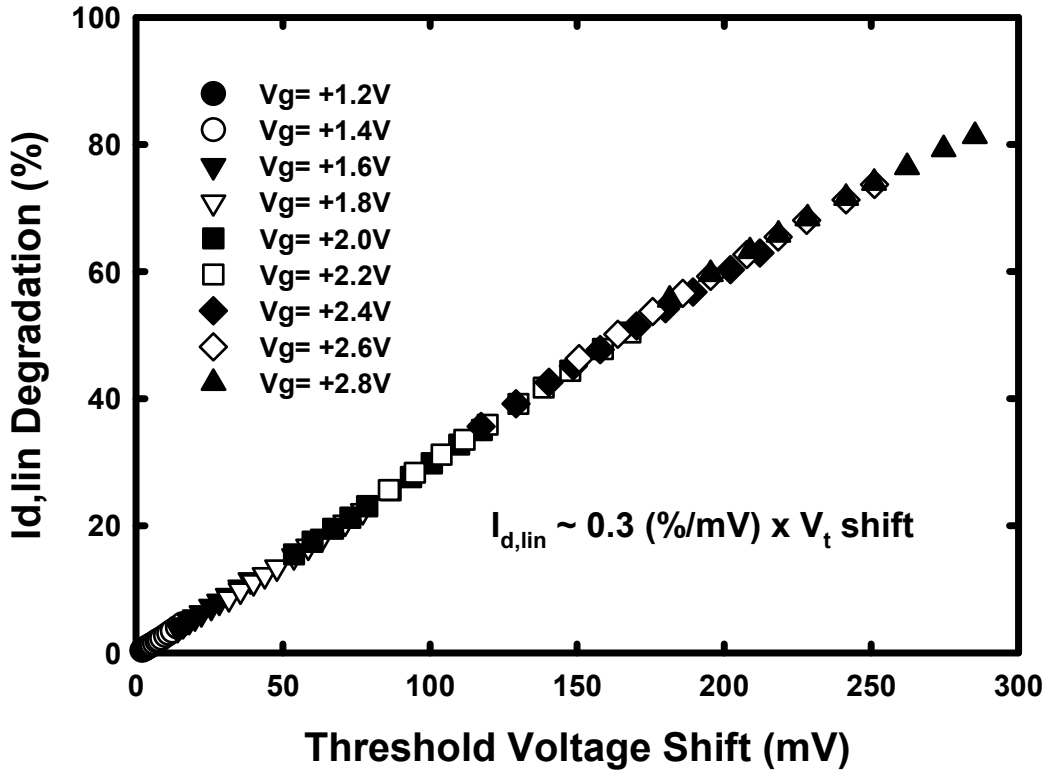


Fig. 3-5 Linear relationship between the threshold voltage shift and drain current degradation biased in the linear region. The increase of V_t is mainly responsible for the $I_{d,lin}$ degradation as that under static positive bias stress.

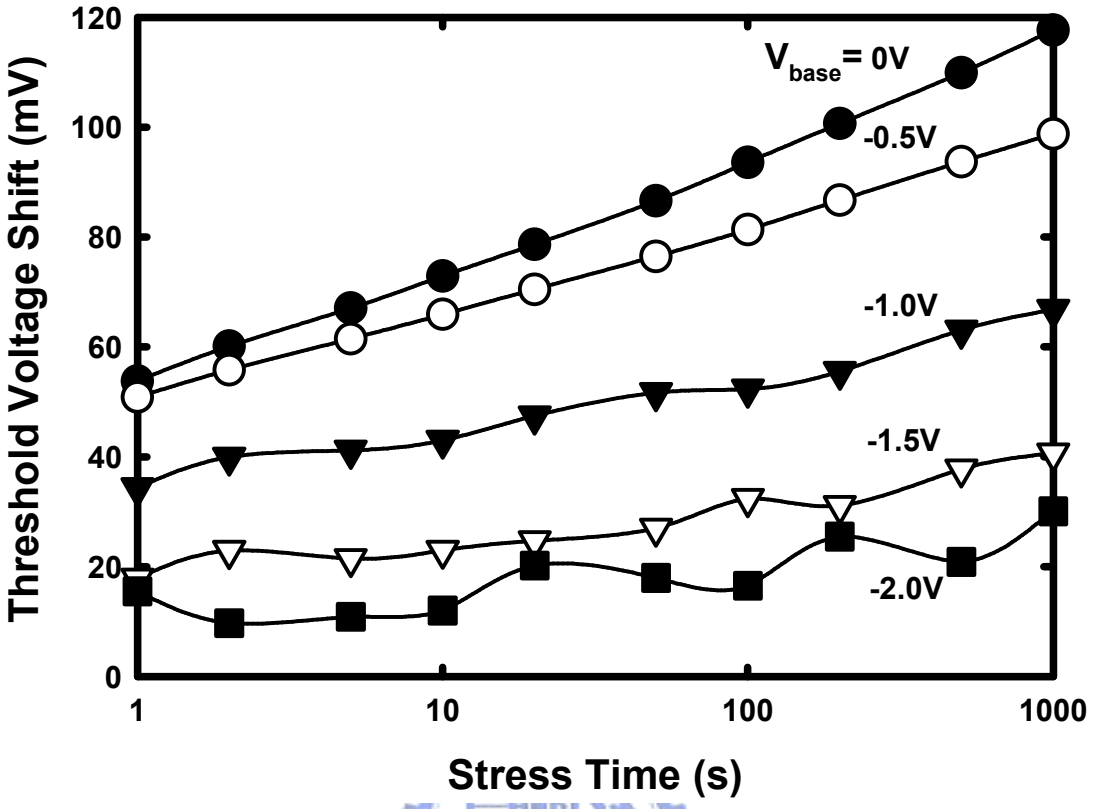


Fig. 3-6 Threshold voltage shift as a function of stress time under the bipolar dynamic stress at f= 100k Hz with fixed peak level voltage V_{peak}= +2.0 V and various base level voltages V_{base}= 0 ~ -2.0 V.

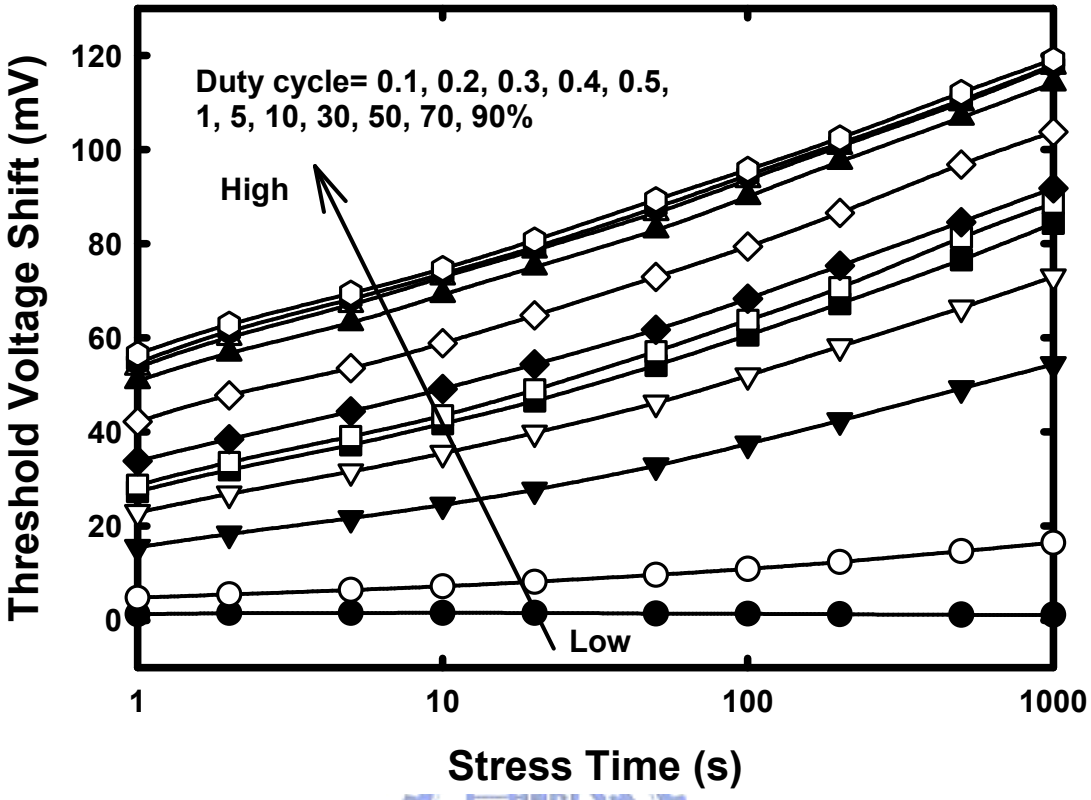


Fig. 3-7 Threshold voltage shift of the dual-layer HfO_2/SiO_2 high-k gate stack as a function of the stress time under dynamic positive bias stress with various duty cycles ranging from 0.1 to 90%. Negligible V_t shift could be observed at very small duty cycles ~0.1-0.2%.

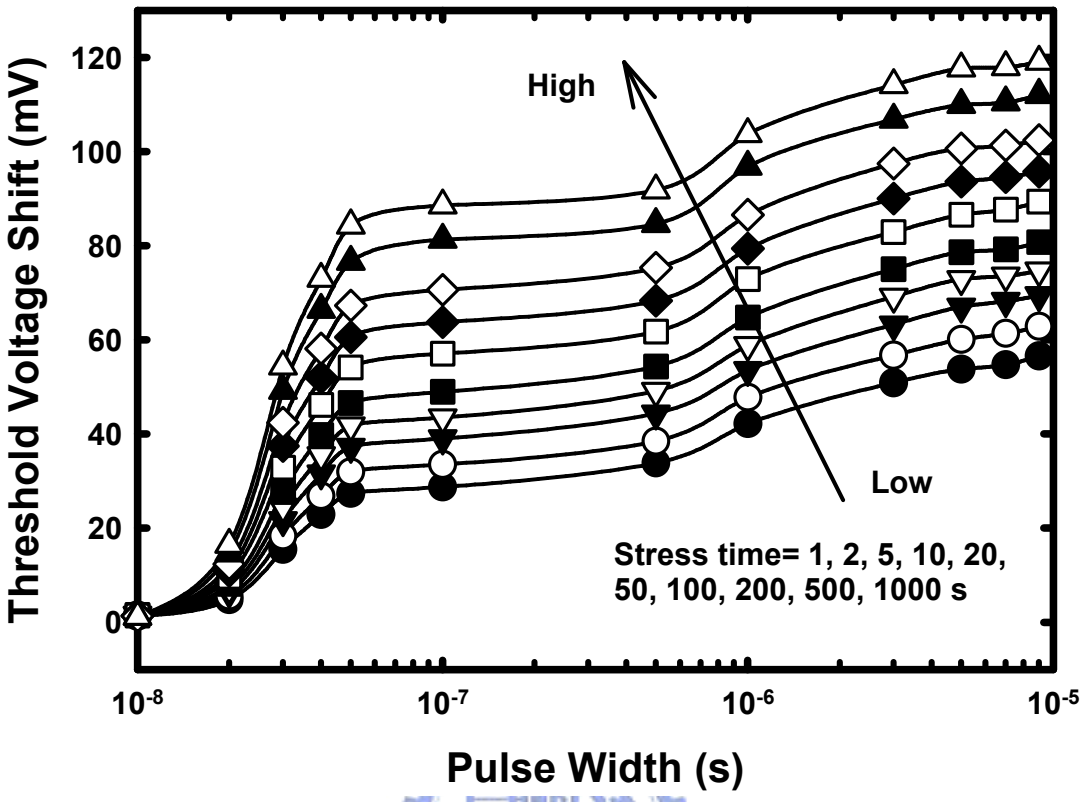


Fig. 3-8 Threshold voltage shift as a function of the pulse width of stress pulse waveform under dynamic positive bias stress (f= 100k Hz, V_{peak}= +2.0 V, and V_{base}= 0 V) at various stress times, where the pulse width is the pulse period multiplied by duty cycles.

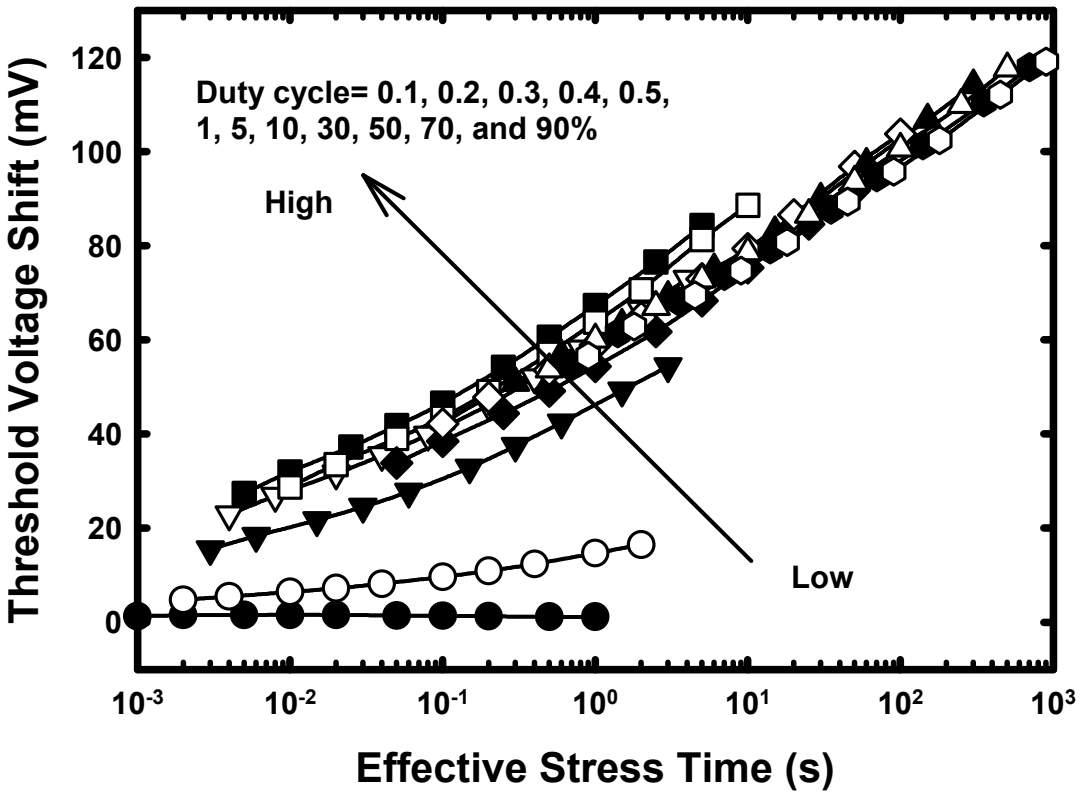


Fig. 3-9 Threshold voltage shift as a function of effective stress time under dynamic positive bias stress (f= 100k Hz, V_{peak}= +2.0 V, and V_{base}= 0 V) with various duty cycles, where the effective stress time is transformed from the stress time multiplied by duty cycles.

Chapter 4: Two-Frequency C-V Correction Method Using Five-Element Circuit Model for High-k Gate Dielectric and Ultrathin Oxide

4.1 Introduction

With the rapid progress of VLSI technologies, the gate dielectric thickness continues to scale down to keep the device performance in advanced progress. The gate dielectric capacitance of advanced MOSFET devices is of great importance for obtaining the equivalent oxide thickness (EOT), inversion layer charge, and interface state density. However, the tunneling leakage current through ultrathin gate oxides may lead to the difficulties in performing the quasi-static and typical 100k-Hz capacitance-voltage (C-V) characterizations. Although the problem of severe capacitance drop under large tunneling leakage current can be improved by measuring at higher frequencies (≥1M Hz), the influences of parasitic components on the measured dielectric capacitance must be taken into account at such high frequencies.

The series resistance R_s arising from well/substrate and contact resistance was first added to the parallel circuit model (C_p-G), and a two-frequency C-V correction method was proposed to extract the accurate dielectric capacitance from this three-element circuit model [4.1], [4.2]. In practice, the validity of this correction method seems to depend upon the two frequencies adopted and the device area. The applicability limits of this two-frequency C-V correction method had been further examined in terms of the frequency and device area selection guidelines [4.3]. Later, some researchers recommended that the dielectric energy absorption and other parasitic components should be considered as well. An improved two-frequency

method of capacitance measurement using a four-element circuit model was proposed for the $SrTiO_3$ high dielectric constant (high-k) dielectrics [4.4]. The shunt resistance was replaced by the loss tangent **tan**δ (or called the dissipation factor) due to the dynamic dielectric loss of high-k dielectrics, and series inductance L_s was added due to cables and the probing system. In addition, a new C-V correction method using another four-element circuit model to extract the EOT of ultrathin gate dielectrics with high gate leakage current was also proposed [4.5]. The shunt resistance R_p was to simulate the static dielectric loss from the gate leakage current, and the parasitic capacitance C_s in parallel with R_s was added due to the device structure, probe contact arrangement, and stray cable capacitance.

In this chapter, a new five-element circuit model has been proposed in section 4.3 to consider both the dielectric imperfections and the parasitic components, and this circuit model could also be transformed into another two four-element circuit models to simplify the analysis and calculations, depending on the gate leakage current. In section 4.4, the two-frequency C-V correction method using a 5-element circuit model will be used to correct the clamped and amplified C-V curves of low-leakage high-k gate dielectrics, and the area dependence of parasitic components will also be studied. Finally, in order to obtain the EOT of ultrathin oxides, the severe capacitance drop due to tunneling leakage current will be suppressed and corrected by measuring at high frequencies with two-frequency C-V correction in section 4.5.

4.2 Device Fabrication and Analysis Method

The fabrication process of the TiN/HfO_2/SiO_2/p-Si metal-oxide-semiconductor (MOS) capacitor is explained in detail as follows: after the definition of shallow trench isolations (STI), the base oxide SiO_2 (~1.0 nm) was thermally grown on

300-mm p-type silicon wafers. Then the HfO_2 (~3.2 nm) high-k gate dielectric was deposited using atomic layer deposition (ALD) technique, followed by rapid thermal annealing (RTA) to improve the dielectric quality. Finally, the mid-gap TiN metal gate electrode was deposited using physical vapor deposition (PVD) technique, and the gate stack was subsequently patterned using lithography and dry etching technologies.

The test structures used in this chapter are the simple MOS capacitors with two-terminal top gate and wafer backside contacts, and all the C-V measurements were performed using the Agilent 4284A precision LCR meter in parallel mode. In addition, the EOT of the TiN/HfO_2/SiO_2 high-k gate stack mentioned above was extracted to be 1.38 nm using the C-V simulation program which has taken the quantum effect into account [4.6].

4.3 General Circuit Model of Five Elements

Fig. 4-1(a) is the two-element parallel circuit model used for capacitance-voltage characterization in a typical impedance meter. However, this simple parallel circuit model may not be enough to describe the behavior of small-signal frequency response of ultrathin oxides and high-k gate dielectrics in various situations. Therefore, a more general circuit model of five elements as shown in Fig. 4-1(b) is proposed to be employed in the two-frequency C-V correction. In this five-element circuit model, C_0 is the ideal dielectric capacitance, R_p is the shunt resistance due to gate leakage current, $\tan\delta$ is the loss tangent due to dielectric energy absorption, R_s is the series resistance due to well/substrate and contact resistance, and L_s is the series inductance due to extension cables and the probing system. It seems to have two types of dielectric losses in a lossy MOS capacitor: one is the static dielectric loss due to the

actual flow of charge carriers, and the other one is the dynamic dielectric loss due to the local movements or vibrations of atoms or molecules in an alternating electric field.

Equating the real and imaginary parts of the total impedance in Figs. 4-1(a) and 4-1(b) results in two complicated equations:

$$\text{Real: } \frac{G}{G^2+\omega^2 C_p{}^2} = R_s + \frac{R_p(1+\tan^2\delta+\omega C_0 R_p \tan\delta)}{1+(\omega C_0 R_p+\tan\delta)^2} \tag{4.1}$$

$$\text{Imaginary: } \frac{C_p}{G^2+\omega^2 C_p{}^2} = -L_s + \frac{C_0 R_p{}^2}{1+(\omega C_0 R_p+\tan\delta)^2} \tag{4.2}$$

The above two equations could be simplified for easy algebraic operations if the criteria $\tan^2\delta << 1 << (\omega C_0 R_p)^2$ are satisfied:

$$\text{Real: } \frac{G}{G^2+\omega^2 C_p{}^2} = R_s + \frac{\tan\delta}{\omega C_0} + \frac{1}{\omega^2 C_0{}^2 R_p} \tag{4.3}$$

$$\text{Imaginary: } \frac{C_p}{G^2+\omega^2 C_p{}^2} = -L_s + \frac{1}{\omega^2 C_0} \tag{4.4}$$

If R_p is defined as V_g/I_g from the static I_g-V_g measurement since $R_p >> R_s$ is valid in most cases, the above criteria could be re-arranged as $\tan\delta < 0.1$ and $J_g < 0.01$ A/cm^2 for the quick verification. In addition, C_0 and the other three circuit elements could be easily solved from (4.3) and (4.4) with the known R_p by measuring C_p and G in parallel mode at two different frequencies[3]:

$$C_0 = \frac{(\omega_2{}^2-\omega_1{}^2)(G_1{}^2+\omega_1{}^2 C_{p1}{}^2)(G_2{}^2+\omega_2{}^2 C_{p2}{}^2)}{\omega_1{}^2\omega_2{}^2[C_{p1}(G_2{}^2+\omega_2{}^2 C_{p2}{}^2)-C_{p2}(G_1{}^2+\omega_1{}^2 C_{p1}{}^2)]} \tag{4.5}$$

As it comes to the high-k dielectrics with low gate leakage current, R_p could almost be regarded as infinity (open circuit), and the $\tan\delta$ in series with C_0 could be transformed into the equivalent one in parallel. This four-element circuit model as

[3] See appendix A for the details of equations to obtain the values of five circuit elements by the two-frequency C-V correction method.

shown in Fig. 4-1(c) is the one proposed by H. T. Lue *et al.* for $SrTiO_3$ high-k dielectrics [4.4]. Equations (4.3) and (4.4) can apply to their model if the $1/\omega^2C_0^2R_p$ term in (3) is deleted, and the same results were obtained from Lue's and our equations.

As it comes to ultrahin oxides or leaky high-k dielectrics, the static dielectric loss due to tunneling leakage current is much more significant than the dynamic one. This is the four-element circuit model for leaky MOS capacitors as shown in Fig. 4-1(d) [4.7]. Equations (4.3) and (4.4) can also apply to this model if the $\tan\delta/\omega C_0$ term in (3) is deleted. Sometimes, if the dielectric is too leaky, the criteria $1<<(\omega C_0R_p)^2$ and $R_p>>R_s$ may not be valid. The two equations from just equating the total impedance in Figs. 4-1(a) and 4-1(d) without any reduction should be employed to obtain C_0R_p first in similar ways as shown above, and then use this C_0R_p to obtain the C_0 and other circuit elements[4]:

$$C_0R_p = \frac{C_{p1}(G_2^2+\omega_2^2C_{p2}^2)-C_{p2}(G_1^2+\omega_1^2C_{p1}^2)}{G_1(G_2^2+\omega_2^2C_{p2}^2)-G_2(G_1^2+\omega_1^2C_{p1}^2)} \tag{4.6}$$

4.4 Corrections for the Amplified and Clamped C-V Curves in Low-Leakage High-k Gate Dielectrics

Figs. 4-2 and 4-3 show the measured and two-frequency corrected C-V curves of the $TiN/HfO_2/SiO_2/p$-Si MOS capacitors with gate areas of 10000 and 400 μm^2, respectively. It has been demonstrated that the frequency dispersion of clamped and amplified C-V curves at high frequencies (>500k Hz) can be effectively eliminated if the influences of parasitic components R_s and L_s are taken into account and that the value of each circuit element at a specific applied gate voltage could be independently

[4] See appendix B for the details of equations to obtain C_0R_p first and then C_0 and R_p of ultrathin oxides step by step.

determined from (4.3) and (4.4) for the given device as shown in the figures. The frequency dispersions of the clamped and amplified C-V curves have been extensively reported in previous studies [4.1]-[4.6], and this could be understood by formulating the measured parallel capacitance C_p as a function of the extracted circuit elements with similar reduction procedures:

$$C_p \approx \frac{(1-\omega^2 C_0 L_s)C_0}{(1-\omega^2 C_0 L_s)^2 + (\omega C_0 R_s)^2}. \quad (4.7)$$

Thus, the C_p at a specific frequency could be obtained from (4.7) with known parasitic components, and the calculated results at f= 500k and 1M Hz are consistent with the measured frequency dispersions in Figs. 4-2 and 4-3. Thus the clamped and amplified C-V curves could be well explained by considering the influences of the series resistance R_s and series inductance L_s.

Note that the **tan**δ is ~0.3-0.35% and is independent of the gate area, and this dynamic dielectric loss might be a intrinsic materials issue. It has been reported that **tan**δ is ~3% in $BaSrTiO_3$ high-k dielectrics and can be improved to 1% with the appropriate doping of Al_2O_3 [4.7]. In general, the tanδ is defined as ϵ_i/ϵ_r by considering the dielectric permittivity as a complex number $\epsilon = \epsilon_r + j\epsilon_i$. Or the tanδ can also be defined as the ratio of the dynamic energy loss to the energy stored inside the capacitor in the viewpoint of circuit level. The physical origin of this dielectric energy absorption in Hf-based high-k dielectrics could be attributed to the local molecular vibration of the flexible Hf-O bondings in an alternating electric field.

The parasitic components such as the series resistance R_s and series inductance L_s exhibit significant area dependences (R_s~1/area$^{1/2}$ [4.8] and L_s~1/area) as shown in the two insets in Figs. 4-2 and 4-3. The R_s could be attributed to the well/substrate and contact resistance, and this speculation has been confirmed by the same R_s extracted

from the high-k gate stacks with different EOT values. In addition, the area dependence of R_s can be explained by considering the electric flow lines from the small top gate electrode on the flat surface of a semi-infinite substrate to the wafer backside contact as shown in Fig. 4-4. This situation is similar to that of measuring the spreading resistance $R_{sp} \sim \rho/2a$, where R_{sp} is the spreading resistance (ohm), ρ is the substrate resistivity (ohm-cm), and *a* is the probe radius (cm). Moreover, the area dependence of L_s is attributed to the phase compensation problems between the measurement signal voltage V_m and signal current I_m, particularly in the connection scheme of probing through the chuck with switch matrix. When the wafer chuck and switch matrix are employed in the probing system, the unequal signal path lengths from the Hi and Lo terminals of Agilent 4284A precision LCR meter may lead to the phase shift problems of the measurement signal current I_m ($I_m = C\frac{dV_m}{dt} \sim Area$), and part of the capacitive signal current could be recognized as the inductive signal current by the impedance meter ($V_m = L\frac{dI_m}{dt}$, $L \sim \frac{1}{C} \sim \frac{1}{Area}$). This may explain the root cause of the L_s area dependence and why the L_s is inversely proportional to C_p as shown in Fig. 4-5.

4.5 Corrections for the Capacitance Drop in Ultrathin Oxides

Fig. 4-6 shows the measured, two-frequency corrected, and theoretical C-V curves of the ultrathin oxynitride with EOT= 1.65 nm. Although the severe capacitance drop could not be completely recovered, adopting two high frequencies in the two-frequency C-V correction using (4.6) could obtain the corrected C-V curve more close to the theoretical one. Then, the C-V simulation program considering both the poly-depletion and quantum effects [4.6] is used to perform the curve fitting at the

overlapping transition region. This may provide a simple and practical approach to extract the EOT of the ultrathin oxides. Since the influences of the parasitic components R_s and L_s have been eliminated by the two-frequency C-V correction using the 4-element (C_0, R_p, R_s, and L_s) circuit model, the severe capacitance drop in ultrathin oxides may result from the decrease of the accumulation charge due to the large tunneling leakage current. One possible solution is to use higher measurement frequencies (shorter period) to reduce the impacts of the tunneling gate leakage. Instruments which provide wider frequency range (e.g., Agilent 4294A precision impedance analyzer, freq= 40 to 110 MHz) are strongly suggested to be accompanied with the two-frequency C-V correction method to eliminate the influences of the parasitic components and tunneling leakage current simultaneously. In addition, radio-frequency (RF) C-V measurement and short channel devices are also highly suggested to be accompanied with the above method [4.9], [4.10].

4.6 Summary

A general circuit model of five elements has been proposed to solve the problem of accurate capacitance extraction from ultrathin oxide or high-k dielectric MOS capacitors. This circuit model can simulate the imperfections of the MOS capacitors (static and dynamic energy losses) and the parasitic components (series resistance R_s and series inductance L_s). The value of each circuit element can be readily extracted from the two-frequency C-V correction and static I_g-V_g measurements if the criteria $\tan^2\delta << 1 << (\omega C_0 R_p)^2$ and $R_s << R_p$ are well satisfied. This five-element circuit model can also be transformed into another two four-element circuit models to further simplify the analysis and calculations, depending on the level of gate leakage current. In addition, the two-frequency C-V correction method using 5-element circuit model

can effectively eliminate the frequency dispersion of the clamped and amplified C-V curves for low leakage high-k dielectrics, and this C-V correction method can also improve the capacitance drop of ultrathin oxides to an acceptable level in order to perform the curve fitting using a C-V simulation program. This technique could be readily integrated into the routine C-V measurements since only simple algebraic operations are needed.

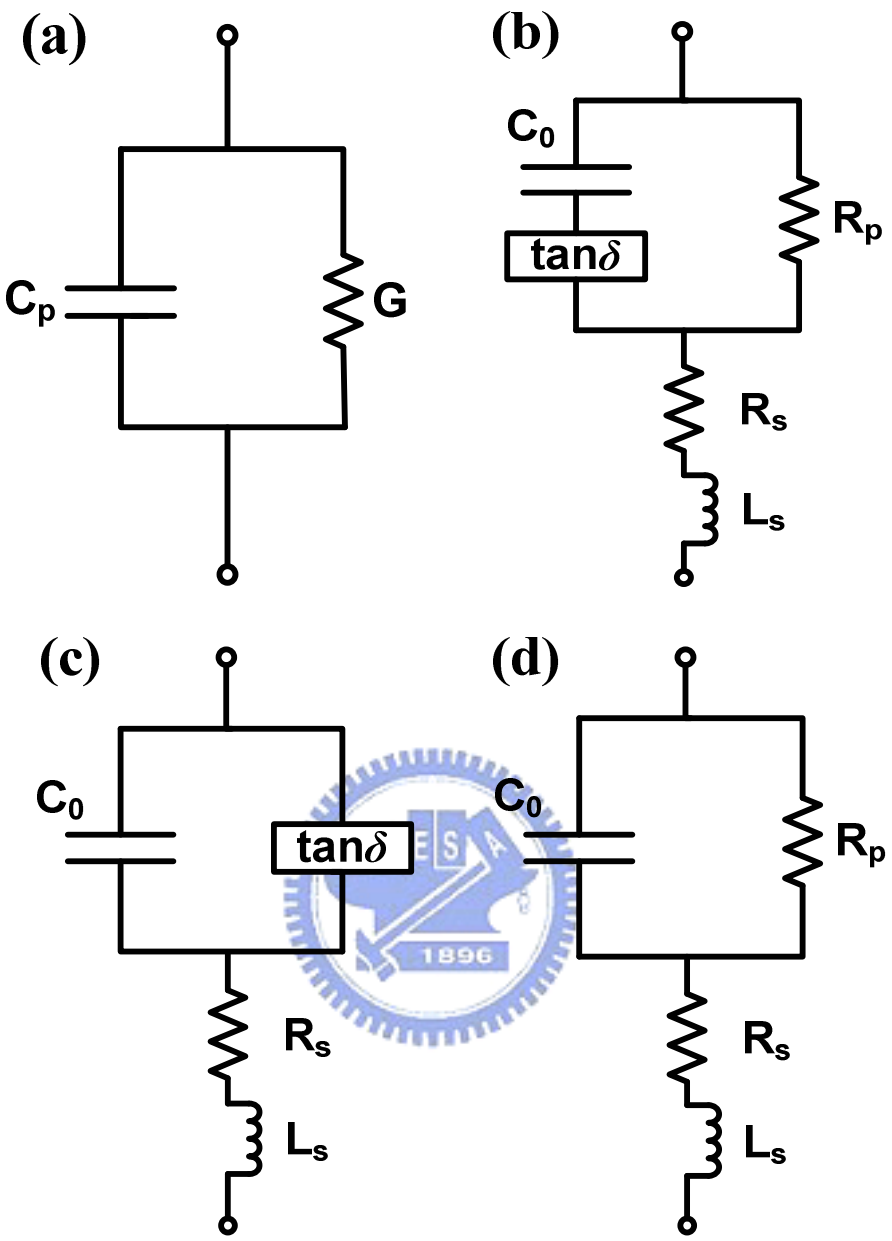


Fig. 4-1 Small-signal equivalent circuit models of MOS capacitors: (a) simple parallel circuit model, (b) new five-element circuit model, (c) four-element circuit model for low leakage high-k dielectrics, and (d) four-element circuit model for ultrathin oxides and leaky high-k dielectrics.

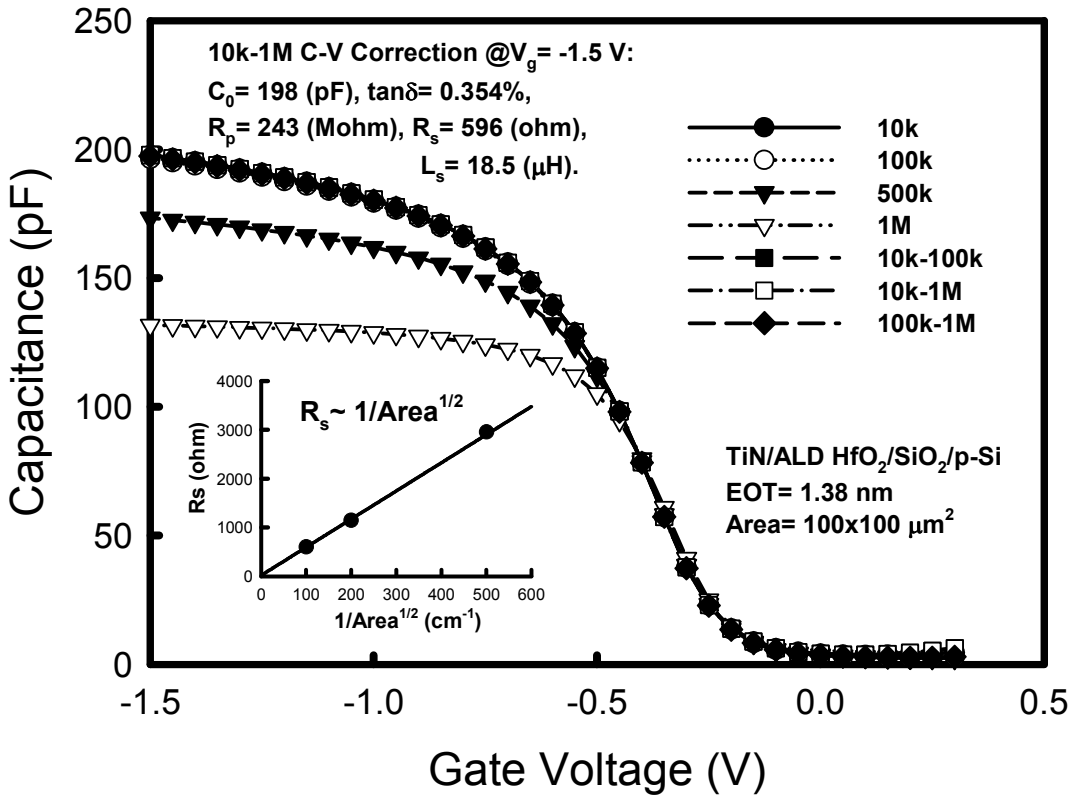


Fig. 4-2 Measured and two-frequency corrected C-V curves of the TiN/HfO_2/SiO_2/p-Si MOS capacitor with gate area of 10000 μm^2. The frequency dispersion of clamped C-V curves could be observed at high frequencies (>500k Hz).

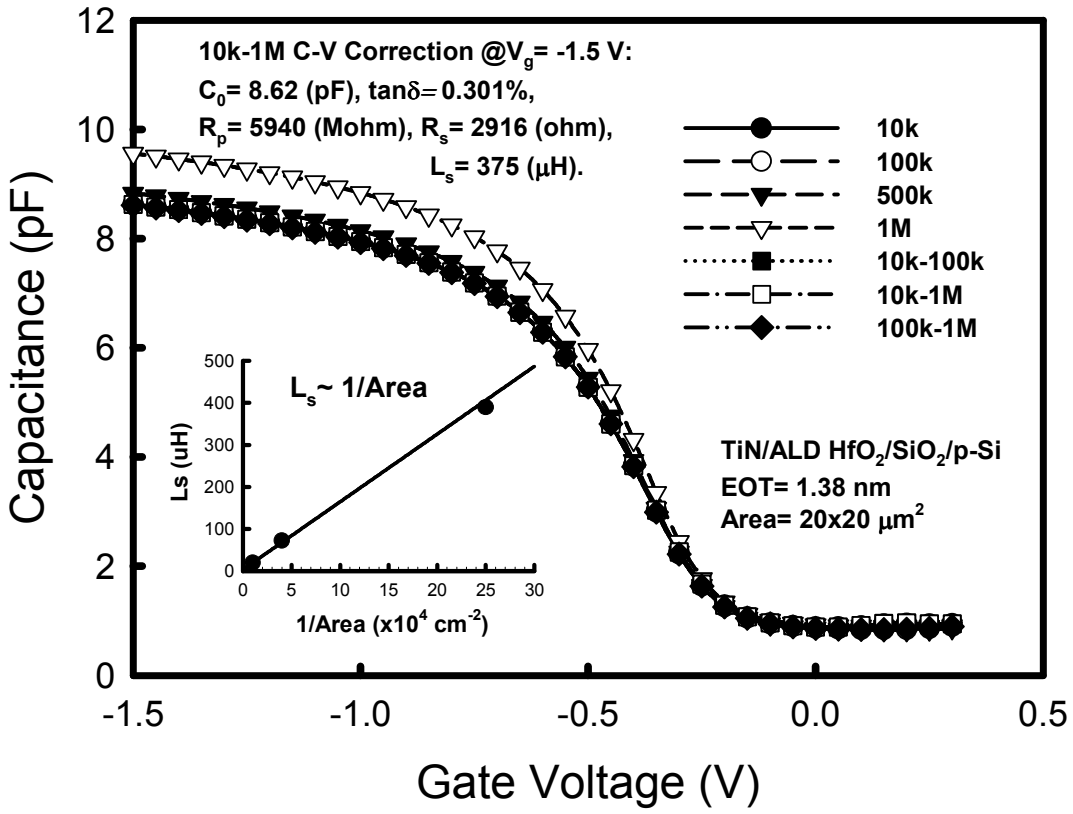


Fig. 4-3 Measured and two-frequency corrected C-V curves of the TiN/HfO_2/SiO_2/p-Si MOS capacitor with gate area of 400 μm^2. The frequency dispersion of amplified C-V curves could be observed at high frequencies (>500k Hz).

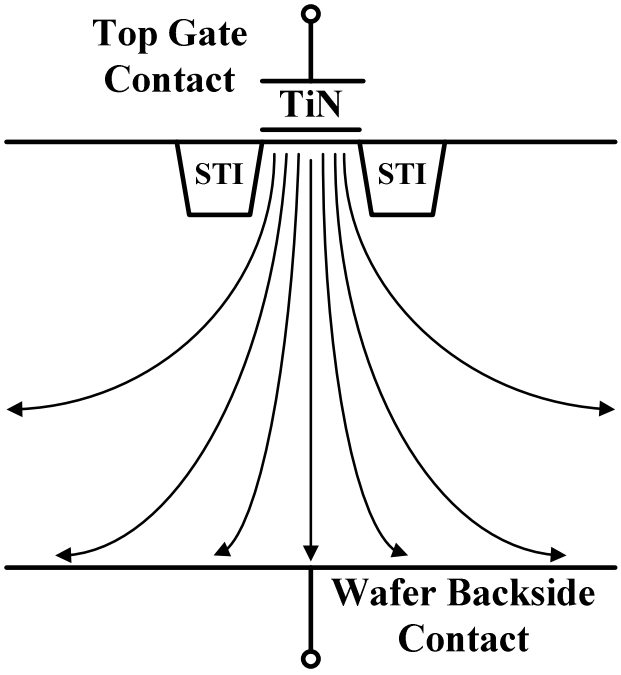


Fig. 4-4 Electric flow lines from the small top-gate contact on the flat surface of a semi-infinite substrate to the large wafer backside contact. This situation is similar to that of measuring the spreading resistance.

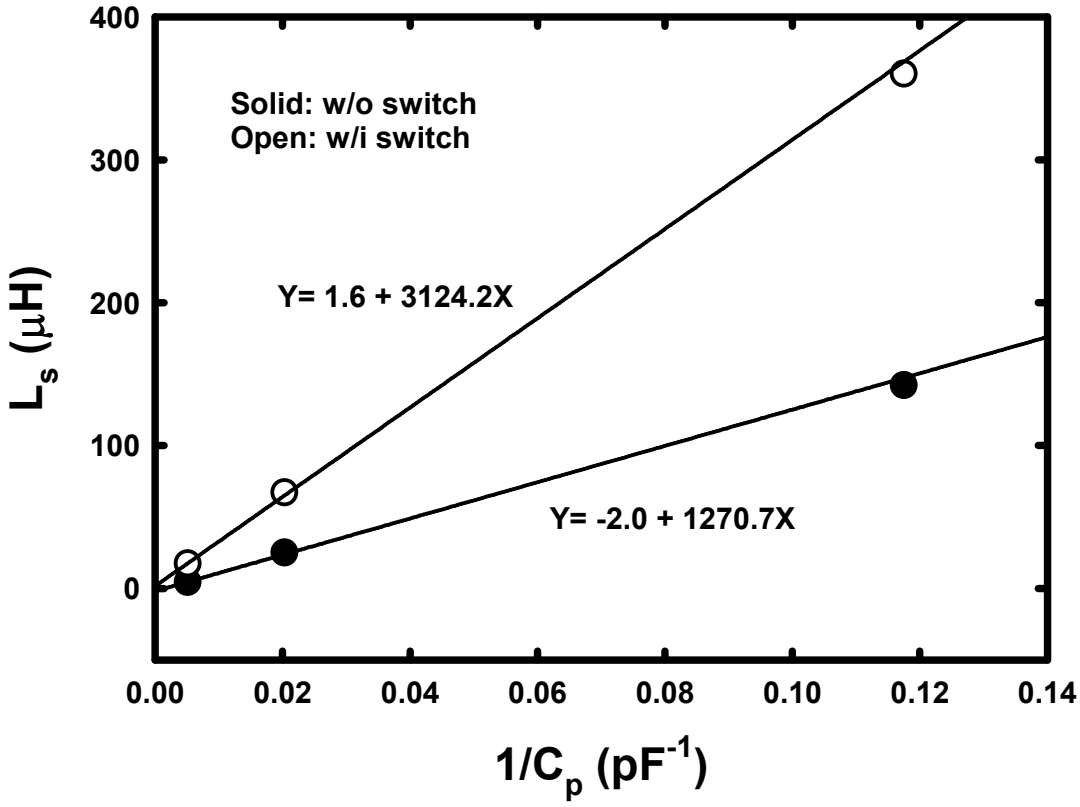


Fig. 4-5 Linear relationship between the L_s and $1/C_p$ in the connection schemes with/without switch matrix. Larger L_s would be observed when probing through the chuck with switch matrix due to the phase compensation problems.

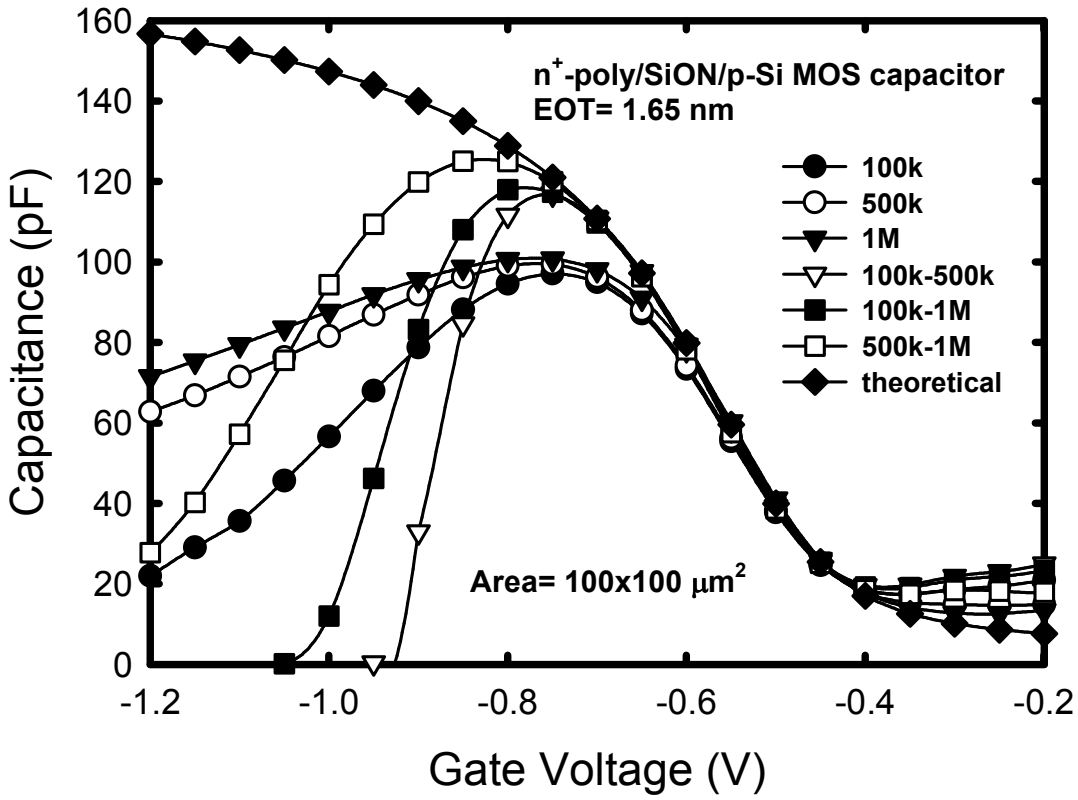


Fig. 4-6 Measured, two-frequency corrected, and theoretical C-V curves of the ultrathin oxynitride with EOT= 1.65 nm. Adopting two high frequencies in the two-frequency C-V correction and then using the C-V simulation program to perform the curve fitting may provide a simple and practical way to extract the EOT of ultrathin oxides.

Chapter 5: Space and Energy Distribution of Border Traps in the Dual-Layer HfO_2/SiO_2 High-k Gate Stack by Low-Frequency Capacitance-Voltage Measurement

5.1 Introduction

Compared to the threshold voltage instability determined by C-V hysteresis or static I_d-V_g characteristics in chapters 2 and 3, transient threshold voltage shift has been reported to be much more significant by using the pulse I_d-V_g technique with reduced switching and measurement time delays [5.1], [5.2]. This problem can be addressed by considering the different charge trapping and de-trapping kinetics of fast and slow high-k bulk traps in the time scales ranging from μsec to sec. Since the trapped charge carriers in the fast high-k traps could be instantly emitted into the Si conduction band during the transition delay between the stress/measure cycles or within the static C-V or I-V sweeps, the impact of charge trapping on device performance might be greatly underestimated or overestimated if not considering the contribution of fast high-k traps, thus leading to the faulty conclusion of device lifetime. Therefore, the lifetime projection made by static or pulse I-V technique may not be appropriate to reflect the actual operation conditions in the circuit level. For instance, the transient charging effect has been demonstrated to be negligible or significantly improved in the high-speed digital circuits such as ring oscillator or single-stage inverter [5.3].

The transient charging and discharging effects may originate from the direct tunneling between the injected charge carriers and pre-existing high-k bulk traps located near the high-k/base oxide interface. The direct tunneling model through the

thin base oxide is similar to that of tunneling into the near-interface oxide traps that has already been studied and proposed [5.4]-[5.6]. These near-interface oxide traps are defined as the oxide traps located near the SiO_2/Si interface that can instantly exchange charge carriers with the underlying Si substrate through direct tunneling and are designated as "border traps" to be distinguished from the interface states and fixed oxide traps. These border traps have also been reported to be highly associated with the low-frequency (1/f) noise level and radiation response in MOS transistors with conventional SiO_2 or SiON gate oxides [5.7]-[5.9].

In this chapter, it is found that the border traps in Hf-based high-k gate dielectrics could be detected by low-frequency capacitance-voltage (C-V) measurement, and this border trap capacitance is highly related to the measurement frequency and applied gate voltage. An elastic direct tunneling model through trapezoidal potential barriers has been proposed to profile the space and energy distribution of the border traps in the dual-layer HfO_2/SiO_2 high-k gate stacks.

5.2 Device Fabrication and Analysis Method

In this chapter, simple TiN/HfO_2/SiO_2/n-Si metal-oxide-semiconductor (MOS) capacitors with two-terminal top gate and backside contacts are used as the devices under testing (DUT). The fabrication process is explained in detail as follows. After the definition of shallow trench isolations (STI), the base oxide (~1.0 nm) was thermally grown on 300-mm n-type silicon wafers. Then the HfO_2 and HfSiO (3.2~ 4.5 nm) high-k gate dielectrics were deposited using atomic layer deposition (ALD) technique, followed by the rapid thermal annealing (RTA) in oxygen ambient to improve the dielectric quality. Finally, the mid-gap TiN metal gate electrode was deposited using physical vapor deposition (PVD) technique, and then the gate stack

was patterned using lithography and dry etching technologies.

Since the test structures used in this chapter are the simple MOS capacitors with two-terminal top gate and wafer backside contacts, the connection scheme of probing through the chuck (not probing directly to the wafer surface) must be used, and all the C-V measurements were performed using the Agilent 4284A precision LCR meter in parallel mode. Therefore, in order to obtain the accurate dielectric capacitance, the two-frequency C-V correction method in chapter 4 was employed to eliminate the unwanted influences of parasitic components at high measurement frequencies. In addition, the EOT of the HfO_2/SiO_2 high-k gate stack was extracted using the C-V simulation program which has taken the quantum effect into account [5.10].

5.3 Border Trap Capacitance at Low Frequencies

Fig. 5-1 shows the capacitance-voltage characteristics of the $TiN/HfO_2/SiO_2/n$-Si MOS capacitor with gate area of 10000 μm^2 measured and corrected at various frequencies. The dielectric capacitance increase at low frequencies could be clearly observed in the strong accumulation region, and the dielectric capacitance measured at low frequencies seems to increase with the decrease of measurement frequency and the increase of applied gate bias voltage. In order to eliminate the influences of the parasitic components on the measured dielectric capacitance, the two-frequency C-V correction method using a 5-element circuit model explained in chapter 4 was employed in the high-frequency C-V curves (≥500 kHz) to extract the substrate/well resistance R_s and external inductance L_s, which were found to be 240 (ohm) and 22 (μH), respectively. Then, it can be demonstrated that such parasitic components are insignificant to the measured dielectric capacitance C_p at frequencies lower than 500 kHz, as can be seen from the formulation of C_p as a function of the measurement

frequency, the ideal dielectric capacitance C_0, and the parasitic components ($C_p \sim \frac{C_0(1-\omega^2 C_0 L_s)}{(1-\omega^2 C_0 L_s)^2 + (\omega C_0 R_s)^2}$). In addition, the dielectric capacitance increase at low frequencies could not be observed in conventional SiO_2 or SiON gate dielectrics even with the tunneling leakage current density much higher than that of the above mentioned high-k gate stack (J_g@V_g= +2.5 V is merely 8.31x10^{-2} A/cm^2). The inset shows the dominant carrier transport mechanisms are ohmic conduction and Frenkel-Poole emission under low and high electric fields, respectively, therefore suggesting the trap-assisted carrier conduction process in the dual-layer HfO_2/SiO_2 high-k gate stack.

The dielectric capacitance increase at low frequencies could be explained by proposing a frequency- and voltage-dependent border trap capacitance C_{bt} in parallel with the ideal dielectric capacitance C_0 as shown in the inset of Fig. 5-2. If the charging and discharging of the border traps in the HfO_2 high-k dielectric can immediately follow the small-signal frequency, these border traps could contribute an additional dielectric capacitance C_{bt}. Moreover, the C_0 can be obtained by measuring at high frequencies (≥500 kHz) with appropriate correction of parasitic components since the C_{bt} is negligible at such high frequencies. Fig. 5-2 shows the extracted border trap capacitance C_{bt} as a function of measurement frequency under various gate bias voltages, and these frequency and voltage dependences of C_{bt} can be transformed into the relations corresponding to the tunneling distance from the Si substrate surface and the trap energy depth from the HfO_2 conduction band edge, respectively. These findings are similar to those of near-interface oxide traps observed by low-frequency charge pumping technique or the transient capacitance signal by tunneling deep-level transient spectroscopy (T-DLTS) [5.11]-[5.13].

In order to verify the assumption of the border trap capacitance C_{bt}, low-frequency C-V measurements of the Hf-based high-k gate stack with various gate areas and Si compositions in the HfSiO film have been studied extensively. Fig. 5-3 shows the multi-frequency C-V curves of the TiN/HfO_2/SiO_2/n-Si MOS capacitors with gate areas of (a) 400 and (b) 2500 μm^2. As can be seen, the dielectric capacitance increase at low frequencies still exhibit similar frequency and voltage dependences as the one with gate area of 10000 μm^2 as shown in Fig. 5-1. Moreover, Fig. 5-4 shows that the border tarp capacitance C_{bt} extracted at V_g= +1.0, +1.5, and +2.0 V and f= 1k and 1M Hz are linearly proportional to the gate area. Fig. 5-5 illustrates the multi-frequency C-V curves of the Hf-based high-k gate stack with (a) pure HfO_2, (b) low Si composition in the HfSiO film, and (c) high Si composition in the HfSiO film. The dielectric capacitance increase at low frequencies seems to be highly associated with the Si composition in the HfSiO film, and it is generally agreed that the appropriate Si incorporation into Hf-based high-k dielectrics could effectively reduce the trap density in the Hf-based high-k dielectrics. These findings are well consistent with our assumption that the capacitance increase at low-frequency C-V curves could be attributed to the existence of the border tarp capacitance C_{bt} which is in parallel with the ideal gate dielectric capacitance C_0. Note that the dielectric capacitance increase of Hf-based high-k gate dielectrics at low frequencies could not only be observed in the high-k MOS capacitors with n-type Si substrate biased in strong accumulation region but also in the high-k nMOSFETs biased in strong inversion region as shown in Fig. 5-6. In other words, the charge carriers tunneling through the thin base oxide must be electrons due to their smaller effective mass and energy barrier height as compared to holes. It should be noted that the MOS capacitors with conventional SiO_2 or SiON as gate dielectric do not exhibit similar capacitance increase at low frequencies because

the amount of border traps in these oxide-based dielectrics are not as many to be detectable. These findings could further support the assumption that the dielectric capacitance increase at low frequencies is attributed to the contribution of border traps in the Hf-based high-k gate dielectrics.

5.4 Physical Model of Elastic Direct Tunneling through Trapezoidal Potential Barriers

Similar to the interface state capacitance C_{it}, the border trap capacitance C_{bt} may result from an equivalent surface density of border traps D_{bt} ($cm^{-2}eV^{-1}$), which is the integration of the border trap volume density from the base oxide thickness x_1 to the maximum tunneling distance x_{max} in the HfO_2 high-k dielectric if the density of border traps is negligible in the thermally-grown base oxide:

$$C_{bt} = qA_G \int_{x_1}^{x_{max}} N_{bt}(x, E_t)dx \tag{5.1}$$

where q is the electron charge, A_G is the gate area, and N_{bt} is the border trap volume density ($cm^{-3}eV^{-1}$) as a function of the tunneling distance x and trap energy depth E_t. Furthermore, it has been proved in Fig. 5-4 that C_{bt} is linearly proportional to the gate area as proposed in the physical model.

Fig. 5-7 shows the schematic band diagram of the TiN/HfO_2/SiO_2/n-Si MOS capacitor biased in the accumulation region with the illustration of tunneling distance and carrier energy coordinates. Assume that the charging and discharging of the border traps mainly occur at the Si conduction band edge through elastic direct tunneling[5] and that the border traps are widely distributed over a defect band, not

[5] The assumption of elastic direct tunneling is the fundamental basis to derive the space and energy distribution of border traps. Since elastic direct tunneling occurs at a single energy level, it allows us to perform the energy scan of border traps inside the high-k dielectrics. However, if there is any thermal transition among different energy levels, it may lead to inaccurate energy distribution of border traps.

merely at a single energy level, in the HfO_2 high-k dielectrics [5.1]. Then the trap energy depth E_t from the HfO_2 conduction band edge could be approximately obtained under various gate bias voltages if the two-band structure (SiO_2 and HfO_2) with trapezoidal potential barriers is assumed by neglecting the field re-distribution due to the trapped charge:

$$E_t(x,\varepsilon) = \phi_{c2} - q\varepsilon_1 x_1 - q\varepsilon_2 (x - x_1) \tag{5.2}$$

where Φ_{c2} (1.9 eV) is the conduction band offset of HfO_2 [5.14], ε_1 and ε_2 are the electric fields in the SiO_2 and HfO_2 dielectrics, respectively, and x_1 is the base oxide thickness (0.8 nm). Assume the above tunneling transition is an elastic tunneling process with symmetric forward and reverse tunneling probability, and then the tunneling time constants between the available Si conduction band states and localized border traps should be equal to or less than a quarter of the measurement period 1/f:

$$\frac{1}{4f} = \tau_0 \exp\left(2\int_0^{x_1} \frac{\sqrt{2m_1^*(\phi_{c1} - q\varepsilon_1 x')}}{\hbar} dx' + 2\int_{x_1}^{x} \frac{\sqrt{2m_2^* E_t(x',\varepsilon)}}{\hbar} dx'\right) \tag{5.3}$$

where f is the measurement frequency, τ_0 is the pre-exponential factor (~10^{-10} sec) which is relatively insensitive to the tunneling distance and trap energy depth [5.15], ħ is the reduced Planck constant, Φ_{c1} (3.1 eV) is the conduction band offset of SiO_2, and m_1^* (0.42 m_0) and m_2^* (0.18 m_0) are the effective mass of electrons in SiO_2 and HfO_2, respectively [5.4], [5.14]. Subsequently, the maximum tunneling distance x_{max} that can be reached during the measurement cycle could be extracted from (5.3) with the given parameters above. Finally, the space and energy distribution of the border trap volume density could also be obtained as follows:

$$N_{bt}(x,E_t) = \frac{-2\sqrt{2m_2^* E_t(x,\varepsilon)}}{qA_G\hbar} \frac{dC_{bt}}{d\ln(f)} \tag{5.4}$$

5.5 Space and Energy Distribution of Border Traps

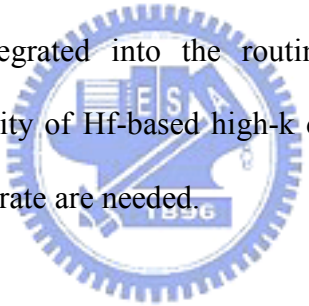
Multi-frequency C-V measurements were first performed to obtain the border trap capacitance C_{bt} as the difference between the measured dielectric capacitances at a specific frequency (<1M Hz) and at f= 1M Hz (two-frequency C-V correction should be employed if the frequency is higher than 500k Hz). Then, the trap energy depth from the HfO_2 conduction band edge could be obtained from (5.2) if the applied electric fields across the SiO_2 amd HfO_2 dielectrics and the tunneling distance x are known. The tunneling distance from the Si substrate surface that can be reached within the measurement period could be obtained from (5.3) by using an elastic direct tunneling model with symmetric forward/reverse tunneling time constant. Finally, the border trap volume density N_{bt} from (5.4) could be profiled in a truly three-dimensional coordinates as a function of the tunneling distance and trap energy depth.

Fig. 5-8 shows the space and energy distribution of border trap volume density N_{bt} (~10^{18}-10^{20} $cm^{-3}eV^{-1}$) in the dual-layer HfO_2/SiO_2 high-k gate stack. Symbols are model-extracted data points, and 3D-mesh is the smoothed surface profiling of these points. As the tunneling distance reaches the HfO_2 high-k dielectrics (x >0.8 nm), N_{bt} begins to increase gradually and eventually becomes saturated. Furthermore, N_{bt} increases exponentially with the decrease of the trap energy depth, and it appears that N_{bt} is insensitive to the tunneling distance inside the high-k bulk layer. These results suggest that most of the pre-existing high-k traps are located in the HfO_2 bulk layer and that considerable parts of these traps are positioned at the shallow energy levels.

5.6 Summary

Dielectric capacitance increase of the dual-layer HfO_2/SiO_2 high-k gate stack has

been observed in the low-frequency C-V curves. This strange phenomenon could be well explained by proposing a frequency- and voltage-dependent border tarp capacitance in parallel with the ideal dielectric capacitance as long as the transient charging and discharging of these border tarps could immediately follow the measurement frequency. In addition, these frequency and voltage dependences of the border trap capacitance could be transformed into the relations corresponding to the tunneling distance from Si substrate surface and the trap energy depth from HfO_2 conduction band edge using an elastic tunneling model between the Si conduction band states and localized border traps through trapezoidal potential barriers. Based on this physical model, the space and energy distribution of border trap volume density in the HfO_2 high-k dielectric could be profiled as a smoothed 3D-mesh. This technique can be easily integrated into the routine measurement and analysis procedure to monitor the quality of Hf-based high-k dielectrics since only the MOS capacitors with n-type Si substrate are needed.



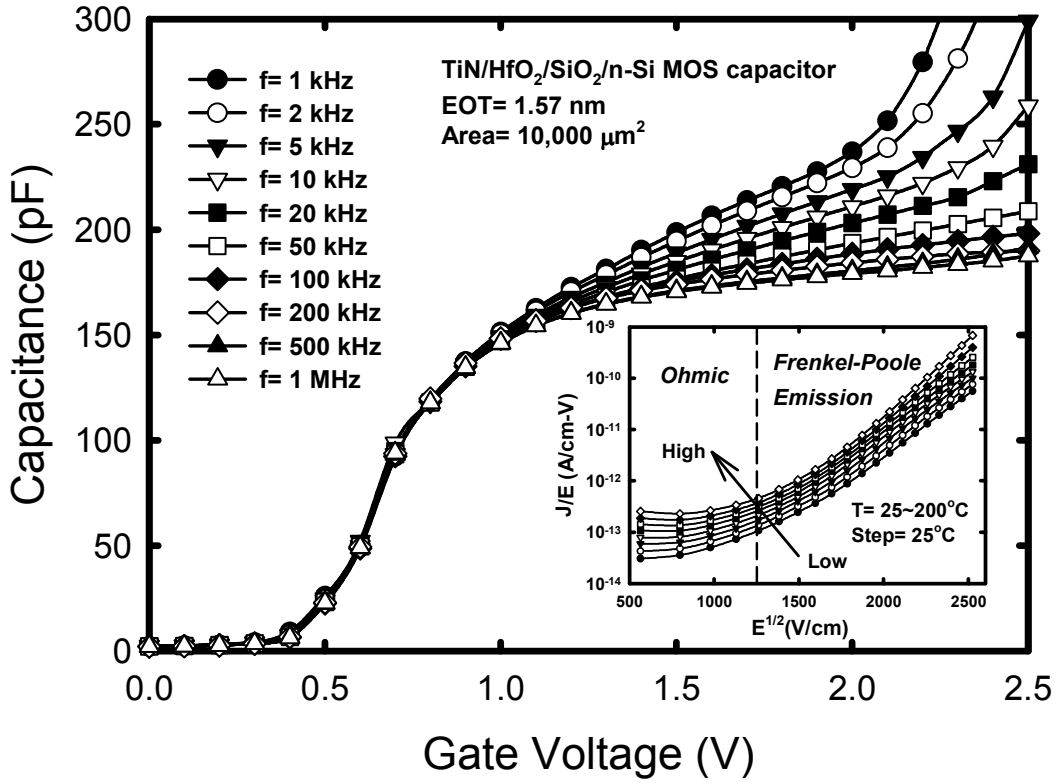


Fig. 5-1 Capacitance-voltage curves of the TiN/HfO_2/SiO_2/n-Si MOS capacitor at various frequencies with gate area of 10000 μm^2. The inset shows that the carrier transport mechanisms of injected substrate electrons are ohmic conduction and Frenkel-Poole emission under low and high electric fields, respectively.

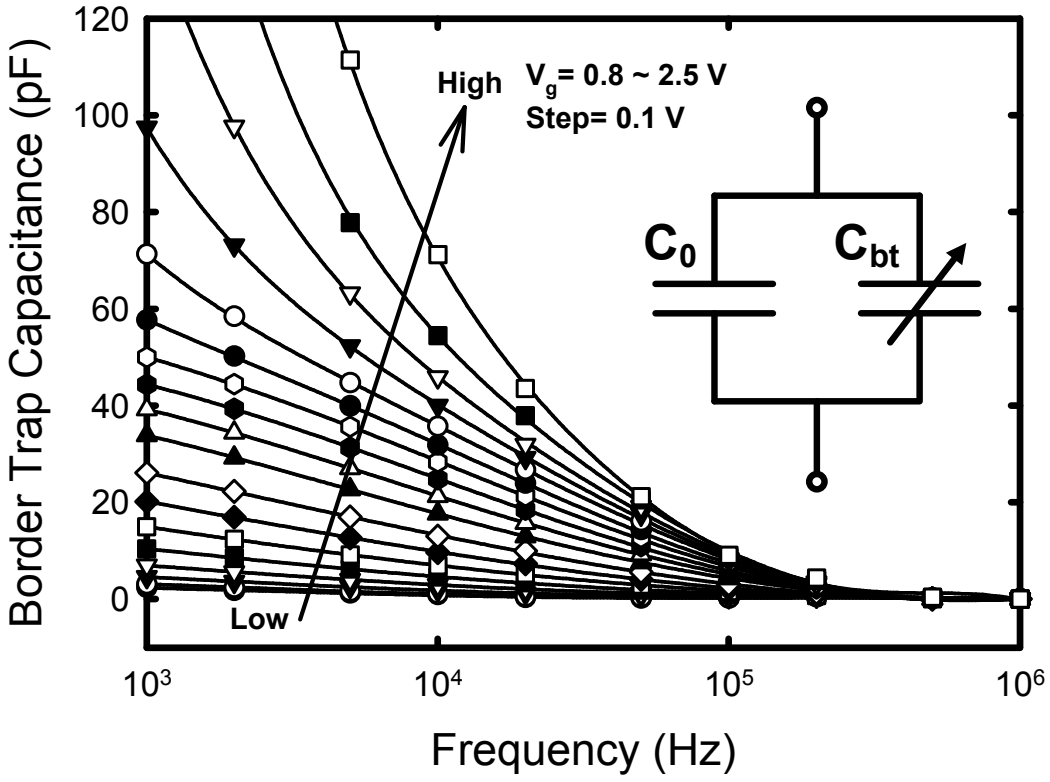


Fig. 5-2 Border trap capacitance as a function of the measurement frequency at various gate bias voltages. The dielectric capacitance increase at low frequencies could be explained by proposing a frequency- and voltage-dependent border trap capacitance in parallel with the ideal gate dielectric capacitance as shown in the inset.

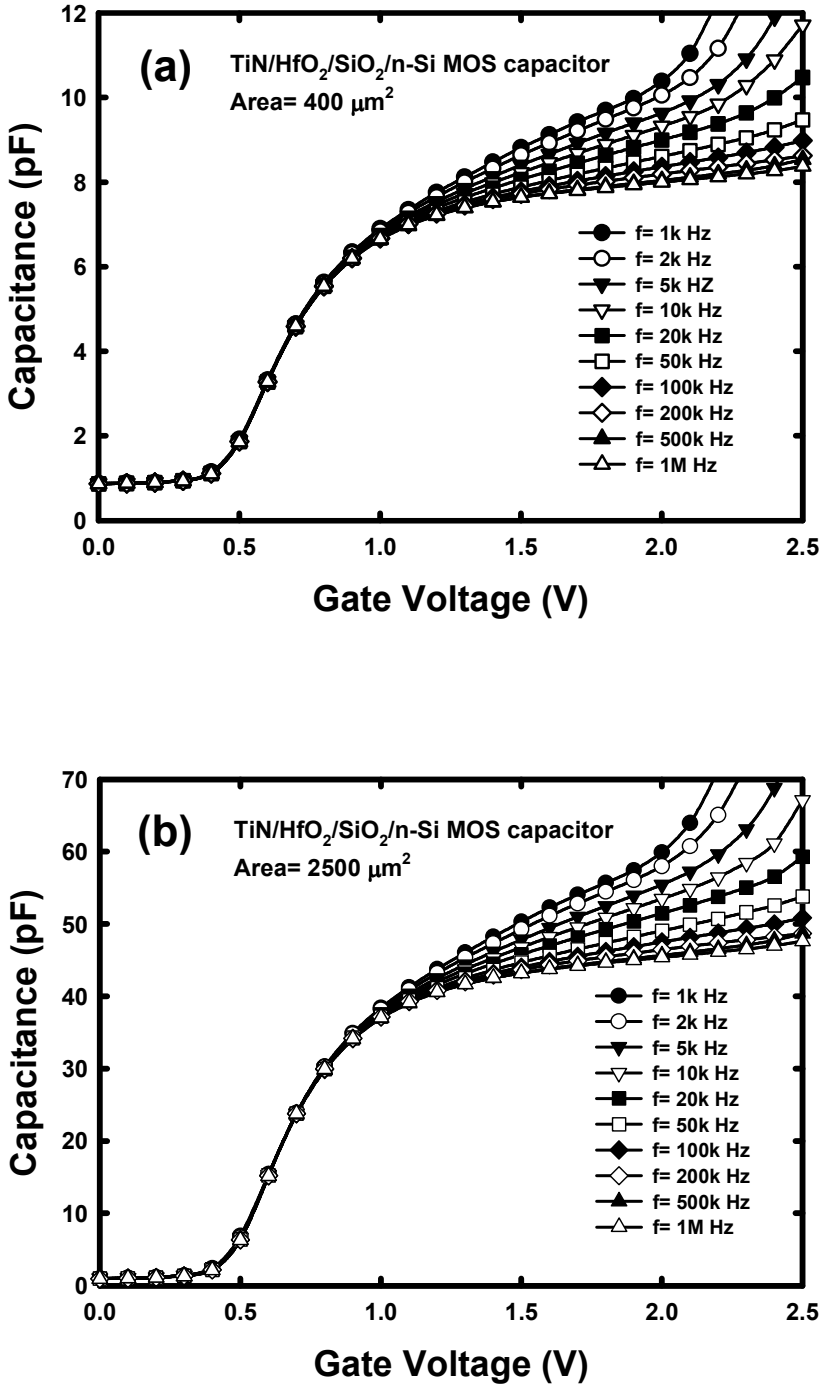


Fig. 5-3 Capacitance-voltage curves of the $TiN/HfO_2/SiO_2$/n-Si MOS capacitor at various frequencies with gate areas of (a) 400 and (b) 2500 μm^2. Similar dielectric capacitance increase at low frequencies has been observed for the capacitors with different gate areas.

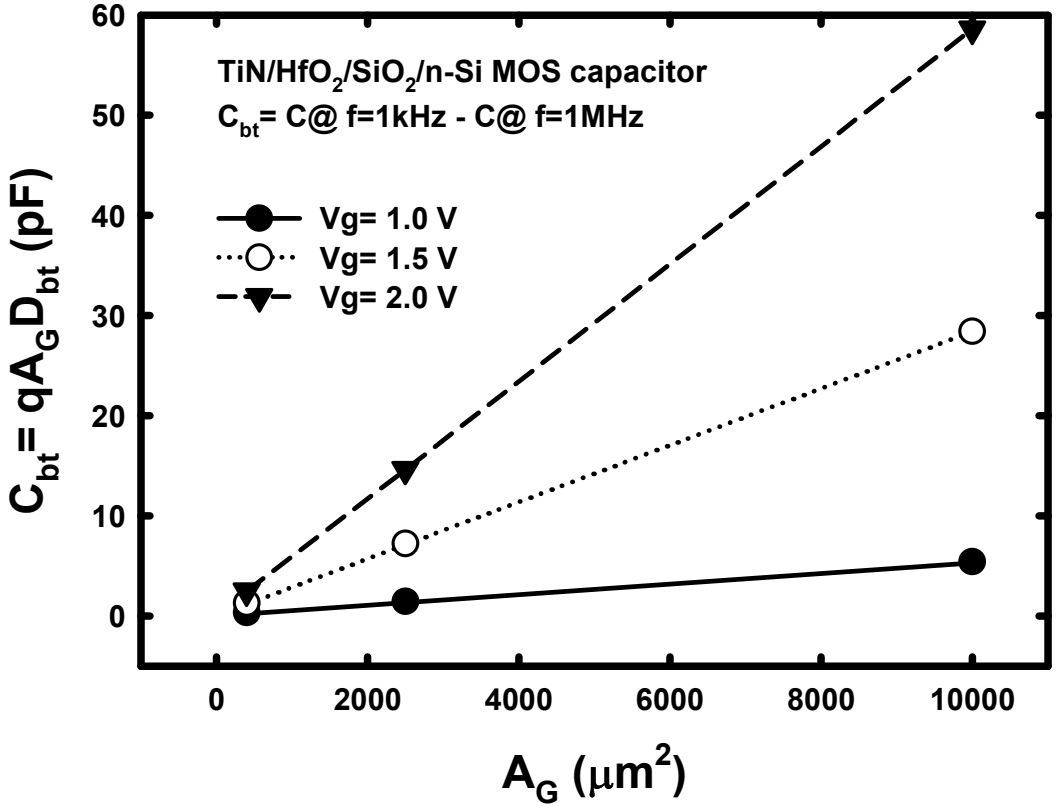


Fig. 5-4 Area dependence of the border trap capacitance C_{bt} under various gate bias voltages. As can be seen, the C_{bt} is linearly proportional to the gate area as proposed in the physical model.

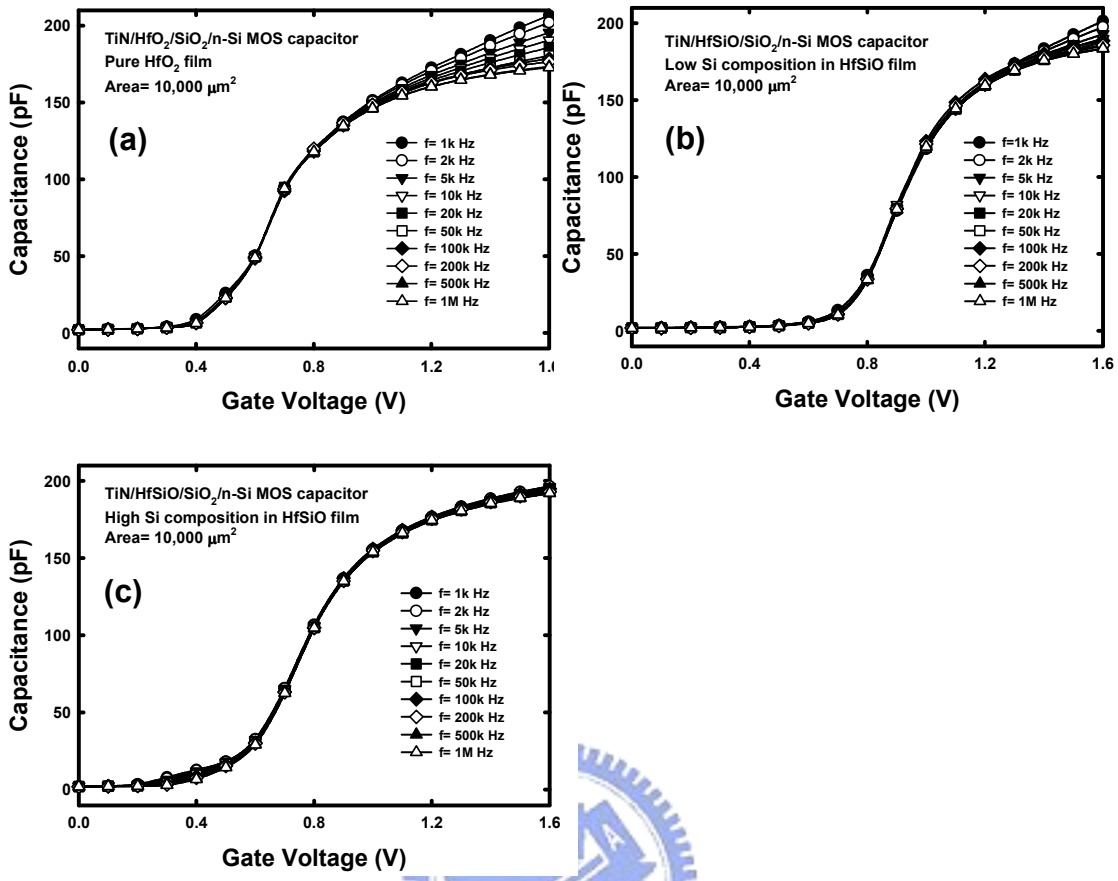


Fig. 5-5 Capacitance-voltage curves of the TiN/Hf-based high-k/SiO_2/n-Si MOS capacitor at various frequencies with (a) pure HfO_2, (b) low Si composition in the HfSiO film, and (c) high Si composition in the HfSiO film.

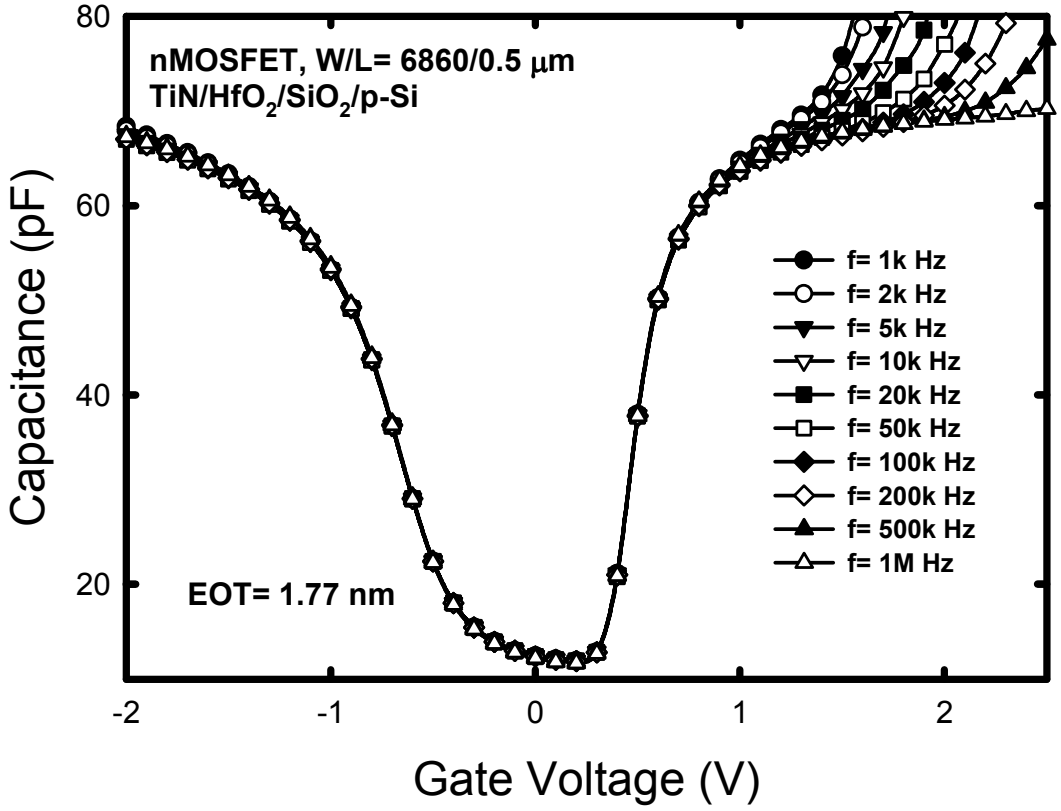


Fig. 5-6 Multi-frequency capacitance-voltage curves of the nMOSFET device with $TiN/HfO_2/SiO_2/p\text{-}Si$ high-k gate stack. Similar dielectric capacitance increase at low frequencies could also be observed in the strong inversion region.

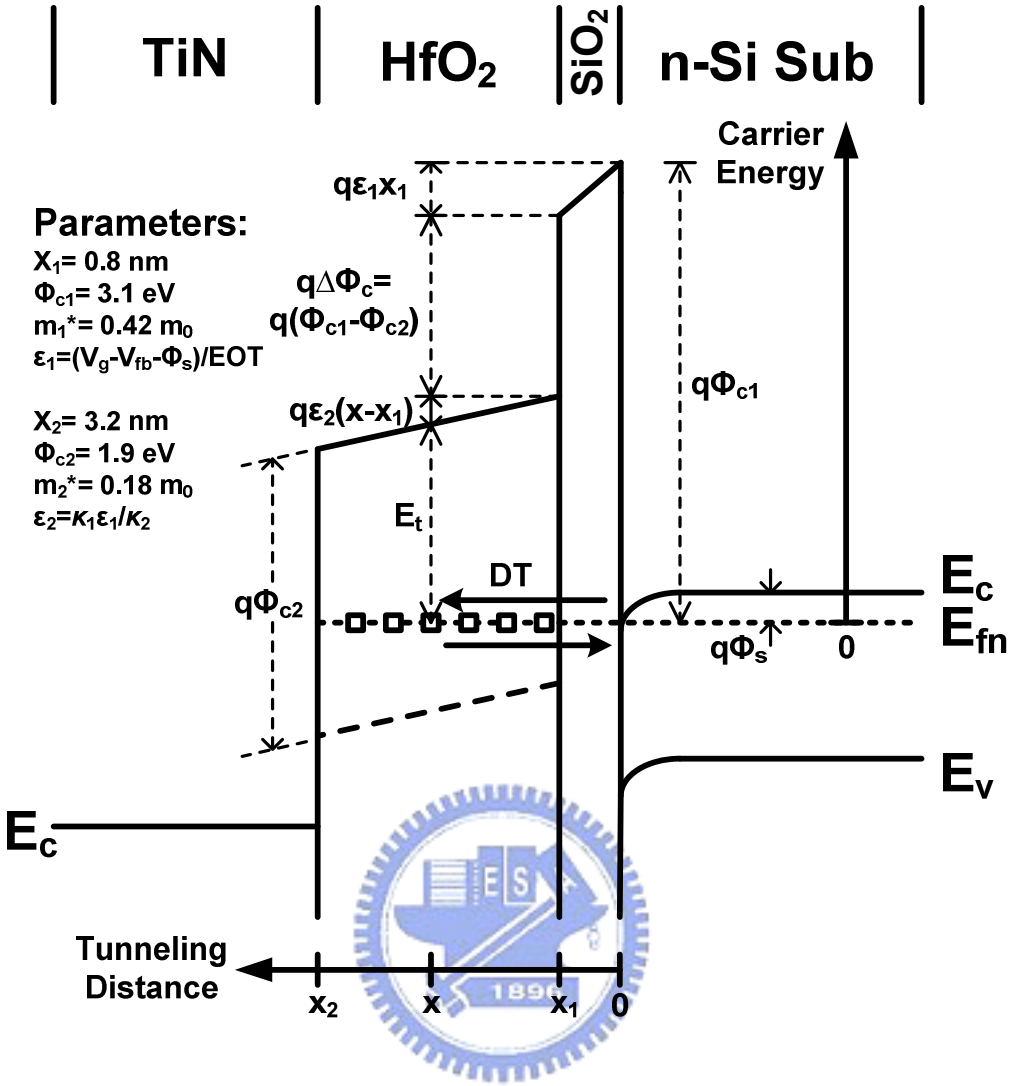


Fig. 5-7 Schematic band diagram of the TiN/HfO_2/SiO_2/n-Si MOS capacitor biased in the accumulation region with the illustration of tunneling distance and carrier energy coordinates.

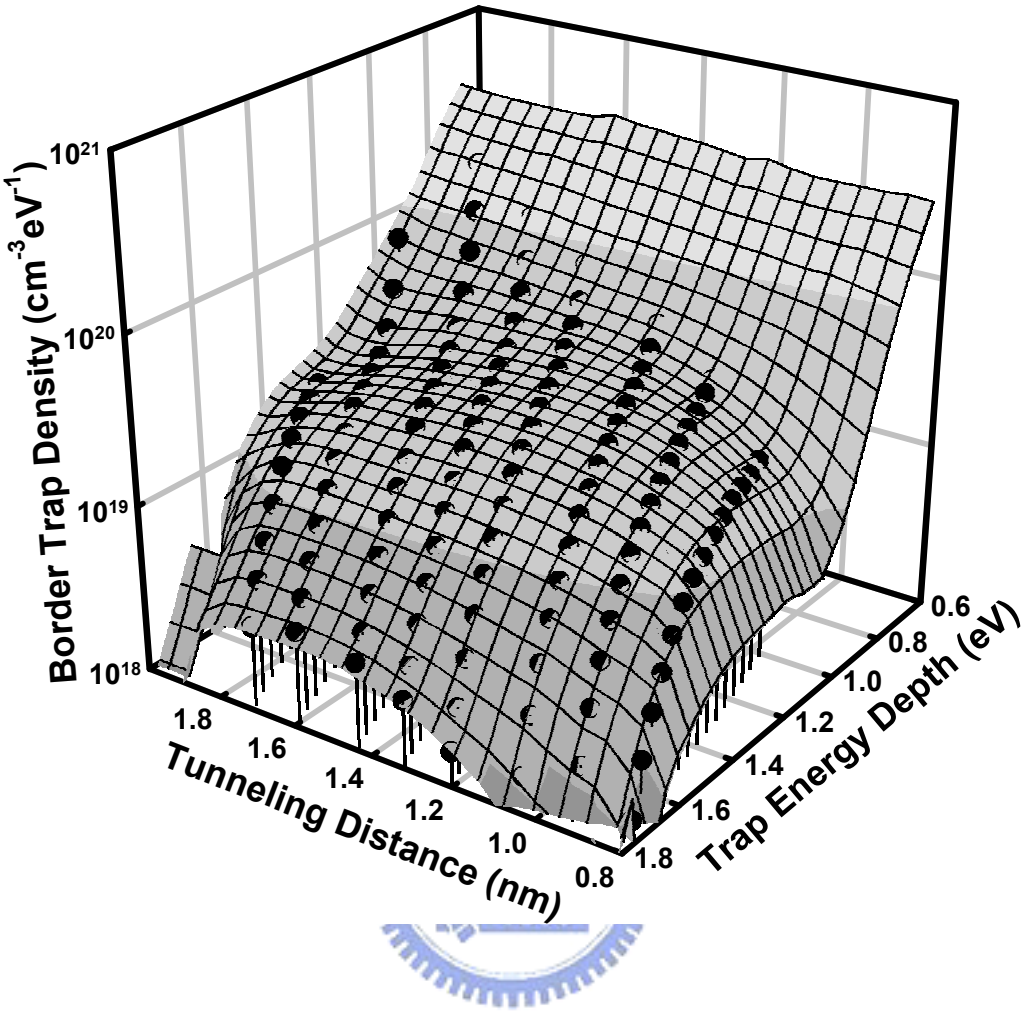


Fig. 5-8 Space and energy distribution of the border trap volume density in the dual-layer HfO_2/SiO_2 high-k gate stack. Symbols are model-extracted data points, and 3D-mesh is the smoothed surface profiling of these points.

Chapter 6: Transient Charging and Discharging of Border Traps in the Dual-Layer HfO_2/SiO_2 High-k Gate Stack by Low-Frequency Charge Pumping Method

6.1 Introduction

Charge pumping is a well-known electrical characterization method to determine the accurate SiO_2/Si interface state density for the past several decades. The basic theory of charge pumping current is the repetitive recombination at the interface states of minority carriers with majority carriers when the gate pulses are switching continuously between the accumulation and inversion regions. In other words, the carrier recombination mainly occurs at the transitions from accumulation to inversion or from inversion to accumulation, and the charge pumping current is supposed to be independent of the duration of ON and OFF times within one pulse cycle since there is only one type of charge carriers being trapped at the interface states (no carrier recombination). Moreover, the energy distribution of these interface states within the Si forbidden bandgap could be obtained by varying the rise and fall times of gate pulses, without knowing the dependence of surface potential on the applied gate voltage, due to the non-steady-state emissions of electrons and holes to the conduction and valence bands, respectively [6.1]. Briefly speaking, chare pumping is a powerful tool to determine not only the degradation mechanisms under all kinds of stress conditions (such as irradiation, hot carrier injection, and Fowler-Nordheim tunneling) but also the position and quantity of device degradation whether under uniform or localized aging conditions [6.2].

As reported in the literature, charge pumping method could also be used to

determine the bulk oxide traps located near the SiO_2/Si interface by measuring at low frequencies (longer injection and relaxation times). These near-interface oxide traps could only be found in the conventional SiO_2 gate oxide with heavy irradiation damage or the poly-Si/oxide/nitride/oxide/Si (SONOS) nonvolatile memory with thin tunneling oxide [6.3], and the additional recombined charge per cycle at low frequencies is attributed to the transient charging and discharging of these near-interface oxide traps located within the tunneling distance that can be reached at a specific frequency. The space distribution of these near-interface oxide traps (or called slow oxide traps as compared to the fast responses of interface states) could be profiled by varying the gate pulse frequency in the charge pumping method [6.4]-[6.6]. In summary, these near-interface oxide traps are defined as the oxide traps located near the interface that can instantly exchange charge carriers with the underlying Si substrate through direct tunneling, and are designated to be named as "border traps" to be distinguished from the conventional interface states and fixed oxide traps [6.7].

The direct tunneling model through thin interfacial oxide into the border traps in the dual-layer HfO_2/SiO_2 high-k gate stack is similar to that of tunneling into the near-interface oxide traps in heavily-irradiated SiO_2 or SONOS nonvolatile memory that has already been studied and proposed [6.8]-[6.11]. Based on these tunneling models, we are able to determine the space and energy distribution of border traps by varying the amplitude and frequency of input gate pulses. Similar to the border traps detected by the low-frequency C-V measurement in chapter 5, the detected fast high-k traps by low-frequency charge pumping method could also be defined as the pre-existing high-k traps located near the high-k/SiO_2 interface that can instantly exchange charge carriers with the underlying Si substrate through direct tunneling,

and thus designated as the border traps in the high-k dielectrics to be distinguished from other fast high-k traps (which have not been detected, depending on the measurement frequency).

In this chapter, it is found, in section 6.3, that not only the interface states but also the border traps located near the high-k/base oxide interface could be detected by the charge pumping method at low frequencies. Moreover, the transient charging and discharging behaviors of these border traps in the dual-layer HfO_2/SiO_2 high-k gate stack are extensively studied by the low-frequency charge pumping method with various input pulse waveforms in section 6.4. Finally, an elastic direct tunneling model through trapezoidal potential barriers is proposed to profile the space and energy distribution of the border traps as a smoothed 3D-mesh surface profiling in section 6.5, and we also made a fair comparison of analysis results between the low-frequency charge pumping method and low-frequency C-V measurement.

6.2 Device Fabrication and Analysis Method

NMOS devices with poly-Si/TaC/HfO_2/SiO_2/p-Si high-k gate stack were fabricated using the conventional CMOS process technology. The thin interfacial oxide SiO_2 (~1.0 nm) was thermally grown on 300-mm p-type silicon wafers, followed by the deposition of HfO_2 (~3.2 nm) high-k gate dielectric using atomic layer deposition (ALD) technique. Then n-type metal gate electrode TaC (Φ_m~4.3 eV on HfO_2 [6.12]) was deposited using physical vapor deposition (PVD) method, and the poly-Si gate served as the capping layer to ensure the process compatibility. Finally, the high-k gate stack was patterned using lithography and dry etching technologies, and the equivalent oxide thickness (EOT) of the above mentioned

HfO_2/SiO_2 high-k gate stack was extracted to be 1.77 nm by using the C-V simulation program which has taken the quantum effect into consideration [6.13].

An extension of the well-known charge pumping method to low frequencies has been employed to distinguish the border traps in the HfO_2/SiO_2 high-k gate stack from the conventional interface states at the SiO_2/Si interface. Fig. 6-1 shows the measurement system setup of the charge pumping method. The gate of a NMOS device is connected to a pulse generator, and a reverse bias voltage (V_r= 50 mV) is applied to the source and drain, while the charge pumping current I_{cp} is measured at the grounded substrate. By applying a series of input pulse waveforms with various frequencies to the gate, the charge pumping current due to the contributions from both the interface states and border traps could be measured at the substrate. Then the individual contributions could be separated by analyzing the recombined trapped charge density per cycle as a function of the frequency of input pulse waveform. If there is no contribution from the border traps, the recombined trapped charge density per cycle would be constant over a wide frequency range. However, in the presence of border traps, the recombined trapped charge density per cycle would increase with the decreasing frequency due to the longer time for charge carrier exchanges between the interface states and border traps located spatially near the interface. In this study, the low-frequency charge pumping method with various input pulse waveform parameters has been employed to study the transient charging and discharging behaviors of border traps, the related tunneling physical model, and the space and energy distribution of the border traps in the dual-layer HfO_2/SiO_2 high-k gate stack.

6.3 Low-Frequency Charge Pumping Results

Fig. 6-2 shows the charge pumping current I_{cp} of the high-k NMOS device as a

function of peak level voltage V_{peak} at various frequencies. As can be seen, different I_{cp} curves could be observed at high and low frequencies. At low frequencies, the I_{cp} continued to increase exponentially with the increasing peak level voltage, and this particular phenomenon could not be seen in SiO_2 and SiON ultrathin oxides.

Fig. 6-3 shows the trapped charge density N_t of the dual-layer HfO_2/SiO_2 high-k gate stack as a function of peak level voltage V_{peak} at frequencies ranging from 1k to 1M Hz, and the inset illustrates the definition of input pulse waveform parameters such as the peak and base level voltages, pulse period, pulse width, and rise/fall time. The typical pulse waveform parameters are illustrated as follows unless specified otherwise: duty cycle is 50%, rise time and fall time are both 10 ns, and peak and base level voltages are +2.0 and -1.0 V, respectively. The N_t detected at a specific frequency is calculated as follows:

$$N_t = I_{cp} / qfA_G, \tag{6.1}$$

where I_{cp} is the charge pumping current measured at the substrate, q is the fundamental electron charge, f is the frequency of input pulse waveform, and A_G is the gate area. As compared to the N_t measured at f= 1M Hz (which is believed to mainly stand for the interface state density N_{it}), the additional N_t measured at lower frequencies is attributed to the contributions from the pre-existing bulk traps in the HfO_2 high-k dielectric since the amount of oxide traps should be negligible in the well-fabricated, thermally-grown interfacial oxide [6.14], [6.15]. Moreover, it was found that these border traps could not be detected in the HfO_2/SiO_2 high-k gate stack with the same HfO_2 high-k dielectric (~3.2 nm) but having thicker interfacial oxide (~1.6 nm), or in the $HfSiON/SiO_2$ high-k gate stack with the optimized HfSiON high-k dielectric (~3.5 nm) and the same interfacial oxide (~1.0 nm). It appears that the pre-existing high-k bulk traps located near the HfO_2/SiO_2 interface or the so called

border traps could instantly exchange charge carriers with the underlying Si substrate if the interfacial oxide is thin enough for these charge carriers to tunnel through within the given pulse cycle. In addition, the N_t increased exponentially with the decreasing frequency and increasing peak level voltage, and these findings are consistent with those of tunneling into and from the near-interface oxide traps in heavily-irradiated thermal oxides SiO_2 [6.3]-[6.6].

6.4 Transient Charging and Discharging Behaviors

Fig. 6-4 shows the trapped charge density N_t as a function of the rise time and fall time (here T_r=T_f) of input pulse waveform at various frequencies (f= 1k, 10k, 100k, and 1M Hz). The N_t remained constant even with a great variety of rise time and fall time ranging from 2 ns to 1 μs except the one measured at f= 1M Hz. Since the rise time and fall time are highly associated with the scanned energy range of interface states in the Si forbidden bandgap [6.1] and the N_t at low frequencies are almost independent of rise time and fall time, the injected channel electrons from the Si conduction band states may directly tunnel into and out of the border traps in the HfO_2 high-k dielectric within the durations of transient charging (V_{peak}, ON state) and discharging (V_{base}, OFF state) stages, respectively. This may also eliminate the possibility of two-step capture and emission process (in which an efficient thermal Shockley-Read-Hall capture into an interface trap followed by a trap-to-trap tunneling transition and vice versa [6.16]).

Fig. 6-5 shows the trapped charge density N_t as a function of the base level voltage V_{base} of input pulse waveform at various frequencies. When the negative V_{base} was increased, the N_t at low frequencies grew gradually and eventually became saturated. Also, note that the N_t at various frequencies are almost identical at V_{base}= 0

~ -0.2 V. This suggests that the negative bias voltage of V_{base} plays a significant role to pull out the trapped electrons from the border traps during the transient discharging stage. Fig. 6-6 shows the trapped charge density N_t as a function of the duty cycle of input pulse waveform at various frequencies. Similar to the capture and emission of the interface states, the transient charging and discharging of border traps should both occur within one pulse cycle to constitute the recombination charge pumping current. With very small (~0%) or very large (~100%) duty cycles, the charge carriers may not have enough time to tunnel into or out of the border traps in the HfO_2 high-k dielectric, and only the interface states that can exchange charge carriers in a very short time could be observed such as the one measured at f= 1M Hz. In addition, symmetric transient charging and discharging behaviors could also be clearly observed at very small and very large duty cycles, therefore suggesting equal forward and reverse tunneling time constant in the elastic direct tunneling model[6].

Fig. 6-7 shows the trapped charge density N_t as a function of transient charging time at various peak level voltages V_{peak} by changing the ON time within one pulse cycle at f= 10k Hz. The N_t began to increase rapidly at the transient charging time ~10^{-7} sec in a power law relation and eventually became saturated except the one with V_{peak}= +0.5 V where only the interface states were observed, thus implying the transient charging effect may occur within 50-100 ns. Symbols are measurement data, dotted line is the fitting line for the interface state density, while solid lines are the model-fitting results using the charge trapping model with dispersive capture time constants [6.17], [6.18]:

$$N_t(t) = N_{bt}(t) + N_{it} = N_{bt,0}[1 - \exp(-(t/\tau)^{\beta})] + N_{it}, \quad (6.2)$$

[6] This proves our previous assumption of elastic direct tunneling due to the symmetric transient charge trapping and de-trapping behaviors, and the temperature dependence observed before may result from the following-up lattice-relaxation multi-phonon emissions (thermal energy transitions) by changing the positions of surrounding lattice ions before and after the capture of injected charge carriers.

where t is the transient charging time, $N_{bt}(t)$ is the detected border trap area density (cm^{-2}) as a function of transient charging time, N_{it} is the interface state density, $N_{bt,0}$ is the pre-existing border trap area density in the HfO_2 high-k dielectric, τ is the capture time constant, and β is the distribution factor of capture time constant (β= 1 for SiO_2). Although the $N_{bt,0}$ and τ vary, the β is ~0.32 for various $V_{peak,}$ and this also confirms that the border traps in the HfO_2/SiO_2 high-k gate stack should be spatially located at the bulk layer of HfO_2 high-k dielectric, not at the SiO_2 interfacial oxide.

Fig. 6-8 shows the trapped charge density N_t as a function of transient discharging time at various peak level voltages V_{peak} by changing the OFF time within one pulse cycle at f= 10k Hz. Similar to the transient charging behavior, transient discharging behavior could also be well described by the charge de-trapping model with dispersive emission time constants which is similar to the charge trapping model. The $N_{bt,0}$ and τ of transient discharging behavior are near to those of transient charging behavior, and the β is also ~0.32. Because the distribution of tunneling time constant is highly associated with the tunneling distance from the Si substrate surface to the localized border traps and the previous studies about slow high-k traps using positive bias temperature instability (PBTI) stress and static I_d-V_g characteristics [6.18] also exhibited the same β (~0.32) value, it may be concluded that the fast and slow traps in the HfO_2 high-k dielectric have similar space trap distribution and that the fast high-k traps might be identical to the slow high-k traps in properties but just located deeper inside the Hf-based high-k dielectric.

6.5 Space and Energy Distribution of Border Traps

Fig. 6-9 shows the detected border trap area density N_{bt} as a function of the frequency of input pulse waveform at various peak level voltages V_{peak} by

transforming the frequency and voltage dependences as shown in Fig. 6-3. These frequency and voltage dependences of N_{bt} could also be transformed into the relations corresponding to the tunneling distance from the Si substrate surface and the trap energy depth from the HfO_2 conduction band edge, respectively.

Fig. 6-10 shows the schematic band diagram of the TaC/HfO_2/SiO_2/p-Si NMOS device biased in the strong inversion region with the illustrations of tunneling distance and carrier energy coordinates. If the transient charging and discharging of border traps mainly occur at the Si conduction band edge through direct tunneling and the border traps are widely distributed over a defect band in the HfO_2 high-k dielectric [6.14], the N_{bt} could be regarded as the equivalent border trap area density D_{bt} at one specific energy level ($cm^{-2}eV^{-1}$), which is the integration of border trap volume density ρ_{bt} ($cm^{-3}eV^{-1}$) from the base oxide thickness x_1 to the maximum tunneling distance x_{max} in the HfO_2 high-k dielectric since there should be negligible border traps in the thermally-grown interfacial oxide SiO_2:

$$N_{bt} \sim D_{bt} = \int_{x_1}^{x_{max}} \rho_{bt}(x, E_t)dx. \tag{6.3}$$

The trap energy depth E_t from the HfO_2 conduction band edge could be approximately obtained at various peak level voltages if the two-band structure (SiO_2 and HfO_2) with trapezoidal potential barriers is assumed:

$$E_t(x, \varepsilon) = \phi_{c2} - q\varepsilon_1 x_1 - q\varepsilon_2 (x - x_1), \tag{6.4}$$

where Φ_{c2} (1.9 eV) is the conduction band offset of HfO_2 [6.19], ε_1 and ε_2 are the electric fields in the SiO_2 and HfO_2 dielectrics, respectively, and x_1 is the base oxide thickness (1.0 nm). If the tunneling transition is an elastic direct tunneling process with symmetric forward and reverse tunneling time constants, the tunneling time constants between the available Si conduction band states and localized border traps should be equal to or less than 1/2f if the duty cycle is 50%:

$$\frac{1}{2f} = \tau_0 \exp(2\int_0^{x_1} \frac{\sqrt{2m_1^*(\phi_{c1} - q\varepsilon_1 x')}}{\hbar} dx' + 2\int_{x_1}^{x} \frac{\sqrt{2m_2^* E_t(x', \varepsilon)}}{\hbar} dx'), \quad (6.5)$$

where f is the frequency, τ_0 is the pre-exponential factor (~10^{-10} sec) which is relatively insensitive to the tunneling distance and trap energy depth [6.20], ħ is the reduced Planck constant, Φ_{c1} (3.1 eV) is the conduction band offset of SiO_2, and m_1^* (0.42 m_0) and m_2^* (0.18 m_0) are the effective mass of electrons in the SiO_2 and HfO_2 dielectrics, respectively [6.12], [6.26]. Then, the maximum tunneling distance x_{max} that can be reached during the given pulse cycle could be extracted from (6.5) with the above physical model parameters. Finally, the space and energy distribution of border trap volume density ρ_{bt} could be obtained as follows:

$$\rho_{bt}(x, E_t) = \frac{-2\sqrt{2m_2^* E_t(x, \varepsilon)}}{\hbar} \frac{dN_{bt}}{d\ln(f)}. \quad (6.6)$$

Fig. 6-11 shows the space and energy distribution of border trap volume density ρ_{bt} (~10^{17}-10^{19} $cm^{-3}eV^{-1}$) in the dual-layer HfO_2/SiO_2 high-k gate stack. Symbols are model-extracted data points, and 3D-mesh is the smoothed surface profiling of these points. As the tunneling distance reaches the HfO_2 high-k dielectric (x >1.0 nm), the ρ_{bt} began to increase gradually and eventually became saturated. Moreover, the ρ_{bt} increases exponentially with the decreasing trap energy depth E_t, and the variation of the ρ_{bt} seems to be less sensitive to the tunneling distance. These results suggest that most of the pre-existing high-k border traps are located in the HfO_2 bulk layer and that considerable parts of these border traps are positioned at the shallow energy levels. Moreover, similar space and energy distribution of border traps could be observed by the low-frequency charge pumping in this chapter and the low-frequency C-V measurement in chapter 5. However, there is some discrepancy in the order of magnitude of detected border trap volume densities due to the different testing conditions, rapid recombination of majority and minority carriers for charge pumping

and small-signal frequency response for C-V measurement.

6.6 Summary

The pre-existing high-k traps located near the HfO_2/SiO_2 interface or the so called border traps could instantly exchange charge carriers with the underlying Si substrate through direct tunneling, and these border traps (detected fast high-k traps) could be measured and analyzed by the low-frequency charge pumping method with fixed base level voltage and varying amplitude. As compared to the interface state density measured at f= 1M Hz, the additional trapped charge density measured at lower frequencies could be attributed to the contribution from the border traps in the HfO_2 high-k dielectric. Moreover, various transient charging and discharging characteristics of these border traps could be observed by varying the rise time and fall time, peak and base level voltages, and duty cycle of input pulse waveform. In addition, the transient charging and discharging behaviors of the border traps could be observed in the time scale of 10^{-8}-10^{-4} sec by changing the ON and OFF times within one pulse cycle at a specific frequency, and this method is much faster than the known pulse I_d-V_g technique (~1-10 μs). Also, the transient charging/discharging behavior could be well described by the charge trapping/de-trapping model with dispersive capture/ emission time constants used in the static positive bias stress, thus suggesting similar space trap distribution of fast and slow traps in the HfO_2 high-k dielectric. Finally, the frequency and voltage dependences of the border trap area density could be transformed into the relations corresponding to the tunneling distance and trap energy depth by using an elastic direct tunneling model between the Si conduction band states and localized border traps through trapezoidal potential barriers. Based on this physical model, the space and energy distribution of the border traps in the HfO_2

high-k dielectric could be profiled as a smoothed 3D-mesh. Although the energy scan of border traps over a defect band is based on the assumption of elastic direct tunneling at a specific single energy level, this assumption could help us realize and profile the truly three dimensional border trap distribution in space and in energy levels to a certain extent.

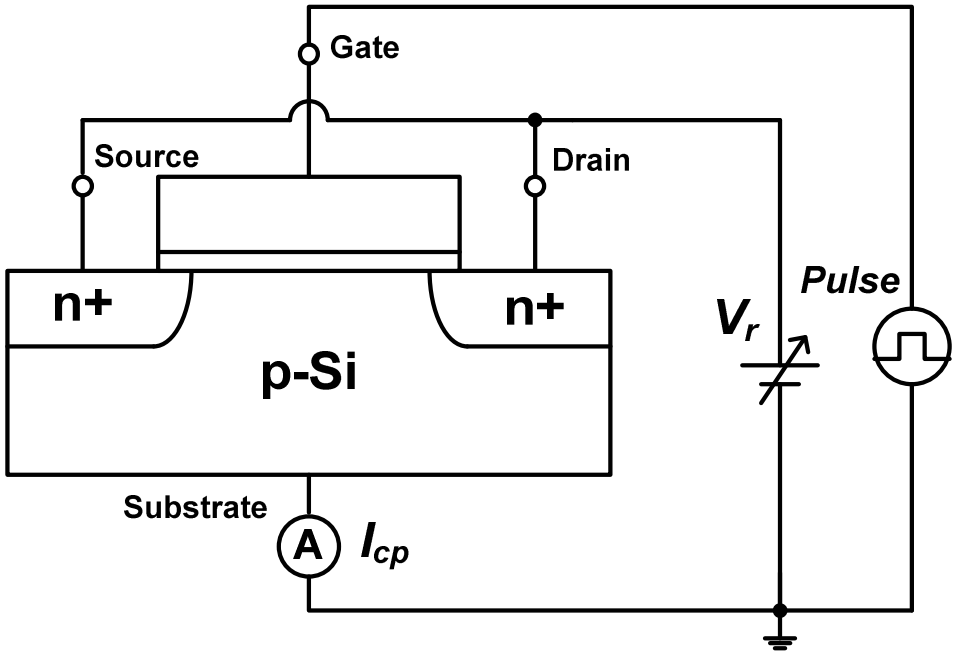


Fig. 6-1 Measurement system setup of charge pumping method. The gate of a NMOS device is connected to a pulse generator, and a reverse bias voltage V_r is applied to the source and drain, while the charge pumping current I_{cp} is measured at the grounded substrate.

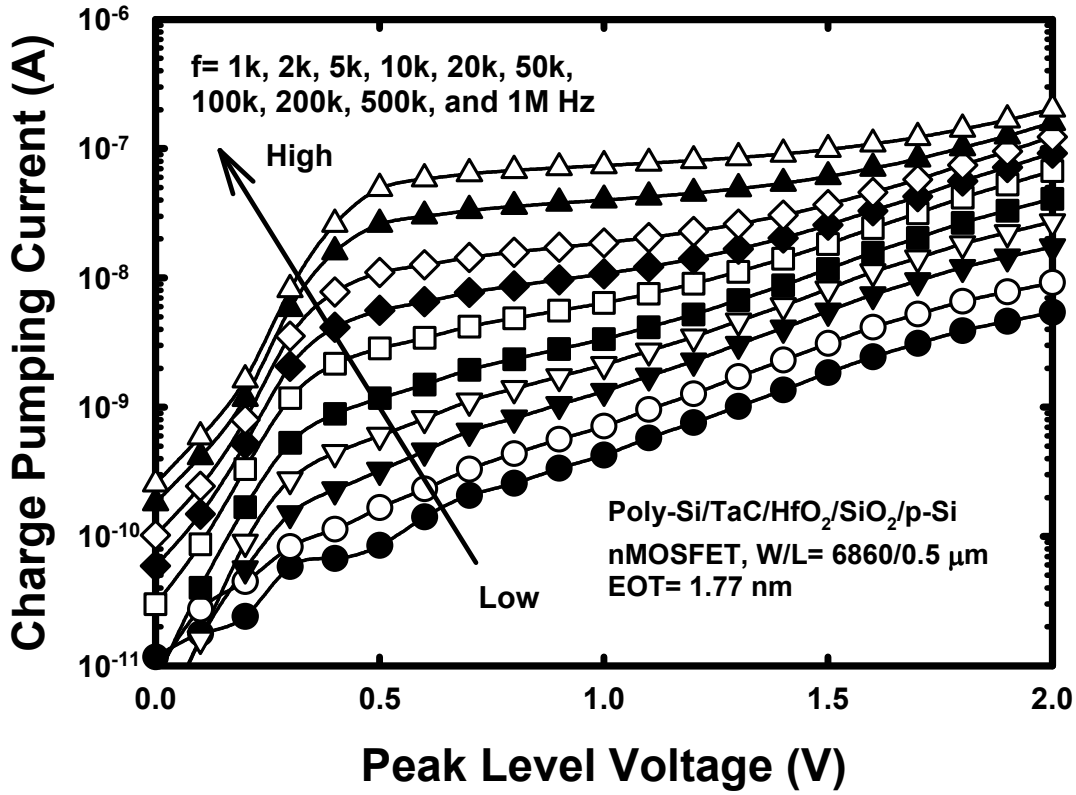


Fig. 6-2 Charge pumping current I_{cp} of the poly-Si/TaC/HfO_2/SiO_2/p-Si high-k gate stack with EOT= 1.77 nm as a function of peak level voltage V_{peak} at various frequencies.

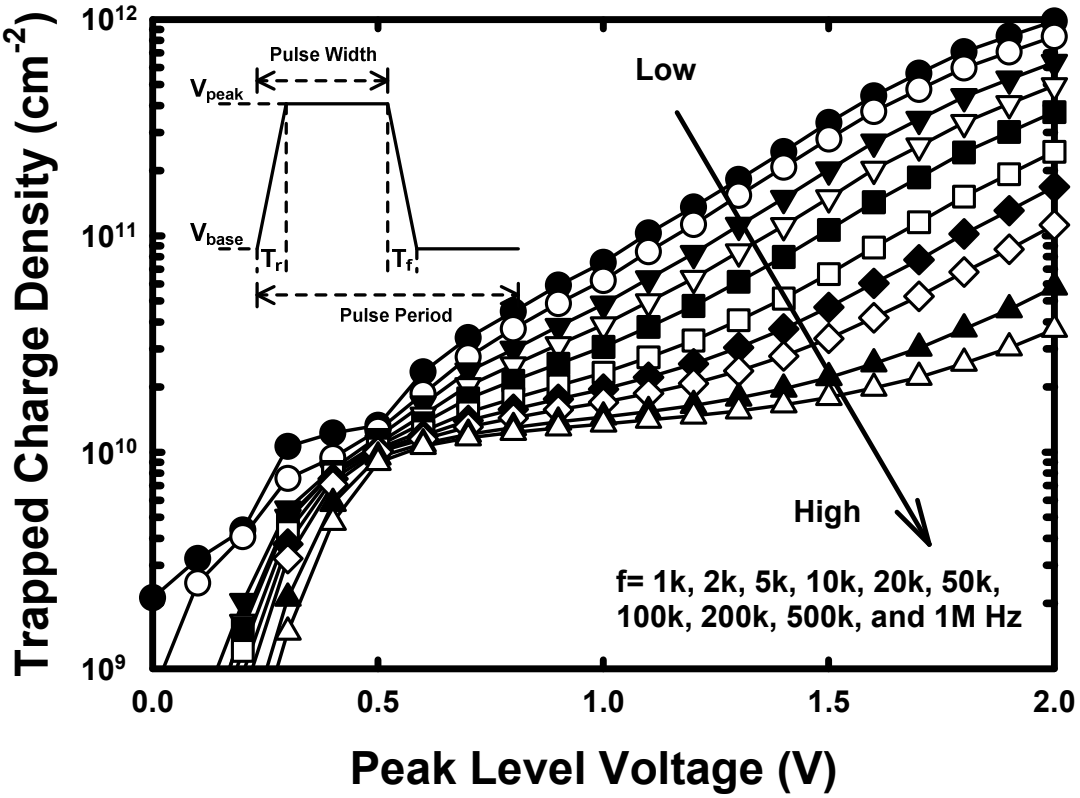


Fig. 6-3 Trapped charge density N_t of the dual-layer HfO_2/SiO_2 high-k gate stack as a function of peak level voltage V_{peak} at various frequencies. The inset illustrates the definition of input pulse waveform parameters.

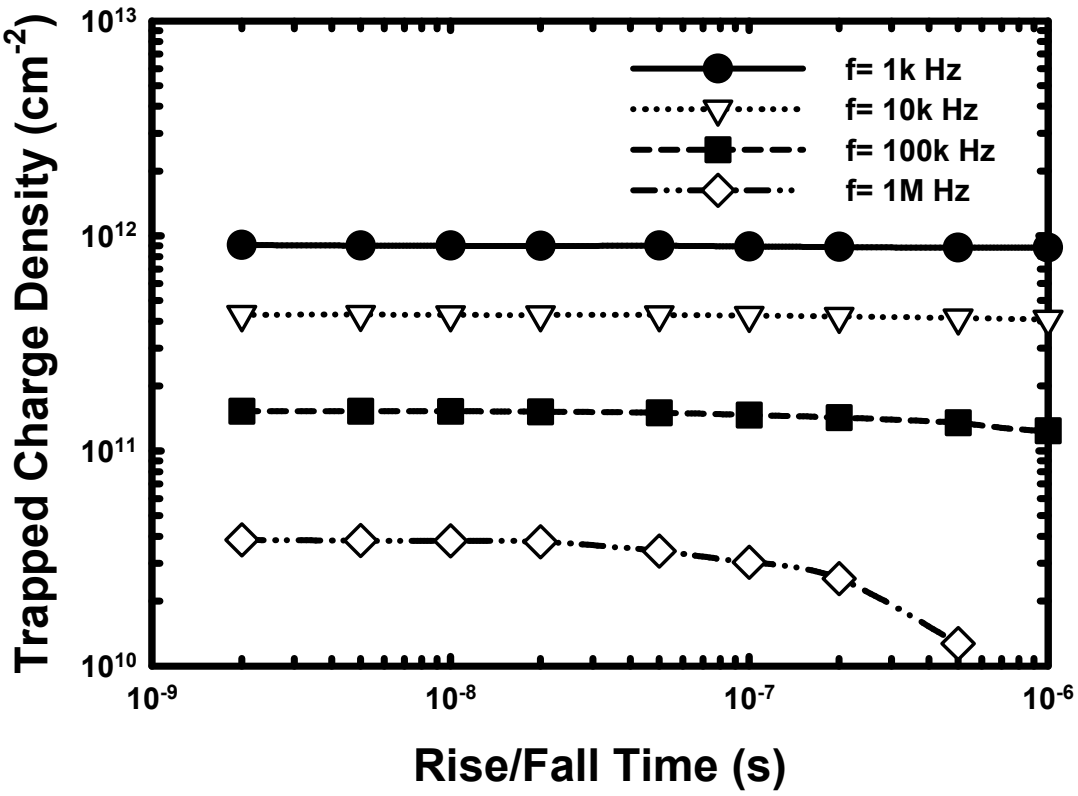


Fig. 6-4 Trapped charge density N_t as a function of the rise time and fall time (here T_r=T_f) of input pulse waveform at various frequencies (1k, 10k, 100k, and 1M Hz). Rise time and fall time are highly associated with the scanned energy range of interface states in the Si forbidden bandgap.

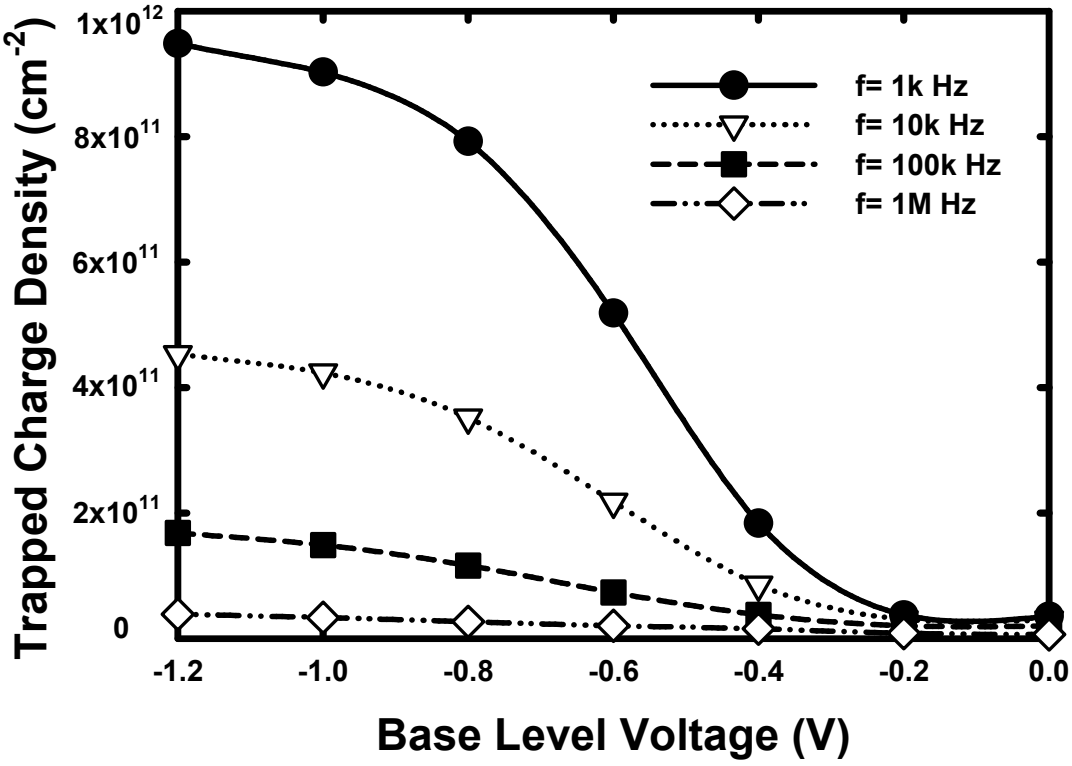


Fig. 6-5 Trapped charge density N_t as a function of the base level voltage V_{base} of input pulse waveform at various frequencies (1k, 10k, 100k, and 1M Hz). The negative bias voltage of V_{base} plays a significant role to pull out the trapped charge carriers during the transient discharging stage.

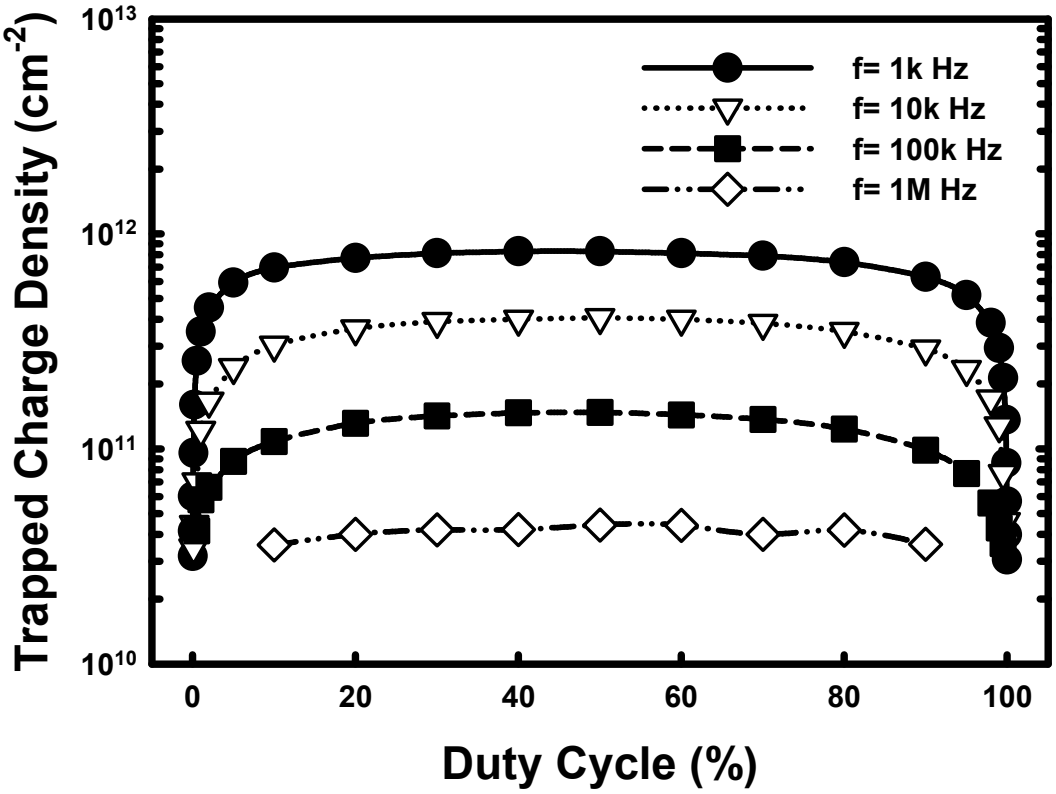


Fig. 6-6 Trapped charge density N_t as a function of the duty cycle of input pulse waveform at various frequencies (1k, 10k, 100k, and 1M Hz). Symmetric transient charging and discharging behaviors could be observed at very small and very large duty cycles.

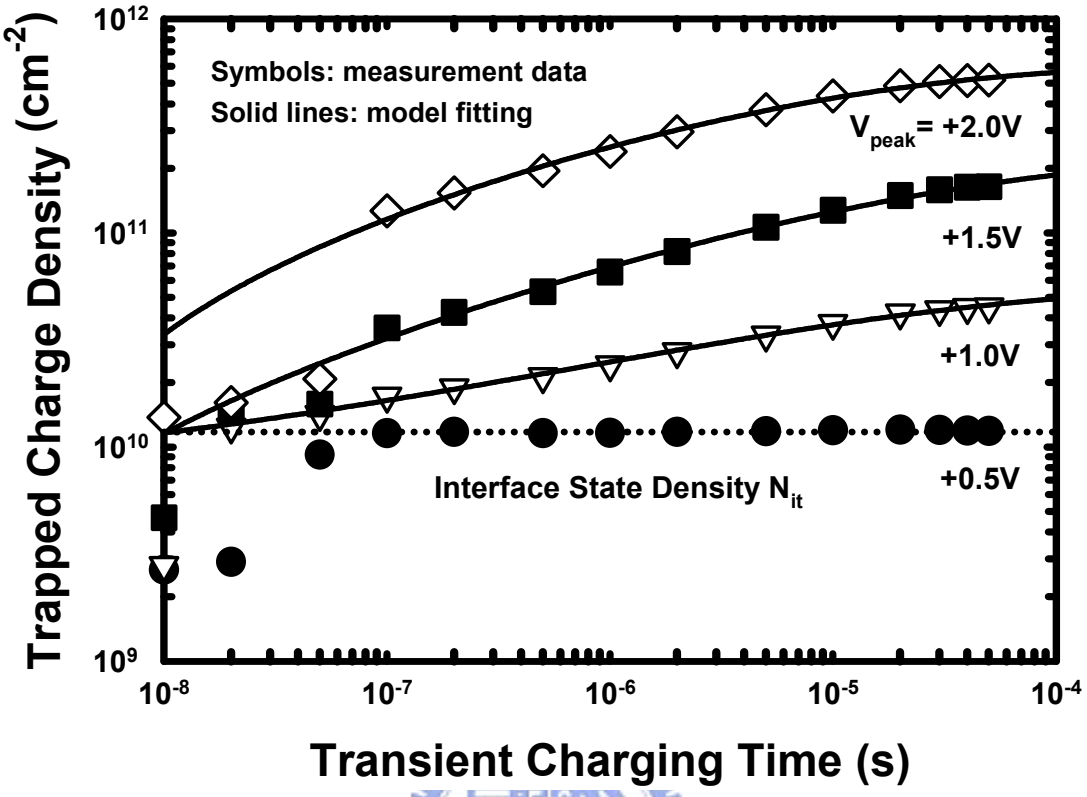


Fig. 6-7 Trapped charge density N_t as a function of transient charging time at various peak level voltages V_{peak} by changing the ON time of input pulse waveform at f= 10k Hz. Symbols are measurement data, dotted line is the fitting line for the interface state density, and solid lines are the model fitting results.

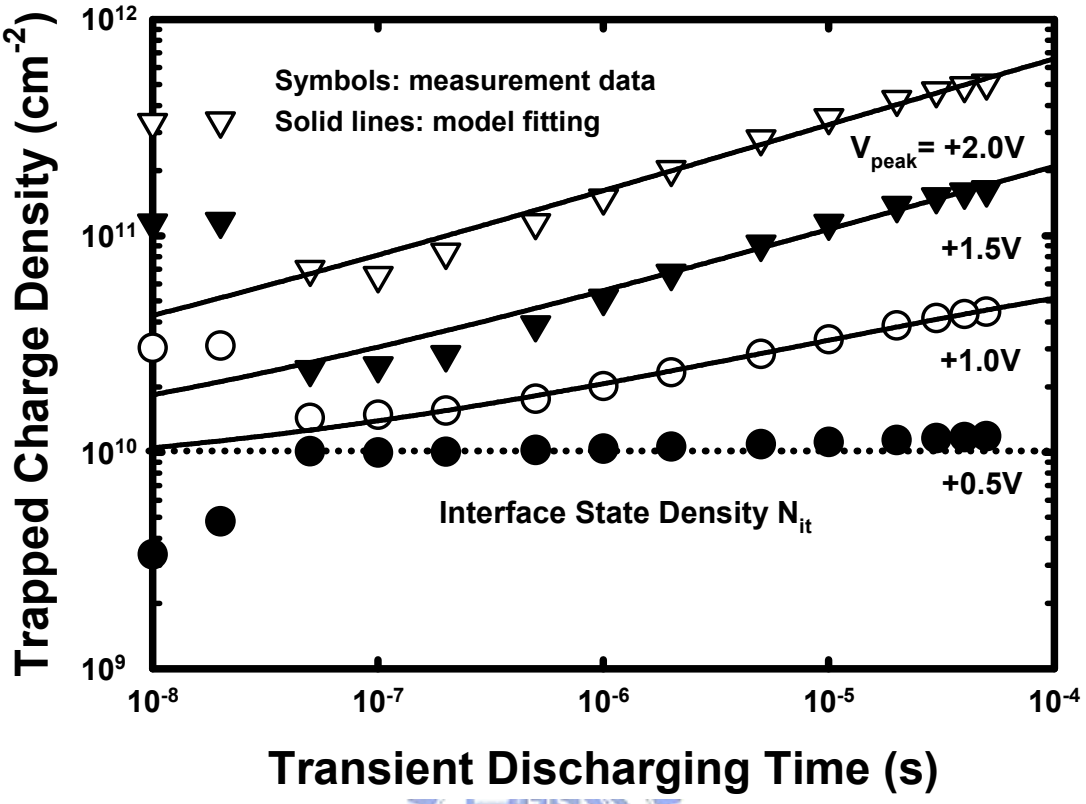


Fig. 6-8 Trapped charge density N_t as a function of transient discharging time at various peak level voltages V_{peak} by changing the OFF time of input pulse waveform at f= 10k Hz. Symbols are measurement data, dotted line is the fitting line for the interface state density, and solid lines are the model fitting results.

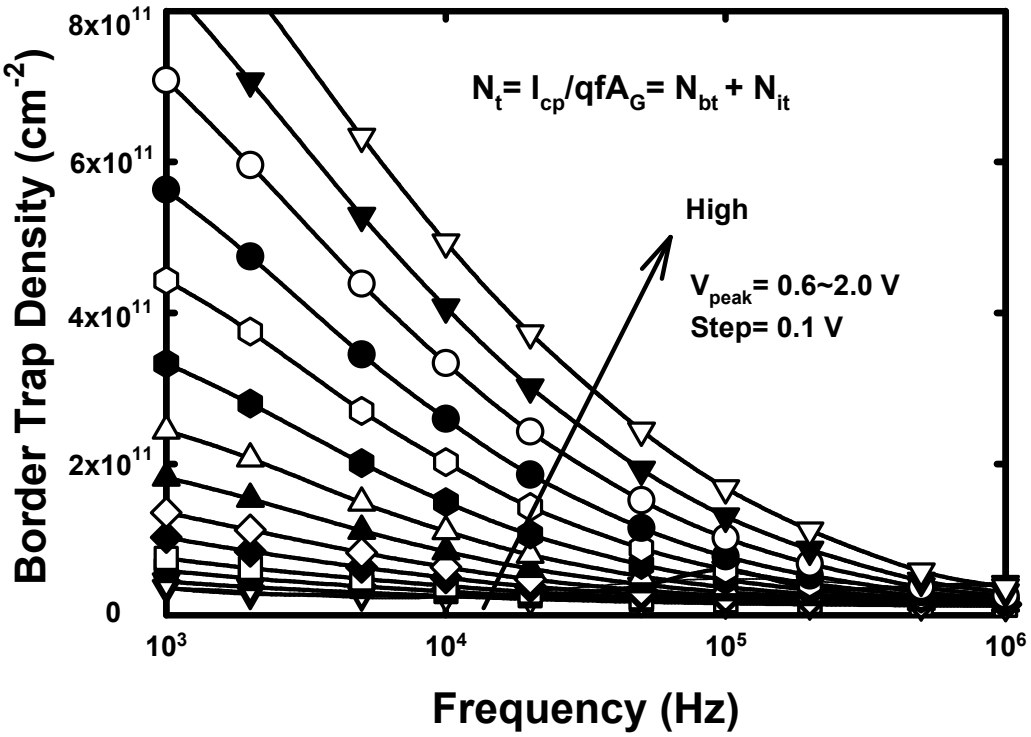


Fig. 6-9 Border trap area density N_{bt} of the dual-layer HfO_2/SiO_2 high-k gate stack as a function of the frequency of input pulse waveform at various peak level voltages V_{peak}. As can be seen, N_{bt} increased exponentially with the decreasing frequency and the increasing peak level voltage.

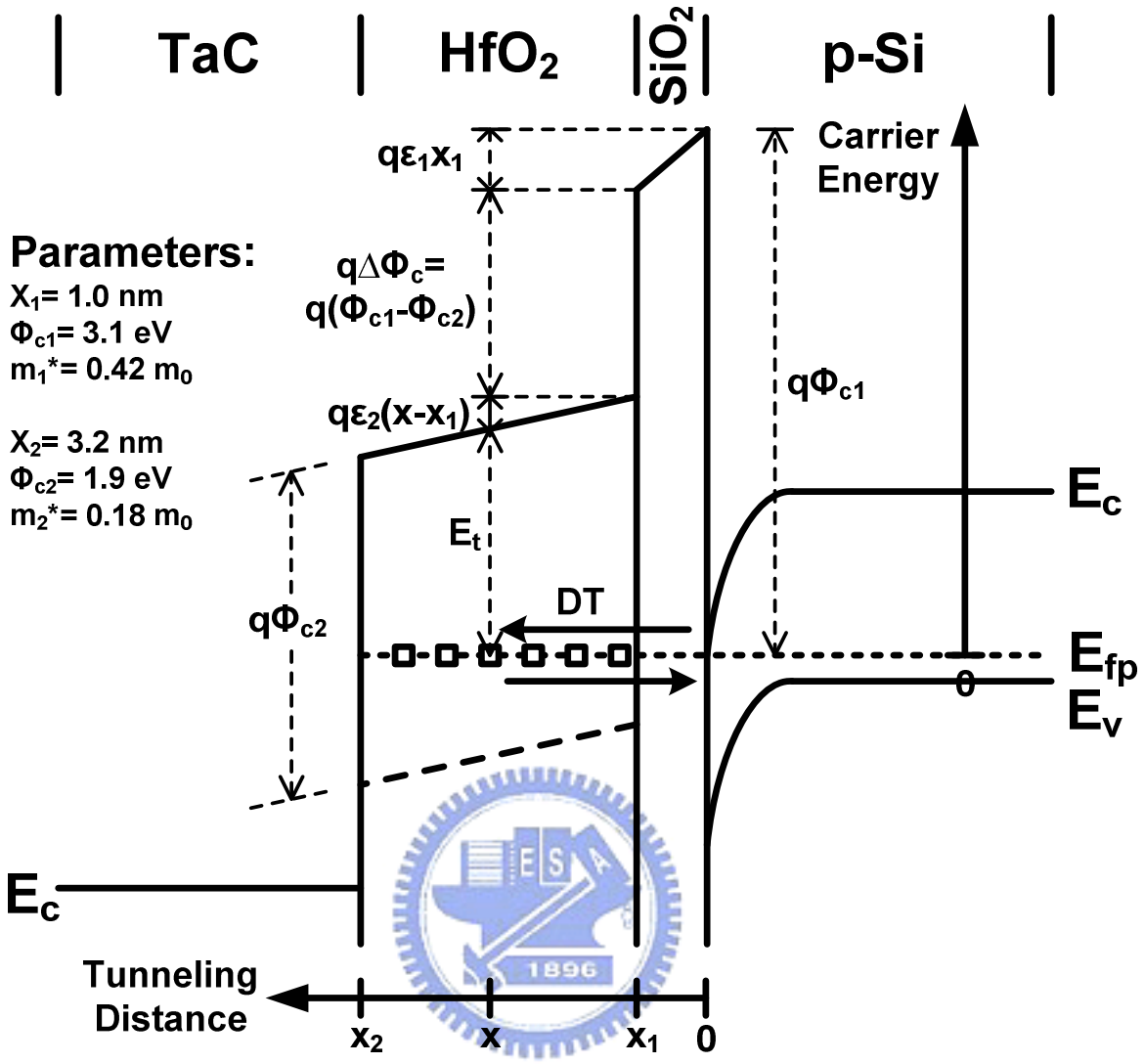


Fig. 6-10 Schematic band diagram of the dual-layer HfO_2/SiO_2 high-k gate stack biased in the strong inversion region with the illustrations of tunneling distance and carrier energy coordinates.

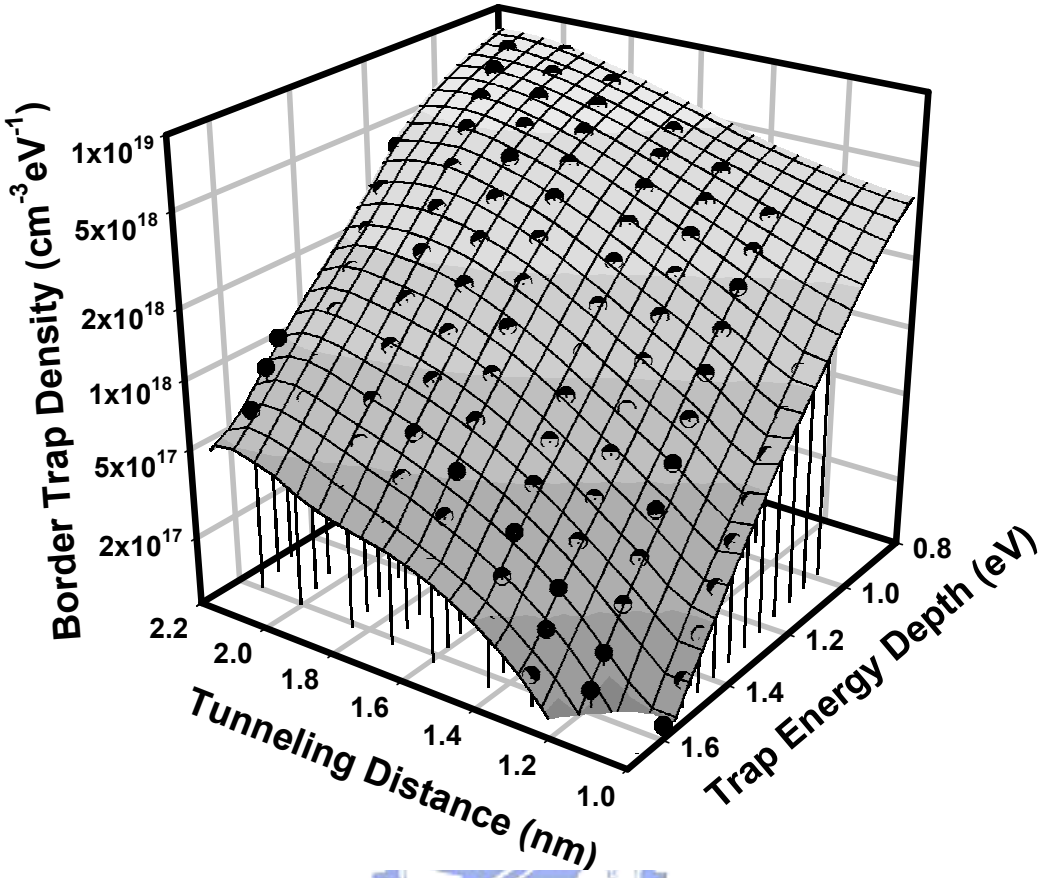


Fig. 6-11 Space and energy distribution of border trap volume density ρ_{bt} in the dual-layer HfO_2/SiO_2 high-k gate stack. Symbols are model-extracted data points, and 3D-mesh is the smoothed surface profiling of these points.

Chapter 7: Conclusions

7.1 Summary of Findings and Contributions

In this dissertation, many different electrical characterization methods have been extensively and intensively studied to understand the fundamental characteristics and physical mechanisms of charge trapping and de-trapping in the pre-existing traps in Hf-based high-k gate dielectrics. Trapped charge carriers in Hf-based high-k gate dielectrics would lead to the serious reliability concern of threshold voltage instability, which is a major issue of performance degradation whether in digital or analog circuits. In chapter 2, charge trapping behavior in the HfSiO high-k gate dielectric could be well described by the charge trapping model in the pre-existing high-k traps with dispersive capture time constants, and it has been demonstrated to be a field-enhanced and thermally-activated process due to the physical nature of trap-assisted tunneling processes (ohmic conduction and Frenkel-Poole emission). Thick interfacial oxide and high Si composition in the HfSiO film have also been proved to be effective approaches to reduce the extent of charge trapping in Hf-based high-k gate dielectrics, while both measures are not preferred for the ultimate scaling of the equivalent oxide thickness (EOT) of gate dielectric. In chapter 3, similar charge trapping behavior could be observed and repeated during the consecutive stress/recovery cycles under static positive bias stress if the recovery bias voltage is strong enough to clean up most trapped charge carriers. This confirms that the high-k traps are pre-existing traps in the high-k gate dielectrics and that no additional traps are generated during the stress cycles. In addition, transient charging behavior could be observed within 10-50 ns by changing the duty cycle of stress pulse waveform under dynamic positive bias stress, and a universal charge trapping model has also

been demonstrated in terms of the effective stress time.

In chapter 4, two-frequency C-V correction using a five-element circuit model has been used to eliminate the faulty clamped and amplified C-V curves in low-leakage high-k gate dielectrics due to the impacts of parasitic components, series resistance R_s and series inductance L_s. The tanδ (or called dissipation factor) represents the dynamic energy loss resulting from the local movement or vibration of flexible Hf-O bonds, which might be an intrinsic materials issue in high-k gate dielectrics. Moreover, this five-element circuit model could be modified as another four-element circuit model to reduce the severe capacitance drop due to tunneling leakage current and to obtain the equivalent oxide thickness of ultrathin oxides or high-k gate dielectrics with high leakage current. In chapter 5, the additional dielectric capacitance increase at low-frequency C-V curves could be regarded as the specific characteristic of the transient charging and discharging of border traps in high-k gate dielectrics, which could only be observed in the high-k MOS capacitors with n-Si substrate biased in strong accumulation region or the high-k nMOSFETs biased in strong inversion region. In addition, the frequency and voltage dependences of border trap capacitance could be transformed into the space and energy distribution of border traps in the high-k dielectric based on an elastic direct tunneling model through trapezoidal potential barriers. In chapter 6, the transient charging and discharging of border traps could also be observed by the low-frequency charge pumping method. By changing the rise/fall time and duty cycle of input pulse waveform, the assumption of elastic direct tunneling model with symmetric forward and reverse tunneling time constant could be further verified and proved. Also, the transient charging and discharging behaviors could be well described by the charge trapping model with dispersive capture time constants in static positive bias stress, thus suggesting similar space

distribution of fast and slow traps in high-k dielectrics. In addition, consistent space and energy distribution of border traps could be obtained by both the low-frequency C-V measurement and low-frequency charge pumping method.

7.2 Suggestions for Future Work

A variety of electrical characterization methods have been adopted to draw the complete picture of charge trapping and de-trapping in the pre-existing traps in Hf-based high-k gate dielectrics, including the physical model of charge trapping, the charge trapping and de-trapping behaviors of slow and fast high-k traps, and the space and energy distribution of fast high-k traps. With all these pieces of information, we could have a better understanding of the over-all charge trapping and de-trapping in Hf-based high-k gate dielectrics. However, there are some topics which have not yet been understood clearly nor verified with strong evidence support. Therefore, these topics deserve to be further studied in the near future:

1. In chapter 2, the physical meaning of the charge trapping model with dispersive capture time constants (stretched exponential growth) and its model parameters should be further studied. It is important to understand why this physical model could well describe the charge trapping behavior in high-k gate dielectrics and how this model could be used to predict the device lifetime under normal operation conditions. Also, this model could be re-arranged as the Weibull distribution (weakest link relation) which is commonly used in time-dependent dielectric breakdown (TDDB) studies. The similarity and discrepancy between these two reliability issues should be understood as well.
2. In chapter 3, the repetitive, reversible charge trapping and de-trapping behaviors indicate the charge carriers are trapped in the pre-existing high-k traps without

generating new high-k traps during the stress/recovery cycles or the amount of generated high-k traps is negligible as compared to the pre-existing high-k traps. Moreover, the transient charging effect could be observed within 10-50 ns even for the slow high-k traps, and this asymmetric capture and emission time constants imply that these trapped charge carriers are located deeply in space distance or in energy levels. These uncertainties deserve to be clarified.

3. In chapter 4, the physical origin of dynamic energy loss **tan**δ and its relationship to the composition of high-k dielectrics (such as HfO_2, HfSiO, and HfSiON) should be studied. Furthermore, the severe capacitance drop due to tunneling leakage current could not be completely recovered by the two-frequency C-V correction only. New circuit element should be added or higher measurement frequencies (Agilent 4294A, f= 40~110M Hz) should be used with appropriate phase compensation and OPEN/SHORT/LOAD calibrations.
4. In chapter 5 and 6, much effort should be made to understand the correlation between the border trap properties (such as the magnitude of border trap density, the space and energy distribution, and the transient charging and discharging behaviors) by low-frequency C-V measurement and by low-frequency charge pumping, and these results could be further verified by pulse I_d-V_g technique in some extent. Moreover, the application limits of these two characterization methods should also be studied in terms of the frequency, gate area, and applied gate voltage since both methods may suffer measurement errors under testing conditions of huge tunneling leakage current. Also, the assumption of elastic direct tunneling at single energy level could be modified as the direct tunneling from multiple sub-bands in the Si conduction band states to obtain more accurate energy distribution of border traps.

5. Much effort should be made to study the charge trapping and de-trapping behaviors under static and dynamic negative bias stress in pMOSFETs with Hf-based high-k gate dielectric. Since gate electrons from metal gate electrode and channel holes from inverted n-Si substrate may be injected into the high-k gate dielectric simultaneously, threshold voltage instability should be considered as the combinational effect of both electron and hole trapping in the high-k gate dielectric, and charge recombination may also occur. This may lead to the faulty understanding of charge trapping and de-trapping behaviors under negative bias stress if the respective contributions of electrons and holes have not been clearly separated.

6. Optimized process conditions should be studied to reduce the number of the pre-existing traps in Hf-based high-k gate dielectric. Oxygen vacancies or crystalline defects in the grain boundaries have been identified as the possible causes to explain the physical origin of these pre-existing high-k traps, which seems to be an intrinsic materials problem regardless of deposition technique, post-deposition annealing temperature, or heat treatment ambient. Effective measures such as the Si incorporation, plasma nitridation, and fluorine implantation have to be taken to passivate these trapping centers, and the low-frequency C-V measurement in chapter 5 or low-frequency charge pumping method in chapter 6 could be readily used to monitor the amount of high-k traps located near the high-k/base oxide interface.

7. The function form of charge trapping model should be further clarified to explain different time dependences (power law, logarithmic, and stretched exponential growth) observed in this dissertation. An appropriate function form should be the basis to describe and to determine the charge trapping behavior and related

mechanisms with consistent physical concepts. In addition, the implications of time dependence should be further studied to understand the charge trapping behavior (charge filling in the pre-existing traps or additional trap generation).

8. The tunneling path into and out of high-k traps deserves to be further studied to realize the actual energy distribution of high-k bulk traps. Since the temperature and time dependences of charge trapping and de-trapping behaviors suggest the two-step thermal-assisted tunneling process (elastic direct tunneling plus lattice-relaxation multi-phonon emission), the thermal transition among different energy levels (ground and many excited states) by cascade phonon emission should be considered to determine the more accurate energy distribution of high-k traps.
9. Charge trapping and de-trapping into and out of the pre-existing high-k traps should be studied in terms of the 1/f low-frequency noise and random telegraph signal (RTS) methods, which have been widely used in the study of oxide traps. In-depth understanding of different analysis methods could help us distinguish the similarities and discrepancies of charge trapping and de-trapping behaviors in conventional oxides and Hf-based high-k gate dielectrics.

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Appendix A

For the general circuit model of five elements, the equations from equating the total impedance of Fig. 4-1(a) and 4-1(b) could be reduced as eqs. (A-1) and (A-2) if the criteria **tan**δ<<1<<$(\omega C_0 R_p)^2$ are well satisfied. This could also be quickly verified by **tan**δ<0.1 and J_g<0.01 A/cm^2. Then each circuit element could be readily obtained by measuring the dielectric capacitance C and conductance G at two frequencies.

Real: $$\frac{G}{G^2+(\omega C)^2} = R_s + \frac{\tan\delta}{\omega C_0} + \frac{1}{\omega^2 C_0^{\,2} R_p} \tag{A-1}$$

Img: $$\frac{C}{G^2+(\omega C)^2} = -L_s + \frac{1}{\omega^2 C_0} \tag{A-2}$$

First, consider the imaginary part,

$$\frac{C_1}{G_1^{\,2}+(\omega_1 C_1)^2} - \frac{C_2}{G_2^{\,2}+(\omega_2 C_2)^2} = \frac{1}{C_0}\left(\frac{1}{\omega_1^{\,2}} - \frac{1}{\omega_2^{\,2}}\right) \tag{A-3}$$

$$C_0 = \frac{(\omega_2^{\,2}-\omega_1^{\,2})(G_1^{\,2}+\omega_1^{\,2}C_1^{\,2})(G_2^{\,2}+\omega_2^{\,2}C_2^{\,2})}{\omega_1^{\,2}\omega_2^{\,2}[C_1(G_2^{\,2}+\omega_2^{\,2}C_2^{\,2}) - C_2(G_1^{\,2}+\omega_1^{\,2}C_1^{\,2})]} \tag{A-4}$$

$$\frac{\omega_1^{\,2}C_1}{G_1^{\,2}+(\omega_1 C_1)^2} - \frac{\omega_2^{\,2}C_2}{G_2^{\,2}+(\omega_2 C_2)^2} = -L_s(\omega_1^{\,2}-\omega_2^{\,2}) \tag{A-5}$$

$$L_s = \frac{\omega_1^{\,2}C_1(G_2^{\,2}+\omega_2^{\,2}C_2^{\,2}) - \omega_2^{\,2}C_2(G_1^{\,2}+\omega_1^{\,2}C_1^{\,2})}{(\omega_2^{\,2}-\omega_1^{\,2})(G_1^{\,2}+\omega_1^{\,2}C_1^{\,2})(G_2^{\,2}+\omega_2^{\,2}C_2^{\,2})} \tag{A-6}$$

Then, the shunt resistance R_p could be determined from static I_g-V_g measurement ($R_p = V_g/I_g$) since the R_p ($10^8 \sim 10^{12}$ ohm) is much larger than R_s (300 ~ 1500 ohm) in most cases. Then apply this given R_p to obtain R_s and **tan**δ in the real part of the circuit impedance using two-frequency C-V correction method.

$$\frac{G_1}{G_1^{\,2}+(\omega_1 C_1)^2} - \frac{G_2}{G_2^{\,2}+(\omega_2 C_2)^2} = \frac{\tan\delta}{C_0}\left(\frac{1}{\omega_1} - \frac{1}{\omega_2}\right) + \frac{1}{C_0^{\,2} R_p}\left(\frac{1}{\omega_1^{\,2}} - \frac{1}{\omega_2^{\,2}}\right) \tag{A-7}$$

$$\tan\delta = \frac{C_0[\frac{G_1}{G_1^{\,2}+(\omega_1 C_1)^2} - \frac{G_2}{G_2^{\,2}+(\omega_2 C_2)^2} - \frac{1}{C_0^{\,2}R_p}(\frac{1}{\omega_1^{\,2}} - \frac{1}{\omega_2^{\,2}})]}{(\frac{1}{\omega_1} - \frac{1}{\omega_2})} \tag{A-8}$$

$$\frac{\omega_1 G_1}{G_1^{\,2}+(\omega_1 C_1)^2} - \frac{\omega_2 G_2}{G_2^{\,2}+(\omega_2 C_2)^2} = R_s(\omega_1 - \omega_2) + \frac{1}{C_0^{\,2}R_p}(\frac{1}{\omega_1} - \frac{1}{\omega_2}) \tag{A-9}$$

$$R_s = \frac{[\frac{\omega_1 G_1}{G_1^{\,2}+(\omega_1 G_1)^2} - \frac{\omega_2 G_2}{G_2^{\,2}+(\omega_2 C_2)^2} - \frac{1}{C_0^{\,2}R_p}(\frac{1}{\omega_1} - \frac{1}{\omega_2})]}{\omega_1 - \omega_2} \tag{A-10}$$

Or we can use the curve fitting technique to obtain R_p, tanδ and R_s. If we look into the insight of eq. (A-1), the real part of the impedance is similar to the 2nd-order polynomial equation: $y= ax^2 + bx + c$ where $y = \frac{G}{G^2+(\omega C)^2}$, $x = \frac{1}{\omega}$, $a = \frac{1}{C_0^{\,2}R_p}$, $b = \frac{\tan\delta}{C_0}$ and $c = R_s$. Since C_0 is already known from equating the imaginary part of circuit impedance, the coefficients (a, b, and c) obtained from curve fitting results can be transformed into the R_p, tanδ, and R_s. Moreover, these findings can also confirm the hypothesis that R_p can be determined as the shunt resistance from static I_g-V_g measurement.

Appendix B

For ultrathin oxides or very leaky high-k gate dielectrics with tunneling leakage current density J_g>1 A/cm^2, the criteria $\mathbf{tan}^2\delta$<<1<<$(\omega C_0R_p)^2$ may not be valid due to the rapidly decreasing R_p. Since R_p represents the static energy loss due to the tunneling leakage current through the gate dielectric, the dynamic energy loss $\mathbf{tan}\delta$ could be neglected to simply the equations of 5-element circuit model under these circumstances. Thus, the two equations from just equating the total impedance of Figs. 4-1(a) and 4-1(d) in chapter 4 should be employed without any reduction equations. The equated real and imaginary parts of total circuit impedance are listed below as eqs. (B-1) and (B2), respectively:

Real: $$\frac{G}{G^2+\omega^2 C_p{}^2} = R_s + \frac{R_p}{1+(\omega C_0 R_p)^2} \tag{B-1}$$

Img: $$\frac{C_p}{G^2+\omega^2 C_p{}^2} = -L_s + \frac{C_0 R_p{}^2}{1+(\omega C_0 R_p)^2} \tag{B-2}$$

Apply the two-frequency C-V correction method to obtain R_p and $C_0R_p{}^2$:

$$\frac{G_1}{G_1{}^2+\omega_1{}^2 C_{p1}{}^2} - \frac{G_2}{G_2{}^2+\omega_2{}^2 C_{p2}{}^2} = R_p\left(\frac{1}{1+(\omega_1 C_0 R_p)^2} - \frac{1}{1+(\omega_2 C_0 R_p)^2}\right) \tag{B-3}$$

$$\frac{C_{p1}}{G_1{}^2+\omega_1{}^2 C_{p1}{}^2} - \frac{C_{p2}}{G_2{}^2+\omega_2{}^2 C_{p2}{}^2} = C_0 R_p{}^2\left(\frac{1}{1+(\omega_1 C_0 R_p)^2} - \frac{1}{1+(\omega_2 C_0 R_p)^2}\right) \tag{B-4}$$

Divide eq. (B-4) by eq. (B-3) to obtain C_oR_p:

$$C_0 R_p = \frac{C_{p1}(G_2{}^2+\omega_2{}^2 C_{p2}{}^2) - C_{p2}(G_1{}^2+\omega_1{}^2 C_{p1}{}^2)}{G_1(G_2{}^2+\omega_2{}^2 C_{p2}{}^2) - G_2(G_1{}^2+\omega_1{}^2 C_{p1}{}^2)} \tag{B-5}$$

Substitute this C_0R_p into eq. (B-3) or (B-4) to obtain R_p first, and then the C_0 could be obtained from the known C_0R_p and R_p values. In addition, the other two circuit elements R_s and L_s can be obtained from eqs. (B-6) and (B-7) in the same way of

two-frequency C-V correction method:

$$R_s = \frac{\dfrac{G_1[1+(\omega_1 C_0 R_p)^2]}{G_1^{\,2}+(\omega_1 C_1)^2} - \dfrac{G_2[1+(\omega_2 C_0 R_p)^2]}{G_2^{\,2}+(\omega_2 C_2)^2}}{(\omega_1 C_0 R_p)^2 - (\omega_2 C_0 R_p)^2} \tag{B-6}$$

$$L_s = \frac{-\dfrac{C_1[1+(\omega_1 C_0 R_p)^2]}{G_1^{\,2}+(\omega_1 C_1)^2} + \dfrac{C_2[1+(\omega_2 C_0 R_p)^2]}{G_2^{\,2}+(\omega_2 C_2)^2}}{(\omega_1 C_0 R_p)^2 - (\omega_2 C_0 R_p)^2} \tag{B-7}$$

Using this four-element circuit model (C_0-R_p-R_s-L_s) could avoid the possible calculation errors resulting from the reduced equations of five-element circuit model since the assumptions of $\mathbf{tan}^2\delta << 1 << (\omega C_0 R_p)^2$ may not be satisfied anymore. By neglecting the dynamic energy loss $\mathbf{tan}\delta$, only simple algebraic manipulations are needed rather than the complicated iterative, numerical analysis method.

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90 年 9 月-95 年 10 月

博士論文題目:

以二氧化鉿為基底之高介電常數閘極介電層中的電荷捕捉與逃逸之電特性分析

Electrical Characterization of Charge Trapping and De-trapping in Hf-Based High-k Gate Dielectrics

Publication List

Journal Paper:

1. [2點，長文] Wei-Hao Wu, Mao-Chieh Chen, Bing-Yue Tsui, Yong-Tian Hou, Liang-Gi Yao, Yin Jin, Hun-Jan Tao, Shih-Chang Chen, and Mong-Song Liang, "Effects of base oxide thickness and Si composition on charge trapping in HfSiO/SiO_2 high-k gate stacks," *Jpn. J. Appl. Phys.*, vol. 44, no. 8, pp. 5977-5981, 2005.
2. [長文] Wei-Hao Wu, Bing-Yue Tsui, Mao-Chieh Chen, Yong-Tian Hou, Yin Jin, Hun-Jan Tao, Shih-Chang Chen, and Mong-Song Liang, "Transient charging and discharging of border traps in the dual-layer HfO_2/SiO_2 high-k gate stack by low-frequency charge pumping method," submitted to the *IEEE Trans. Electron Devices* for possible publication.

Letter Paper:

1. [3點，短文] Wei-Hao Wu, Bing-Yue Tsui, Yun-Pei Huang, Feng-Chiu Hsieh, Mao-Chieh Chen, Yong-Tian Hou, Yin Jin, Hun-Jan Tao, Shih-Chang Chen, and Mong-Song Liang, "Two-frequency C-V correction using five-element circuit model for high-k gate dielectric and ultrathin oxide," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 399-401, May 2006.
2. [3點，短文] Wei-Hao Wu, Bing-Yue Tsui, Mao-Chieh Chen, Yong-Tian Hou, Yin Jin, Hun-Jan Tao, Shih-Chang Chen, and Mong-Song Liang, "Spatial and energetic distribution of border traps in the dual-layer HfO_2/SiO_2 high-k gate stack by low-frequency capacitance-voltage measurement," accepted by the *Appl. Phys. Lett.* and will be published soon.
3. [短文] Wei-Hao Wu, Bing-Yue Tsui, Mao-Chieh Chen, Yong-Tian Hou, Yin Jin, Hun-Jan Tao, Shih-Chang Chen, and Mong-Song Liang, "Charge trapping and de-trapping behaviors in the dual-layer HfO_2/SiO_2 high-k gate stack under static and dynamic positive bias stress," submitted to the *IEEE Electron Device Lett.* for possible publication.

International Conference Paper:

1. [1點] Wei-Hao Wu, Mao-Chieh Chen, Ming-Fang Wang, Tuo-Hung Hou,

Liang-Gi Yao, Yin Jin, Shih-Chang Chen, and Mong-Song Liang, "Effects of base oxide in $HfSiO/SiO_2$ high-k gate stacks," *IEEE the 11th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2004, pp. 25-28.

2. Wei-Hao Wu, Mao-Chieh Chen, Ming-Fang Wang, Tuo-Hung Hou, Liang-Gi Yao, Yin Jin, Shih-Chang Chen, and Mong-Song Liang, "Effects of base oxide and silicon composition on charge trapping in $HfSiO/SiO_2$ high-k gate stacks," *Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials*, Tokyo, 2004, pp. 740-741.
3. Wei-Hao Wu, Yong-Tian Hou, Yin Jin, Hun-Jan Tao, Shih-Chang Chen, Mong-Song Liang, Bing-Yue Tsui, and Mao-Chieh Chen, "Threshold voltage instability in nMOSFETs with $HfSiO/SiO_2$ high-k gate stacks," *Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials*, Kobe, 2005, pp. 498-499.
4. Bing-Yue Tsui, Yun-Pei Huang, Feng-Chiu Hsieh, and Wei-Hao Wu, "A new method to correct capacitance of high-leakage ultra-thin gate dielectric," *Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials*, Kobe, 2005, pp. 496-497.

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