國 立 交 通 大 學

光電工程研究所

博 士 論 文

主動顯示器用低溫多晶矽薄膜電晶體之元件特性與補償電路研究

Study on Characterization and Compensation Circuits of Low-Temperature Polycrystalline Silicon Thin-film Transistor for Active Matrix Displays

研 究 生：盧皓彥

指導教授：祁　甦　教授

張鼎張　教授

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研 究 生：盧皓彥　　Student: Hau-Yan Lu

指導教授：祁　甦　博士　　Advisor: Dr. Sien Chi

張 鼎 張 博士　　Dr.Ting-Chang Chang

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摘要

本論文首先提出一種具有金屬遮光層(Metal shielding layer)的新穎低溫多晶矽薄膜電晶體元件結構。於玻璃基板上先沉積一層金屬薄膜，並依序沉積緩衝層(Buffer layer)與非晶矽薄膜，再利用主動層之光罩進行一次蝕刻，如此並不會增加光罩數，此遮光層可以阻擋背光照射到多晶矽層，完全消除光漏電與次臨界擺幅(Sub-threshold swing)於背光環境下之劣化，然而，此新式結構低溫多晶矽薄膜電晶體之臨界電壓於暗態下會隨著汲極電壓而飄動，由於金屬遮光層與汲極電極互相重疊，形成一寄生電容，汲極電壓會經由此寄生電容耦合至金屬遮光層中，造成一電壓分佈於其中，進而影響元件之臨界電壓；為了消除此一問題，我們將金屬遮光層利用額外一道光罩來定義其圖案，並研究此部分金屬遮光層位於通道中央或接面區之元件特性，具有部分金屬遮光層之元件，無論遮光層位於哪一區，

其臨界電壓皆不再隨汲極電壓而改變，此外，當部分金屬遮光層位於汲極接面區時，能夠有效的抑制光漏電流之大小，反之，置於源極接面區或中央通道區之部分遮光層皆無降低光漏電流之功效，然而，一旦施加大的汲極電壓，位於汲極接面之金屬遮光層其遮光效果便會減弱，我們亦根據所獲得之實驗數據提出了一合理模型來解釋此現象。

此外，我們亦嘗試對緩衝層之成分與其表面進行調變來抑制光電流的產生，本論文提出了一種可吸收光源之介電層作為緩衝層，可將大部份之背光吸收，所以多晶矽層所吸收的光強度便會減少，進而達到降低光漏電的效果，此光吸收緩衝層主要為富含矽(Si-rich)之二氧化矽層或是矽化氮層，實驗發現，富含矽介電層之光吸收能力與其薄膜厚度成正比，不論是使用富含矽之二氧化矽層或是矽化氮層來製作元件，皆可達到３０％～５０％的光漏電流改善。此外，本論文亦對一般緩衝層之表面進行氨電漿(NH_3 plasma)處理，利用氨電漿對緩衝層表面進行轟擊(Bombardment)，使其表面裂化以產生大量之介面缺陷，此製程不僅不需要增加額外的光罩數，且可以完全相容於一般標準製程，而緩衝層表面電漿處理過之元件其基本特性與主要參數皆與標準元件相同，沒有金屬遮光層結構臨界電壓飄移的問題，如此一來，光激發出的電子－電洞隊將可透過多晶矽薄膜與緩衝層介面之缺陷密度進行複合，可有效降低光漏電與改善照光下之元件次臨界擺幅。

本論文也研究探討多晶矽薄膜電晶體元件於照光下之光漏電與次臨界擺幅增加的物理機制，首先將緩衝層利用氬離子(Argon)佈植進行表面轟擊，使多晶矽薄膜與緩衝層介面產生許多缺陷密度，我們發現經由緩衝層表面轟擊之元件，其光漏電與照光下次臨界擺幅特性具有顯著的改善，由於多晶矽薄膜吸收被光後會產生許多電子－電洞對，透過引入之缺陷密度可減少光致電子與電洞，因而造成較低的光漏電流與較佳的次臨界擺幅，此外，一種新式的測式結構亦在本論文中被提出，利用圖案化之金屬遮光層結構，我們可定義照光區於汲極或源極接面區，其中當照光區位於源極接面且施加大汲極電壓時，照光下次臨界擺幅有著顯著的上升，因此，根據此實驗結果，可推論次臨界擺幅於照光下之機制並於本論文中提出物理模型與能帶圖以解釋之。

由於多晶矽薄膜電晶體能夠整合週邊驅動電路進而由於多晶矽元件應用於面板週邊驅動邏輯電路時，需要考量到多晶矽元件可靠度的問題，本論文中亦以電容－電壓法(Capacitance-Voltage measurement)來研究低溫多晶矽薄膜電晶體於交流操作下之可靠度，研究中發現交流訊號測試會造成元件導通電流嚴重的下降，但其起始電壓變化並不大，同時汲/源極寄生電阻的也急劇增加，此外，元件劣化後之低頻電容電壓曲線無明顯變化，但高頻下之電容電壓曲線卻隨著閘極正電壓而變化，說明了多晶矽薄膜電晶體於交流操作下之劣化機制主要為淺態能階(Tail state)的增加而深態能階(Deep state)密度並無太大變化，同時透過電容電壓曲線，我們也發現交流訊號所產生之淺態能階為對稱分佈於源極與汲極。此外，具有橫向結晶之低溫多晶矽元件於交流訊號下之可靠度亦在此論文中被研究，我們可以將橫向結晶晶晶界(Grain boundary)分為主晶界(main-GB)與次晶界(sub-GB)，主晶界的特徵在於其分布方向垂直元件通道，並且為一突起(Protrusion)結構；次晶界則是平行通道方向且較平坦，論文中挑選兩種較明顯對比之電晶體進行分析，GB-TFT 為一含有主晶界在通道中央，NGB-TFT 中則僅有次晶界存在，經過施加交流訊號測試，發現 GB-TFT 之劣化情形較 NGB-TFT 嚴重，我們量測了此兩種元件之電容電壓曲線並進行通道電場電腦模擬，發顯 GB-TFT 之突起結構將會造成尖端電場效應，使得此區聚集的載子較多，進而在源極與汲極兩端之高電場下造成元件的劣化。

本論文也提出了一種用於有機電激發光顯示器(AMOLED)之補償畫素電路設計，此電路設計包含了五顆低溫多晶矽薄膜電晶體與一儲存電容結構，由於低溫多晶矽薄膜電晶體其均勻度受到結晶晶界的影響，畫素之間的元件特性皆不相同，使得各畫素輸出亮度會友不均勻的情形，同時，由於金屬導線之電阻效應會造成電壓供應端(V_{DD})經過長距離導線時產生一電壓下降的現象，此現象亦會造成有一電激發光顯示器畫面亮度有沿著某方向遞減的情形，本論文所提出的畫素電路與新補償方法可在一次操作中同時消除元件臨界電壓飄移與電壓源下降所導致之輸出電流變動，經由 HSPICE 軟體的驗證，此電路設計可用於高解析度與

大尺寸之有機電激發光顯示器中。

本論文最後研究提出一種利用非晶矽薄膜電晶體之有機電激發光顯示器畫素設計，由於非晶矽薄膜電晶體具有良好的元件均勻度與相當低的製造成本，非常適合做為有機電激發光顯示器之背板(Backplane)，然而非晶矽薄膜電晶體之臨界電壓會隨著操作時間而上升，且有機電激發光二極體之起始電壓亦有隨著使用時間增加的趨勢，造成輸出亮度之下降，此新式非晶矽薄膜電晶體畫素設計利用源極隨耦器(Source follower)之概念，不僅結構與補償步驟簡單，並可同時補償元件臨界電壓與有機電激發光二極體起始電壓的影響，可應用於大尺寸有機電激發光顯示器。

Study on Characterization and Compensation Circuits of Low-Temperature Polycrystalline Silicon Thin-film Transistor for Active Matrix Displays

Student: Hau-Yan Lu **Advisor: Dr. Sien Chi**
Dr. Ting-Chang Chang

Department of Photonics & Institute of Electro-Optical Engineering
College of Electrical and Computer Engineering
National Chiao Tung University

Abstract

A novel technology to eliminate the photo leakage current of poly-silicon thin film transistor (poly-Si TFT) with top gate is developed. A thin metal film is formed on the glass substrate to be used as light-shielding layer. The light-shielding layer, buffer layer and active island are patterned by employing the same mask. The leakage current and the variation of sub-threshold swing in the proposed devices are suppressed completely under illumination. Owing to the parasitic capacitance in the overlap region between the drain side and the metal shielding layer, a floating voltage coupled from drain bias would influence the threshold voltage of the proposed poly-Si TFTs. In order to solve this issue, a partial metal shielding structure for poly-Si TFT is

studied. The metal shielding layer is formed and etched to be located in the channel region and junction regions. According to this structure, the shift of threshold voltage with increasing drain bias is entirely eliminated. Furthermore, the photo leakage current of poly-Si TFT with partial metal shielding layer located in the drain junction is suppressed. However, the shielding effect is vanished as the drain voltage is high. Based on these data, this study also proposes a model to explain the mechanism of partial metal shielding layer located at drain side for lowing photo leakage current.

In addition, poly-Si TFT with light absorption structure is proposed to lower the photo leakage. No need of adding process steps or number of masks, the oxide film or SiN_X film of buffer layer is replaced by Si-rich dielectric films. By this method, the photo leakage can be markedly lowered and the degradation of sub-threshold swing is also reduced. It is observed that the light absorption capacity of Si-rich dielectric material is strongly proportional to the film thickness. In addition, the technology of poly-Si TFTs with low photo leakage current is developed in this work. The electrical characteristics of poly-Si TFT under illumination were significantly improved employing the NH_3 plasma treatment on the buffer layer, no need for complicate device structure and additional masks. The generation of trap states originated from the plasma bombardment on the interface between poly-Si layer and buffer oxide can effectively recombine the light-induced electron-hole pairs. The fewer residual electron-hole pairs in the bottom of poly-Si layer leads to the lower photo leakage current and improved sub-threshold swing, as well as also maintain the good electrical characteristics in the dark sate.

Next, poly-Si TFTs with different process flows are used to investigate the electrical characteristics under illumination. First, the surface of buffer layer of poly-si TFT is degraded by Argon ion implant to generate plenty of trap densities on the interface of poly-Si layer and buffer layer. The photo leakage current and the

degradation of sub-threshold swing are improved substantially, compared to the conventional poly-Si TFT. It is attributed to that the light induced electron-hole in the bottom of poly-Si film may be recombined directly via the surface state densities. Therefore, the fewer electrons and holes lead to the lower photo leakage current and less increase of sub-threshold swing, respectively. Moreover, The electrical characteristics of poly-Si TFTs with patterned metal shielding layer under illumination are investigated in this study. The location of the exposure region in poly-Si layer is well defined by employing the proposed structure. The photo leakage current increases obviously as the exposure region is located in drain junction. Therefore, the drain junction under light exposure is effective region to induce the photo leakage current. However, the sub-threshold swing of TFT under illumination is significantly degraded while the exposure region is located in source junction with high drain voltage. It is indicated that the key factors to affect the sub-threshold swing is the residual excess holes accumulated in source junction. From the results of poly-Si TFT with degraded buffer layer and partial metal shielding layer, the model for mechanism of increased sub-threshold swing under illumination is proposed.

The electrical degradation of n-channel poly-Si TFT has been investigated under dynamic voltage stress by capacitance-voltage (C-V) measurement. In C-V measurements, the fixed charges in the gate oxide film of TFTs are not affected by the applied small signal, whereas the trap states in the band gap would respond to the applied frequency, so that the dominant degradation mechanism of poly-Si TFTs can be evaluated. Our experimental results show that the degradation of n-type TFTs is caused by additional trap states located at the drain and the source junction in the poly-Si thin film. Furthermore, through the experimental results of the C-V characteristics measured at 10 kHz and 1 MHz, we can infer that the tail states produced by the strained bounding in poly-Si film are mostly responsible for the

electrical degradation of n-channel poly-Si TFTs after dynamic stress. In addition, this work also studies the electrical degradation of laterally grown poly-Si TFTs under dynamic voltage stress. The experimental results show the severity of the degradation of poly-Si TFTs with a protruding grain boundary. The concentration of the electric field in the protrusion region was verified by capacitance-voltage measurements and simulation of the device characteristics. These results reveal that more electrons are induced at the grain boundary of the poly-Si channel because of the relatively high electric field in the protrusion region. Based on these data, this study proposes a model to explain the enhanced electrical degradation of poly-Si TFTs with a protruding grain boundary, generated by laser-crystallized lateral growth technique.

A new pixel design and driving method for active-matrix organic light emitting diode (AMOLED) display using poly-Si TFT is proposed. The new circuit consists of five TFTs and one capacitor to eliminate the variation in the threshold voltage of the TFTs, and the drop in the supply voltage in a single frame operation. The proposed pixel circuit has been verified to realize uniform output current by the simulation work using HSPICE software. The simulated error rate of the output current is also discussed in this paper. The novel pixel design has great potential for use in large size and high resolution AMOLED displays. Finally, this work also presents a new a-Si:H pixel circuit with source-follower type compensation method for large-size AMOLED displays. The proposed pixel circuit consists of five TFTs and one capacitor to compensate the shift in the threshold voltage of the driving TFT and OLED used in AMOLED and the compensation process is simplified by the proposed driving scheme. The high immunity to degradation of TFT and OLED in proposed pixel has been verified by the simulation work using HSPICE software. The novel pixel design has great potential for use in large-size AMOLED displays.

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盧 皓 彥

誌於風城交大

2008 年 仲夏

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Chapter 1

Introduction

1.1 General Background

Thin film transistor (TFT) is a metal-oxide-silicon field effect transistor (MOSFET) fabricated on an insulator substrate by employing all thin film constituents. Thin film transistors have been widely used as switching devices in flat panel display, such as active-matrix liquid crystal display (AMLCD) [1.1-1.5] and active-matrix organic light emitting diode (AMOLED) display [1.6-1.10]. The active layers of thin film transistors can be mainly divided into two types, amorphous silicon (a-Si) and poly-crystalline silicon (poly-Si), according to the crystallization status. The hydrogenated a-Si (a-Si:H) TFT is commonly applied in large size active matrix displays (AMDS) due to its highly mature process, low manufacturing cost and good device uniformity. However, the threshold voltage of a-Si:H TFT would increase with long time operation. Therefore, the poor stability limits the application of a-Si TFT in AMDs. On the contrary, poly-Si TFT is suitable for the high-resolution, compact size active matrix display in mobile electrical products. Since mobility and stability of poly-Si TFT is higher than a-Si TFT, it offers a promising solution to realize the "System on Panel" technology. The high driving capability and existence of complementary devices lead to integrate functional and driver circuits on the glass substrate. The improvement of electrical characteristics and understanding of degraded mechanism of poly-Si TFTs is important for development of advanced mobile display technology. In addition, AMLCD requires back-light source to display

input image. However, poly-Si TFT operated in illumination environment exhibits an undesired high leakage current to affect the function of pixel switch [1.11].

Furthermore, AMOLED technology with high brightness, high color saturation and fast response time has attracted more and more attention worldwide. Since the brightness of OLED is strongly dependent of driving current, it needs a well-controlled current source to provide the uniform brightness among numerous pixels. Since the main backplane technologies of AMLCD, a-Si TFT and ploy-Si TFT have been developed in the past 20 years, they can be directly taken as the pixel switch and the driving current source for AMOLED. Using excimer laser to re-crystalline a-Si active layer, poly-Si TFT can offer very high current capability. However, the laser re-crystallization process also generates plenty of the grain boundaries in poly-Si TFT, leading to poor uniformity and very huge variation due to the narrow laser process windows for producing large grain size poly-Si TFT. The fluctuation of pulse-to-pulse laser energy and non-uniform laser beam profile make laser energy density hard to hit the super lateral regime everywhere. The random grain boundaries and traps exist in the channel region [1.12-1.14]. This will cause serious non-uniformity of brightness in AMOLED panel. Since the device-to-device uniformity is hard to control, it is essential to develop circuits to compensate the variation. Another one of promising approaching for AMOLED backplane is to use a-Si TFT because of its many advantages, including simple manufacturing process low-cost in large size panel and good device uniformity. However, it had been reported that the threshold voltage of a-Si TFT would shift during operation with increasing time [1.15-1.16]. The increasing threshold voltage of a-Si TFT would reduce the current driving capability to result in the lower brightness of OLED after long time operation. In addition, the threshold voltage of OLED is also shifted with

time. Therefore, the current originated from a-Si TFT would be very sensitive to the OLED degradation.

1.2 Motivation

Hydrogenated amorphous silicon (a-Si:H) technology is quite attractive in AMDs due to its low processing temperature and low manufacture cost. The bottom gate inverted-staggered back-channel-etched (BCE) type of a-Si:H TFT shown in Fig 1.1 has been widely used as a switching element to control the gray level in AMLCD and to drive AMOLED. AMLCD panels are usually used in an illumination environment such as under the back-light. Therefore, the leakage current of TFT under back-light illumination in TFT-LCD displays should be reduced to avoid losing the storage charges in the pixel. Although photo leakage current of inverted staggered a-Si:H TFT was also a serious problem, it had been solved by light-shielding structure proposed by Akiyama *et al*.

Compared with a-Si:H TFT technology, the poly-Si TFT technology has some distinct advantages but its manufacture is more complex and high cost. The major advantage of poly-Si TFT is the higher field effective mobility than that of the amorphous silicon (a-Si) based devices. The high carrier mobility and the existence of complementary pairs permit the integration of drive circuits and the smaller area of pixel transistor. The integration of drive circuits could reduce manufacturing costs, and increase the functionality of large-area microelectronics [1.17-1.18]. The smaller area of pixel transistor leads to a larger aperture ratio for a given pixel size, or enables a high resolution display for a given aperture ratio, resulting in fine image quality for mobile display. Recently, the demand of high-end mobile electronic products such as

cell phone, digital camera, GPS, mobile TV and so on is continuing to grow, so that the development of mobile displays with high resolution and high image quality is inevitable. Since most of people would like to use mobile electronic products outdoors under the sunlight, the readability in ambient illumination is a critical issue for mobile displays. To meet the requirement of superior readability under sunlight, the brightness of backlight becomes higher and higher. However, poly-Si TFTs operated in the high illumination environment exhibit substantial photo leakage current and degraded sub-threshold-swing (S.S), leading to the errors of gray level and difficulty in pixel design.

In addition, the application of circuit integration using poly-Si TFT continuously grow up as device characteristics improve further. Enlarging the grains in poly-silicon layers is an effective approach for improving TFT performance. Several poly-Si re-crystallization methods based on laterally grown grains have been proposed to enlarge the grains and control the location of the grain boundaries [1.19-1.20]. In poly-Si TFT devices, however, the status of defect states at grain boundaries plays a crucial role for electrical characteristics, as shown in Fig. 1.2 and Fig. 1.3. The stability of poly-Si TFT is one of the important issues for poly-Si technology. Recently, the researches about the stabilities of conventional excimer laser-crystallized (ELC) poly-Si TFTs have been reported. The creation of trap states at poly-Si/gate dielectric interface or the charge trapping in the gate insulator is responsible for the degradation in electrical characteristics of poly-Si TFTs. Since TFT devices in driving circuits are frequently subjected to high-frequency voltage pulses, the degradation behavior under dynamic stress is a critical issue for integrated peripheral circuits.

AMOLED displays have been widely developed due to their high brightness, high

efficiency, fast response time and wide viewing angle. Although poly-Si TFT is considered as the main backplane technology for AMOLED, the device variation is still a most critical issue to implant AMOLED panel with good image quality. The conventional 2T1C pixel shown in Fig. 1.4 directly suffers from the non-uniformity of brightness among pixels. For the demand of large size AMOLED panel, this problem will become more and more serious. To solve this issue, several methods have been proposed to compensate for the variation in poly-Si TFT characteristics. The pixel circuit of AMOLED displays can be divided into two catalogs, including voltage driving and current driving methods [1-21-1.22]. The current driving method can provide an excellent uniformity of brightness. However, it need a long time to driving panel for high resolution displays. The voltage driving method can compensate for the variation of the threshold voltage and is easy to integrate poly-Si TFT drivers on the glass substrate. Therefore, the voltage driving method would be considered as a great potential solution for eliminate the variation of poly-Si devices.

In addition, recently, a-Si:H TFT attract much attention to be taken as pixel element for large size and low cost panels in AMOLED display because of its good uniformity and simple fabrication process [1.23-1.24]. However, the threshold voltage shift of a-Si:H TFT over time under operation is another critical issue to degrade the image quality on AMOLED panels [1.25]. Moreover, since OLED is placed on the source node of a-Si:H TFT in the conventional pixel circuit and I_{OLED} is determined by V_{GS} of the driving TFT, the threshold voltage shift in OLED raise the source voltage of the driving TFT to decrease the driving current..

In this thesis, the electrical characteristics of poly-Si under illumination are studied in detail. In order to solve the photo leakage current problem, a metal shielding layer structure for poly-Si TFT is used for top gate poly-Si TFT structure. From the SEM

image and transfer curves of poly-Si TFT with metal shielding layer, the elimination of photo leakage current and increase in S.S are confirmed. However, V_{TH} of poly-Si TFT with metal shielding layer would shift with the drain bias. Therefore, a simple method to improve the electrical characteristics of poly-Si TFT under illumination and maintain the original key parameters is proposed. In addition, the behavior of S.S under illumination is also discussed based on the result of proposed test devices. An energy band diagram is proposed to explain the degradation of S.S under light exposure. Furthermore, the mechanism of conventional ELC poly-Si TFT under dynamic stress is investigated by voltage-capacitance measurement. We also proposed a model to describe the degradation of laser-crystallized laterally grown poly-Si under dynamic stress. For the application of poly-Si TFT in AMOLED, a 5T1C design is proposed to eliminate the V_{TH} variation of poly-Si TFT and the voltage drop of supply power in one time operation. Additionally, a simple pixel circuit composed of 4T1C with source follower type compensation is presented to release the issue of degradation in a-Si TFT and OLED.

1.3 Thesis Organization

In this thesis, novel methods to lower the leakage current and improve the sub-threshold swing of low-temperature polycrystalline silicon thin film transistors (poly-Si TFT) under illumination were proposed. Furthermore, the models of electrical characteristics of poly-Si TFT under illumination were investigated and established in detail. In addition, the new compensation pixel circuits and driving schemes for AMOLED employing poly-Si TFT and a-Si:H TFT were developed in this work. The dissertation is organized in to the following chapters:

In chapter 1, a brief overview of TFT technology and the pixel circuit for AMOLED displays are introduced. We describe the trend and issues of poly-Si TFT development and the problems of TFT applied for the element device of AMOLED pixel circuits. Then, the outline throughout the dissertation is discussed here.

In chapter 2, a new structure of top gate poly-Si TFT to eliminate the photo leakage was first proposed. By this structure, the photo leakage and degradation of sub-threshold swing in poly-Si TFT under illumination are totally eliminated. However, the threshold voltage of device with this structure would shift as drain bias is increasing. Therefore, a modified shielding structure of poly-Si TFT with low photo leakage current is developed to release this issue.

In chapter 3, the buffer layer is modified to improve the electrical characteristics of poly-Si TFT under illumination. A Si-rich dielectric film is taken as the buffer layer to absorb the backlight. Therefore, the light absorbed by poly-Si layer is reduced to lower photo leakage current and sun-threshold swing. Furthermore, the state densities in the interface of poly-Si film and buffer layer are induced by NH_3 plasma treatment on the surface of buffer layer. The light-excited electrons and holes would recombine directly via the extra state densities. The fewer excess electron-hole pairs lead to the less photo leakage current and sub-threshold swing.

In chapter 4, the mechanism of photo leakage current and the increase of sub-threshold swing in poly-Si TFT under illumination are studied in detail. By the results of treated poly-Si TFT, the excess electron-hole pairs in the bottom of poly-Si film are the main factor to influence the electrical characteristics of device operated in the backlight environment. Furthermore, the patterned metal shielding layer is used to control the light exposure region in the source or drain junction. Based on the experimental results, the effective factors to degrade the sub-threshold swing and raise

the photo leakage current are verified.

In chapter 5, the AC stress effect of poly-Si TFT with excimer laser crystallization (ELC) and laser-crystallized laterally grown grain is studied. The generated tail state densities in the source and drain junction in confirmed by capacitance-voltage (C-V) measurement. In addition, the grain boundary effect in reliability of poly-Si TFT under AC stress is investigated.

In chapter 6, a novel poly-Si TFT pixel circuit and driving scheme is proposed. It is composed of five poly-Si TFT and one capacitor. The control line is two lines, including [n]scan and [n]EM. The function of this design is verified by simulation work using HSPICE software. Furthermore，a simple pixel a-Si:H TFT circuit and driving scheme is proposed. It is composed of five a-Si:H TFT and one capacitor to compensate for the shift in the threshold voltage of driving TFT and OLED at one time operation. The function of this design is verified by simulation work using HSPICE software.

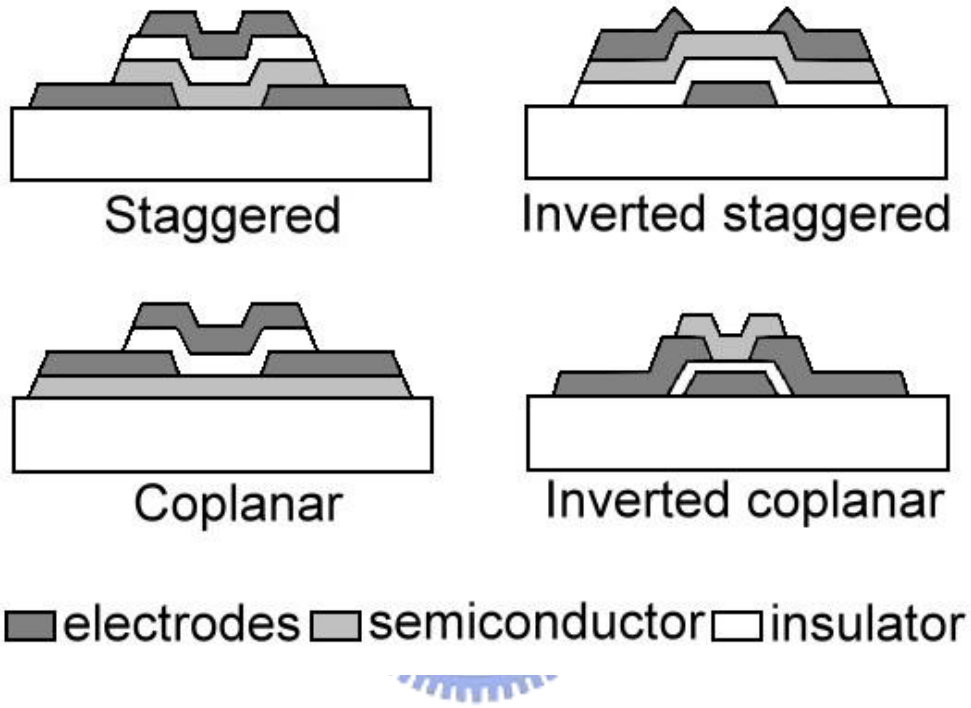


Fig. 1-1 Four device structures for a-Si:H TFTs.

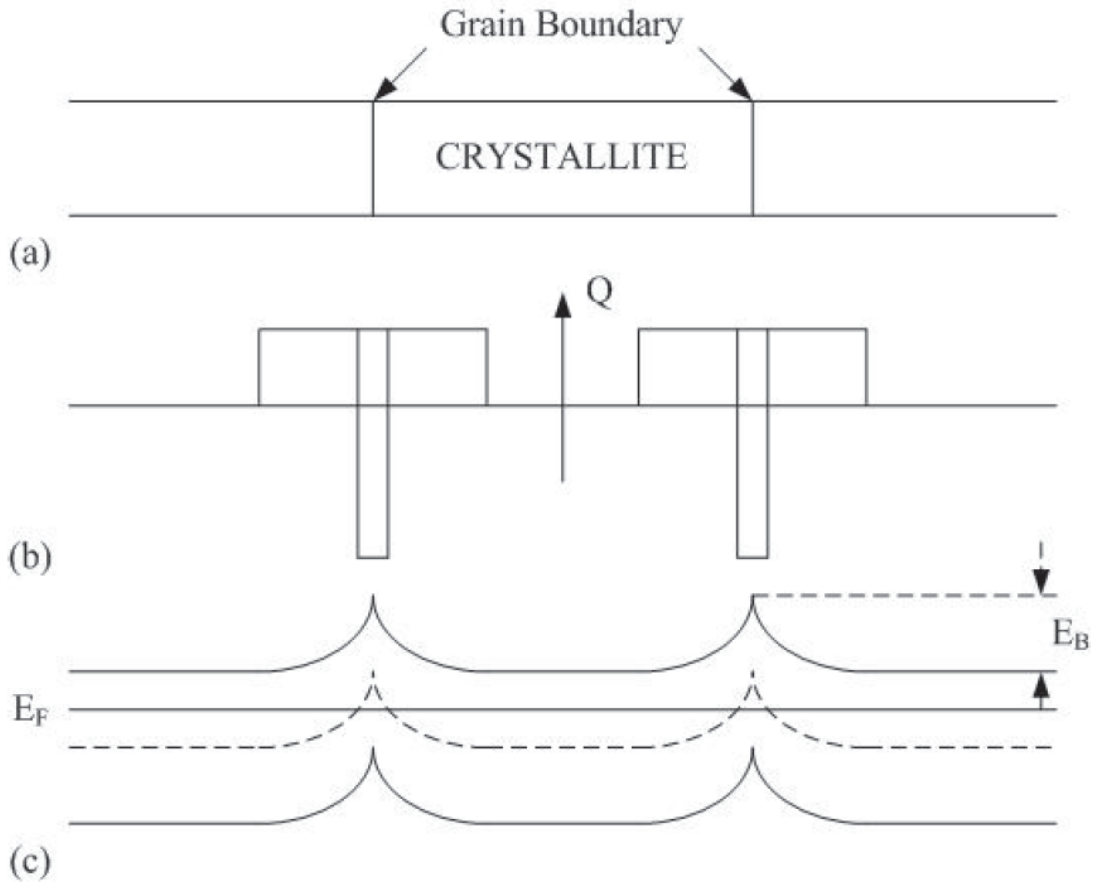


Figure 1-2 (a) Model for the crystal structure of polysilicon films. (b) The charge distribution within the crystallite and at the grain boundary. (c) The energy band structure of the polysilicon crystallites

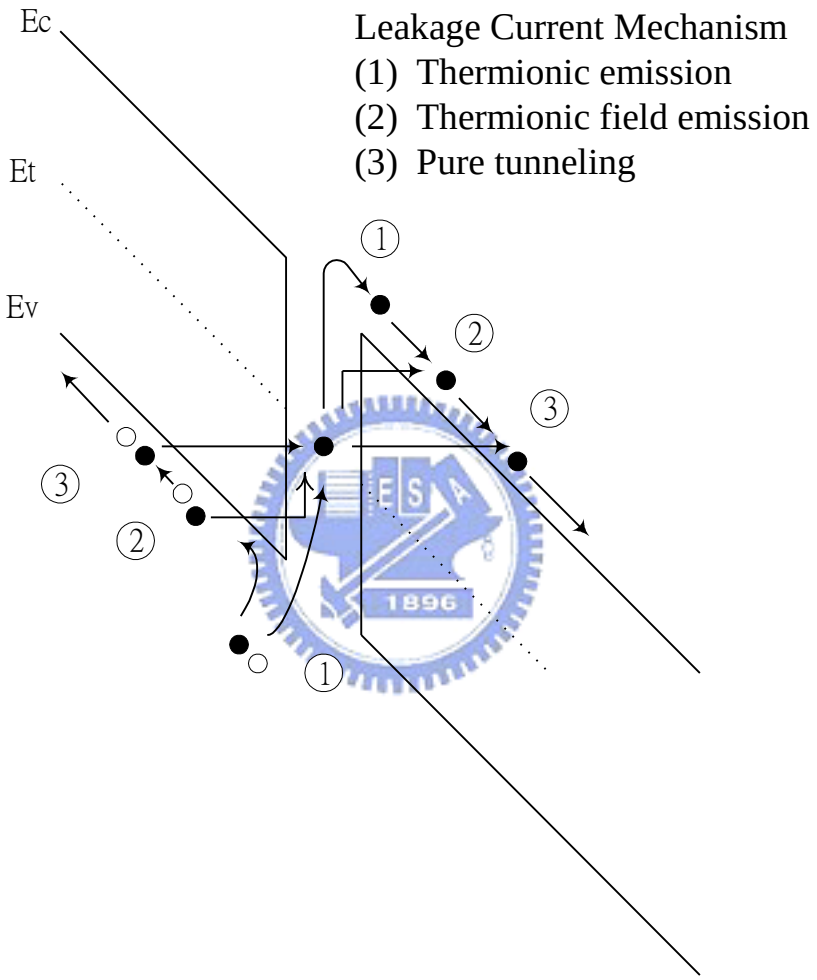


Fig. 1-3 Three possible mechanisms of leakage current in poly-Si TFTs, including thermionic emission, thermionic field emission and pure tunneling.

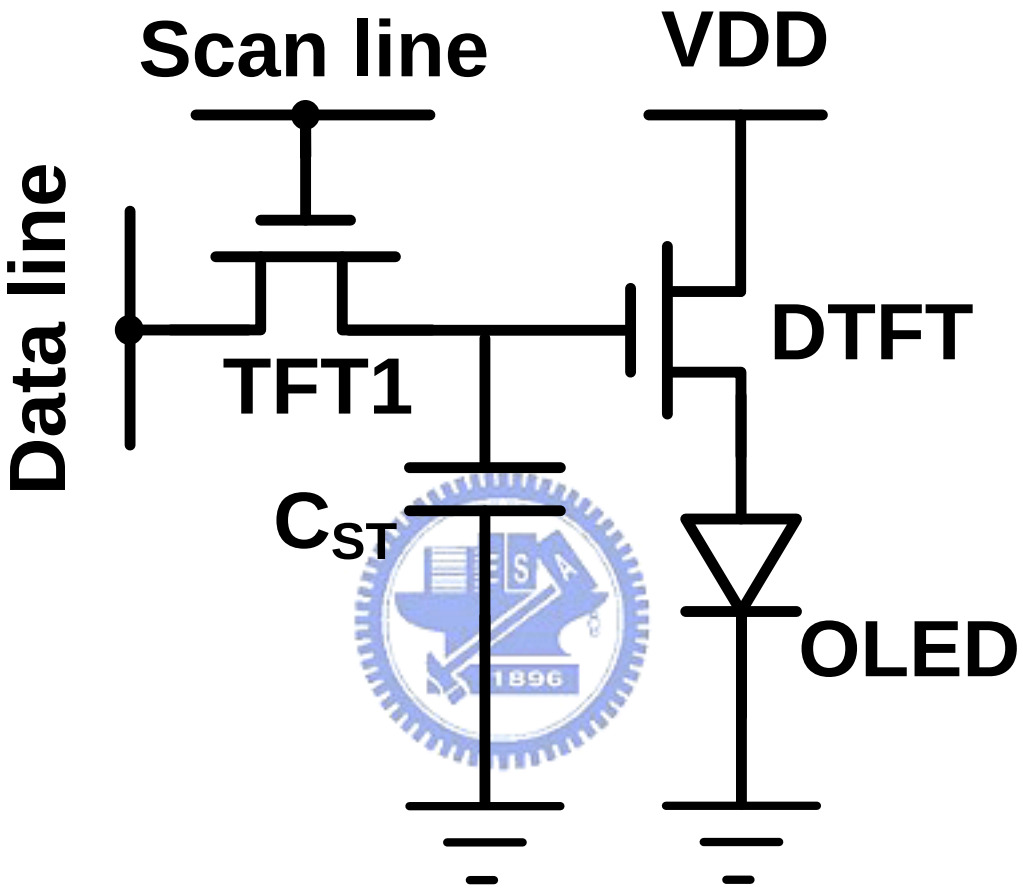


Fig. 1-4 Diagram of conventional 2T1C pixel structure for AMOLED displays

Chapter 2

Polycrystalline Thin Film Transistor with Metal Shielding Layer

2.1 Introduction

Low-temperature polycrystalline-silicon thin film transistors (poly-Si TFTs) have been widely investigated for flat-panel applications such as active matrix liquid crystal display (AMLCD) and active matrix organic light-emitting diode display (AMOLED) [2.1-2.3]. Recently, the demand of high-end mobile electronic products such as cell phone, digital camera, GPS, mobile TV and so on is continuing to grow rapidly, so that the development of mobile displays with high resolution and high image quality is inevitable. Since most of people would like to use high-end mobile electronic products outdoors under the sunlight, the readability in ambient illumination is a critical issue for mobile displays [2.4-2.5]. To meet the requirement of superior readability under sunlight, the brightness of backlight becomes higher and higher. However, poly-Si TFTs operated in the high illumination environment exhibit substantial photo leakage current (I_{PLC}). The leakage current of TFT under back-light illumination in AMLCD displays should be reduced to avoid losing the storage charges in the pixel. Therefore, the voltages that are held across the pixel electrodes would be diminished to affect the gray level controlling, which in turn, would cause a low contrast ratio and error color display. Although I_{PLC} of inverted staggered a-Si:H TFT was also a serious problem, it had been solved by light-shielding structure proposed by Akiyama *et al* [2.6]. Since the gate metal is normally under a-Si:H layer for inverted staggered structure, the light-shielding structure can be performed easily

by patterning a-Si:H layer to be located totally inside the gate metal. Figure 2.1(a) shows the conventional poly-Si TFT structure. It is a top gate structure, indicating the gate metal is on the top of active layer, so that light form back-light directly emit into poly-Si film to be absorbed, generating I_{PLC} and increasing sub-threshold swing (S.S). However, the studies for lowering I_{PLC} in poly-Si TFTs with top gate structure are very few [2.7-2.8].

In this chapter, we propose a new light-shielding structure for poly-Si TFT with top gate to eliminate the I_{PLC} originated from the illumination of back-light. The I_{PLC} and the S.S variation of proposed TFTs are entirely cancelled by the light-shielding layer. In addition, the electrical characteristics of poly-Si TFTs with light-shielding layer are investigated first. As drain bias changes, the shift of threshold voltage (V_{TH}) of poly-Si TFT with metal shielding layer is observed, inducing the un-saturation phenomenon of I_D-V_D characteristics. Therefore, the V_{TH} of poly-Si TFT is affected by the insert metal shielding layer. In order to solve the variation of V_{TH} with drain bias, the metal shielding layer is patterned to be partially under poly-Si layer. The location of partial metal shielding layer is designed to be channel or close to junction region. The relationship between location of partial metal shielding layer and effect of lowering I_{PLC} is discussed as device is operated in linear and saturation regions.

2.2 Full Metal Shielding Layer Structure

2.2.1 Experimental Procedure

The poly-Si TFTs with top gate p-channel and lightly doped drain (LDD) structure were fabricated on Corning1737 glass substrate. First of all, an 80nm thick molybdenum film was sputtered to be a shielding layer on the glass substrate. The buffer layer and a thin 50 nm-thick un-doped amorphous-Si (a-Si) film were

sequentially deposited by plasma enhanced chemical vapor deposition (PECVD) at 380℃, followed by dehydrogenated via furnace annealing process at 450℃. Then the a-Si films were crystallized by 308nm XeCl excimer laser with the line-shaped beam power of 350mJ/cm^2. The active island, the buffer and the light-shielding layers were patterned using the same mask by plasma dry etching. The 100nm thickness gate insulator was deposited by tetraethyl orthosilicate base (TEOS) oxide. The source/drain regions were defined by a mask and formed by the mass-separated ion implanter technique. Then, MoW was sputtered and patterned as a gate metal. Following, implantation for LDD region is preformed on overall device after the S/D photo resistor is removed. The doping activation was performed by RTA irradiation. The dimensions of TFTs in this work were L = 6 μm, W = 6 μm and the LDD length is 1.25 μm. The brightness of back-light for photo state measurement is set as 3000nits. In the manufacture process, the number of masks is equal to the conventional poly-Si TFT procedure.

2.2.2 Results and Discussion

The cross-sectional view of proposed TFT is illustrated in Fig. 2.1(b). A thin metal film is deposited on the glass substrate to block the light emitted into poly-Si thin film. For the AMLCD application, most pixel regions should be allowed light to pass through so that the metal shielding layer must be patterned to be an opaque area only for the poly-Si active island. To simplify the manufacture process, the metal shielding layer, buffer layer and active island layer are patterned in the same mask employing plasma dry etching process. Therefore, the process of the proposed structure is compatible with conventional one. Figure 2.2 shows the SEM image of poly-Si TFT

with the light-shielding layer. After one time etching process, the triple layers, including metal film, buffer oxide and poly-Si film, show a taper-like shape and the area of metal layer is larger than that of the active layer. Since the poly-Si island is completely located inside the coverage of metal shielding layer, the result confirms that the proposed device exhibits a strong immunity to high brightness illumination.

Figure 2.3 shows the I_D-V_G transfer curves of standard poly-Si TFT at the linear operation under the dark and photo states. The leakage current of poly-Si TFTs in the dark was around 10^{-13} A as the gate bias is varied from 0 to -12 V. With the same range of gate bias, the leakage current of poly-Si TFTs under illumination is as high as two orders of magnitude, about 10^{-11}A. It is clearly observed that the on/off current ratio of poly-Si TFTs was substantially decreased to seriously affect the function of TFTs used as the pixel switch under illumination environment. In addition, the sub-threshold swing is increased under illumination, about 0.49 V/decade, as the initial value in dark is 0.28 V/decade. The variation of sub-threshold swing is about 75%. Since the light from back-light is mainly absorbed at the interface of poly-Si and the glass substrate, plenty of light-induced electron-hole pairs are accumulated in the bottom of poly-Si film to generate the I_{PLC} [2.9].

To solve this issue, the poly-Si TFT with full metal shielding structure was proposed. The I_D-V_G transfer curves of proposed poly-Si TFT under the dark and photo states are shown in Fig. 2.4. It is clearly observed that the I_{PLC} is entirely eliminated in the proposed poly-Si TFT and the shielding effect is independent of drain bias. The leakage current is about 10^{-13} A under illumination at the linear operation, as same as that in the dark state. The sub-threshold slope is also unchanged absolutely under illumination by the light-shielding structure. Figure 2.5(a) plots the I_D-V_G curves of the poly-Si TFT with increasing drain bias under dark. As the drain

voltages are -4.5V and -9V, the negative shifts of V_{TH} are 1.08V and 2.07V, respectively. It indicates that the proposed TFTs are easier to be turned on by the high drain voltage. However, the V_{TH} of conventional poly-Si TFT slightly shifts under high drain voltage operation at dark and photo states. In addition, from the result shown in Fig. 2.5(b), the un-saturation phenomenon of I_D-V_D of poly-Si TFT with full metal shielding layer is found clearly. The V_{TH} of proposed TFT is dependent of drain voltage so that the drain current would increase with drain bias.

Since the metal film is located under the poly-Si active layer, a parasitic capacitance in the overlap of source and drain side is generated. The negative voltage at drain side would lead to a negative potential distribution, V_M, in the metal film owing to the coupling effect. V_M is regarded as the substrate bias to affect the threshold voltage of the proposed poly-Si TFTs [2.10]. Therefore, the threshold voltage shifts in positive are explained by the negative V_M coupled from the applied drain bias. In practical application of TFT-LCD, the range of gate voltage applied to pixel switch is from -10V to 6 V for p-channel device and the input range of data signal is from 0V to 5V. It means that the TFT used as pixel switch is operated at the linear region. Considering the advantages of proposed TFT such as high on/off ratio and unchanged sub-threshold swing due to the elimination of I_{PLC} under illumination, the slight shift of threshold voltage is acceptable. However, poly-Si TFT is taken not only as switch device in pixel but also component for integration of peripheral driving circuits. The shift in V_{TH} with drain voltage is a rather serious issue for circuits design. Therefore, the partial metal shielding structure for poly-Si TFT is proposed and discussed in the next section.

2.3 Partial Metal Shielding Layer Structure

2.3.1 Experimental Procedure

The n-channel poly-Si TFTs with LDD structure were fabricated on Corning1737 glass substrate. First of all, a 50nm thick molybdenum film was sputtered and was patterned using additional mask to be a shielding layer on the glass substrate. The buffer layer and a thin 50 nm-thick undoped a-Si film were sequentially deposited by PECVD at 380℃, followed by dehydrogenated via furnace annealing process at 450 ℃. Then the a-Si films were crystallized by 308nm XeCl excimer laser with the line-shaped beam power of 350mJ/cm^2. The 100nm thickness gate insulator was deposited by TEOS oxide. The source/drain regions were defined by a mask and formed by the mass-separated ion implanter technique. Then, MoW was sputtered and patterned as a gate metal. Following, implantation for LDD region is preformed on overall device after the S/D photo resistor is removed. The doping activation was performed by RTA irradiation. The dimensions of TFTs in this work were L = 18 μm, W = 18 μm and the LDD length is 1.25 μm.

2.3.2 Results and Discussion

The partial metal shielding layer is located junction in and channel region as shown in Fig. 2.6(a) and 2.6(b), respectively. As the shielding metal is located in the channel and shorter than the gate metal shown in Fig. 2.6(b), the space between the edge of shielding metal and the gate metal is set to 3μm. Figure 2.6(a) plots the poly-Si TFT with shielding metal remained to be located in junction side. Similarly, the overlap region between the edge of shielding metal and the gate metal is 3μm. Therefore, the

effect of location for I_{PLC} is investigated employing the two types of poly-Si TFT with different partial metal shielding structure.

Figure 2.7 plots the I_D-V_G relationships of poly-Si TFT with partial metal shielding layer located in channel region (Channel-shielding TFT) and drain junction region (Drain-shielding TFT) as drain voltage is varied at dark state. It is clearly found that the V_{TH} of poly-Si TFT with partial metal shielding layer is independent of drain bias and the location of shielding metal. As shielding metal is located in junction region, the parasitic capacitance is performed in the overlap region between drain side and shielding metal. However, the floating potential, V_M, induced by drain voltage is distributed in the shielding metal region located only in drain side. The channel region would not be affected by V_M to induce the back channel in the bottom of poly-Si layer. Therefore, V_{TH} of Drain-shielding TFT is unchanged with increasing drain bias. By contrast, the shielding metal is completely located inside the coverage of gate metal so that the parasitic capacitance originated from overlap region between shielding metal and drain side is vanished. Therefore, the increasing drain voltage of Channel-shielding TFT could not induce V_M to attribute to the shift of V_{TH}.

Figure 2.8(a) reveals the comparison of I_{PLC} which is extracted at a voltage $|V_G-V_{TH}|$ of 7V as V_D is 0.1V for TFT with partial metal shielding layer located in channel region (Channel-shielding TFT), drain side (Drain-shielding TFT) and source side (Source-shielding TFT) as brightness of back-light is in Channel creased (2160, 3100, 4110, 5620 nits). The I_{PLC} of Drain-shielding TFT is much lower than that of Channel-shielding TFT and Source-shielding TFT. The maximum values of I_{PLC} of Drain-shielding TFT, Channel-shielding TFT and Source-shielding TFT are 4.1, 19.2 and 24.5 pA. In addition, the I_{PLC} of Drain-shielding TFT exhibits a weak dependence on the increasing brightness of back-light. The result confirms that drain side is the

dominant region for I_{PLC} of poly-Si TFT operated in linear region. Figure 2.8(b) shows the I_{PLC} of Drain-shielding TFT, Channel-shielding TFT and Source-shielding TFT as drain voltage is 9V. It is observed the shielding effect of Drain-shielding TFT is reduced markedly even if the I_{PLC} of Drain-shielding TFT is still less than that of Channel-shielding TFT and Source-shielding TFT.

While poly-Si TFT is exposure to back-light, the excess electron-hole pairs are generated. The regions generating photo-induced electron-hole pairs can be divided into two parts. One is drain junction region and another is channel region. The excess electron-hole pairs generated in drain junction would be separated due to the electric field and the excess electrons could flow to drain to become leakage current. By contrast, since Si is an indirect band gap material, photo-induced electron-hole pairs in channel region could not be recombined directly. Therefore, the excess electrons in channel region would diffuse to drain to form current. It is inferred that the I_{PLC} is attributed to the diffusion current and drift current from channel region and drain junction, respectively. As shown in Fig. 2.9, the band diagram to explain the generation of I_{PLC} for Source-shielding TFT is proposed. Since the shielding metal is located in source side, the excess electrons generated at channel and junction region flow to drain by diffusion and drift, leading to the high I_{PLC}. Figure 2.10 shows the band diagram of Drain-shielding TFT under illumination. As the shielding metal is located in drain side, light emitting to the junction region is blocked to eliminate the junction part of I_{PLC}. In addition, the electrons induced by light outside the shielding metal are difficult to diffuse to drain since the excess electrons must to pass through an intrinsic poly-Si region, while drain voltage is 0.1V. Hence, Drain-shielding TFT operated in linear region exhibits a highest immunity to illumination environment compared to Source-shielding TFT and Channel-shielding TFT. However, as the high

voltage is applied at drain, a positive potential distribution, V_M, in the shielding metal of Drain-shielding TFT owing to the coupling effect is generated due to the parasitic capacitance in the overlap of drain and shielding metal. Hence, electrons induced by V_M gather to form the back channel near drain in the bottom of poly-Si layer, as illustrated in Fig. 2.11. So that excess electrons at channel region would flow to drain through the back channel under high drain bias, generating I_{PLC}. Therefore, the shielding effect of Drain-shielding TFT under illumination would be suppressed by applied high drain voltage.

2.4 Conclusions

We have demonstrated a new and simple method to fabricate the top gate poly-Si TFT with the light-shielding structure first. The proposed full metal shielding TFT is free of photo leakage current under illumination for high image quality AMLCD application. The process of the proposed structure without adding the number of masks is compatible with the conventional poly-Si TFTs. In addition, the shift in threshold voltage of the proposed TFTs with the increasing drain bias in dark state is explained by the coupling effect. In order to overcome this issue and investigate the generation mechanism of I_{PLC}, poly-Si TFT with the partial shielding metal located in junction and channel region is fabricated. It is shown that V_{TH} of poly-Si TFT with partial metal shielding layer is independent of increasing drain bias. Furthermore, the Drain-shielding TFT exhibits impressively low I_{PLC} and the shielding effect of the Source-shielding TFT and Channel-shielding TFT are rather poor. The I_{PLC} of Drain-shielding TFT, Channel-shielding TFT and Source-shielding TFT are 4.1, 19.2 and 24.5 pA as brightness of back-light is 5610 nits. From the comparison of I_{PLC} of

Drain-shielding TFT, Source-shielding TFT and Channel-shielding TFT, the band diagram of poly-Si TFT under illumination is proposed. In addition, the shielding effect of Drain-shielding TFT would be suppressed as the high drain voltage.

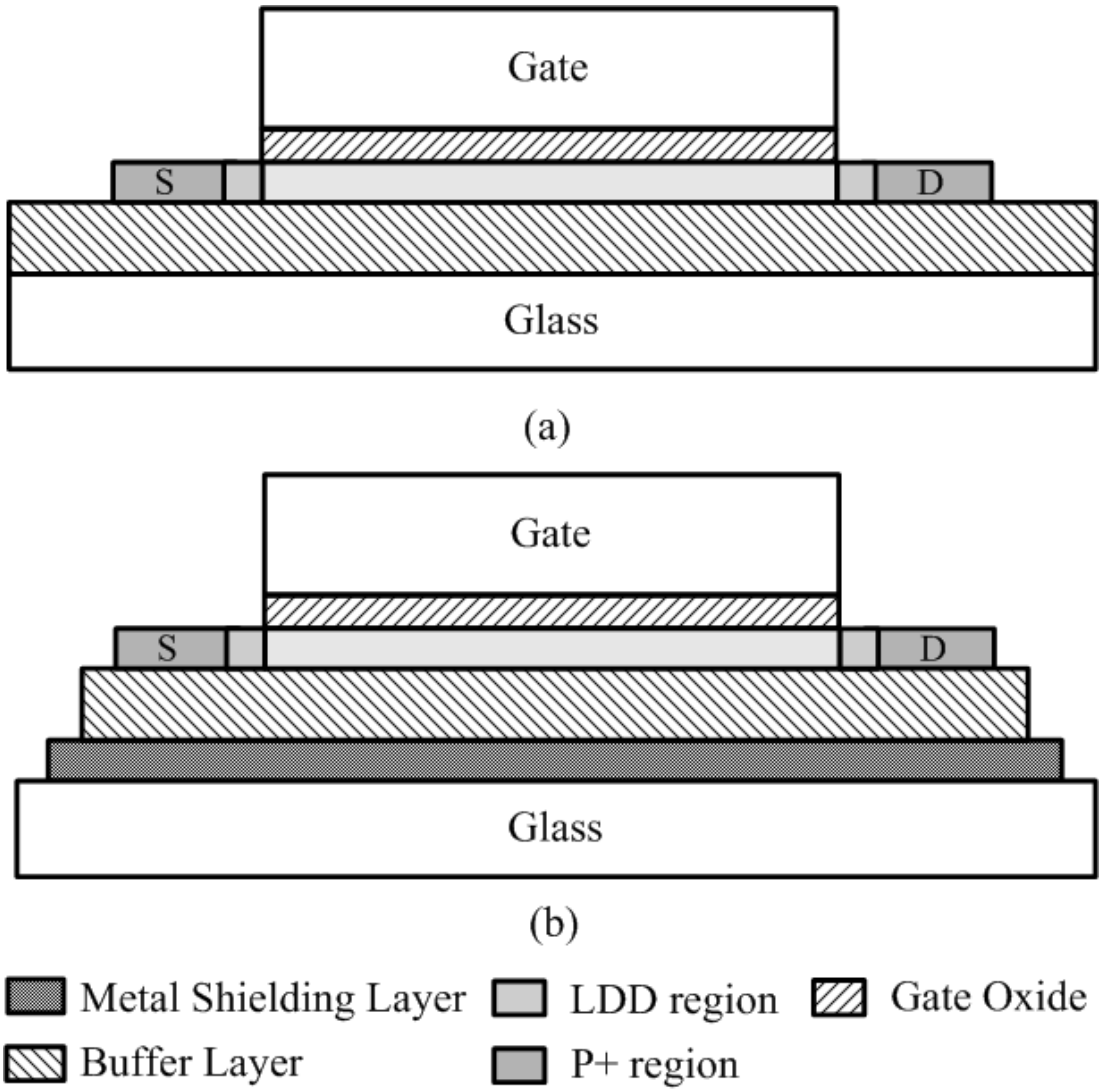


Fig. 2-1 (a) Conventional top gate structure of poly-Si TFT. (b) The new structure of proposed Poly-Si TFT. A metal film is located under the active island to be a light-shielding layer.

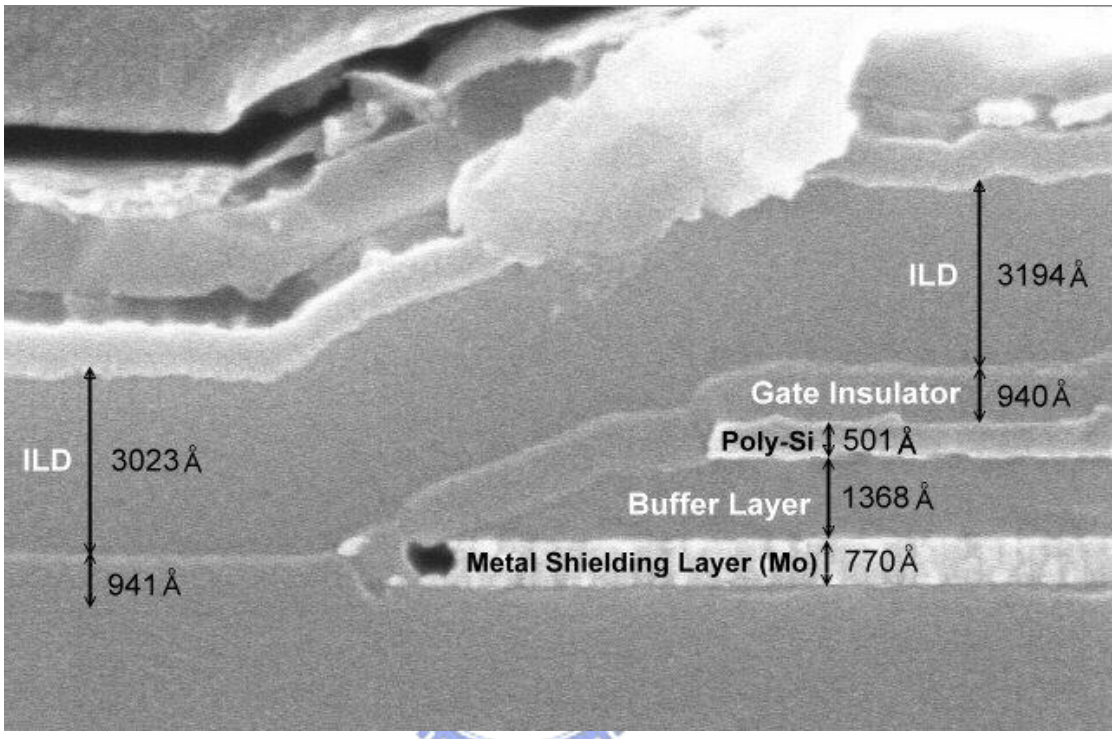


Fig. 2-2 The SEM image of metal shielding layer, buffer layer and Poly-Si layer after etching process using the same mask.

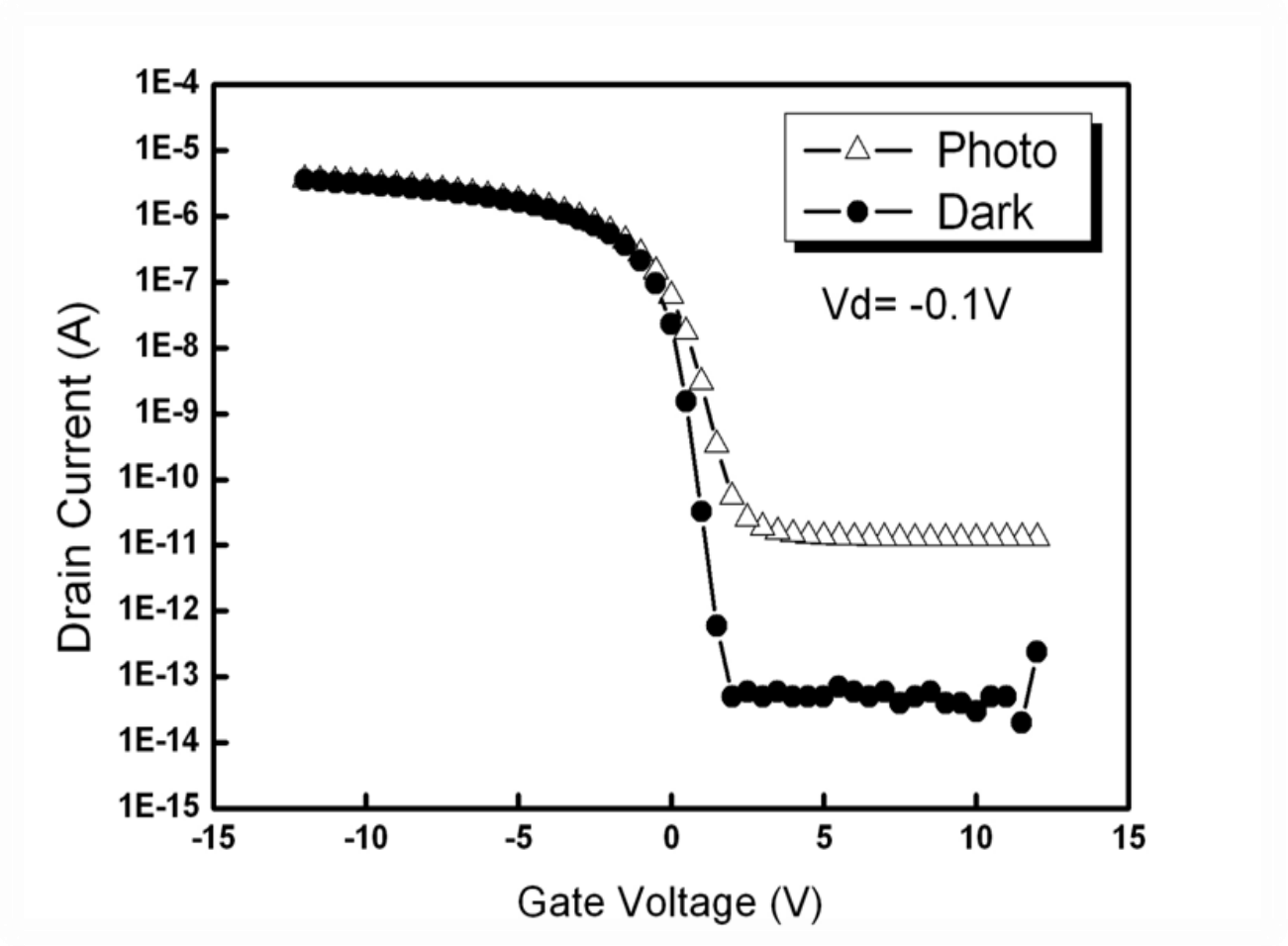


Fig. 2-3 I_D-V_G curves of the conventional poly-Si TFT operated in the linear region under illumination and dark states. A significantly increase of leakage current was found.

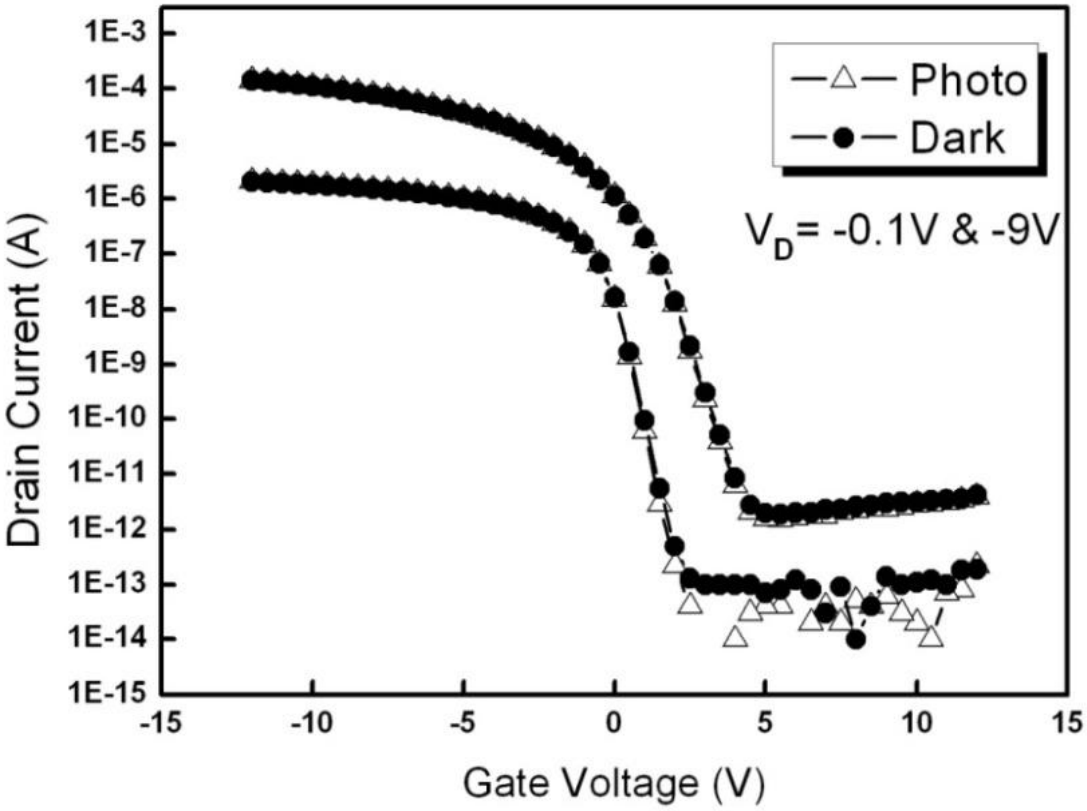
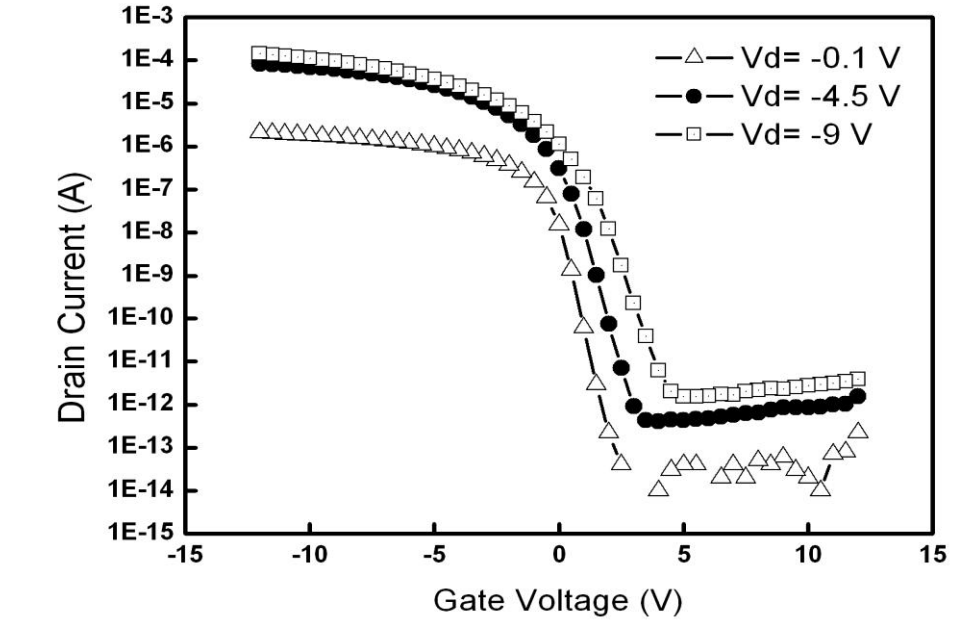
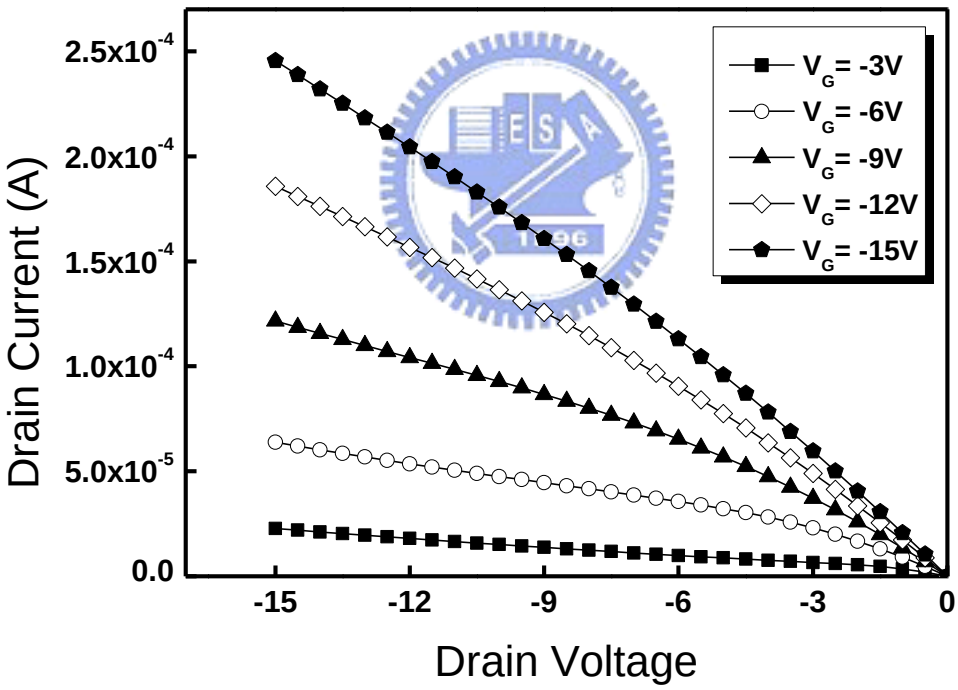


Fig. 2-4 I_D-V_G curves of proposed Poly-Si TFT under illumination and dark states. The photo leakage current and the variation of sub-threshold swing under illumination are eliminated entirely.

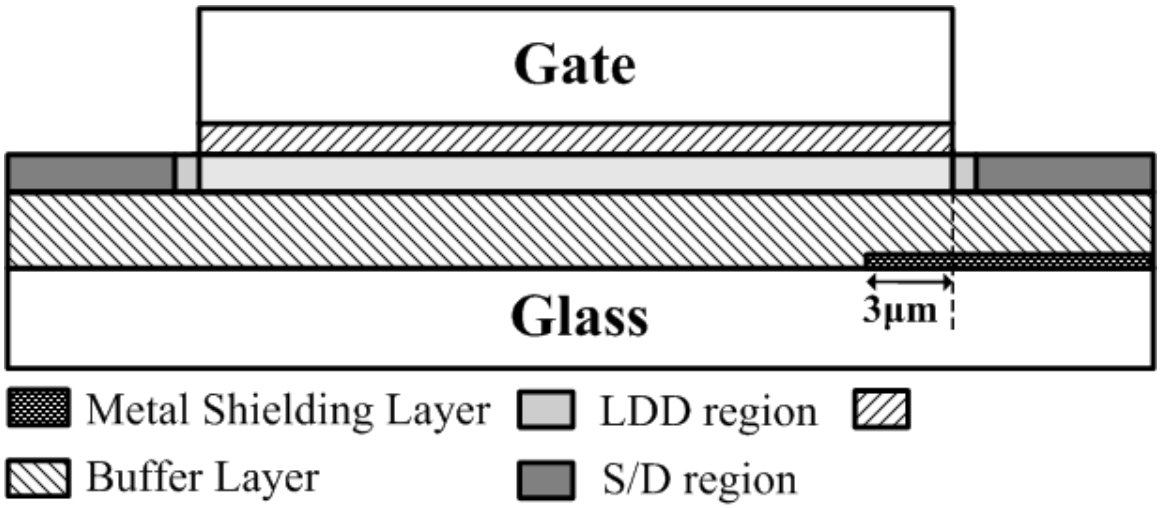


(a)

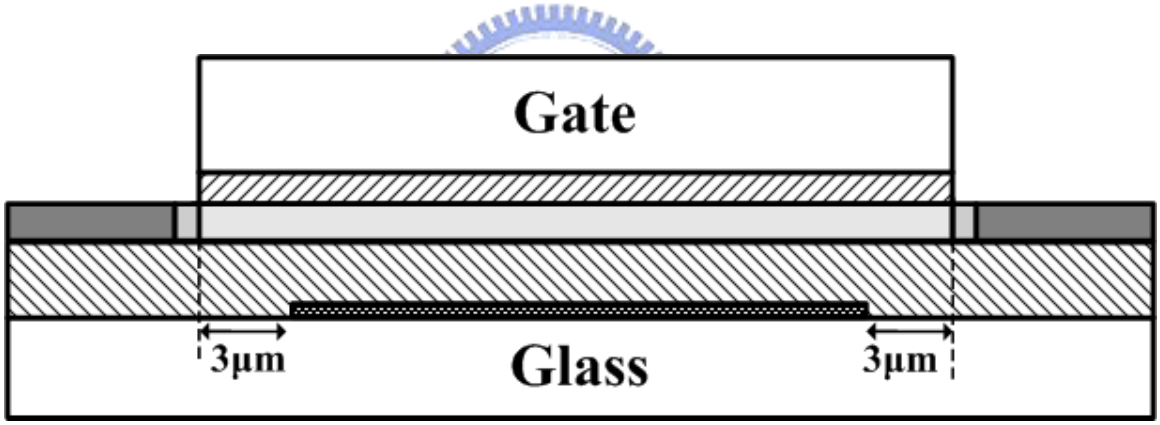


(b)

Fig. 2-5 (a) I_D-V_G curves of proposed Poly-Si TFT as V_D is set as -0.1, -4.5 and -9V. It is found that the threshold voltage shifts with the increasing drain voltage. (b) I_D-V_D curves of Poly-Si TFT with full metal shielding layer as V_G is varied. It shows that the drain current is strongly dependent of the applied drain voltage.



(**a**)



(b)

Fig. 2-6 (a) Proposed Poly-Si TFT with partial metal shielding layer which is located in the junction region. (b) Proposed Poly-Si TFT with partial metal shielding layer which is located in the central channel region.

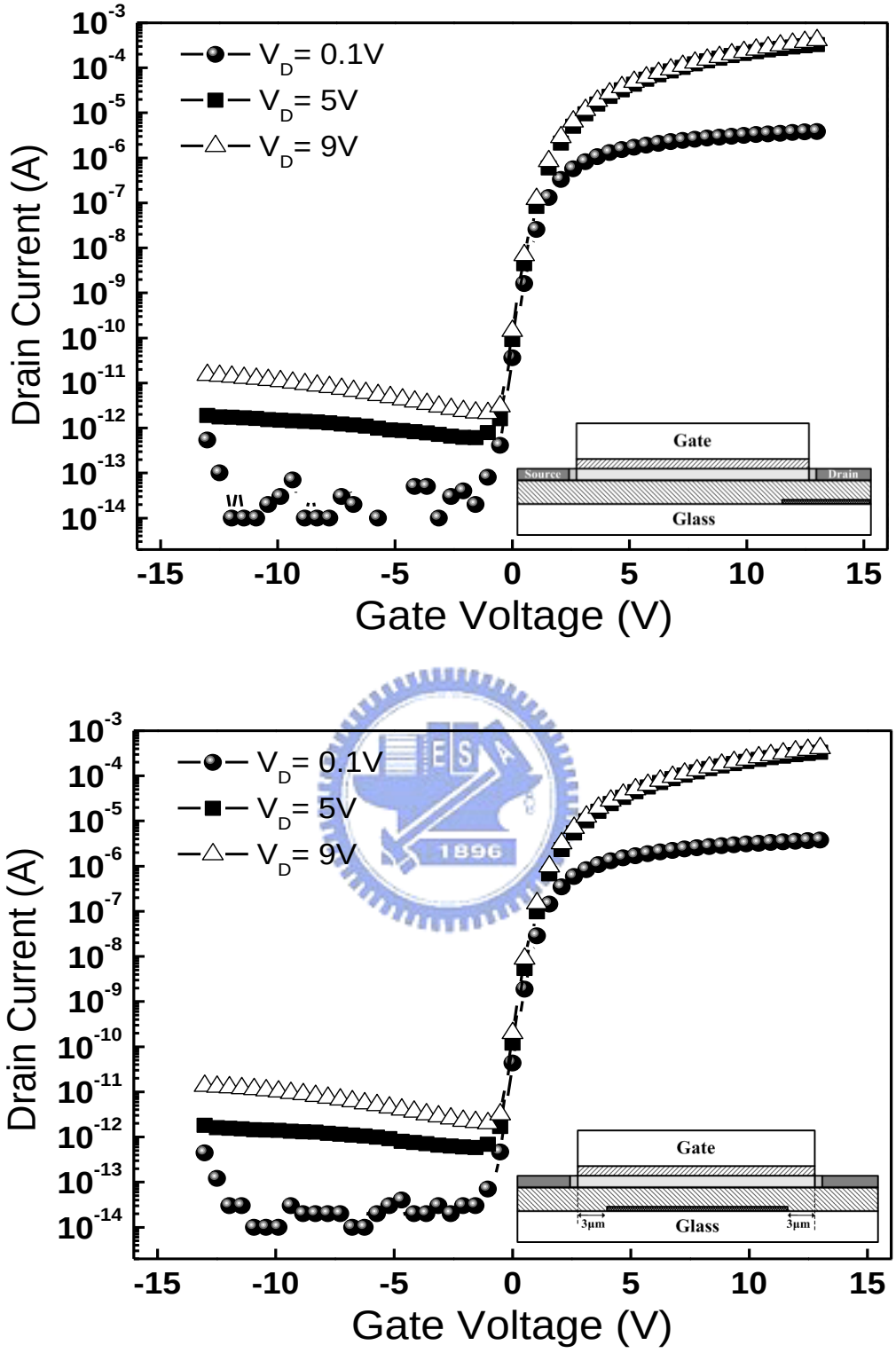
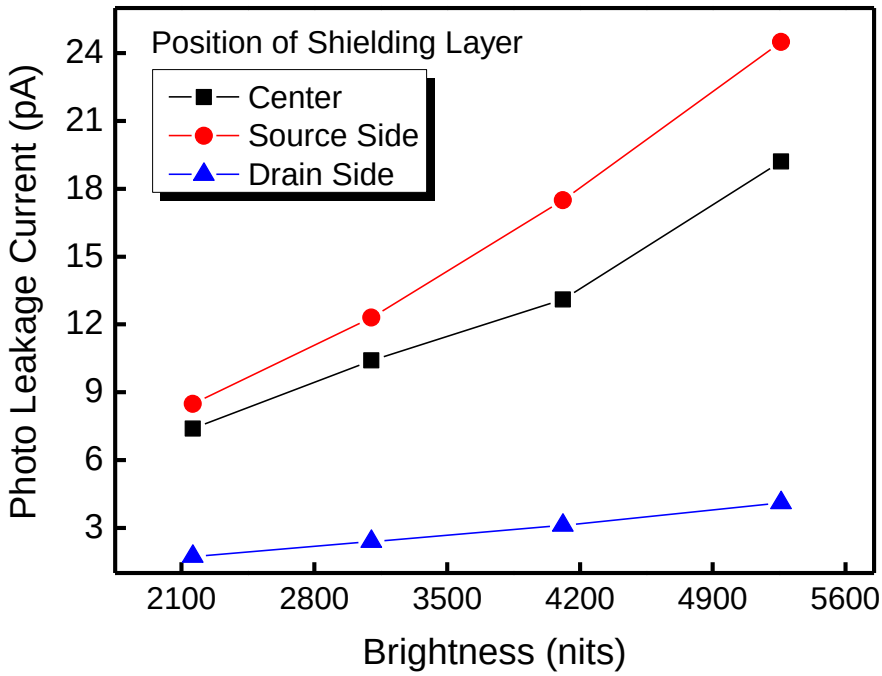
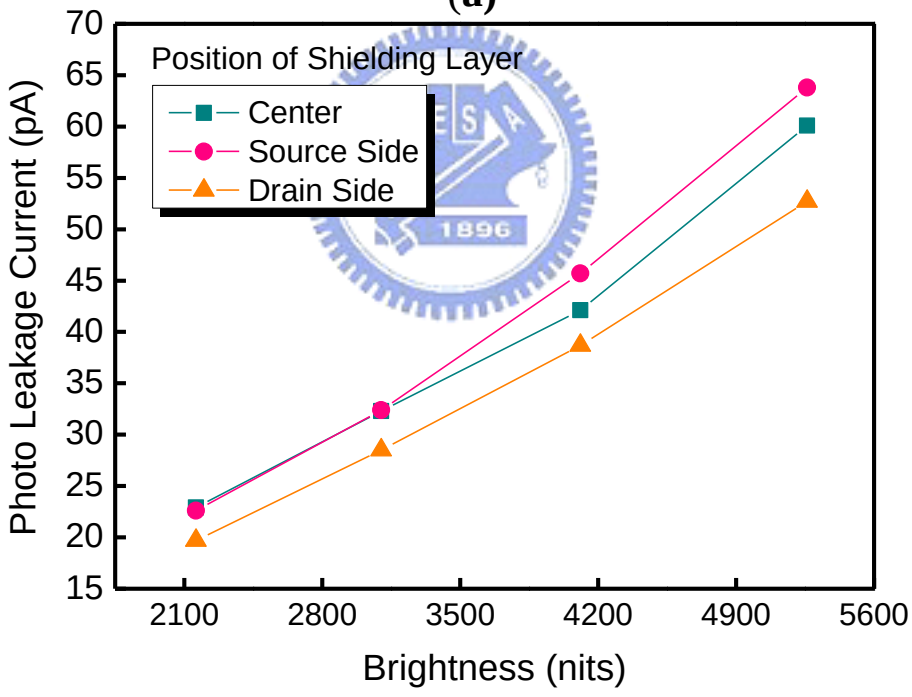


Fig. 2-7 the transfer curves of poly-Si TFT with partial metal shielding layer located in channel region (Channel-shielding TFT) and drain junction region (Drain-shielding TFT) as drain voltage is varied at dark state.



(a)



(b)

Fig. 2-8(a) Photo leakage current of poly-Si TFT with partial metal shielding layer located in varied regions as increasing brightness and V_D is 0.1V. (b) Photo leakage current of poly-Si TFT operated in saturation region with partial metal shielding layer located in varied regions as increasing brightness.

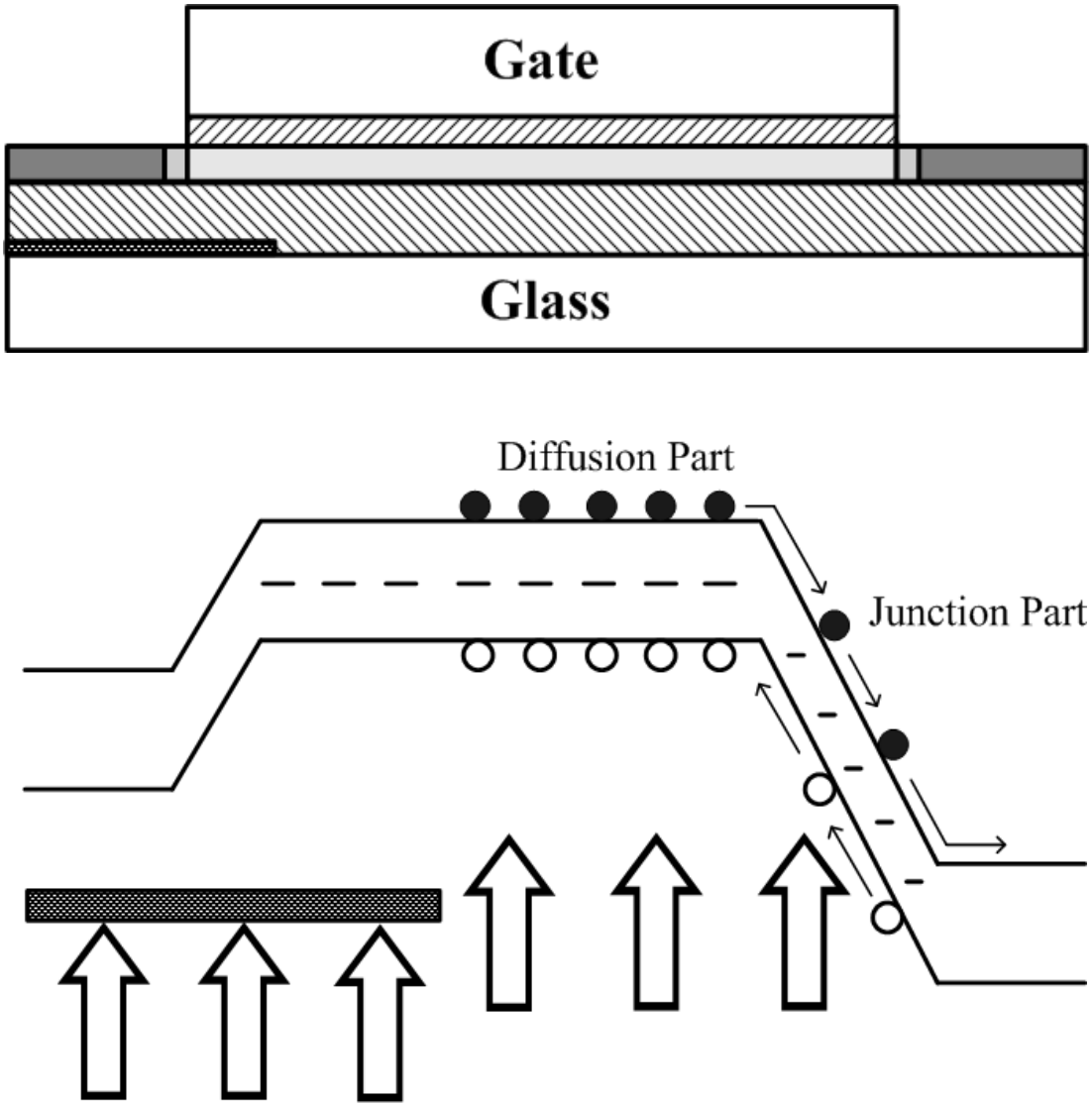


Fig. 2-9 Band diagram for generation of photo leakage current of poly-Si TFT with partial metal shielding layer located in source side.

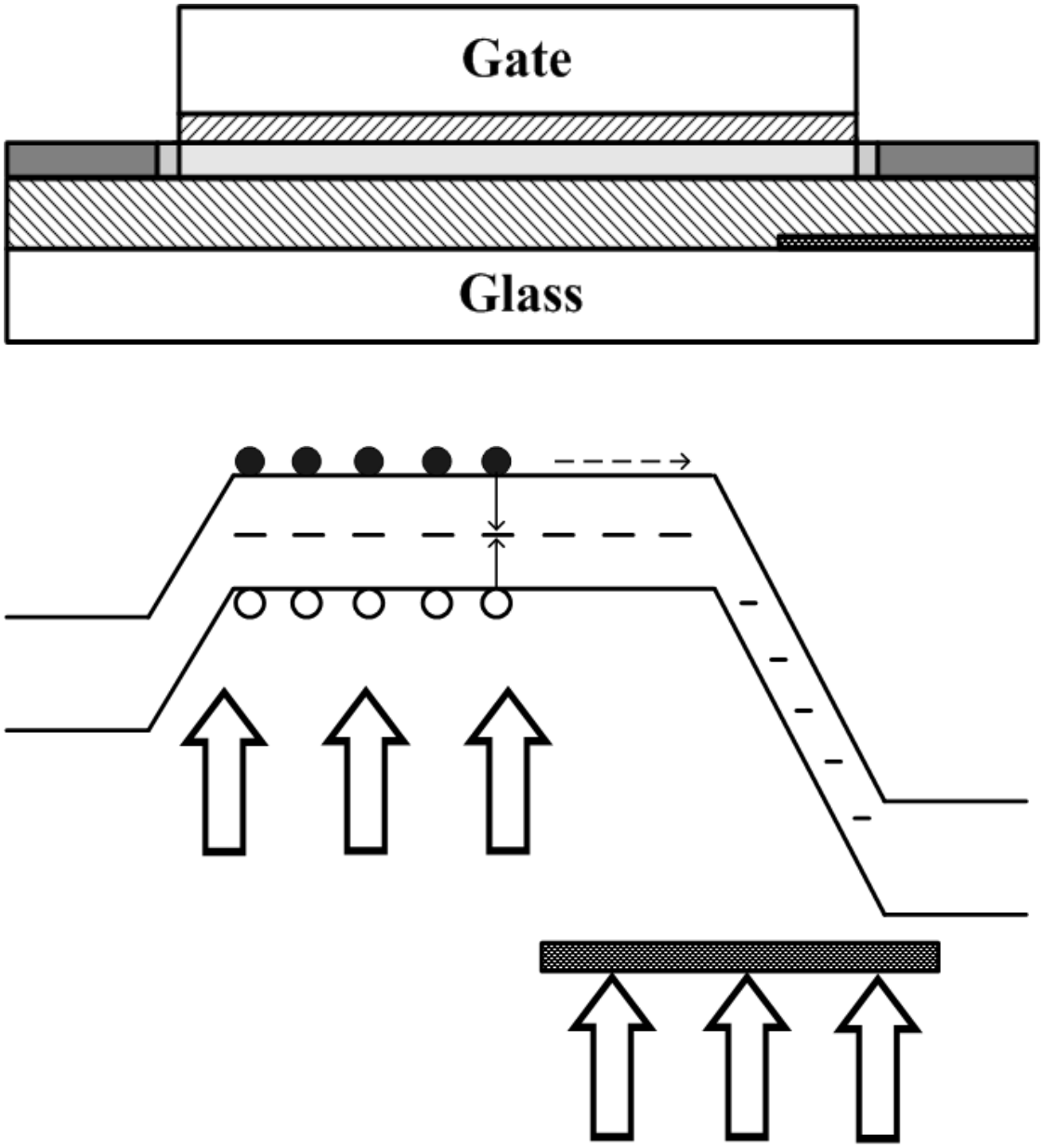


Fig. 2-10 Band diagram for poly-Si TFT with partial metal shielding layer located in drain side under illumination.

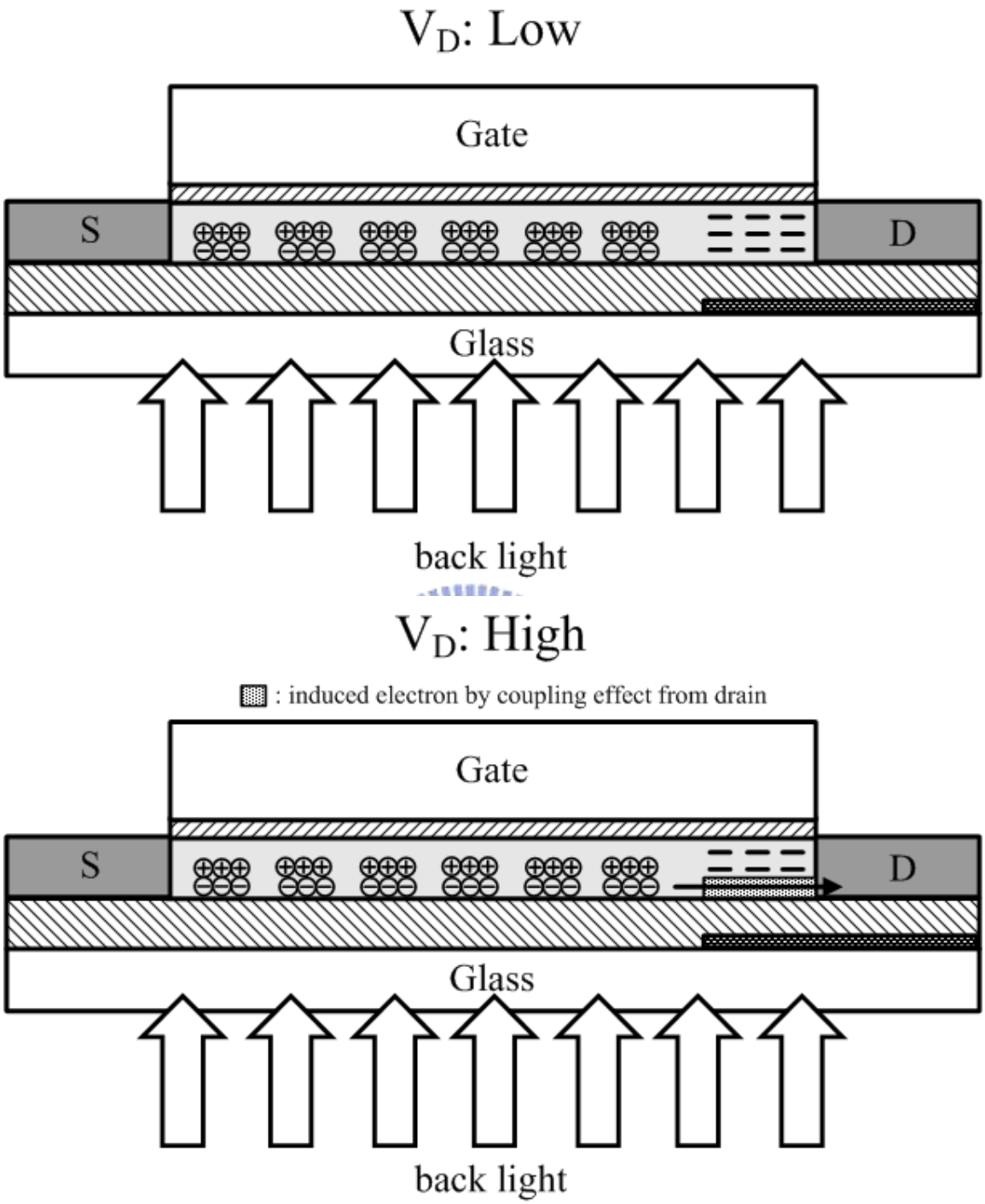


Fig. 2-11 Proposed model to explain that the shielding effect would be suppressed under high drain bias.

Chapter 3

Improvement of Electrical Characteristics of Poly-Si TFT under Illumination Using Modified Buffer Layer

3.1 Introduction

Polycrystalline silicon thin film transistors (poly-Si TFTs) have been widely used in active matrix liquid crystal displays (AMLCDs) and active matrix organic light-emitting diode display (AMOLED) [3.1-3.4]. The poly-Si TFTs offer great potential for AMDs technology, due to their superior electrical characteristics over those of hydrogenated amorphous Si thin film transistors (a-Si:H TFTs). Recently, the demand of high-end mobile electronic products such as digital camera, cell phone, and mobile TV is continuing to grow up, so that the high resolution and high image quality becomes the critical issues in the development of mobile displays. Therefore, the brightness of back-light is getting higher and higher to meet the requirement for fine image quality and superior readability as people use these mobile electronic products under sunlight outdoor [3.5-3.6]. However, the poly-Si TFTs usually suffer from undesirable photo leakage current (I_{PLC}) under a high illumination environment [3.7-3.10]. The high leakage current and increased sub-threshold swing (S.S) of poly-Si TFT under illumination in AMLCD displays should be reduced to avoid losing the charges stored in pixels. Therefore, the voltages that are held across the pixel electrodes would be diminished to affect the gray level controlling, which in turn, would cause a low contrast ratio and error color display. However, the researches about improving the electrical characteristics in poly-Si TFTs under illumination are

very few and the mechanism of photo leakage current in poly-Si TFT is still not clarified.

In our previous studies, we propose a full metal shielding structure for poly-Si TFT to eliminate entirely the I_{PLC} and the degradation of S.S without adding the number of masks. The measurement result confirms that poly-Si TFT with full metal shielding layer is free of I_{PLC} and the degraded S.S in photo state. However, the threshold voltage of poly-Si TFT with full metal shielding layer would shift with increasing drain bias. Although the shift of V_{TH} is acceptable for pixel switching element, it is still a critical issue for application of integrating peripheral driving circuits. Hence, the partial metal shielding layer with different location in poly-Si TFT is used to solve the shift of V_{TH}. From our experimental data, the issue of V_{TH} varied with drain voltage is release by partial metal shielding layer, compared to full metal shielding structure. As partial metal shielding layer is located in drain side, the I_{PLC} is significantly reduced but not vanished totally. However, the number of masks for poly-Si TFT with partial metal shielding layer is increased to pattern additionally the shielding metal layer. It means that the manufacturing cost is raised for poly-Si TFT with partial metal shielding layer. In addition, the process of partial shielding TFT is difficult to align the metal shielding layer.

In this chapter, we proposed two simple methods to improve electrical characteristics of poly-Si TFT under illumination with original parameters measured in dark state. First, a Si-rich buffer layer is used to absorb the back light. Since Si-rich dielectric layer exhibits high absorption coefficient, using Si-rich dielectric material as buffer layer would reduce the light intensity emitted into poly-Si layer to improve the electrical characteristic of TFT under illumination without change the number of masks. In addition, without complicated device structure or process steps, another

method to reduce the I_{PLC} of poly-TFTs has been developed. The surface of conventional buffer layer in the proposed poly-Si TFT is treated employing the NH_3 plasma, to lower the photo leakage current and improve the S.S characteristics under back-light illumination with the original characteristics of poly-Si TFTs.

3.2 Photo Characteristics in Poly-Si TFT with Si-rich Buffer layer

3.2.1 Experimental Procedure

In this work, the proposed method to fabricate poly-Si TFT would not add extra thin film deposited or photo process. The p-channel poly-Si TFTs with lightly doped drain (LDD) structure were fabricated on Corning1737 glass substrate. The silicon-rich (Si-rich) oxide film and the Si-rich SiN_X film are used to replace the conventional buffer layer for poly-Si TFTs. Figure 3.1 shows the split conditions for buffer layer replaced by Si-rich oxide film or Si-rich SiN_X film. Since the light transmittance of Si-rich dielectric film is rather low, it is essential to etch back the transparent area of array pixel for display. The following is the detail procedure. A 50 nm-thick undoped amorphous-Si (a-Si) film were deposited by plasma enhanced chemical vapor deposition (PECVD) at 380℃, followed by dehydrogenated via furnace annealing process at 450℃. Then the a-Si films were crystallized by 308nm XeCl excimer laser with the line-shaped beam power of 350mJ/cm^2. The active island was patterned by plasma dry etching. The 100nm thickness gate insulator was deposited by tetraethyl orthosilicate base (TEOS) oxide. The source/drain regions were defined by a mask and formed by the mass-separated ion implanter technique. Then, MoW was sputtered and patterned as a gate metal. Following, implantation for LDD region is preformed on overall device after the S/D photoresistor is removed. The doping activation was performed by RTA irradiation. The LDD length of TFTs in

this work was 1.25 μm. The brightness of back-light for photo state measurement is set as 3000nits. In the manufacture process, the number of masks is equal to the conventional poly-Si TFT procedure.

3.2.2 Results and Discussion

Figure 3.2 shows the transmittance of conventional buffer layer with varied wavelength. As wavelength is in visual light range of human (400nm-700nm), all of transmittance is over 89% to meet the requirement of high efficiency for back-light. However, the transmittance of Si-rich SiN_X film with 300nm thickness is reduced significantly as wavelength is varied from 400nm to 650nm as shown in Fig. 3.3, including most of visual light range of human. It is inferred that the light emitted from back-light Figure is almost totally absorbed by the Si-rich SiN_X buffer layer. Figure 3.4 plots the transmittance of Si-rich SiN_X film as the thickness is 100nm, 200nm and 300nm. As wavelength is 500nm, the transmittance of Si-rich SiN_X with 100nm thickness is about 80%, but the drop of transmittance in 300nm thickness Si-rich SiN_X is 45%. It confirms that the transmittance of Si-rich dielectric film is strongly dependent of its thickness. The thicker Si-rich dielectric film can provide the higher light absorption capacity. However, the Si-rich SiN_X film with 200nm and 300nm thickness exhibits a abnormally high transmittance for the range of long wavelength. It may be attributed to the reflection property in the long range of wavelength. Figure 3.5(a) and 3.5(b) show the photo leakage current (I_{PLC}) results of poly-Si TFT with Si-rich buffer layer for linear and saturation region, respectively. The I_{PLC} normalized with channel width (W) is extracted from 3 TFTs as V_G is 7.5V. It is obvious that I_{PLC} of poly-TFT with Si-rich SiN_X buffer layer is significantly reduced.

The average of I_{PLC} of TFT with Si-rich SiN_X buffer is lowered 38% of the magnitude of that of the conventional ones. Furthermore, the average I_{PLC} is decreased 60% by using Si-rich oxide buffer film, compared to that in the conventional TFT. Since the thickness of Si-rich oxide buffer layer is thicker than Si-rich SiN_X, the transmittance of the Si-rich oxide film structure must be much lower than that of the conventional buffer film especially in the 400nm to 650nm wavelength. Therefore, the I_{PLC} of poly-Si TFT with Si-rich oxide buffer layer under illumination is lowest. It is important that the major light wavelength absorbed by Si-rich oxide film could is the visual light range of human used as back-light. Therefore, the fewer light is absorbed by the active poly-Si layer, the lower photo leakage current is produced. In addition, the variation of S.S in poly-Si TFT with Si-rich buffer layers is shown in Fig. 3.6, to prove the effect of this proposed method. The variation ratio of sub-threshold swing ΔS.S is defined as ($S.S_{PHOTO}/S.S_{DARK}$-1), where $S.S_{PHOTO}$ and $S.S_{DARK}$ are the sub-threshold swing of poly-Si TFT at drain voltage of -0.1V under photo and dark states. Similarly, poly-Si TFT with Si-rich oxide buffer layer shows a more improved S.S, compared to that with the conventional and Si-rich SiN_X buffer layer. The ΔS.S of TFT with Si-rich oxide buffer layer and TFT with Si-rich oxide buffer layer is 23% and 28.7%, respectively as that of conventional one is 40%.

3.3 Photo Characteristics of Poly-Si TFT with Treated Buffer Layer

3.3.1 Experimental Procedure

Top-gate p-type poly-Si TFTs with LDD were fabricated in this letter. First of all, a 50 nm-thick SiN_X and a 150nm-thick SiO_2 films with conventional recipe were sequentially deposited to form buffer layer by PECVD. Then, the surface of buffer layer was treated employing NH_3 plasma for 10 minute. A thin 50 nm-thick undoped

a-Si film was deposited by PECVD at 380℃, followed by dehydrogenated via furnace annealing process at 450℃. The a-Si films were crystallized by 308nm XeCl excimer laser with the line-shaped beam power of 350mJ/cm^2. The 100nm thickness gate insulator was deposited by TEOS oxide. The source/drain and LDD region were formed by the mass-separated ion implanter technique. The doping activation was performed by RTA. MoW was sputtered as a gate metal. The dimensions of TFTs in this work were channel length (L) 6μm, channel width (W) 6μm and the LDD length 1.25μm.

3.3.2 Results and Discussion

Figure 3.7 shows the I_D-V_G transfer curves of conventional p-channel poly-Si TFT operated in linear region under the dark and photo states. The brightness of back-light for photo state measurement is set as 3100nits. As the gate bias is swept from 12 to 0 V, the leakage current of poly-Si TFTs in the dark state was about 10^{-13} A. With the same range of gate bias, the leakage current of poly-Si TFT under illumination is as high as two orders of magnitude, around 10^{-11}A. In addition, the sub-threshold swing is increased under illumination, about 0.45 V/dec, as the initial value in dark is 0.29 V/dec. The variation of sub-threshold swing is about 55%. The on/off current ratio of poly-Si TFTs was substantially reduced due to the high photo leakage current, so that the function of TFTs used as the pixel switch under illumination would be affected seriously.

Since the light emitted from back-light is mainly absorbed at the interface between the poly-Si layer and the buffer layer, plenty of electron-hole pairs are generated in the bottom of poly-Si film [3.9]. Furthermore, the energy-band structure of Si material is indirect bandgap. The excess electron-hole pairs induced by the absorption of light

would not be recombined from band to band directly due to the momentum conservation principle. The numerous electron-hole pairs are accumulated in the bottom of poly-Si layer. It follows that the excess holes flow to the drain under the negative drain bias for p-channel devices, generating the photo leakage current. To release the issue, the trap states on the surface of the buffer layer were induced by the NH_3 plasma treatment to assist the recombination of excess electron-hole pairs. Figure 3.8 plots the key process flow of proposed poly-Si TFTs. The surface quality in the top SiO_2 film of buffer layer would be degraded to generate the surface trap density employing the NH_3 plasma bombardment. After plasma treatment, the process flow is as same as the standard one.

Figure 3.9 shows the transfer curves of the conventional and proposed TFTs. The electrical characteristics of poly-Si TFTs with NH_3 plasma treatment on the buffer layer are almost entirely identical to the conventional ones. It is verified that the crystallization status of poly-Si would not be affected by the surface states of buffer layer. Therefore, the proposed method can be completely compatible with the conventional poly-Si TFT process. Furthermore, in order to confirm the uniformity of poly-Si TFTs with proposed method, the average of key parameters extracted at linear operation in 12 TFTs with various location of substrate are summarized in the inset table of Fig. 3.9. It is found that the uniformity of proposed poly-Si TFTs kept in a good condition and the key parameters were nearly unchanged in comparison with the conventional devices.

The photo leakage current of the conventional and the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 7V as V_D is 0.1V, with the increasing brightness of back-light (2160, 3100, 4110, 5620 nit) are illustrated in Fig. 3.10. The photo leakage current of conventional poly-Si TFTs increases substantially with increasing

brightness of back-light. In contrast, for proposed device, the leakage current under illumination is slightly increased and remain a weak dependence of the brightness of back-light. The maximum of photo leakage current in the TFT with NH_3 plasma treatment is 8.1 pA. It is still much lower than, 13.6 pA, the minimum of that in conventional TFT. Figure 3.11 shows the comparison of sub-threshold swing in the conventional and proposed TFTs under illumination with increasing brightness. The increasing ratio of sub-threshold swing ΔS.S is defined as ($S.S_{PHOTO}/S.S_{DARK} - 1$), where $S.S_{PHOTO}$ and $S.S_{DARK}$ is the sub-threshold swing of devices at drain voltage of -0.1V under photo and dark states, respectively. As the brightness of back-light is 5610 nit, the maximum ΔS.S of the conventional and proposed TFT are 46.4% and 85.3%, respectively. The significant improvement of variation in sub-threshold swing of poly-Si TFT under illumination is confirmed.

3.4 Conclusions

We have provided two effective ways to improve the electrical characteristics of poly-Si TFT under illumination without adding the number of masks or requiring complicated device structure. The first one is to use Si-rich dielectric films as the buffer layer. Since Si-rich dielectric layers owns high absorption coefficient, they can reduce the intensity of light emitting into poly-Si layer from back to suppress the photo-induced electron-hole pairs. The photo leakage current and the degradation of S.S in poly-Si TFT with Si-rich oxide or SiN_X buffer layers are markedly lower than those in conventional ones. Because the thickness of Si-rich oxide buffer layer is 200 nm, thicker than that of Si-rich SiN_X buffer layer, the suppression effect of photo leakage is highest for TFT with Si-rich oxide buffer. The average of I_{PLC} in TFT with Si-rich oxide buffer layer and TFT with Si-rich SiN_X buffer layer is lowered 38% and

60% of the magnitude of that of the conventional ones, respectively. Then, we have demonstrated another simple method to fabricate the poly-Si TFT with low photo leakage current without changing the structure or process flow. The proposed poly-Si TFT exhibits the impressively low leakage current and improved sub-threshold swing under illumination. The uniformity and electrical characteristics of proposed devices are almost same as the conventional ones. As the brightness of back-light is set to 5610 nit, the photo leakage and the variation of sub-threshold swing in proposed TFT are 8.1 pA and 46.3 %, respectively while those in conventional TFT are 35.6 pA and 85.3%.

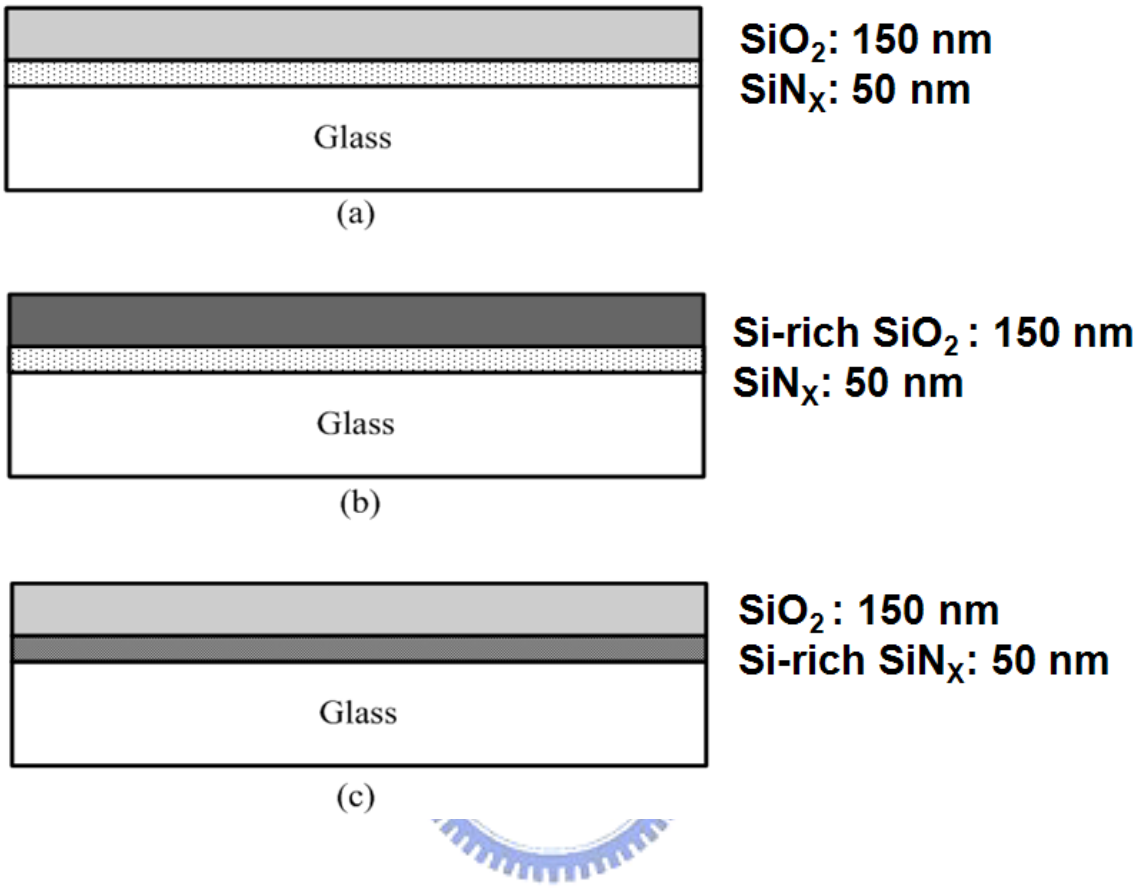


Fig. 3-1 (a) Conventional buffer layer structure. (b) Si-rich oxide buffer layer: the conventional oxide layer is replaced by Si-rich oxide film. (c) Si-rich SiNX buffer layer: the conventional SiN_X layer is replaced by Si-rich SiN_X film

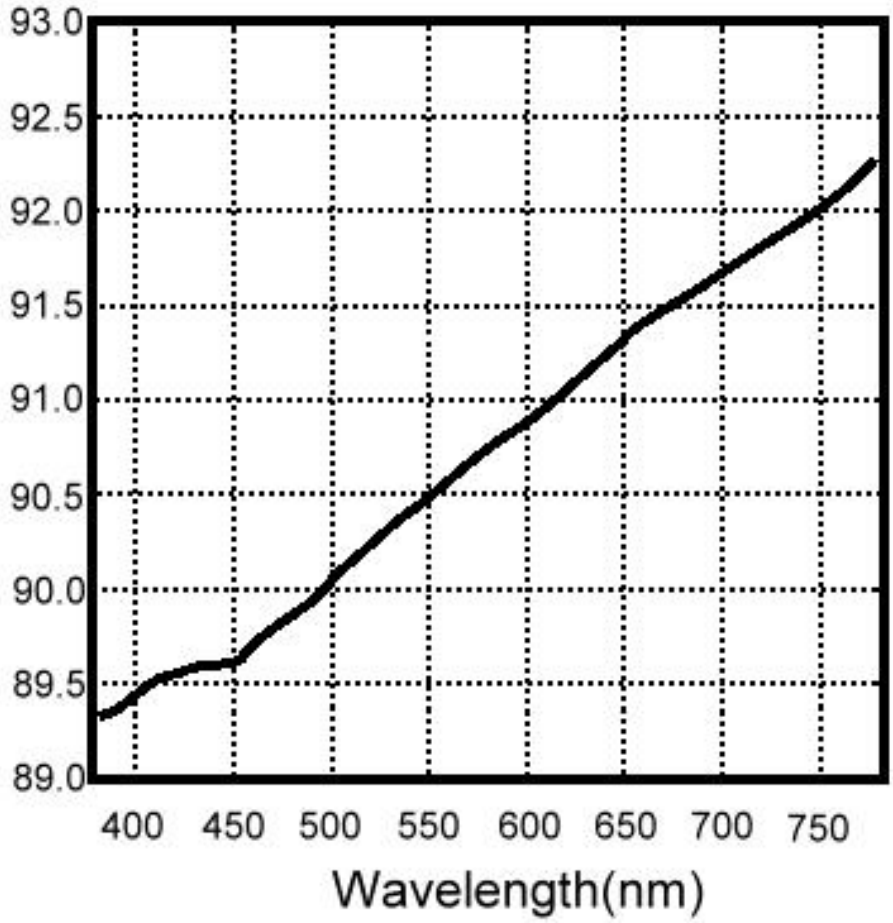


Fig. 3-2 The transmittance of conventional buffer layer within visual light range of human.

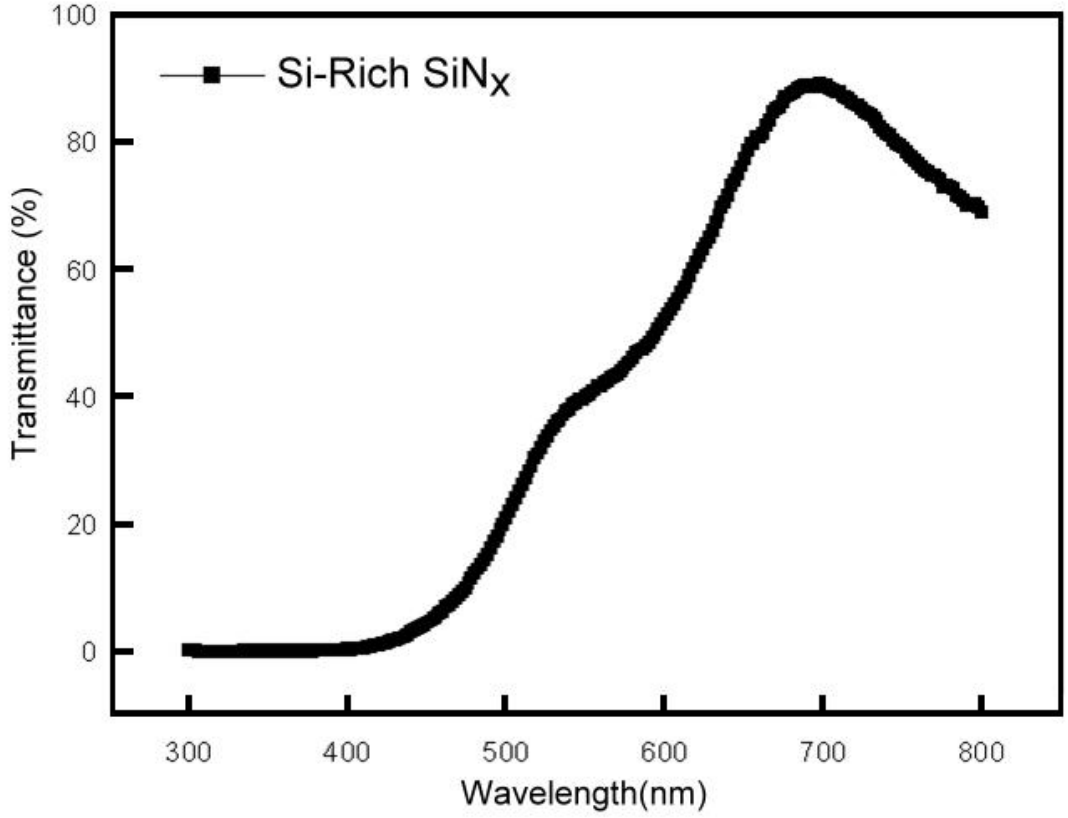


Fig. 3-3 The transmittance of Si-rich SiN_X buffer layer as the wavelength sis varied from 300nm to 800nm.

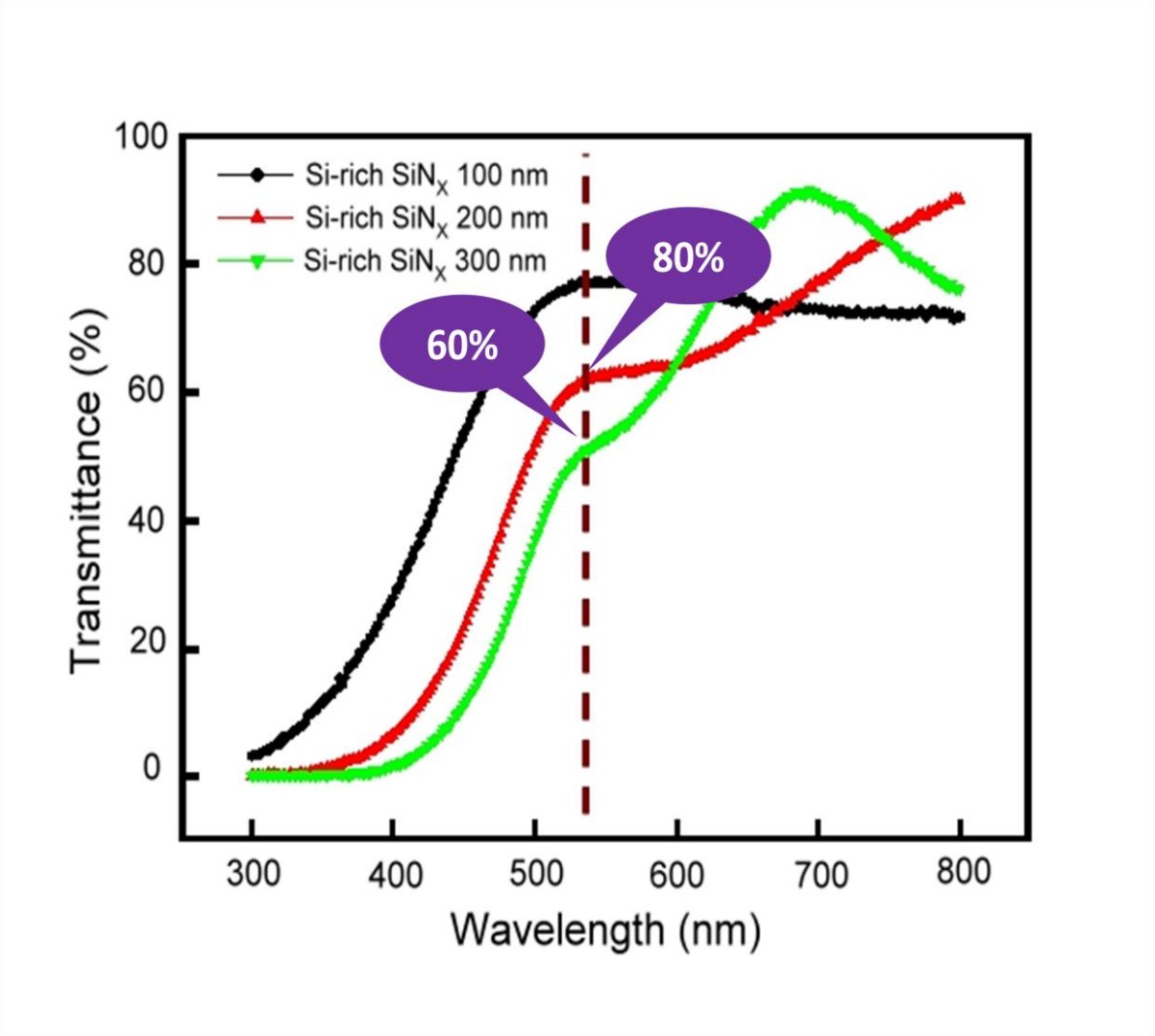


Fig. 3-4 The comparison in transmittance of Si-rich SiN_X buffer layer as the film thickness is 100nm, 200nm and 300nm

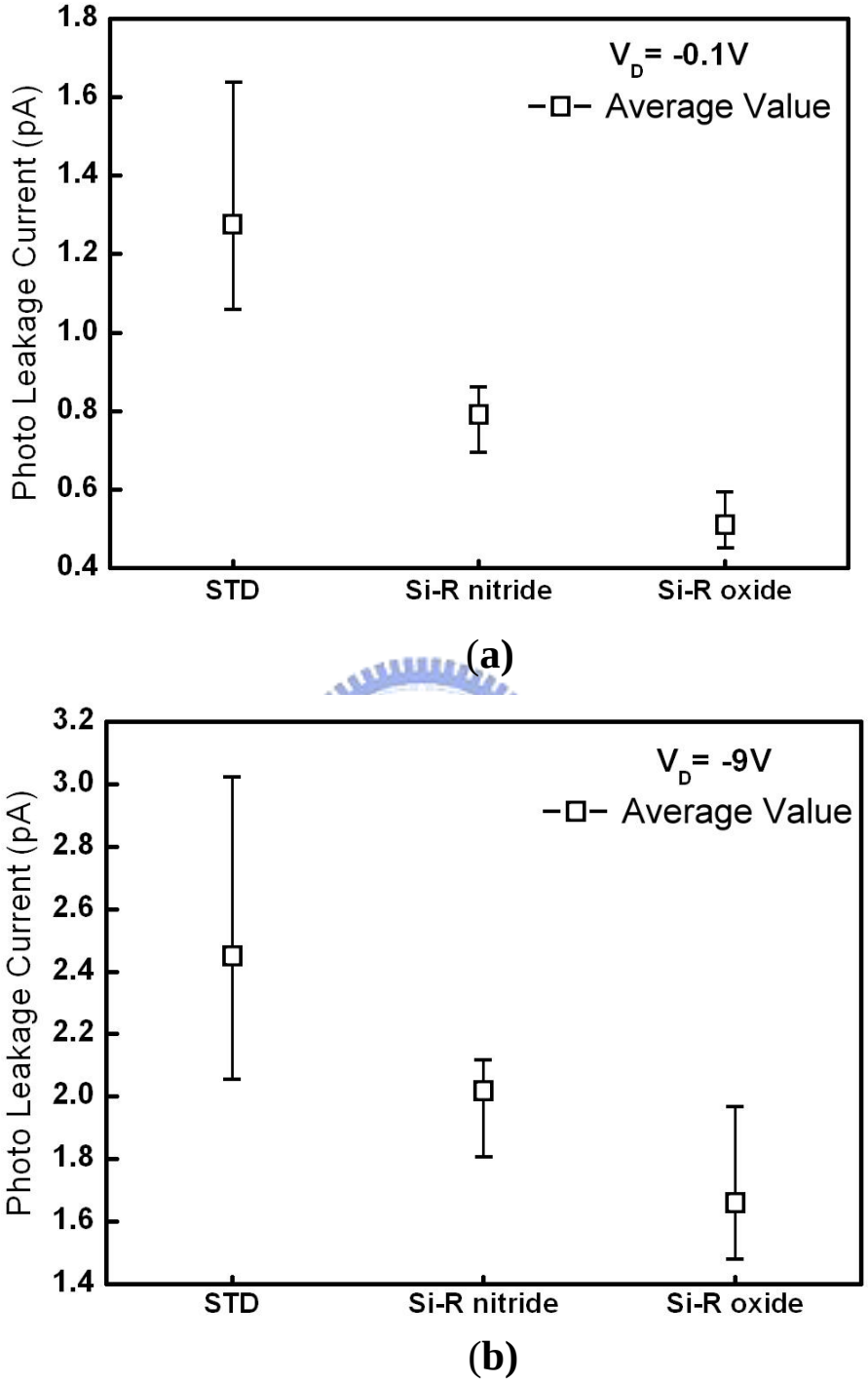


Fig. 3-5 (a)The results of photo leakage current in poly-Si TFT with conventional buffer layer, Si-rich oxide buffer layer and Si-rich SiN_X buffer layer as V_D is -0.1v. (b)The results of photo leakage current in poly-Si TFT with conventional buffer layer, Si-rich oxide buffer layer and Si-rich SiN_X buffer layer as V_D is -9v.

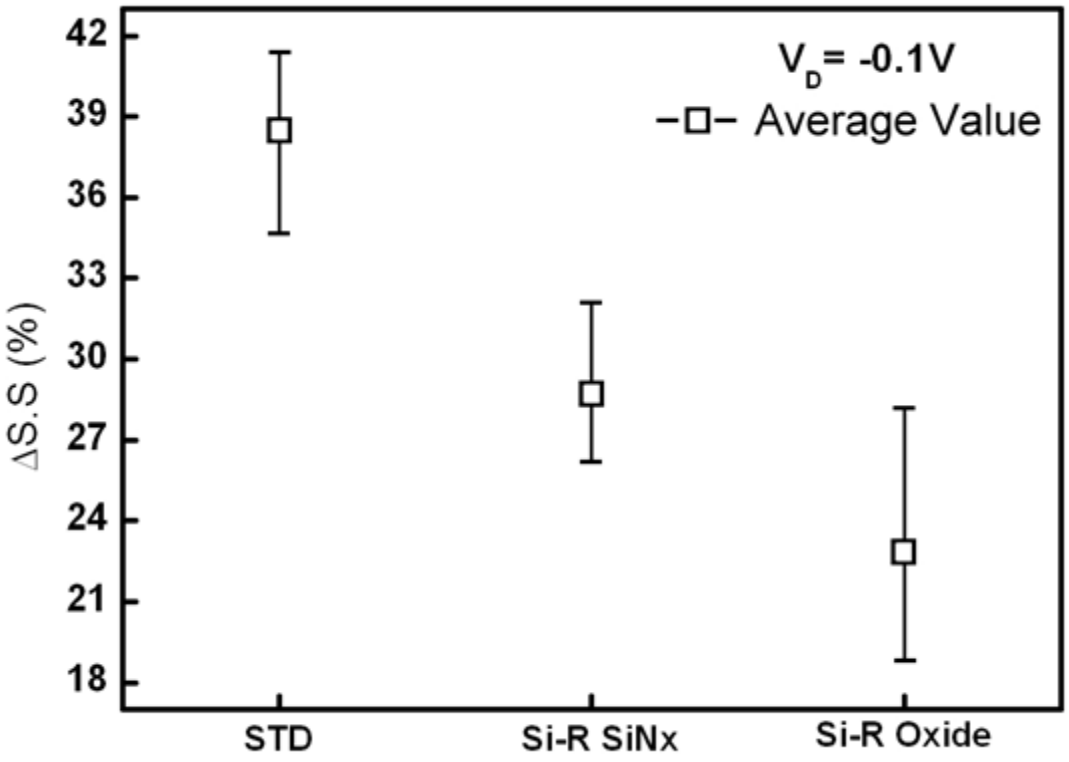


Fig. 3-6 The comparison of variation in sub-threshold swing extracted at linear region of poly-Si TFT with conventional buffer layer, Si-rich oxide buffer layer and Si-rich SiN_X buffer layer under illumination.

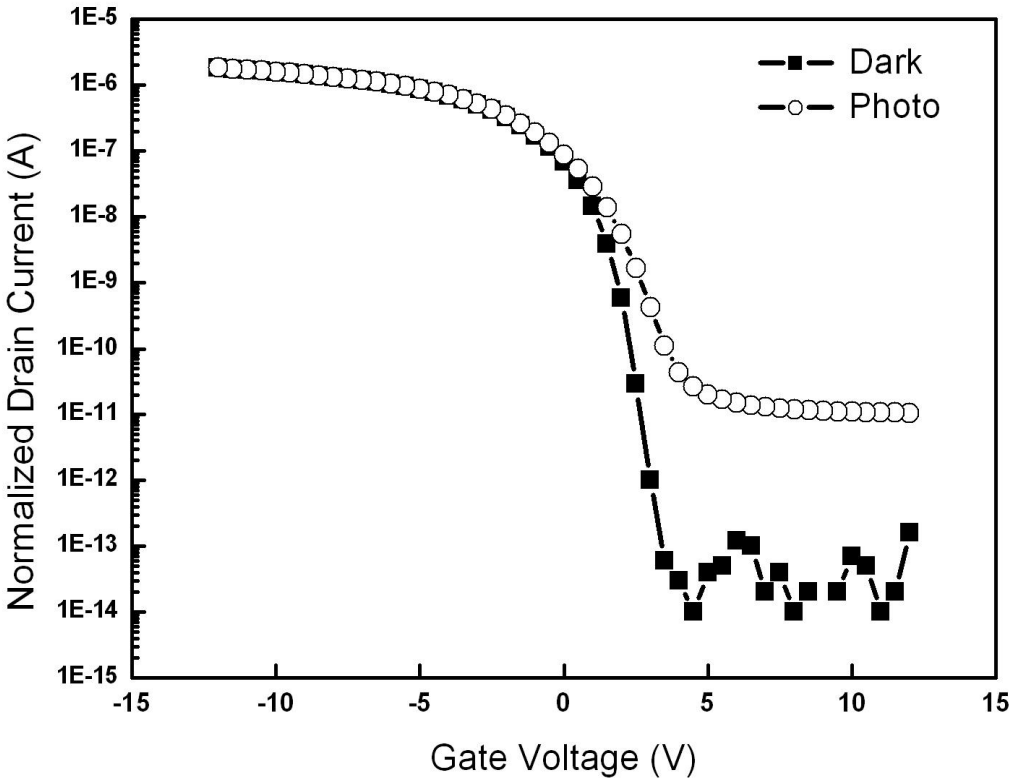


Figure 3-7 I_D-V_G curves of the conventional poly-Si TFT operated in the linear region under illumination and dark states. A significantly increase of leakage current was found.

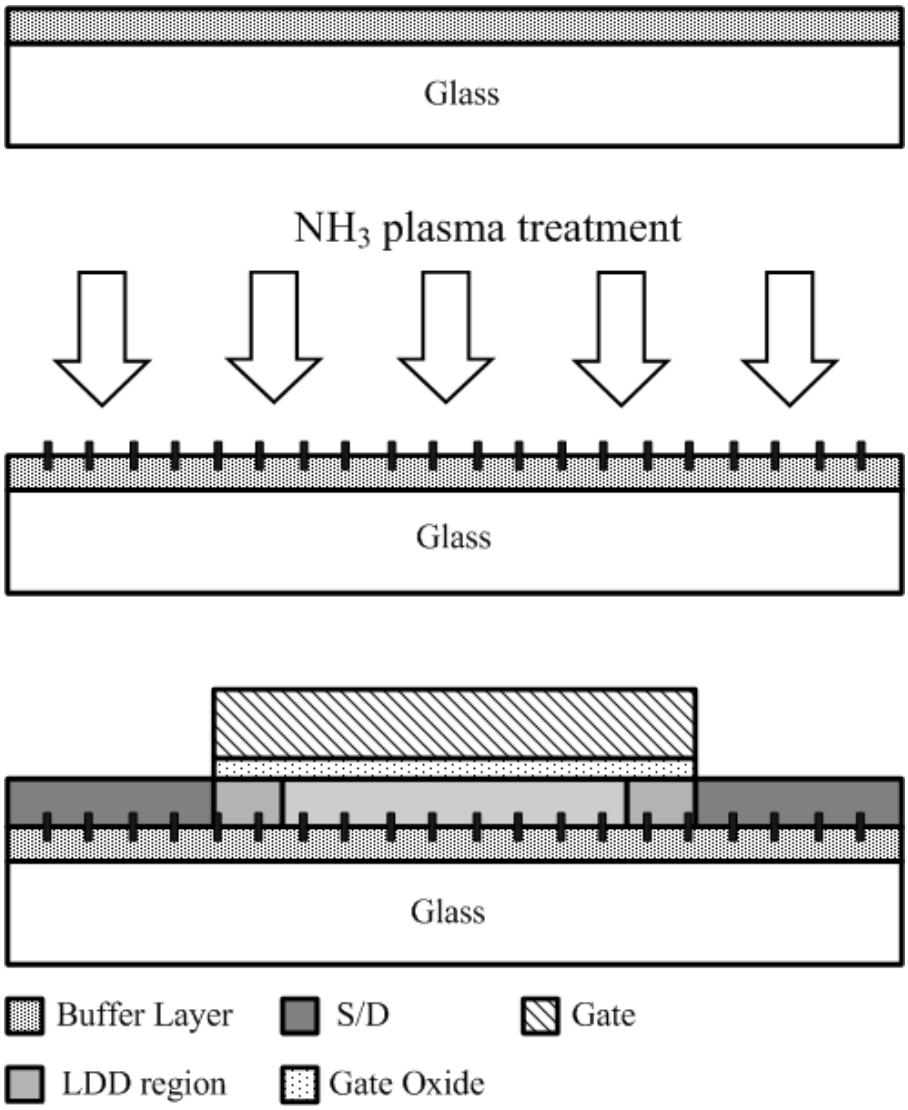


Figure 3-8 The proposed process diagram for treating the surface of buffer layer using NH_3 plasma bombardment. Numerous state densities are generated to be taken as the recombination center for light-induced electron-hole pairs.

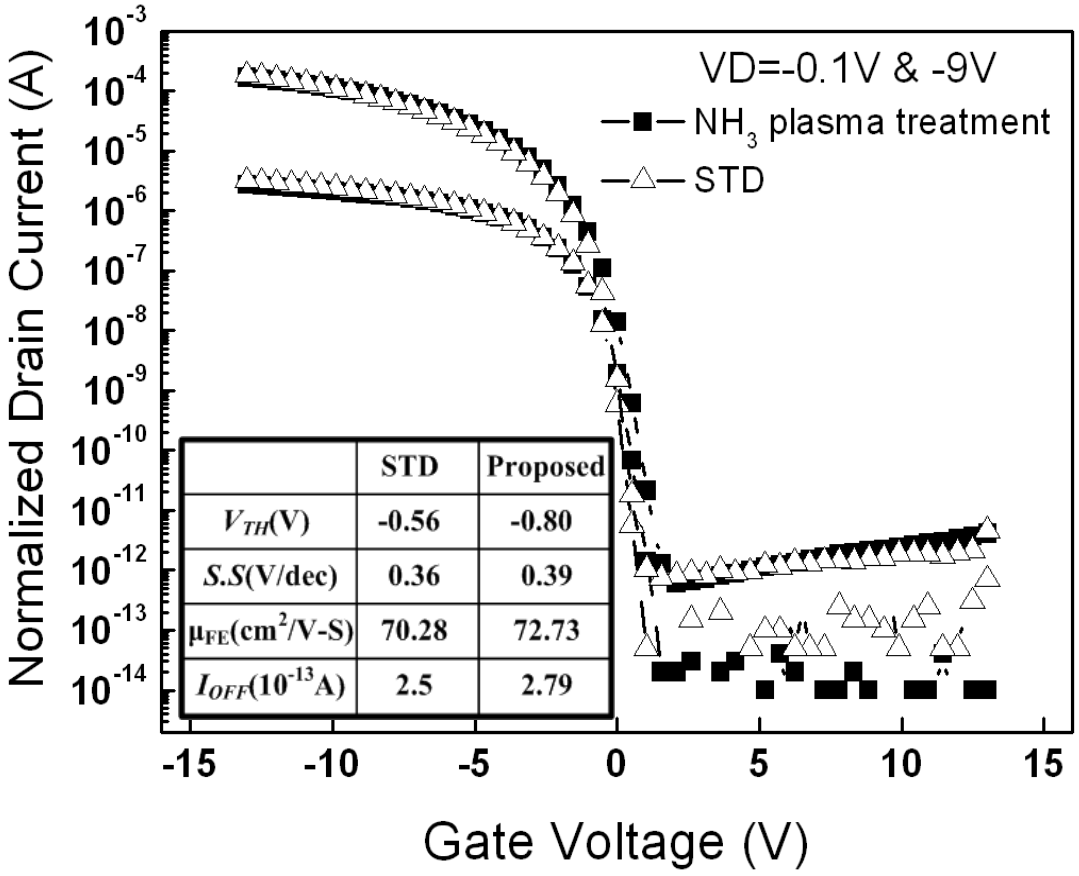


Fig. 3.9 The comparison of electrical characteristics in conventional and proposed TFTs under dark state

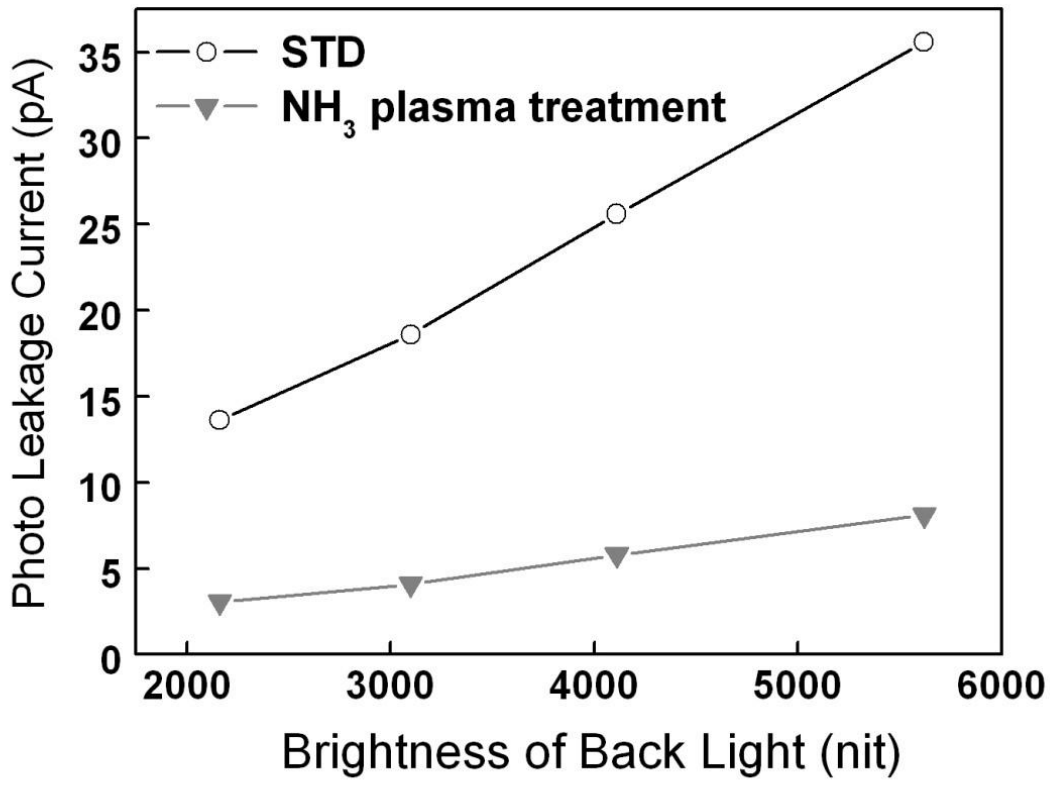


Figure 3-10 As the brightness of back-light is set as 2160, 3100, 4110 and 5620 nit, the comparison in photo leakage current of conventional and proposed devices. The remarkable reduction of photo leakage current in proposed TFT is observed.

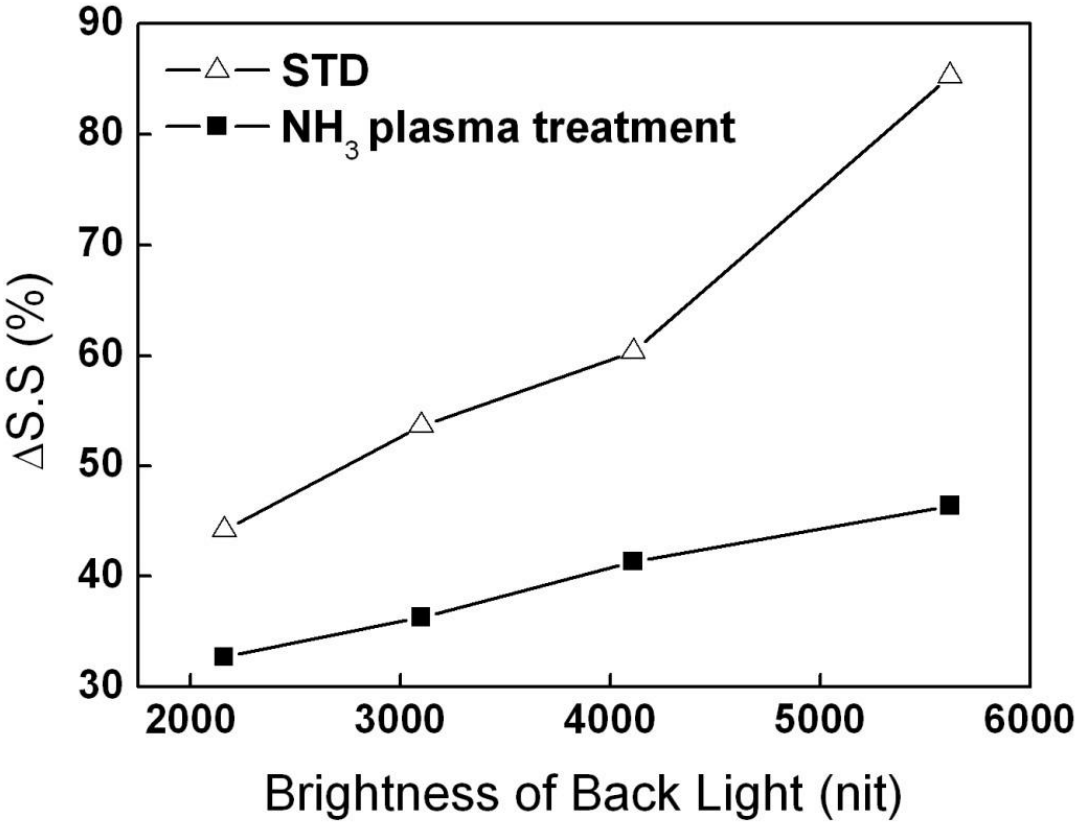


Fig. 3-11 As the brightness of back-light is set as 2160, 3100, 4110 and 5620 nit, the sub-threshold swing of conventional and proposed devices. As the brightness of back-light is 5610 nit, the maximum ΔS.S of conventional and proposed TFT are 46.4% and 85.3%

Chapter 4

Study on Electrical Characteristics of Poly-Si TFT under Illumination

4.1 Introduction

Low-temperature polycrystalline-silicon thin film transistors (poly-Si TFTs) are attractive as the active devices in pixel switch element and driving circuits of active matrix liquid crystal displays (AMLCDs) and active matrix organic light-emitting diode display (AMOLED) applications [4.1-4.4]. The poly-Si TFTs offer great potential for AMDs technology, due to their superior electrical characteristics over those of amorphous Si thin film transistors (a-Si:H TFTs) and the existence of complementary devices. Recently, to meet the demand of high-end mobile devices which include functions such as cellular phone, digital camera, music player, GPS, mobile TV and so on, the development of mobile displays with higher resolution, higher image quality, lower power consumption and cost competitiveness is inevitable. Since people usually use these mobile electronic products under sunlight, the outdoor readability becomes a critical issue for high-end mobile AMLCDs. Therefore, the brightness of back-light is getting higher and higher for the requirement for clear image quality and superior readability outdoor [4.5-4.6]. However, the poly-Si TFTs exhibit undesirable photo leakage current under a high illumination environment [4.7-4.9]. The high leakage current and increased sub-threshold swing of poly-Si TFT under illumination in TFT-LCD displays should be reduced to avoid losing the charges stored in pixels. Therefore, the voltages that are held across the pixel

electrodes would be diminished to affect the gray level controlling, which in turn, would cause a low contrast ratio and error color display. Several studies for characterization and suppression of photo leakage current in poly-Si TFT have been proposed [4.10]. However, the investigations about the electrical characteristics of poly-Si TFTs under illumination are very few and the mechanism of degradation of sub-threshold swing (S.S) in poly-Si TFT exposed to back-light is still not clarified.

In this chapter, I_{PLC} and S.S behavior of poly-Si TFT with specific process steps under illumination is discussed. First, the I_{PLC} and sub-threshold properties of poly-Si TFT with treated buffer layers at photo and dark states are investigated. It is observed that the I_{PLC} and the degradation of S.S in TFT with treated buffer layers are significantly reduced. Therefore, the photo-induced degradation of S.S is strongly dependent of the amount of excess electron-hole pairs as poly-Si TFT is operated in illumination environment. In order to clarify the factors to affect the sub-threshold properties of poly-Si TFT under illumination, a patterned metal shielding layer is used to investigate the electrical characteristics of poly-Si TFTs under light exposure. By patterned metal shielding structure, the exposure region is controlled to be located in the drain or source junction. Based on the analysis of measurement results, the key factors effectively influencing the photo leakage and the sub-threshold swing are observed clearly in this work.

4.2 Experimental Procedure

Two kinds of n-type poly-Si TFTs with lightly doped drain (LDD) were fabricated in this letter. First, a 50 nm-thick SiNx and a 150nm-thick SiO_2 films were sequentially deposited to form buffer layer by plasma enhanced chemical vapor deposition (PECVD). Then the surface of buffer oxide is bombarded by Argon (Ar)

ion implanter for 1 minute, as shown in Fig. 4.1. Next, 50-nm-thick undoped amorphous-Si (a-Si) film was deposited by PECVD at 380℃, followed by dehydrogenated via furnace annealing process at 450℃. The a-Si films were crystallized by 308nm XeCl excimer laser with the line-shaped beam power of 350mJ/cm^2. The 100nm thickness gate insulator was deposited by TEOS (Tetra-Ethyl-Ortho-Silicate)-base oxide. The source/drain and LDD region were formed by the mass-separated ion implanter technique. The doping activation was performed by RTA. MoW was sputtered as a gate metal. Therefore, the treated TFT is obtained by the process above mentioned.

In addition, before the formation of buffer layer, an 80nm thick molybdenum film was sputtered on glass substrate to be a shielding layer and was patterned using additional mask for the shielding TFT. Then, the following process is identical totally as the standard one, without bombardment on the surface of buffer layer by Ar ion implantation. Figure 4.2 indicate the cross-sectional view of poly-Si TFT with patterned metal shielding layer. The space between the edge of metal shielding layer and gate metal is defined as 1.5μm. Therefore, a 3μm-width region in the junctions would be exposed to the back light. The dimensions of two type TFTs both were channel length (L) 30μm, channel width (W) 6μm and the LDD length 1.25μm. The brightness of back-light for photo state measurement is set as 3100nits.

4.2.1 Photo Sub-threshold Properties of Treated Poly-Si TFT

Figure 4.3 and Fig. 4.4 shows the I_D-V_G transfer curves of conventional TFT and treated TFT operated in linear region, respectively, under the dark and photo states. The photo leakage current (I_{PLC}) of conventional TFTs is 17 pA and the S.S is degraded significantly under illumination, about 0.45 V/decade, as the initial value in

dark is 0.29 V/decade. The variation of S.S is about 75%. By contrast, for treated TFT, the I_{PLC} is 3.6 pA and the S.S under illumination increases 35% compared to that in dark state. It is observed that not only I_{PLC} in treated TFT is lowered but also the change of S.S is less than that of conventional TFTs. As poly-Si TFT is exposure to light, plenty of electron-hole pairs are generated in the bottom of poly-Si film as shown in Fig. 4.5 [4.8]. The excess electrons flow to the drain directly under the positive drain bias for n-channel devices, generating the I_{PLC}. It follows that the residual holes are accumulated in the channel of poly-Si TFTs. Therefore, the trap states on the surface of the buffer layer in treated TFT induced by the Argon ion bombardment would assist the recombination of excess electron-hole pairs. Therefore, the fewer excess electron-hole pairs lead to the lower I_{PLC} and less variation in S.S. It is verified that the I_{PLC} and the degradation of S.S in poly-Si TFT under illumination are strongly dependent of the photo-induced excess electron-hole pairs. However, the mechanism of the leakage current and S.S of poly-Si TFT under illumination influenced by photo-induced electron-hole pairs is not clarified in detail. Therefore, we use a patterned metal shielding layer to control the light exposure region of poly-Si TFT. By this ingenuity, the effective regions leading to I_{PLC} and variation of S.S can clearly observed to investigate the behavior of poly-Si TFT under illumination.

4.2.2 Investigation of Electrical Characteristics in Poly-Si TFT under Illumination Using Patterned Metal Shielding Layer

Figure 4.6 shows the I_D-V_G characteristics of shielding TFT with low drain bias measured in forward and reverse modes at dark. The exposure region is located close to the drain and source junction for forward and reverse measurement, respectively. The two curves are almost identical and V_{TH} of TFT in forward mode (Forward TFT)

is as same as that of TFT in reverse mode (Reverse TFT). However, the V_{TH} of Reverse TFT is slightly less than that of Forward TFT while drain voltage is 9V, as shown in Fig. 4.6. Since the shielding layer for Forward TFT has a gap in drain junction, the potential distribution coupling from drain voltage would not extend into channel region. Therefore, V_{TH} of Forward TFT is independent of applied drain bias. By contrast, the shielding metal of Reverse TFT is distributed over most of channel region from drain. It is indicates that the potential distribution induced by high drain voltage, V_M, in the metal film of Reverse TFT would induce electrons in the back side to affect the V_{TH}. In addition, the S.S of Forward TFT and Reverse TFT is unchanged by drain voltage at dark.

Figure 4.7 plots transfer curves of Forward TFT operated in linear region at the dark and photo states. As the gate bias is -12V, the leakage current of Forward TFTs is about 10^{-14}~10^{-13} A at dark but is significantly increased under illumination. The I_{PLC} is $2.5x10^{-11}$A, approximately three orders of magnitude greater than the dark leakage current. In addition, the S.S is slightly raised under illumination. The S.S under dark and photo states is 0.36 V/dec and 0.39 V/dec, respectively. As the drain bias is 9V, the I_D-V_G relationships of Forward TFT at dark and photo states are illustrated in Fig. 4.7. Similarly, a markedly high I_{PLC} and the nearly unaltered S.S of Forward TFT under illumination are observed clearly. Since the width of depletion region at drain would be increased with high drain bias, the more electron-hole pairs induced by light would be separated in the depletion region. Therefore, in forward mode, the I_{PLC} at high drain voltage is higher than that under low drain voltage.

The I_D-V_G characteristics of Reverse TFT are also investigated in this work, as shown in Figs. 4.8. As V_D is 0.1V, the I_{PLC} of Reverse TFT is $2.7x10^{-12}$A, as low as one order of magnitude, compared to that in Forward TFT under same drain voltage.

Furthermore, the S.S of TFT under illumination in Fig. 4.8 is almost unchanged. The increase ratio of S.S in Reverse TFT is about 7.96% as drain bias is 0.1V. Figure 4.8 indicates that the S.S of Reverse TFT with high drain voltage, however, is substantially degraded under illumination. It is increased 64% of the magnitude of that at dark state. With high drain bias, the I_{PLC} is also increased in Reverse TFT but still lower than that in Forward TFT. From the comparison in Forward TFT and Reverse TFT with high and low drain bias, it is inferred the significant increase of S.S in the Reverse TFT would be attributed to that the exposure region is located in source junction and the device is operated with high drain voltage.

For Forward TFT, the exposure region is located at the drain junction so that plenty of electron-hole pairs originated from light would be easily separated due to the electrical field at junction. Therefore, excess electrons could flow directly to the drain, leading to the I_{PLC}, as shown in Fig. 4.9. By contrast, the exposure region of Reverse TFT is close to source side. As the drain bias is low, numerous electron-hole pairs generated in source junction is difficult to be separated by lateral electrical field. Therefore, the excess electrons flowing to drain is fewer to cause the lower I_{PLC}. However, as the drain voltage is high, a positive potential distribution, V_M, in the metal film owing to the coupling effect is generated from the parasitic capacitance in the overlap of drain and metal shielding layer [4.11]. Hence, electrons induced by V_M gather to form the back channel in the bottom of poly-Si layer, as illustrated in Fig. 4.9. So that excess electrons at source junction would flow to drain through the back channel and excess holes is residual to be accumulated in the source junction to form the floating body which offers a positive potential. It can be inferred that the degraded S.S in poly-Si TFTs under illumination is mainly caused by the floating body with positive potential near the source side. The key factors to affect I_{PLC} and the S.S under

illumination are clarified clearly using the patterned metal shielding layer in poly-Si TFTs.

When the gate bias is below the threshold and the semiconductor surface is in weak inversion or depletion, the corresponding drain current is the sub-threshold current. In weak inversion and depletion, the electron charge is small, the drain current is dominated the diffused electron from source in n-type poly-Si TFT. Therefore, it would be affected strongly by the barrier height of source. As the gate bias is applied, the barrier height of source is lowered to increase the amount of electron in channel diffused from source. Therefore, it is clearly observed that the S.S current is dependent of the applied gate voltage. The sub-threshold current in poly-Si TFT is empirically expressed [4.8]:

$$\mathbf{I_{sub} = I_{sub0} exp[\frac{q(V_G - V_{G0})}{nk_BT}]}$$

For simplify and giving more clear physics picture, it is also can be expressed as following equation [4.12]:

$$\mathbf{I_{sub} \propto exp(\beta \varphi_s)}$$

It indicates that, the drain current varies exponentially with $\boldsymbol{\varphi_s}$ in the sub threshold region, where $\boldsymbol{\varphi_s}$ is the surface potential.

Based on the experimental results of treated TFT and shielding TFT, a model of band diagram to explain the S.S degradation of poly-Si TFT is proposed, as shown in Fig. 4.10. First, as the excess electron-hole pairs are generated under illumination with positive drain voltage, the light-induced electrons flow to drain directly, forming the photo leakage current. Therefore, the residual excess holes are accumulated in the poly-Si film to form the floating body with a positive channel potential, ΔV. Hence, the source barrier is lowered by ΔV due to the floating positive potential distributed in the channel. While the applied gate bias is swept from negative to positive directions

and smaller than the threshold voltage, TFT would be operated at sub-threshold region. So the source barrier would be lower again by the positive gate bias. However, the more lowering source barrier induce that the excess holes accumulated in channel are more easily diffuse to the source to reduce the positive channel potential. So that the fewer channel potential leads to a raise of source barrier. It means that the source barrier is not only controlled by applied gate bias but also affected by the floating body with positive potential, ΔV when poly-Si TFTs are under illumination. In our method of treated TFT, the trap states on the top face of buffer layer can effectively recombine the excess electron-hole pairs induced by back light. So that amount of accumulated holes is also reduced effectively to suppress the effect of floating body. Hence, the improvement of sub-threshold swing is clearly observed in this work. In addition, the results of shielding TFT confirm that the effective region affecting by floating positive potential is the source junction.

4.3 Conclusion

In conclusion, the I_{PLC} and S.S properties of poly-Si are discussed in detail by two approaches. For treated TFT, the top surface of buffer layer is degraded by Ar ion bombardment. Due to the surface state densities induced by Ar ion implant, the excess electron-hole pairs are recombined directly. It is clearly found that the I_{PLC} is significantly reduced, compared the conventional poly-Si TFT. Furthermore, the degradation of S.S in treated TFT under illumination is suppressed. In addition, this work explores the electrical characteristics of poly-Si TFTs under illumination using patterned metal shielding layer. The Forward TFT exhibits the significantly high I_{PLC} and the slightly modified S.S under illumination. By contrast, the I_{PLC} in Reverse TFT is lower than that in Forward TFT at the same drain bias. The S.S under illumination is almost unchanged in reverse mode at low drain bias. However, a marked

degradation in S.S is observed in Reverse TFT with high drain bias operation. The increased ratio of sub-threshold swing for this case is 64%. Based on the results and proposed model, the causes of I_{PLC} and degraded S.S in poly-Si TFTs under illumination are demonstrated in this work.

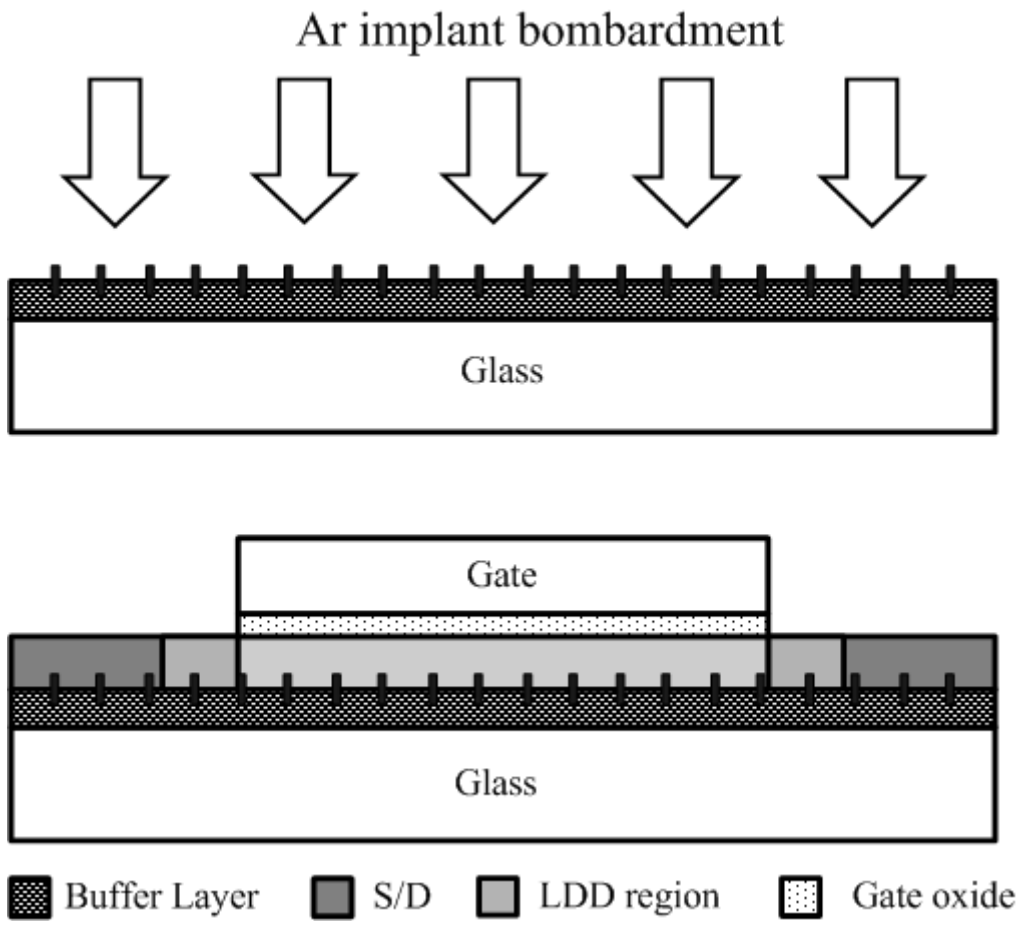


Fig. 4-1 The key process diagram for treating the surface of buffer layer using Ar ion implant bombardment. Numerous state densities are generated to be used as the recombination center for light-induced electron-hole pairs

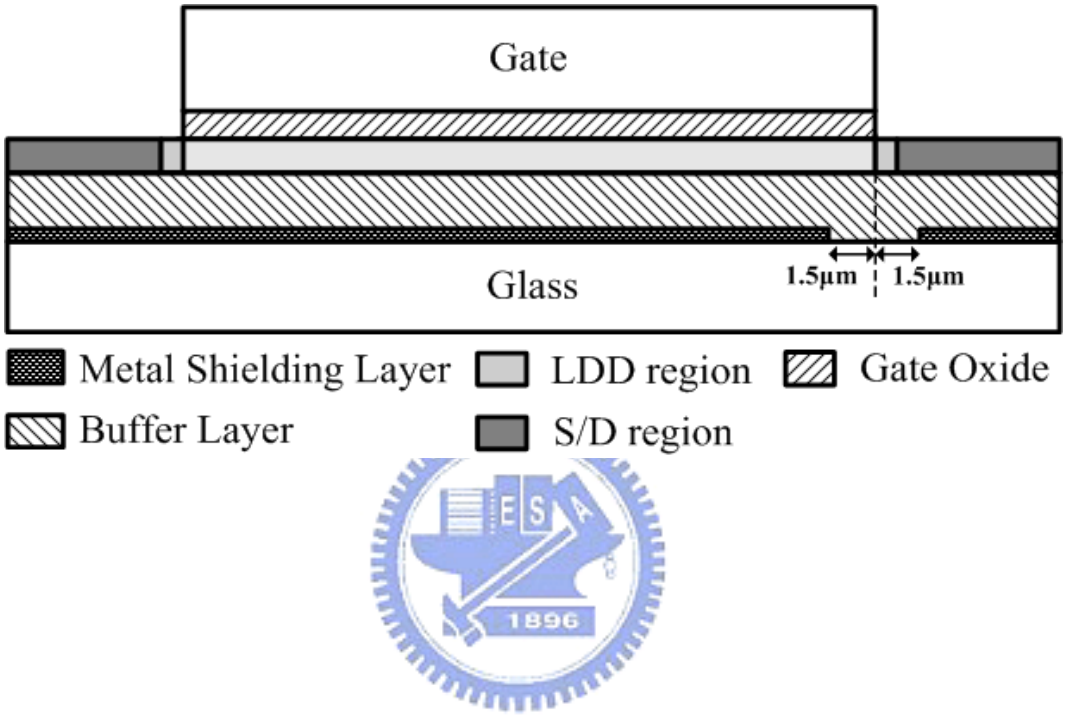


Fig.4-2 The proposed poly-Si TFT with patterned metal shielding layer. The width of exposure region is 3μm.

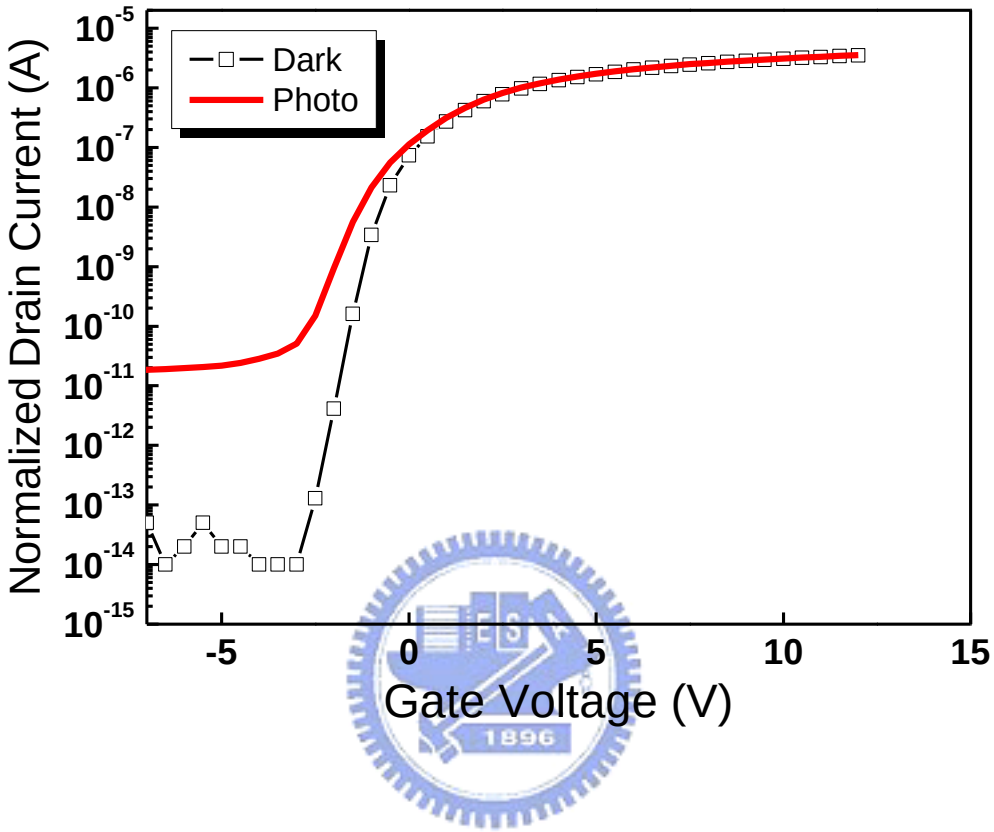


Fig. 4-3 I_D-V_G curves of the conventional poly-Si TFT operated in the linear region under illumination and dark states. A significantly increase in leakage current and sub-threshold swing was observed.

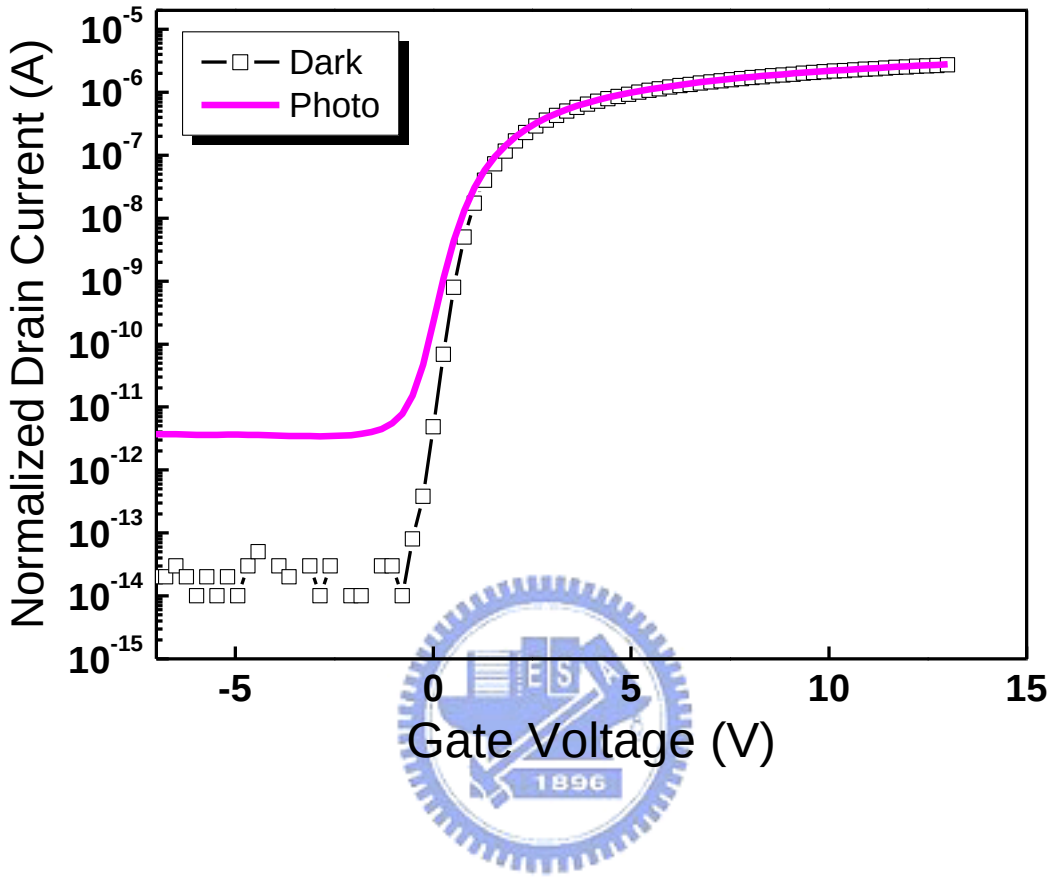


Fig. 4-4 The I_D-V_G characteristics in treated TFTs under dark state and photo state.

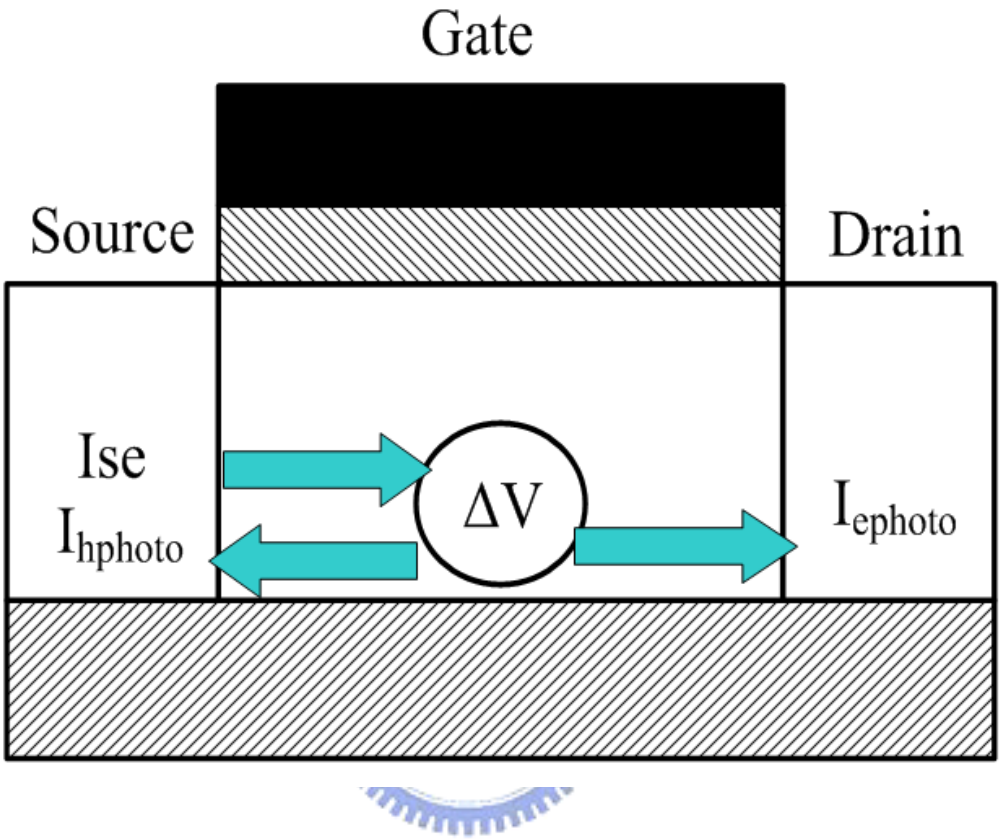
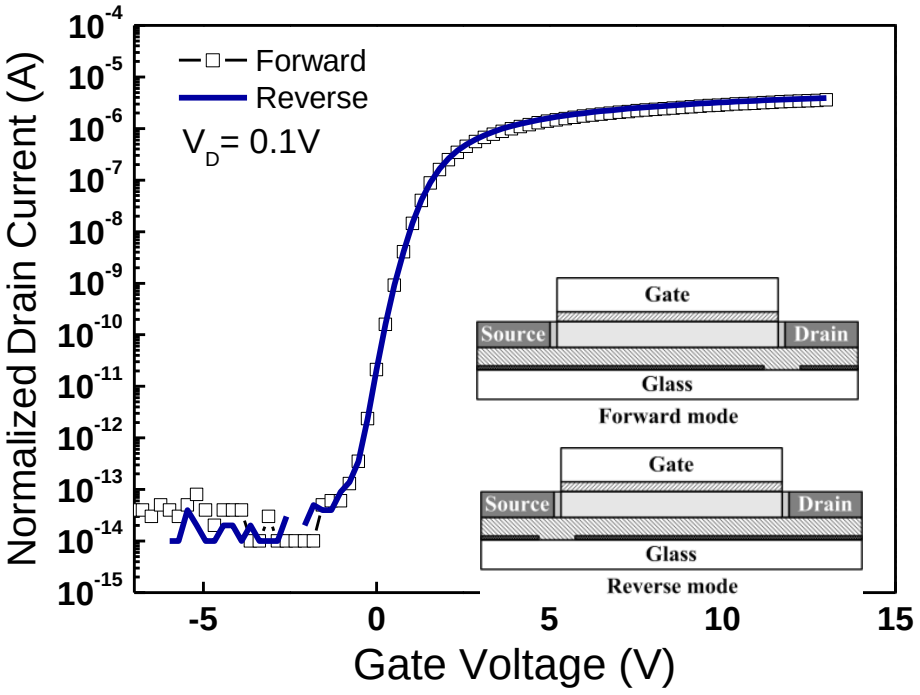
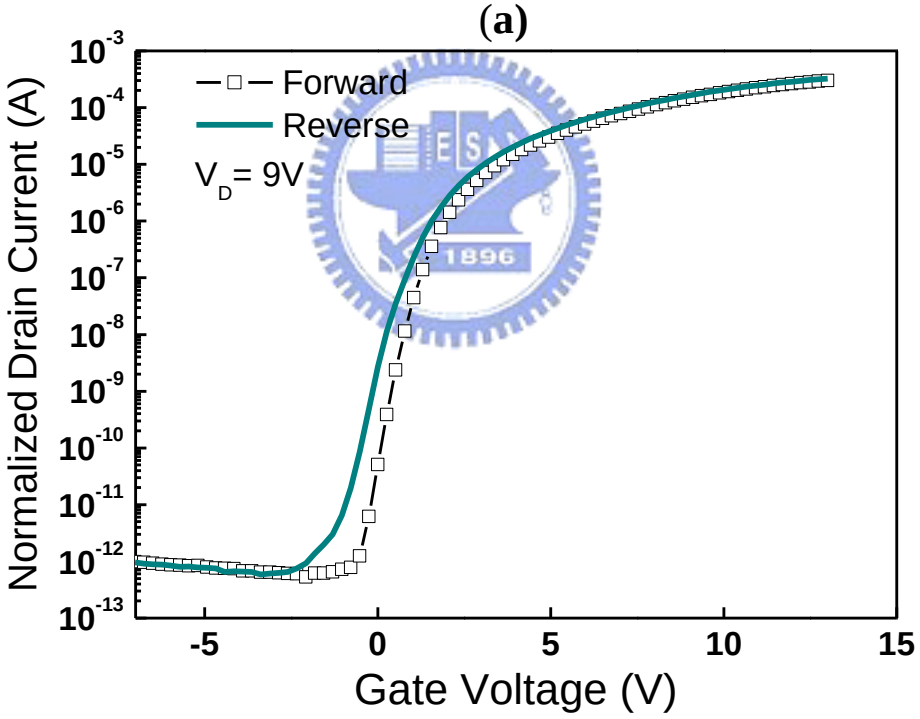


Fig. 4-5 Explanation of current flow of poly-Si operated under illumination.

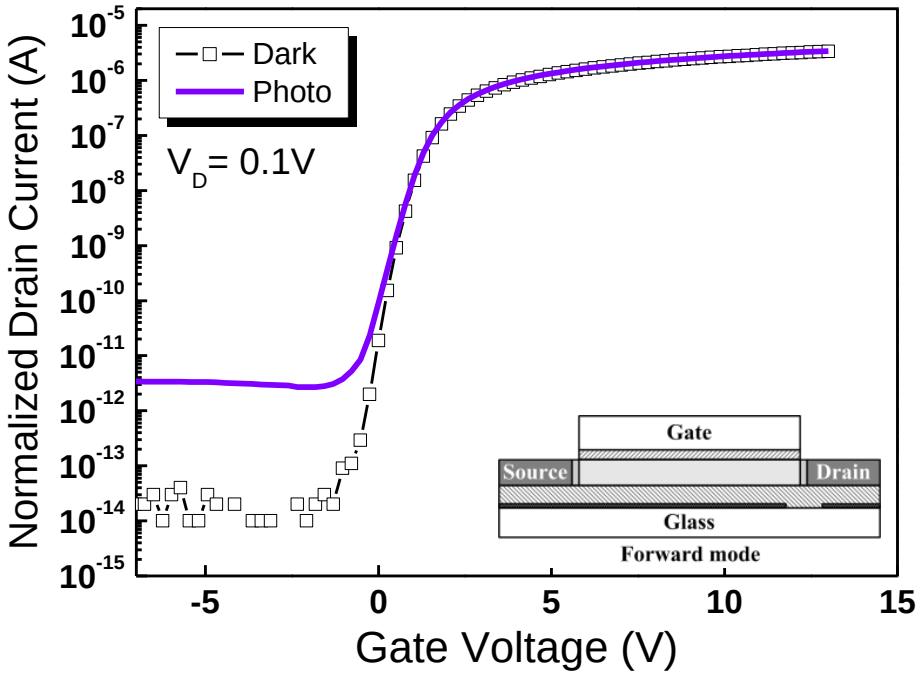


(a)

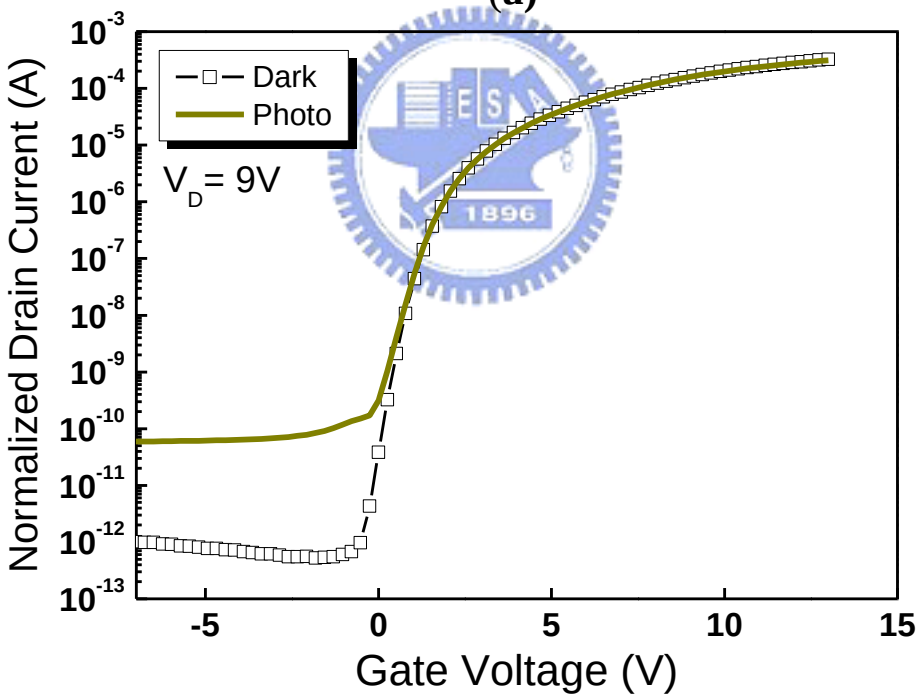


(b)

Fig. 4-6 I_D-V_G characteristics of proposed TFT operated with low and high drain voltage in forward and reverse modes at dark

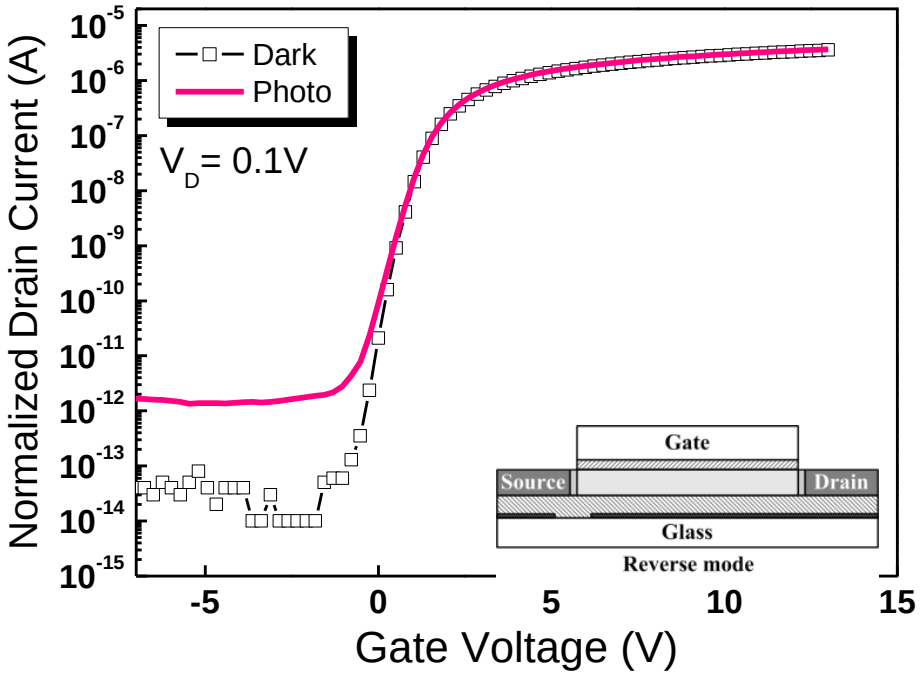


(a)

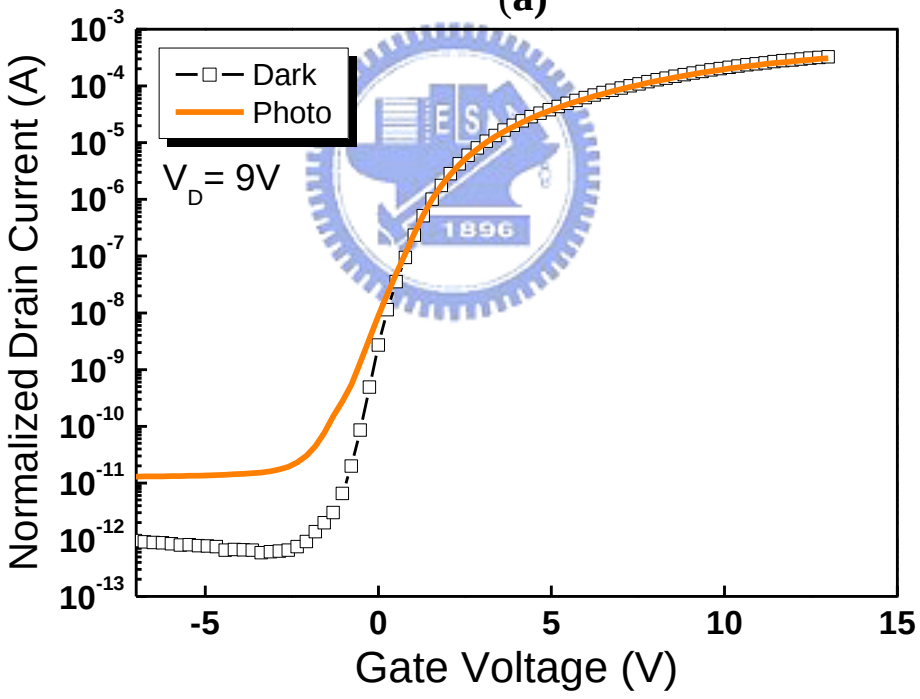


(b)

Fig. 4-7 I_D-V_G curves of poly-Si TFT in forward measurement as drain bias is 0.1V and 9V. A high photo leakage current and almost unchanged sub-threshold swing are observed.



(a)



(b)

Fig. 4-8 I_D-V_G curves of poly-Si TFT in reverse measurement as drain bias is 0.1V and 9V. With the low drain bias, the photo leakage current is lower than that in forward mode and the sub-threshold swing is also nearly unchanged. However, S.S is degraded markedly with high drain voltage.

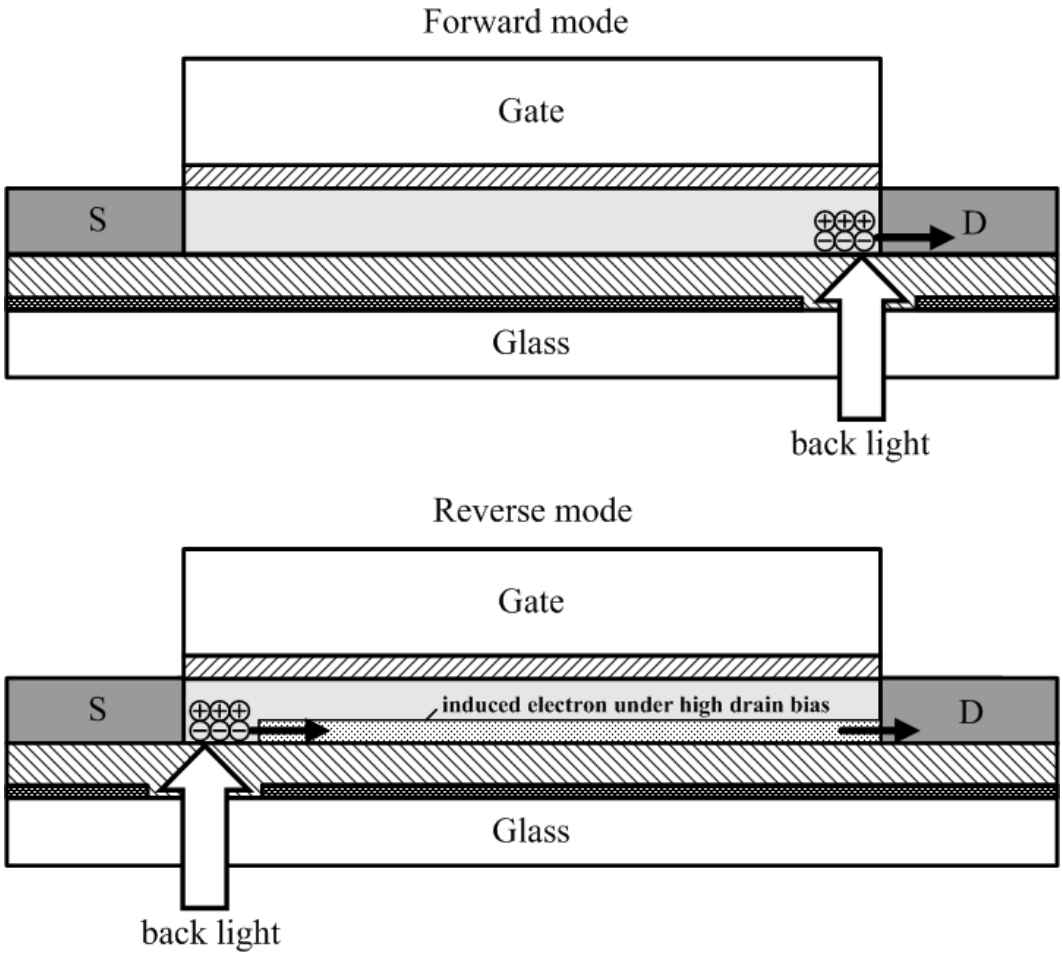


Fig. 4-9 The diagrams of proposed model for electrical characteristics of poly-Si TFT with patterned metal shielding layer under back light in forward and reverse modes, respectively.

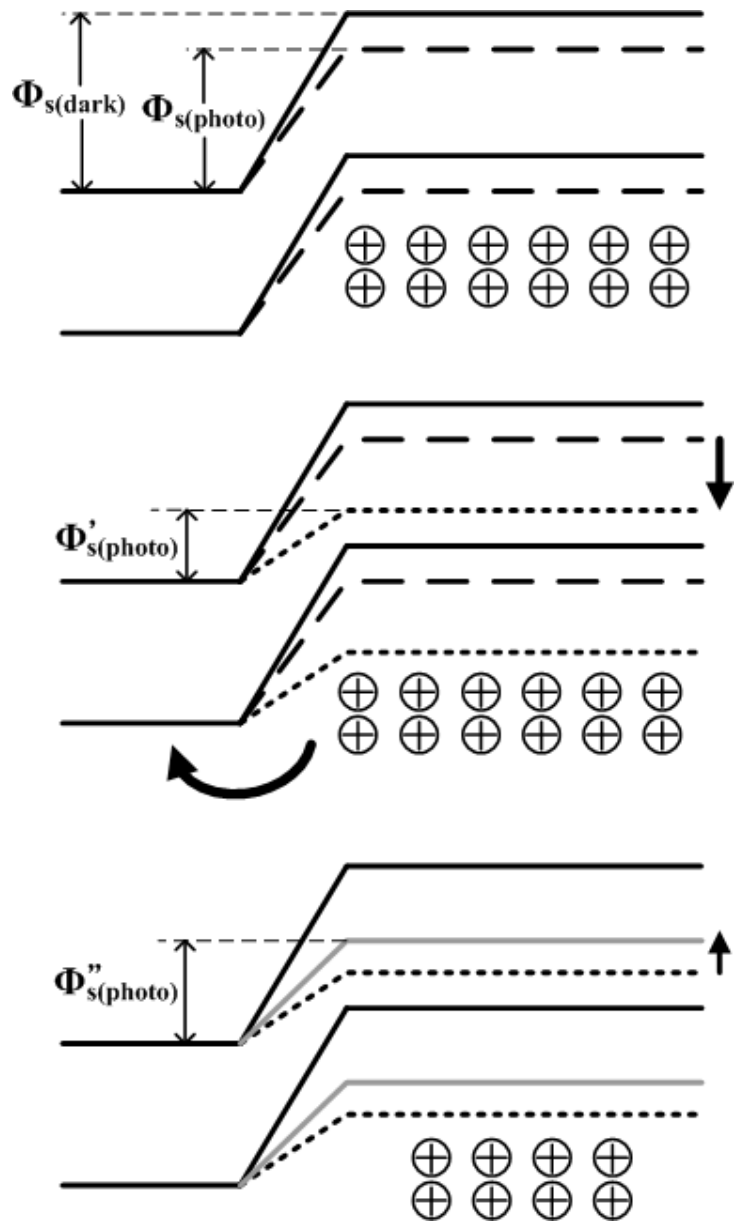


Fig. 4-10 Proposed band diagram to explain the degradation of sub-threshold swing in poly-Si TFT under illumination

Chapter 5

Study on Characteristics in Poly-Silicon Thin Film Transistors under Dynamic Stress

5.1 General Background

Low-temperature polycrystalline-silicon thin film transistors (poly-Si TFTs) have been widely investigated for flat-panel applications such as active matrix liquid crystal display and active matrix organic light-emitting diode display [5.1-5.3]. Poly-Si TFTs can be fabricated on the low-cost glasses substrate, because the maximum process temperature is lower than 600℃. However, a low temperature process often results in numerous defects at the poly-silicon boundaries. The defects in poly-Si grain structures play an important role in the electrical performance and stabilities of poly-Si TFTs. The poly-Si TFT can be produced as complementary N-channel and P-channel transistors. Taking advantage of these features, poly-Si TFTs are applied for pixel TFTs and the driver circuits (e.g., scan driver). Substantial improvement in the electrical characteristics of poly-Si TFTs is the most critical issue in the further integration of peripheral circuits on glass substrates. Enlarging the grains in poly-silicon layers is an effective approach for improving TFT performance. Several poly-Si re-crystallization methods based on laterally grown grains have been proposed to enlarge the grains and control the location of the grain boundaries [5.4-5.5]. However, protrusion at grain boundaries is a result of the laser crystallization of poly-Si films - especially with laterally grown grains [5.6].

The operation of TFT devices in driving circuits are frequently subject to

high-frequency voltage pulses [5.7]. The degradation behavior under dynamic stress is even critical for the real operation than the static stress conditions. Therefore, investigation of degradation mechanism in poly-Si TFTs under dynamic stress is really essential requirement in realization of system-on-panels (SOP) technology. Previous research reports have shown a relationship between the creation of states and hot-carriers effect by performing dc stress [5.8-5.9]. The degradation mechanism of ELC and laser-crystallized laterally grown poly-Si TFT under dynamic voltage stress, however, has not been clarified.

In this study, the degradation under dynamic operation for poly-Si n-channel TFT will be clarified by C-V measurement. Since the trap states in the Si band gap would respond to the applied signal frequency, the degradation mechanism and damaged sites of n-channel poly-Si TFTs after dynamic stress can be evaluated in C-V measurements. Moreover, the trap states located in the band gap is also identified by the C–V results with various small signals. In addition, poly-Si TFT with protruding grain boundaries observably exhibits degradation under AC operation. Based on the analysis and simulation of electrical characteristics, a model of the electrical degradation of TFT with protruding grain boundaries is proposed.

5.2 Electrical Degradation Analysis of N-Channel Poly-Silicon Thin Film Transistors under Dynamic Stress by C-V Measurement

5.2.1 Experimental Procedure

N-channel poly-Si TFTs with top-gate structure were fabricated on a glass substrate. First, a thin 50 nm-thick undoped amorphous-Si (a-Si) film was deposited in a plasma enhanced chemical vapor deposition (PECVD) chamber, followed by dehydrogenated via furnace annealing process. After dehydrogenation, the a-Si films were crystallized

by XeCl excimer laser with the line-shaped beam power of 350 mJ/cm^2. Then, the 100-nm-thick gate oxide was deposited by PECVD. The source and drain regions were formed by the implantation of phosphorous ions at a dose of 5 x 10^{15} cm^{-2}. An annealing process was then performed to activate the dopant impurities. MoW layer was sputtered and patterned by photolithography and etch process as a gate metal electrode. The dimensions of TFTs in channel length and width were L = 30 μm and W = 30 μm, respectively. The stress pulses were conducted on the gate electrode as the dynamic stress, and source/drain electrodes were grounded. As for the stress condition, we used the rectangular pulse with amplifier of ±15 V and frequency of 500 kHz, as shown in Fig. 5.1. Both the rising time (Tr) and falling time (Tf) were set for 100 ns. Since the channel length is sufficiently long, the charge variation in the floating node induced by the small signal only slightly affects the total charge. The gate-source capacitance (C_{GS}) was measured with a floating drain, while the gate drain capacitance (C_{GD}) was measured with a floating source. Therefore, the C_{GS} and C_{GD} values may be not affected by the floated node [5.10].

5.2.2 Results and Discussion

Figure 5.2 shows the I_D-V_G transfer curves of n-channel poly-Si TFT with dynamic stress duration for 10, 100, and 1000 s. The ON-current was significantly decreased with the increasing stress duration. With the stress duration for 10s and 100s, the conducting current of TFT operated at V_G =15V was 92% and 40% of the magnitude of the initial value, respectively. After stress for 1000s, the ON-current degraded to 4% of the magnitude of the initial value was observed. However, for the different stress durations, the sub-threshold slope (0.12 V/dec) and the threshold voltage (2.37

V) were almost unchanged. In contrast, operated at the linear operation regions, on-current decrease of TFTs in a form of parallel shift was noticeable with the increasing dynamic stress time at the above threshold region of the I_D-V_G. The degradation in poly-Si TFTs is dependent on the nature of state generation after dynamic stress. In order to investigate the degradation mechanism and damaged regions in the n-channel poly-Si TFT after dynamic stress, the C-V measurement was conducted.

The I_D-V_D characteristics at V_G=10 V of the TFT with the dynamic stress times are illustrated in Fig. 5.3. It is observed that the current crowding effect on the TFT is significantly enlarged with the increase of stress time. Figure 5.3 also indicates parasitic resistance contributed to the degradation on electrical properties of the TFT. The parasitic resistance is dependent on the following several factors, such as the trap states near the source/drain junctions, sheet resistance of n+ poly-Si layer, and source/drain contact quality [5.11]. For a constant W/L ratio, the effect of parasitic resistance can be clearly seen in the output characteristics of TFTs. The large parasitic resistance would result in the current crowding effect, as shown in Fig. 5.3.

Figure 5.4 shows that the initial C_{GD} curve at the different measurement frequencies are stretched out and shifted in the positive voltage direction. The trap states present in the grain boundaries of the poly-Si TFT reduce the effective transit time of the carriers. Therefore, the behavior of C-V curves is affected by the measurement frequencies [5.12]. Since the charges trapped in the gate oxide and at the interface states are independent of the measurement frequency, the degradation mechanisms can be clarified by the C-V characteristics with various measurement frequencies.

Figures 5.5(a) and 5.5(b) show the C_{GS} and C_{GD} values separately after the stress

for 1000s. The C_{GD} and C_{GS} curves exhibit the same behavior due to the symmetrical device structure [5.13]. The stretched C-V characteristics with the measurement frequency indicate that degradation caused by dynamic stress was attributed to the generation of trap states in the grain boundaries rather than the interface trap states or the fixed trap charges. In addition, it means evidently the damaged regions are located in both the source and drain junctions. Figure 5.6(a) shows that the C-V curve measured at 10 KHz is not significantly changed. However, the C-V curve measured at 1MHz is stretched out seriously, shown in Fig. 5.6(b). In the C-V measurement, the carrier emission time from trap energy levels in the Si energy band gap will respond to the period of applied small signal. For the measurement frequency 10 kHz and 1 MHz, it would correspond the emission time of the deep trap states energy level (E_{deep}) closed to the middle of the band gap and tail state energy level ($E_{shallow}$) closed to the conduction band, respectively. For the n-channel poly-Si TFTs considered in this work, E_{deep} is 0.62 eV and $E_{shallow}$ is 0.75 eV above the valence band [5.14]. The trap energy level below E_{deep} has longer carrier detrapping time than the ones at trap state levels closer to the conduction band. If the number of traps at energy states below E_{deep} increases, the effective transit time of carriers is reduced effectively leading to the stretching out of the C-V curves at 10 kHz. As a result, the unchanged C-V characteristics at 10 kHz indicate that the amount of the traps at deep energy states is not enormously increased after dynamics stress. The significant stretched out of C-V characteristics at 1MHz are thereby attributed to the increase of traps at energy states near $E_{shallow}$, as the stress duration increases. The creation of additional traps at state closed to the conduction band after dynamic stress can be corresponding to the decrease of ON-current of TFTs in the form of parallel shift at linear region. The generated trap states produced by the strained bounds in poly-Si film are responsible

for the electrical degradation of n-channel poly-Si TFTs after dynamic stress.

5.3 Degradation of Laser-Crystallized Laterally Grown Poly-Silicon Thin Film Transistors under Dynamic Stress

5.3.1 Experimental Procedure

Buffer SiO_2 films and 50nm-thick amorphous silicon films were deposited by plasma-enhanced chemical vapor deposition (PECVD), and the films were then dehydrogenated by furnace annealing. Following dehydrogenation, the a-Si films were crystallized by lateral solidification laser annealing. The crystallization process is an excimer-laser projection-based scheme for the crystallization of thin films on amorphous substrates. This process was conducted using a system that comprised 1) a 308nm XeCl excimer laser, 2) "A reticle mask with one rectangle and two triangles on the edge", 3) projection optics and 4) a high-precision) translation system, as shown in Fig 5.7. Following re-crystallization, 100 nm-thick gate oxides was deposited by PECVD. Metallic alloy MoW film was sputtered as a gate electrode, and phosphorous ion doping was performed to form source and drain (S/D) regions. The stress pulses were applied to the gate electrode when the dynamic stress and source/drain were grounded. Under stress, a rectangular pulse with amplitude of ±10V and a frequency of 500 kHz was used.

5.3.2 Results and Discussion

Figure 5.8(a) presents the high-resolution scanning electron microscopy (SEM) top-view image of the poly-Si film. The poly-Si thin film includes a domain region that contains a mixture of a plurality of crystals that are mostly parallel to the carrier

body. The grain boundaries (GBs) that are present in the poly-Si film can be divided into two types, referred to as main-GBs and sub-GBs as shown in Fig. 5.8(b). The grain boundaries lie between main-GBs are called sub-GBs, and most are parallel to the transport paths of carrier flow in the electric field of the drain side. The width of each main-GB is about100 nm and the space between main-GBs is approximately 3.5 μm, as measured by atomic force microscopy (AFM) which is illustrated in Fig. 5.8(c). The height of the protrusion is about 80nm at the grain boundary region. The channel length of TFTs in this work is 3μm for all samples and smaller than the grain size (3.5μm). Accordingly, the channel region of TFT might be located entirely inside the grain zone, but some TFT devices contain a main-GB within the channel.

Figure 5.9 plots the I_D-V_G relationships of TFT with main-GB (GB-TFT) and with no main-GB (NGB-TFT) during 10 to 1000 s of dynamic stress. Both the sub-threshold swing and the threshold voltage of GB-TFT and NGB-TFT were slightly damaged during stressing. The on-current in the TFT decreased significantly as the stress duration increased. The $\Delta\mu/\mu_o$ of NGB-TFT and GB-TFT is 27.9% and 43.6% after 1000s of stress, respectively. The significant degradation in mobility is consistent with the result of the conventional ELC poly-Si TFTs under AC stress. However, the electrical characteristics of GB-TFT degraded more under AC gate pulse stress. The distinct differences between the NGB and the GB-TFT device are the existence of GB and the surface roughness of the poly-Si film. The NGB-TFT has a channel region with a smooth surface, and an obvious protrusion of 80nm is located in the middle of GB-TFT.

Figure 5.10 plots the capacitance-voltage (C-V) curves of the GB and NGB-TFTs. The bold and dashed lines plot the C-V characteristics of the GB and NGB TFTs, respectively, at a measurement frequency of 50 kHz. The maximum capacitance of the

GB TFTs substantially exceeds that of the NGB-TFTs. As the gate bias (VG) of an n-channel TFT device is increased, capacitance rises from a minimum to a maximum, which equals the capacitance of the gate oxide. The thickness of the gate oxide deposited on the protrusion is only approximately 10% lower than that observed from the TEM image of GB-TFTs. The device simulator software, ISE TCAD, was used to clarify this result. Figure 5.11 plots the simulated electric field distribution for the TFT with and without a protrusion grain boundary, for V_G=10V and V_S=V_D=0V. Since the protrusion peak causes the concentrated electric field, the electric field is enhanced from 1MV/cm for the even surface between the oxide and poly-Si to 5.3MV/cm at the protrusion grain boundary. Hence, the carrier density is higher in the protrusion region, such that the gate oxide capacitance of the GB TFTs is superior, indicating that more free carriers are induced into the channel of the GB TFTs than into the channel of the NGB TFTs, at a high gate bias voltage.

Based on the results described above, a model of the degradation mechanism is proposed, as presented in Fig. 5.12. When the gate voltage is “high”, more electrons gather to form a channel in the GB TFTs because of the electric field concentration in the protrusion peak. Since the protrusion region comprises numerous trap states, plenty of the electrons that are transported to the protrusion region are trapped at the grain boundaries. Consequently, the induction of more electrons in the channel of GB-TFTs increases the concentration of trapped electrons. As the gate voltage settles from high to low, most of the free carriers are swept out before the electric field rises. When the various trapped electrons in GB TFTs are exposed to the high electric field, they gain energy from that field. The degradation in GB TFTs is thus more severe than that of NGB TFTs.

5.4 Conclusion

In this work the distinct decrease in ON-current of n-channel poly-Si TFT was observed during the dynamic voltage stress. The damaged regions which contain numerous trap states are evidenced to be near the source/drain region by the C-V measurements of C_{GD} and C_{GS} curves at increasing frequencies. Also, the electrical degradation is mainly attributed to the generation of additional trap states near the source/drain regions. Since the C-V characteristics at 10 kHz are unchanged but the ones at 1MHz are stretched out significantly, the creation of traps at state closed to the conduction band after dynamic stress is responsible for the degradation in ON-current of TFT. Furthermore, this investigation explores for the first time the electrical degradation in laser-crystallized laterally grown poly-Si TFTs with and without a protrusion grain boundary. The degradation in the I_D-V_G transfer characteristics of TFT is similar to that in those of conventional ELC TFTs. However, the electrical degradation of GB-TFT is worse because of the effect of protrusion grain boundary. C-V measurements and device simulation demonstrate reasonably that the concentration of the electric field in the protrusion region causes intense electron gathering at the grain boundary. As the AC gate bias is varied from high to low, trapped electrons in GB TFTs gain energy, severely degrading the electrical characteristics of NGB-TFT.

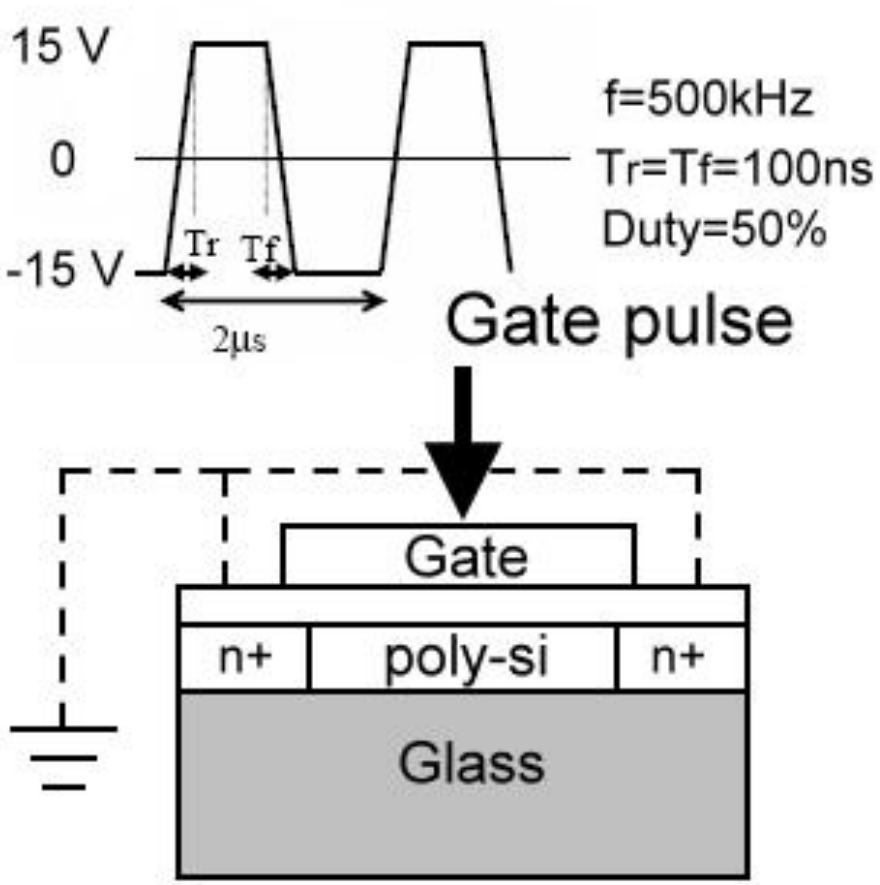


Fig. 5-1 The stress pulses were conducted on the gate electrode as the dynamic stress and source/drain were grounded. The rectangular pulse with amplifier of ±15V and frequency of 500kHz. Both the rising time (Tr) and falling time (Tf) were 100 ns.

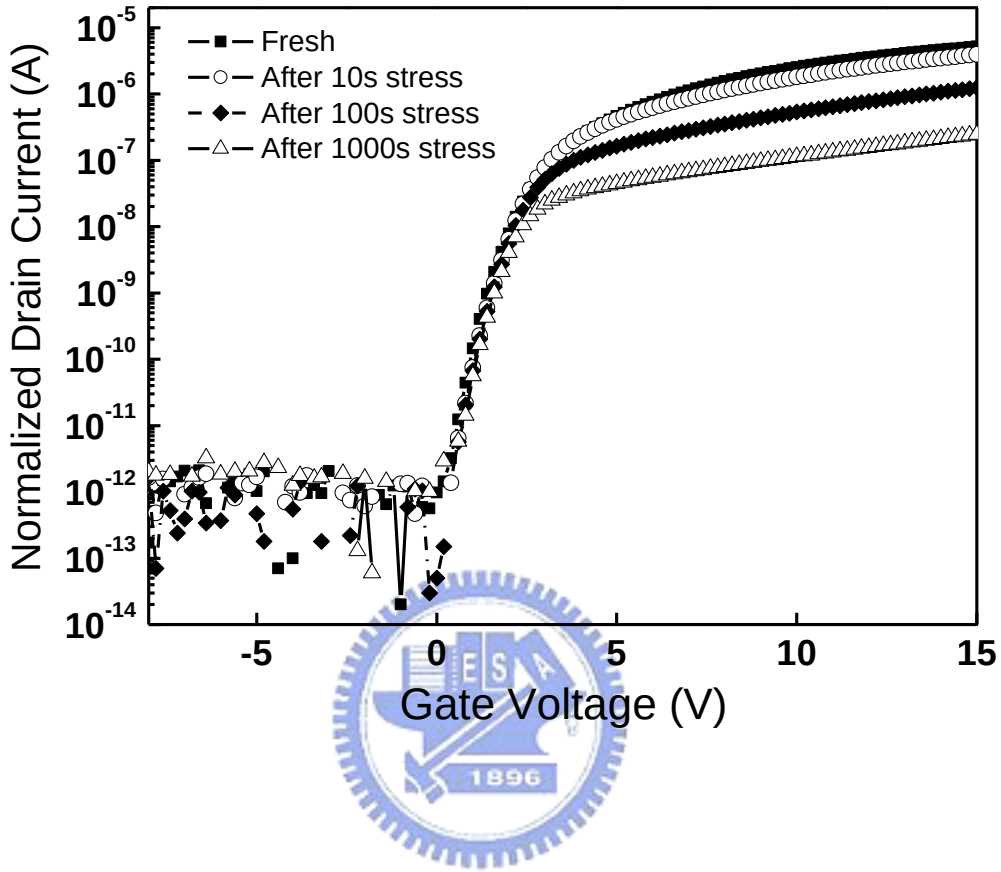


Fig. 5-2 The I_D-V_G relationships of n-channel poly-Si TFT (L=9μm) with the dynamic stress times for 10 to 1000 seconds.

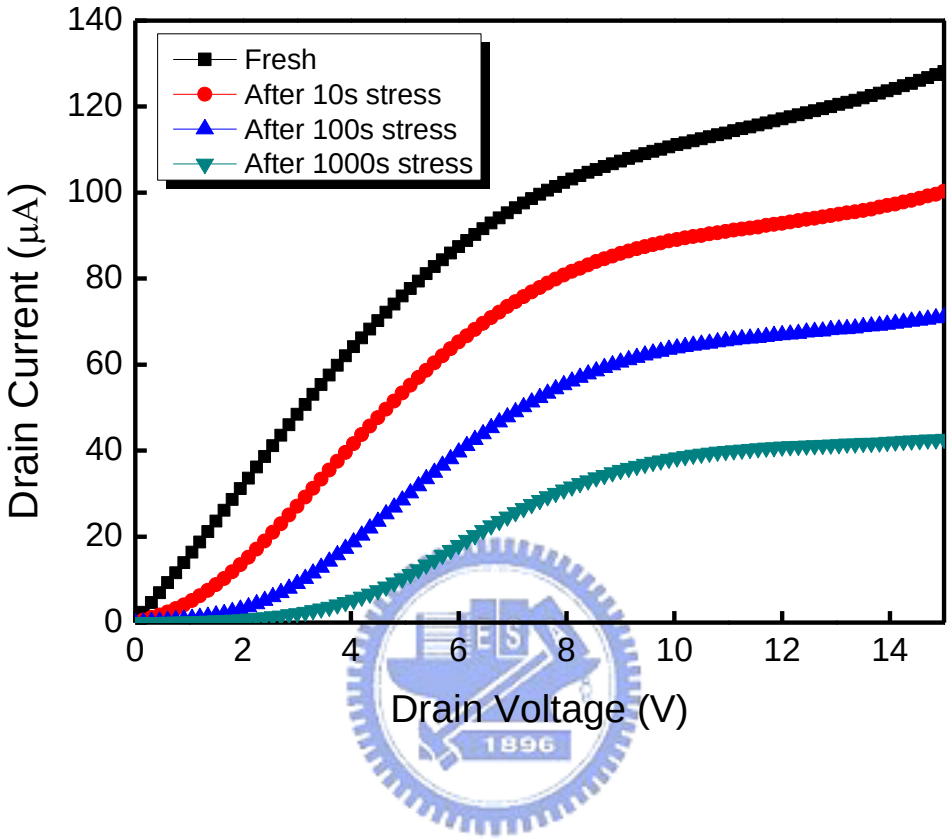


Fig. 5-3 The I_D-V_D characteristics of the TFT with the dynamic stress times.

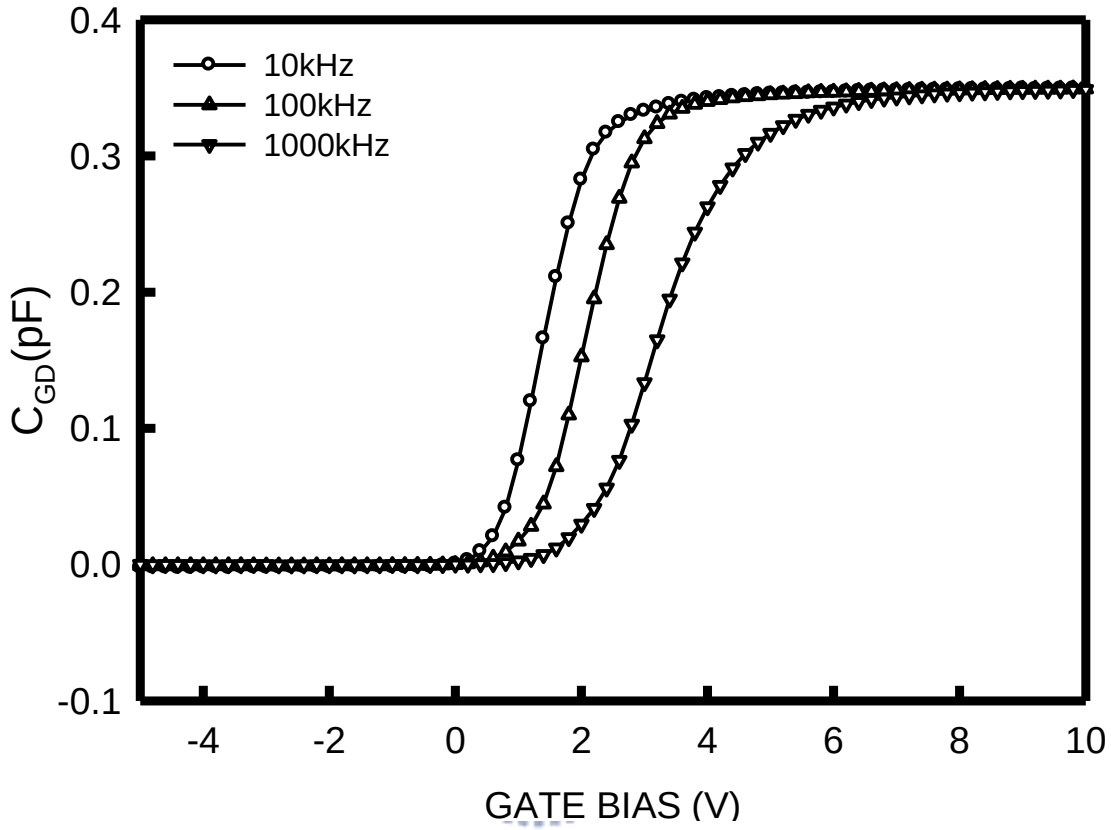
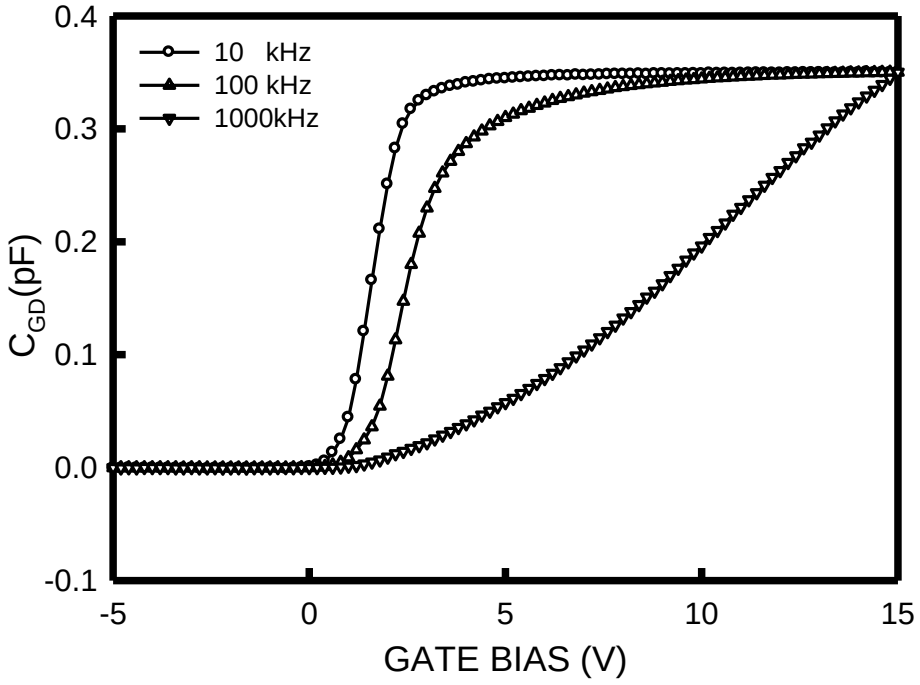
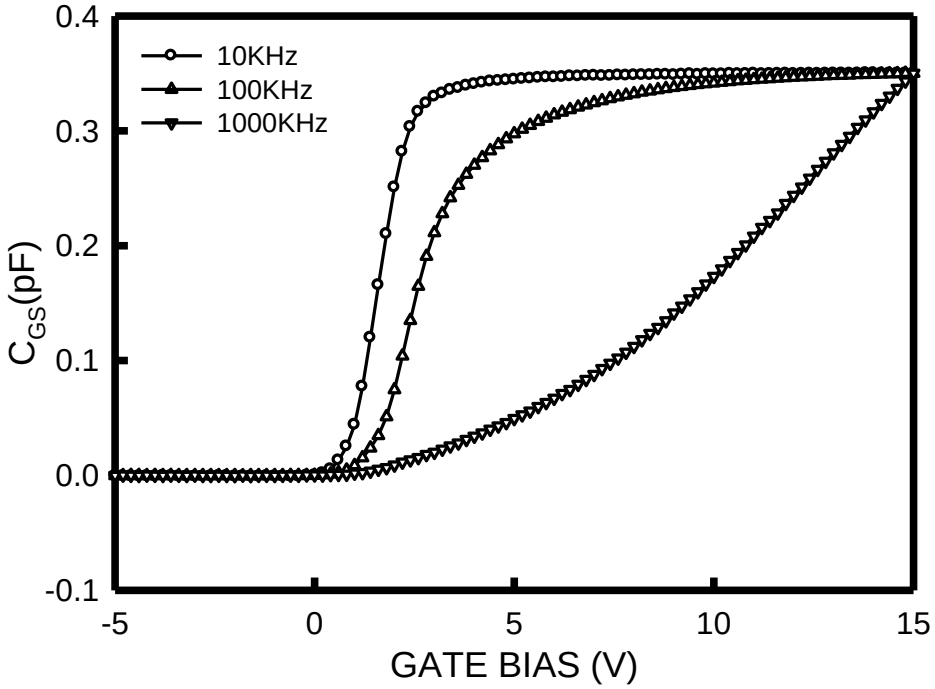


Fig. 5-4 The initial C_{GD} of n-channel poly-Si TFTs curves at the different measurement frequency

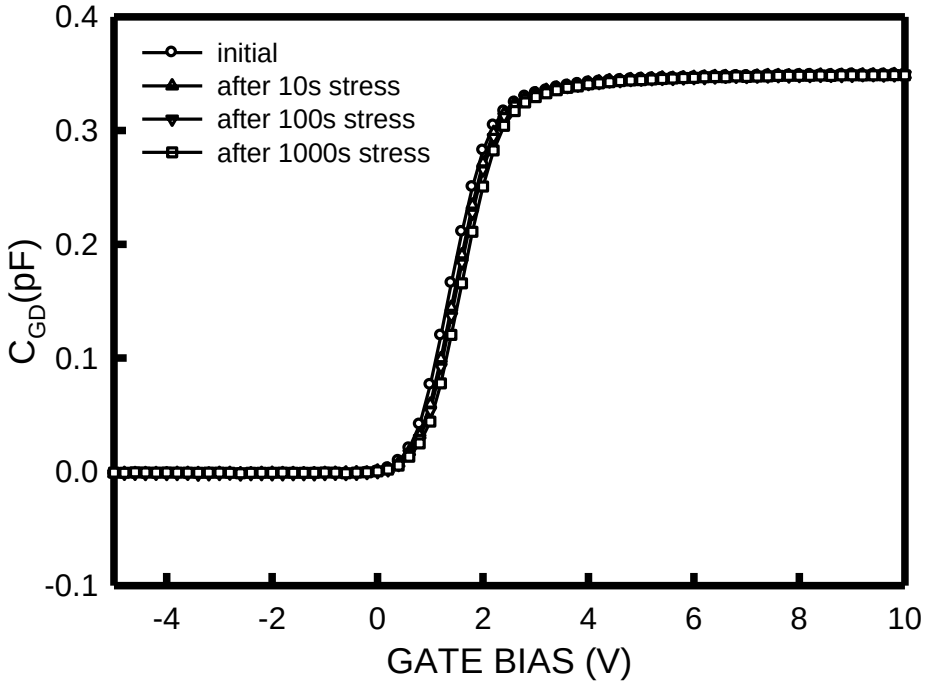


(a)

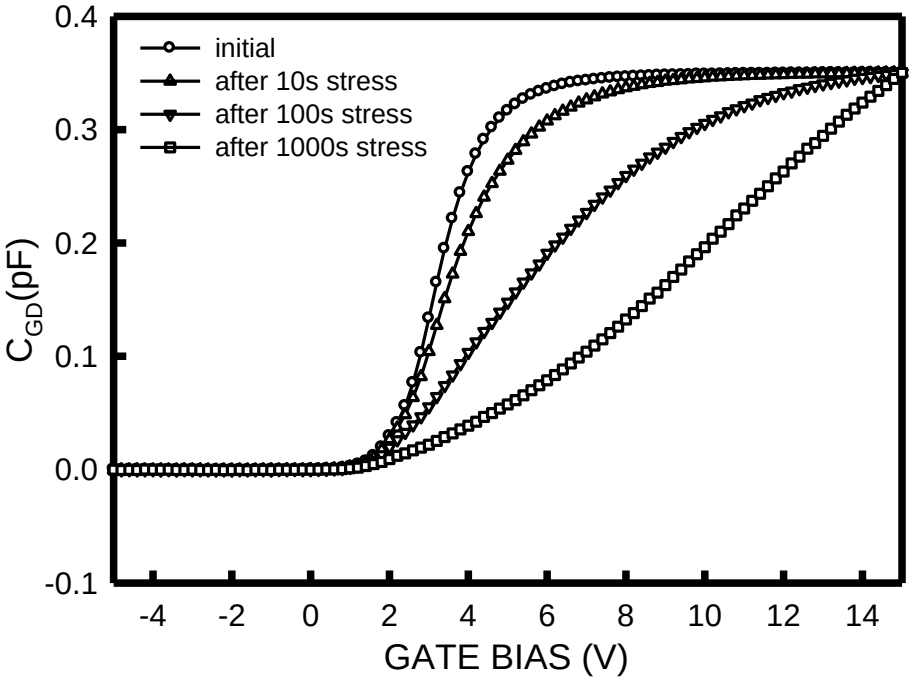


(b)

Fig. 5-5 C–V curves of an n-channel TFT after dynamic stress for 1000s. (a) Gate-to-drain capacitance. (b) Gate-to-source capacitance.



(a)



(b)

Fig. 5-6 C–V curves of an n-channel TFT after dynamic stress. (a) Gate-to-drain capacitance at 10 kHz. (b) Gate-to-drain capacitance at 1MHz.

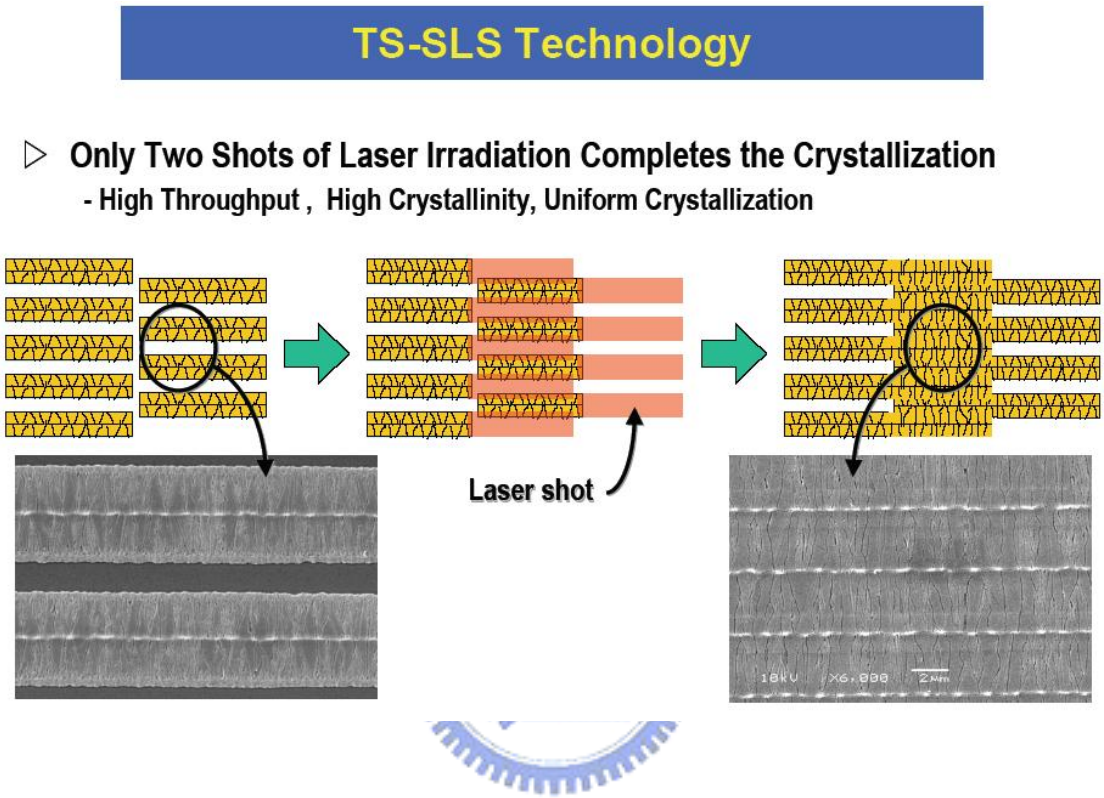
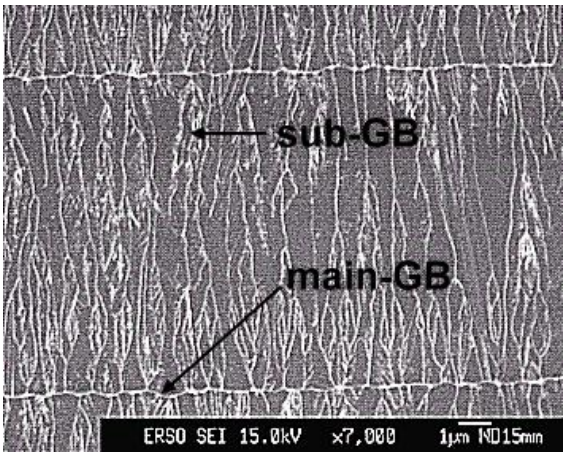
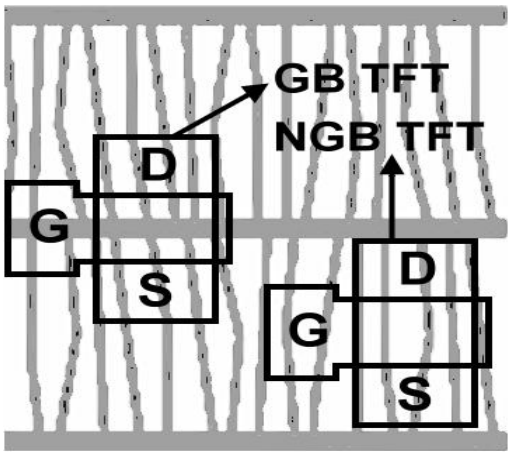


Fig. 5-7 The process flow of two shot SLS crystallization technology.



(a)



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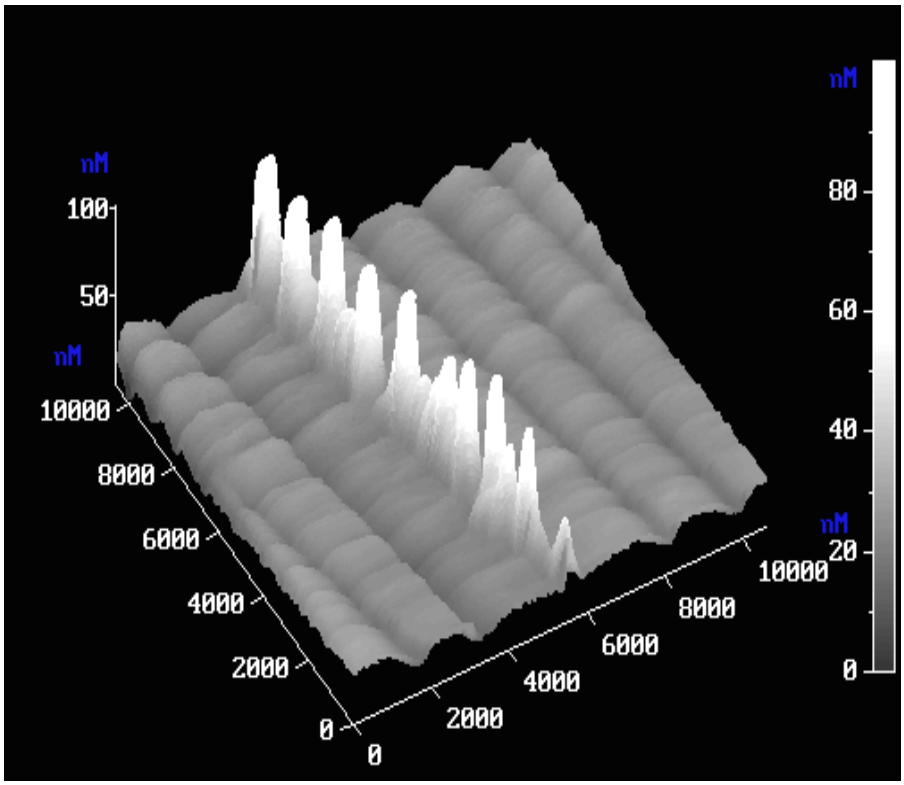


(c)

FIG. 5-8 (a) The top view of a high-resolution scanning electron microscopy (SEM) image of laser-crystallized laterally grown poly-Si film. (b) The orientation of main-GB and sub-GB is perpendicular and parallel to channel direction of the TFTs we utilized, respectively (c) The AFM image of laser-crystallized laterally grown poly-Si film.

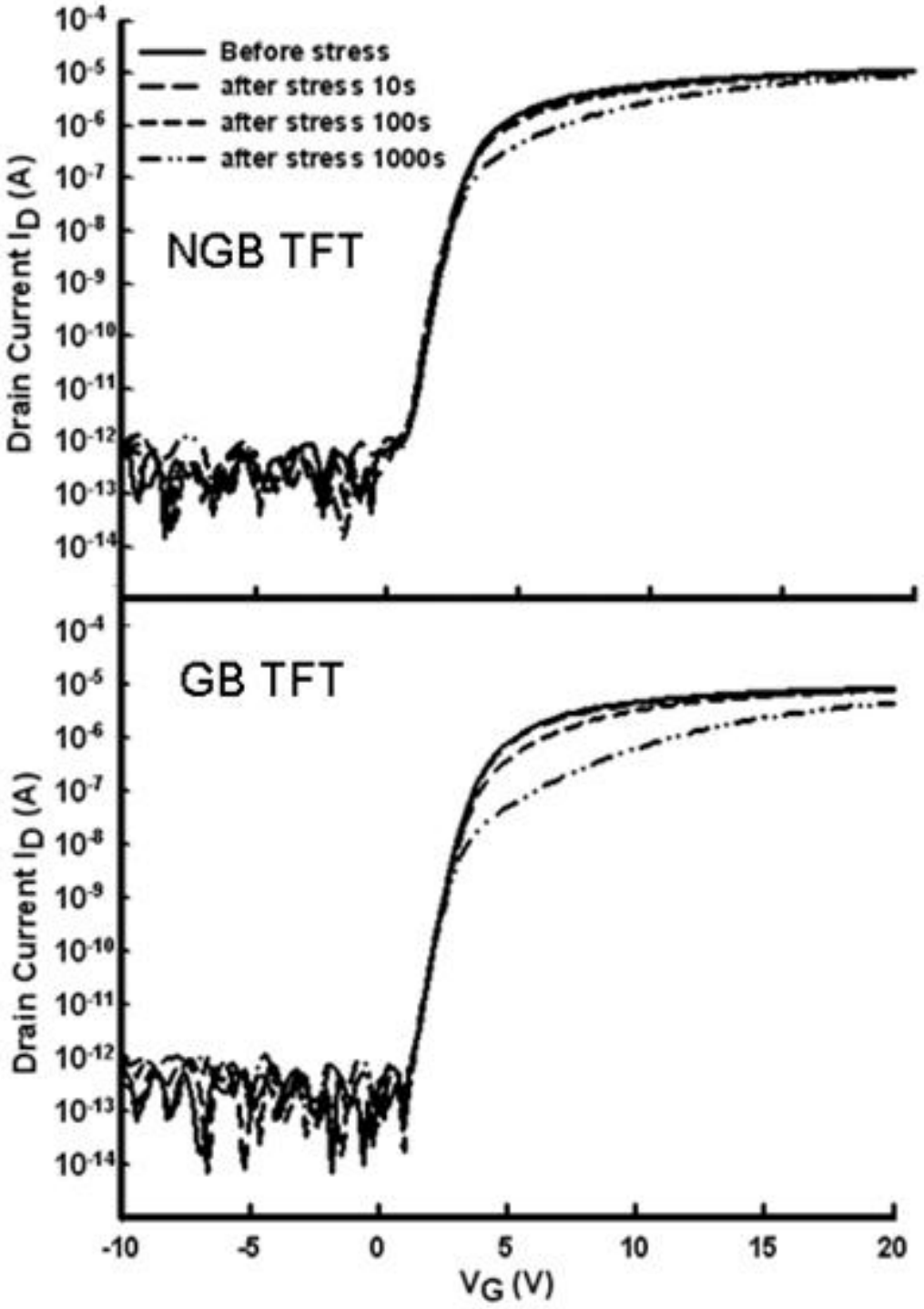


Fig. 5-9 The I_D-V_G curves of NGB and GB TFTs under the dynamic stress times for 10 to 1000 s. The degradation in GB TFTs is more severe.

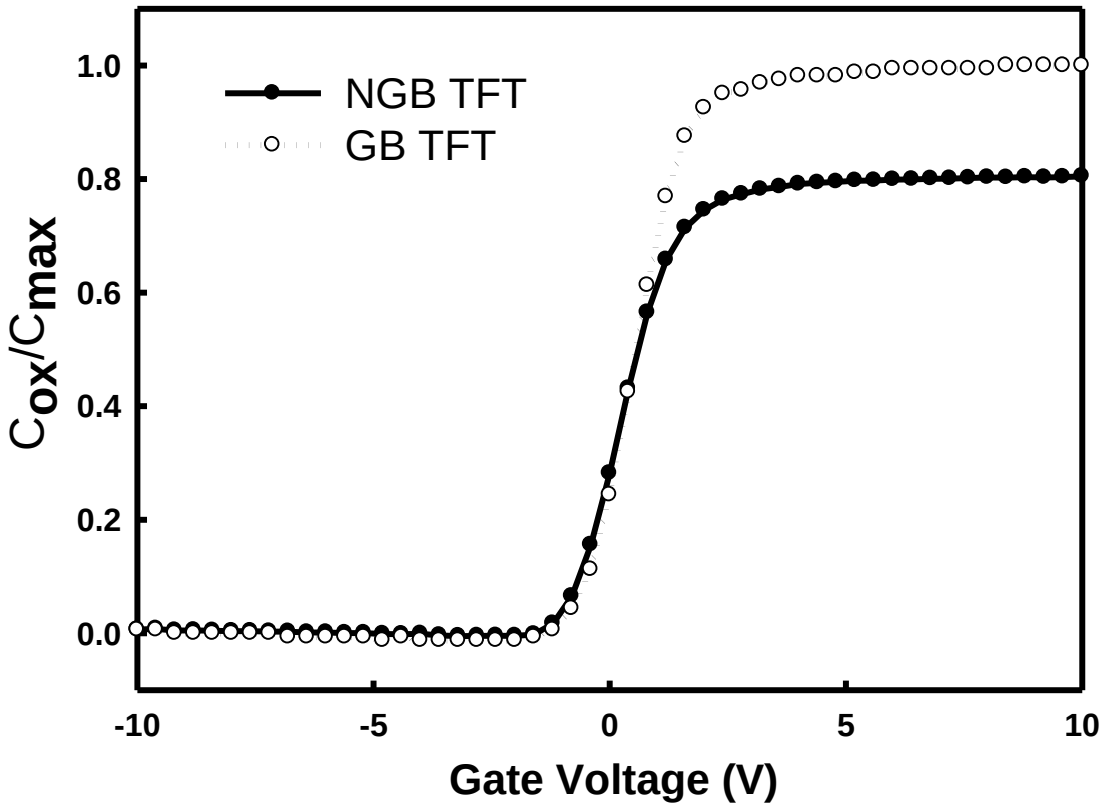


Fig. 5-10 The C–V curves of NGB and GB TFTs. It is shows that the gate oxide capacitance in GB TFTs is higher than the one in NGB TFTs.

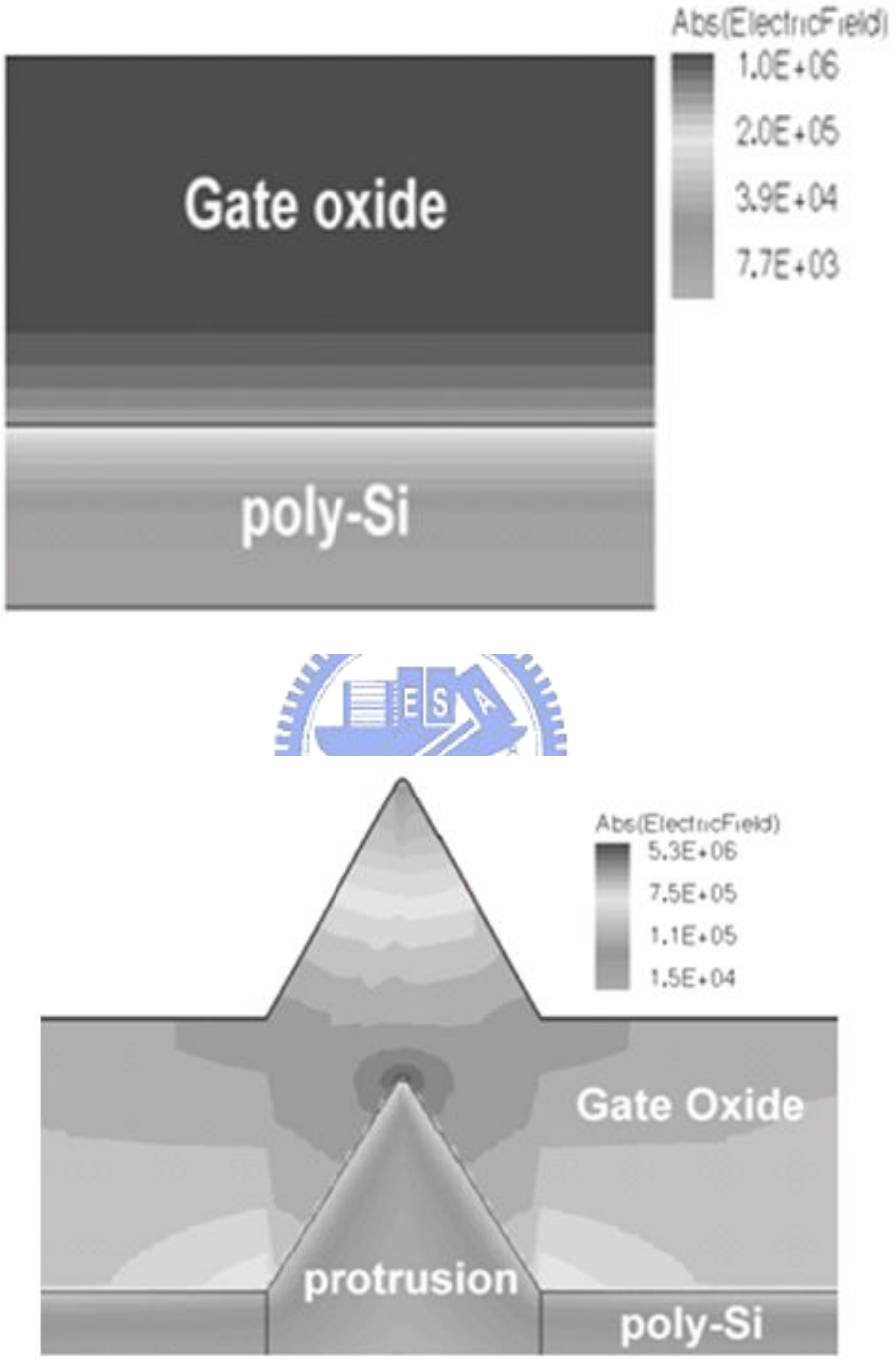


Fig. 5-11 The simulation result of the electric filed distribution in the protrusion region.

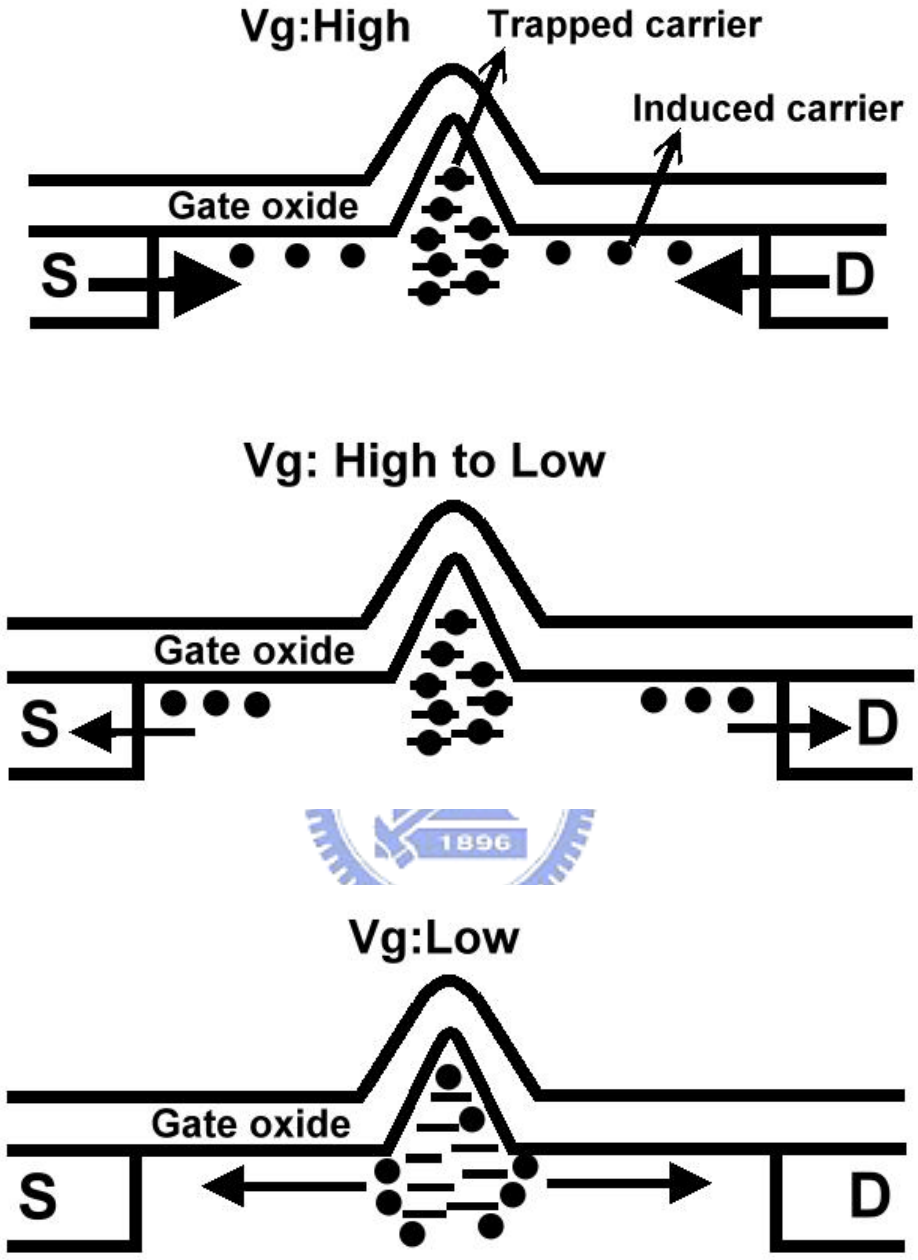


Fig. 5-12 The degradation model which considers the effect of protrusion grain boundaries as poly-Si TFT is operated under dynamic stress.

Chapter 6

Compensation Pixel Circuits for AMOLED Displays

6.1 General Background

Active-matrix organic light emitting diode (AMOLED) displays with polycrystalline silicon (poly-Si) thin film transistors (TFTs) and amorphous silicon TFTs have been widely researched and developed because of its superior characteristics in flat displays. These advantages include wide viewing angle, high brightness, and fast response time, compact and light weight [6.1-6.2]. However, it is difficult to implement an AMOLED panel with good image quality because of variations in the threshold voltage and in the mobility of poly-Si TFTs among pixels and the expensive maintenance of an ELA facility [6.3]. Several voltage modulation and current programming schemes have been devised to solve the non-uniformity problem [6.4-6.7]. The current programming methods can compensate both threshold voltage and mobility variation, these need very high addressing speed for high resolution displays. The voltage driving method using poly-Si TFTs formulated by Dawson et al. may effectively compensate for threshold voltage variations. Furthermore the driving current in AMOLED panels and the number of scan lines should be increased with the panel size and the brightness in the high resolution and large size displays. The intrinsic display loading effects of a voltage drop across the parasitic resistance of the supply power line also causes non-uniformity of brightness in voltage-driven AMOLED panels. The drop in the supply voltage on the panel (V_{DD} IR Drop) is a critical issue leading to image degradation and crosstalk [6.10]. The use

of AMOLED displays for large size applications is expected to have many advantages, so the driving method and pixel structure should be applicable to large size panels. However, most compensating pixel circuits with simple structures only solve one of the aforementioned problems [6.11-6.12]. Some complicated designs have very uniform output current among pixels but these may reduce the aperture ratio or require additional peripheral driving circuits [6.13-6.14].

Recently, hydrogenated amorphous silicon (a-Si:H) TFTs are used as pixel element for large size and low cost panels in AMOLED display because of its good uniformity and simple fabrication process [6.15]. However, the threshold voltage shift of a-Si:H TFTs over time under operation is a critical issue to degrade the image quality on AMOLED panels [6.16]. Several voltage modulation and current programming schemes have been devised to solve the degradation problem [6.17-6.18]. The current programming methods exhibit uniform output current among pixels; however, it requires a longer pixel charging time compared to a voltage modulation method. The voltage driving method formulated by Goh et al. may effectively compensate for threshold voltage shifts of a-S:H TFT [6.19]. However, since OLED is placed on the source node of a-Si:H TFT in the conventional 2-TFT pixel circuit and I_{OLED} is determined by V_{GS} of the driving TFT, the threshold voltage shift in OLED raise the source voltage of the driving TFT to decrease the driving current [6.20]. The degradation of OLED causes the uneven brightness of voltage-driven AMOLED panels as well. The issues above mentioned make the luminance different from pixel to pixel and degrades the image brightness. Since the large-size AMOLED displays with low cost panels are expected to have many advantages, the driving method and pixel circuit should be applicable to large size panels. A compensation pixel circuit, developed by Lee *et al.*, supplies highly stable OLED current, compensating for the

threshold-voltage degradation of both a-Si:H TFTs and OLEDs [6.21]. Notably, however, the driving current is slightly reduced by the degradation of the switch TFT that is used to connect the power supply line to the driving TFT. Moreover, the pixel circuit that was proposed by Lee *et al*. requires six TFTs and four operating periods for each frame.

This study develops a new driving method with source-follower type connection and the bootstrap using poly-Si TFT, to improve the brightness variation due to the variations in the threshold voltage of the driving TFT and the drop in the supply voltage. The simulation results demonstrate that the variation in the current driving OLED among pixels can be significantly reduced. In addition, a new driving method with simple a-Si:H TFTs pixel design capable of eliminating simultaneously the shift of threshold voltage in the driving TFT and OLED used in pixel element is proposed in this work. The simulation results demonstrate that the degradation in the current driving OLED among pixels can be significantly reduced.

6.2 Proposed Poly-Si TFT Pixel Structure and Driving Method

Figure 6.1 shows the distribution of the threshold voltage among 600 p-channel poly-Si TFTs. The maximum shift of the threshold voltage is about 0.2V, at a mean threshold voltage of -2.41V. The electrical characteristics of 600 p-channel poly-Si TFTs had been measured and the threshold voltage of these TFTs were extracted at current density of 10 nA with normalized channel width (W)/channel length (L) ratio. This result confirms the necessity of threshold voltage variation compensation for brightness uniformity of OLED pixels and gray level expression.

In the conventional architecture, the OLED is driven by the current generated by

the potential difference between the gate and the source, V_{GS}, of the driving TFT (DTFT), given by $|V_{DATA}-V_{DD}|$. However, the driving current that passes through the supply power electrode causes a voltage drop due to the parasitic resistance of the power line, as shown in Fig. 6.2. Even if the pixel circuit can compensate for the variation of the threshold voltage in the DTFT, the V_{GS} in each DTFT still varies from pixel to pixel along the electrode, generating various driving currents. This phenomenon causes the brightness to be non-uniform from the top to the bottom of the panel.

Figures 6.3 shows the proposed pixel circuit based on poly-Si TFTs and timing scheme of signal line. The design includes one driving TFT (DTFT), four switching TFT (T1, T2, T3 and T4) and one capacitor (C_{ST}). V_{DATA} represents a voltage data signal line and V_{DD} refers to a constant voltage source line. The operation of the proposed circuit is divided into three stages shown in Fig. 6.4. During stage (1), source-follower type connection, [n]Scan is set at the high level and [n]EM is set at the low level, respectively, to turn on T1, T2 and T3, so that the node voltage of DTFT connected to the right side of C_{ST} is increased to V_{DD}, and this node becomes the source of DTFT. Therefore, the pixel circuit is a p-type source follower. The next stage is the V_{TH} detecting period. Only [n]EM is set high to turn off T1 as scan[n] remains high. The source voltage of DTFT is discharged until it is turned off. This node voltage settles from V_{DD} to $V_{DATA}+V_{TH}$, where V_{TH} is the threshold voltage of DTFT. Accordingly, the threshold voltage of DTFT and the data signal are stored in the right side of CST. The left side of CST is set to ground during stages (1) and (2) so that the drop voltage of CST is $V_{DATA}+V_{TH}$. After the pixel scanning period, the third stage, the display period, is implemented. During stage (3), [n]scan and [n]EM are set to low to turn off T2&T3 but turn on T4 &T1 so that the gate of DTFT can be

connected to the left side of C_{ST}; the source voltage of DTFT is charged up to V_{DD} from $V_{DATA}+V_{TH}$. Immediately, the gate voltage of DTFT should be boosted to $V_{DD}-V_{DATA}-V_{TH}$ by the conservation of charge in the capacitor as bootstrap is performed. Accordingly, DTFT starts to generate current (I_{OLED}), driving the OLED. C_{ST} sustains the gate voltage of DTFT, V_{DD} -V_{DATA}-V_{TH}, for the period of a frame. I_{OLED} is also the saturation current of DTFT. This work focused on eliminating the brightness non-uniformity caused by the variation of the threshold voltage and the drop in supply voltage. The first order current equation is directly affected by V_{TH} and V_{DD}. And the minimum design rule for the channel length of TFT devices is 5 μm, so that the second order effect is not thereby considered in the proposed analysis. As a result, in this paper the first order equation is used to evaluate if the proposed circuit can exhibit high immunity to both voltage variation in poly-Si TFTs and the drop in the supply voltage.

$$\mathbf{I_{OLED}} = \mathbf{K}[\mathbf{V_{GS}} - \mathbf{V_{TH}}]^2$$

$$= \mathbf{K}[(\mathbf{V_{DD}} - \mathbf{V_{DATA}} - \mathbf{V_{TH}}) - \mathbf{V_{DD}} - \mathbf{V_{TH}}]^2 = \mathbf{K}[\mathbf{V_{DATA}}]^2$$

Therefore, I_{OLED} is independent of the threshold voltage of DTFT and the supply voltage, and is affected only by data voltage. The threshold voltage variations and the drop in supply voltage can be both compensated effectively and uniform brightness image performance can be achieved.

6.3 Simulation results of Proposed Poly-Si TFT Pixel Design

The HSPICE software with the RPI poly-silicon TFT model (Level=62) were used to verify the proposed circuit. The aspect ratio, mobility and threshold voltage of DTFT were 3.3/5, 80 cm2/V•s and -2V. The C_{ST} was set to 0.4 pF and V_{DD} were set as

9V. The high and low level of the signals ([n]Scan and [n]EM) were set as 10V to -10V, respectively. The initial data voltage modulated such that the I_{OLED} in the following cases was approximately 1 μA as luminance and resolution were designed to be 300 Cd/m^2 and 133 PPI. In this work, the variation of the threshold voltage of DTFT is set as 0.3V to evaluate the validation of this design in the worst case.

Figure 6.5 plots simulation result for the conventional 2-TFTs & 1-capacitor pixel structure, when the threshold voltage of the driving TFT was set to -1.7V, -2V and -2.3V. The I_{OLED} of the conventional 2-TFTs & 1 capacitor pixel structure is fluctuated with the variation of the threshold voltage of DTFT very seriously. The variation range of I_{OLED} is about 1.3~0.55 uA due to the variation of threshold voltage in the DTFT caused by process variation, non-uniform image quality over the display will become a critical issue.

Figure 6.6 verifies that the modulated data voltage and the threshold voltage of DTFT are stored in the right side of C_{ST} as the threshold voltages are varied. The difference of the stored voltage in the capacitor almost equals the variation value in threshold voltage, namely 0.3V. Figure 6.7(a) plots the simulation result in I_{OLED} of the proposed design, when the threshold of the driving TFT was set to -1.7V, -2V and -2.3V. The simulation results indicate that the variation of I_{OLED} in the proposed pixel is clearly reduced using the adoption of the new threshold voltage compensation method. In a display period, the variation of I_{OLED} in the proposed design is very small, being between around 1.01 and 0.99 μA. Therefore the strong immunity to the variation of the threshold voltage in the DTFT in the proposed pixel structure is demonstrated. Figure 6.7(b) shows that simulated degradation of the supply voltage on the panel is 0.5 V. According to Fig. 6.7(b), the deviation of I_{OLED} in the presented pixel structure is less than 2.5%, confirming the effectiveness of the prevention

against the degradation of the supply voltage. The conventional 5T pixel circuit proposed by N. Komiya *et al.* is considered to compare the proposed one [6.22]. From the simulation result, the I_{OLED} degradation is 68.4% in the same simulation condition.

Figure 6.8 shows the comparison of the I_{OLED} degradation in the conventional pixel structure (2T1C) with that in the proposed structure (5T1C), which is caused by the drop in the supply voltage as the number of scan lines increase (240, 480, 600, 768) [6.23]. The y-axis shows the non-uniformity of output current and the x-axis indicates the distance from the supply voltage point to each pixel by the number of scan lines. As increasing the number of scan lines for large size or high resolution AMOLED displays, the resistance of the power line leading to the larger supply voltage drop in the conventional 2T1C pixel design. In contrast, in the proposed 5T1C pixel design, the non-uniformity of the output current remains almost constant while the number of scan lines increases, and the maximum degradation of I_{OLED} is just approximately 3.1%. Therefore, the proposed pixel structure is a promising candidate for use in large size and high resolution AMOLED displays.

Figure 6.9 shows the error rate of I_{OLED} in the proposed pixel circuit due to the threshold voltage variation. The output current errors of conventional 2T1C pixel circuit are all above 20% when input data voltage ranges 0.5–5 V, which is below 2.5% in proposed pixel circuit.

6.4 Proposed a-Si:H TFT Pixel Structure and Driving Method

Figure 6.10 presents the proposed circuit and its timing scheme of signal lines. The circuit includes one driving TFT (DTFT), four switching TFT (T1, T2, T3 and T4)

and one capacitor (C_{ST}). The control lines include two scan lines (sacn and EM) and two column lines (V_{DD} and V_{DATA}). V_{DD} and V_{REF} refer to a constant voltage source line and a reference voltage line, respectively. V_{DATA} is a voltage data signal line. The operation of the proposed circuit is divided into two periods in one frame operation, as shown in Fig. 6.11. During period (1), the threshold voltage of DTFT and OLED are detected. Scan is set at the high level to turn on T1, T2, so that the gate voltage of DTFT is V_{DATA}, and the voltage in the left side of C_{ST} is V_{REF}. Therefore, the circuit is a source-follower type connection, including DTFT and OLED. Assume that the voltage across the OLED is V_{OLED} and the threshold voltage of DTFT is V_{TH}, respectively. The voltage in the right side of C_{ST} would be charged up to V_{DATA}-V_{TH}-V_{OLED}. After the compensation period, the second stage is the display period. In stage (2), scan is set to low to turn off T1&T2 but EM is set to high, so that the right side of C_{ST} is ground. Immediately, the gate voltage of DTFT should be boosted to V_{REF}-V_{DATA}-V_{TH}-V_{OLED} by the conservation of charge in the capacitor as bootstrapping is performed. In the proposed architecture, the V_{TH} of DTFT and V_{OLED} are detected and stored in C_{ST} during one scan period. The gate voltage of DTFT, V_{DATA}-V_{TH}-V_{OLED}, is maintained in C_{ST} until next frame time. Accordingly, DTFT starts to generate current (I_{OLED}) to drive the OLED. I_{OLED} is also the saturation current of DTFT.

$$\begin{aligned} \mathbf{I_{OLED}} &= \mathbf{K[V_{GS} - V_{TH}]^2} \\ &= \mathbf{K[(V_{REF} - V_{DATA} + V_{TH} + V_{OLED}) - V_{OLED} — V_{TH}]^2} \\ &= \mathbf{K[V_{REF} - V_{DATA}]^2} \end{aligned}$$

Therefore, I_{OLED} is independent of the threshold voltage of DTFT and OLED, and is controlled only by input data voltage and the reference voltage

6.5 Simulation results of Proposed a-Si:H TFT Pixel Design

The proposed circuit simulation is performed by the HSPICE software with the RPI amorphous-silicon TFT model (Level=61) to verify the compensating capability. The aspect ratio of DTFT was 80/4. The initial threshold voltage of DTFT and C_{ST} were set to 2V and 0.5 pF. V_{DD} and the high level of the signals (Scan and EM) were set as 15V and 25V, respectively. The initial supply voltage modulated such that the IOLED in the following cases was approximately 1 μA as luminance and resolution were designed to be 300 Cd/m^2 and 133 PPI.

Figure 6.12 plots the transition simulation result of the nodes in the proposed pixel circuit. In the compensation period, the gate voltage is V_{DATA} to turn on DTFT so that the right side of C_{ST} is charged until DTFT and OLED are turn off. Therefore, the voltage in the right side of C_{ST} eventually becomes V_{DATA}-V_{TH}-V_{OLED}. The voltage stored in the C_{ST} is V_{REF}-V_{DATA}-V_{TH}-V_{OLED}. During display period, the gate node of DTFT is connected to the left side of C_{ST} and the gate voltage becomes V_{REF}-V_{DATA}-V_{TH}-V_{OLED} as the left side of C_{ST} is ground. Thus, the proposed pixel circuit compensates threshold voltage degradation of TFTs and OLED in one frame time. Figure 6.13(a) and 6.13(b) plots the simulation result of the output current in the conventional 2-TFTs & 1 capacitor (2T1C) pixel structure and the proposed pixel structure, when the threshold shift of the DTFT was set to 1.2V. From the simulation result, the I_{OLED} of the conventional 2-TFTs & 1 capacitor (2T1C) pixel structure is fluctuated significantly due to the shift of the threshold voltage of DTFT. The variation range of I_{OLED} in 2T1C pixel is about 1.04 to 0.68 μA. The result confirms the necessity of compensation for the threshold voltage shift, gaining uniform brightness of OLED pixels and superior gray level expression. The simulation results

indicate that the variation of I_{OLED} in the proposed pixel is clearly reduced using the adoption of the new threshold voltage compensation method. In a display period, the degradation of I_{OLED} in the proposed design is very small, being around 28 nA. Therefore the strong immunity to the shift of the threshold voltage in the proposed pixel structure is verified.

Fig 6.14(a) and Fig. 6.14(b) shows the simulation results for the proposed pixel structure in which the shift of the OLED threshold voltage is 0.7V. The I_{OLED} is degraded about 30% for the 2T1C pixel. Since the brightness of OLED is controlled by the current I_{OLED}, the shift of threshold voltage in OLED would make the panel brightness decrease. According to Fig. 6.14(b), the deviation of I_{OLED} in the presented pixel structure is approximately 58nA, confirming the effectiveness of the prevention against the degradation voltage across OLED.

In order to investigate the V_{TH} compensation capability of proposed pixel design, the simulation of driving current with increasing threshold voltage shift is performed in this chapter. The shift in V_{TH} of DTFT is increased from 1V to 5V in our simulation condition. It is observed that the driving current of conventional 2T1C pixel is degraded very seriously, as shown in Fig. 6.15. For the initial current is about 1uA, the driving current of conventional pixel only remains 0.2uA as V_{TH} shift is 5V. The variation of driving current exceeds 80% as the increase of V_{TH} is settles to 5V. By contrast, the proposed pixel could provide 900nA current when threshold shift is set 5V, showing that the proposed pixel structure has great eliminating performance against the degradation of the supply voltage.

The a-Si:H TFTs with inverted-staggered structures were fabricated and the shift in threshold voltage under dc stress was measured to evaluate the real performance of the proposed pixel circuit. Figure 6.16 plots the threshold voltage of a-Si:H TFT with

increasing gate bias stress time when the source and drain were grounded. The shift in the threshold voltage versus stress time is given by the following equation [6.16]. The initial value of threshold voltage, V_{TO}, is about 2.53V.

$$\Delta V_{TH} = A(V_{ST} - V_{TO})t^{\beta}$$

The values of the parameters A and β were 0.006 and 0.25, respectively, as determined from the straight lines fitted in Fig. 6.16 Since the linear stress causes greater shift than a saturation stress, the extracted values of parameters A and β were used to validate the worst-case design [6.24]. A threshold voltage degradation in OLED of 0.2mV/h is considered with the degradation of a-Si:H TFT to evaluate the compensatory effectiveness of the proposed design [6.20]. Figure 6.17 plots the simulated lifetime of 2T1C and the proposed pixel circuit. Considering the degradation of both a-Si:H TFT and OLED with time in the simulation work, it is found that the proposed circuit suffers from only 10% current degradation after 5000 hours. Simulation results based on the measurements data demonstrate that the proposed pixel circuit effectively compensates for the threshold-voltage shift of TFT and OLED.

6.6 Conclusion

A new voltage-modulation pixel circuit is developed for application to large size and high-resolution AMOLED displays. The non-uniformity of the output current is improved substantially using the proposed compensation operation. The average deviation of the TFT driving current is about 50 nA as the threshold voltage is varied by 0.3 V and the non-uniformity of the I_{OLED} with increasing number of the scan lines in the proposed pixel structure is less than 3.1%. Also the error rate of the I_{OLED} with

the threshold voltage variation is below 2.5%.The simulation results demonstrate successfully that the proposed circuit has high immunity to both the voltage variation in poly-Si TFTs and the drop in the supply voltage. Therefore, the proposed pixel structure is a promising candidate for the large size and high resolution AMOLED displays.

A new voltage-modulation compensation method using a source-follower type connection is developed to simplify the compensation cycles. The proposed compensation operation markedly reduces the non-uniformity of the output current. The mean deviation of the TFT driving current is about 28nA at a threshold voltage shift of 2V. Furthermore, the shift of the I_{OLED} is 50nA, and is associated with a shift in the OLED threshold voltage of 0.7V. Based on the measured results, the simulated current degradation in the proposed pixel is approximately 10% after 5000 hours. The simulation results show that the proposed circuit has high immunity to both the threshold voltage degradation both in a-Si:H TFTs and the OLED that is used in AMOLED display .

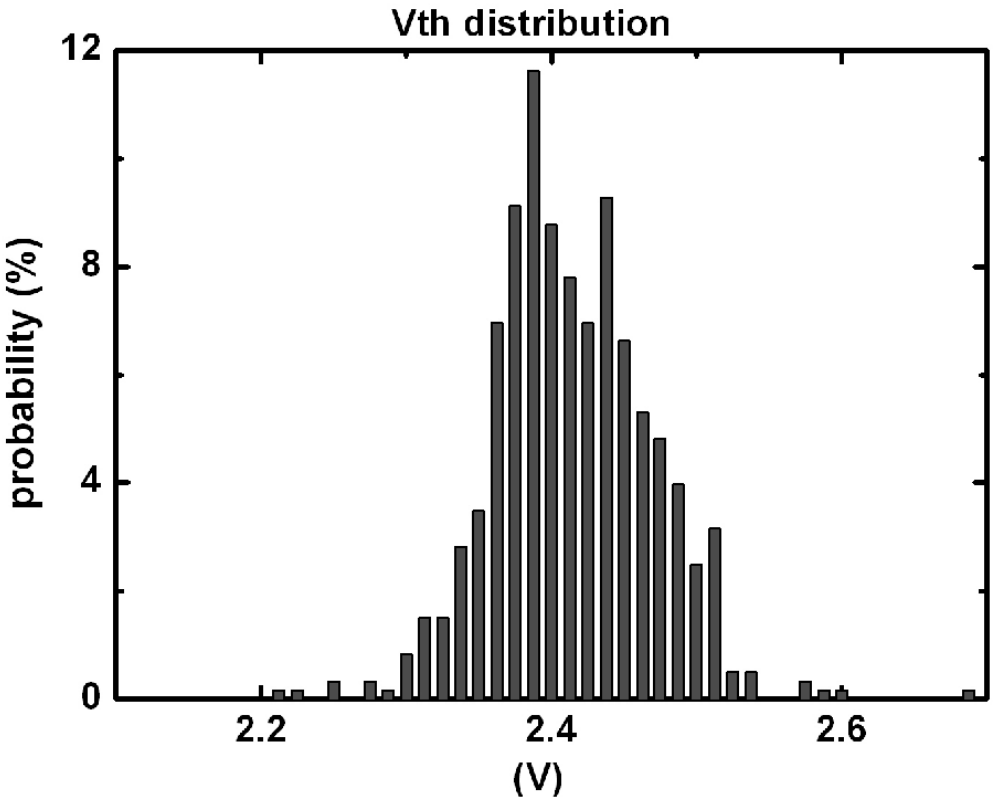


Fig. 6-1 The distribution of the threshold voltage among 600 TFTs and the maximum shift of the threshold voltage are about 0.2V.

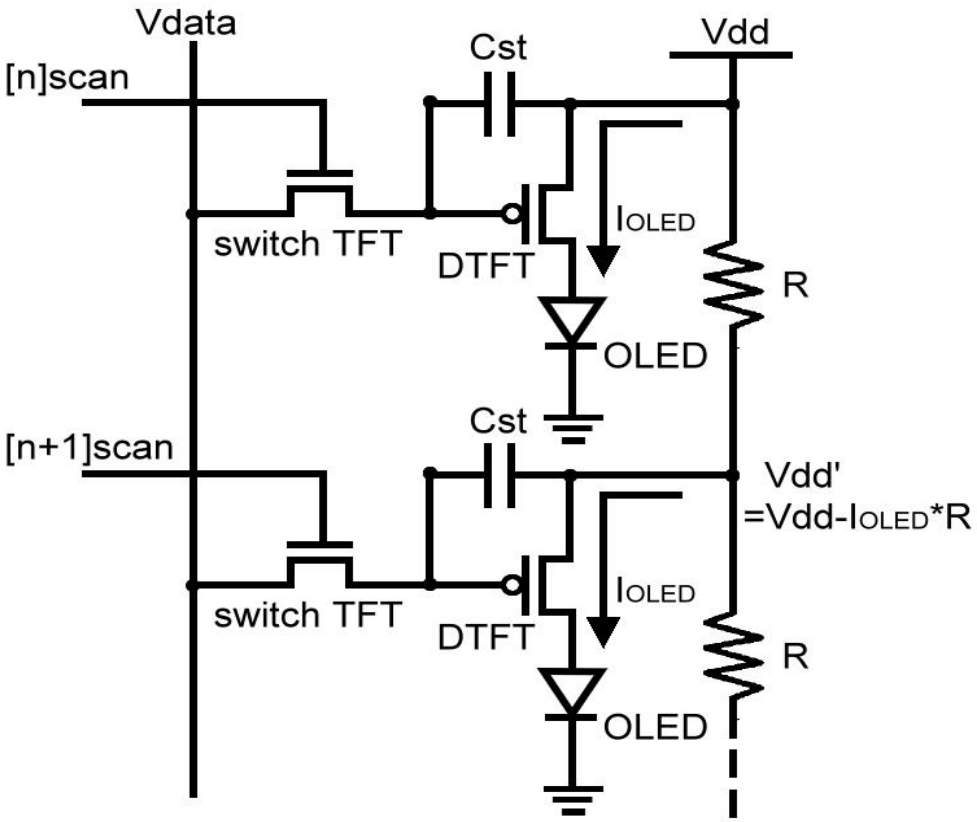


Fig. 6-2 Circuit scheme of conventional pixel circuit (2T1C) and the voltage drop caused by the intrinsic parasitic resistance (R) at V_{DD} supply power line.

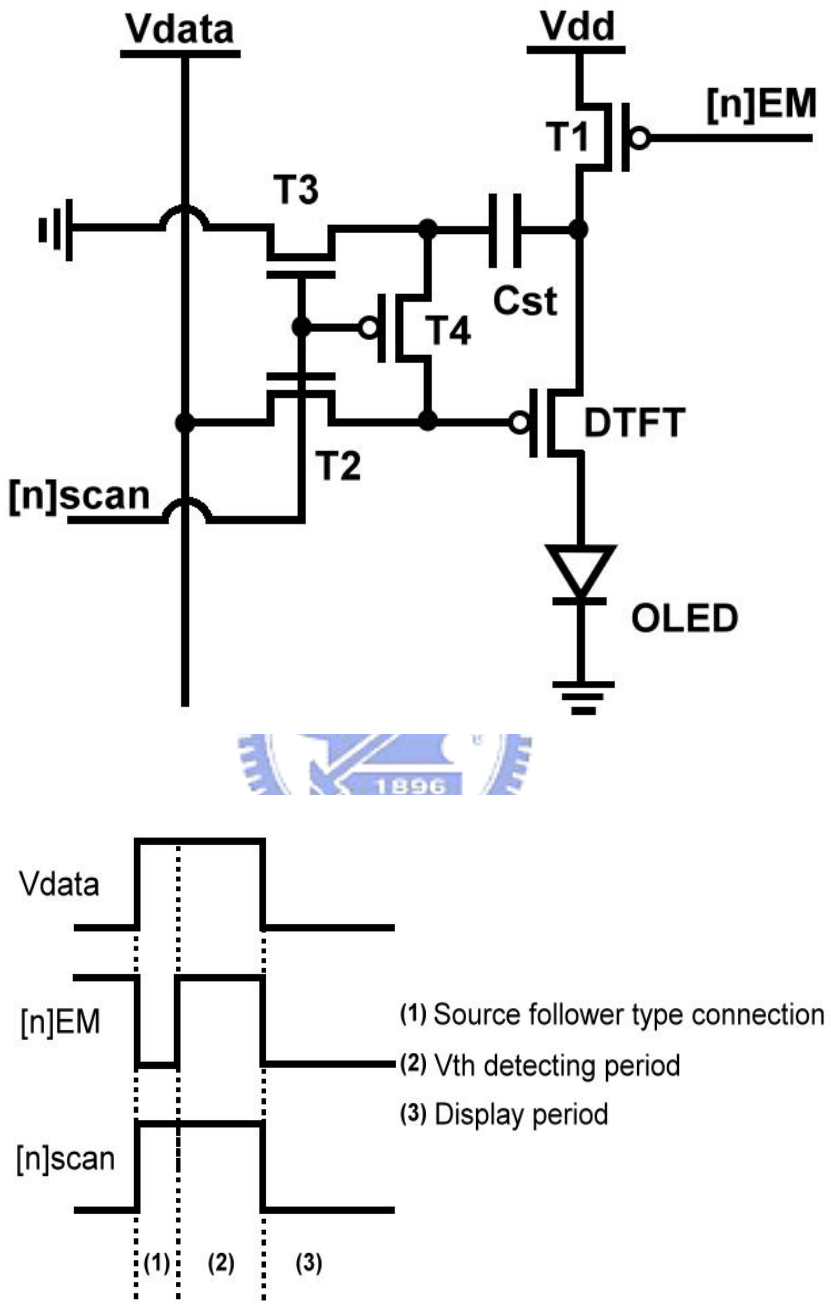


Fig. 6-3 The proposed pixel design and timing scheme of the signal line.

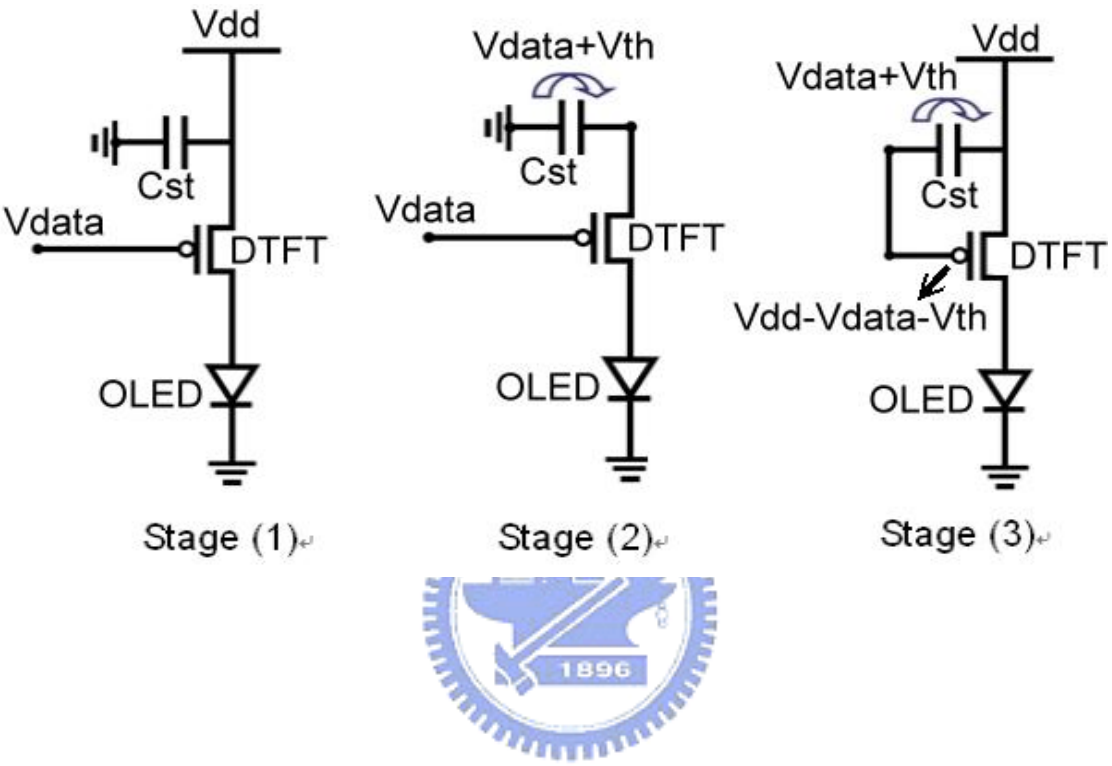


Fig. 6-4 The equivalent circuit at each stage in operation.

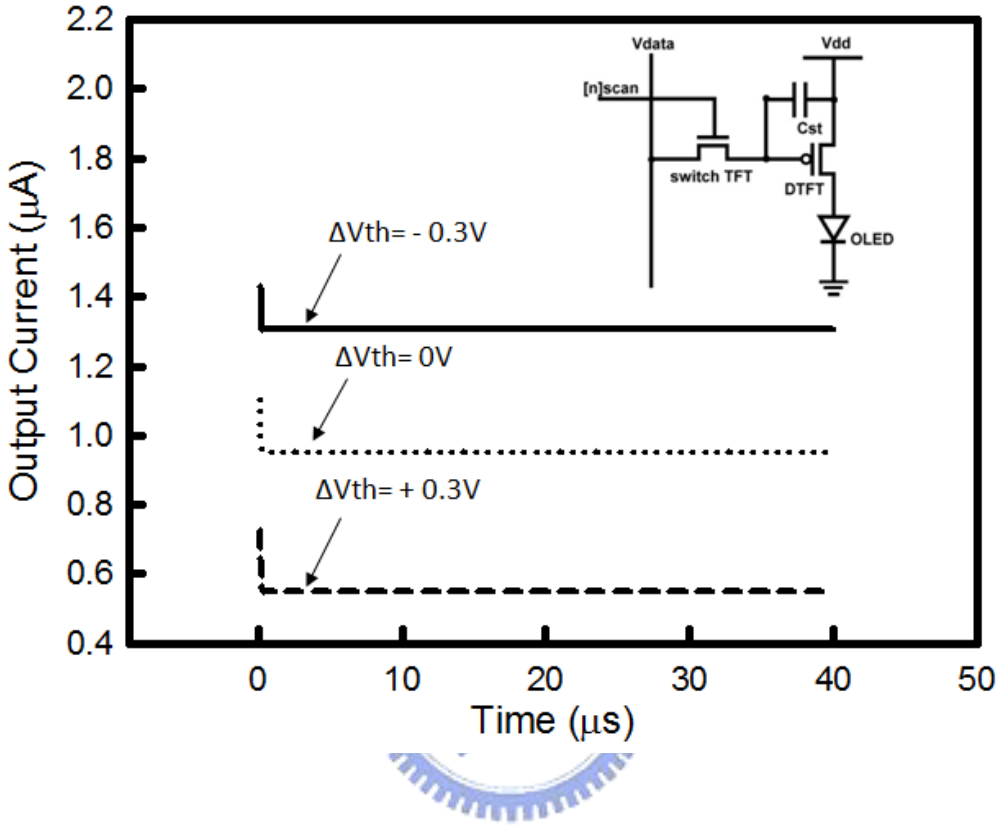


Fig. 6-5 The transient simulation results for the conventional 2T1C pixel structure with the variation in the threshold voltage of DTFT

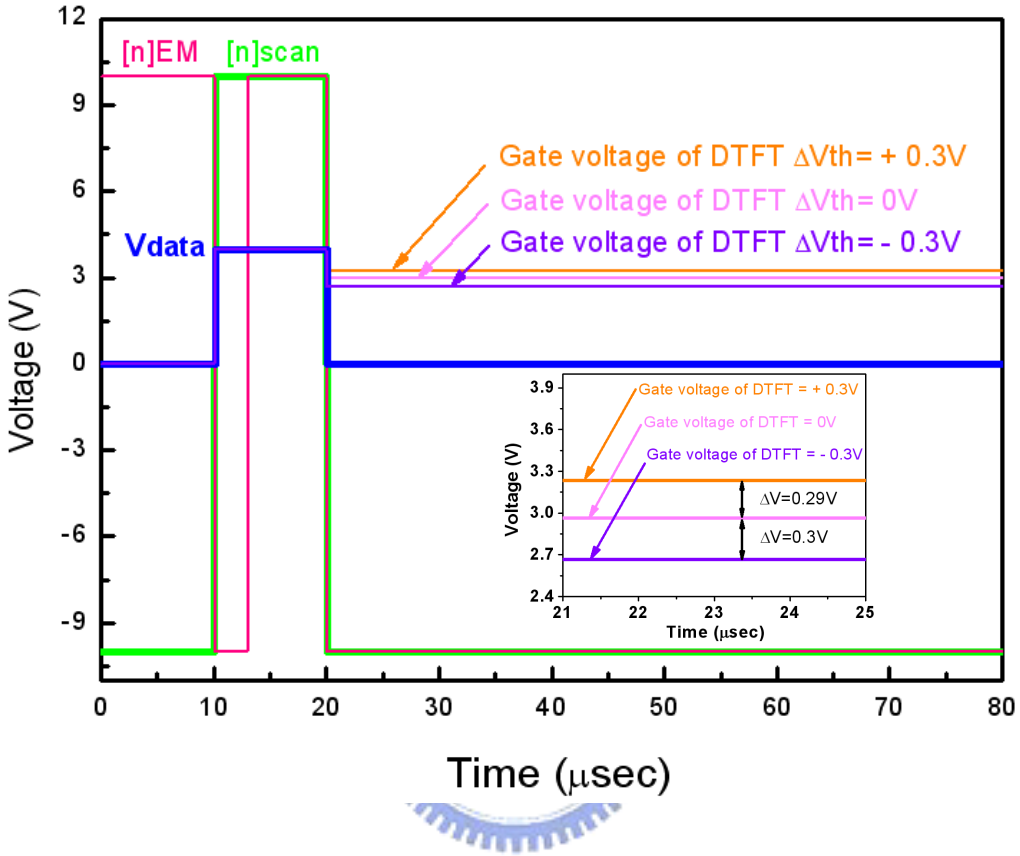
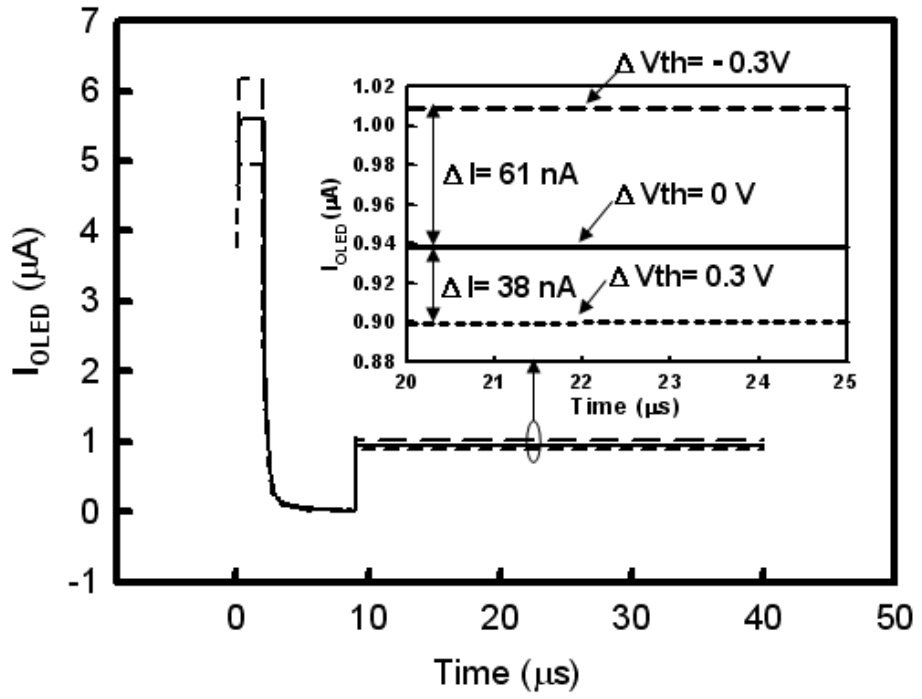
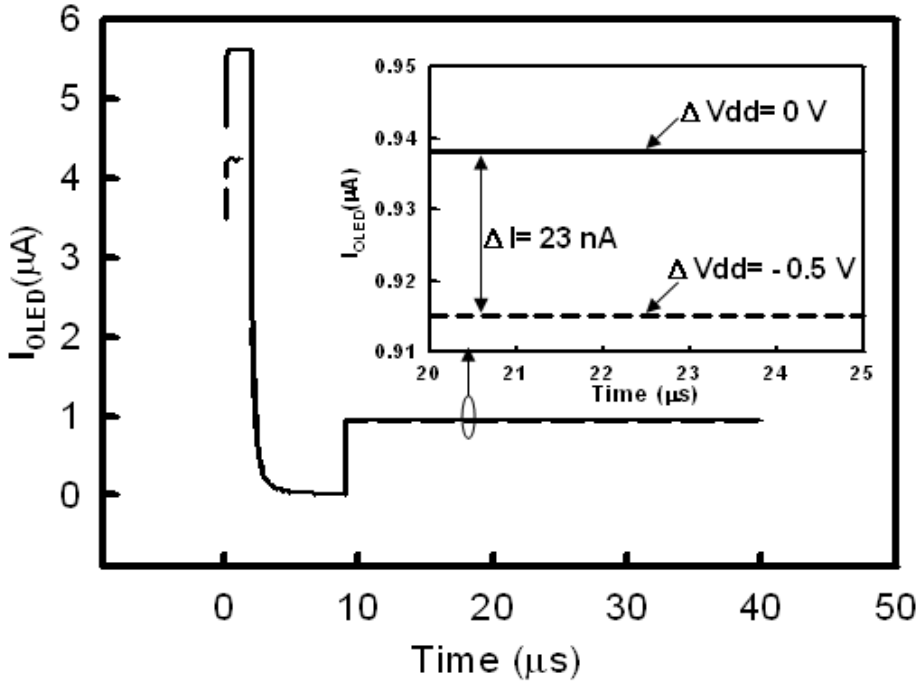


FIG. 6-6 The gate voltage stored in the capacitor with varied threshold voltages of DTFT



(a)



(b)

Fig 6-7 (a) The transient simulation results for the proposed pixel structure. With the threshold voltage shift of DTFT set as ±0.3V, the variation of output current is about 1.01~0.99 μA. (b) The transient simulation results for the proposed pixel structure. The deviation of I_{OLED} in the proposed pixel structure is less than 2.5% in the degradation of the supply voltage on panel is 0.5V.

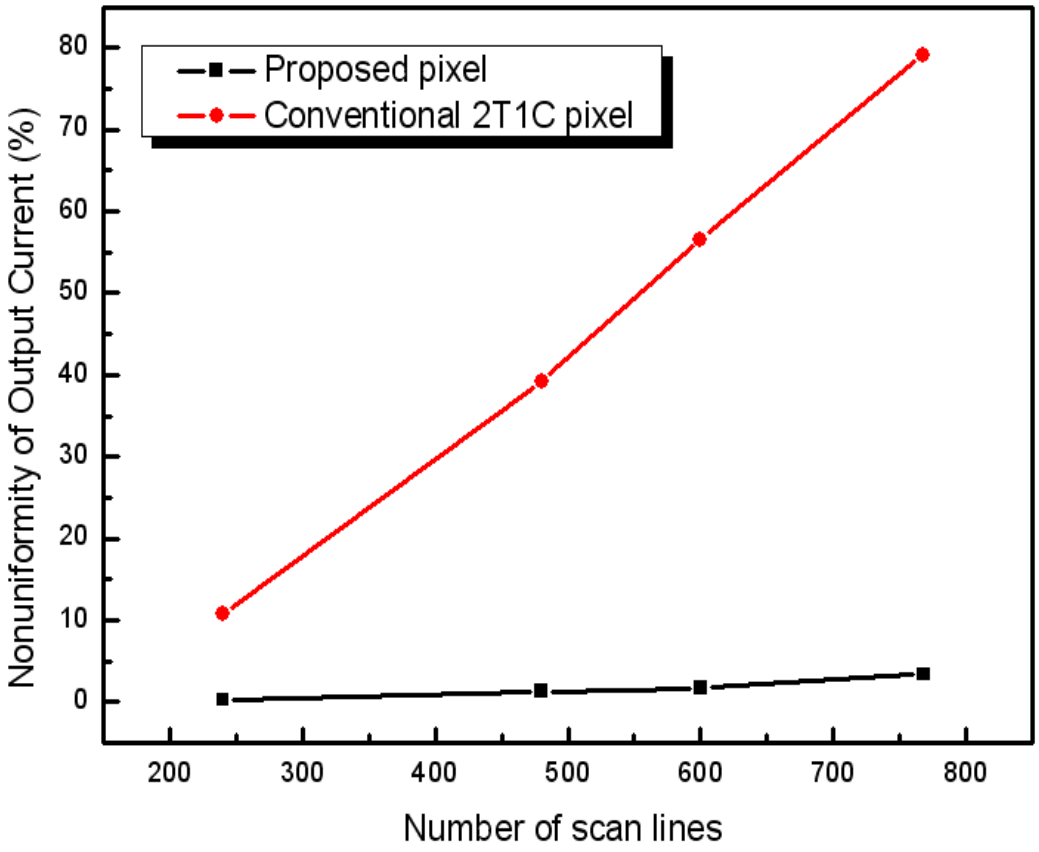


Fig. 6-8 Comparison of non-uniformity of output current between the conventional pixel structure (2T1C) and the proposed one (5T1C), caused by the drop in supply voltage with increasing number of scan lines (240, 480, 600, 768).

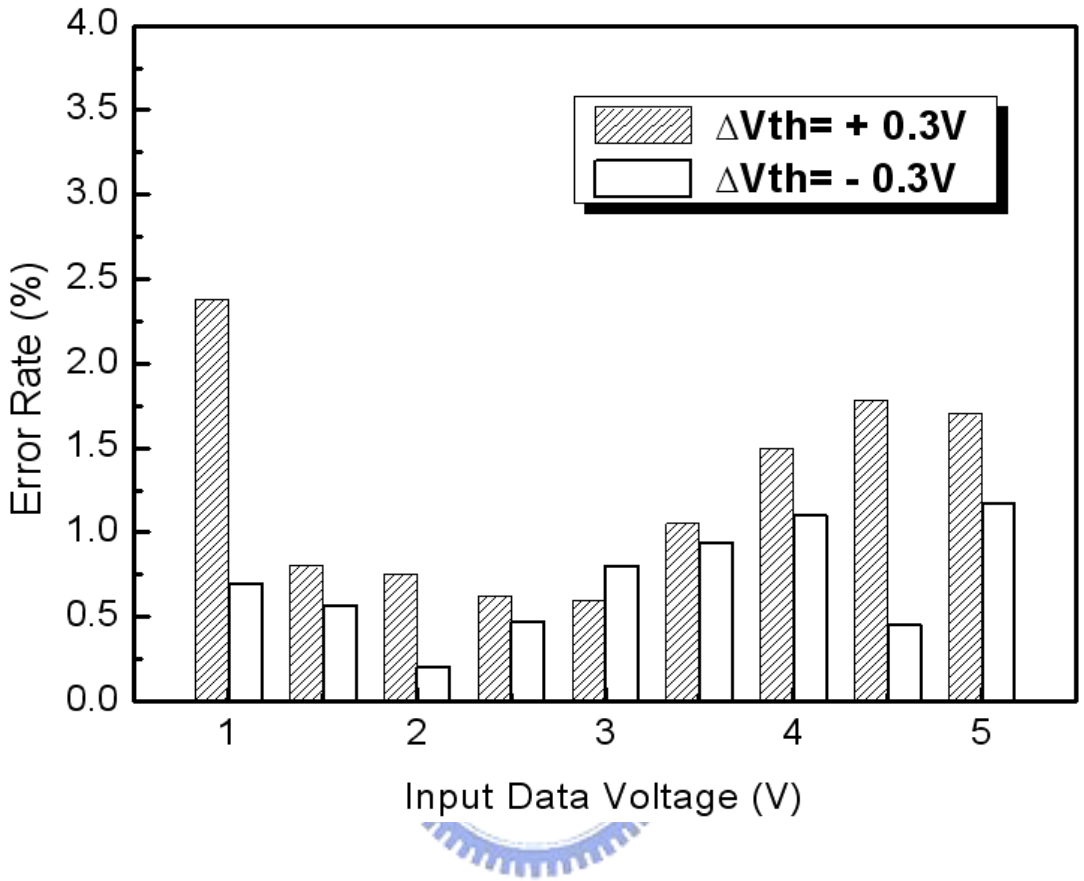


Fig. 6-9 Error rate of output current in our proposed pixel circuit due to the threshold voltage variation. The error rate of output current with the proposed design is all less than 2.5% as input data voltage ranges 1–5 V.

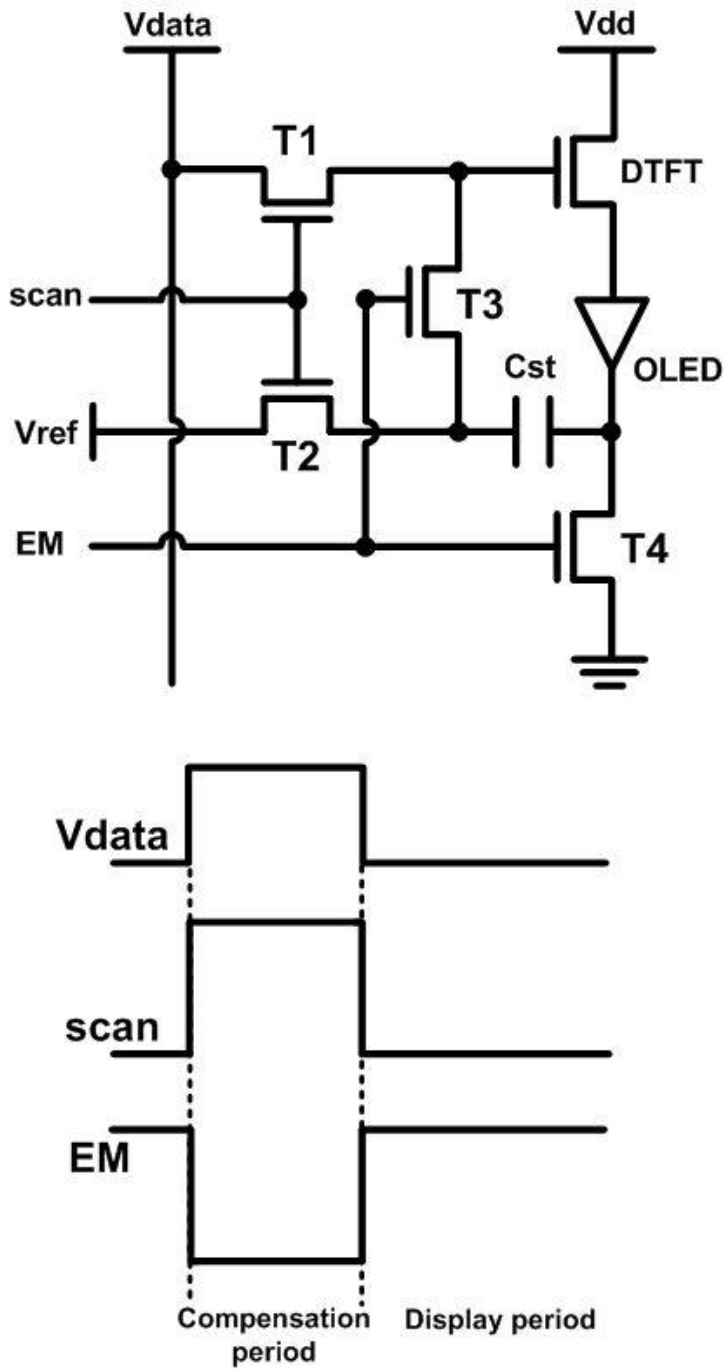
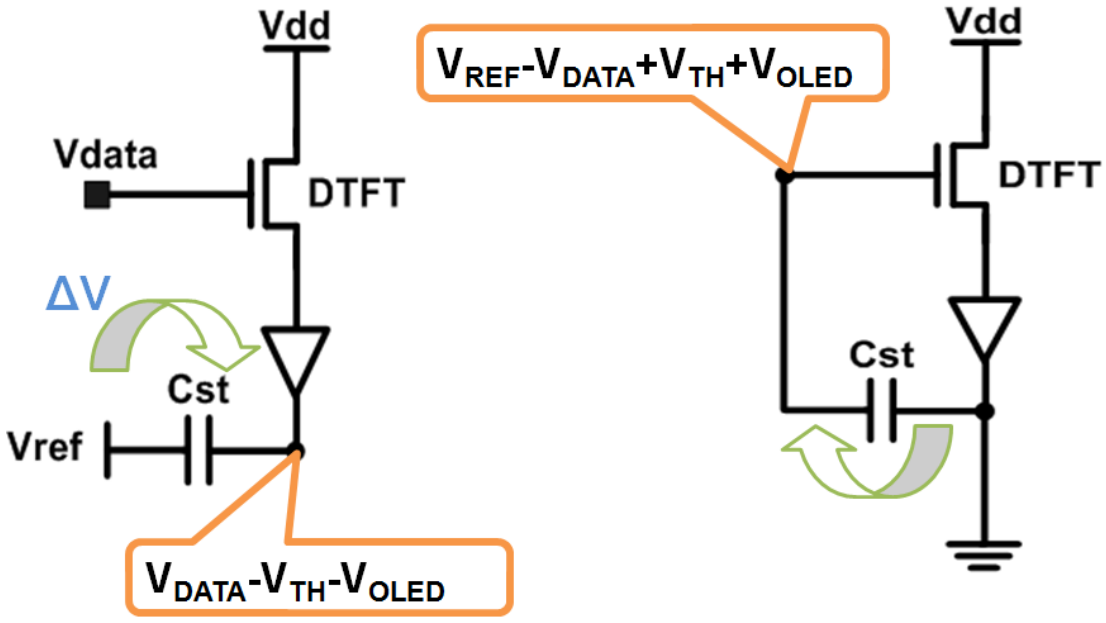


Fig. 6-10 The proposed pixel design and its timing scheme of the signal line.



(1) Compensation Period **(2) Display Period**

Fig. 6-11 The equivalent circuit at each stage in operation.

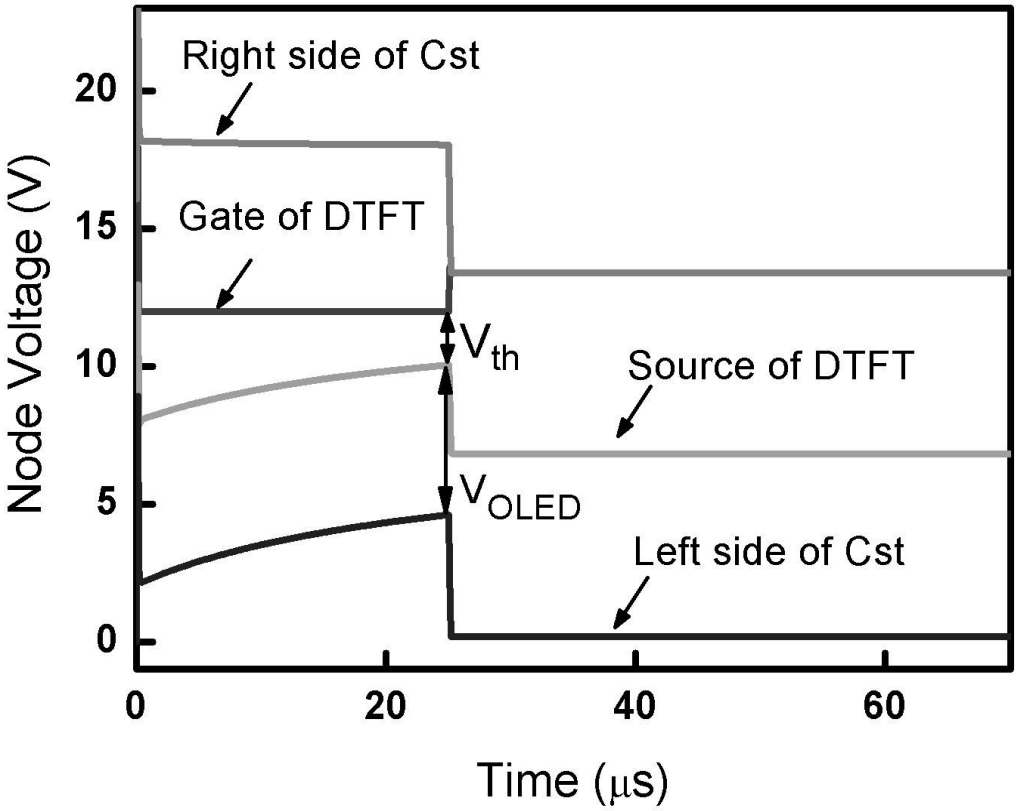
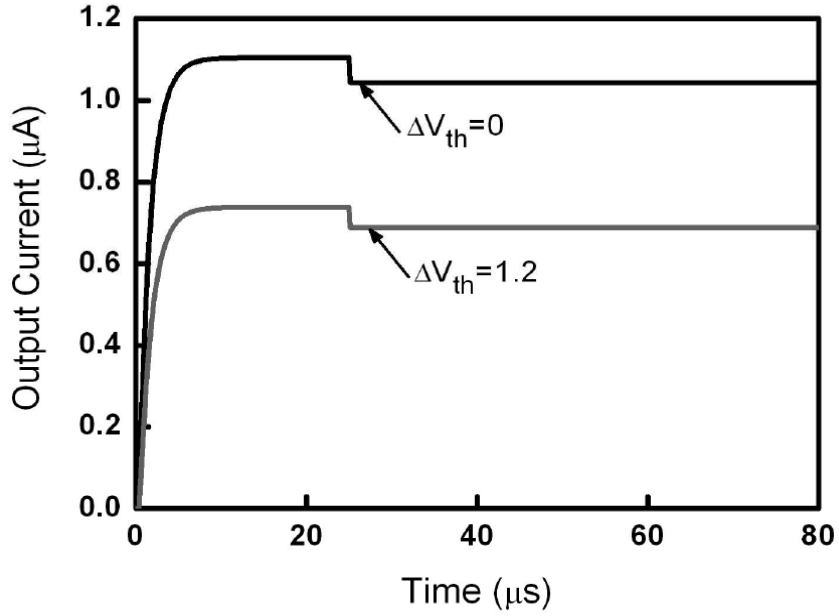
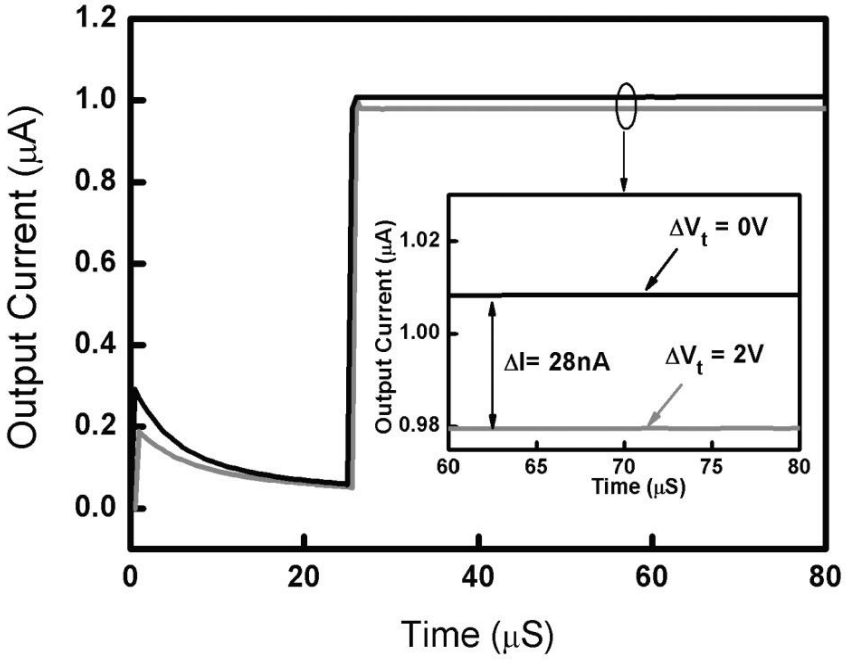


Fig. 6-12 The transient simulation result of proposed pixel design.

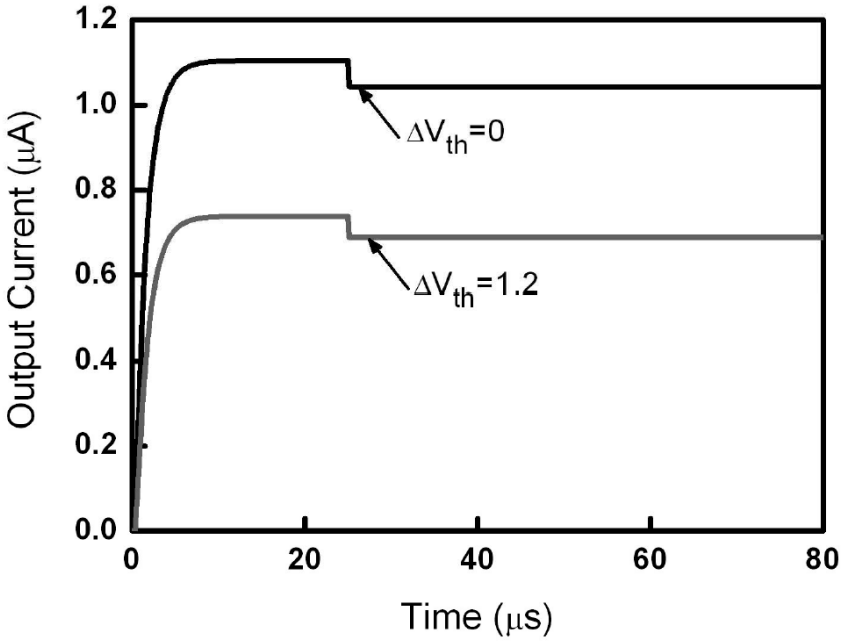


(a)

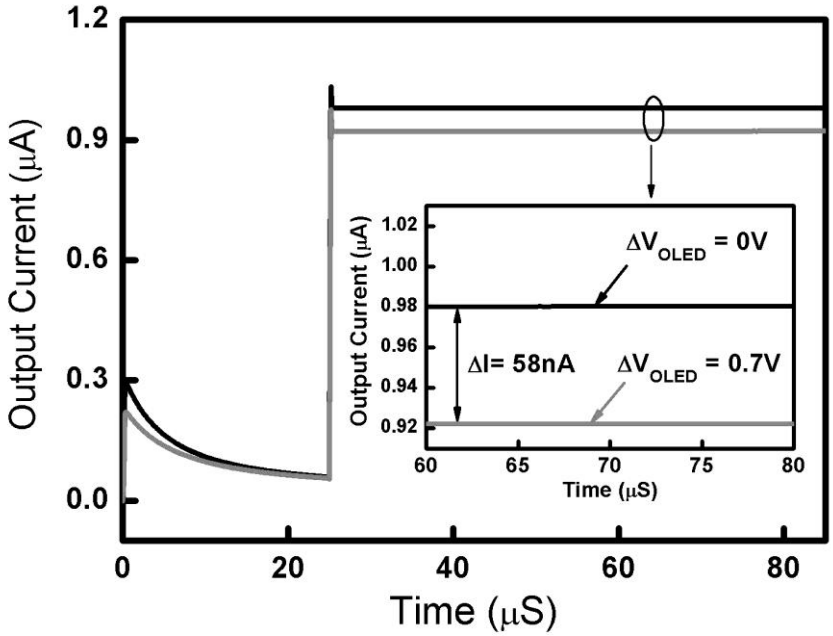


(b)

Fig. 6-13 (a)Simulation result of the conventional 2T1C pixel circuit. The variation range of I_{OLED} in 2T1C pixel is about 1.04 to 0.68 μA. (b) Simulation result of the conventional 2T1C pixel circuit as the threshold voltage shift in DTFT is set to 1.2V



(a)



(b)

Fig. 6-14 (a) Simulation result of the conventional 2T1C pixel circuit. The degradation of I_{OLED} in 2T1C pixel is about 1.04 to 0.76 μA. (b) Simulation result of the conventional 2T1C pixel circuit as the threshold voltage in OLED is set to 0.7V

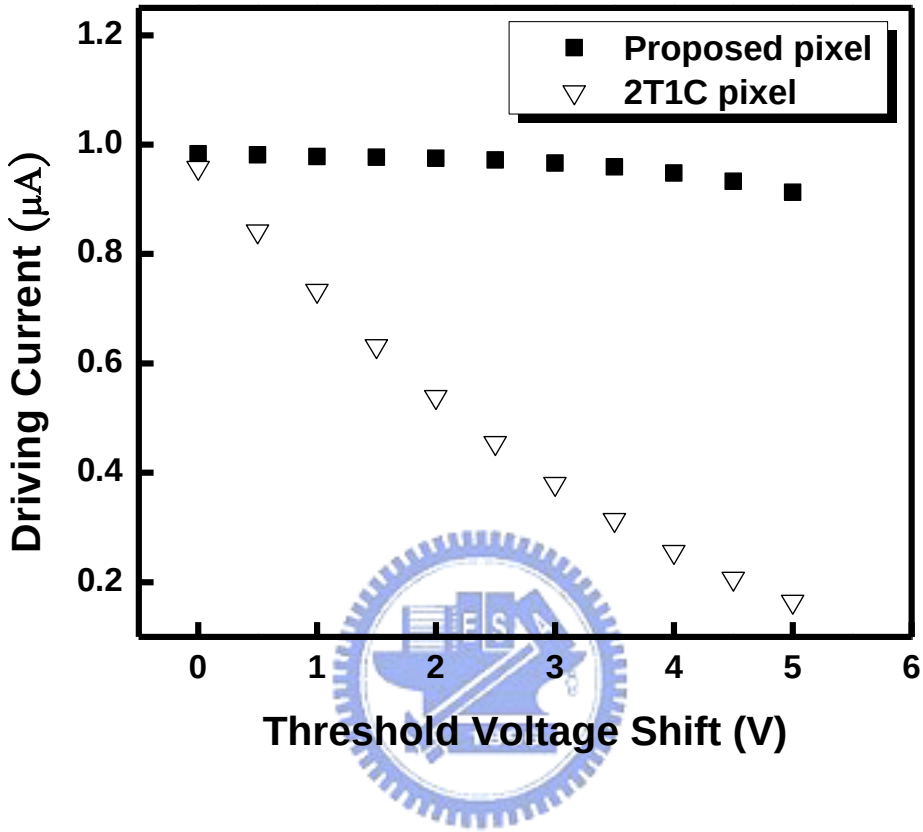


Fig. 6-15 The simulation result of driving current of proposed pixel circuit with increasing threshold voltage shift.

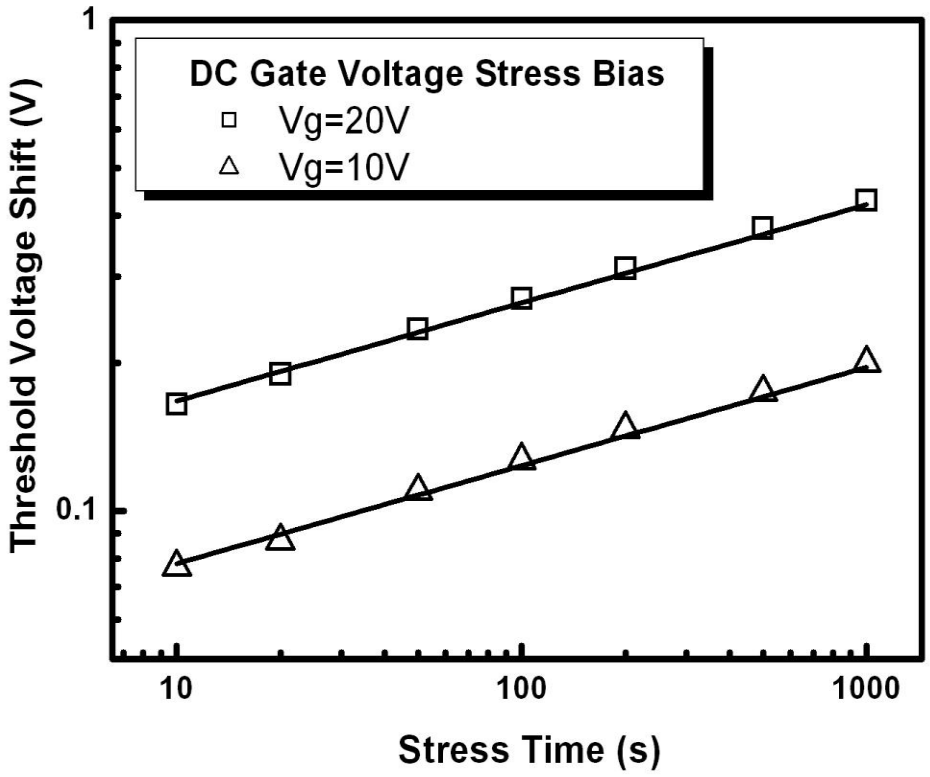


Fig. 6-16 Threshold voltage of a-Si:H TFT shifts versus stress time. The straight lines are from the plots of threshold voltage shift against stress duration.

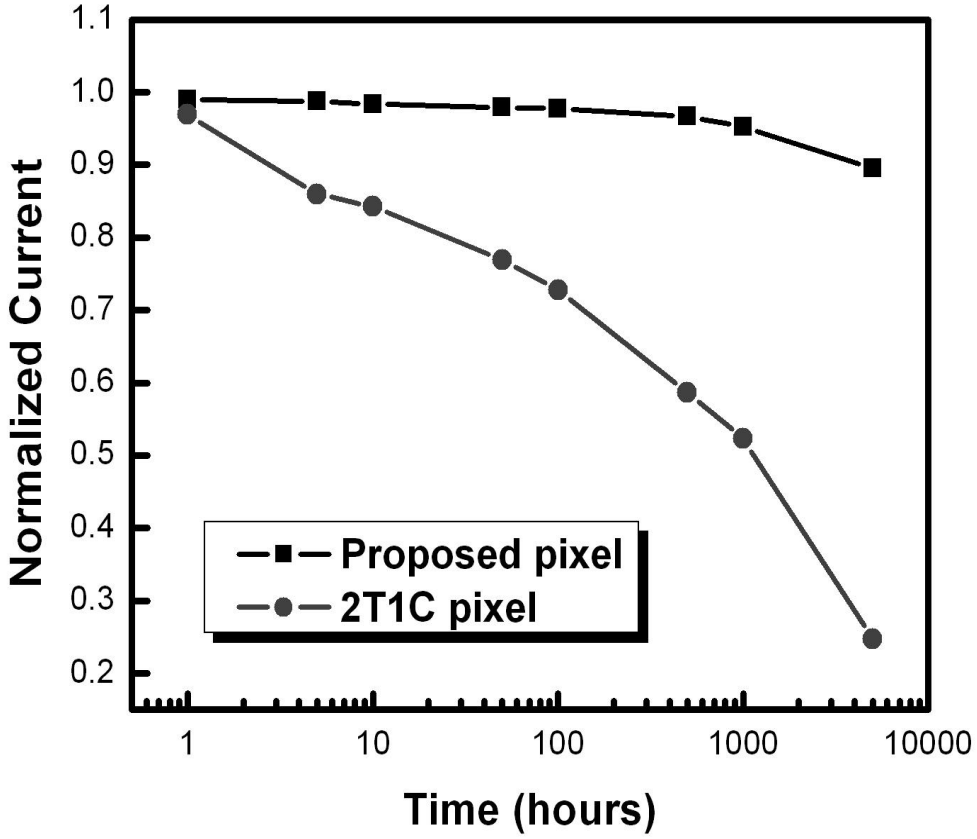


Fig. 6-17 The simulated result about the lifetime of 2T1C and proposed pixel. Considering the degradation in threshold voltage of both DTFT and OLED with increasing time, the proposed circuit exhibits only 10% current degradation at 5000H.

Chapter 7

Conclusion Remarks

In chapter 2, the photo leakage current and degraded sub-threshold swing of poly-Si TFT under illumination is completely eliminated by the full metal shielding structure. The leakage current sub-threshold swing of proposed TFT under illumination is entirely identical as those of conventional ones at dark. However, as the drain voltages are -4.5V and -9V, the negative shifts of threshold voltage (V_{TH}) are -1.08V and -2.07V, respectively. The coupling effect originated from the parasitic capacitance between drain side and shielding metal layer is proposed to explain the V_{TH} shift. In order to lower photo leakage current (I_{PLC}) with the original electrical characteristics of poly-Si TFT, the full metal shielding layer is patterned by additional mask. The issue of V_{TH} shift is released by the structure of partial metal shielding layer. In addition, the partial metal shielding layer located in the drain junction provides the shielding effect to lower $I_{PLC.}$ As drain bias is high, the shielding capability of the partial metal shielding layer located in the drain junction is vanished due to the coupling effect originated from the parasitic capacitance between drain side and shielding metal layer.

In chapter 3, we proposed two simple methods to reduce I_{PLC} and keep the electrical characteristics of poly-Si TFT. The Si-rich dielectric film is taken as light absorption layer to reduce the amount of light into the poly-Si film. The I_{PLC} of poly-Si THT with Si-rich oxide film and with Si-rich SiN_X film is lowered by 60% and 38%, respectively. The sub-threshold swing (S.S) is also improved significantly by employing Si-rich oxide film or with Si-rich SiN_X film as buffer layer. For the

AMLCD application, most pixel region should be allowed light to pass through so that the Si-rich buffer layer must be patterned to be a low-transmittance area only for the poly-Si active island. Therefore, we proposed a new process flow without adding the number of masks or complicated device structure. The proposed poly-Si TFT exhibits the impressively low leakage current and improved sub-threshold swing under illumination by using NH_3 plasma bombardment on the surface of buffer layer. The uniformity and key parameters of proposed devices are almost identical as the conventional ones. As the brightness of back-light is 5610 nit, the I_{PLC} and the variation of S.S in proposed TFT are 8.1 pA and 46.3 %, respectively while those in conventional TFT are 35.6 pA and 85.3%.

In chapter 4, we discuss the electrical characteristics of poly-Si TFT under illumination using proposed TFT with surface treated buffer layer and with patterned metal shielding layer. For treated TFT, the I_{PLC} and S.S exposed to light are markedly suppressed. It is shown that the fewer light-induced electrons and holes result in the lower I_{PLC} and improved sub-threshold properties, respectively. The S.S of poly-Si TFT under illumination is increased due to the positive potential originated from accumulated excess holes in the bottom of poly-Si layer. Furthermore, as the expose region is located in the drain junction, only I_{PLC} is raised but S.S is almost unchanged. The S.S is dramatically degraded as the expose region located in the source junction and the drain bias is high. Based on the results and proposed model, the causes of photo leakage current and degraded sub-threshold swing in poly-Si TFTs under illumination are demonstrated in this work.

In chapter 5, the degradation mechanism of poly-Si TFT with excimer laser crystallization (ELC) and with laser-crystallized laterally grown grain is investigated, respectively. The distinct decrease in on-current of poly-Si TFT is found after

dynamic stress and both the S.S and V_{TH} are kept in a good condition. The damaged region which contains numerous trap states are evidenced to be near the source /drain regions and the electrical degradation was mainly attributed to the generation of the trap states by capacitance-voltage (C-V) measurement for poly-Si TFT with ELC. Since the C-V characteristics at 10 kHz were almost unchanged but the ones at 1MHz were stretched out significantly, this can be inferred that the tail states were produced in poly-Si film due to the AC stress. In addition, the electrical degradation of GB-TFT is worse because of the effect of protrusion grain boundary. C-V measurements and device simulation demonstrate reasonably that the concentration of the electric field in the protrusion region causes intense electron gathering at the grain boundary. The degradation model which considers the effect of protrusion grain boundaries is proposed.

In chapter 6, we have developed a novel pixel circuit composed of five TFTs and one capacitor for large size and high resolution AMOLED displays. Much improved non-uniformity of output current and simple configuration are implemented by a new compensation operation. The simulation results indicate that the proposed circuit has high immunity to the variation of poly-Si TFT characteristics and the drop of supply power. We also have developed a simple pixel circuit and driving scheme for AMOLED with a-Si:H backplane. It is only composed of five transistors and one capacitor. The significant improvement in the degradation of output current is achieved by using the new compensation architecture. The simulation results have been demonstrated successfully that the proposed circuit has high immunity to the shift of threshold voltage in the a-Si TFTs and OLED. The proposed pixel design has great potential for the large size and low cost AMOLED panel.

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簡　歷

姓　　名：盧皓彥

性　　別：男

出生年月日：民國 69 年 12 月 14 日

籍　　貫：高雄縣

住　　址：高雄市楠梓區壽民路180巷9號八樓

學　　歷：

國立中山大學物理學系學士　(88.09-92.06)

國立交通大學光電工程研究所碩士班　(92.09-93.06)

國立交通大學光電工程研究所博士班　(93.09-97.06)

博士論文題目：

主動顯示器用低溫多晶矽薄膜電晶體之元件特性與補償電路研究

Study on Characterization and Compensation Circuits of Low-Temperature Polycrystalline Silicon Thin-film Transistor for Active Matrix Displays

Publication List

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