國立交通大學

電子工程學系電子研究所

博士論文

K–Band 傳收器之互補式金氧半前端關鍵積體電路設計與分析

The Design and Analysis of CMOS *K*–Band Transceiver Front-End Circuits

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摘要

本論文分別闡述兩個使用電流操作模式的射頻 (Radio Frequency, RF) 前端電路，以及使用 45 奈米 Planar Bulk CMOS 電晶體製作的低雜訊放大器 (Low Noise Amplifier, LNA) ，這些電路的操作頻率皆位在 *K* 頻段上。論文主要包含下列三個部分： (1) 設計與分析一個操作在 *K* 頻段的電流操作模式 (Current-Mode) CMOS 接收機 (Receiver) 前端電路； (2) 設計與分析一個操作在 *K* 頻段的電流操作模式 CMOS 傳送機 (Transmitter) 前端電路； (3) 使用 45 奈米 Planar Bulk CMOS 之製程技術，以及 Wafer-Level Package (WLP) 技術所製作的高 *Q* 值 Above-IC 電感，完成設計 *K* 頻段之低雜訊放大器。

本論文第二章提出一個 CMOS 電流操作模式射頻接收機前端電路，此接收機前端電路主要由一個電流操作模式的低雜訊放大器以及一個電流操作模式的降頻混波器所組成，此接收機前端電路使用 0.13-μm 1P8M CMOS 製程技術實現，並可適用在 24-GHz 的頻段上操作。量測結果顯示此接收機的轉換增益 (Conversion Gain) 為 11.3 dB ，雜訊指數 (Noise Figure ， NF) 為 14.2 dB ，等效輸入端之增益 1-dB 壓縮點 (IP_{-1dB}) 為–13.5 dBm ，等效輸入端之三階互調失真點 (P_{IIP3}) 為–1 dBm 。當低雜訊放大器的工作電壓使用 0.8 伏特，以及降頻混波器的電壓使用 1.2

伏特時，此接收器總共消耗 27.8 mW 。接收機的晶片面積為 1.45 × 0.72 mm^2 ，此晶片面積包含了測試用的銲墊 (Pad) 。由實驗的結果分析得知，本論文所提出的電流操作模式的降頻混波器電路可以操作在 *K* 頻段，操作在低電壓下，並可達到低功率消耗的特性。此外，此一整合了電流操作模式的降頻混波器以及低雜訊放大器的接收器前端電路具有低電壓操作以及低功率消耗的特點。

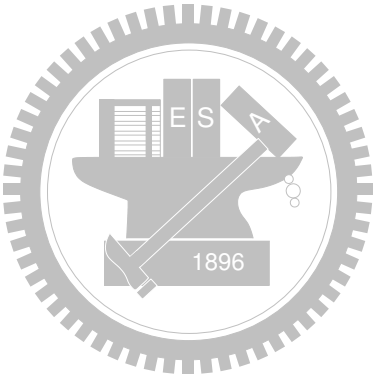
本論文第三章提出一個 CMOS 電流操作模式射頻傳送機前端電路，此傳送機前端電路主要由一個電流操作模式的升頻混波器、一個電流操作模式的基頻 (Baseband) 緩衝電路、一個電壓控制震盪器，以及一個本地震盪訊號之緩衝器電路 (VCO Buffer) 。此傳送機前端電路使用 0.13-μm 1P8M CMOS 製程技術實現，並可適用在 24-GHz 的頻段上操作。量測結果顯示此傳送機的轉換增益為–5 dB ，雜訊指數為 12.7 dB ，等效輸入端之增益 1-dB 壓縮點為–22 dBm ，等校輸入端之三階互調失真點為–9.6 dBm 。等效輸出端之增益 1-dB 壓縮 (OP_{-1dB}) 點為–28 dBm ，等效輸入端之三階互調失真點 (P_{OIP3}) 為–14.6 dBm 。整合於此傳送機中的電壓控制震盪器，可提供頻率從 20.8 GHz 至 22.7 GHz 的本地震盪訊號，當電壓控制震盪器的在輸出頻率為 22.7 GHz 時，在 10 MHz 偏移頻率的條件下，其相位雜訊 (Phase Nose) 為–108 dBc/Hz 。當工作電壓使用 1 伏特時，此傳送機前端電路總共消耗 11.7 mW 。其中，電流操作模式的升頻混撥器消耗 3.1 mW ，電壓控制震盪器消耗 2.2 mW ，本地震盪訊號之緩衝器電路消耗 3.3 mW ，電流操作模式的中頻放大電路消耗 3.1 mW 。此接收機的的晶片面積為 1.5 × 1.1 mm^2 ，此晶片面積包含了測試用的銲墊。由實驗的結果分析得知，本論文所提出的電流操作模式的升頻混波器電路可以操作在 *K* 頻段，操作在低電壓下，並可達到低功率消耗的特性。此外，此一整合了電降流操作模式的升頻混波器、基頻緩衝電路、電壓控制震盪器，以及本地震盪訊號之緩衝器電路的傳送器前端電路具有低電壓操作以及低功率消耗的特點。

由本論文所提出的接收器前端電路以及傳送器前端電路的實驗結果分析得知，電流操作模式的電路設計方法可運用在設計射頻積體電路，並具有低功率消耗的特點。此外，電流操作模式的電路設計方法更具有低電壓操作的特點，對於運用先進奈米 CMOS 製程技術來設計射頻積體電路具有相當大的潛力。

除了探討電流操作模式在射頻積體電路的可行性之外，本論文第四章分析與比較 45 奈米 CMOS 製程中之 Planar Bulk 以及 FinFET 電晶體元件之特性。並利用 45 奈米 Planar Bulk CMOS 之製程技術，以及 WLP 技術所製作的高 Q 值 Above-IC

電感，成功地實現兩個操作於 *K* 頻段之高性能低雜訊放大器。經量測驗證後，單端一級 Cascode 架構的低雜訊放大器的中心操作頻率為 23 GHz ，其增益為 7.1 dB ，雜訊指數為 4 dB ，等效輸入端之增益 1-dB 壓縮點為–9.5 dBm ，等效輸入端之三階互調失真點為 +2.5 dBm 。在工作電壓為 1 伏特的條件下，功率消耗為 3.6 mW 。此單端一級 Cascode 架構的低雜訊放大器的晶片面積為 0.72×1.12 mm^2 ，此晶片面積包含了測試用的銲墊。除此之外，單端兩級串接的 Cascode 架構的低雜訊放大器的中心操作頻率為 23.4 GHz ，其增益為 11.6 dB ，雜訊指數為 4.4 dB ，等效輸入端之增益 1-dB 壓縮點為–16 dBm ，等效輸入端之三階互調失真點為–4.2 dBm 。在工作電壓為 1 伏特的條件下，功率消耗為 9.3 mW 。此單端兩級串接的 Cascode 架構的低雜訊放大器的晶片面積為 1.28×1.12 mm^2 ，此晶片面積包含了測試用的銲墊。

本章所提出的兩個低雜訊放大器，為第一個成功的使用 45 奈米 Planar Bulk CMOS 製程，實現操作於 *K* 頻段的低雜訊放大器；此外，透過使用 Figure-of-Merit (FOM) 進行綜合效能評比，與已發表的操作在相同頻率的 CMOS 低雜訊放大器相互比較後，所設計的單端一級 Cascode 架構的低雜訊放大器，為當前性能最佳的低雜訊放大器，其 FOM 值可達到 15.2 GHz 。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The Design and Analysis of CMOS K–Band Transceiver Front-End Circuits

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Abstract

In this dissertation, two radio-frequency (RF) front-end circuits using current-mode design methdologies have been proposed and implemented. Moreover, two low-noise amplifier (LNA) using 45-nm planar bulk-CMOS technology have also been implemented. The operation frequency of the two current-mode RF front-end circuits and the two 45-nm LNAs are within the frequency of K-Band. This dissertation can be mainly divided into three parts, including (1) design and analysis of the K-Band current-mode CMOS receiver front-end circuits, (2) design and analysis of the K-Band current-mode CMOS transmitter front-end circuits, and (3) The K-Band LNAs using 45-nm planar bulk-CMOS technology with high-Q above-IC inductors implemented through wafer-level package (WLP) technology.

A CMOS current-mode receiver front-end integrated circuit has been proposed. The proposed current-mode receiver front-end is composed of a current-mode LNA and a current-mode down-conversion mixer. This receiver front-end is fabricated in 0.13-μm 1P8M CMOS technology and is operated in the frequency band of 24 GHz. From the

measurement results, the proposed integrated current-mode receiver front-end has the conversion gain of 11.3 dB, the input-referred 1-dB compression point (IP_{-1dB}) of –13.5 dBm, and the input-referred third-order intercept point (P_{IIP3}) of –1 dBm. The measured noise figure (NF) is 14.2 dB at the RF frequency of 24 GHz and LO frequency of 19 GHz. The total power dissipation of this current-mode receiver front-end dissipates 27.8 mW under the condition that the supply voltage of LNA is 0.8 V and the supply voltage of mixer is 1.2 V. The proposed current-mode receiver front-end occupies the active area of 1.45 × 0.72 mm^2 where testing pads are included. From the experimental results, the proposed CMOS current-mode down-conversion mixer can operate well in the K-band, and achieves low-power consumption under low power supply voltage. It can also be shown that the proposed receiver front-end circuit that is integrated with a current-mode down-conversion and LNA has the advantage of low-voltage operation and low-power consumption.

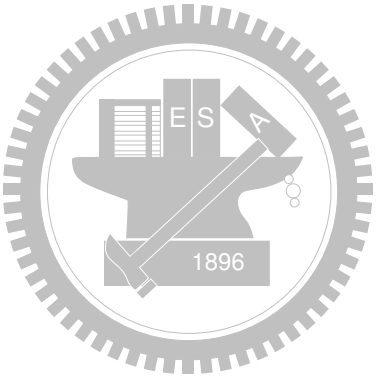
A CMOS current-mode transmitter front-end integrated circuit has been proposed. The proposed current-mode transmitter front-end is composed of a current-mode up-conversion mixer, a current-mode baseband amplifier/repeater, a VCO and a transformer-based VCO buffer/repeater. This transmitter front-end is fabricated in 0.13-μm 1P8M CMOS technology and is operated in the frequency band of 24 GHz. The measured results have shown that the proposed integrated current-mode transmitter front-end exhibits a measured conversion power gain of –5 dB, an IP_{-1dB} of –22 dBm, an output-referred 1-dB compression point (OP_{-1dB}) of –28 dBm, P_{IIP3} of –9.6 dBm, and an output-referred third-order intercept point (P_{OIP3}) of –14.6 dBm. The single-sideband (SSB) noise figure (NF) is about 12.7 dB. The on-chip VCO provides the LO frequency from 20.8 GHz to 22.7 GHz with the control voltage varied from 0 V to 2 V. The phase-noise of the VCO is -108 dBc/Hz at 10-MHz offset from 22.7 GHz. Under the 1-V supply voltage, the fabricated current-mode double-balanced up-conversion mixer, VCO, VCO buffer/repeater and baseband current buffer/repeater circuits dissipate 3.1 mW, 2.2 mW, 3.3 mW, and 3.1 mW, respectively. The proposed transmitter front-end occupies the active area of 1.5 × 1.1 mm^2 where testing pads are included. From the experimental results, the proposed CMOS current-mode up-conversion mixer can operate well in the K-band, and has a very small power consumption. Moreover, it can also be sown that the proposed transmitter front-

end circuit that is integrated with a current-mode up-conversion mixer, a baseband current buffer/repeater, a VCO, and a transformer-based VCO buffer/repeater has the advantage of low-voltage operation and low-power consumption.

From the experimental results of the proposed receiver front-end and transmitter front-end circuits, it can be shown that the current-mode design approach is suitable for designing RF integrated circuits and has the advantage of low-power consumption. Moreover, the current-mode approach also has the advantage of low-voltage operation and has great potential for designing RF integrated circuits in advanced nanometer CMOS technologies.

In addition to investigating current-mode approach to the RF integrated circuits, two K-band high performance LNAs have been successfully realized by using the 45-nm planar bulk-CMOS technology and high-Q above-IC inductors in WLP technology. The first LNA is made up of a single-ended one-stage cascode amplifier. The measurement results of the implemented one-stage cascode LNA show that the one-stage LNA has a NF of 4 dB, a gain of 7.1 dB, an IP_{-1dB} of –9.5 dBm, and a P_{IIP3} of +2.25 dBm. The center frequency of this LNA is about 23 GHz. The LNA consumes 3.6 mW from 1-V power supply voltage. The one-stage cascode LNA occupies the active area of 0.72×1.12 mm^2. Moreover, the measurement results of the implemented two-stage cascaded cascode LNA show that the two-stage LNA has a NF of 4.4 dB, a gain of 11.6 dB, an IP_{-1dB} of –16 dBm, and a P_{IIP3} of –4.2 dBm. The center frequency of the two-stage LNA is about 23.4 GHz. The LNA dissipates 9.3 mW from 1-V power supply voltage. The two-stage cascaded cascode LNA occupies the active area of 1.28×1.12 mm^2.

It is at present the first two successfully verified 45-nm planar bulk-CMOS LNAs operated above 10 GHz. Moreover, as compared to prior works which are operated at the frequency around K-band, it has been shown that the proposed one-stage cascode LNA has the best performance in terms of figure-of-merit (FOM). The FOM of the proposed one-stage cascode LNA is 15.2 GHz.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王文傑

WEN-CHIEH WANG

National Chiao-Tung University

2009, June

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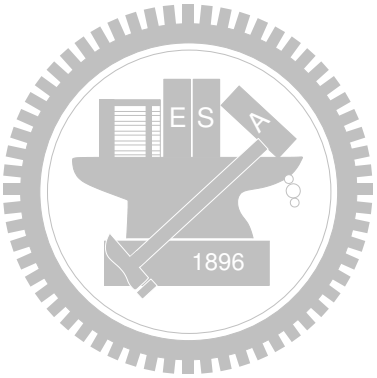

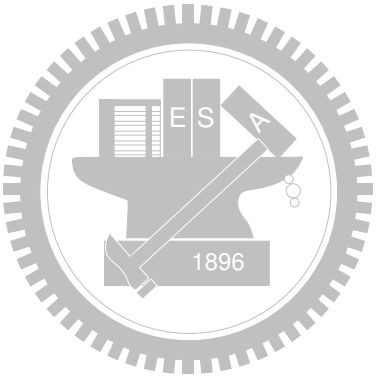

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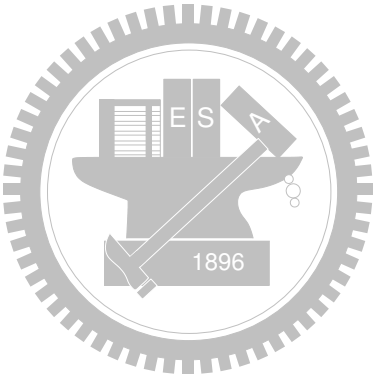

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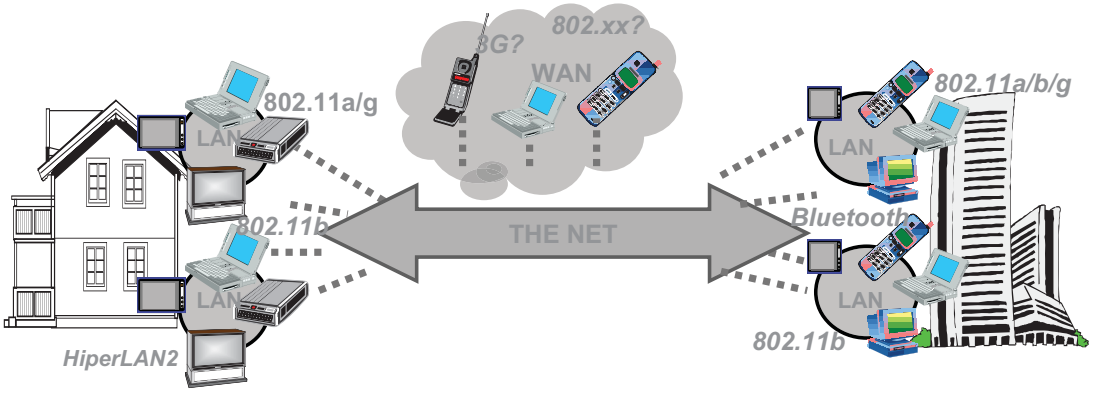
Chapter 1

Introduction

1.1 Background

Over the last two decades, the frequency spectra within 1 GHz to 10 GHz have gradually become crowded because the massive requirements of data transmission from the modern wireless applications have intensively sprung up. These popular wireless standards and their application are shown in Fig. 1.1 [1]. Fig. 1.2 depicts the different application coverage of personal-area network (PAN), local-area network (LAN), metropolitan-area (metro) network (MAN) and wide-area network (WAN). These modern wireless communication systems, such as global system for mobile (GSM), general packet radio service (GPRS), enhanced data GSM environment (EDGE), wideband code division multiple access (W-CDMA), personal handy-phone system (PHS), digital video broadcasting–handheld (DVB–H), radio-frequency identification (RFID), ZigBee, Bluetooth, wireless local area network (WLAN), high performance radio LAN (HiperLAN) type-I and type-II, ultra-wideband (UWB), etc., have induced a great deal of interferences which will influence the quality of data transmission [2]–[49]. Due to overcrowding and interferences at low frequency spectra, the operating frequencies of these applications have been pushed toward the higher frequency bands. Sufficient free spectra for future wireless networks or wireless services are allocated at industrial-science-medical (ISM) radio bands around 17 GHz, 24 GHz, and 60 GHz [50]. Consequently, many researchers start to investigate millimeter-wave transceiver front-end circuits at the higher frequency



WLAN	Fixed Wireless Access	Mobile Wireless Access	PAN	WAN
802.11a/b/g/n	802.16d	802.16e	Bluetooth UWB	GPRS/EDGE WCDMA

Figure 1.1 The popular wireless standards and applications today [1].

bands, 24 GHz (*K*-Band) [51]–[67] and 60 GHz (*V*-Band) [68]–[72] for example, where the spectra are much cleaner and can provide higher bandwidth. As shown in Fig. 1.3, the higher bandwidth of these radio bands enables significantly the higher data rata applications. Moreover, the relationship between transmission bit-rate and coverage is shown in Fig. 1.4. As shown in Fig. 1.5 [73], the required data rates of the consumer electronics has been increased from 20 Mbps to 10 Gbps. To make these consumer electronics wireless, it demands very high data bandwidth and, therefore, higher operating frequency such as 24 GHz and 60 GHz. In the recent years, several standards have been set for the wireless consumer electronics with very high data rates in the frequency bands of 24 GHz and 60 GHz.

In the globally available 60-GHz frequency band, a large amount of spectrum is available on an unlicensed basis in many regulatory domains. The band 57–64 GHz is allocated in North America [74], [75] and South Korea, while 59–66 GHz is allocated in Japan [76]. Besides, European Union (EU) is in the process of creating similar alloca-

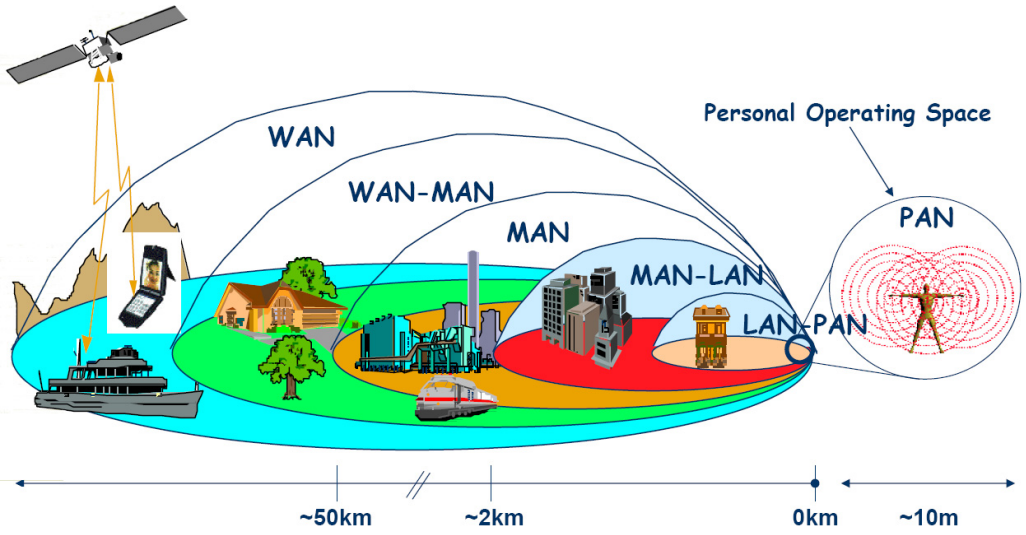


Figure 1.2 The application coverage of PAN, LAN, MAN and WAN.

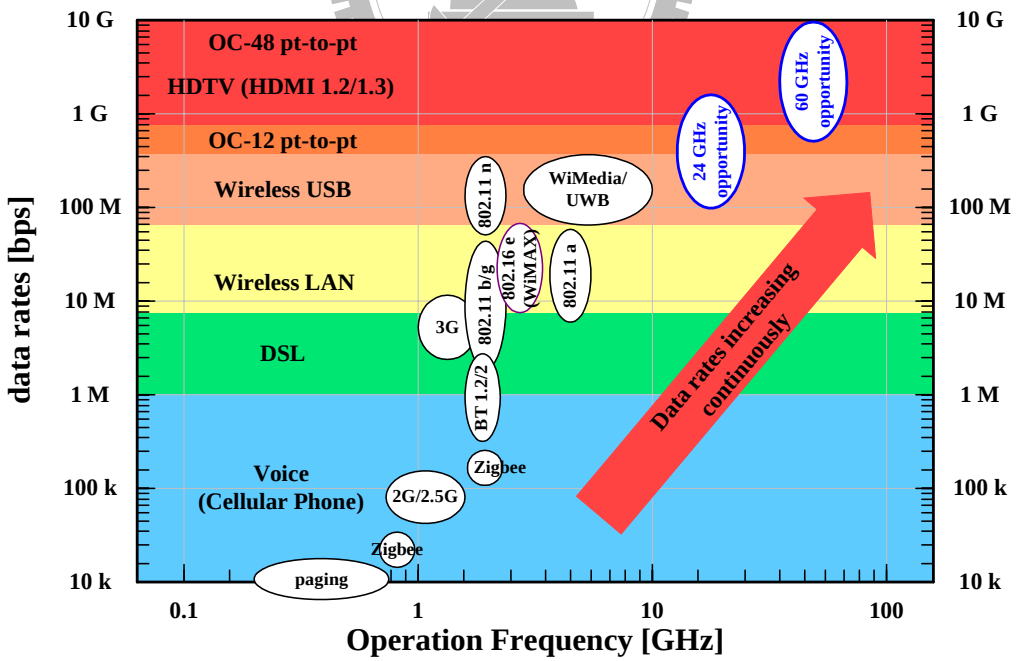


Figure 1.3 The evolution and landscape of wireless communication.

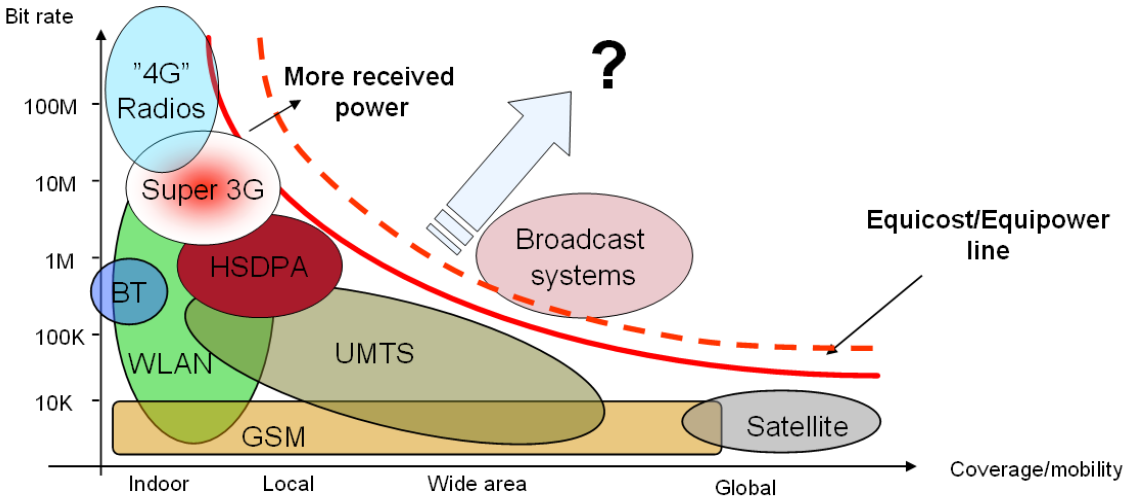


Figure 1.4 The bit rate versus coverage of the today wireless applications.

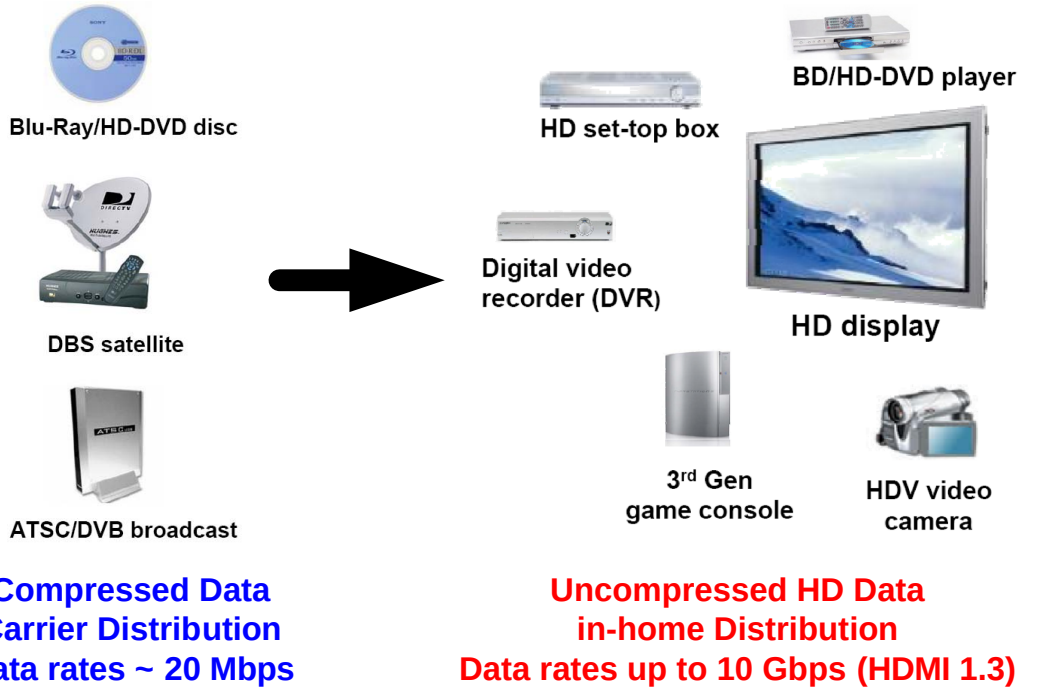


Figure 1.5 The bandwidth demands in consumer electronics [73].

tions [77]. A total of 7 GHz is allocated for use, 5 GHz of which is overlapping. With 7 GHz of bandwidth, there are many high data rate applications that one can envision. The 60-GHz radio can be useful in the design of high-speed (up to several Gbps) wireless links. Recent development in 60-GHz radio technologies are for two main applications: a) fixed wireless, and b) wireless personal area network (WPAN). In fixed wireless application, it has been used in point-to-point high speed links for telecommunications backhauls. In WPAN applications, particularly with increased use of high-definition television (HDTV), the standard organizations, such as Institute of Electrical and Electronics Engineering (IEEE), WirelessHD Alliance, European Computer Manufacturers Association (ECMA), and European Telecommunications Standard Institute (ETSI), as well as several industrial companies are working for the standardization of the 60-GHz radio [78]–[84]. In addition to the IEEE 802.16 standard for wireless metropolitan area network (WMAN) which covers 10 to 66 GHz [79], the IEEE is already home to a standard initiative for 60-GHz WPANs, called IEEE 802.15.3c [80]. Besides, the WLAN portion of the IEEE, 802.11, which sets the base standards for Wi-Fi, is considered to create a standard for 60 GHz. The IEEE 802.15.3c group is firmly focused on distribution of high-definition video and other content, and on high speed synchronization of devices, which does not seem to leave much space for 60-GHz Wi-Fi where the study group IEEE 802.11 is focusing on very high throughput (VHT) Wi-Fi but under IEEE rules [81].

The WirelessHD Alliance has completed the WirelessHD (WiHD) Version 1.0 high-speed radio communication standard for data rates of up to 4 Gbps via the globally unlicensed 60-GHz band of the spectrum [82]. The wide bandwidth makes it possible to attain a high data transfer rate. It was developed to provide a way of connecting high-definition content sources and screens cordlessly. Note that the core technology of WiHD promotes theoretical data rates as high as 25 Gbps. The WiHD replaces the wires in the high definition multimedia interface (HDMI) with radio links, and is designed to handle HDTV video streams between audio/video (AV) equipments. The target is defined as handling full HD video without high-efficiency coding. The ECMA TC-48 is developing a standard for short-range communications in the unlicensed 60-GHz band of the spectrum [83], [84]. The standard will provide high-rate WPAN (including point-to-point) transport for both data transfer and multimedia streaming. The key applications are HD

AV streaming, wireless docking station, and short-range Sync&Go.

The bands at higher frequency are attractive to RF designers despite their associated high dispersion losses. So far, numerous work have been targeted at the free spectrum of 60 GHz. However, most of the standards for 24-GHz and 60-GHz applications are still under development. In the near future, the commercial applications may prefer the frequency spectra at 24-GHz frequency band, because several standards have been developed for this frequency band and the CMOS technology is gradually matured for the wireless applications in the 24-GHz frequency band. In addition to the ISM band within 24–24.25 GHz [50], [85], the Federal Communications Commission (FCC) has also opened the spectrum from 22 GHz to 29 GHz in 2002. The 7-GHz spectra have been allocated for ultra-wideband vehicular radar applications, short-range automotive radar systems, and autonomous cruise control (ACC) applications [86]–[88], making the 24-GHz band appealing from both wireless communication and car radar perspectives, which are shown in Fig. 1.6 [89]. Some applications such as WLANs, local multi-point distribution services (LMDS) [85], point-to-point wireless communications [90], and other ISM applications have been also proposed in the frequency band of 24 GHz. Furthermore in Europe, the ETSI has specified that the HiperLink standard will be allocated in the 17-GHz ISM band to provide point-to-point short-range connections, and the HiperAccess will adopt frequencies higher than 20 GHz to cover long-range distances [91]. Of particular interest for the next WLAN generation is the 17 GHz band in the frequency range from 17.1 GHz to 17.3 GHz [66], [67]. Several promising studies have been published about indoor propagation conditions and its potential for future wireless network systems. It is intended to use 17 GHz band for a parallel network to the existing WLANs with data rates up to 54 Mb/s (HiperLAN) and for short range links with data rates up to 155 Mb/s (HiperLink). Such short range high data rate connections are ideally suited to link modern multimedia devices within the office or home. The ETSI has also specified the automotive collision warning short-range radars will be allocated in 24 GHz band which is from 24.05 GHz to 24.25 GHz [92]–[95].

According to the above-mentioned situations, Fig. 1.7(a) [89] and Fig. 1.7(b) [96] show such scenarios with clusters for short-range and long-range backbone wireless communication networks for home-RF applications at 17 GHz, 24 GHz, and 60 GHz in the

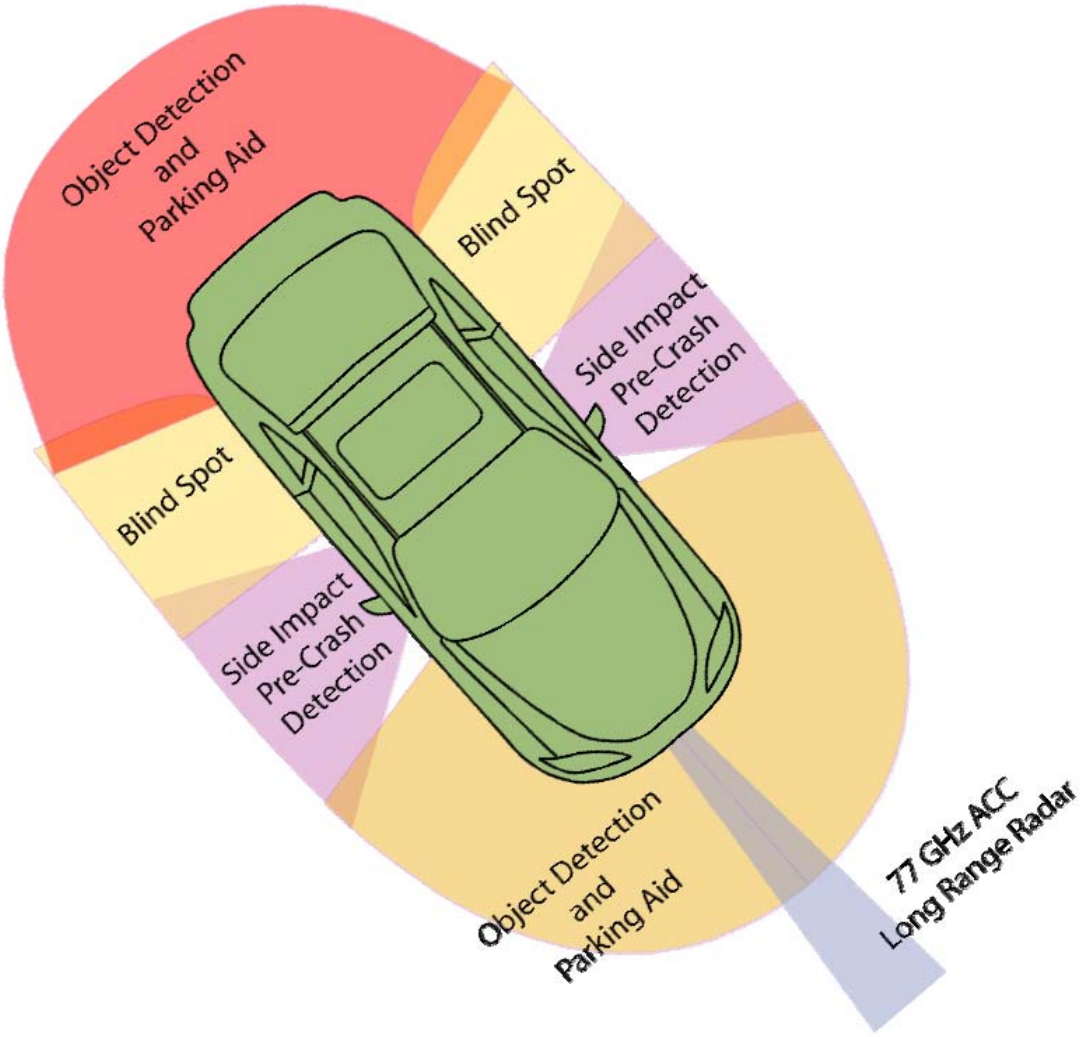
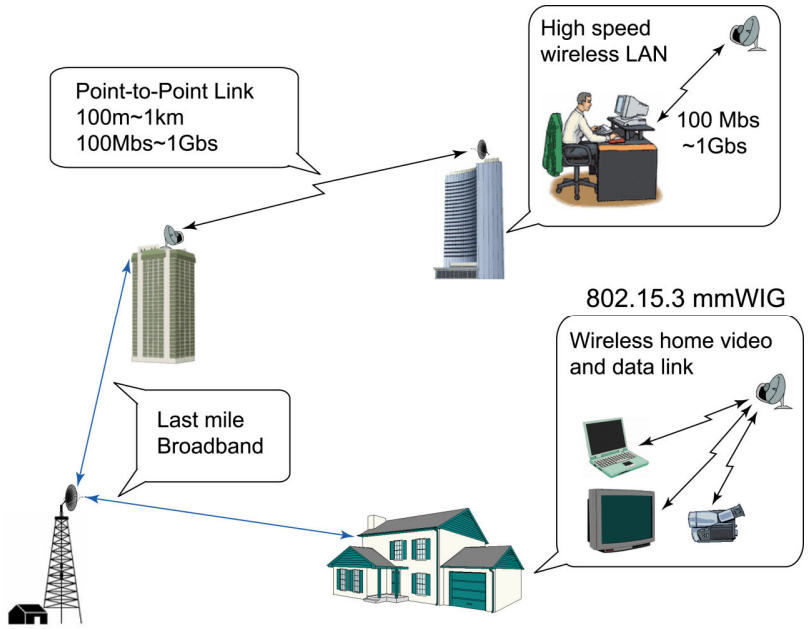


Figure 1.6 The illustration of vehicular radar applications [89].

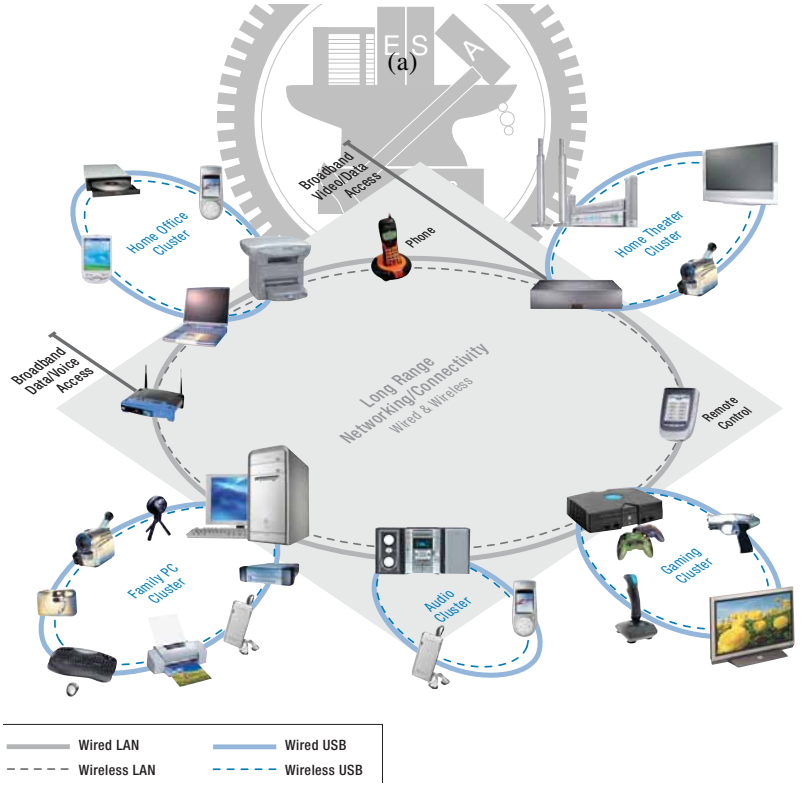
near future. Although the standardizations of both applications have not been accomplished, the possibilities of new huge wireless market lead to the interest of the communication industries.

To implement new hardware for wireless communication systems, low manufacturing costs are of paramount importance to be competitive in the stringent wireless markets. This argument drives the research on highly integrated semiconductor chips, and the ultimate goal is a low cost solution of a wireless transceiver combined both analog RF front-end and digital baseband signal processing on the same die without any external components. Nevertheless, in the past, the millimeter-wave circuits that operated in 24-GHz, 60-GHz, or even higher frequency bands were usually realized by the SiGe(C), BiCMOS, or III-V devices because of their high unity gain frequency f_T and maximum operating (or oscillation) frequency f_{MAX} [19], [20], [97]–[104]. Although SiGe(C), BiCMOS, and III-V devices exhibit good performance in high-frequency circuits, these technologies suffer from high cost and great difficulties to integrate with complex digital systems which are usually realized by CMOS technologies. In the past, CMOS technologies are not well suited for high frequency analog and RF circuits. The CMOS transistors have poor characteristics in terms of gain, noise, and high frequency behavior in comparison to bipolar transistors. Furthermore, high substrate conductivity of silicon-based processes introduces additional inductive and capacitive energy loss mechanisms in passive components, such as inductors, capacitors, and transmission lines, which are intensively used in high-speed, RF, and microwave ICs. These effects together with relatively thin metallization layers degrade the quality factor of the on-chip passive devices [105]–[109].

In recent years, significant performance improvement of CMOS digital applications comes from continuous scaling of CMOS channel length. In MOSFETs, smaller dimensions result in shorter transient times and lower parasitic capacitances. Even in a velocity-saturated MOSFET, the reduction in the channel length improves the f_T by lowering the gate-to-source capacitance. From ITRS prediction, the advancement of the CMOS transistors in accordance with the reduction in the gate length has been shown in Fig. 1.8 [89]. As shown in Fig. 1.9, the f_T of CMOS devices have been beyond several tens GHz with the fast advancement of CMOS technologies into nanometer or decananometer nodes and comparable to those of SiGe(C) bipolar and BiCMOS and III-V



(a)



(b)

Figure 1.7 The scenarios for short-range and long-range backbone wireless communication networks for home-RF applications (a) [89], and (b) [96].

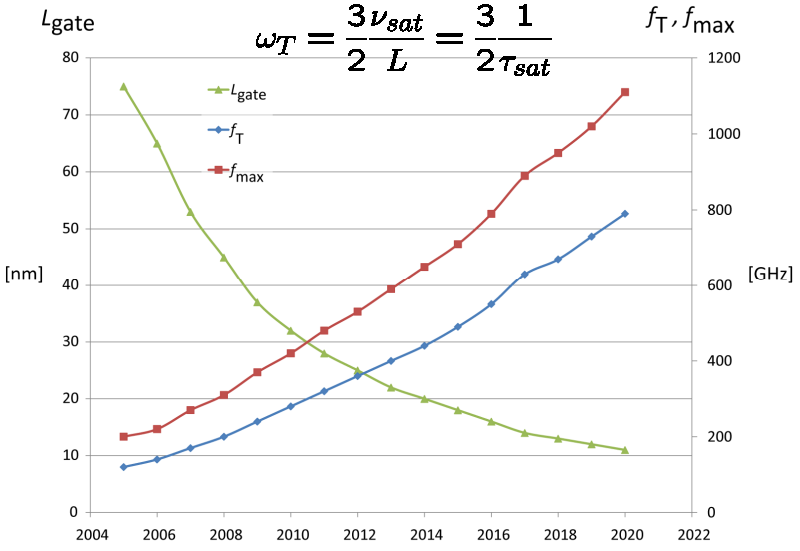


Figure 1.8 The prediction of advancement of CMOS transistors in accordance with the reduction in the gate length by ITRS [89].

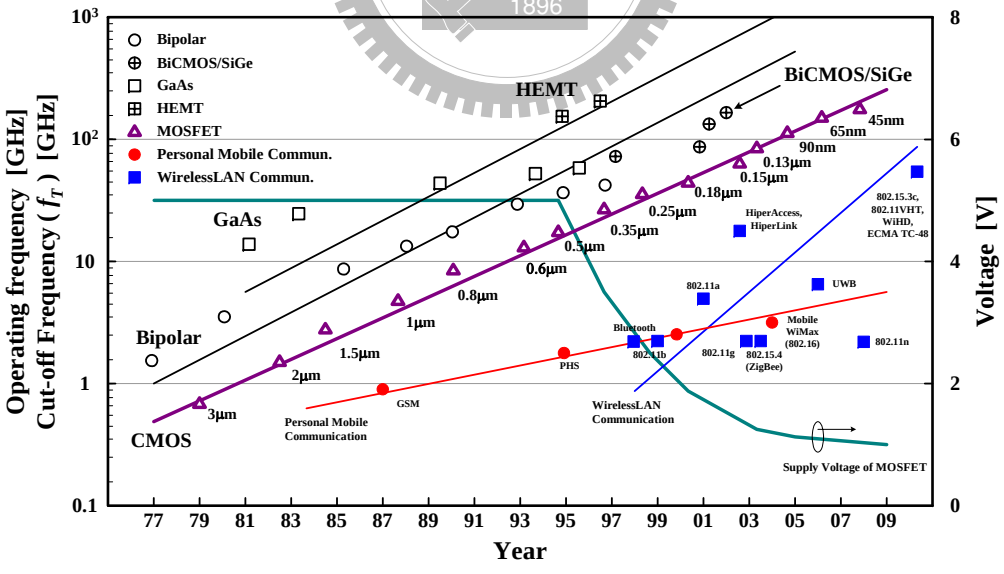


Figure 1.9 f_T of various kinds of technologies and frequency of personal mobile and wirelessLAN communication are plotted versus years. The supply voltage of MOSFET is also plotted.

Table 1.1
PROS AND CONS OF DIFFERENT TECHNOLOGIES

Technology	GaAs, HEMT	SiGe/BiCMOS	CMOS
g_m	High	Moderate	Low
f_T	High	Moderate	Low
RF performance	High	Moderate	Low
Yield	Low	Moderate	High
Integration capability	Low	Moderate	High
Cost	High	Moderate	Low
Technology improvement	Slow	Moderate	Fast

technologies [19], [20], [110], [111]. Hence, nanometer CMOS technologies have already become attractive solutions for wireless communication system in 24-GHz, 60-GHz, or even higher frequency. Together with the capability of high-level integration, nanometer CMOS are good candidates to realize high-frequency wireless systems. It has been also demonstrated that CMOS offers great potential to achieve high performance, small chip area, low cost, low power dissipation, and long battery life-time for implementing potable devices. Table 1.1 shows the pros and cons of different technologies which are used for the implementation of wireless systems.

Furthermore, higher quality factor of passive components, like transmission lines and inductors, have been achieved by the thicker metal in the highest metallization layers in the modern RF-CMOS processes, by the micro-electro-mechanical system (MEMS) technology [112]–[115], or even by the gradually developed and matured wafer-level packaging (WLP) technologies [116]–[119].

The development of modern integration technologies is normally driven by the needs of digital CMOS circuit design. The reduction in physical dimensions of the transistors must be accompanied by a proportional reduction in the width of the depletion regions inside the transistor to maintain its basic operation. This can be achieved by an overall increase in the doping concentration of the transistors. However, the higher doping levels increase the electric field inside the transistors and reduce the breakdown voltage of the transistors. Thereby, lower voltage swings and supply voltages are necessary [120]. As

shown in Fig. 1.9, the supply voltage of CMOS decreases rapidly as the sizes of devices shrinks [111]. The supply voltage is 1.8 V for 0.18-μm CMOS. It becomes 1.2 V for 0.13-μm and 90-nm CMOS. In the 65nm/45nm CMOS, the supply voltage becomes 1 V approximately. Although decreased supply voltages do not restrict the design of digital circuits, this brings the difficulties for designing analog and RF circuits in modern sub-micron CMOS process with low supply voltage. This situation would become worse and worse as CMOS technologies continue to scale down [121]. These issues impose significant challenge in terms of circuit design for analog and RF front-ends. Consequently, there is a growing need to explore new low-voltage analog and RF circuit design techniques to overcome afore-mentioned limitations. The current-mode circuit design technique is proposed as one of the promising techniques [121]–[125].

1.2 Review on RF Transceiver Architectures

1.2.1 Receiver Architectures

1) Heterodyne or IF Receivers

The most straightforward receiver architecture for implementing a cellular receiver front-end is evidently the heterodyne receiver [2]–[4], [24], [25], [31], [34], [37], [41]–[43], [51], [57], [65], [69], [70], [72]. The system block diagram is illustrated in Fig. 1.10. The main feature is the use of an intermediate frequency (IF). For this reason, the heterodyne is often also called the IF receiver.

The received RF signals from the antenna are firstly filtered by a band select filter, BPF_{RF1}, which suppresses interferences residing outside of the application band. By removing these out-of-band blocking signals which could saturate the following stages, the required dynamic range of the receiver can be relaxed considerably. A LNA amplifies the received RF signals which are then filtered by an image-reject filter, BPF_{RF2}, to remove the image. The image has an offset of twice the intermediate frequency by the mixer. The received RF signals after BPF_{RF2} are down-converted to IF by the down-conversion mixer, and then passed through the channel-select filter BPF_{IF} to remove the interferences at the adjacent channels. Finally, the channel-selected signal is demodulated

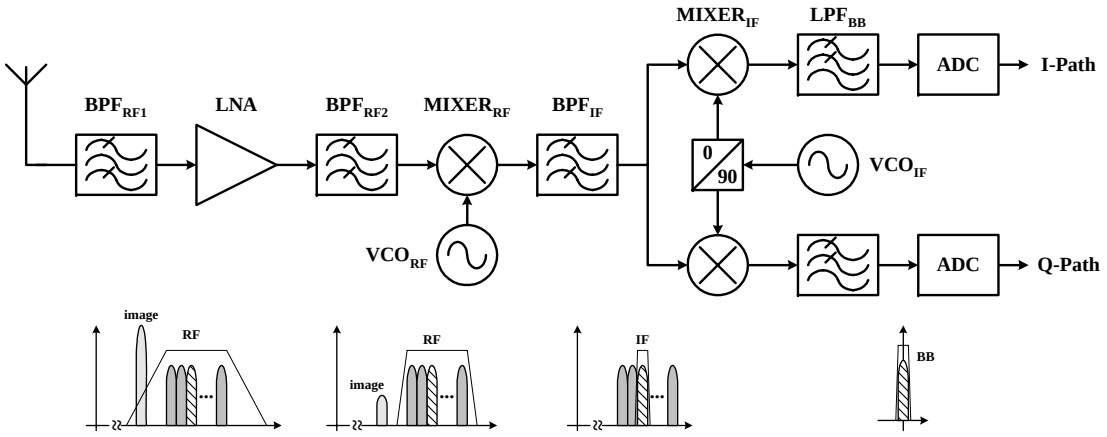


Figure 1.10 Block diagram of the heterodyne or IF receiver.

into baseband I/Q signals to retrieve the desired signal information. The high-frequency noise and distortion from intermodulation and high-order harmonics are removed by the baseband low-pass filter LPF_{BB}.

In the frequency translation, both the desired signal and image signal are mapped to the IF frequency after mixing. Although the image-reject filter BPF_{RF2} is used to attenuate the image signal, suitable attenuation of the image may not be practical unless the IF frequency is selected relatively high. The trade-off is that filtering at a high IF requires more complicated filters in order to maintain selectivity. It is difficult to realize an on-chip high-Q filter at the RF frequency. The required high-Q high frequency image-reject filter is therefore placed off-chip. Consequently, the integration ability of the heterodyne or IF receiver is limited, and the cost is increased because of several off-chip filters are needed. Additional buffers to drive off-chip filters also require high power and reduce the gain of this kind of receivers.

The path mismatch is not a big issue because the image rejection does not rely on any matching between two signal paths, but is mainly achieved by the image-reject filter. Also LO feed-through and DC offset do not affect the signal quality since the desired signal frequency is never close to these frequencies. The same applies to the self-mixing of either

RF or LO signal. Another important property is that the channel selection occurs before the ADC. Hence, the ADC only requires to handle minimum dynamic range. Due to the bandpass nature of the channel, even the sub-sampling ADC can be used. Additionally, the number of bits can be kept low since both the out-of-band and in-band blocking signals have already been removed.

Regarding the integration capability, it is clear that the heterodyne or IF receiver is not a good solution because this topology probably never get rid of the external high-Q filters. Hence, a sense of realizing a full CMOS implementation to achieve low cost is raised. Furthermore, such kinds of receiver do not effectively exploit the power of digital signal processing which is the core competence of CMOS.

2) Direct-Conversion (Homodyne, Zero-IF) Receiver

The direct-conversion (homodyne, zero-IF) receiver (DCR) has the advantage of high integration capability [7], [10]–[13], [15], [16], [21]–[23], [26], [32], [33], [35], [39], [40], [44]–[49], [52]–[56], [68], [71]. As shown in Fig. 1.11, both BPF_{RF2} and IF components are not required in the DCR, and this helps for the integration. The desired RF signal is directly down-converted to zero-IF in one-step frequency mixing with single LO signal. Therefore, in this type of the receiver, the LO frequency is nearly equal to the RF frequency. The baseband signal is then filtered with a low-pass filter to select the desired channel.

For frequency- and phase-modulated signals, the down-conversion must provide quadrature outputs to avoid the loss of signal information. The main advantage of DCR is that it does not possess the image problem when the incoming RF signal is directly down-converted to baseband without any IF stage. Another advantage is its simple architecture. However, the major disadvantage is DC offsets. As shown in Fig. 1.12, the severe DC offsets can be generated at the output of the mixer when the leakage from the local oscillator VCO_{RF} is self-mixed with LO signal. The second source of DC offsets is the large nearby interferers leaking to the VCO_{RF} and then self-mixing. The generated DC offsets could saturate the following stage. The DC offsets can be removed by capacitive coupling. However, the signal power near DC could be lost. Hence, the size of capacitors should be chosen quite large. Feedback loops from the baseband or the digital part are

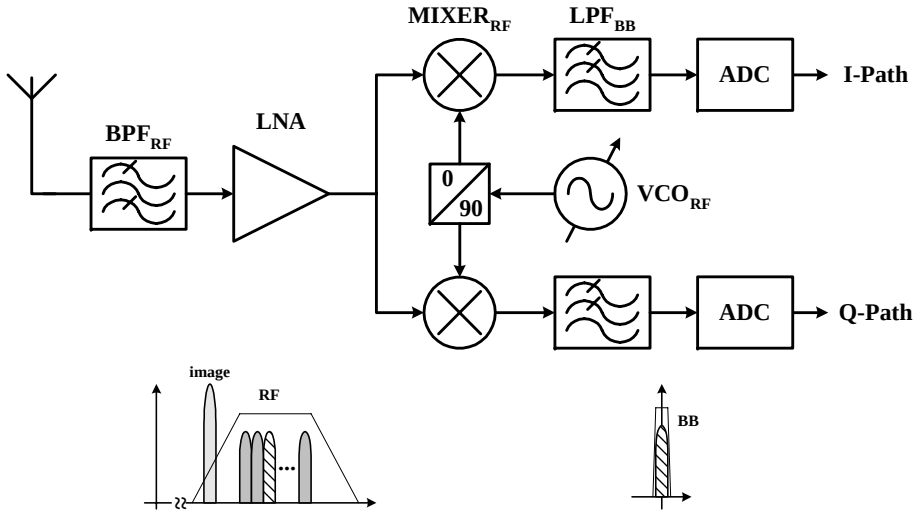


Figure 1.11 Block diagram of the homodyne, direct-conversion, or zero-IF receiver.

also proposed to reduce the DC offsets. But these methods increase the complexity of the DCR.

Equally critical is the flicker noise of the mixer since the mixer output is the baseband signal and can be easily corrupted by large noise. It is because that the flicker noise of active devices becomes the dominant noise source as the frequency below 1 MHz. The flicker noise should be considered in designing DCR. Active devices with large dimension can be chosen to reduce flicker noise. In addition, PMOS contributes less flicker noise than NMOS.

So far, some 24-GHz CMOS receiver front-ends have been proposed in [51]–[57],[65]. Among them, [51], [57], [65] adopts the heterodyne receiver architectures. The RF signal at 24 GHz is down-converted to the IF frequency of around 5 GHz in [51], [57]. In [52]–[56], the direct-conversion receiver architecture has been adopted. In [52], [53], sub-harmonic mixers are adopted to overcome the design issues of dc offsets from self-mixing in the conventional direct-conversion receiver. Moreover, this mixer topology does not consume any dc power and, hence, is ideally avoid of $1/f$ noise. In addition, it does not have any dc offset under ideal conditions owing to its subharmonic mixing function. In [55], the direct-conversion receiver adopts the phased-array receiver architecture

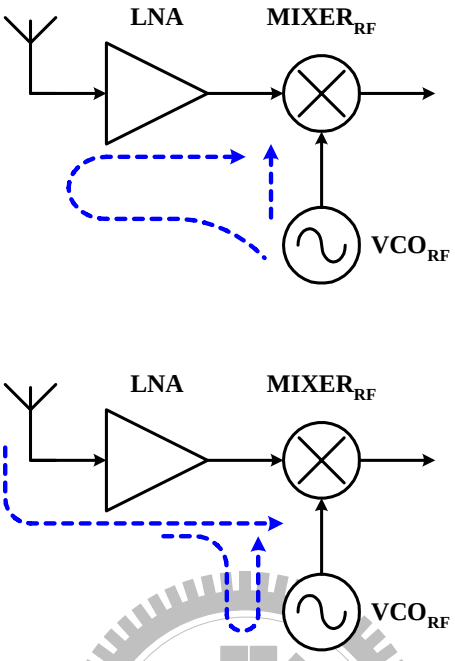


Figure 1.12 Two sources of DC offsets in the direct-conversion receiver.

in its RF domain. After the 4 channels are combined, the RF signal is directly down-converted to the baseband. The phased-array systems have the advantage of improved spatial selectivity and spectral efficiency. These systems are good solution for broadband communications.

1.2.2 Transmitter Architectures

1) Direct-Conversion Transmitter

The direct-conversion transmitter, shown in Fig. 1.13, is attractive because of its simplicity of the signal path [2], [4], [13], [16], [17], [21], [22], [28], [29], [32], [33], [35], [37], [39], [41], [44]–[46], [48], [49], [62]. The IF signals are modulated and up-converted to RF in a single step by the quadrature modulator. The RF signal then amplified by the following PA. After the PA, the bandpass filter BPF_{RF} is typically needed to meet the spectral mask requirements. A single RF frequency synthesizer provides the LO signal and performs channel selection.

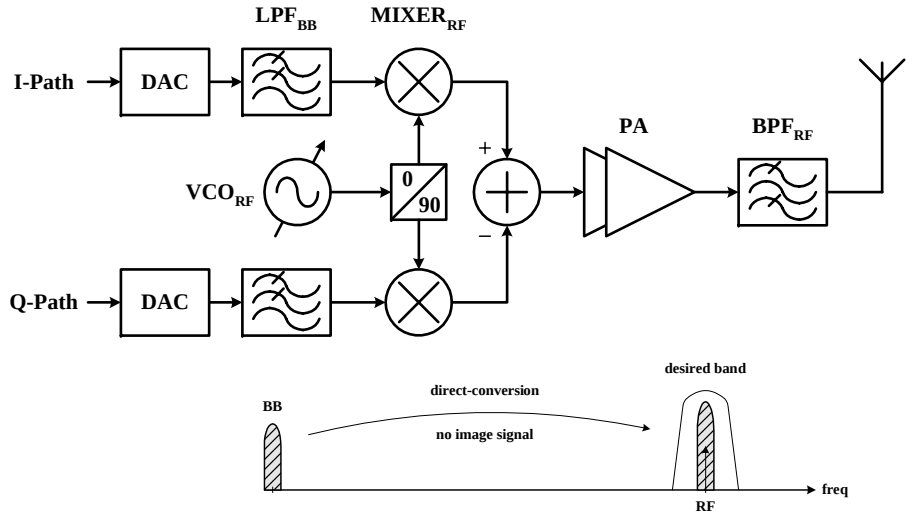


Figure 1.13 Block diagram of the direct-conversion transmitter.

The performance of a direct-conversion transmitter is typically limited by two factors. Firstly, this architecture requires quadrature LO signals like all quadrature modulators. Quadrature generator at RF frequency is less accurate than at lower frequency. Hence, the modulation accuracy of the direct-conversion transmitter is reduced by this effect. The other limitation to the performance of direct-conversion transmitter involves the inter-modulation in the PA. When the baseband signals mixed with the LO signals, harmonics of the LO are generated. These harmonics are inherent to switching mixers. The harmonics generate copies of the baseband signals which intermodulate in the PA and reduce the modulation accuracy. The phenomenon is shown in Fig. 1.14. The spectrum before the non-linear PA includes the desired signal located at the sum of the LO and baseband frequencies, and an undesired signal located at one baseband frequency below the third harmonic of the LO frequency. The third-order intermodulation of two tones f_1 and f_2 results in new tones located at $(2f_2 - f_1)$ and $(2f_1 - f_2)$. In this case, the distortion component closed to the RF output is given by

$$(3f_{LO} - f_{BB}) - 2(f_{LO} + f_{BB}) = (f_{LO} - 3f_{BB}) \tag{1.1}$$

where f_{LO} is the frequency of LO signal and f_{BB} is the frequency of baseband signal. This distortion component, located three baseband frequency below the LO frequency, could

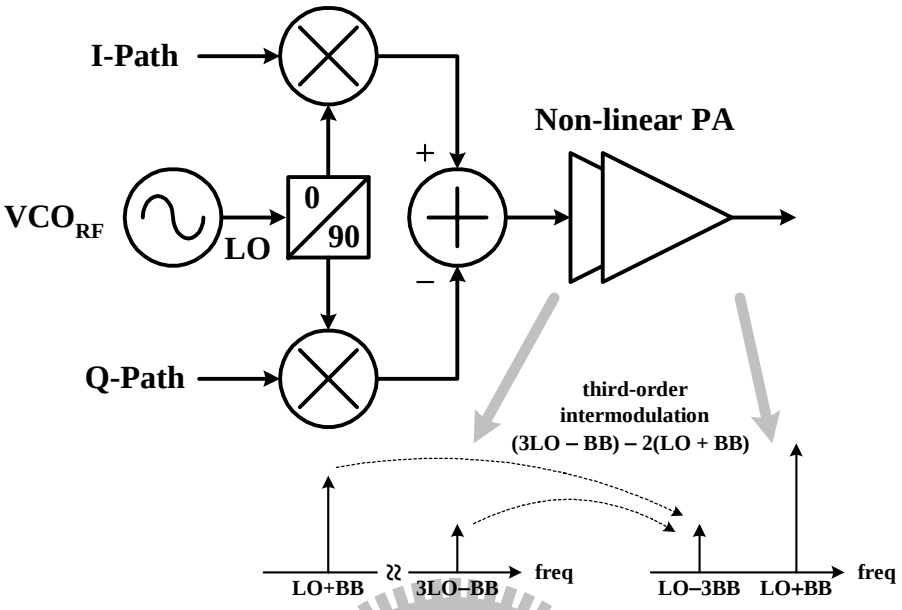


Figure 1.14 Third-order intermodulation by a non-linear PA in a direct-conversion transmitter.

lead to modulation error and spectra mask violations. As a result, the filter before the PA is often needed to attenuate the signals before intermodulation occurs in the PA. However, the need for this filter often requires a discrete component and is thus not amenable to a single chip integration solution.

Because the RF frequency is the same as LO frequency in direct-conversion transmitter, another potential problem for this architectures is the LO Pulling which is illustrated in Fig. 1.15. Although the simplicity of direct-conversion transmitter is attractive for integration, all circuit blocks are located on the same substrate and it is a very challenge task to achieve sufficiently high isolation, especially for the on-chip PA. The large modulated signals after the output of PA could interfere with other sensitive analog circuits by coupling through the silicon substrate. A particular problem occurs when the PA as well as VCO runs at a frequency close to each other.

One method to reduce LO Pulling involves using two oscillators and mixing them to create the LO signal. In doing so, the frequency of the LO is moved away from the frequency of the PA output and thus reduce the LO Pulling. However, additional harmonics

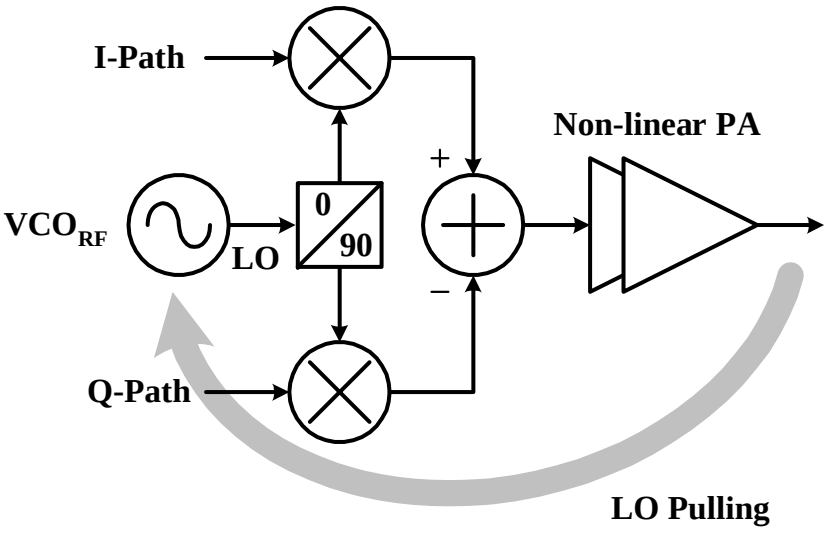


Figure 1.15 LO Pulling in a direct-conversion transmitter.

are generated with this technique that either needs to be filtered or the performance may suffer. The second technique is used in which the output of the VCO is divided and then mixed to create the LO signal. Again, the frequency of LO is changed to reduce the LO Pulling. Yet another method employs multiple phases of LO at lower frequency to perform up-conversion. This method can avoid the LO frequency near the transmitted frequency. Although all of the above mentioned solutions decrease the impact of LO Pulling, they increase the complexity of the transmitter, and thus may diminish the attractive structure simplicity of the direct-conversion transmitter.

In addition to the afore-mentioned issues, other potential issues include the difficulty of power control and the LO feed-through. Because there is no IF stage, all the power control should be performed at baseband or RF. Baseband power control could suffer from very strict linearity requirements on the baseband circuits. Coupling between the LO signal to the RF output is another potential problem due to the high frequency LO used in the quadrature modulator. Although the direct-conversion transmitter has a vey simple circuit and potentially offers for the multi-standard operation, a number of limitations exist. Some of these problems can be alleviated by using heterodyne transmitter with two-step frequency conversion which will be reviewed in the next section.

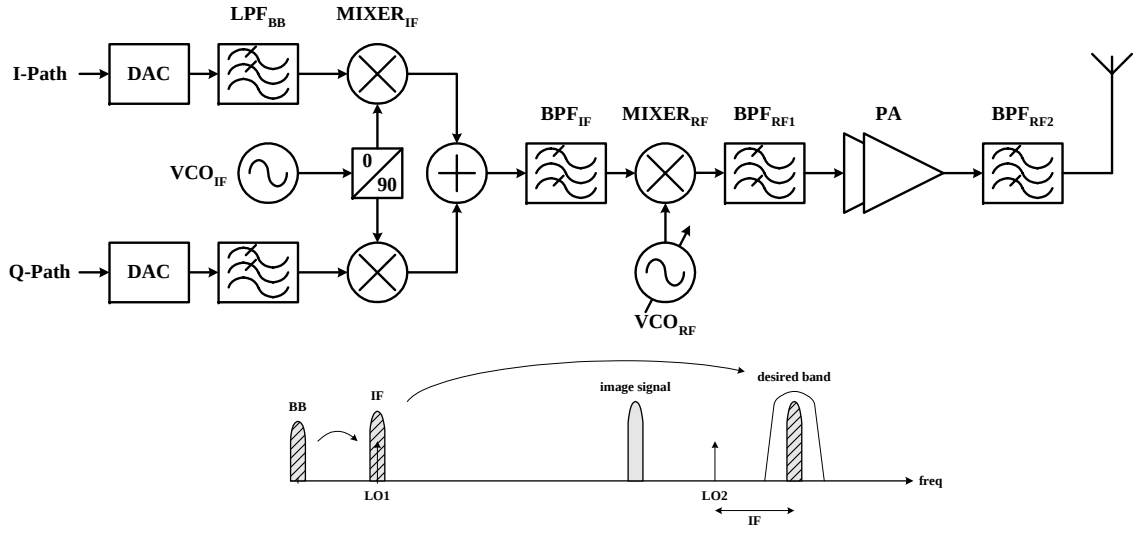


Figure 1.16 Block diagram of the two-step heterodyne transmitter.

II. Heterodyne Transmitter

The heterodyne transmitter which performs two-step up-conversion is widely used topology [24], [25], [31], [34], [37], [42], [43], [58]–[61], [66], [67], [69]. The heterodyne architecture, depicted in Fig. 1.16, uses a quadrature modulator to frequency translate the baseband signal to IF. At this point, an IF bandpass filter BPF_{IF} is needed to suppress the harmonics created by $MIXER_{IF}$. IF signal is then up-converted to RF where the RF bandpass filter BPF_{RF1} is needed to remove the image created by the $MIXER_{RF}$. Finally, the RF signal is applied to the PA and is typically filtered again by BPF_{RF2} to meet the spectral mask requirements. These filters, BPF_{IF}, BPF_{RF1}, and BPF_{RF2}, are typically discrete components that are not amenable to integration on a single CMOS substrate.

The heterodyne transmitter has a number of performance advantages over direct-conversion approach. It avoids the LO Pulling problem since the up-conversion is performed in two steps, and therefore neither LO is operating at the transmitted frequency. The modulation accuracy in the quadrature modulator is improved since low-frequency quadrature VCO allows for more accurate quadrature generation. In addition, lower fre-

quency of the LO leads to less LO feed-through at the RF output. The issue of third-order intermodulation is also alleviated because the undesired distortion component near $3(f_{LO1} + f_{LO2})$ is attenuated by the bandpass RF filter BPF_{RF1}. The filter requirements can be relaxed by an optimizing frequency mapping. The demands of BPF_{IF} can be relaxed if the IF is chosen in a way that none of the harmonics fall directly in the transmit band. Further, a higher IF will push the image sideband far away from the RF which results in a better image rejection by BPF_{RF1}.

Although the heterodyne transmitter shows promise for higher performance, this structure does have some drawbacks with respect to single-chip integration which may be the advantage of direct-conversion transmitter. This architecture is well suited for multi-standard operation, since heterodyne transmitters are capable of both constant envelop and non-constant envelop modulation schemes. Meanwhile, the heterodyne transmitter is a versatile architecture that allows a large gain control range because the amplification can be distributed to several stages. Hence, if the limitations to integration can be overcome, heterodyne transmitter is a good choice when the target is multi-standard operation on a single CMOS substrate.

Although the direct-conversion transmitter suffers from LO Pulling, LO feed-through, and lower accurate quadrature LO signals, direct-conversion architecture still exhibits several advantages of low power consumption, high integration ability, and low cost. Recently, there has been increasing research interests and efforts on the design of CMOS direct-conversion transmitter.

So far, some CMOS transmitter front-ends operated around 20 GHz have been proposed [58]–[64], [66], [67]. Among them, the direct-conversion configuration has been adopted in [62] for the consideration of low-power consumption. The dual-conversion transmitter is the most popular configuration and has been adopted in [58]–[61], [66], [67]. For the application of general purpose, [58]–[62], [67] have proposed CMOS transmitters in 24-GHz ISM band, where on-chip dipole antenna has been integrated in [61] to avoids high frequency wired I/O, thus eliminating the losses associated with RF chip-to-PC-board and transmission line connections. [66] has proposed a CMOS transmitter in 17-GHz ISM band. In [63], [64], the 24-GHz CMOS transmitter has been designed for automotive short-range radar (SRR) applications.

1.3 Review on CMOS RF Building Blocks

1.3.1 Voltage-Mode Down-Conversion Mixer

Down-conversion mixers are required for the frequency conversion in wireless communication systems, especially in the receiver front-ends [126]. In the past, due to the limited speed of MOSFETs and the low quality factor of the passive devices, the use of CMOS technology is restricted to relatively low operation frequencies. The down-conversion mixers operated above 20 GHz have been mostly implemented by GsAs-based HEMT, HBT, and SiGe/BiCMOS processes. Nevertheless, over the last years, the speed gap of CMOS devices to III/V and SiGe technologies has been significantly decreased by aggressive scaling of the transistors [111]. This has made it possible to design the down-conversion mixers operated above 20 GHz with the advanced nanometer CMOS devices.

So far, some down-conversion mixers have been proposed to investigate the operation feasibility at around 20 GHz [51]–[54],[56],[57],[65],[68],[70],[71],[127]–[132]. Among them, the Gilbert mixer has been adopted in [51],[54],[56],[57],[65],[68],[70],[71],[127]. The current-bleeding technique has been applied to the Gilbert mixers to achieve higher conversion gain [56], [71]. With current-bleeding method, the switching transistors can be operated at lower gate-to-source voltage with smaller size.

In addition to the Gilbert mixers, sub-harmonic mixers (SHMs) have also been investigated in the operating frequency around 20 GHz [52], [53], [128]–[132]. The burden of designing a LO at high frequencies can be alleviated by the SHM topology. Because the LO frequency is a sub-harmonic of the RF frequency, this alleviates the DC-offset due to the LO–RF feedthrough. Furthermore, the Gilbert mixer requires high dc power consumption for the specific conversion gain and speed. Therefore, the passive SHM without dc power consumption becomes an attractive candidate for high frequency applications. There are mainly two different techniques which are known for sub-harmonic down-conversion mixers: 1) exploiting the non-linear behavior of active devices to produce higher harmonics of the LO waveform [131], [132] and 2) multiplying the received signal with a number of uniformly spaced LO phase [52], [53], [128]–[130]. While the type 1) mixers have a penalty in conversion gain and noise, the type 2) mixers have per-

formance similar to the Gilbert mixers at the expense of a more complex LO generation circuits.

1.3.2 Voltage-Mode Up-Conversion Mixer

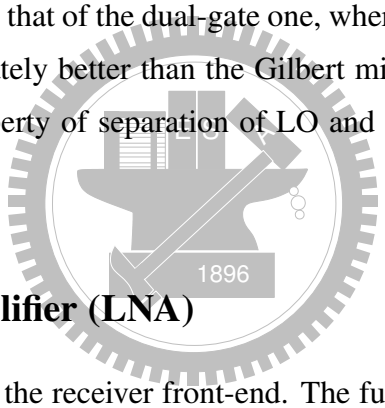
As down-conversion mixers which are described in the prior paragraph, up-conversion mixers are required for the frequency conversion in wireless communication systems, especially in the transmitter front-ends [126]. The up-conversion mixers operated above 20 GHz have been mostly implemented by GsAs-based HEMT, HBT, and SiGe/BiCMOS processes. Nevertheless, over the last decade, the significant improvement of CMOS devices into nanometer nodes has made the speed of the CMOS devices comparable to the devices in SiGe/BiCMOS and III-V technologies [111]. This has made it possible to design the up-conversion mixers operated above 20 GHz with the advanced nanometer CMOS processes.

So far, little has been done to investigate the feasibility of implementing CMOS up-conversion mixers for such a frequency range around 20 GHz [58]–[61], [66], [67], [133], [134]. Among them, the CMOS Gilbert mixer has been adopted in [58]–[60], [66], [67], [134]. In the Gilbert mixer, the LO signal at the drain of differential pairs is ideally zero, and the mixing is caused by the switching action of LO switching transistors between the cutoff and saturation region. Hence, the switching behavior of the LO switching transistors is quite important. To minimize the period of LO switching transistors into linear region, the current-bleeding technique can be used to enhance the switching speed. In [58]–[60], [67], the current-bleeding technique has been applied to the up-conversion Gilbert mixer to enhance the conversion gain and make the switching transistors operate faster with lower gate-to-source voltages and smaller sizes.

The input of the Gilbert mixer is actually a voltage-to-current stage. While the non-linearity in the switching operation is necessary for frequency translation, a distortion of the drain current caused by the transconductance stage is highly unwanted. This distortion deteriorates the compression and intermodulation characteristic of the up-conversion Gilbert mixer. The transconductance stage in [66] is with resistive source degeneration to enhance its linearity performance.

The CMOS dual-gate up-conversion mixer has been proposed in [133], where the dual-gate structure is realized using a cascode connection of two single-gate n-type MOSFETs for which relatively accurate simulation models are available. In a dual-gate mixer, a finite LO signal must be preset at the drains of lower transistors, which cause the change of drain-to-source voltages. This leads to the switching of the devices between linear and saturation regions. Due to this, the transconductance of the lower transistors is modulated by the LO frequency.

In the Gilbert mixer, the transconductance stage is primarily biased in the saturation region, whereas in a dual-gate mixer, the lower FETs are operated in the linear region during the most part of the LO cycle, resulting in lower transconductance than that of an FET biased in the saturation region. As a result, the conversion gain of the Gilbert mixer is normally higher than that of the dual-gate one, whereas the linearity performance of dual-gate mixer is moderately better than the Gilbert mixer. Both of these two kinds of mixers have inherent property of separation of LO and RF ports, which makes them amenable for integration.



1.3.3 Low Noise Amplifier (LNA)

LNA is the first circuit in the receiver front-end. The functions of LNAs are not only to amplify RF signals but to contribute as minimum noise as possible to enlarge the power difference between the received signal and noise. Considering the noise contributions in LNA design, channel thermal noise and induced gate current noise are the main sources of noise in MOS devices [126], [135]. The thermal noise occurs because of channel resistance, whereas the induced gate current noise results from the fluctuating channel charges that induce a physical current towards the gate by capacitive coupling.

Recently, the rapid development of Si-based CMOS technologies has made the realization of low-cost and high-integration RF integrated circuits at frequencies above 20 GHz feasible [111]. So far, numerous CMOS LNAs designed for the frequencies around 20 GHz have been reported [51]–[57], [65], [136]–[152]. Among them, the single-ended structure has been used in [51], [52], [54]–[57], [136]–[140], [142]–[145], [147], [148], [150], [151], whereas the differential topology has been adopted in [53], [57], [141], [146],

[149], [152]. Generally, the single-ended structure has the advantage of good NF and low-power consumption. Although the differential configuration provides the immunity to common-mode noise from power supply, it dissipates more power consumption than single-ended configuration.

To achieve simultaneous noise and input impedance matching, common source amplifier configuration with the inductive source degeneration at the input stage is used in [52]–[54], [56], [57], [136]–[138], [140], [142], [143], [145]–[152]. The csccode amplifier configuration is mostly used to achieve better reverse isolation due to reducing the Miller effect [52], [53], [65]. The common-gate input stage topology has been adopted in [51], [55], [139]. The transistor is sized for the common-gate stage to achieve a near simultaneous power and noise match. To enhance the amplifier gain, the multi-stage configuration has been adopted in [51], [52], [54]–[57], [136]–[138], [140], [141], [144]–[149], [151], [152]. But multi-stage amplifiers will consume more power and lose some linearity performance.

1.4 Review on CMOS RF Current-Mode Circuits

As CMOS technologies reach the scale of nanometer or deca-nanometer nodes, the supply voltage is gradually reduced accordingly to around 1 V or less owing to the consideration of reliability of CMOS device. The reduction in the supply voltage of modern digital CMOS technologies originated by the aggressive downscaling of MOS devices has many prominent effects on the characteristics of monolithic CMOS circuits including high packing density, small device parasitics, high device speed, and low power consumption. In the same time, the threshold voltage Vth of CMOS is also reduced and becomes lower than 0.5 V [111], [121]. As shown in Fig. 1.17, the supply voltage and threshold voltage are reduced in accordance with the scaling of channel length of CMOS technologies. Unlike the supply voltage, the threshold voltage of MOS devices, however, is reduced at a rather slower pace, and is mainly constrained by the sub-threshold conduction. Consequently, this leads to smaller voltage headroom left for the analog and RF circuits designed in nanometer CMOS technologies. The dynamic range left for RF and analog circuits is decreased. Besides, small effective gate-to-source voltage and low

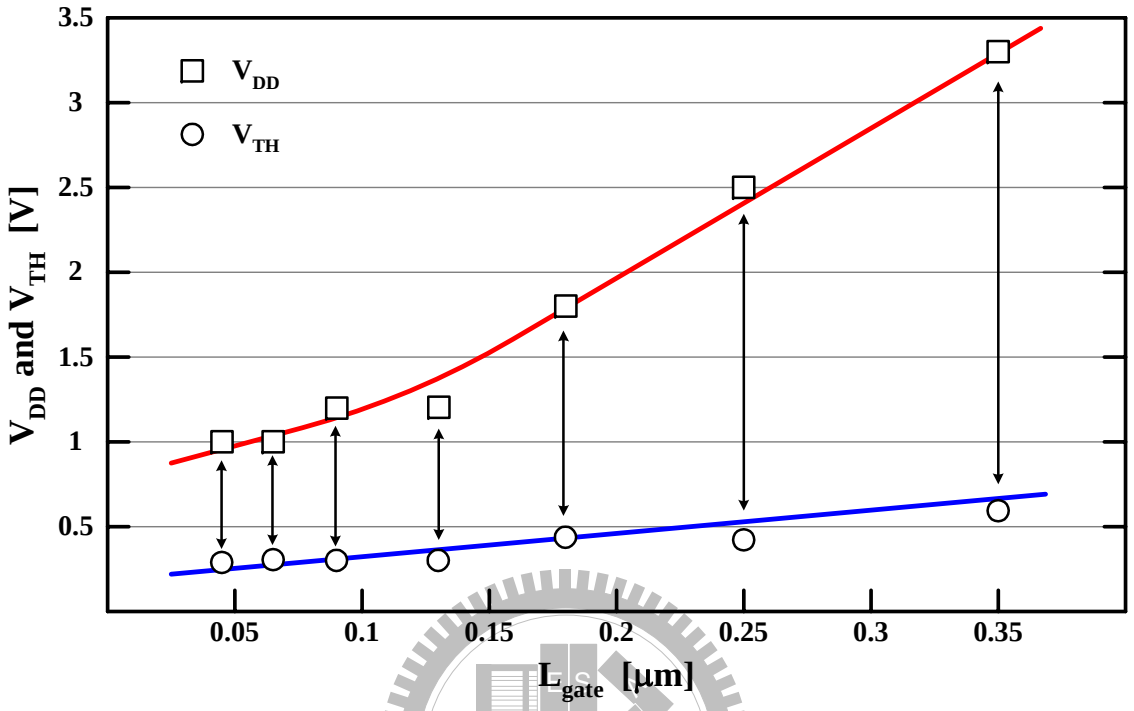


Figure 1.17 The reduction of supply voltage and threshold voltage in accordance with the scaling of channel length of CMOS technologies.

device output impedance also critically affect the performance of analog and RF CMOS circuits [111], [121]. The situation will become worse and worse as CMOS technologies continue to scale down. It is because that the voltage-mode circuits in general require large voltage signal swings to keep signal information. The reduction of voltage headroom in nanometer CMOS technologies affects conventional voltage-mode analog and RF CMOS circuits more. Although the effective technique of reducing power dissipation of the wireless communication systems is to decrease the supply voltage, the benefit is mainly from digital circuits. In analog and RF CMOS circuits, performance degradation caused by the aggressive reduction of the supply voltage of modern CMOS technologies becomes a critical challenge. Therefore, analog and RF CMOS integrated circuits that are capable of operating at low supply voltage have become an important consideration.

Take voltage-mode circuits into consideration, the impedances of internal nodes are

generally large so that signal information can be mostly carried with the time-varying voltage signals. Since a large voltage swing is required to keep signal information in voltage-mode analog and RF circuits, conventional voltage-mode analog and RF circuits gradually face the problem of insufficient voltage headroom. It becomes difficult to design conventional voltage-mode analog and RF circuits in reduced voltage headroom under low supply voltage. Furthermore, when signals are distributed as voltage in voltage-mode circuits, the parasitic capacitances are charged and discharged with the voltage swing as large as possible, which limits the speed and increase the dynamic power consumption. Consequently, different analog and RF circuit topologies, design techniques, and operational principles need to be explored to overcome such limitations in nanometer CMOS technologies.

One procedure for finding alternative, preferably simpler, circuit realizations is to use current signals rather voltage signals for signal processing. MOS transistors in particular are more suitable for processing currents rather than voltage signals because the output signal is current both in common-source and common-gate amplifier configurations. When the signal is conveyed as a current, the voltages in MOS circuits are proportional to the square-root of the signal, if saturation region operation is assumed for the device. Therefore, a compression of voltage signal swing and a reduction of supply voltage are possible.

In current-mode circuits, the impedances of internal modes are in general smaller than those in voltage-mode circuits, the voltage swings at the internal nodes become smaller and the signal information is then mainly carried with the time-varying current signals. Consequently, current-mode circuits can be easily designed under small voltage headroom. Besides, as the signals are distributed as current in current-mode circuits, the parasitic capacitances are not required to charged and discharged with large voltage swings, which can therefore improve the speed of circuits and decrease the dynamic power dissipation. Moreover, when dealing with signal processing, it is easy to perform function of summation by simply connecting the signal paths together without additional amplifiers; thus, the power consumption can be further reduced. With the above advantages, current-mode analog and RF circuits are capable of operating in low supply voltage and dissipating smaller power. The current-mode design techniques have great potential in

the design of CMOS RF front-end circuits in the advanced nanometer or deca-nanometer CMOS technologies.

So far, some CMOS current-mode circuits in analog front-ends have been proposed in [121]–[125], [153]–[160]. Among them, current-mode circuits have found increasing applications in multi-Gbps wire-line data communications. The most challenge block in the wire-line systems is the front-end, also known as the preamplifier, arising from the stringent requirement on both the noise and bandwidth. In [121], [122], CMOS high-frequency wide-bandwidth current-mode preamplifiers have been proposed. These preamplifiers have the advantage of low-voltage and low-power operation. In [121], [122], the design and analysis of CMOS current-mode amplifiers are discussed. A positive transformer feedback LNA fabricated in 0.13-μm CMOS has been proposed in [123]. With the current-current feedback around a common gate stage with an integrated transformer, the wide-band input matching (avoiding any resonant network) can be provided, and a current gain greater than one through the positive transformer feedback can also be achieved. This LNA has been applied into a current-mode receiver front-end operated at 4 GHz.

Moreover, a 2-GHz current-mode self-switching up-converter with a 1-V supply has been proposed in [153]. The mixer is fabricated in 0.13-μm CMOS. It has a large conversion gain of +6.7 dB, and a good output 3^{rd}-order intermodulation intercept point (P_{OIP3}) of +6.5 dBm. The current-mode self-switching mixer requires very small LO input power of –15 dBm. A 0.13-μm CMOS 24-GHz current-mode PA has been proposed in [154]. This PA has achieved large output power with high PAE in the 24-GHz frequency range. Besides, the PA is capable of operating in the low supply voltage of 1.2 V. The 0.13-μm CMOS *K*-band current-mode CMOS receiver front-end [155], the 0.13-μm CMOS 24-GHz CMOS current-mode transmitter front-end [62], and the 0.13-μm CMOS *K*-band CMOS current-mode up-conversion mixer [160] have been proposed. The concept of current-squaring is used to realize the up-conversion and down-conversion mixer in [62], [155] [160]. These circuits have the advantages of low supply voltage and low power consumption.

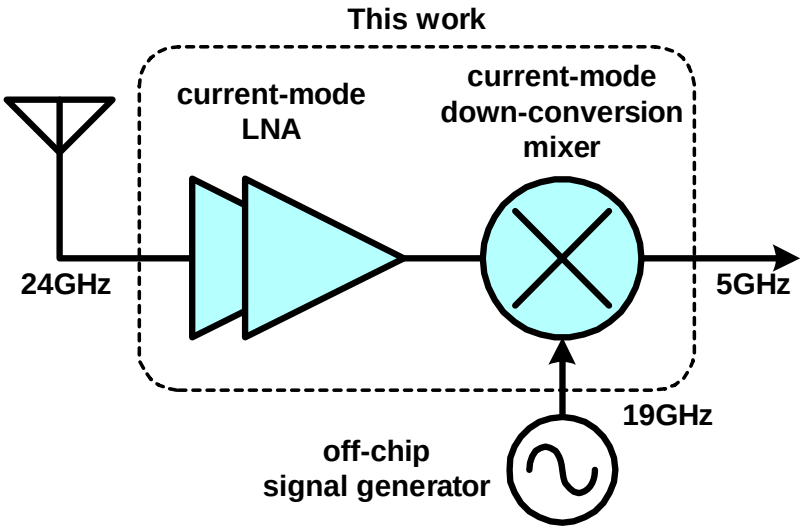


Figure 1.18 The proposed K-band receiver front-end integrated with newly current-mode down-conversion mixer.

1.5 Research Motivation

It is the aim of this dissertation to investigate the new design methodology to the CMOS RF integrated circuits to overcome the reduced voltage-headroom in the low supply voltage in the advanced CMOS technologies. The current-mode design methodology has been discussed the feasibility to realize K-band down-conversion and up-conversion mixers. As shown in Fig. 1.18 and Fig. 1.19, the newly designed CMOS current-mode down-conversion mixer has also been integrated in the CMOS K-band receiver front-end with a LNA. Moreover, the proposed new CMOS current-mode up-conversion mixer has also been integrated in the CMOS K-band transmitter front-end with a baseband current buffer/repeater, a VCO and a transformer-based VCO buffer/repeater.

In addition to propose the new circuit design techniques to millimeter-wave transceiver front-end circuits, two K-band CMOS low noise amplifiers in 45-nm CMOS technology are also proposed. The two benchmark circuits of K-band CMOS low noise amplifiers are implemented to demonstrate the feasibility of designing millimeter-wave circuits in 45-nm CMOS technology.

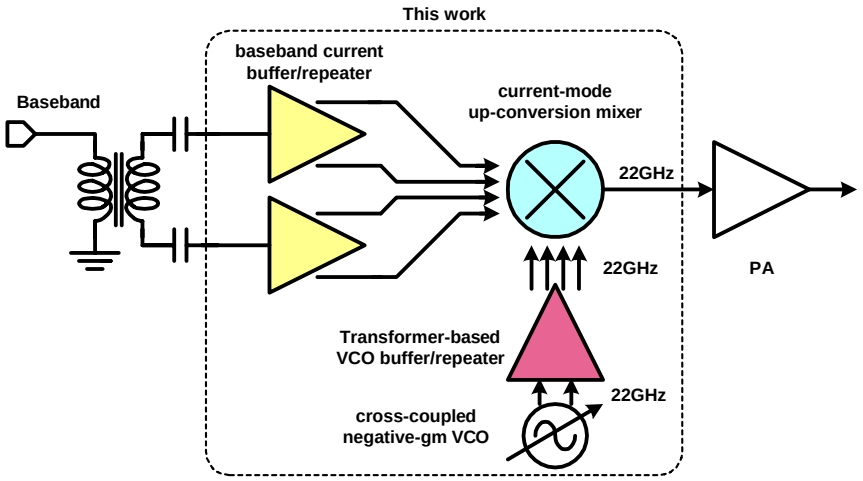


Figure 1.19 The proposed K-band transmitter front-end integrated with newly current-mode up-conversion mixer.

1.6 Organization of This Dissertation

This dissertation contains six chapters, which include analyses, designs, and implementations of CMOS current-mode down-conversion mixer and current-mode up-conversion mixer, a CMOS integrated K-band current-mode receiver front-end circuit, a CMOS integrated K-band current-mode transmitter front-end circuit, and a K-band 45-nm planar bulk-CMOS low noise amplifier with above-IC technologies.

Chapter 1 introduces the background, describes the research motivation, and explains the main topics of this dissertation. Several CMOS RF key building blocks and RF transceiver architectures will be discussed. Moreover,the principle and the advantage of current-mode design techniques of CMOS analog and RF circuits will be discussed, and several published high-frequency CMOS current-mode circuits will also be reviewed in this chapter.

In Chapter 2, a low-power K-band CMOS integrated current-mode receiver front-end circuits has been proposed, analyzed, and implemented in 0.13-μm 1P8M CMOS technology. The proposed current-mode receiver front-end is of single-balance structure and integrated with a current-mode low noise amplifier and a current-mode down-conversion mixer. In the proposed low noise amplifier, two cascaded current-mirror amplifiers are

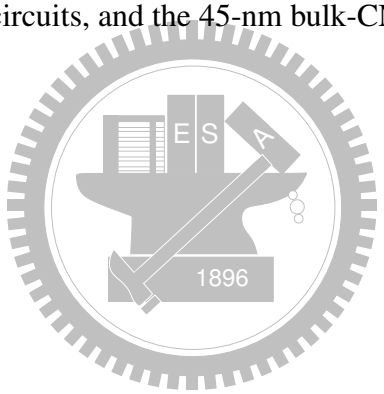
adopted to fulfill the amplification of RF current signal. Following the low noise amplifier is the current-summing circuit to perform the RF and LO current signals. The summed signal is sent to the current-squaring circuit to perform the function of current mixing of RF and LO signals. The analyses of the current-mode low noise amplifier and current-squaring circuit is given. The short-channel effects of the current-squaring circuit are investigated. Circuit simulations through Agilent ADS are performed to evaluate the performance of the proposed integrated receiver front-end circuits. Finally, the experimental results are given to verify the circuit performance. It is shown that the current-mode circuit design technique has great potential for low-voltage and low-power CMOS receiver front-end circuits in nanometer CMOS technologies.

In Chapter 3, a low-power K-band CMOS integrated current-mode transmitter front-end circuits has been proposed, analyzed, and implemented in 0.13-μm 1P8M CMOS technology. The integrated current-mode transmitter consists of a current-mode double-balanced up-conversion mixer, a voltage controlled oscillator (VCO), a transformer-based VCO buffer/repeater, and a baseband current buffer/repeater. The proposed current-mode double-balanced up-conversion mixer is composed of four units of analog current-squaring circuit. The body effect and short-channel effects of the proposed current-mode double-balanced up-conversion mixer are investigated. On-chip passive transformers and inductors are designed and extracted through electromagnetic (EM) simulation tool Ansoft HFSS. Circuit simulations through Agilent ADS and Cadence SpectreRF are performed to evaluate the performance of the proposed integrated transmitter front-end circuits. The experimental results are given to verify the circuit performance. The results achieved demonstrate that the proposed current-mode up-conversion mixer offers great potential for the application in low-voltage and low-power CMOS transmitter front-ends in advanced nanometer CMOS technologies.

In Chapter 4, a K-band low noise amplifier with wafer-level packaging (WLP) technology has been proposed, analyzed, and implemented in IMEC 45-nm 1P5M bulk-CMOS process. The WLP technology, which consists of a 5-μm thick electroplated copper layer on an 18-μm low-k dielectric of Benzo-Cyclo-Buthene (BCB), is post-processed on top of the IMEC's 45-nm CMOS process. A one-stage cascode low noise amplifier and a two-stage cascaded cascoded low noise amplifier are realized. The passive induc-

tors and transmission inductors by WLP technology are designed and extracted through electromagnetic (EM) simulation tool Ansoft HFSS. Circuit simulations through Cadence SpectreRF are performed to evaluate the performance of the low noise amplifier. The experimental results are given to verify the performance. The measurement results show that the proposed low noise amplifier in 45-nm planar bulk-CMOS with high-Q above-IC inductors achieves very good performance. It is also demonstrated that the 45-nm planar bulk-CMOS technology has great potential for the design of high performance RF circuits. Furthermore, high-Q passive inductors from WLP technology can provide great benefit to the millimeter-wave circuit designs.

Finally, the main results and conclusions of this dissertation are summarized in Chapter 5. Some suggestions and future works about the implementations of current-mode receiver, transmitter front-end circuits, and the 45-nm bulk-CMOS LNA are also addressed in this chapter.



Chapter 2

Low-Power Current-Mode CMOS *K*–Band Receiver Front-End ICs

It is the aim of this chapter to introduce a new current-mode receiver front-end. The proposed integrated current-mode receiver front-end which is operated in the frequency of K-band has been fabricated in 0.13-μm 1P8M CMOS technology. The proposed receiver front-end is of single-balanced structure and is integrated with a current-mode LNA and a current-mode down-conversion mixer. This work has been published in [155]. In the proposed current-mode LNA, two cascaded current-mirror amplifiers are adopted to realize the amplification of current signals. Following the LNA is the current-mode down-conversion mixer which is accomplished by a current-summing circuit and a current-squaring circuit. The current summing circuit performs the summation of RF and LO signals. The summed signal is sent to the current-squaring circuit to perform the function of current mixing of RF and LO signals.

The measured results have shown that the current-mode receiver front-end exhibits a conversion gain of 11.3 dB, the input-referred 1-dB compression point (IP_{-1dB}) of –13.5 dBm and the input-referred third-order intercept point (P_{IIP3}) of –1 dBm. The measured noise figure (NF) is 14.2 dB at the RF frequency of 24 GHz and LO frequency of 19 GHz. The total power dissipation of this current-mode receiver front-end dissipates 27.8 mW under the condition that the supply voltage of LNA is 0.8 V and the supply voltage of mixer is 1.2 V. Note that the power consumption of output buffer is not included. The

proposed receiver front-end occupies the active area of 1.45 × 0.72 mm^2 where testing pads are included.

This chapter is organized as follows. In Section 2.1, the architecture and operational principles of the proposed 24-GHz current-mode receiver front-end is described. In Section 2.2, circuit designs of current-mode LNA, current-mode down-conversion mixer, and integrated receiver front-end are described. The simulation results are also presented and analyzed in this section. The layout considerations and experimental results are presented in Section 2.3. Finally, the summary is given in Section 2.4.

2.1 Operational Principles

The block diagram of the proposed current-mode 24-GHz receiver front-end is illustrated in Fig. 2.1. The designed receiver front-end circuit is composed of a LNA and a down-conversion mixer. The off-chip signal generator provides the first LO signal for the first-step down-conversion of the receiver. With the first LO signal at 19 GHz, the received RF signal amplified by the current-mode LNA at 24 GHz is down-converted to the IF at 5 GHz by the current-mode mixer. The reason why the IF frequency is set a 5 GHz is that several kinds of RF receiver front-ends are matured at the frequency band of 5 GHz. Such 5-GHz receiver front-ends, the direct-conversion receiver structure (DCR) or the double-quadrature receiver (DQR) structure for examples, can be adopted to realize the second-step down-conversion from IF to the baseband, and channel selection can also be performed by this matured 5-GHz receivers.

The image signal of the first-step down-conversion is at the frequency band of 14 GHz which is far away from the received RF signal at 24 GHz. This image signal can be removed from the off-chip RF pre-select filter BPF_{RF}. Besides, the bandpass current-mode LNA can also provide the rejection of this image signal. To deal with the image signal at the first-step down-conversion, the matured 5-GHz DCR can be used because of this structure inherently has no image problem. Furthermore, the matured 5-GHz DQR can also be used, because the DQR can provide better IRR and is less sensitive to I/Q-imbalances of the second-step down-conversion.

In the design of CMOS LNA, the CMOS current-mirror structure is adopted as the

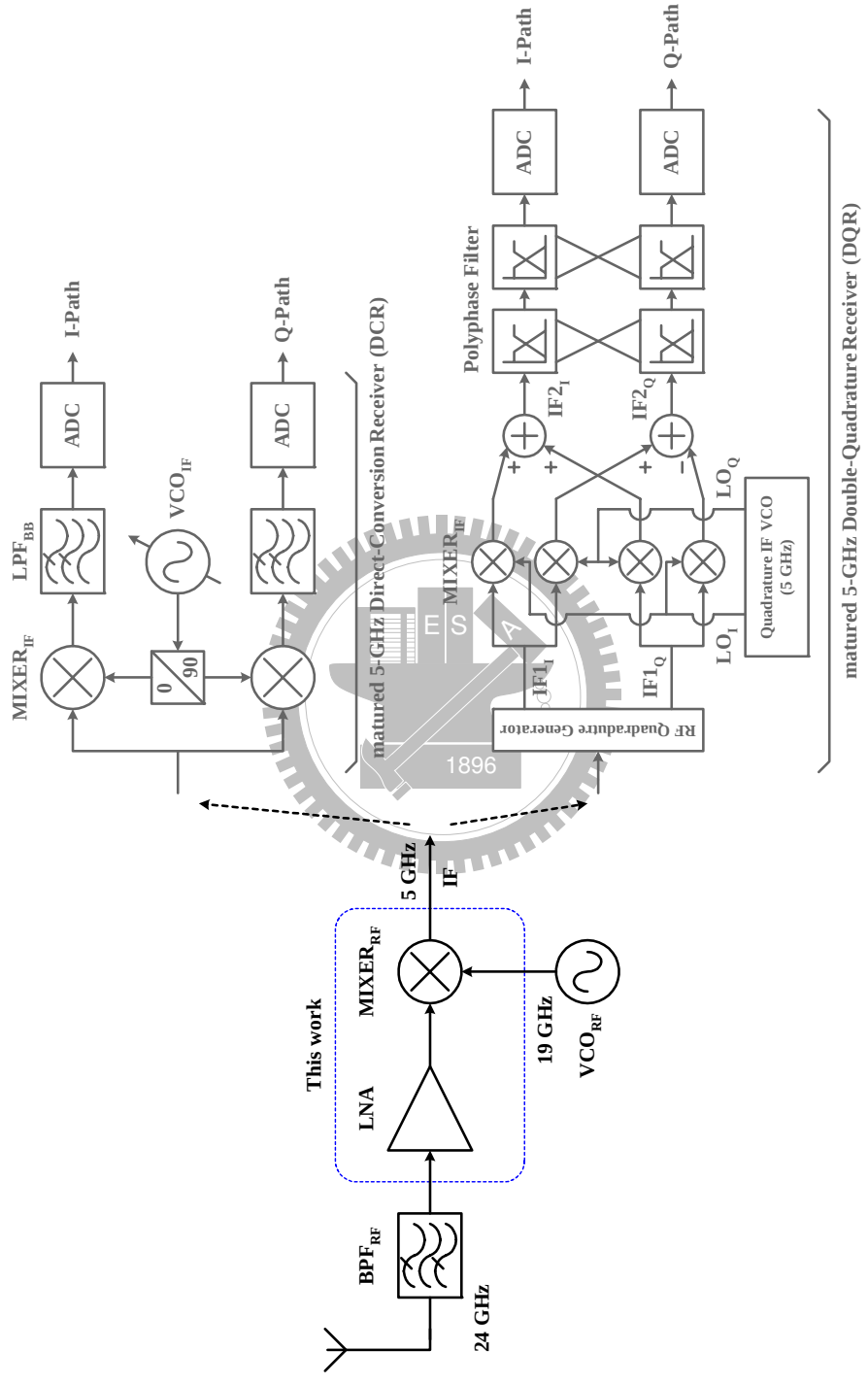


Figure 2.1 The block diagram of the 24-GHz current-mode receiver front-end.

current amplifier and two stages of current-mirror amplifiers are cascaded to provide sufficient gain. As for the current-mode down-conversion mixer, the high frequency analog current multiplier is proposed. It consists of a current summing circuit and a current squaring circuit. Detailed circuit designs and analyses are described in the following section.

2.2 Circuit Designs

2.2.1 Current-Mode Low-Noise Amplifier

The circuit diagram of the proposed two-stage cascaded current-mode LNA is shown in Fig. 2.2 where the first-stage current-mirror amplifier is composed of M_1 and M_2, and the second-stage current-mirror amplifier is composed of M_3 and M_4. All NMOS transistors are operated in the saturation region. The aspect ratio of M_2 is designed M times of that of M_1 whereas the aspect ratio of M_4 is designed N times of that of M_3. Accordingly, the gate-to-source capacitance of M_2 (M_4), C_{GS,M_2} (C_{GS,M_4}, is about M (N) times of gate-to-source capacitance of M_1 (M_3), C_{GS,M_1} (C_{GS,M_3}). To reduce the signal losses at the operating frequency, the inductors L_1–L_3 are chosen as the loads of the current-mode LNA to resonate out the parasitic capacitors C_{T1}, C_{T2}, and C_{T3} at the nodes A_1, A_2, and A_3, respectively, where

$$C_{T1} = (1 + M)\, C_{GS,M_1} + C_{DS,M_1} \tag{2.1}$$

$$C_{T2} = (1 + N)\, C_{GS,M_3} + C_{DS,M_2} + C_{DS,M_3} \tag{2.2}$$

$$C_{T3} = C_{DS,M_4} \tag{2.3}$$

The input ac coupling capacitor C_{IN} and the input pad with the capacitance of C_{PAD1} form the input matching network of the current-mode LNA. C_{OUT} is the capacitor that blocks dc between LNA and the following current-mode mixer. Only the ac current signal $i_{out,LNA}$ is sent to the next stage. L_{GD} is designed to resonate out the gate-to-drain capacitor $C_{GD,M2}$ of M_2 at the operating frequency ω_0 in order to enhance the reverse isolation of the LNA. After resonating out the parasitic capacitances $C_{GD,M2}$ of M_2 between its gate and drain, the transistor M_2 becomes more unilateral such that the stability can be further improved. Because the reverse isolation is high enough when using L_{GD} to resonate out

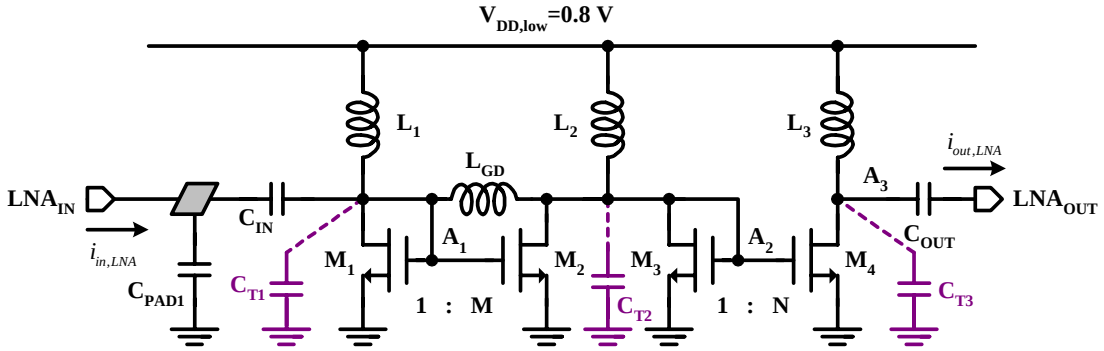


Figure 2.2 The circuit diagram of the proposed two-stage cascaded current-mode LNA at the low supply voltage of 0.8 V.

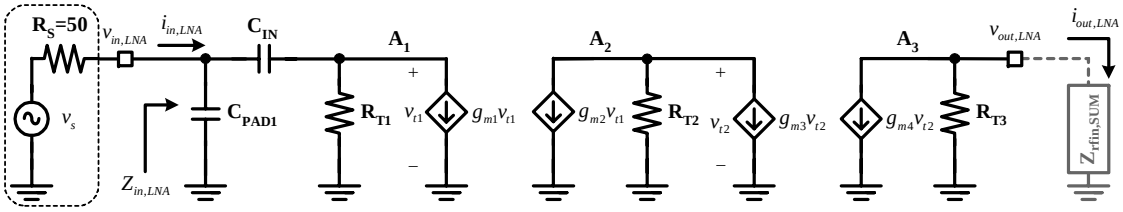


Figure 2.3 The small-signal equivalent circuit of the two-stage cascaded current-mode LNA at the operating frequency of ω_0.

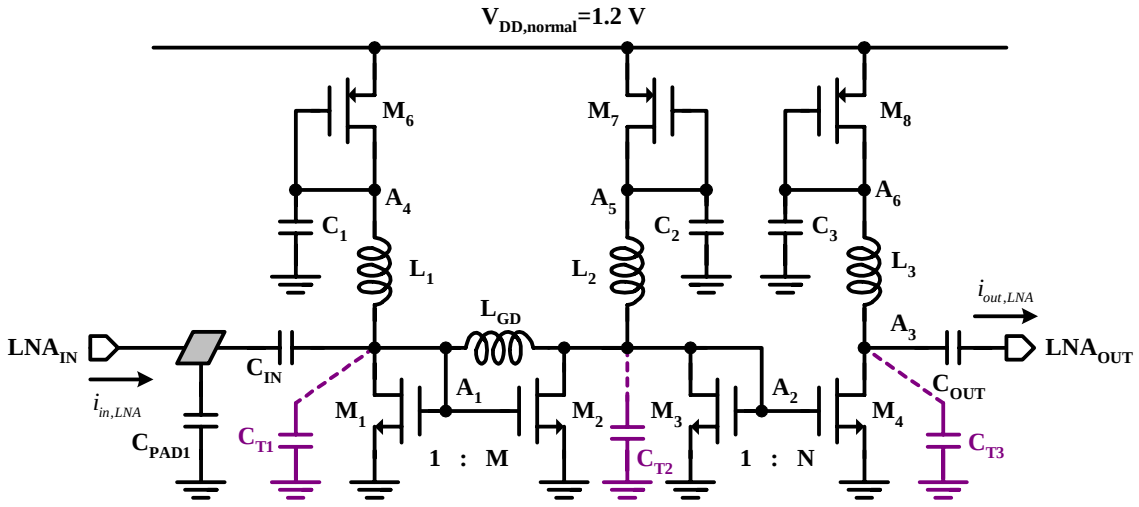


Figure 2.4 The circuit diagram of the proposed two-stage cascaded current-mode LNA at the normal supply voltage of 1.2 V.

the $C_{GD,M2}$, the second-stage LNA will not adopt this method to prevent from the area overhead. Besides, input matching network will not be affected by the following stage because of good isolation, and it will become easier to design.

At the operating frequency ω_0, inductors L_1–L_3 and the respective parasitic capacitors C_{T1}–C_{T3} are resonated. The small-signal equivalent circuit of the proposed current-mode LNA at the operating frequency ω_0 can be depicted in Fig. 2.3 and

$$\omega_0 = \frac{1}{\sqrt{L_1 C_{T1}}} = \frac{1}{\sqrt{L_2 C_{T2}}} = \frac{1}{\sqrt{L_3 C_{T3}}} = \frac{1}{\sqrt{L_{GD} C_{GD,M_2}}} \tag{2.4}$$

$$R_{T1} = R_{p,L_1} \parallel r_{o,M_1} \tag{2.5}$$

$$R_{T2} = R_{p,L_2} \parallel r_{o,M_2} \parallel r_{o,M_3} \tag{2.6}$$

$$R_{T3} = R_{p,L_3} \parallel r_{o,M_4} \tag{2.7}$$

where R_{p,L_1}–R_{p,L_3} are the equivalent parallel resistances of the inductors L_1–L_3. r_{o,M_1}–r_{o,M_4} and g_{m1}–g_{m4} are the output impedance and transconductance of the transistors M_1–M_4, respectively. R_S is the source impedance, and $Z_{rfin,SUM}$ is the input impedance of the following circuit of current-summing circuit. Because the circuit dimensions are much

smaller than the wavelengths involved, the distributed effect of circuits is negligible. Thus the lumped small-signal equivalent circuit is adopted to analyze the circuit behavior.

From Fig. 2.3, the input impedance $Z_{in,LNA}$ in s–domain can be expressed as

$$\begin{aligned} Z_{in,LNA}(s) &= \frac{1}{sC_{PAD1}} \parallel \left[\frac{1}{sC_{IN}} + (R_{T1} \parallel \frac{1}{g_{m1}})\right] \\ &= \frac{(1+g_{m1}R_{T1}) + sR_{T1}C_{IN}}{s\left(C_{PAD1}+C_{IN}\right) + s^2 C_{PAD1}C_{IN}R_{T1}} \end{aligned} \tag{2.8}$$

Let $s = j\omega$, and the input impedance of the LNA $Z_{in,LNA}(j\omega)$ can be calculated as g_{m1}

$$\begin{aligned} Z_{in,LNA}(j\omega) &= \frac{\omega R_{T1}C_{IN}\left[\left(C_{PAD1}+C_{IN}\right) - \left(1+g_{m1}R_{T1}\right)C_{PAD1}\right]}{\omega\left[\left(C_{PAD1}+C_{IN}\right)^2 + \left(\omega R_{T1}C_{PAD1}C_{IN}\right)^2\right]} \\ &\quad -j\frac{\left(1+g_{m1}R_{T1}\right)\left(C_{PAD1}+C_{IN}\right) - \omega^2 R_{T1}^2 C_{IN}^2 C_{PAD1}}{\omega\left[\left(C_{PAD1}+C_{IN}\right)^2 + \left(\omega R_{T1}C_{PAD1}C_{IN}\right)^2\right]} \end{aligned} \tag{2.9}$$

In order to achieve maximum power transfer, the real part of $Z_{in,LNA}$ should be equal to 50Ω at the operation frequency ω_0, and the imaginary part of $Z_{in,LNA}$ can be eliminated at ω_0 if the following equation is satisfied.

$$0 = \left(1+g_{m1}R_{T1}\right)\left(C_{PAD1}+C_{IN}\right) - \omega_0^2 R_{T1}^2 C_{IN}^2 C_{PAD1} \tag{2.10}$$

Thus the relation among C_{IN}, C_{PAD1}, R_{T1}, g_{m1}, and ω_0 can be designed according to the following equation

$$\omega_0 = \frac{1}{R_{T1}C_{IN}}\sqrt{\left(1+g_{m1}R_{T1}\right)\left(1+\frac{C_{IN}}{C_{PAD1}}\right)} \tag{2.11}$$

where ω_0 is defined in (2.4). Substituting (2.11) into (2.9), the real part of $Z_{in,LNA}$ at the operation frequency ω_0 should equal to 50Ω, and can be expressed as

$$Z_{in,LNA}\mid_{\omega=\omega_0} = 50 = \frac{R_{T1}C_{IN}\left[\left(C_{PAD1}+C_{IN}\right) - \left(1+g_{m1}R_{T1}\right)C_{PAD1}\right]}{\left(C_{PAD1}+C_{IN}\right)^2 + \left(\omega_0 R_{T1}C_{PAD1}C_{IN}\right)^2} \tag{2.12}$$

The current gain A_i and voltage gain A_v of the LNA are also calculated when taking the input impedance of the following stage of current-summing circuit $Z_{rfin,SUM}$ into

considerations at the operating frequency ω_0. They can be expressed as

$$\begin{aligned} A_i \mid_{\omega=\omega_0} &\equiv \frac{i_{out,LNA}}{i_{in,LNA}} \mid_{\omega=\omega_0} \\ &= \frac{g_{m2}g_{m4}R_{T1}R_{T2}\left(\dfrac{R_{T3}}{R_{T3}+Z_{rfin,SUM}}\right)}{(1+g_{m3}R_{T2})\sqrt{(1+g_{m1}R_{T1})^2\left(1+\dfrac{C_{PAD1}}{C_{IN}}\right)^2+(\omega_0 R_{T1}C_{PAD1})^2}} \end{aligned} \tag{2.13}$$

$$\begin{aligned} A_v \mid_{\omega=\omega_0} &\equiv \frac{v_{out,LNA}}{v_{in,LNA}} \mid_{\omega=\omega_0} \\ &= \frac{\omega_0 g_{m2}g_{m4}R_{T1}R_{T2}C_{IN}}{(1+g_{m3}R_{T2})\sqrt{(1+g_{m1}R_{T1})^2+(\omega_0 R_{T1}C_{IN})^2}} \cdot \left(R_{T3} \parallel Z_{rfin,SUM}\right) \end{aligned} \tag{2.14}$$

The LNA circuit shown in Fig. 2.2 is designed for low supply voltage of 0.8 V. If the normal power supply of 1.2 V is used, the circuit is depicted in Fig. 2.4. M_6–M_8 with gate shorted to drain are used to reduce the supply voltage to the amplifiers so that the LNA can be biased well and operated at low dc power dissipation. Bypass capacitors C_1–C_3 are used at the nodes A_4–A_6, respectively, to make these three nodes look like ac ground, and in the meanwhile, C_1–C_3 can bypass the supply noise. With M_6–M_8, the dc voltages at the nodes A_4–A_6 are about 0.8 V. The small signal equivalent circuit model of Fig. 2.4 is still the same as Fig. 2.2, and is shown in Fig. 2.3.

The simulated gain, input matching characteristics, and the reverse isolation characteristics of the proposed current-mode LNA is shown in Fig. 2.5(a). The LNA can achieve the maximum simulated gain of 17 dB at the operating frequency of 24 GHz. The simulated NF and NF_{min} of the LNA are depicted in Fig. 2.5(b). This LNA has the simulated NF of 3.4 dB at 24 GHz. Besides, the NF of the LNA is approached to NF_{min} at 24 GHz. The simulation results in 5 process corners are shown in Fig. 2.6(a) and Fig. 2.6(b), which are the simulation results for the circuit depicted in Fig. 2.2 and Fig. 2.4, respectively. The S_{21} is varied from around 17.6 dB to 13.8 dB at the supply voltage of 0.8 V, and is varied from about 18.1 dB to 16.9 dB at the supply voltage of 1.2 V. The linearity performance of the LNA is verified by Harmonic Balance (HB) simulation. With the signal at 24 GHz, the simulated linearity curve which is shown in Fig. 2.7(a) reveals that the IP_{-1dB} is about –24 dBm. With the signals at 23.9 GHz and 24.1 GHz, the simulated

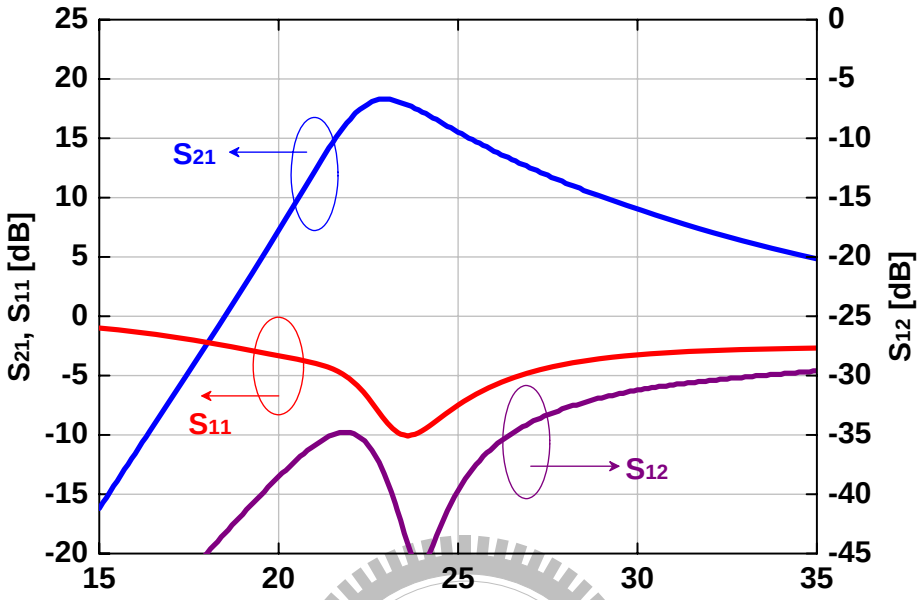
linearity curves which are shown in Fig. 2.7(b) depict a P_{IIP3} of –10.8 dBm. The LNA in Fig. 2.2 drains 20.4 mA from the supply voltage of 0.8 V and drains 34.82 mA from the supply voltage of 1.2 V. The increase in simulated current consumption from 20.4 mA to 34.82 mA is because the gate-to-source voltage of LNA is changed from 0.8 V to 1.2 V as the supply voltage is increased from 0.8 V to 1.2 V. In Fig. 2.3, the gate-to-source voltage of LNA can be kept to about 0.8 V under the supply voltage of 1.2 V, and this LNA drains about 20.4 mA from the supply voltage of 1.2 V.

2.2.2 Current-Mode Down-Conversion Mixer

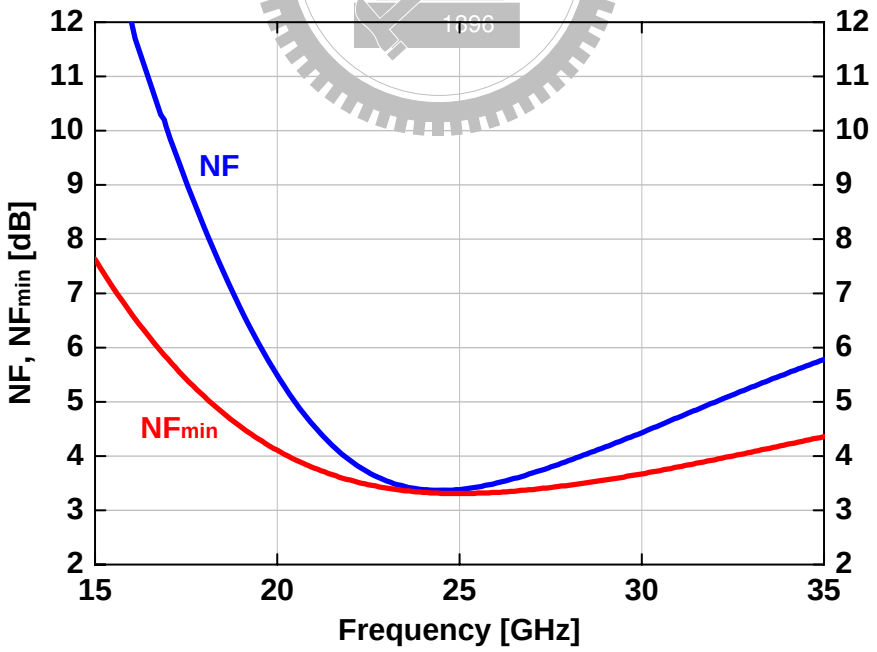
The conceptual block diagram of the proposed current-mode down-conversion mixer is depicted in Fig. 2.8. This mixer is composed of a current summing circuit, a current squaring circuit, and a band-pass filter (BPF). The RF input current signal $i_{LNA} = I_{LNA}\cos\omega_{RF}t$ from the current-mode LNA and the LO input current signal $i_{LO} = I_{LO}\cos\omega_{LO}t$ from the off-chip signal generator are summed through the current-summing circuit. The summed current signal $i_{SUM} = (i_{LNA} + i_{LO}) = (I_{LNA}\cos\omega_{RF}t + I_{LO}\cos\omega_{LO}t)$ is sent to the following current-squaring circuit which results in the square components of i_{LNA}^2 and i_{LO}^2 and the multiplication component $i_{LNA} \times i_{LO}$. The multiplication component of two current signals provides the function of double sideband mixing.

Through the double sideband mixing, the received 24-GHz signal is converted to 5 GHz which is the lower sideband (LSB) and 43 GHz which is the upper sideband (USB) with the LO signal at 19 GHz. Following the current squaring circuit is the bandpass filter (BPF) which is capable of frequency selectivity. In this receiver design, the center frequency of the BPF is designed at 5 GHz so that the targeted LSB can be obtained and the unwanted USB can be attenuated. The detailed operational principles of the current squaring circuit and the current summing circuit are described in the following sub-sections.

The circuit diagram of the current squaring circuit as modified from [161], [162] is shown in Fig. 2.9 where M_{SQ1} and M_{SQ2} are current mirror circuit. The bulk and source of M_{SQ3} are connected together to eliminate the body effect. Assume that both short-channel effect and channel-length modulation effect are negligible, and the MOS transistors M_{SQ1}–M_{SQ3} are well matched with the same channel width/length (W/L). If all

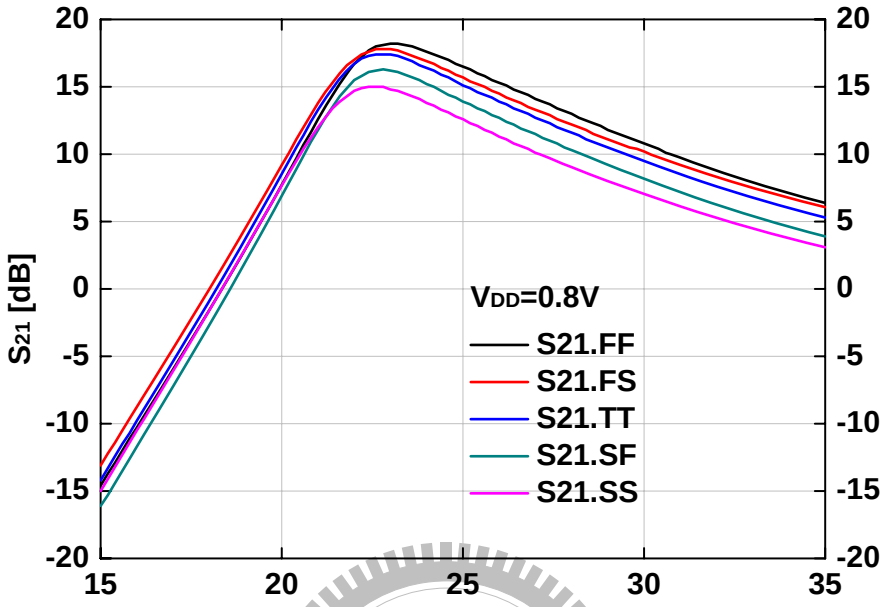


(a)

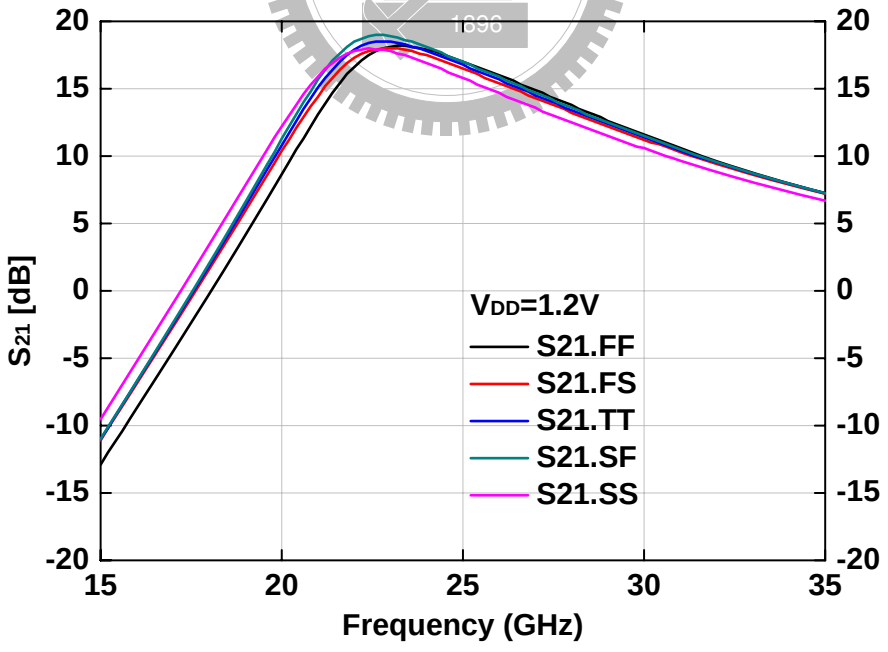


(b)

Figure 2.5 The simulated (a) S-parameters, and (b) NF and NF_{min} of the proposed current-mode LNA.



(a)



(b)

Figure 2.6 The simulated S_{21} of the current-mode LNA in different process corners (a) at the supply voltage of 0.8 V, and (b) at the supply voltage of 1.2 V.

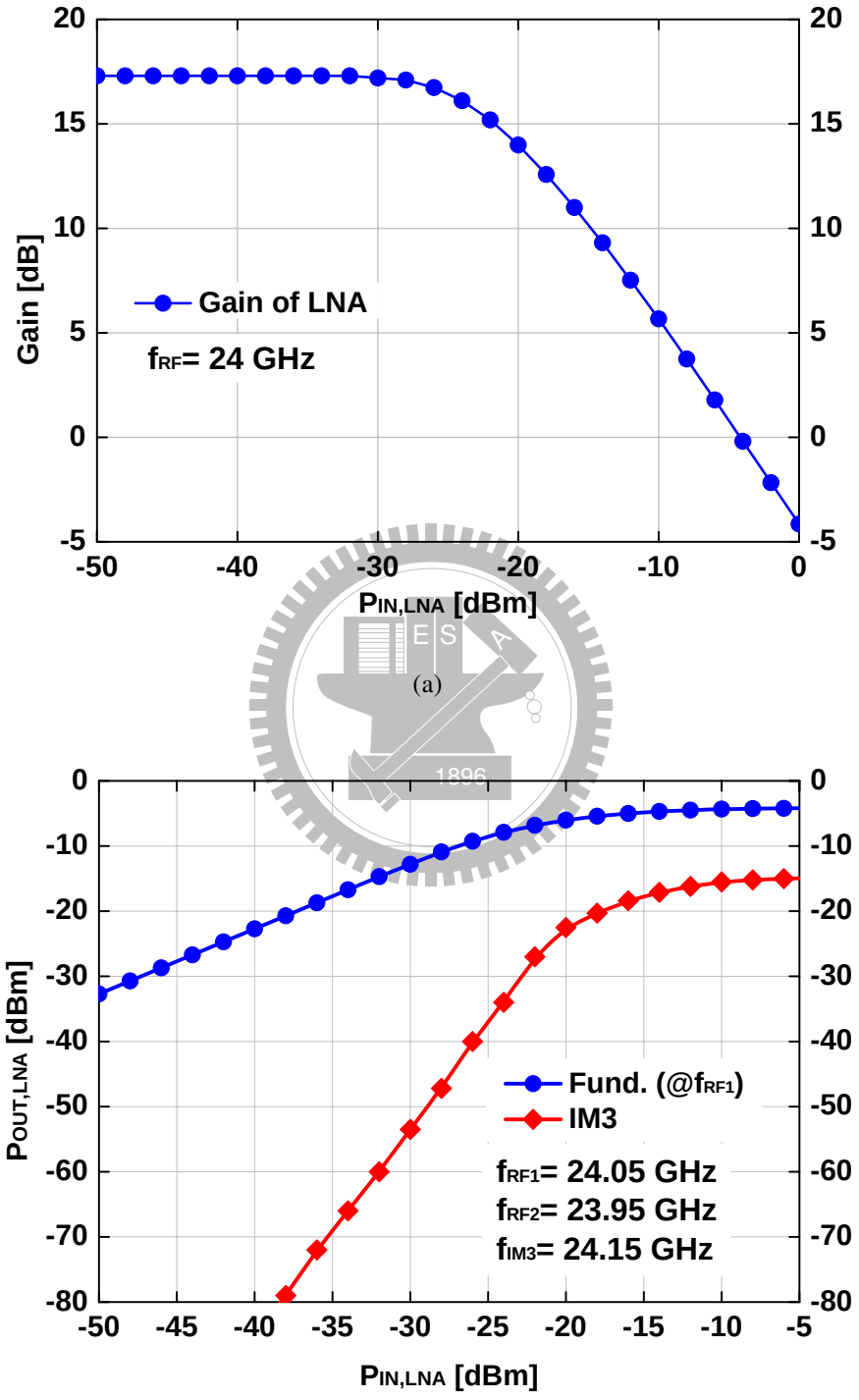


Figure 2.7 Simulated linearity performance of the current-mode LNA by (a) 1-tone analysis, and (b) 2-tone analysis.

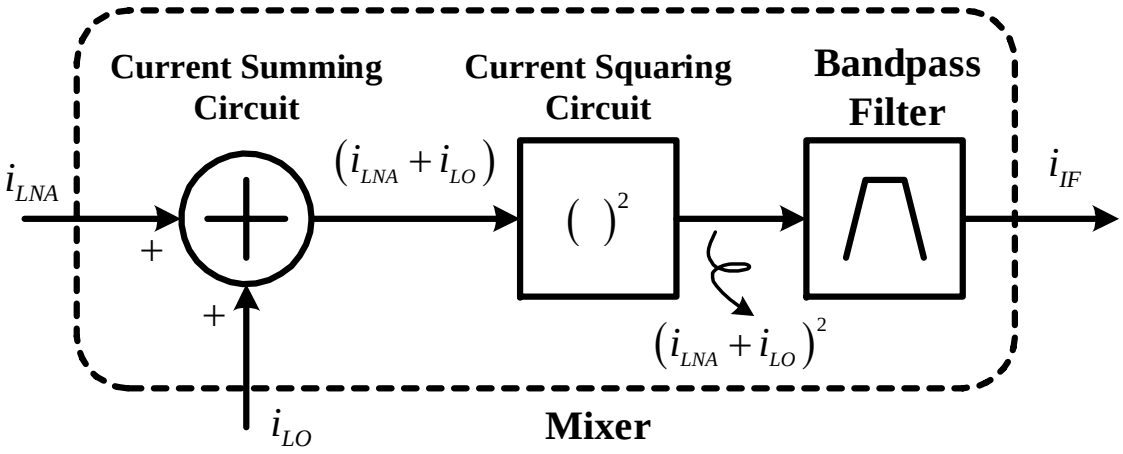


Figure 2.8 Conceptual block diagram of the current-mode down-conversion mixer.

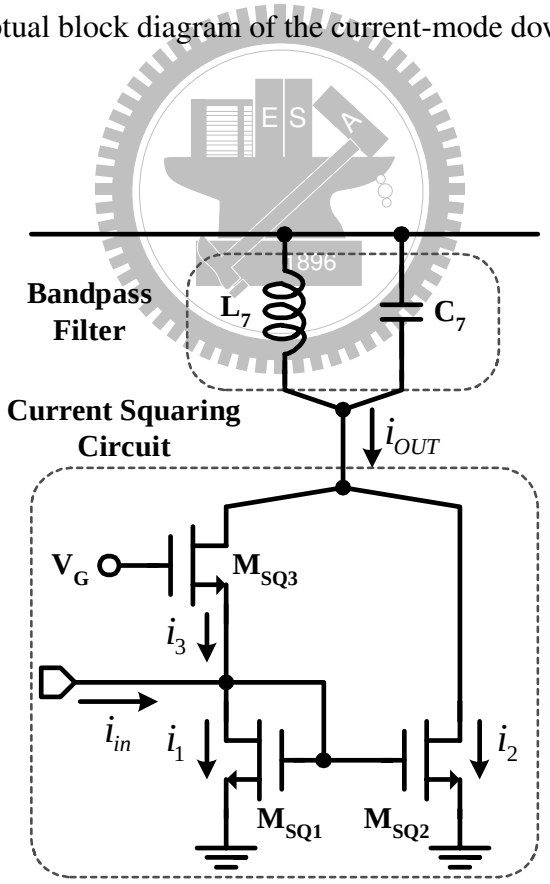


Figure 2.9 Circuit diagram of the current-squaring circuit and bandpass filter.

MOS devices are in the saturation region, the relation between $v_{GS,M_{SQ1}}$, $v_{GS,M_{SQ3}}$,and the input current i_{in} can be expressed as

$$v_{GS,M_{SQ1}} = \frac{V_G}{2} + \frac{i_{in}}{k_n \frac{W}{L}(V_G - 2V_{th})} \tag{2.15}$$

$$v_{GS,M_{SQ3}} = \frac{V_G}{2} - \frac{i_{in}}{k_n \frac{W}{L}(V_G - 2V_{th})} \tag{2.16}$$

where $k_n = \mu_n C_{ox}$ is the mobility μ_n times the oxide capacitance per unit area C_{ox}, V_{th} is the threshold voltage, v_{GS} is gate-to-source voltage, and V_G is the dc bias voltage of the current squaring circuit and equal to $(v_{GS,M_{SQ1}} + v_{GS,M_{SQ2}})$. From (2.15) and (2.16), the drain currents i_1 and i_3 of M_{SQ1} and M_{SQ3}, respectively, can be calculated. Since $i_1 = i_2$, the output current i_{OUT} can be written as

$$i_{OUT} = i_1 + i_3 = I_B + \frac{i_{in}^2}{4I_B} \tag{2.17}$$

where

$$I_B = \frac{1}{4} k_n \frac{W}{L}(V_G - 2V_{th})^2 \tag{2.18}$$

Supposed the input current i_{in} of the current squaring circuit equals $(I_{RF}\cos\omega_{RF}t + I_{LO}\cos\omega_{LO}t)$, the output current signal of the current squaring circuit from (2.17) can be expressed as

$$\begin{aligned} i_{OUT}(t) &= \left(I_B + \frac{I_{RF}^2 + I_{LO}^2}{8I_B}\right) \\ &+ \frac{1}{8I_B}\left(I_{RF}^2\cos 2\omega_{RF}t + I_{LO}^2\cos 2\omega_{LO}t\right) \\ &+ \frac{I_{RF}I_{LO}}{4I_B}\left[\cos\left(\omega_{RF} + \omega_{LO}\right)t + \cos\left(\omega_{RF} - \omega_{LO}\right)t\right] \end{aligned} \tag{2.19}$$

From the last term in (2.19), the double sideband mixing is achieved and the RF signal at the frequency ω_{RF} is mixed with the LO signal at the frequency of ω_{LO}. The signal at ω_{RF} is converted into the signals at at $(\omega_{RF} + \omega_{LO})$ and at $(\omega_{RF} - \omega_{LO})$. The ω_{IF} in this design is set to $(\omega_{RF} - \omega_{LO})$. The current conversion gain of the current squaring circuit

can be defined as

$$\begin{aligned} \text{Current Conversion Gain} &\equiv \frac{i_{out}\mid_{\omega=(\omega_{RF}-\omega_{LO})}}{i_{rf}} \\ &= \frac{I_{LO}}{4I_B} \\ &= \frac{I_{LO}}{k_n\frac{W}{L}(V_G-2V_{th})^2} \end{aligned} \tag{2.20}$$

From (2.20), the current conversion gain can be controlled by the magnitude of LO signal and the biasing voltage V_G.

The proposed current-mode mixer is operated as current multiplier. Compared to the Gilbert mixers, the proposed current-mode mixer generate less harmonics and intermodulation products, and therefore, the proposed current-mode mixers is more linear than the Gilbert mixers. If V_G is designed approach to $2V_{th}$ and M_{SQ1} - M_{SQ3} are also in saturation region, bias current I_B can be kept small, and the LO current signal can be kept small such that small LO power can be obtained.

As shown in (2.19), the second order harmonics of the RF and LO exist because the single-balanced down-conversion mixer is used. To eliminate these harmonic terms, the load of the current squaring circuit can be designed by a LC tank which is resonated at IF and serves as a BPF. Because of its bandpass characteristics, both harmonic and intermodulation components with frequencies far away from the IF can be suppressed. Only the IF signal at the desired frequency are selected and sent to the output.

In the advanced deep sub-micron CMOS technologies, the relationship between the drain current and the gate overdrive voltage of CMOS devices is not exactly square. Due to the short channel and channel length modulation effects, the drain current i_{DS} is approximated as [163], [164]

$$i_{DS} \approx \frac{1}{2}k_n\frac{W}{L}\frac{\mu_n}{(1+\theta v_{OV})}\frac{v_{OV}^2}{\left(1+\frac{v_{OV}}{E_C L}\right)}(1+\lambda v_{DS}) \tag{2.21}$$

where $v_{OV} = (v_{GS} - V_{th})$ is the gate overdrive voltage, E_C is the critical value of the horizontal electric field, θ is inversely proportional to the oxide thickness, and the coefficient λ models the effect of the channel length modulation which is related to v_{DS}. Because V_G

is usually designed a little higher than two times threshold voltage of M_{SQ1} and M_{SQ3} from the consideration of the current conversion gain as shown in (2.20). The overdrive voltage voltages of both M_{SQ1} and M_{SQ3} are not high, and are of several mV such that $v_{OV} \ll \theta^{-1}$ and $v_{OV} \ll E_C L$. To analyze the behavior of the current-squaring circuit with short channel and channel length effects, (2.21) can be simplified approximately as

$$i_{DS} \approx \frac{1}{2} k_n \frac{W}{L} v_{OV}^2 (1 + \lambda v_{DS}) \tag{2.22}$$

Therefore, the channel length-length modulation will have some effects of the proposed current-squaring circuit and need to be investigated further more.

If $\delta = (v_{DS,M_{SQ3}} - v_{DS,M_{SQ1}})/2$ and $\sigma = (v_{DS,M_{SQ3}} + v_{DS,M_{SQ1}})/2 = V_{DD}/2$ is assumed, $v_{DS,M_{SQ3}} = (\sigma+\delta) = (V_{DD}/2+\delta)$ and $v_{DS,M_{SQ1}} = (\sigma-\delta) = (V_{DD}/2-\delta)$. After considering the channel-length modulation by (2.22), the expression i_{OUT} in (2.17) is modified and expressed as

$$i_{OUT} = \chi_1 \frac{i_{in}^2}{4I_B} + \chi_2 i_{in} + \chi_3 I_B \tag{2.23}$$

where

$$\chi_1 = \frac{2 + 3\sigma\lambda + 4\delta\lambda}{2\left[(1+\sigma\lambda)^2 - \delta\lambda(1+\sigma\lambda+\delta\lambda)\right]} \tag{2.24}$$

$$\chi_3 = \frac{\delta\lambda(4+5\sigma\lambda) + \sigma\lambda(1+\sigma\lambda)}{2\left[(1+\sigma\lambda)^2 - \delta\lambda(1+\sigma\lambda+\delta\lambda)\right]} \tag{2.25}$$

$$\chi_3 = \frac{(1+\sigma\lambda+\delta\lambda)^2(2+3\sigma\lambda)}{2\left[(1+\sigma\lambda)^2 - \delta\lambda(1+\sigma\lambda+\delta\lambda)\right]} \tag{2.26}$$

Note that χ_1 and χ_3 are less than 1, whereas χ_3 is larger than 1. Furthermore, the above derivations only consider the channel length modulation effect, and the rest of short channel effects are ignored under the condition of small gate overdrive voltage of M_{SQ1} and M_{SQ3}. If the effect of channel-length modulation effect is neglected as $\lambda = 0$, $\chi_1 = 1$, $\chi_2 = 0$, and $\chi_3 = 1$. Hence, (2.23) can be simplified to (2.17). The factor χ_1 of the i_{in}^2 in (2.23) reveals that the conversion gain of the squaring circuit with the channel-length modulation becomes χ_1 times smaller than that without channel-length modulation. The detailed derivations of (2.23)–(2.26) are shown in Appendix A.

Moreover, even if the drain-to-source voltage differences of M_{SQ1} and M_{SQ3} are the same, the channel-length modulation still has effects on the proposed squaring circuit. In

this case where $\delta = 0$ and $\lambda \neq 0$, (2.23) is simplified to

$$i_{OUT} = \gamma_1 \frac{i_{in}^2}{4I_B} + \gamma_2 i_{in} + \gamma_3 I_B \tag{2.27}$$

where

$$\gamma_1 = \frac{2 + 3\sigma\lambda}{2(1 + \sigma\lambda)^2} \tag{2.28}$$

$$\gamma_2 = \frac{\sigma\lambda}{2(1 + \sigma\lambda)} \tag{2.29}$$

$$\gamma_3 = \frac{2 + 3\sigma\lambda}{2} \tag{2.30}$$

From the above derivations, channel-length modulation effect degrades the conversion gain of the current squaring circuit which is χ_1 smaller in (2.23) or γ_1 smaller in (2.27). Besides, this effect also leads to the leakage of the fundamental signal of LO and RF signals.

The simulated conversion gain versus the biasing voltage V_G of the proposed current-squaring circuit is depicted in Fig. 2.10. In this design, the conversion gain approaches maximum value when V_G equals 1.2 V. Meanwhile, the drain-to-source voltage difference of M_{SQ1} and M_{SQ3}, $|v_{DS,M_{SQ1}} - v_{DS,M_{SQ3}}|$, is at the minimum value.

Fig. 2.11 shows the current summing circuit. Two common-gate transistors M_9 and M_{10} in the saturation region are operated as current buffers. The bulks of M_9 and M_{10} are connected to ground. Although M_9 and M_{10} suffer from the body effect resulting in slightly increase of their threshold voltage, the isolation among the input port of RF, the input port of LO, and the output port can be improved. Besides, the voltage headroom of this circuit is sufficient because the inductor L_4 is tied to V_{DD} and L_5–L_6 are tied to ground. This current summing circuit can be operated at very low supply voltage. The input impedance of the LO port is small because of the input of the common-gate current buffer. As the power signal is applied to the LO port, the LO signal will be mainly carried by the current signal. Therefore, additional circuit for voltage to current conversion is not required to prevent from the overhead of power consumption.

Due to the advantage of current-mode signal processing, the current signals $i_{out,LNA}$ from LNA circuit and $i_{in,LO}$ from off-chip LO signal generator are summed by connecting the drains of M_9 and V_{10} together. L_4 is designed to provide high impedance at the output

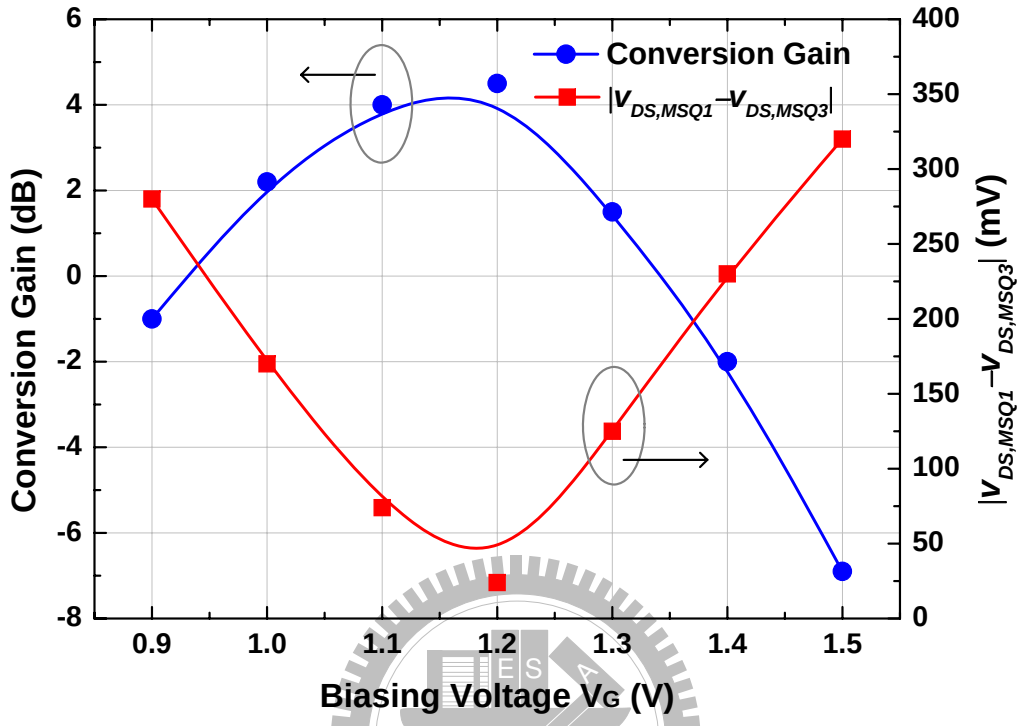


Figure 2.10 Circuit diagram of the current-summing circuit.

so that the summed current signal ($i_{out,LNA} + i_{in,LO}$) can be fed into the following current squaring circuit. C_5 is the dc blocking capacitor to prevent from disturbing the biasing point of the LNA. At the frequency of RF, L_5 is resonated with the parasitic gate-to-source capacitance C_{GS,M_9} and the parasitic source-to-bulk capacitance C_{SB,M_9} of M_9 to provide high impedance to ac ground so that the input RF current signal from the LNA circuit can flow into M_9. L_6, C_6, and C_{PAD2} constitute the input matching network for LO input port. The parasitic gate-to-source capacitance $C_{GS,M_{10}}$ and the parasitic source-to-bulk capacitance $C_{SB,M_{10}}$ of M_{10} are also considered within the input matching network of LO input port.

2.2.3 Integrated Current-Mode Receiver Front-End

The detailed connections of the current-mode receiver front-end circuits are shown in Fig. 2.12. The circuits include a two-stage current-mode LNA of low-voltage version, a

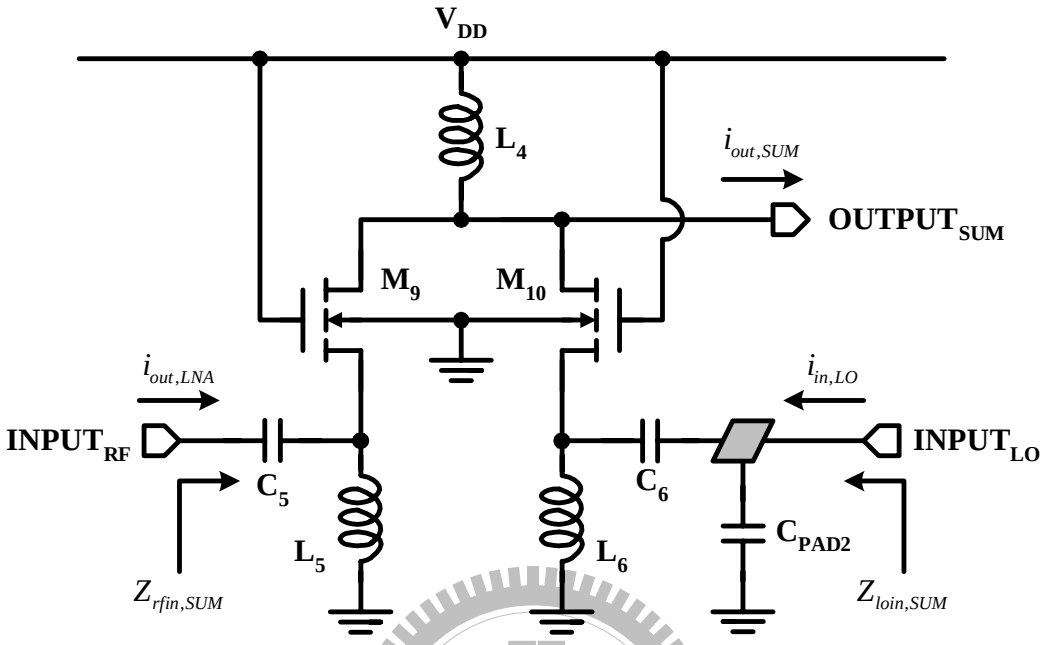


Figure 2.11 Circuit diagram of the current-summing circuit.

current summing circuit, and a current squaring circuit. The input signal at ω_{RF} is firstly amplified by LNA, and then is mixed with the LO signal at ω_{LO} by the current-mode mixer formed by a current summing circuit and a current squaring circuit. The down-converted signal at ω_{IF} is finally sent to output buffer which is a current-mirror amplifier formed by M_{14}, M_{15}, and L_8. The output matching network is designed by L_8, C_9, and C_{PAD3} so that the output impedance of the measuring buffer equals 50 Ω and the maximum power transfer can be achieved. Table 3.1 shows the design parameters of the two-stage current-mode LNA of low-voltage version. Table 3.2 shows the design parameters of current-mode down-conversion mixer and output buffer.

In this work, the RF input frequency is set at 24 GHz, the LO frequency is set at 19 GHz, and accordingly the IF output frequency is at 5 GHz. The image frequency is at 14 GHz. According to Fig. 2.5(a), the image rejection of the proposed receiver front-end is more than 30 dB before the first down-conversion mixer due to the large IF frequency of 5 GHz is selected. This performance is achieved due to the multistage nature of bandpass LNA. If much higher image rejection is required, the off-chip pre-select filter

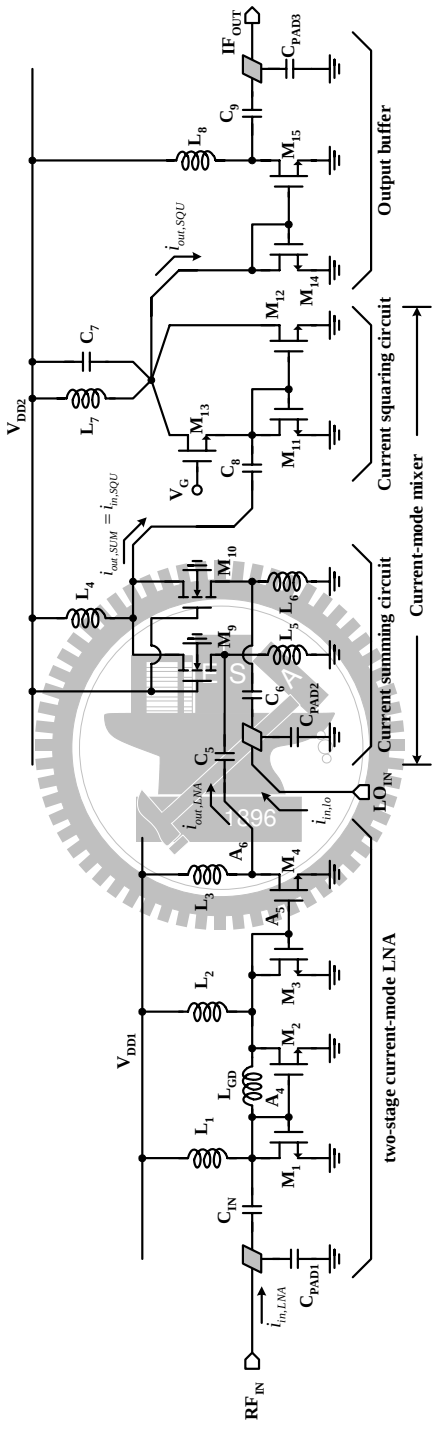


Figure 2.12 Detailed connections of the 24-GHz current-mode receiver front-end with output buffer.

Table 2.1
DEVICE PARAMETERS OF 24-GHZ CMOS CURRENT-MODE LNA

Low-Noise Amplifier	
M_1, M_3	1.2 μm / 0.13 μm
M_2	52.8 μm / 0.13 μm
M_4	31.2 μm / 0.13 μm
C_{IN}	89 fF
C_{PAD1}	20 fF
L_{GD}	506 pH
L_1	297 pH
L_2, L_3	315 pH

Table 2.2
DEVICE PARAMETERS OF 24-GHZ CMOS CURRENT-MODE DOWN-CONVERSION MIXER AND OUTPUT BUFFER

Current-Squaring Circuit	
M_9, M_{10}	38.4 μm / 0.13 μm
C_5	63 fF
C_6	274 fF
C_{PAD2}	20 fF
L_4	443 pH
L_5	945 pH
L_6	916 pH
Current-Squaring Circuit	
M_{11}, M_{12}, M_{13}	14.4 μm / 0.13 μm
C_7	1 pF
C_8	132 fF
L_7	884 pH
Output Buffer	
M_{14}	1.2 μm / 0.13 μm
M_{15}	150 μm / 0.13 μm
C_9	583 fF
C_{PAD3}	20 fF
L_8	1.69 nH

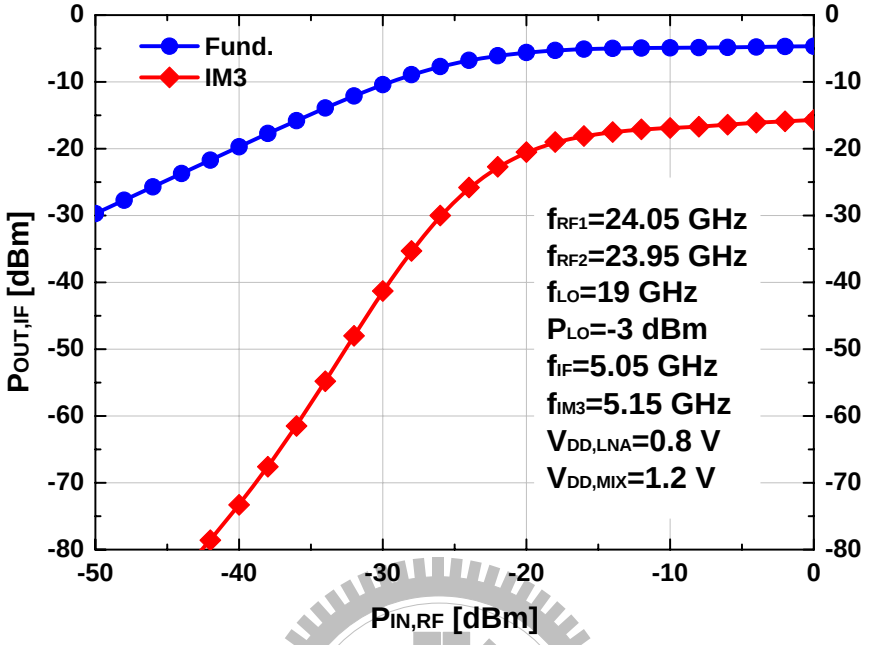


Figure 2.13 Simulated linearity performance of the 24-GHz current-mode receiver by two-tone HB analysis.

before the LNA can be used to enhance the performance of image rejection. For testing consideration, the three ports are also designed to match with 50 Ω.

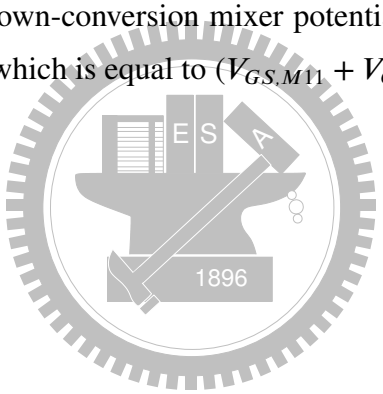
If multiple power supplies can be used in the receiver front-end, the simulated power consumption of the current-mode receiver is 29.94 mW where the two-stage current-mode LNA of low-voltage version drains 20.4 mA from the supply voltage of 0.8 V, and the current summing circuit and current squaring circuit drain 8.8 mA and 2.55 mA, respectively, from the supply voltage of 1.2 V. Under this condition, the two-tone analyses by HB simulation with two RF input signals at 23.95 GHz and 24.05 GHz and the LO signal at 19 GHz with the power level of –3 dBm are depicted in Fig. 2.13. It reveals that the receiver has a simulated conversion gain of 21.5 dB, an IP_{-1dB} of –29 dBm, and a P_{IIP3} of –18.2 dBm. The simulated NF of the proposed integrated current-mode receiver front-end is 4.2 dB with the RF at 24 GHz and LO at 19 GHz.

Moreover, if the receiver front-end is restricted to use single power supply, it consumes 55.4 mW from the supply voltage of 1.2 V. The excess power consumption is from the

LNA because higher voltage is adopted to bias the LNA of the low-voltage version, and the LNA drains 34.82 mA from the supply voltage of 1.2 V. The use of multiple supply voltage of 0.8 V and 1.2 V complicates the design.

In this design, the supply voltages are from different off-chip power supplies. Therefore, the smaller supply voltage can be easily supported. If the receiver is restricted to use a single supply voltage of 1.2 V, the LNA is recommended to use the circuit in Fig. 2.4 where M_6–M_8 provide a simple way to have the voltage drop of around 400 mV for the LNA such that the voltages at the nodes of A_4–A_6 are around 0.8 V and M_1–M_4 can be well biased.

In the 0.13-μm CMOS process, the threshold voltage of NMOS transistors is about 450 mV. With 50-mV overdrive voltage of the transistors M_{11} and M_{13} for proper operation, the proposed current-mode down-conversion mixer potentially can be operated at lower supply voltage of about 1 V, which is equal to $(V_{GS,M11} + V_{GS,M13})$.



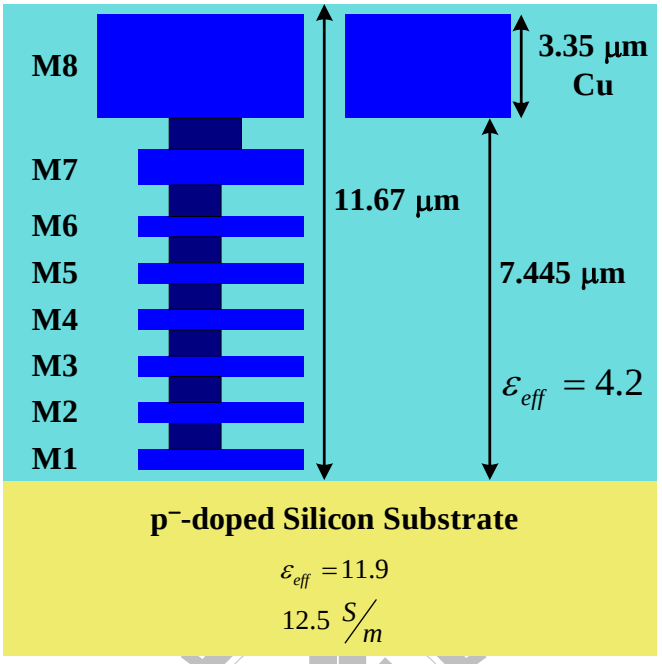


Figure 2.14 Cross-section view of back-end process.

2.3 Experimental Results

The designed 24-GHz current-mode receiver front-end circuit was fabricated in 0.13-μm 1P8M CMOS technology. Shown in Fig. 2.14 is the cross-section view of the backend process. The top metal of this process is copper (Cu) and is with the thickness of 3.35 μm. The height of the oxide evaluated from the surface of p-type silicon substrate to the bottom of the top metal-8 is about 7.445 μm. The equivalent relative permittivity ε_{eff} is about 4.2. Based on the technology information of the backend process, the electromagnetic (EM) tool Ansoft HFSS^{TM} [165] is used to evaluate and extract the characteristics of the on-chip octagonal spiral inductors, and it is also used to extract the parasitic of the proposed circuit from the layout view to perform post-simulation.

The floor plans of the proposed receiver front-end are depicted in Fig. 2.15. Nine on-chip octagonal spiral inductors are used. The distances of each inductor are more than 100 μm to mitigate the magnetic coupling between on-chip inductors. In addition, the distances of the active devices of current-mode LNA, current summing circuit, current-

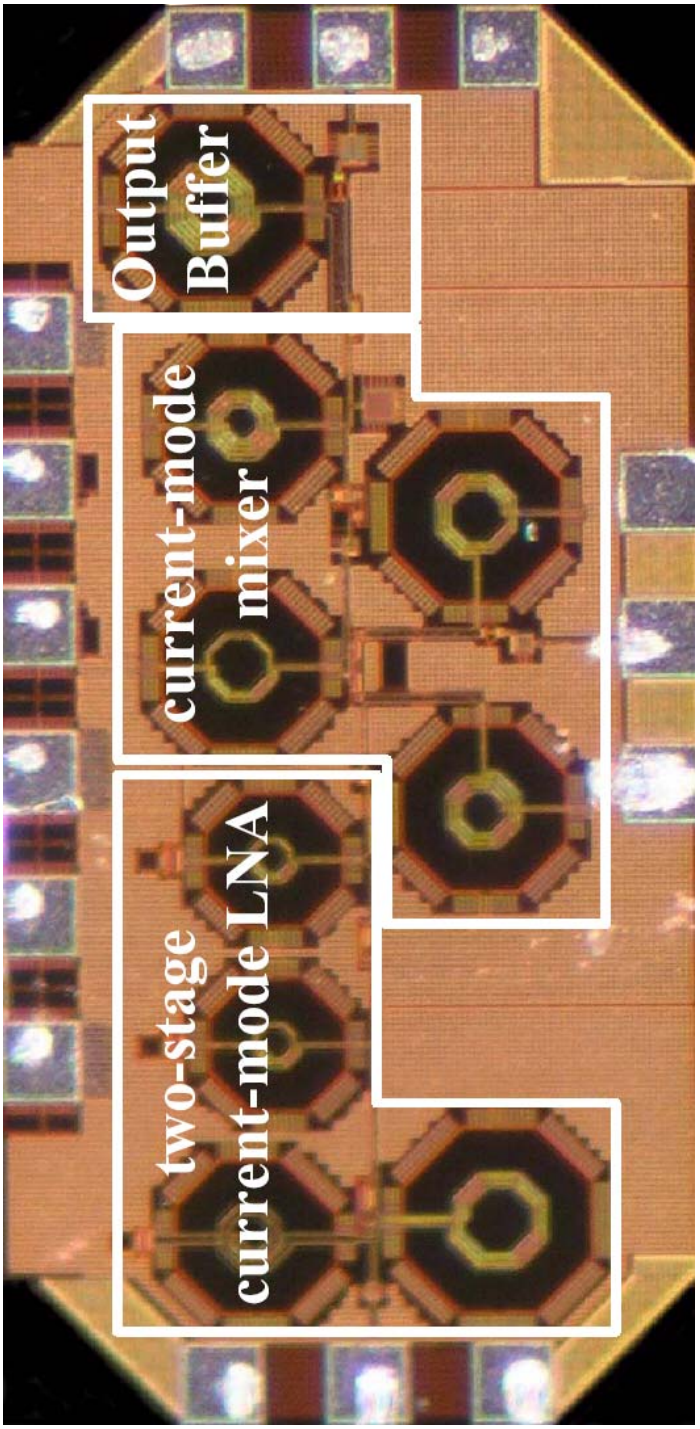


Figure 2.15 Chip microphotography of the fabricated 24-GHz current-mode receiver front-end.

squaring circuit and output buffer are arranged far, the noise influence between these circuits are kept small. The signal path between input pad and the input of the LNA is drawn as short as possible to avoid additional signal losses and increase of NF. Besides, large on-chip decoupling capacitors are used between the biases and ground, such that high frequency noises can be bypassed to ground and consequently stable biases and supplies of the receiver can be achieved. All dc pads are protected by ESD diodes to enhance the reliability of the proposed receiver. The performance of each circuit block in this 24-GHz current-mode receiver is over-designed to overcome process variations. This chip occupies the active region of 1.45×0.72 mm^2 including testing pads.

The measurement setups of this fabricated receiver are described as follows. The on-wafer probing measurement is adopted to verify the performance of the receiver front-end. Three GSG RF probes with the pitch of 150 μm and a 6-pin dc probe with the pitch of 150 μm are applied to probe the testing pads. As shown in Fig. 2.16(a), the S parameters are measured to analyze both the input and output matching characteristics by the network analyzer, Agilent E8364B, which can characterize the S-parameter performance from 10 MHz to 50 GHz. To measure conversion gain and linearity, three signal generators Agilent E8257D are used to provide two RF and one LO signals for the device under test (DUT). The spectrum analyzer Agilent E4448A is used to monitor the spectrum to verify the linearity and conversion gain of the receiver. The measurement environment is illustrated in Fig. 2.16(b). The noise figure analyzer Agilent N8975A with a broadband noise source HP 346C are used to measure the performance of NF of the receiver. The measurement environment is illustrated in Fig. 2.16(c).

Owing to the layout mistake of the fabricated chip, the focused ion beam (FIB) post-process is used to modify the metal connections of the current-mode LNA. The FIB metal lines connect the LNA circuit to the power supply. Under the condition that multiple power supplies can be used so that the power supply of LNA and current-mode mixer are 0.8 V and 1.2 V, respectively, the measured total power consumption is 27.8 mW. Moreover, if the single power supply of 1.2 V is applied to the receiver front-end, the measured power dissipation is increased to about 49.8 mW. The reason why the increase in measured power dissipation from 27.8 mW for the multiple supply voltages to 49.8 mW for the single supply voltage is the supply voltage of LNA is increased from 0.8 V

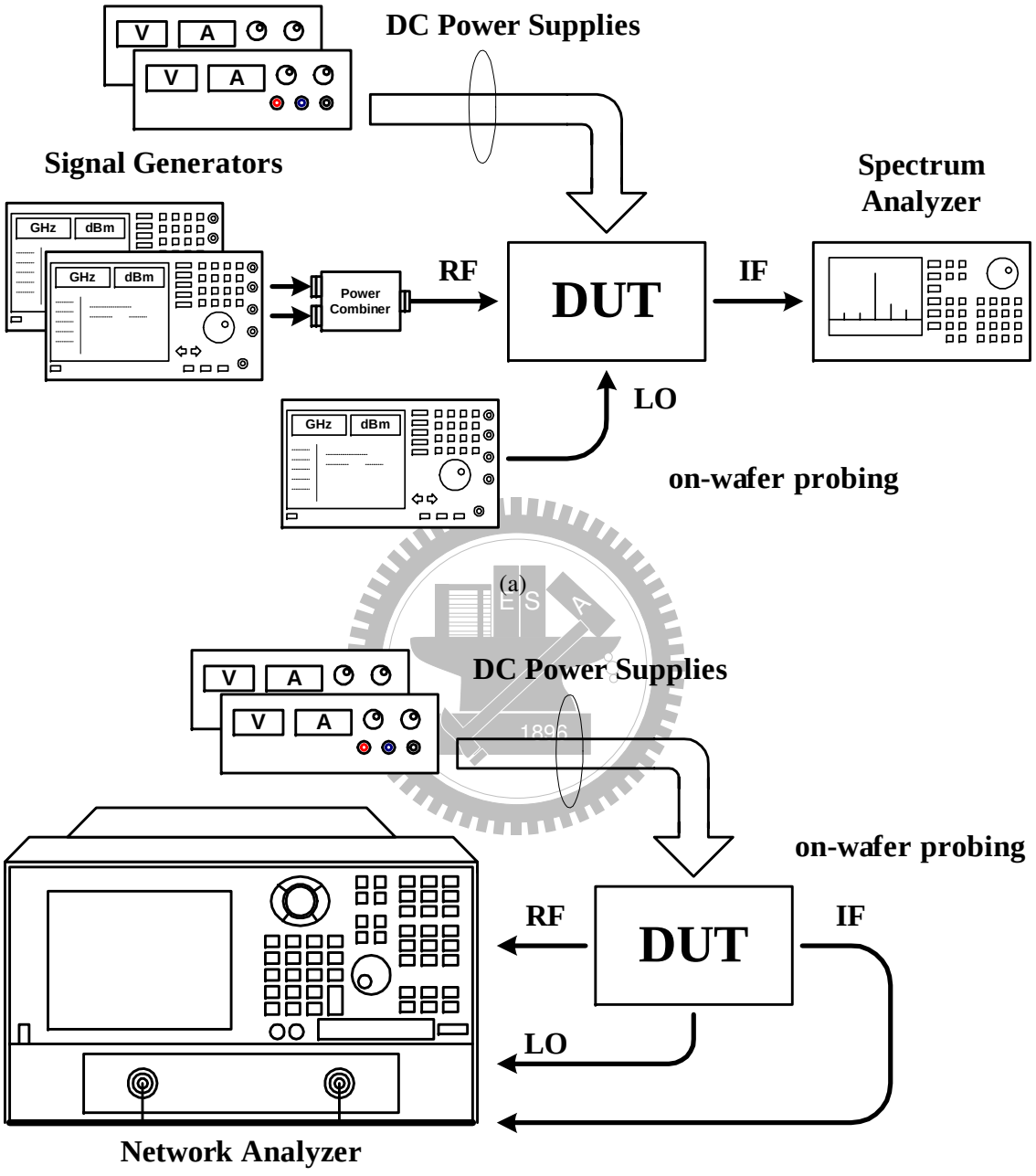
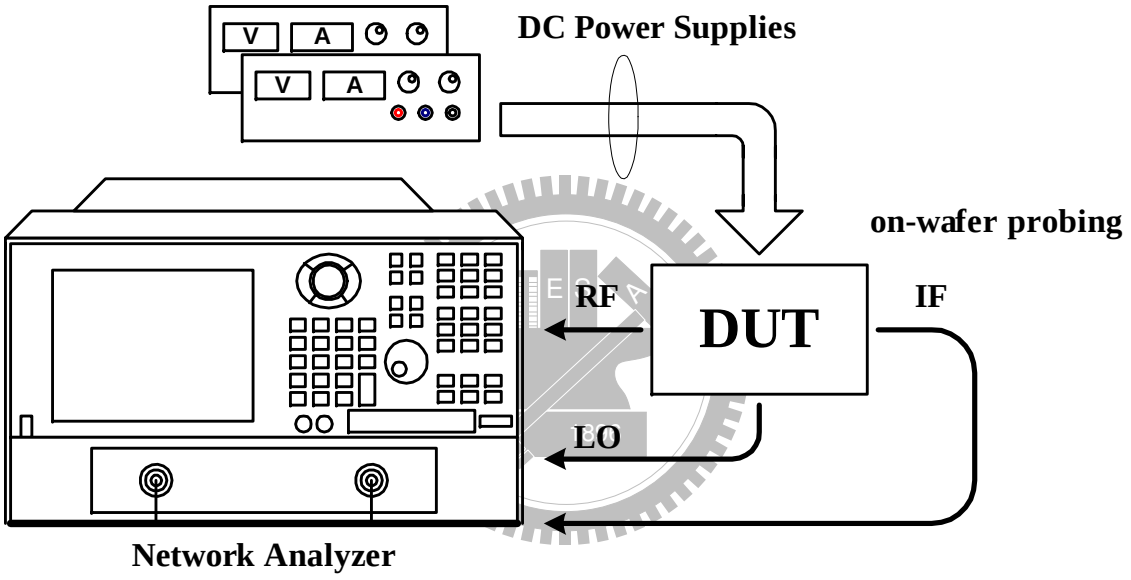


Figure 2.16 The environment setup of (a) S-parameter measurement, (b) linearity measurement, and (c) noise figure measurement.



(c)

Figure 2.16 The environment setup of (a) S-parameter measurement, (b) linearity measurement, and (c) noise figure measurement (*Con't*).

to 1.2 V. This results in increasing more overdrive voltage of 400 mV of the LNA, and consequently the measured power dissipation of LNA itself is increased. The measured current consumption of the LNA is 19.45 mA from the supply voltage of 0.8 V and is 31.3 mA from the supply voltage of 1.2 V.

Fig. 2.17 presents the measured and revise-simulated conversion gain versus RF input frequency. The losses from cables, probes and adaptors are compensated. Moreover, the parasitic resistances resulting from FIB post-process are considered in the revise-simulated results. The tested RF input power is –30 dBm. The LO is set to the frequency which is 5 GHz lower than the RF, $f_{LO} = f_{RF} - 5\text{GHz}$, and the tested LO input power is –3 dBm. The output is observed at the fixed IF frequency of 5 GHz. The measured conversion gain of the RF frequency at 24 GHz is 11.3 dB under the condition that the power supplies of the LNA and Mixer are 0.8 V and 1.2V, respectively. In addition, the conversion gain is 12 dB under the condition that the power supply of both LNA and Mixer is 1.2 V. Because the parasitic resistances from FIB post-process are in series with the inductive loads of the current-mode LNA, the quality factor of the loads of the LNA is decreased. This makes the gain of the LNA decrease, and consequently the conversion gain of the receiver is decreased.

The two-tone test results are shown in Fig. 2.18. Two RF inputs with 100 MHz frequency spacing are at the frequency of 24.05 GHz and 23.95 GHz and the LO is at 19 GHz with the power of –3 dBm. Because of the conversion gain reduction of the receiver, the measured IP_{-1dB} and P_{IIP3} are raised to –13.5 dBm and –1 dBm, respectively, under the condition that the power supplies of LNA and Mixer are 0.8 V and 1.2 V, respectively. Besides, the measured IP_{-1dB} and P_{IIP3} are about –12 dBm and –1.5 dBm, respectively, under the condition that the single power supply of 1.2 V for LNA and Mixer is adopted. At the RF frequency of 24 GHz and the LO frequency of 19 GHz, the measured total NF of the receiver is 14.2 dB and 13.3 dB if the power supply of LNA is 0.8 V and 1.2 V, respectively.

Table 3.3 summaries the performance of the proposed current-mode receiver front-end. In addition, some comparison results of published 24-GHz receiver front-end circuits are also provided. Compared to the works published in [51], [57], [157], [166], the proposed 24-GHz CMOS current-mode receiver front-end has the advantage of smaller

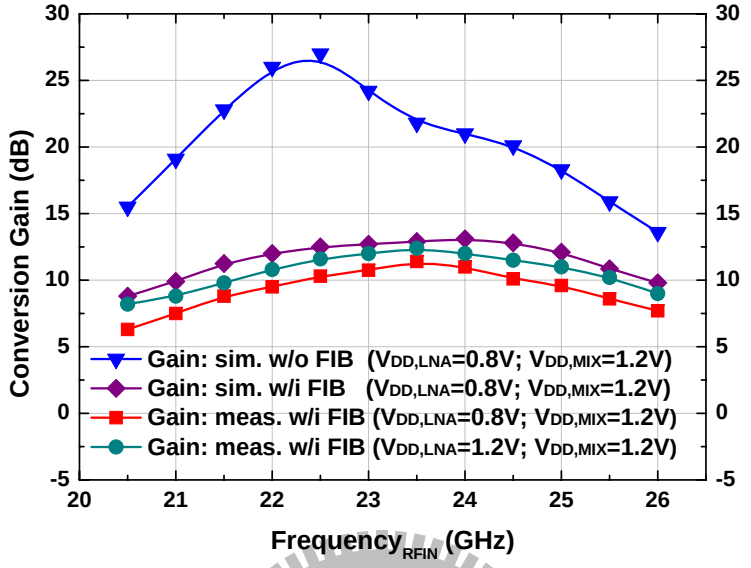


Figure 2.17 The measured and simulated conversion gain of the receiver versus RF input frequency.

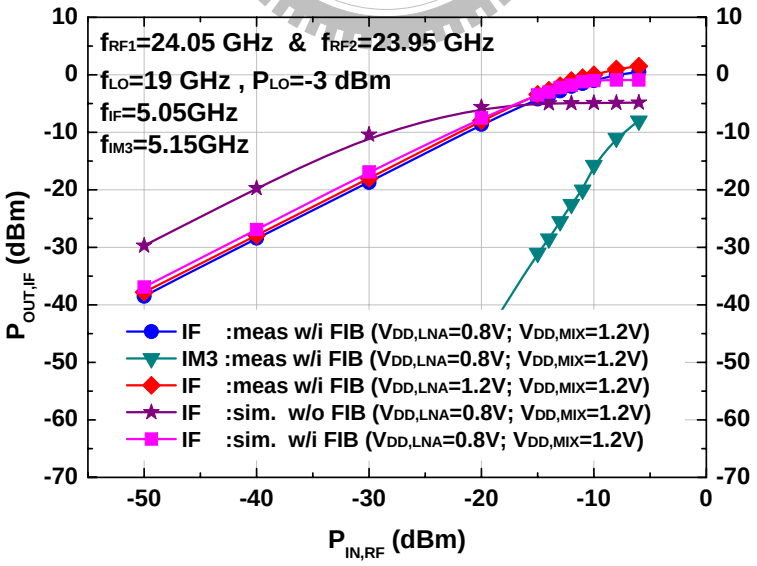


Figure 2.18 The measured linearity performance of the receiver by two-tone testing.

power dissipations and can be operated in low supply voltage. This current-mode receiver front-end also has better linearity performance.

2.4 Summary

In this work, the current-mode design techniques of CMOS RF circuits are developed and are applied to realize the first 24-GHz CMOS current-mode receiver front-end. The receiver integrated with a current-mode LNA and a current-mode down-conversion mixer is designed, fabricated in 0.13-μm 1P8M CMOS technology and measured. Two-stage current-mirror amplifiers cascaded are used to realize the current-mode LNA. The LNA has the capability of low-voltage operation. The current summing circuit and current-squaring circuits are adopted to perform the mixing of the current signals. The proposed current-mode mixer potentially can be operated in the low supply voltage of 1 V. The measured results demonstrate that the proposed current-mode receiver front-end can operate well in the 24-GHz frequency band. Although the receiver does not achieve the expected performance because of the layout mistake, after the FIB post-process to remedy for the layout mistake, the designed 24-GHz CMOS current-mode receiver front-end still can exhibit the conversion gain of 11.3 dB, the NF of 14.2 dB, and the P_{IIP3} of –1 dBm under the condition that power supply of the current-mode LNA is 0.8 V and the power supply of the current-mode mixer is 1.2 V. The total power dissipation of the current-mode receiver front-end under this condition is 27.8 mW. Besides, the proposed current-mode circuits require less currents than conventional voltage-mode circuits. Therefore, the current-mode design techniques have the capability of designing low-voltage and low-power RF circuits in the advanced nanometer CMOS technologies. Future research on the applications of a parallel wireless network to the existing WLANs at 17 GHz, short-range data link of HiperLink, long-distance data link of HiperAccess, or point-to-point wireless communication systems will be explored and discussed by the proposed current-mode approaches.

Table 2.3
THE MEASURED PERFORMANCE AND COMPARISON RESULTS OF PUBLISHED 24-GHZ RECEIVER FRONT-END CIRCUITS

	This work		[157]	[57]	[51]	[166]
Receiver architecture	Heterodyne		Heterodyne	Heterodyne	Heterodyne	Direct-conversion
Building blocks	2-stage LNA + single-balanced current-mode mixer		LNA + double-balanced RF Mixer + I/Q differential IF Mixer + DCOC + VCO with quadrature divider	3-stage LNA + Single-Balanced Gilbert Mixer + Two IF Amplifiers	3-stage LNA + single-balanced Gilbert Mixer	3-stage diff. LNA + I/Q diff. Gilbert Mixer
Topology	Current-mode		Current-mode	Voltage-mode	Voltage-mode	Voltage-mode
Technology	0.13-μm CMOS		0.13-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.8-μm SiGe HBT f_T=80 GHz
RF frequency [GHz]	24		24	24	21.8	24.1
LO frequency [GHz]	19		16	19.18	16.9	23.9
IF frequency [GHz]	5		0	4.82	4.9	0.2
Supply voltage [V]	1.2	0.8/1.2	1	1.8	1.5	4
Power [mW]	49.8	27.8	35	54	64.5	640
Receiver gain [dB]	12	11.3	19.5	28.4	27.5	31
Receiver NF [dB]	13.3	14.2	15	6	7.7	8.8
Receiver P_{IIP3} [dBm]	–1.5	–1	–	–	–	–
Receiver IP_{-1dB} [dBm]	–12	–13.5	–25	–23.2	–23	–27
Chip area [mm^2]	1.45 × 0.72		1.85 × 1.806	1.1 × 1.2	0.4 × 0.5	1.48 × 1.15

Chapter 3

Low-Power Current-Mode K–Band Transmitter Front-End ICs

It is the aim of this chapter to introduce a new current-mode transmitter front-end. The proposed integrated current-mode transmitter front-end which is operated in the frequency of K-band has been fabricated in 0.13-μm 1P8M CMOS technology, and been published in [62], [160]. The proposed transmitter front-end is of double-balanced structure and is integrated with a current-mode double-balanced up-conversion mixer, a baseband current buffer/repeater, a voltage-controlled oscillator (VCO), and a VCO buffer/repeater. The proposed current-mode double-balanced up-conversion mixer consists of four current-squaring circuit units of which the input and output are both current signals. Fully balanced current-mirror amplifiers are adopted to deal with differential baseband input current signals. Two identical differential baseband current signals are copied through the current-mirror amplifiers. The on-chip cross-coupled VCO provides the differential LO signals. Through the transformer-based VCO buffer/repeater, the differential voltage signals of LO is converted to two identical differential current signals of LO by two on-chip transformers. These LO current signals are sent to the proposed current-mode mixer. Another purpose of the transformer-based VCO buffer/repeater is to increase the isolation between VCO and current-mode mixer to prevent from disturbing VCO.

The measured results have shown that the proposed integrated current-mode transmitter front-end exhibits a measured conversion power gain of –5 dB, an input-referred

1-dB compression point (IP_{-1dB}) of –22 dBm, an output-referred 1-dB compression point (OP_{-1dB}) of –28 dBm, an input-referred third-order intercept point (P_{IIP3}) of –9.6 dBm, and an output-referred third-order intercept point (P_{OIP3}) of –14.6 dBm. The single-sideband (SSB) noise figure (NF) is about 12.7 dB. The on-chip VCO provides the LO frequency from 20.8 GHz to 22.7 GHz with the control voltage varied from 0 V to 2 V. The phase-noise of the VCO is –108 dBc/Hz at 10-MHz offset from 22.7 GHz. Under the 1-V supply voltage, the fabricated current-mode double-balanced up-conversion mixer, VCO, VCO buffer/repeater and baseband current buffer/repeater circuits dissipate 3.1 mW, 2.2 mW, 3.3 mW, and 3.1 mW, respectively. The proposed transmitter front-end occupies the active area of 1.5 × 1.1 mm^2 where testing pads are included.

This chapter is organized as follows. In Section 3.1, the design and extraction of on-chip planar transformer is described. In Section 3.2, the architecture and operational principle of the proposed current-mode transmitter front-end is described. In Section 3.3, circuit designs of the proposed double-balanced current-mode up-conversion mixer, on-chip VCO, transformer-based VCO buffer/repeater, baseband current buffer/repeater, and integrated current-mode transmitter front-end are described. Body effect and short channel effects of the proposed current-mode mixer are also investigated. Simulation results are also given in this section. In Section 3.4, the layout consideration and experimental results are presented and analyzed to verify the advantageous performance of the proposed current-mode double-balanced up-conversion mixer and the current-mode transmitter front-end. Finally, the summary is given in Section 3.5.

3.1 Design of On-Chip Transformer

The transformer is realized with two planar symmetric windings where the primary winding is 1 turn and the secondary winding is also 1 turn. Additionally, each winding has a center-tap which allows a usage in differential applications. Fig. 3.1 shows the two winding structures of transformers, *XFMR-I* and *XFMR-II*, used in this design. The transformers are fabricated in 0.13-μm 1P8M CMOS process. In this process, the metal layers consist of copper (Cu), embedded in the oxide which have an equivalent relative permittivity ε_{eff} of 4.2. Fig. 3.2 illustrates the cross-section view from the CMOS technology,

and Fig. 3.3 depicts the metal structure of *XFMR-I* and *XFMR-II*. The drawing parameters of the *XFMR-I*, shown in Fig. 3.3(a), are with $R = 80\mu m$, $W = 9\mu m$, $S = 3\mu m$. The number of turn is 2. Both the primary and secondary windings have center-tap point connections. In addition, the drawing parameters of the *XFMR-II*, shown in Fig. 3.3(b), are with $R = 60\mu m$, $W = 9\mu m$, and $S = 3\mu m$. The number of turn is 2. The primary winding of the *XFMR-II* has a center-tap point connection. According to the information of backend process from the CMOS technology, the electromagnetic (EM) tool Ansoft HFSS^{TM} [165] is used to evaluate and extract the characteristics of the on-chip octagonal transformers.

The two on-chip transformers *XFMR-I* and *XFMR-II* are connected as Fig. 3.4 to evaluate their performance. Fig. 3.5 shows the simulated reflection factors S_{11} and S_{22} of the two port transformers, *XFMR-I* and *XFMR-II*, where port-1 is related to the primary side and port-2 is related to the secondary side. Fig. 3.6 shows the simulated transmission factor S_{21} of *XFMR-I* and *XFMR-II*. In Fig. 3.5 and Fig. 3.6, the center-tap on each side is left open.

Fig. 3.7 presents the self-inductance of *XFMR-I* and *XFMR-II* as a function of frequency. The self-inductances are derived from the impedance parameters by

$$L_{P,\text{self}} = \frac{\Im\{Z_{11}\}}{\omega} \tag{3.1}$$

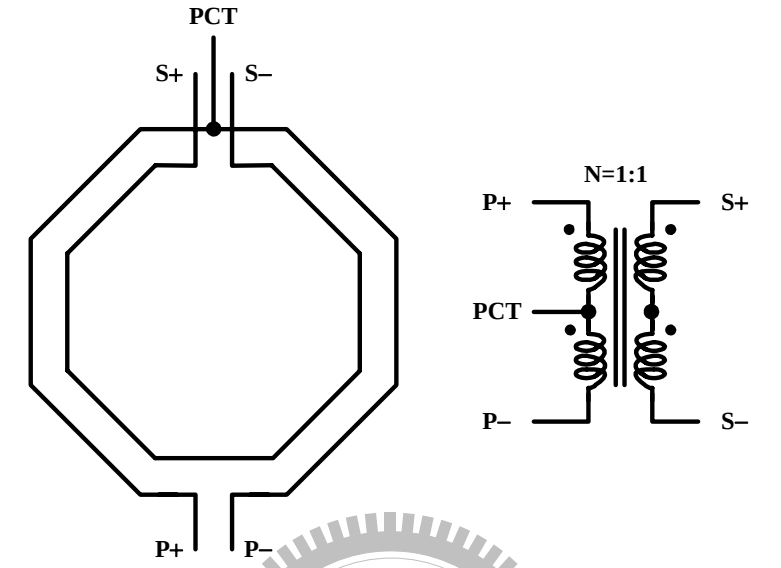
$$L_{S,\text{self}} = \frac{\Im\{Z_{22}\}}{\omega} \tag{3.2}$$

where $L_{P,\text{self}}$ and $L_{S,\text{self}}$ represent the self-inductance of the primary and of the secondary winding respectively. Z_{11} and Z_{22} are the input impedances when output is open. Moreover, the simulated coupling-coefficient k_{PS} and quality factor Q of *XFMR-I* and *XFMR-II* as a function of frequency is depicted in Fig. 3.8. The coefficient denotes the strength of magnetic coupling between the primary and secondary winding and can be expressed by the mutual inductance M and self-inductances, $L_{P,\text{self}}$ and $L_{S,\text{self}}$, of the windings as the following.

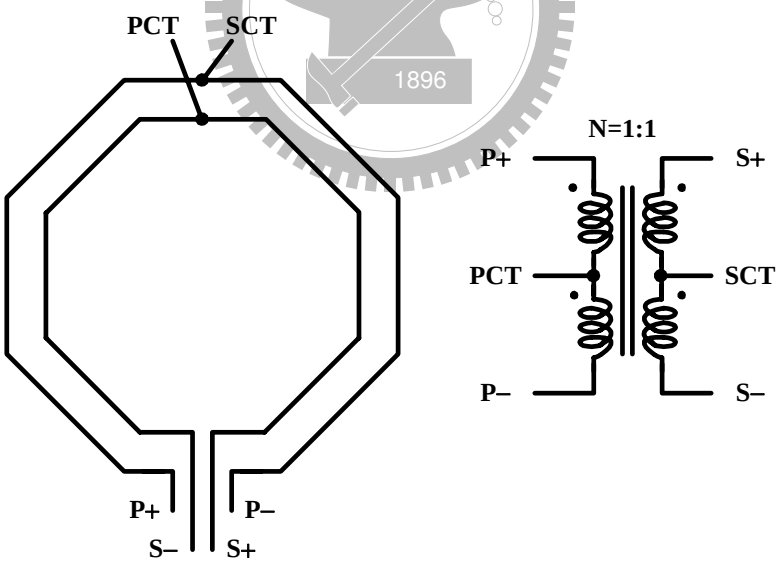
$$k_{PS} = \frac{M}{\sqrt{L_{P,\text{self}} L_{S,\text{self}}}} \tag{3.3}$$

The mutual inductance M is extracted from the impedance and admittance parameters as

$$M = \sqrt{\left(Y_{11}^{-1} - Z_{11}\right) \frac{Z_{22}}{\omega^2}} \tag{3.4}$$



(a)



(b)

Figure 3.1 The winding scheme of (a) XFMR-I, and (b) XFMR-II.

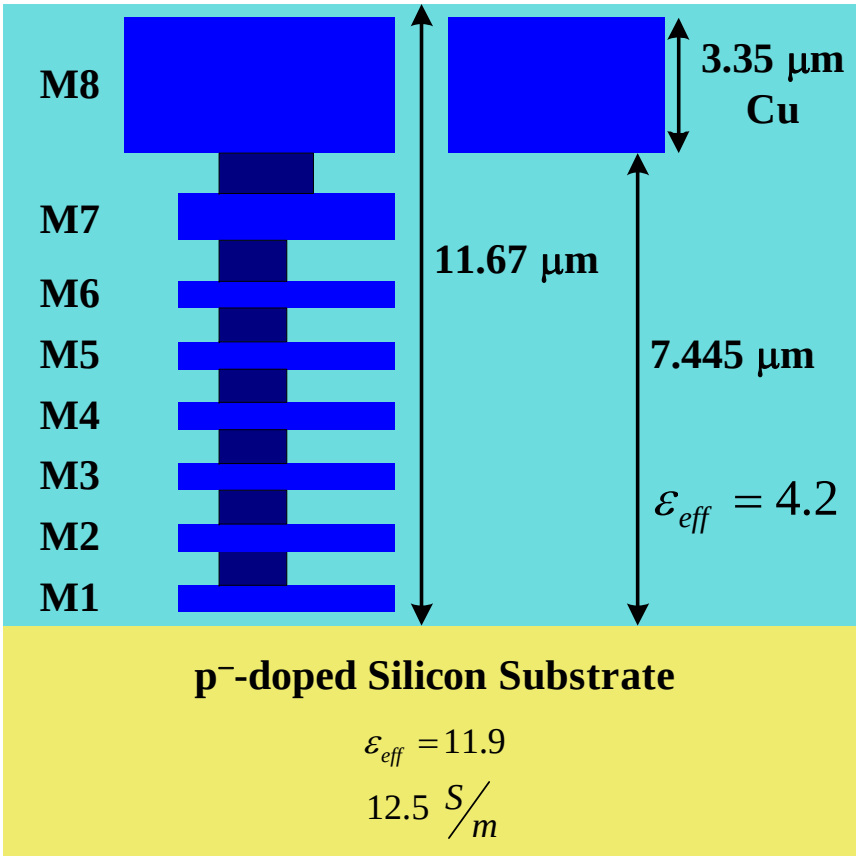


Figure 3.2 Cross-section view of the back-end from the technology.

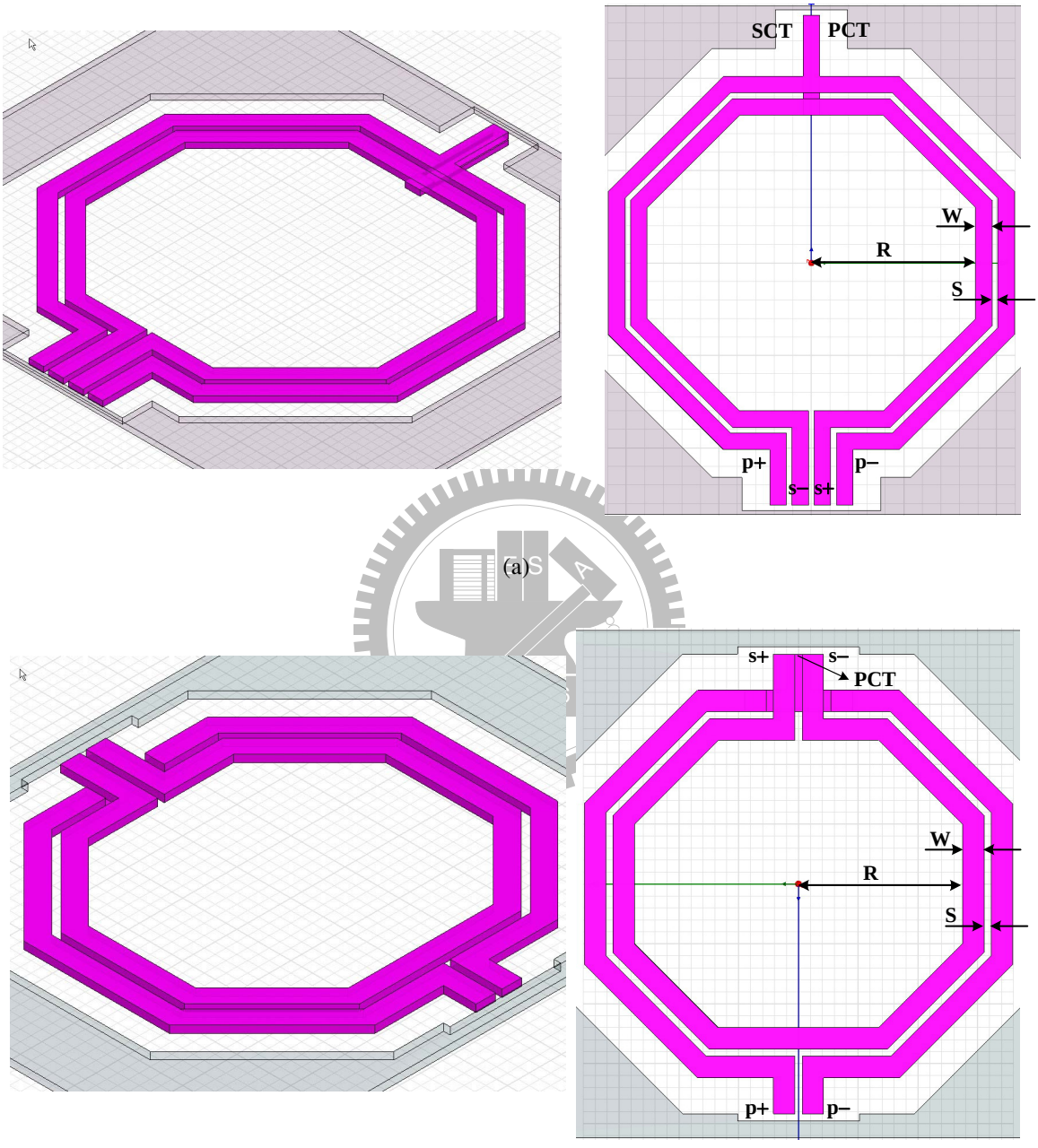


Figure 3.3 The metal structure of (a) XFMR-I, and (b) XFMR-II.

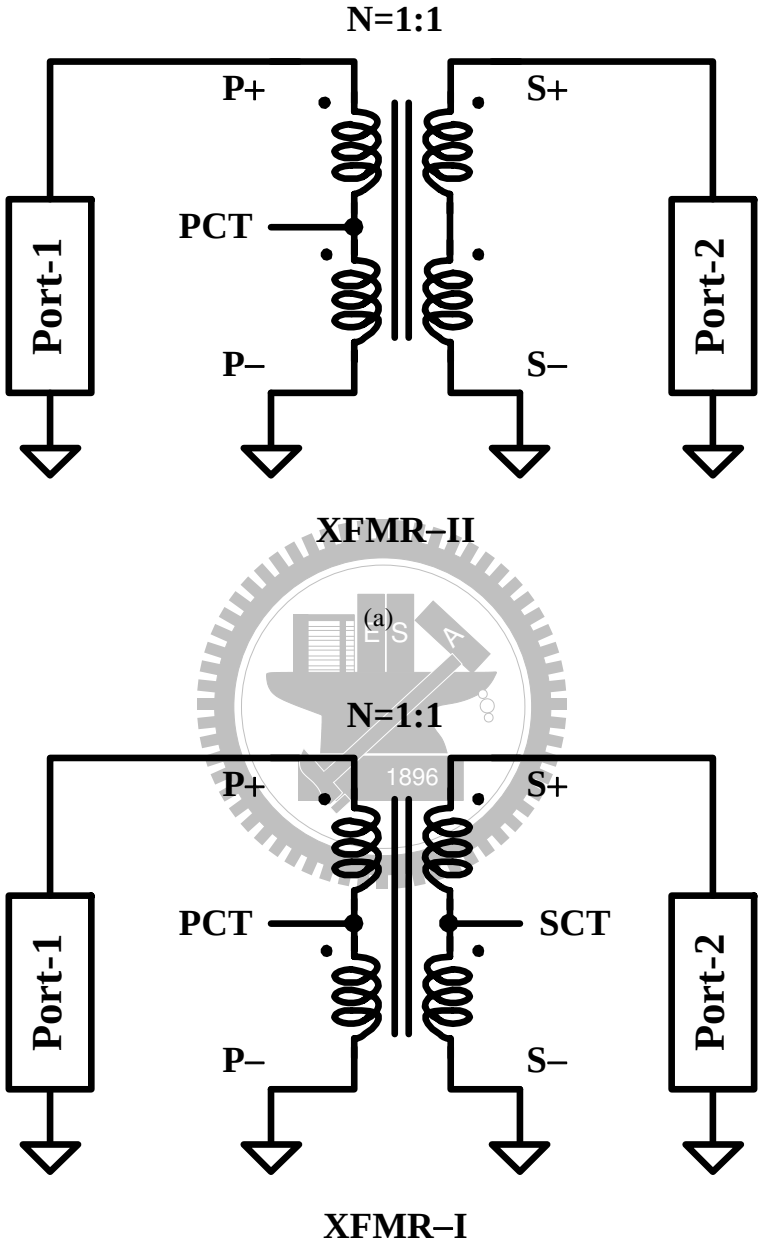


Figure 3.4 The circuit connections of the transformer to be tested. (a) XFMR-I, and (b) XFMR-II.

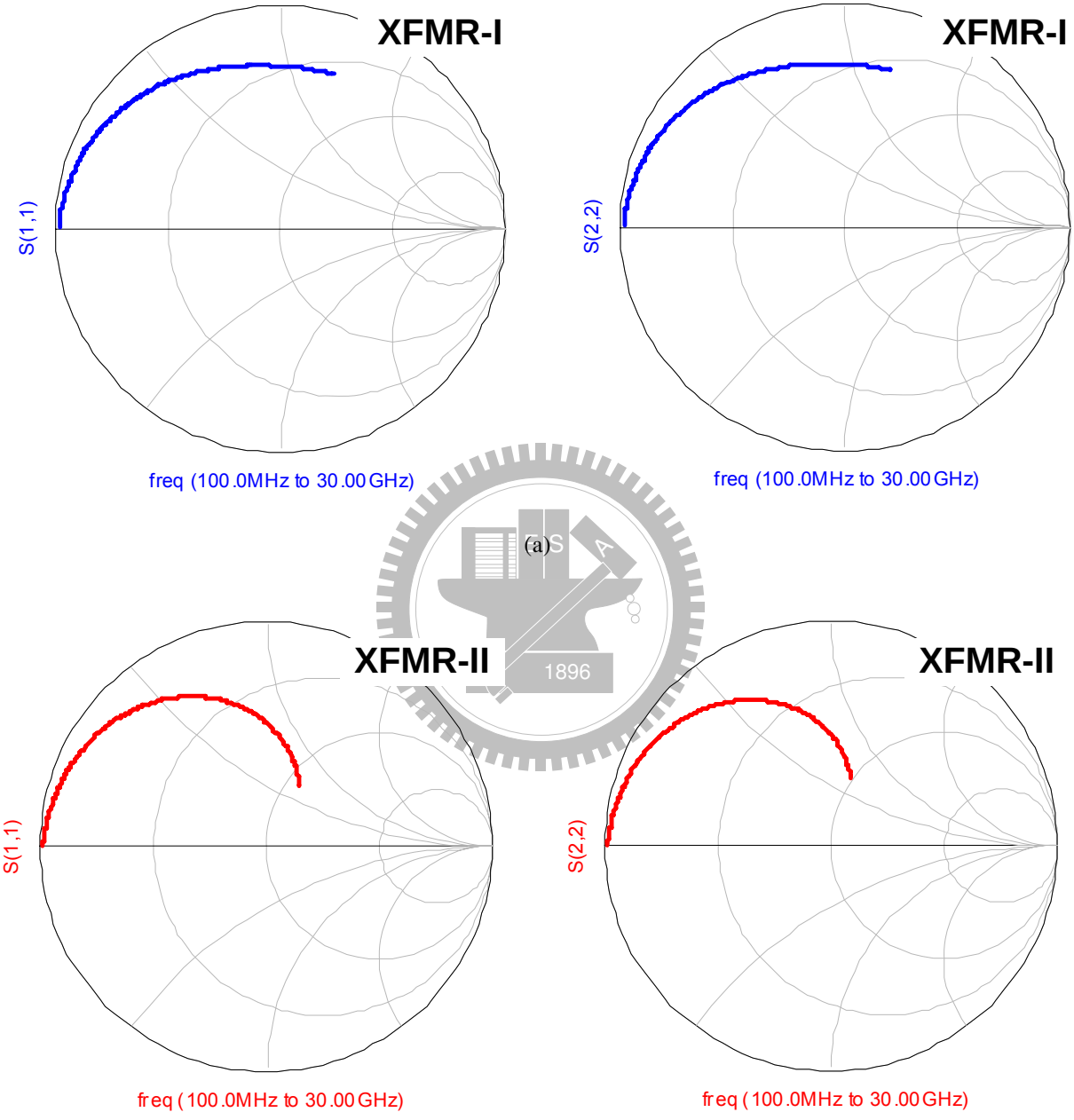
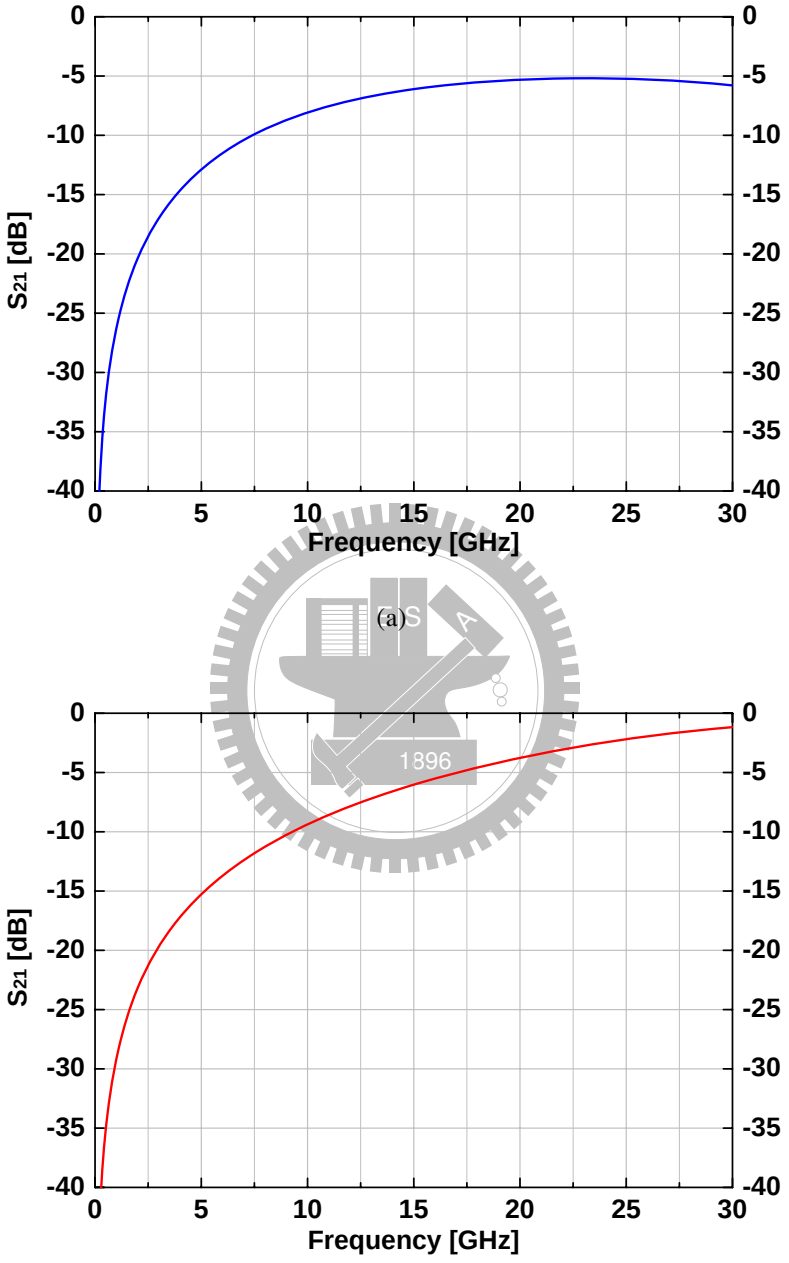


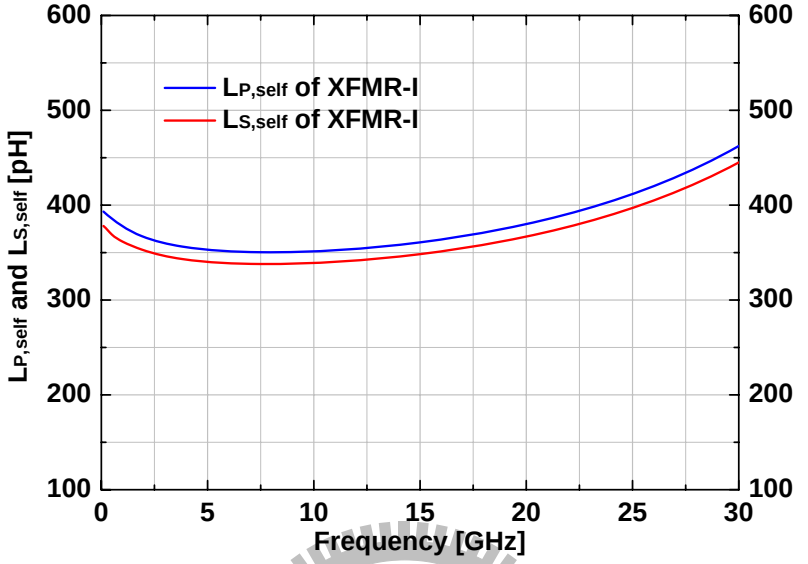
Figure 3.5 Simulated S_{11} and S_{22} of (a) XFMR-I, and (b) XFMR-II.



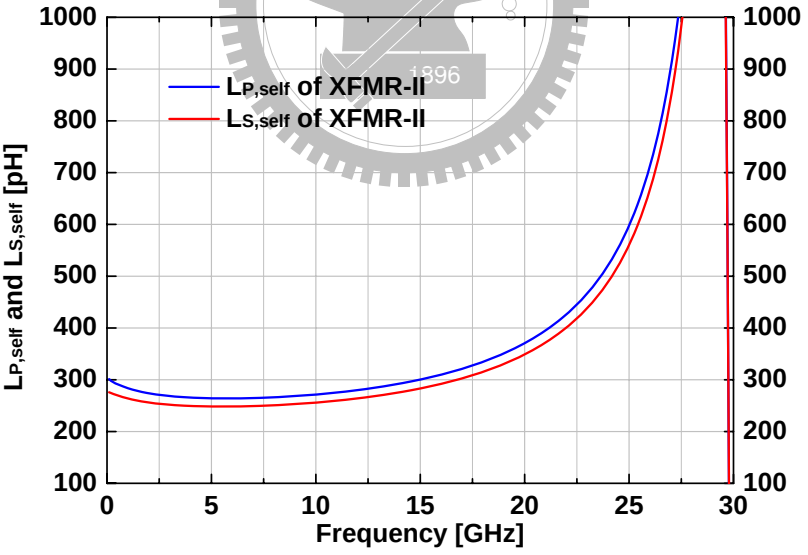
(a)

(b)

Figure 3.6 Simulated S_{21} of (a) XFMR-I, and (b) XFMR-II.

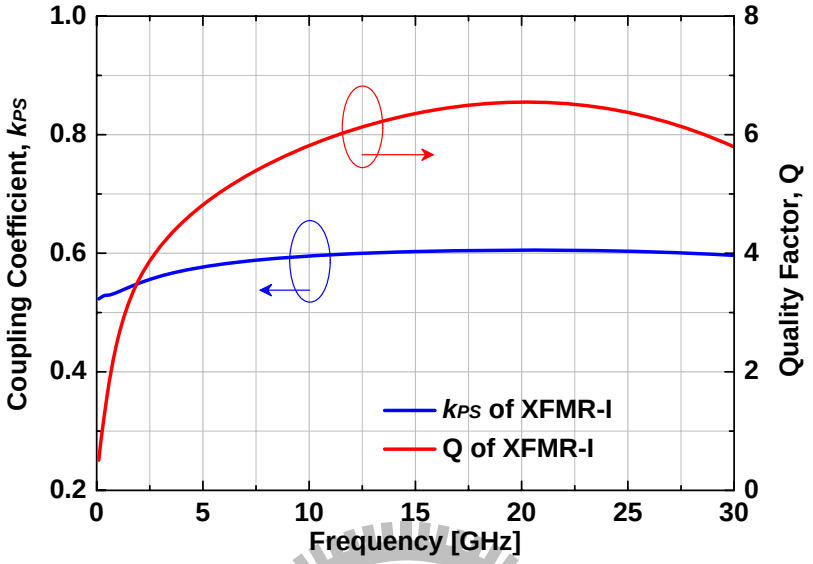


(a)

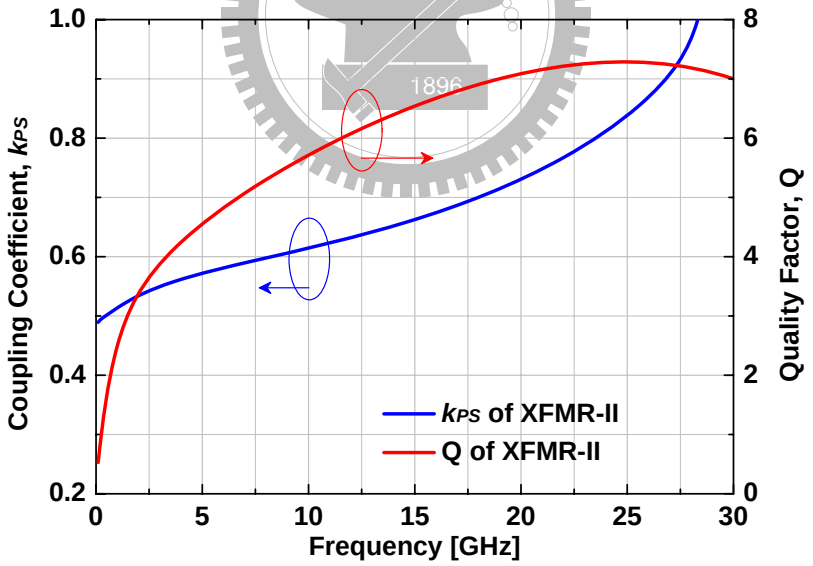


(b)

Figure 3.7 Simulated self-inductance of primary and secondary windings $L_{P,\text{self}}$ and $L_{S,\text{self}}$ of (a) XFMR-I, and (b) XFMR-II.



(a)



(b)

Figure 3.8 Simulated coupling-coefficient k_{PS} and quality factor Q of (a) XFMR-I, and (b) XFMR-II.

where Y_{11} (or Y_{22}) is the input admittance at primary (or secondary) side when output is short. From (3.1)–(3.4) it follows

$$k_{PS} = \sqrt{\frac{\left(Y_{11}^{-1} - Z_{11}\right) Z_{22}}{\Im\{Z_{11}\}\Im\{Z_{22}\}}} \tag{3.5}$$

Note that the coupling coefficient k_{PS} has its minimum value at the self-resonant frequency. Beyond the self-resonant frequency, k_{PS} grows over than a value of 1. However, it is not physically possible because the coupling in a passive system is limited to a maximum value of 1. In addition, such a behavior can be explained taking (3.5) into consideration as the relation is validated to frequencies below resonant frequency. The quality factor of the transformer is extracted from the impedance or admittance parameters as

$$\begin{aligned} Q &= \frac{\Im\{Z_{11}\}}{\Re\{Z_{11}\}}\Big|_{\text{output open}} \\ &= \frac{\Im\{Y_{11}^{-1}\}}{\Re\{Y_{11}^{-1}\}}\Big|_{\text{output short}} \end{aligned} \tag{3.6}$$

The afore-mentioned on-chip transformers are applied to the design of double-balanced current-mode up-conversion mixer in the following section.

3.2 Operational Principles

The block diagram of the proposed current-mode CMOS current-mode direct-conversion transmitter front-end is shown in Fig. 3.9. The transmitter is composed of a current-mode double-balanced up-conversion mixer, a baseband current buffer/repeater, a VCO, and a VCO buffer/repeater. The single-ended IF input current signal i_{if} is transformed into differential IF current signals i_{if+} and i_{if-} by the off-chip transformer. The baseband current buffer/repeater will output the differential IF current signals into two-pair differential signals $i_{if+,1}$, $i_{if-,1}$, $i_{if+,2}$, and $i_{if-,2}$ where $i_{if+,1} = i_{if+,2}$ and $i_{if-,1} = i_{if-,2}$. The integrated VCO provides LO signals for up-conversion mixer. The differential transformer-based VCO buffer/repeater not only enhances the isolation between the VCO and mixer, but also provides the two-pair differential LO signals $i_{lo+,1}$, $i_{lo-,1}$, $i_{lo+,2}$, and $i_{lo-,2}$ for the mixer where $i_{lo+,1} = i_{lo+,2}$ and $i_{lo-,1} = i_{lo-,2}$. Through the current-mode mixer, the signals at

baseband frequency are directly up-converted to the RF frequency by mixing with LO current signals. The double-balanced up-conversion mixer finally sends out the RF current signal i_{rf} to the following power amplifier.

The detailed operational principles and circuit designs of the current-squaring circuit, current-mode double-balanced up-conversion mixer, VCO, and transformer-based VCO buffer/repeater, and baseband current amplifier/repeater are described in the following sections.

3.3 Circuit Designs

3.3.1 Current-Mode Up-Conversion Mixer

The core of the proposed current-mode double-balanced up-conversion mixer is composed of four analog current-squaring circuits, as shown in Fig. 3.10, which are originally modified from [161], [162]. The transistors M_1–M_4 are biased in the saturation region. The bulk and source of M_2 and M_4 are separated to reduce the parasitic capacitances at the nodes N_1 and N_2. Lower signal loss is achieved due to smaller parasitic capacitances appeared at nodes N_1 and N_2. With the resistor R_1 (R_2), the impedance of the path from the node N_1 (N_2) to ground through the source-to-bulk parasitic capacitance of M_2 (M_4) is increased. Hence, the signal loss to ground is further reduced.

The current-squaring circuit is further improved by adding the transistor M_4 which acts as a current buffer and keeps the V_{DS} of M_3 the same as the V_{DS} of M_1 in order to alleviate the channel length modulation effect between M_1 and M_3. The current i_1 is multiplied by the current-mirror circuit formed by M_1 and M_3, where the aspect ratio of M_3 (M_4) is N times that of M_1 (M_2). The sum of the gate-to-source voltages of M_1 and M_2 is kept constant and equal to V_{DD}, where $V_{DD} = (v_{GS,M_1} + v_{GS,M_2})$. Suppose that the respective threshold voltages of M_1 and M_2 are $(V_{th} - \Delta V_{TH})$ and $(V_{th} + \Delta V_{TH})$ where $V_{th} = (V_{th,M_1} + V_{th,M_2})/2$ and $\Delta V_{TH} = (V_{th,M_2} - V_{th,M_1})/2$, and based on the square-law drain current equation for simplicity, the relationship among i_{in}, i_O, v_{GS,M_1}, and v_{GS,M_2} is

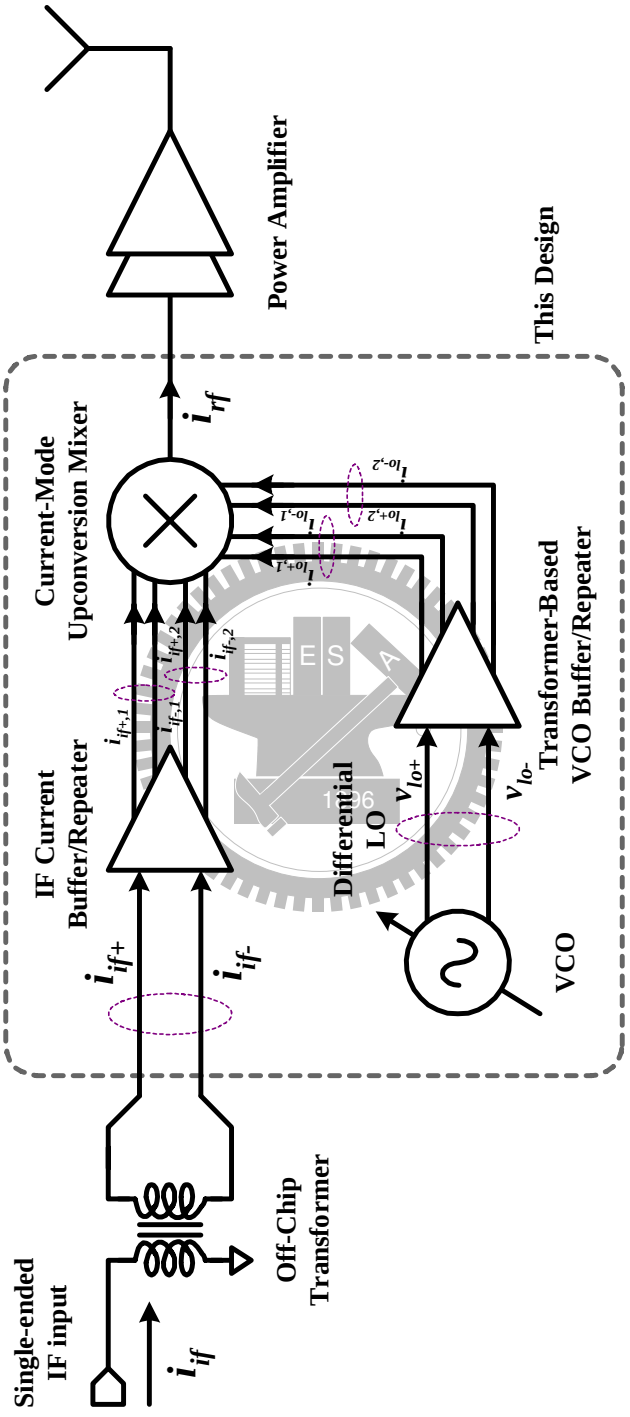


Figure 3.9 Block diagram of the proposed current-mode transmitter front-end.

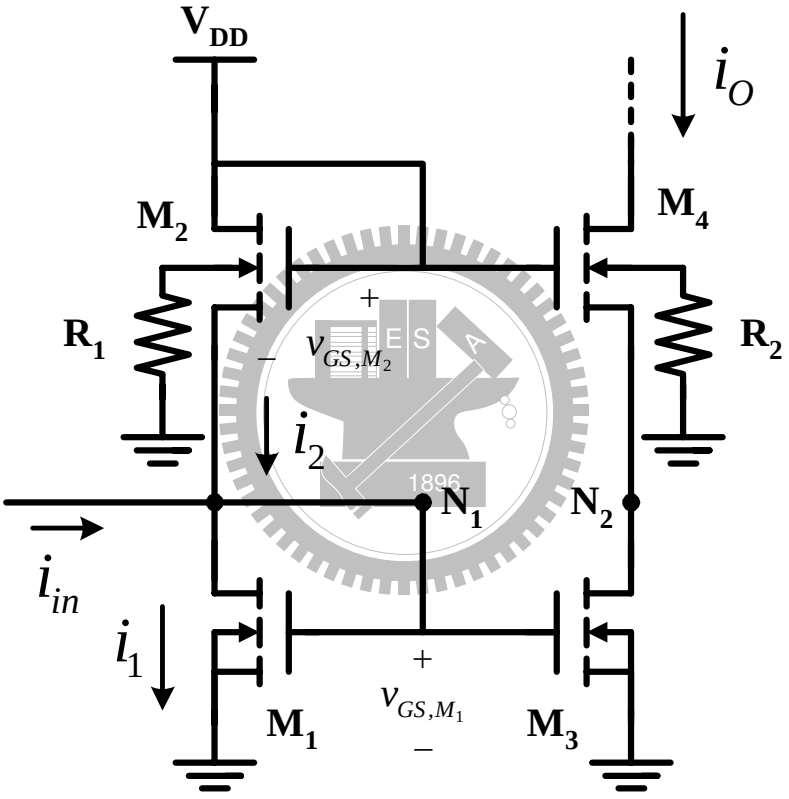


Figure 3.10 Circuit diagram of current-squaring circuit.

expressed as

$$v_{GS,M_1} = \left(\frac{V_{DD}}{2} - \Delta_{VTH}\right) + \frac{i_{in}}{k_n \frac{W}{L}(V_{DD} - 2V_{th})} \tag{3.7}$$

$$v_{GS,M_2} = \left(\frac{V_{DD}}{2} - \Delta_{VTH}\right) - \frac{i_{in}}{k_n \frac{W}{L}(V_{DD} - 2V_{th})} \tag{3.8}$$

$$i_O = N \times i_1 = N \times \left(\frac{i_{in}^2}{16 I_B} + \frac{i_{in}}{2} + I_B\right) \tag{3.9}$$

$$I_B \equiv \frac{1}{8} k_n \frac{W}{L}(V_{DD} - 2V_{th})^2 \tag{3.10}$$

where V_{th} is the threshold voltage, W/L is the channel width to channel length ratio of the MOS devices, and $k_n = \mu_n C_{ox}$ is the zero vertical-field mobility μ_n multiplied by the oxide capacitance per unit area C_{ox}. From the first term of (3.9), the current-squaring function is realized. The second and third terms of (3.9) are unwanted components and are to be removed. With the input $i_{in} = I_{LO}\cos\omega_{LO}t + I_{IF}\cos\omega_{IF}t$, the output i_O of the proposed square circuits can be derived as

$$\begin{aligned} i_O &= N \times \left[\frac{I_{LO}^2(1 + \cos 2\omega_{LO}t) + I_{IF}^2(1 + \cos 2\omega_{IF}t)}{32 I_B}\right] \\ &\quad + N \times \left\{\frac{I_{LO} I_{IF}\left[\cos(\omega_{LO} + \omega_{IF})t + \cos(\omega_{LO} - \omega_{IF})t\right]}{16 I_B}\right\} \\ &\quad + N \times \frac{(I_{LO}\cos\omega_{LO}t + I_{IF}\cos\omega_{IF}t)}{2} + N I_B \end{aligned} \tag{3.11}$$

Shown in Fig. 3.11 is the proposed current-mode double-balanced up-conversion mixer which consists of four current-squaring circuits and an on-chip octagonal transformer. Four signal inputs of this mixer are $i_{in1} = (i_{lo+,1} + i_{if+,1})$, $i_{in2} = (i_{lo-,1} + i_{if-,1})$, $i_{in3} = (i_{lo+,2} + i_{if-,2})$, and $i_{in4} = (i_{lo-,2} + i_{if+,2})$. $i_{if+,1}$, $i_{if-,1}$, $i_{if+,2}$, and $i_{if-,2}$ are two-pair IF current signals where $i_{if+,1} = i_{if+,2} = i_{if+} = I_{IF}\cos\omega_{IF}t$ and $i_{if-,1} = i_{if-,2} = i_{if-} = -I_{IF}\cos\omega_{IF}t$. Furthermore, $i_{lo+,1}$, $i_{lo-,1}$, $i_{lo+,2}$ and $i_{lo-,2}$ are two-pair differential LO current signals where $i_{lo+,1} = i_{lo+,2} = i_{lo+} = I_{LO}\cos\omega_{LO}t$ and $i_{lo-,1} = i_{lo-,2} = i_{lo-} = -I_{LO}\cos\omega_{LO}t$. The summation of IF and LO current signals is performed by directly connecting the wires of LO and IF together without additional power dissipations.

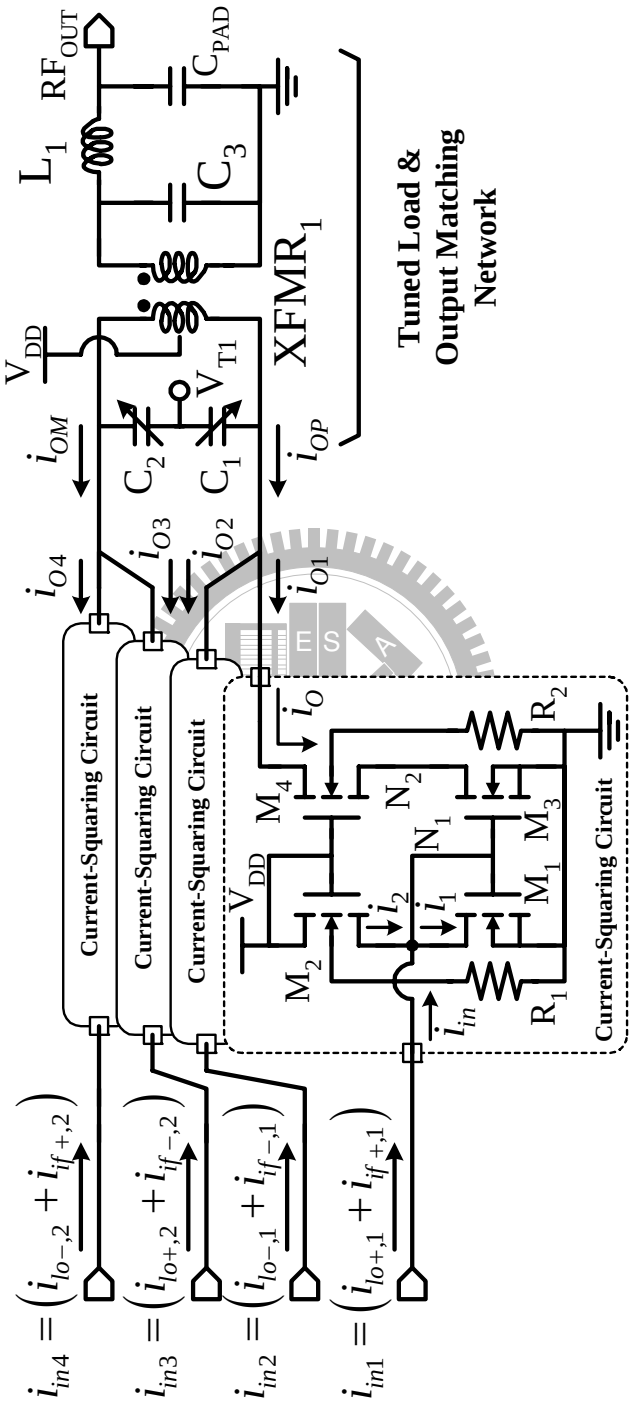


Figure 3.11 Circuit diagram of current-mode double-balanced up-conversion mixer.

As shown in (3.12)–(3.18), with the differential LO and IF signals, the LO and IF leakages which result from the second term of (3.9) can be eliminated at the output of the proposed current-mode mixer if the output currents i_{O1} i_{O4} of the four current-squaring circuits are summed together as $i_{OP} = (i_{O1} + i_{O2})$ and $i_{OM} = (i_{O3} + i_{O4})$. The summations of these current signals are performed using wire connections. In addition, as shown in (3.19), the even-order harmonics resulted from squaring terms of LO and IF current signals are eliminated through the subtraction of i_{OP} and i_{OM}.

$$i_{in1} = (I_{LO}\cos\omega_{LO}t + I_{IF}\cos\omega_{IF}t) \tag{3.12}$$

$$i_{in2} = (-I_{LO}\cos\omega_{LO}t - I_{IF}\cos\omega_{IF}t) \tag{3.13}$$

$$i_{in3} = (I_{LO}\cos\omega_{LO}t - I_{IF}\cos\omega_{IF}t) \tag{3.14}$$

$$i_{in4} = (-I_{LO}\cos\omega_{LO}t + I_{IF}\cos\omega_{IF}t) \tag{3.15}$$

$$\begin{aligned} i_{OP} &= i_{O1} + i_{O2} \\ &= N \times \left[\left(\frac{i_{in1}^2}{16I_B} + \frac{i_{in1}}{2} + I_B \right) + \left(\frac{i_{in2}^2}{16I_B} + \frac{i_{in2}}{2} + I_B \right) \right] \\ &= I_{DC} + N \times \frac{1}{16I_B} \left(I_{LO}^2 \cos 2\omega_{LO}t + I_{IF}^2 \cos 2\omega_{IF}t \right) \\ &\quad + N \times \frac{I_{LO}I_{IF}}{8I_B} \left[\cos\left(\omega_{LO} + \omega_{IF}\right)t + \cos\left(\omega_{LO} - \omega_{IF}\right)t \right] \end{aligned} \tag{3.16}$$

$$\begin{aligned} i_{OM} &= i_{O3} + i_{O4} \\ &= N \times \left[\left(\frac{i_{in3}^2}{16I_B} + \frac{i_{in3}}{2} + I_B \right) + \left(\frac{i_{in4}^2}{16I_B} + \frac{i_{in4}}{2} + I_B \right) \right] \\ &= I_{DC} + N \times \frac{1}{16I_B} \left(I_{LO}^2 \cos 2\omega_{LO}t + I_{IF}^2 \cos 2\omega_{IF}t \right) \\ &\quad - N \times \frac{I_{LO}I_{IF}}{8I_B} \left[\cos\left(\omega_{LO} + \omega_{IF}\right)t + \cos\left(\omega_{LO} - \omega_{IF}\right)t \right] \end{aligned} \tag{3.17}$$

$$I_{DC} = N \times \left[2I_B + \frac{\left(I_{LO}^2 + I_{IF}^2 \right)}{16 I_B} \right] \tag{3.18}$$

$$i_{OP} - i_{OM} = \frac{N I_{LO} I_{IF}}{4 I_B} \left[\cos\left(\omega_{LO} + \omega_{IF} \right) t + \cos\left(\omega_{LO} - \omega_{IF} \right) t \right] \tag{3.19}$$

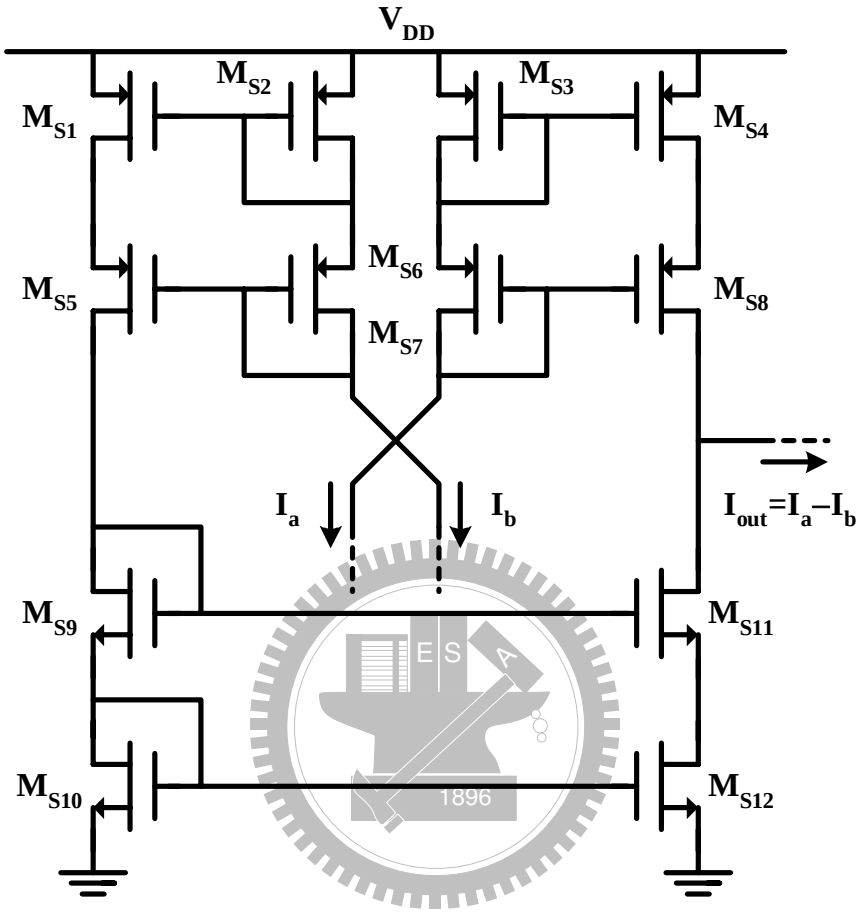
Some circuits that deal with current subtraction have already been reported in [162] and [167]. As shown in Fig. 3.12(a) [162], the current-mirror circuit is adopted to deal with subtraction of current signals. The two current signals I_a and I_b that are to be subtracted flows through two imbalanced paths. The two imbalanced paths will result in gain and phase differences. Additional poles from the current mirror will lead to loss of current signals in high frequency. Furthermore, higher voltage headroom and additional power are required for this subtraction circuit of current signals. As shown in Fig. 3.12(b) [167], another subtraction circuit of current signals by LC phase-shift network is adopted. This circuit can perform good subtraction, but only at the resonant frequency. No additional power consumption is required, and this circuit avoids excessive voltage drop. When dealing with signals with wide bandwidth, the LC phase-shift network will not be suitable.

In this design shown in Fig. 3.11, the on-chip passive transformer $XFMR_1$ is adopted for high-frequency and wide-bandwidth subtraction of current signals. The use of $XFMR_1$ avoids the excessive voltage drop, and no additional power consumption is required. This also ensures that the proposed current-mode double-balanced up-conversion mixer operates well at a low power supply. From (3.9) and with the four inputs of the mixer, the resultant RF output current $i_{rf} = \eta \times (i_{OP} - i_{OM})$ can be derived as

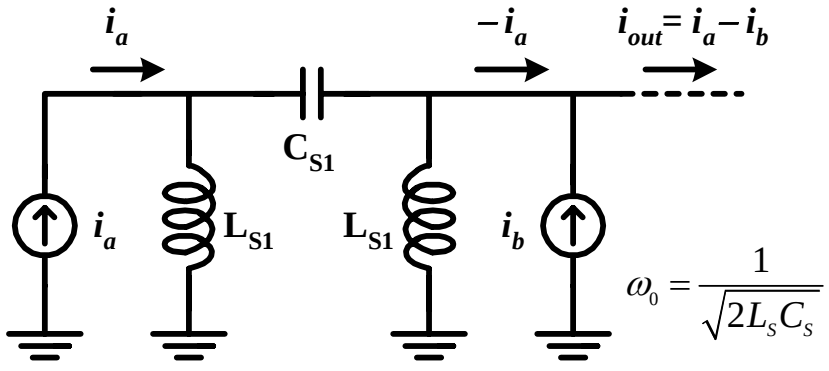
$$i_{rf} = \frac{\eta N I_{LO} I_{IF}}{4 I_B} \left[\cos(\omega_{LO} + \omega_{IF}) t + \cos(\omega_{LO} - \omega_{IF}) t \right] \tag{3.20}$$

where η represents the losses from the on-chip transformer $XFMR_1$ and the output impedance matching network. From (3.20), it can be seen that the function of mixer is realized. With the exclusion of the loss η, the intrinsic current conversion gain $CG_{intrinsic}$ of the proposed current-mode double-balanced up-conversion mixer is expressed as

$$\begin{aligned} CG_{intrinsic} &\approx \frac{(i_{OP} - i_{OM}) \mid_{\omega=(\omega_{LO}+\omega_{IF}) \text{or} \omega=(\omega_{LO}-\omega_{IF})}}{2(i_{if_+} - i_{if_-}) \mid_{\omega=\omega_{IF}}} \\ &= \frac{N I_{LO}}{16 I_B} \end{aligned} \tag{3.21}$$



(a)



(b)

Figure 3.12 Schematic diagram of the subtraction of current signals by (a) current mirror circuits [162], (b) LC phase-shift network [167].

As can be seen from (3.21), the $CG_{intrinsic}$ is proportional to the magnitude of the LO current I_{LO}.

In the advanced deep sub-micron CMOS technologies, the relationship between the drain current i_{DS} and the gate overdrive voltage $v_{OV} = (v_{GS} - V_{th})$ of CMOS devices in the saturation region is not exactly square due to short channel effects, and the drain current i_{DS} is approximated as [163], [164]

$$i_{DS} \approx \frac{1}{2} k_n \frac{W}{L} \frac{\mu_n}{(1 + \theta v_{OV})} \frac{v_{OV}^2}{\left(1 + \frac{v_{OV}}{E_C L}\right)} (1 + \lambda v_{DS}) \tag{3.22}$$

where E_C is the critical value of the horizontal electric field, θ is inversely proportional to the oxide thickness, and the coefficient λ models the effect of the channel length modulation which is related to v_{DS}. From the simulation under the supply voltage of 1 V, the threshold voltages of M_1 and M_2 are about 420 mV and 500 mV, and the gate-to-source voltages of M_1 and M_2 are about 455 mV and 545 mV, respectively. Hence, the gate overdrive voltages of M_1 and M_2 are small enough such that $v_{OV} \ll \theta^{-1}$ and $v_{OV} \ll E_C L$. The drain current i_{DS} is further simplified approximately as the following equation to analyze the second-order effects of the proposed current-mode double-balanced up-conversion mixer.

$$i_{DS} \approx \frac{1}{2} k_n \frac{W}{L} v_{OV}^2 (1 + \lambda v_{DS}) \tag{3.23}$$

Although both M_1 and M_2 are with the same device size and are diode-connected, the drain-to-source voltages of M_1 and M_2 are different due to the fact that the latter suffers from body effect. As a result, the channel length modulation effect should be considered. From Fig. 3.10, $V_{DD} = (v_{DS,M_1} + v_{DS,M_2})$. If $\delta = (v_{DS,M_2} - v_{DS,M_1})/2$ is assumed, $v_{DS,M_1} = (V_{DD} - 2\delta)/2$ and $v_{DS,M_2} = (V_{DD} + 2\delta)/2$. After some derivations, the expression i_O in (3.9) is modified and expressed as

$$i_{O,\text{short}} \approx N \times \left(\chi_1 \frac{i_{in}^2}{16 I_B} + \chi_2 \frac{i_{in}}{2} + \chi_3 I_B \right) \tag{3.24}$$

where

$$\chi_1 = \frac{2(2 + \lambda V_{DD} - 6\lambda\delta)}{(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\lambda\delta) + 2\lambda\delta(2 + \lambda V_{DD} + 2\lambda\delta)} \tag{3.25}$$

$$\chi_2 = \frac{2(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\lambda\delta) - (2 + \lambda V_{DD} - 2\lambda\delta)^2}{(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\lambda\delta) + 2\lambda\delta(2 + \lambda V_{DD} + 2\lambda\delta)} \tag{3.26}$$

$$\chi_2 = \frac{(2+\lambda V_{DD})(2+\lambda V_{DD}+2\lambda\delta)(2+\lambda V_{DD}-4\lambda\delta)}{2\left[(2+\lambda V_{DD})(2+\lambda V_{DD}-4\lambda\delta)+2\lambda\delta(2+\lambda V_{DD}+2\lambda\delta)\right]} \tag{3.27}$$

Note that χ_1 and χ_2 are less than 1, whereas χ_3 is greater than 1. As $V_{DD} = 1V$, $\lambda \approx 0.77V^{-1}$, and $\delta \approx 45mV$, $\chi_1 \approx 0.68$, $\chi_2 \approx 0.97$, and $\chi_3 \approx 1.38$. Furthermore, the above derivations only consider body effect and channel length modulation effect, and the rest of short channel effects are ignored under the design condition of small v_{OV} of M_1 and M_2. The detailed derivations of (3.24)–(3.27) are shown in Appendix B.

Moreover, even if the drain-to-source voltage differences of M_1 and M_2 are the same, the channel-length modulation still has effects on the proposed squaring circuit. In this case where $\delta = 0$ and $\lambda \neq 0$, (3.24) is simplified to

$$i_{O,\text{short}} \approx N \times \left(\gamma_1 \frac{i_{in}^2}{16I_B} + \frac{i_{in}}{2} + \gamma_2 I_B\right) \tag{3.28}$$

where

$$\gamma_1 = \left(1+\frac{\lambda V_{DD}}{2}\right)^{-1} \tag{3.29}$$

$$\gamma_2 = \left(1+\frac{\lambda V_{DD}}{2}\right) \tag{3.30}$$

Note that γ_1 is less than 1, whereas γ_2 is greater than 1.

From the above derivations (3.21), (3.24) and (3.25), the $CG_{intrinsic}$ with the body effect and channel length modulation effect can be further expressed as

$$CG_{intrinsic} \approx \chi_1 \frac{N I_{LO}}{16 I_B} \tag{3.31}$$

This indicates that the current conversion gain of the proposed mixer with short-channel devices is less than that with long-channel devices. Besides, the parameter λ that models channel length modulation has a significant effect on $CG_{intrinsic}$.

Under the simulated conditions of the IF Frequency at 200 MHz and the LO frequency at 24 GHz, the relationship among the simulated $CG_{intrinsic}$, the equivalent calculated input LO power $P_{LO,IN}$, and the amplitude of the differential LO current signal $i_{diff-loin} = 2\times(i_{lo+}-i_{lo-})$ is depicted in Fig. 3.13. It can be seen that the simulated $CG_{intrinsic}$ is higher than 0 dB if the amplitude of $i_{diff-loin}$ is greater than 1.5 mA or $P_{LO,IN}$ is greater than –8.2 dBm. Fig. 3.14 is the relationship between the simulated $CG_{intrinsic}$ and the amplitude of differential IF current signal $i_{diff-ifin} = 2\times(i_{if+}-i_{if-})$. When the amplitude of $i_{diff-loin}$ is

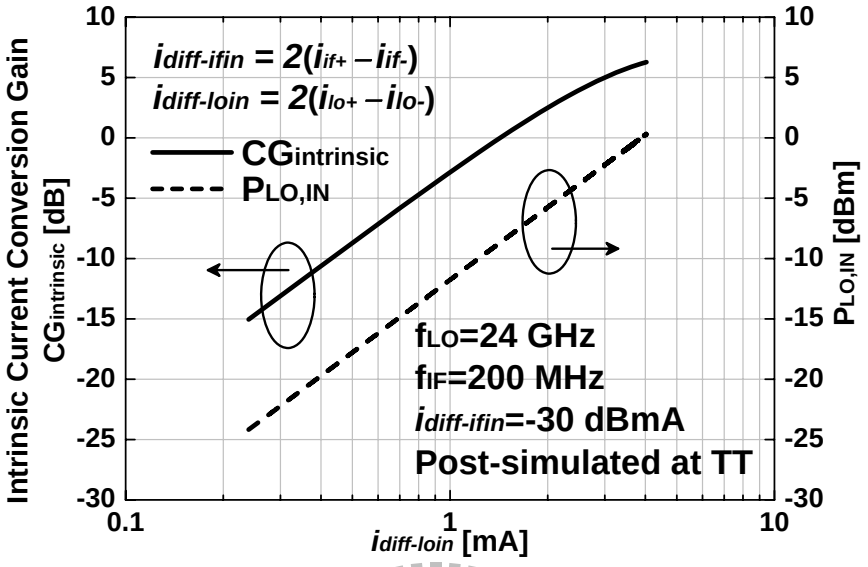


Figure 3.13 The relation among simulated $CG_{intrinsic}$, the equivalent $P_{LO,IN}$, and the amplitude of the differential LO current signal $i_{diff-loin}$.

equal to 1 mA where the equivalent $P_{LO,IN}$ is equal to –11.7 dBm, the simulated $CG_{intrinsic}$ is –2.3 dB and the 1-dB compression point of intrinsic current conversion gain (C_{P1dB}) is –0.9 dBmA. As the amplitude of $i_{diff-loin}$ is increased to 3 mA where the equivalent $P_{LO,IN}$ is equal to –2.9 dBm, the simulated $CG_{intrinsic}$ achieves 5.0 dB and the C_{P1dB} equals 1.8 dBmA.

The operating frequency of the proposed current-mode mixer can be altered by varying the control voltage V_{T1} in order to change the capacitance values of N+/N-well varactors C_1 and C_2. The output matching network of the proposed mixer formed by C_3, C_{PAD}, and L_1 is designed to match 50Ω for the purpose of measurement.

3.3.2 Voltage-Controlled Oscillator

The cross-coupled VCO is illustrated in Fig. 3.15. The inductor L_2 is realized by on-chip center-tapped octagonal symmetric inductor and the N+/N-well varactors C_4 and C_5. The cross-coupled transistors M_6 and M_7 provide negative transconductances to cancel the parasitic resistances of the inductor and varactors to guarantee oscillation. The values

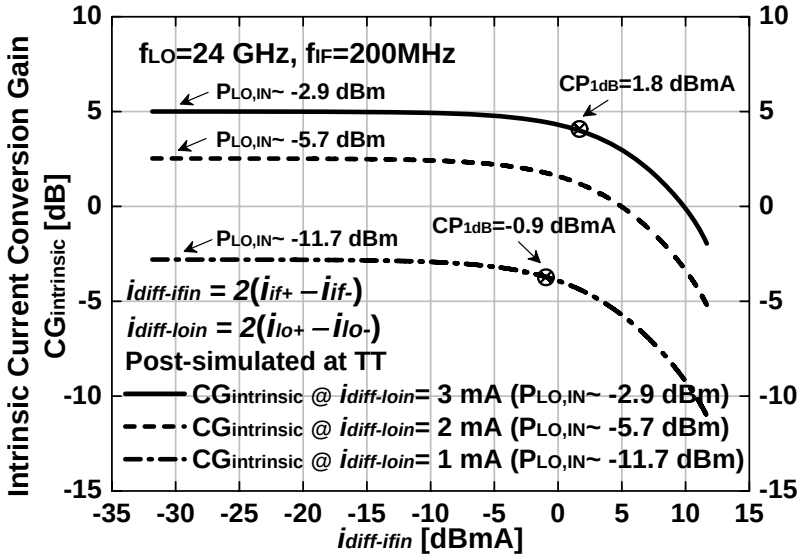


Figure 3.14 The relation between simulated $CG_{intrinsic}$ and the amplitude of the differential IF current signal $i_{diff-ifin}$.

of varactors are tuned by varying the control voltage V_{T2} to obtain the desired oscillation frequency.

Fig. 3.16 depicts the simulated tuning curve of the proposed VCO. The designed VCO can be tuned from 25 GHz to 27.5 GHz as the control voltage V_{T2} is varied from 0 V to 2 V. The operating frequency of VCO is over-designed to overcome the process variations. Shown in Fig. 3.17 is the simulated result of phase noise of the designed VCO. The phase noise is –117 dBc/Hz at 10-MHz offset from the LO frequency of 26 GHz with the V_{T2} of 1 V. The simulated power dissipation of the VCO is 3.89 mW from the supply voltage of 1 V.

3.3.3 Transformer-Based VCO Buffer/Repeater

The circuit diagram of transformer-based VCO buffer/repeater is shown in Fig. 3.18, which is realized by a fully differential amplifier with the loads of two transformers $XFMR_2$ and $XFMR_3$ in parallel and two N+/N-well varactors C_6 and C_7. M_8-M_{10} are biased in the saturation region. M_8 with long channel length is operated as a current

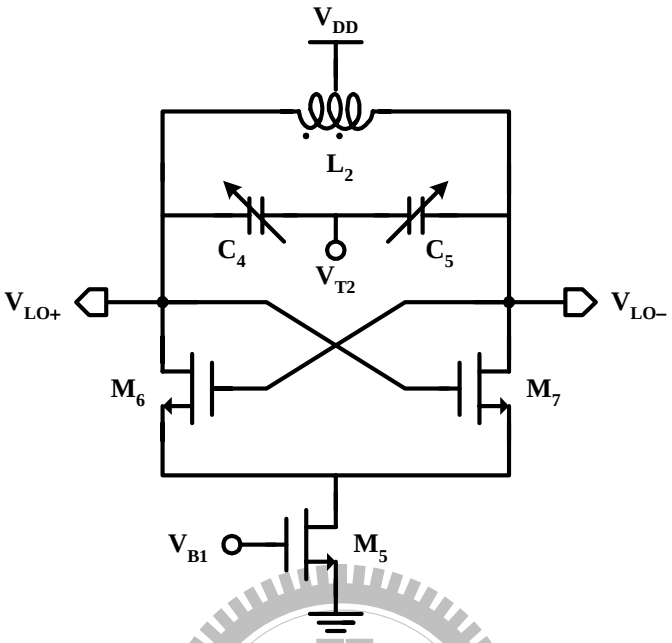


Figure 3.15 Circuit diagram of VCO.

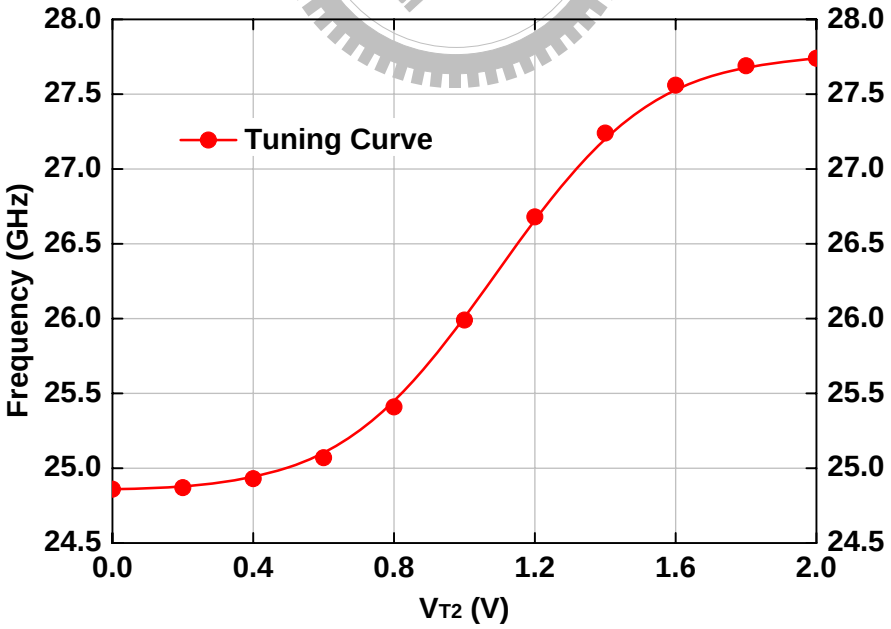


Figure 3.16 Simulated tuning curve of VCO.

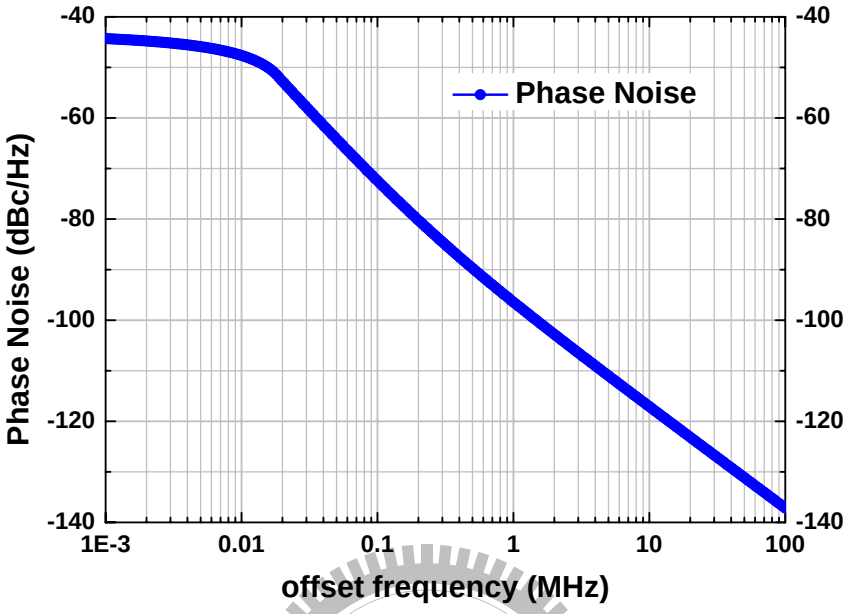


Figure 3.17 Simulated phase noise of the VCO.

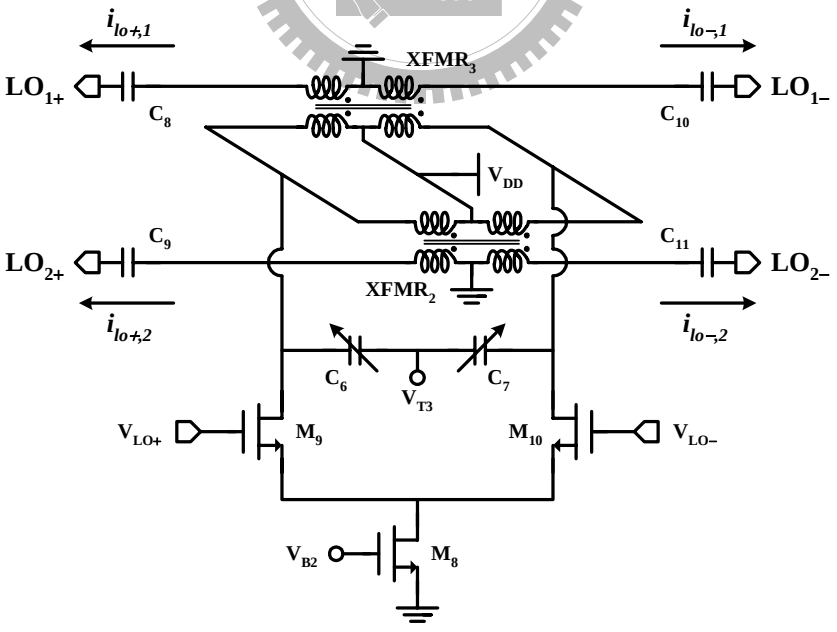


Figure 3.18 Circuit diagram of transformer-based VCO buffer/repeater.

source and provides the capability for common-mode rejection. C_8-C_{11} are dc blocking capacitors. The operating frequency of transformer-based VCO buffer/repeater is designed to track with the LO frequency by varying the control voltage of V_{T3}. As a result of the magnetic coupling of the transformers, four LO output currents $i_{lo+,1}$, $i_{lo-,1}$, $i_{lo+,2}$, and $i_{lo-,2}$ are provided, where $i_{lo+,1} = i_{lo+,2}$ and $i_{lo-,1} = i_{lo-,2}$.

Compared with generating the two differential LO current signals $i_{lo,1}$ and $i_{lo,2}$ by active current mirrors with the technique of series inductive peaking to extend the bandwidth, the proposed circuit has the advantage of lower power consumption and smaller phase and magnitude differences between the two differential LO current signals $i_{lo,1}$ and $i_{lo,2}$, but at the cost of moderate increase of chip area.

3.3.4 Baseband Current Buffer/Repeater

Shown in Fig. 3.19 is the fully balanced differential baseband current buffer/repeater which is based on current-mirror circuit. The input current signal $i_{if in+}$ ($i_{if in-}$) is copied to two identical output current signals $i_{if+,1}$ ($i_{if-,1}$) and $i_{if+,2}$ ($i_{if-,2}$). M_{11}–M_{16} are biased in the saturation region. Both M_{17} and M_{18} are diode-connected to provide bias voltage V_{B3} for M_{14}–M_{16}. C_{12} is the dc blocking capacitor. C_{13} is the bypass capacitor used to keep V_{B3} stable. Transistors M_{11}–M_{16} should be laid out carefully to minimize the number of possible mismatches of the two-pair differential baseband current signals.

3.3.5 Integrated Current-Mode Transmitter Front-End

The detailed connections of the proposed integrated current-mode transmitter front-end circuits are illustrated in Fig. 3.20. Table 4.1 shows the design parameters of the proposed current-mode double-balanced up-conversion mixer. Table 4.2 shows the design parameters of VCO and transformer-based VCO buffer/repeater. Table 4.3 shows the design parameters of baseband current buffer/repeater.

The performance of the proposed integrated CMOS current-mode transmitter front-end is verified by Cadence SpectreRF, Agilent ADS, and Ansoft Designer/Nexxim. Fig. 3.22 shows the simulated matching characteristics of IF port and RF port. The linearity is verified by Harmonic Balance analysis. Fig. 3.21 depicts the two-tone simulation results with

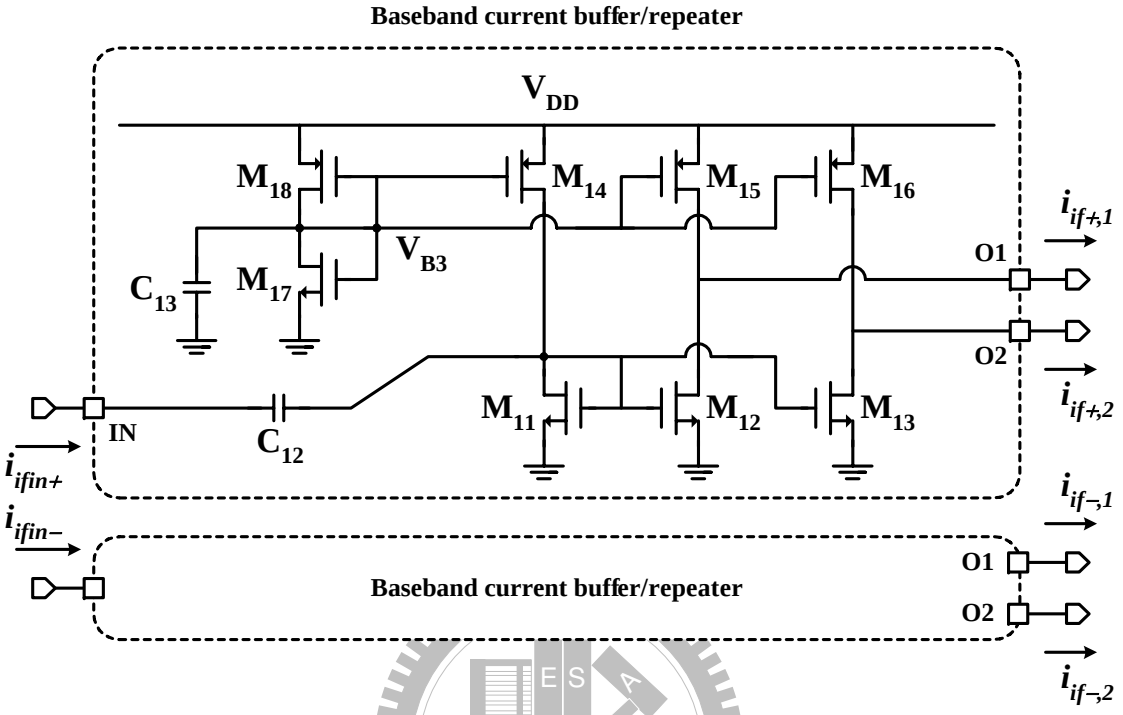


Figure 3.19 Circuit diagram of baseband current buffer/repeater.

Table 3.1
DEVICE PARAMETERS OF THE PROPOSED CURRENT-MODE DOUBLE-BALANCED UP-CONVERSION MIXER

Current-Squaring Circuit	
M_1, M_2	6 μm / 0.13 μm
M_3, M_4	48 μm / 0.13 μm
R_1, R_2	2 kΩ
Load and output matching network	
C_1, C_2	W = 1 μm, L= 0.3 μm, finger = 36 (N+/N-Well varactors)
C_3	20 fF
C_{PAD}	20 fF
L_1	488 pH
$XFMR_1$	Rad = 60 μm, W = 9 μm, S = 3 μm (XFMR Type–II)

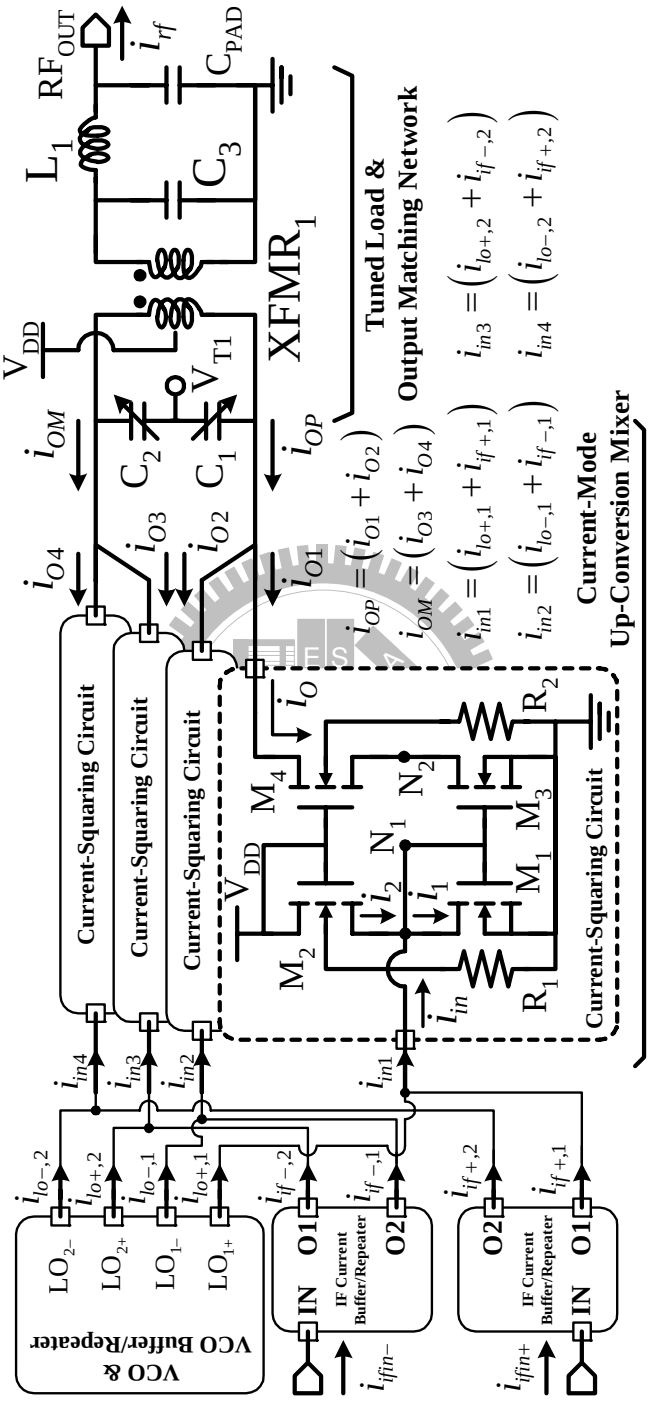


Figure 3.20 Detailed connections of the proposed integrated current-mode transmitter front-end circuits.

Table 3.2
DEVICE PARAMETERS OF VCO AND TRANSFORMER-BASED VCO BUFFER/REPEATER

VCO	
M_5	192 μm / 0.35 μm
M_6, M_7	60 μm / 0.13 μm
C_4, C_5	W = 1μm, L= 0.3μm, finger = 36 (N+/N-Well varactors)
L_2	210 pH
Transformer-based VCO buffer/repeater	
M_8	120 μm / 0.26 μm
M_9, M_{10}	30 μm / 0.13 μm
C_6, C_7	W = 1 μm, L= 0.3 μm, finger = 36 (N+/N-Well varactors)
C_8, C_9, C_{10}, C_{11}	200 fF
$XFMR_2$, $XFMR_3$	Rad = 80 μm, W = 9 μm, S = 3 μm (XFMR Type–I)

Table 3.3
DEVICE PARAMETERS OF BASEBAND CURRENT BUFFER/REPEATER

Baseband current buffer/repeater	
M_{11}	48 μm / 0.13 μm
M_{12}, M_{13}	96 μm / 0.13 μm
M_{14}	96 μm / 0.13 μm
M_{15}, M_{16}	192 μm / 0.13 μm
M_{17}	6 μm / 0.13 μm
M_{18}	12 μm / 0.13 μm
C_{12}	$>$ 30 pF
C_{13}	$>$ 10 pF

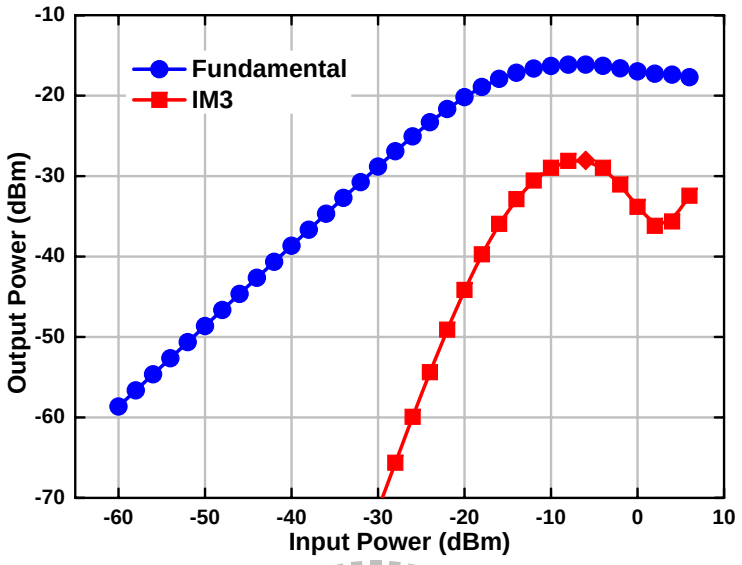
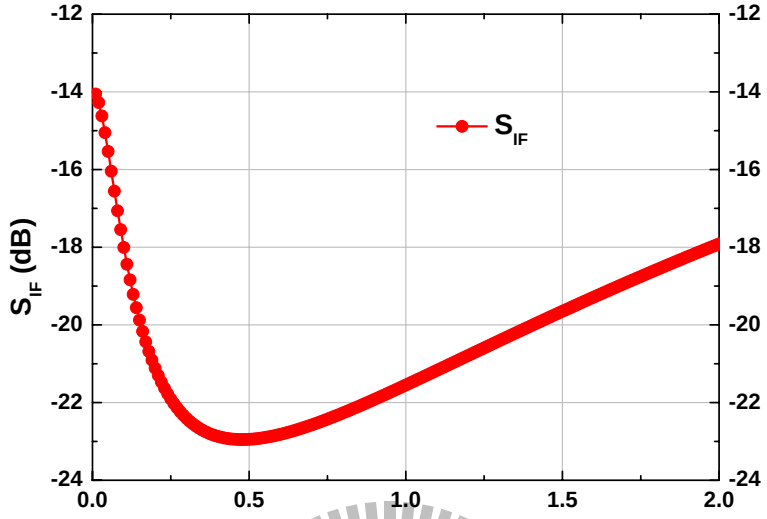


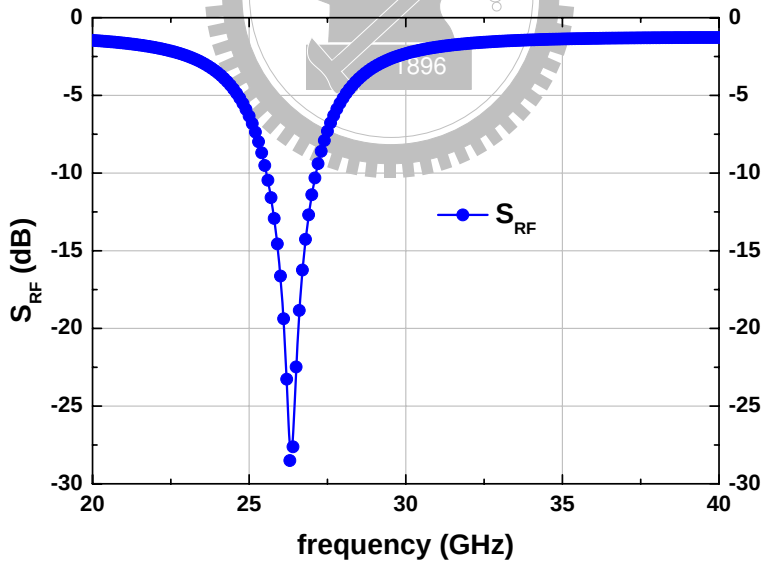
Figure 3.21 Simulated linearity performance of the proposed current-mode transmitter front-end.

a conversion power gain of 1.3 dB, an IP_{-1dB} of –22 dBm, a P_{IIP3} of –8.75 dBm, and a P_{OIP3} of –7.44 dBm. Fig. 3.23 shows the transient simulation results with two input baseband signals at 400 MHz and 500 MHz of which the signal level is –20 dBm and the LO signal at 26 GHz. The simulated average single-sideband (SSB) noise figure (NF) of the proposed current-mode transmitter front-end is about 9 dB. Generally, the noise figure is not an important design parameter for a transmitter design due to high signal-to-noise ratio (SNR) of determinable baseband signal.

From the supply voltage of 1 V, the total power dissipation of the whole circuits is 15.4 mW, where the power consumptions of the current-mode double-balanced up-conversion mixer, VCO, transformer-based VCO buffer/repeater, and baseband current buffer/repeater are 3.89 mW, 3.23 mW, 4.67 mW, and 3.58 mW, respectively.



(a)



(b)

Figure 3.22 Simulated matching characteristics of (a) IF port, and (b) RF port.

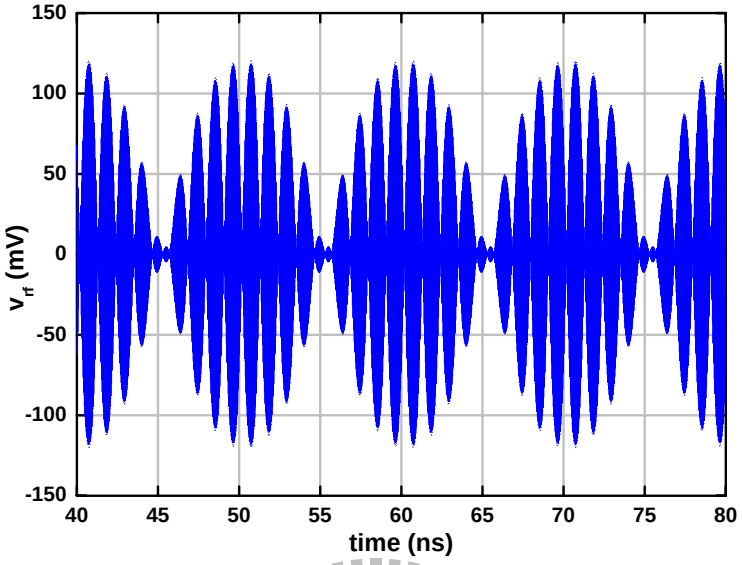


Figure 3.23 Transient simulation results of the proposed current-mode transmitter front-end.

3.4 Experimental Results

The proposed current-mode transmitter front-end circuit is fabricated in 0.13-μm 1P8M triple-well CMOS process. As shown in Fig. 3.2, it illustrates the cross-section view of the backend process. The top metal is with the material of Cu, and is with the thickness of 3.35 μm. The height of the oxide evaluated from the surface of p-type silicon substrate to the bottom of the top metal-8 is about 7.445 μm. The equivalent relative permittivity ε_{eff} is about 4.2. The 3-D EM tool Ansoft HFSS is used to evaluate and extract the on-chip octagonal transformers before the circuit designs. Furthermore, HFSS is also used to extract the parasitic effects of the layout to perform the post-simulation.

The chip microphotograph is shown in Fig. 3.24. The distance among each inductor and transformer is more than 100 μm in order to mitigate the magnetic coupling. Besides, large on-chip decoupling capacitors are placed between each bias/power supply and ground to reduce the occurrence of high-frequency noises and to obtain stable biases and supplies of the mixer. The differential signal paths are drawn as symmetric as possible to reduce the mismatches. The chip area of this current-mode transmitter front-end is

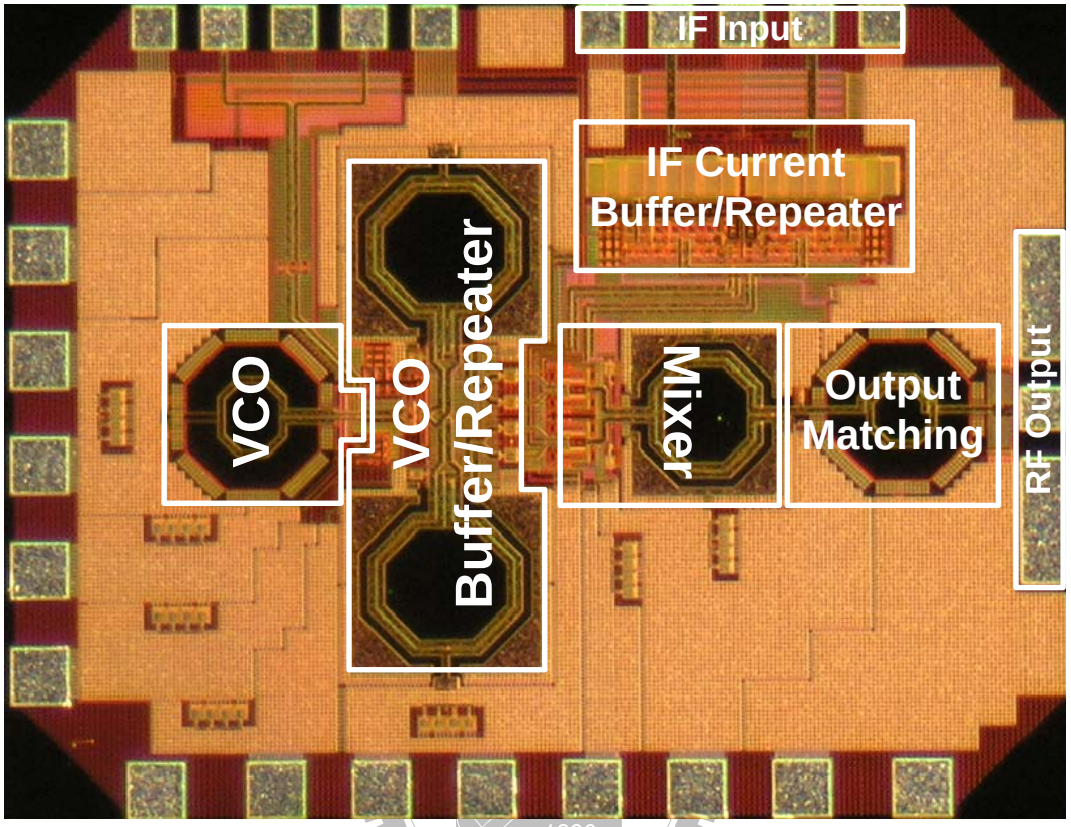


Figure 3.24 Chip microphotograph of the proposed integrated current-mode transmitter front-end.

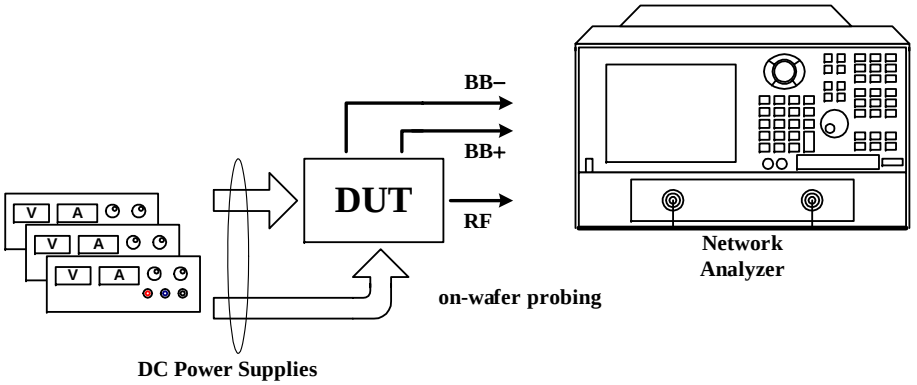
1.5×1.1 mm^2 including testing pads.

The measured environment setups of the fabricated transmitter are described as follows. On-wafer probing measurement is adopted to verify the performance of the proposed current-mode transmitter front-end. One GSG RF probe with the pitch of 100 μm, one GSGSG RF probe with the pitch of 100 μm, and two 6-pin dc probes with the pitch of 150 μm are applied to probe the testing pads. As shown in Fig. 3.25(a), the S-parameters are measured to analyze the matching characteristics of baseband input port and RF output port by the network analyzer, Agilent E8364B, which can characterize the S-parameter performance from 10 MHz to 50 GHz. To measure conversion power gain and linearity, two signal generators Agilent E8257D are used to provide two baseband signals for the DUT. The LO signals are generated by the on-chip VCO. The spectrum an-

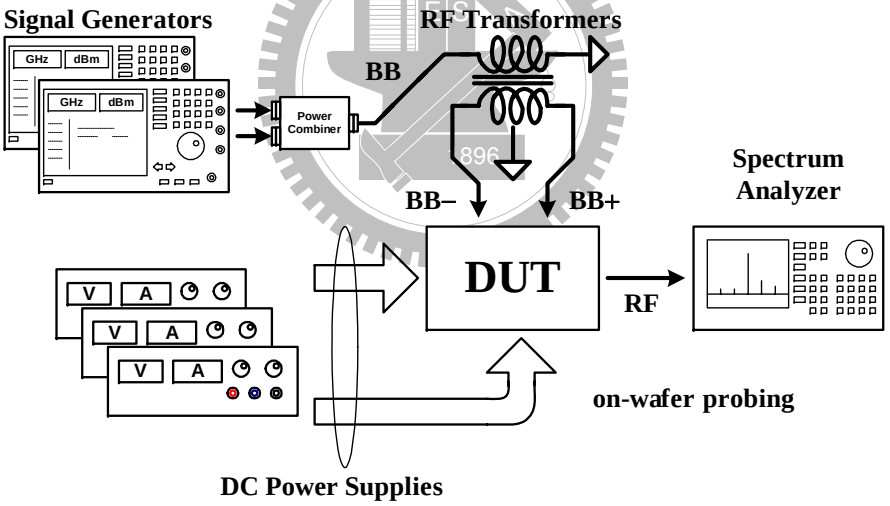
alyzer Agilent E4448A is used to monitor the spectrum to verify the linearity and conversion power gain of the proposed transmitter. The measurement environment is illustrated in Fig. 3.25(b). Furthermore, the characteristics of the on-chip VCO is also measured and analyzed through the spectrum analyzer. The noise figure of the transmitter is measured by the spectrum analyzer Agilent E4448A embedded with noise figure option. The broadband noise source of Agilent 346CK01 is used. The measurement environment is illustrated in Fig. 3.25(c).

The measured tuning curve of the integrated VCO is shown in Fig. 3.26. The on-chip VCO provides the frequency of the LO signal from 20.8 GHz to 22.7 GHz as the control voltage V_{T2} is varied from 0 V to 2 V. The measured phase noise is –108 dBc/Hz at 10-MHz frequency offset from 22.7 GHz. The measured matching characteristics of the IF input and RF output port are shown in Fig. 3.27. The return loss of the IF input port is below –20 dB within the frequency range from 170 MHz to 1.2 GHz. The return loss of the RF output port is below –10 dB within the frequency range from 21.2 GHz to 22.8 GHz. Under the 1-V supply voltage, the proposed current-mode double-balanced up-conversion mixer dissipates a very small amount of power of 3.1 mW. The VCO, transformer-based VCO buffer/repeater, and baseband current buffer/repeater circuits dissipate 2.2 mW, 3.3 mW, and 3.1 mW, respectively. The total power dissipation of the integrated current-mode transmitter front-end is only 11.7 mW.

Before verifying the linearity performance of the proposed current-mode transmitter front-end, the losses from the RF cables, probes, adaptors, 180° phase shifter, and power combiner are measured. These sources of losses in the measuring environment are compensated when analyzing the measurement data. The measured and post-simulated conversion power gains versus the IF input powers are shown in Fig. 3.28. In the measurement, the IF frequency is at 200 MHz, and the LO frequency is at 20.8 GHz where V_{T2} is equal to 0 V. The double-sideband RF outputs are observed at the frequencies of 21 GHz (upper sideband, USB) and 20.6 GHz (lower sideband, LSB). The measured conversion power gain is about –5 dB where the losses from on-chip transformer and output matching network are included. The measured input 1-dB compression point (IP_{-1dB}) and output 1-dB compression point (OP_{-1dB}) are –22 dBm and –28 dBm, respectively. Furthermore, the average single sideband (SSB) noise figure of the transmitter front-end is around 12.7

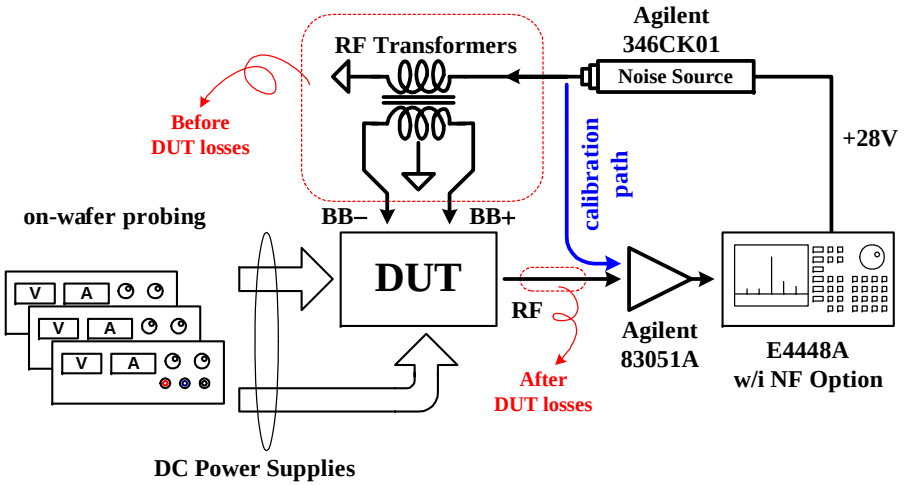


(a)



(b)

Figure 3.25 The environment setup of (a) S-parameter measurement, (b) linearity measurement, and (c) noise figure measurement.



(c)

Figure 3.25 The environment setup of (a) S-parameter measurement, (b) linearity measurement, and (c) noise figure measurement (*Con't*).

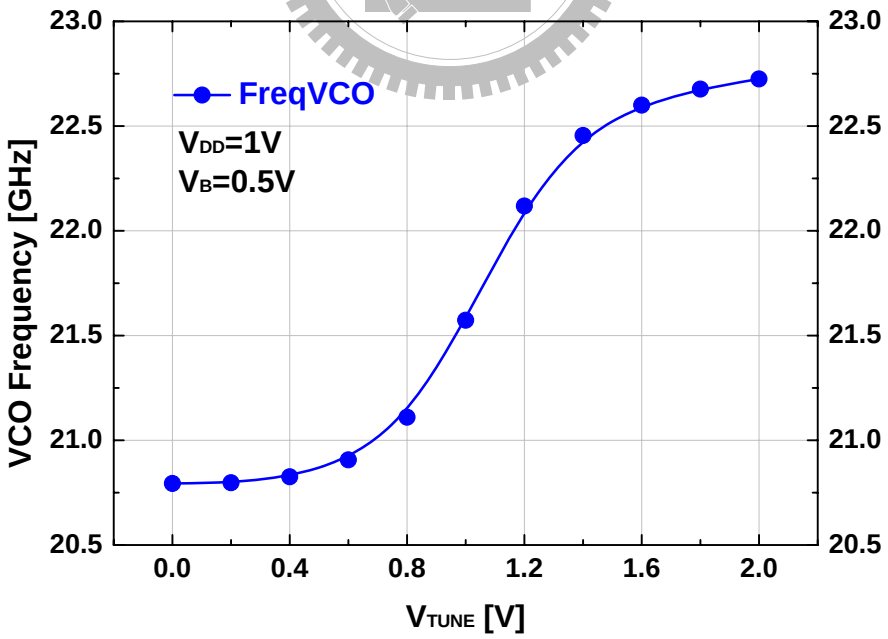
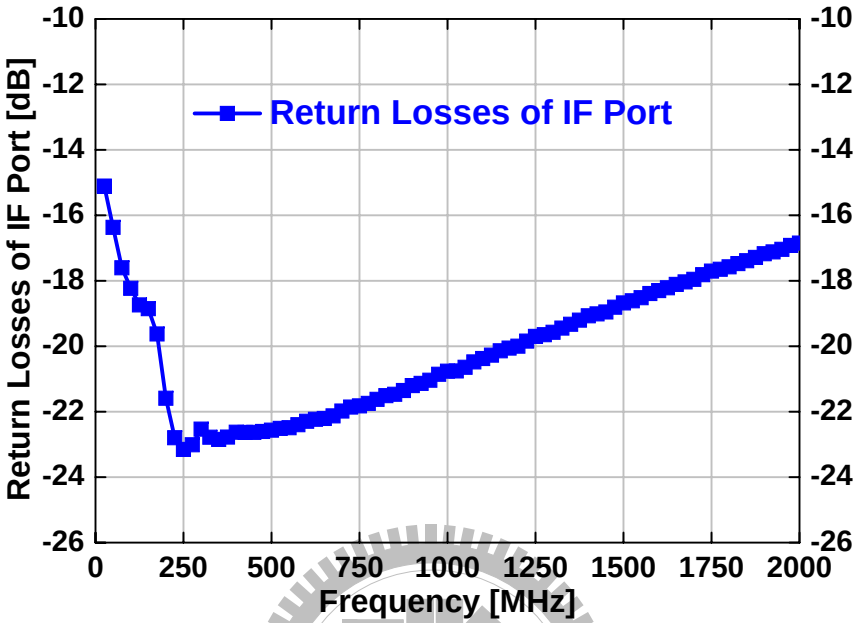
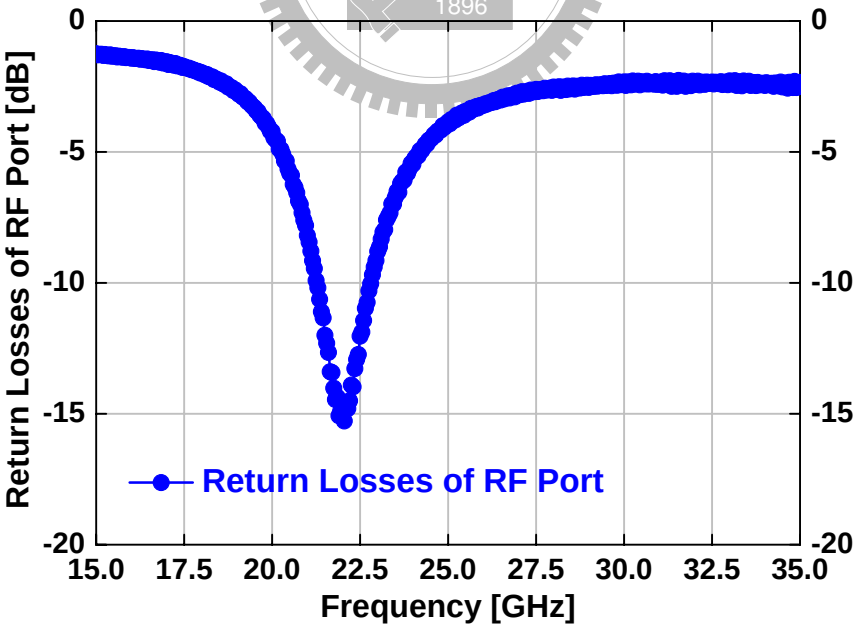


Figure 3.26 Measured tuning range of VCO.



(a)



(b)

Figure 3.27 Measured matching characteristics of (a) IF port, and (b) RF port.

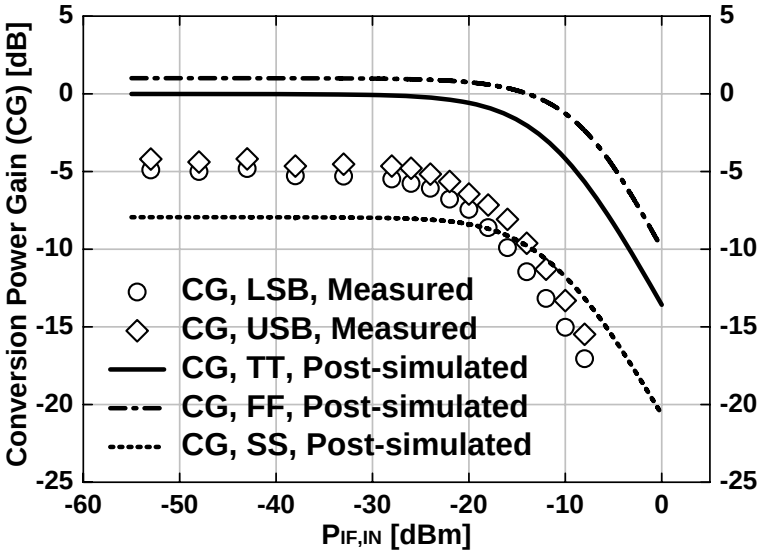


Figure 3.28 Measured and post-simulated power conversion gain versus IF input power from one-tone testing result.

dB. The LO suppression of the proposed current-mode transmitter front-end is only 16 dB.

The performance of intermodulation is measured by two-tone testing. Two IF inputs with the same signal power level are at the frequencies of 150 MHz and 250 MHz. The LO frequency is also tuned to 20.8 GHz where V_{T2} is equal to 0 V. The measured results under these conditions are represented in Fig. 3.29. It reveals that the proposed mixer has the measured input 3^{rd}-order intermodulation intercept point (P_{IIP3}) and output 3rd-order intermodulation intercept point (P_{OIP3}) of about –9.6 dBm and –14.6 dBm, respectively.

As the LO frequency is increased, the measured power conversion gain decreases because of the reduced output magnitude of the VCO at the higher frequency and therefore the reduced LO current signal. As shown in Fig. 3.30, the measured conversion gain of the mixer is degraded from –5 dB to –14 dB as the LO frequency is increased from 20.8 GHz to 22.7 GHz.

As shown in Fig. 3.28, the measured conversion power gain is –5 dB which is close to the simulated results in the process corner SS. The gain is about 5 dB smaller than the simulated results in the process corner TT. It is because the process variations make the bias

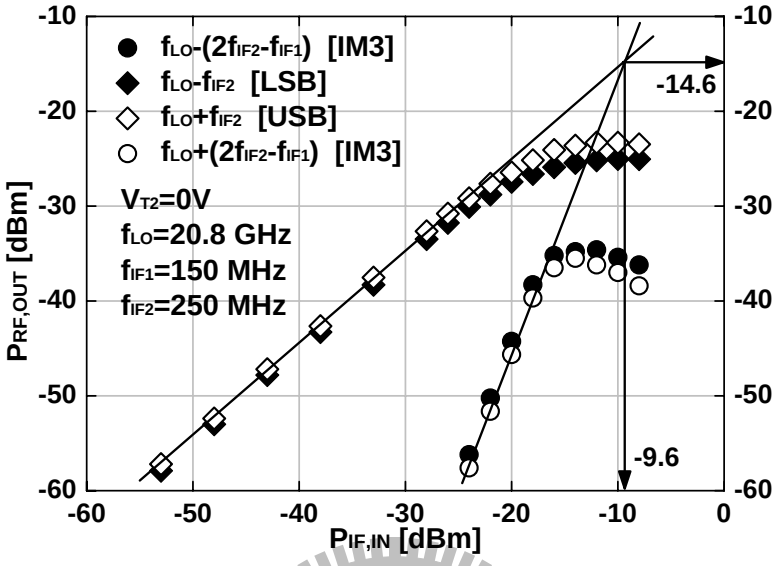


Figure 3.29 Measured 3^{rd}-order intermodulation from two-tone testing result.

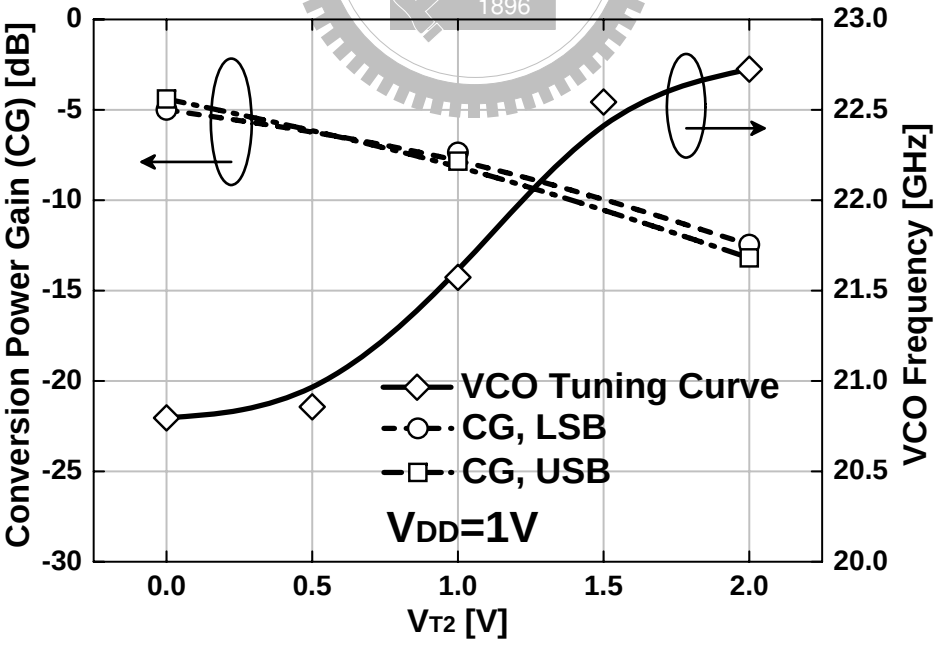


Figure 3.30 Measured conversion power gain versus LO frequency.

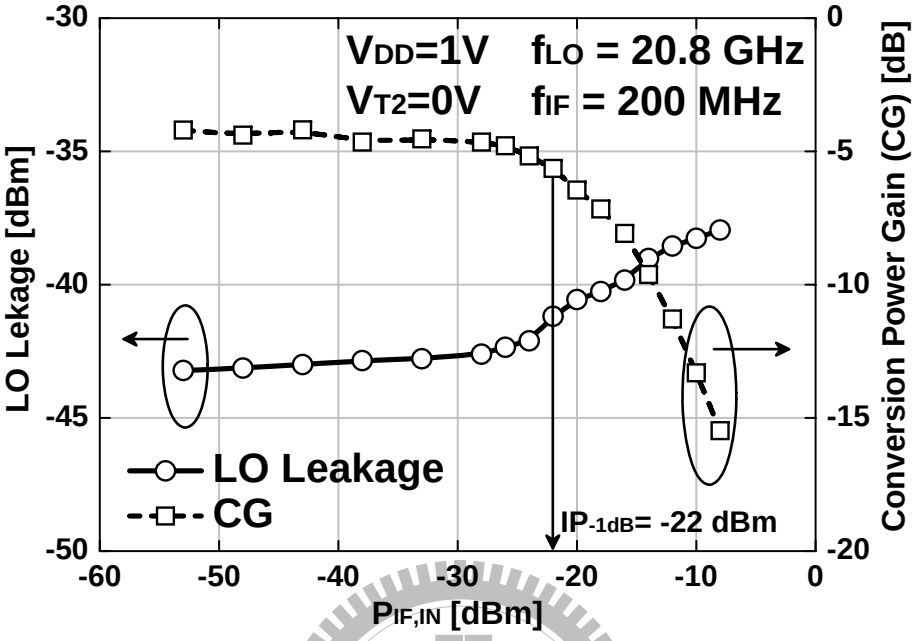


Figure 3.31 Measured LO leakage versus IF input power $P_{IF,IN}$ at the RF output port

current of the on-chip VCO smaller and therefore the g_m of M_6 and M_7 decreases. This results in a smaller equivalent negative resistance. Hence, the output magnitude of the VCO becomes smaller than the predicted one. This results in smaller LO current signals being generated through the transformer-based VCO buffer/repeater. According to the discussion in Fig. 3.13, the $CG_{intrinsic}$ is degraded when the LO input current magnitude or equivalent LO signal power decreases.

The performance of the proposed mixer is given in Table 4.4 and Table 4.5, along with comparisons with previously published CMOS up-conversion mixers [58]–[60], [133], [134], [153], [168], [169]. As can be seen from Table 4.1 and Table 4.5, the proposed CMOS current-mode up-conversion mixer has the advantage of a very low power consumption of 3.1 mW from a 1-V power supply, which is much smaller than other published CMOS up-conversion mixers [133], [134], [153]. Compared to the CMOS Gilbert mixer in [134] and the dual-gate mixer in [133], the proposed current-mode mixer can be operated in lower supply voltage. Another advantage is that the proposed mixer requires small equivalent LO signal power of –2.9 dBm to achieve simulated $CG_{intrinsic}$ of

5 dB, which is about 6 dB smaller than other CMOS voltage-mode up-conversion mixers in [133], [134]. The proposed current-mode up-conversion mixer has smaller power consumption as compared to the Gilbert-mixer in [58]–[60], which dissipates 34.5 mW where 9.5 mW for converting baseband signals to 4.8 GHz and 25 mW for converting the signals at 4.8 GHz to 24 GHz from 2.5-V supply. As compared to other Gilbert mixers operated at 20 GHz [168] and 17 GHz [169], this current-mode mixer also has much smaller power consumptions.

3.5 Summary

The current-mode design technique of CMOS RFICs has been developed and applied to the design of the first *K*-band CMOS current-mode up-conversion mixer. Furthermore, the proposed current-mode mixer is integrated with an on-chip VCO, a baseband current buffer/repeater, and a transformer-based VCO buffer/repeater to realize a current-mode transmitter front-end in the frequency of *K*-band. This current-mode transmitter has been designed and fabricated in 0.13-μm 1P8M triple-well CMOS process. From the experimental results, we observe that the proposed current-mode up-conversion mixer has a very low power consumption of 3.1 mW under the low power supply of 1 V. In addition, smaller LO signal power is required. The integrated VCO provides LO frequency from 20.8 GHz to 22.7 GHz. In addition, the total power consumption of the integrated current-mode transmitter is only 11.7 mW which is very small as compared to previously published CMOS transmitter front-end. The results achieved demonstrate that the proposed current-mode mixer offers great potential for the application in low-voltage and low-power CMOS transmitter front-ends in advanced nano-CMOS technologies.

Table 3.4
PERFORMANCE COMPARISON WITH PREVIOUSLY PUBLISHED LOW-VOLTAGE CMOS UP-CONVERSION MIXER

	This work ††	This work ††	This work ††	[153] ‡‡	[133] ‡‡	[134] ‡‡	[168] ‡‡	[58]–[60] ††
Mixer Feature	Current-mode squaring ckt.	Current-mode squaring ckt.	Current-mode squaring ckt.	Current-mode self-switching	Voltage-mode dual-gate	Voltage-mode Gilbert	Voltage-mode Gilbert	Voltage-mode Gilbert
Technology	0.13-μm 1P8M CMOS	0.13-μm 1P8M CMOS	0.13-μm 1P8M CMOS	0.25-μm CMOS	0.13-μm CMOS	0.13-μm CMOS	0.13-μm CMOS	0.13-μm CMOS in BiCMOS
Supply [V]	0.9	1	1.1	1	1.2	1.2	1.2	2.5
Power [mW]	1.54	3.1	6.4	49	8	11.1	–	9.5 + 25
$Freq_{RF}$ [GHz]	20.9∼23	20.8∼22.7	20.7∼22.5	2	18∼28	20∼26	20	24
$Freq_{LO}$ [GHz]	20.9∼23 †	20.8∼22.7 †	20.7∼22.5 †	2.38	14∼26	27.3∼23.3	–	19.2, 4.8
$Freq_{IF}$ [GHz]	0.2	0.2	0.2	0.38	2.3	2.7	–	–
Gain [dB]	–8∼–15	–5∼–14	–9∼–17	6.7	–2∼–0.7	2	1	–
IP_{-1dB} [dBm]	–23	–22	–20.5	–	–	–14.8	–12	–
OP_{-1dB} [dBm]	–32	–28	–32	–	–7∼–5.2	–	–	–
P_{IIP3} [dBm]	–11	–9.6	–8	–	–	–	–	–
P_{OIP3} [dBm]	–21	–14.6	–19	6.5	3∼5.8	–	–	–
Area [mm^2]	1.65 ‡	1.65 ‡	1.65 ‡	2.25	0.47	1.85	8.2	–
$P_{LO,IN}$ [dBm]	–7∼–15	–4∼–12	–2∼–9	–15	3	5	–	–

† The measured tuning frequency of the **integrated on-chip** VCO.
‡ This denotes whole chip area. The area of mixer itself is 0.18 mm^2.
†† LO is provided by on-chip VCO.
‡‡ LO is provided by off-chip signal generator.

Table 3.5
PERFORMANCE COMPARISON WITH PREVIOUSLY PUBLISHED CMOS TRANSMITTER FRONT-END OPERATED AROUND 20 GHZ

	This work	[58]–[60]	[169]
Technology	0.13-μm 1P8M CMOS	0.18-μm CMOS in BiCMOS	0.13-μm CMOS
Supply [V]	1	2.5	1.5
$Freq_{RF}$ [GHz]	20.8∼22.7	24	16.6∼19.6
$Freq_{LO}$ [GHz]	20.8∼22.7 †	–	–
$Freq_{IF}$ [GHz]	0.2	–	–
Gain [dB]	–5∼–14	–	4 ‡‡
IP_{-1dB} [dBm]	–22	–	–
OP_{-1dB} [dBm]	–28	–	4.2 ‡‡
P_{IIP3} [dBm]	–9.6	–	–
P_{OIP3} [dBm]	–14.6	–	13 ‡‡
Total power [mW]	11.7	34.5 ‡	93
Area [mm^2]	1.65 ††	–	0.5 ‡‡
Mixer configuration	Current-mode	Gilbert	Gilbert

† The measured tuning frequency of the **integrated on-chip** VCO.
†† This denotes whole chip area. The area of mixer itself is 0.18 mm^2.
‡ Two-step up-conversion configuration.
‡‡ Output buffer is included.

Chapter 4

45-nm CMOS K–Band LNA With High-Q Above-IC Inductors

The LNA is a key building block of the receiver front-end. The aim of this chapter is to introduce the design of K-band CMOS LNAs. Two LNAs which are one-stage cascode and two-stage cascaded cascode configurations are designed and implemented by IMEC 45-nm 1P5M planar bulk-CMOS technology with high-Q above-IC inductors. The high-Q above-IC inductors are implemented through the IMEC Wafer-Level Packaging (WLP) technology, which consists of a 5-μm thick electroplated copper layer on an 18-μm low-k dielectric of Benzo-Cyclo-Buthene (BCB), is post-processed on top of the IMEC's 45-nm 1P5M bulk-CMOS process. In additions, the transmission-line inductor is also realized in WLP technology. The presented one-stage cascode LNA has been published in [170], [171].

In the design LNA, the cascode topology is chosen because of its better isolation, improved bandwidth, and higher gain than common gate or common source topology. The source degenerative inductor is also used to provide the real part of the input impedance for the input matching. By using the cascode topology with source degenerative inductor, the LNA can be simultaneously noise- and input-impedance matched. The output of the LNA is loaded with an inductive load to provide parallel resonance with the output parasitic capacitance and increase the gain at the design frequency. With the mentioned advantage of cascode topology, there are two LNAs are realized where they are a one-

stage cascode LNA and a two-stage cascaded cascode LNA.

The measurement results of the implemented one-stage cascode LNA show that the one-stage LNA has a NF of 4 dB, a gain of 7.1 dB, an IP_{-1dB} of –9.5 dBm, and a P_{IIP3} of +2.25 dBm. The center frequency of this LNA is about 23 GHz. The LNA consumes 3.6 mW from 1-V power supply voltage. The Shallow Trench Isolation (STI) P+/N-well and N+/P-well diodes are implemented between supply/bias and ground for the ESD protection. With these power-clamp ESD diodes, the LNA has an ESD protection level of 3-kV Human-Body Mode (HBM). This one-stage cascode LNA occupies the active area of 0.72×1.12 mm^2. This work has been published in [170].

In addition, the measurement results of the implemented two-stage cascaded cascode LNA show that the two-stage LNA has a NF of 4.4 dB, a gain of 11.6 dB, an IP_{-1dB} of –16 dBm, and a P_{IIP3} of –4.2 dBm. The center frequency of the two-stage LNA is about 23.4 GHz. The LNA dissipates 9.3 mW from 1-V power supply voltage. The STI P+/N-well and N+/P-well diodes are implemented between supply/bias and ground for the ESD protection. With the power-clamp ESD diode, the LNA also has an ESD protection level of 3-kV HBM. This two-stage cascaded cascode LNA occupies the active area of 1.28×1.12 mm^2. This work has been published in [171].

Compared to other K-band CMOS LNAs, the measurement results show that the implemented one-stage cascode LNA in 45-nm bulk-CMOS with high-Q above-IC inductors has the highest Figure-of-Merit (FOM). The gain of two-stage cascaded cascode LNA is smaller than predicted. It may be because that the process variations or inaccurate parasitic modeling of the active devices make the two parallel LC network of two-stage LNA resonate at different frequency. The total gain therefore becomes smaller. Although the gain of the two-stage LNA is not large enough, the FOM still shows that this LNA have comparable performance to other CMOS K-band LNAs. It is also demonstrated that the 45-nm planar bulk-CMOS technology has great potential for the design of high performance RF circuits. Furthermore, high-Q passive inductors from above-IC technology can provide great benefit to the RF circuit designs.

This chapter is organized as follows. In Section 4.1, the technology of IMEC is introduced, including 45-nm CMOS process and wafer-level packing technology. The characteristics of planar device and FinFET devices are discussed in this section. The advan-

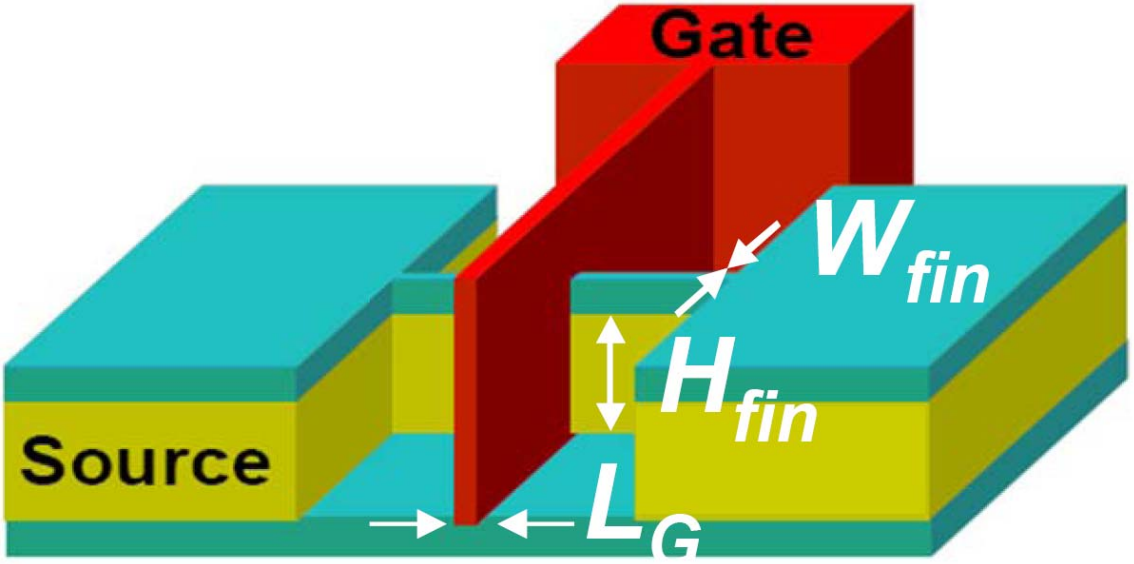
tage of the above-IC spiral inductors and transmission-line inductors fabricated through wafer-level packing technology is illustrated. In Section 4.2, the circuit designs of LNAs are described. Simulation results are also given within this section. In Section 4.3, the layout consideration and experimental results are presented and analyzed to verify the performance of the proposed 45-nm bulk-CMOS LNA with high-Q above-IC inductors. Finally, the summary is given in Section 4.4.

4.1 45-nm CMOS Technology and Wafer-Level Packaging (WLP)

4.1.1 45-nm CMOS Technology [175]–[182]

Multi-Gate Field Effect Transistor (MuGFET), also known as FinFET or gate wrap-around FET, is emerging as a strong candidate [172]–[174] for nano-CMOS technologies. Shown in Fig. 4.1 [175] is the 3-D drawing of the FinFET device with its important geometrical parameters. In a FinFET, the gate wraps around a thin slice of (preferably un-doped) silicon, also known as a "fin", and current flows along the top and side surfaces of the fin. In Fig. 4.1, L_G is the gate length, H_{fin} is the fin height, and W_{fin} is the fin width. The wrap-around nature of the gate enhances the gate control over the channel, thus reducing the short-channel effects and leakage currents [176].

For the IMEC 45-nm planar bulk-CMOS device, as shown in Fig. 4.2 [177], Si wafers with 20 $\Omega\cdot$ cm p-type are used. The shallow trench isolation is used followed by low dose, high energy deep Well implants to electrically isolate the devices from each other. A high-k gate dielectric SiON layer is deposited on top of an interfacial oxide as gate dielectric. The equivalent gate oxide thickness of 1.4 nm is used. The metal gate with a thin metal layer of 5-10 nm is deposited for work-function engineering, and covered by a 100-nm Poly-Si layer on top. For the present experiments, the gates are defined using 193-nm DUV lithography combined with resist and hard-mask trimming. After gate-etch, halos are implanted to locally increase the channel doping near the extension region to suppress short-channel effects, after which Shallow Extensions (SE) are down. To position the deep source and drain implants (HDDs), spacers are first formed next to



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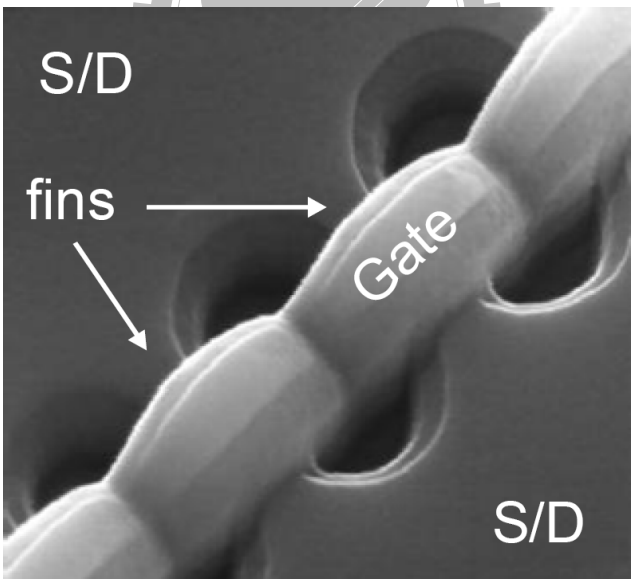

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Figure 4.1 The 3-D drawing of the FinFET device and the SEM picture of FinFET device [175].

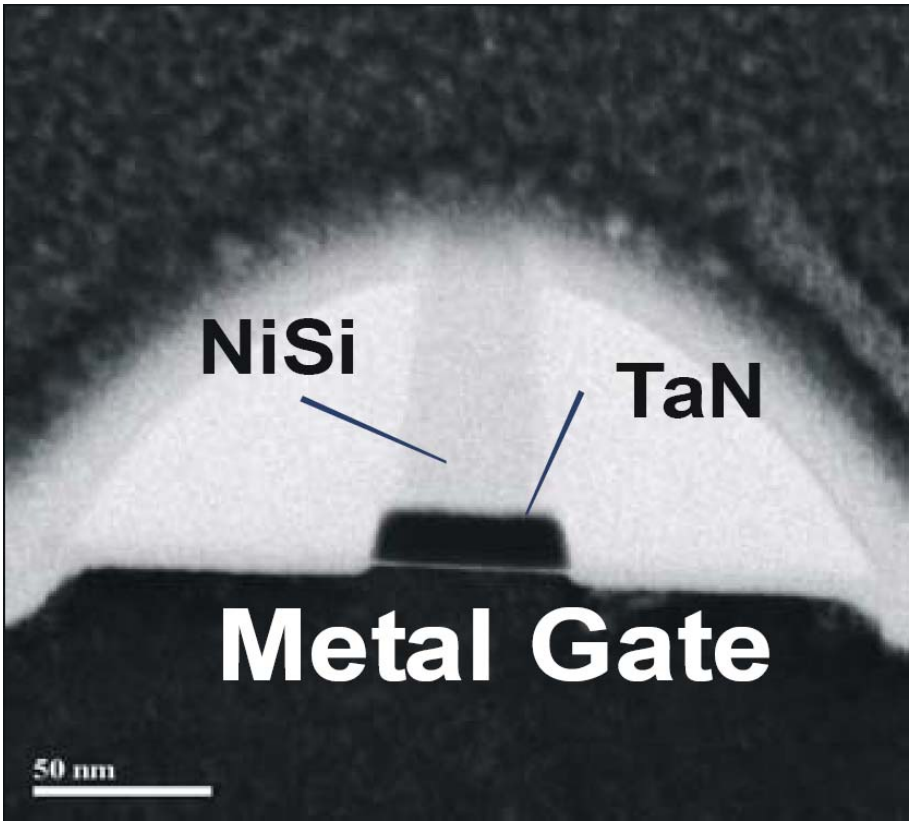
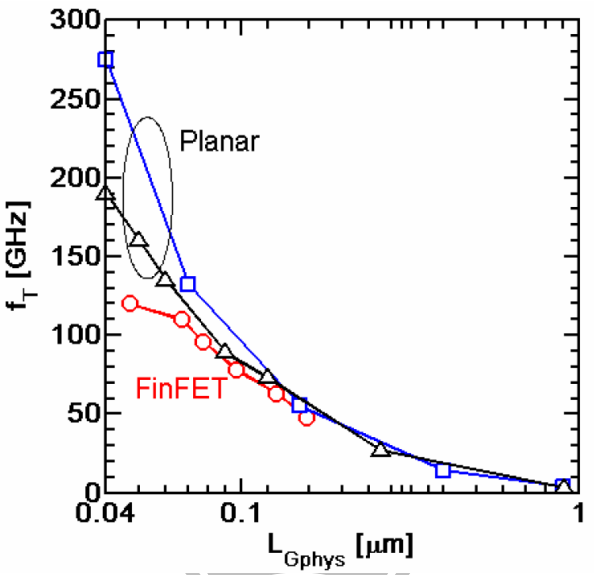


Figure 4.2 The SEM picture of the device. Cross-section view of planar bulk metal-gate transistor [177].

the gate, at low temperature to avoid any diffusion of the SE and halo implants. A single spike annealing activates the dopants and removes implantation damage. To lower contact and sheet resistance, source and drain active areas and the poly area are silicided (NiSi). For metal-1, single damascene Cu back-end is used with tungsten plugs. For the higher metal layers, double damascene Cu back-end with oxide dielectric is used [175], [177].

With the scaling of gate length of CMOS devices, the peak f_T and f_{MAX} should be strongly improved. However, due to the velocity saturation, the observed increase might not be as strong as the first-order extrapolations indicate. On top of that, for FinFET technology, series resistance of the fins and the lower mobility along the sidewalls imposes a serious limitation at present. Technologies as selective epitaxial growth on top of the source and drain regions to reduce the series resistance, are proposed to only partially relieve the problem. A typical example is given in Fig. 4.3 [175], [177], comparing f_T of planar bulk NMOS versus FinFETs for different technology nodes. Today, the peak RF performance of FinFET is inferior to planar bulk CMOS, even for technologies nodes with larger nominal gate lengths.

For future system-on-chip (SOC) solutions in the advanced deca-nanometer technologies, not only digital but also analog and RF building blocks with low power consumption is mandatory. Several previous work has analyzed the performance of these devices, reporting that FinFETs are attractive for low-power, low-frequency analog and RF applications [178]–[186]. For high gate overdrives and high-frequency analog and RF applications, the planar devices still outperform the FinFETs. It is because FinFETs suffer from a high series resistance, which degrades the drive current and transconductance. The impact of the series resistance is amplified at high gate overdrive voltages. As a result, for high-frequency applications, planar bulk devices are seen to hold the advantage over FinFETs due to their lower series resistance and high peak transconductance. For the conventional planar bulk MOSFET, the analog performances does benefit from improvements in transconductance as a result of scaling. However, this is accompanied by a degraded output conductance and voltage gain. FinFETs, on the other hand, have been shown to have potential for analog applications. Although 45-nm FinFETs are attractive for low-power low-frequency analog and RF applications, the 45-nm planar technology still outperforms the FinFET one for high gate overdrives and high-frequency applications



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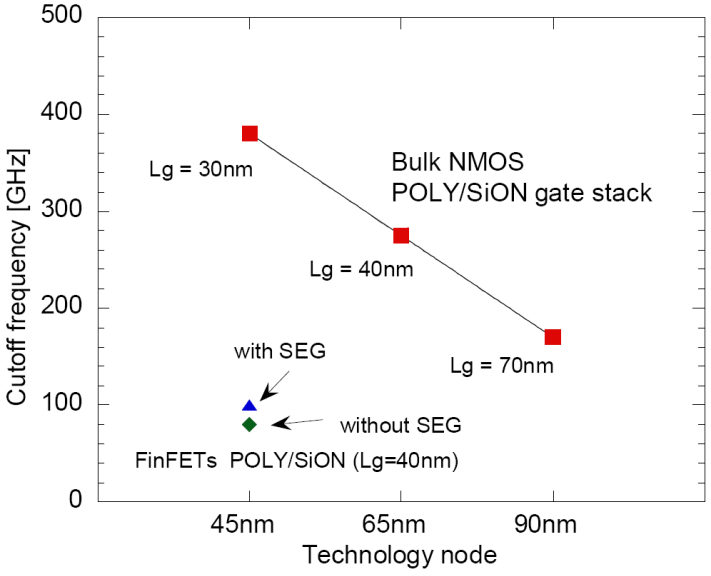


(b)

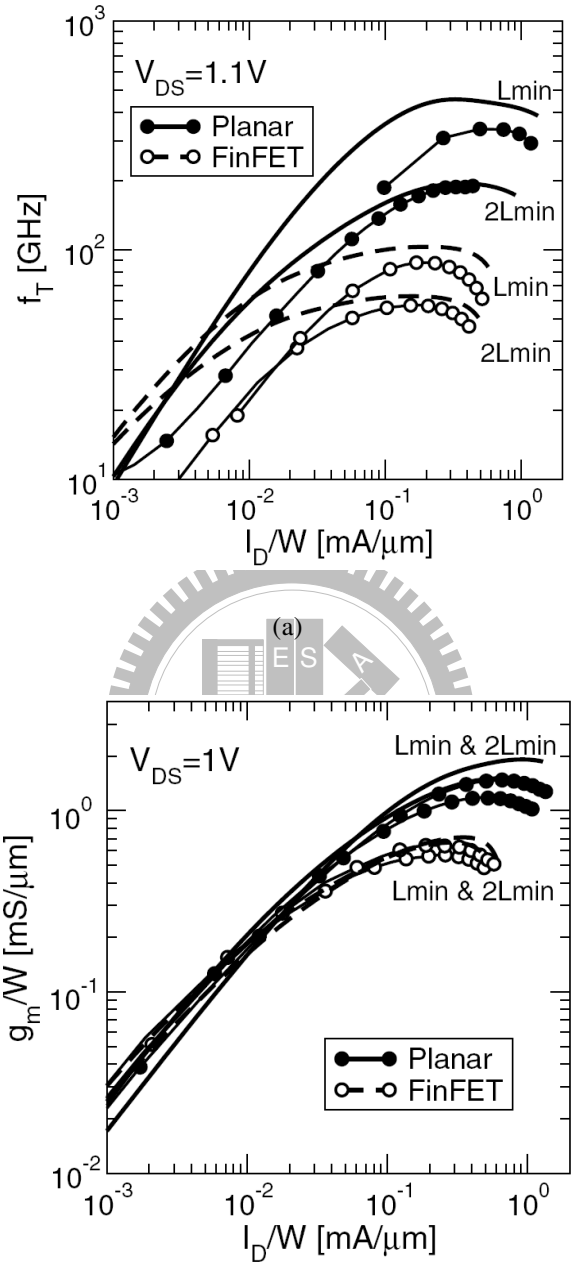
Figure 4.3 Cut-off frequencies f_T for different gate lengths, comparing bulk CMOS with FinFETs. (a) [175] and (b) [177].

by requiring lower power consumption with comparable performance. This is due to the superior f_T of the planar device in the inversion region. Although analog performance of FinFETs probably benefit from scaling, high-frequency RF design in FinFETs still has its challenges. On the other hand, the FinFET technology benefits from lower parasitics in the passive elements because of the SOI substrate.

The compact models of 45-nm FinFETs were obtained by an appropriate scaling of a 65-nm technology. In particular, the 45-nm planar bulk-CMOS device is modeled by the PSP model, while the FinFET device is modeled by the Philips MM11 model and a "black-box" approach is used. In both cases, the RF behavior is reproduced by the adoption of extrinsic elements. Self-heating and threshold voltage hysteresis are not accounted for.

Since g_m and f_T are the key parameters of the LNA. The simulated curves of f_T and g_m/W versus I_D/W for both planar devices and FinFET devices are shown in Fig. 4.4 [182]. The g_m/W values are very similar for the two devices in sub-threshold or weak inversion region, featuring a different peak value in the strong inversion region; on the other hand, substantial differences appear in the f_T. The simulated f_T of FinFET device is comparable or higher than for planar device at low I_D/W value (i.e. sub-threshold region), while at high I_D/W (i.e. strong inversion) the peak f_T of the planar device is much higher with respect to the FinFET one, reaching values close to 350 GHz [178],[179],[182]. The preliminary measurements performed by IMEC on the technologies based on similar processes and featuring similar gate lengths essentially confirm the behavior predicted by the compact models by the PSP model for planar devices and the MM11 model for FinFET devices.

From the aforementioned, planar devices are more suitable for designing high-frequency RF building blocks. The high-frequency RF performance of 45-nm planar bulk-CMOS transistors is evaluated by a one-stage cascode LNA and a two-stage cascaded cascode LNA designed at the operating frequency of 24 GHz. The circuit designs will be discussed in the following section. The passive spiral inductors and microstrip-line inductors have been designed with a process option of IMEC Wafer-Level Packing (WLP) technology, which will be introduced in the following section.



(b)

Figure 4.4 Results of the compact model for planar and FinFET 45-nm CMOS devices (lines) compared with preliminary experimental data for similar processes (symbols). (a) The cutoff frequency f_T versus current density I_D/W for different channel lengths, and (b) the g_m/W versus I_D/W [182].

4.1.2 Wafer-Level Packaging (WLP) Technology [116]–[119]

High-Q integrated inductors are important components for modern RFICs. Nevertheless, on-chip RF inductors have fairly low-Q factors due to the relatively thin-metal layers and the close proximity to the lossy silicon substrate. The performance of the inductor can be improved by using low-k materials and thick Cu metallization. However, thick Cu is usually not a standard backend-of-line (BEOL) process, and the dielectric in between inductor and lossy silicon substrate is still relatively thin. Alternative reported options such as micromachining techniques to remove the lossy substrate underneath the spiral inductor in a post-processed step, or to create an air gap in between spiral inductor and substrate using suspended on-chip MEMS inductors [115] are mechanically less stable and are not preferred for subsequent packaging process.

In the past, IMEC provides a more attractive and cost-effective solution to realize the above-IC inductors using thin-film wafer-level packaging (WLP) techniques [116]–[119]. The inductors are realized above the passivation by using thin-film post-processing techniques. Thin-film technology offers the advantage of high precision, low temperature, and low cost. When applied above IC, thin-film WLP technology offers novel opportunities to the functionality of ICs, besides the redistribution of bonding pads, as the added metallization may be used for the integration of high-Q on-chip inductors and low-loss interconnects. Furthermore, IMEC has demonstrated that a measured Q-factor above 40 at 4.7 GHz for a 1.8 nH inductor with a resonance frequency of 28 GHz. The ultra low-loss transmission lines with insertion loss lower than 0.3 dB/mm at 100 GHz has also been proposed in the thin-film WLP technology.

The WLP technology is performed on top of IMEC's 45-nm RF CMOS process where a p-type 20-$\Omega\cdot$ cm Si substrate with a five levels of metal Cu/oxide BEOL is used. The BEOL Cu layer (Metal-1 to Metal-5, with Metal-5 being the top metal layer) has a thickness of 625 nm, and an inter-metal level dielectric of 475 nm. Thereby, a space between the passivation and the substrate is about 6.1 μm. The high-Q above-IC inductors and microstrip lines by WLP technology, which consists of a 5-μm thick electroplated Cu layer of WLP-M1 on an 18-μm low-k dielectric (k = 2.65) of Benzo-Cyclo-Buthene (BCB), are realized and post-processed above the BEOL passivation. Overpasses are realized in

WLP-M2 (2-μm Cu, 3-μm Ni/Au) and separated from WLP-M1 by 8-μm thick BCB-2. Fig. 4.5(a) [118] illustrates the schematic cross-section view of the "inductor above passivation" concept. Fig. 4.5(b) [118] illustrates the SEM cross-section view of the stack of WLP-M1 and WLP-M2 on top of Metal-1–Metal-5, with high aspect ratio HARVi and conventional via. Processing masks for the WLP are very cheap compared to masks used for metal layers in the standard BEOL interconnect structure. The thick BCB layers lower the parasitic capacitance to the silicon substrate, hereby increasing the inductor resonance frequency. In addition, thick Cu yields low series resistance.

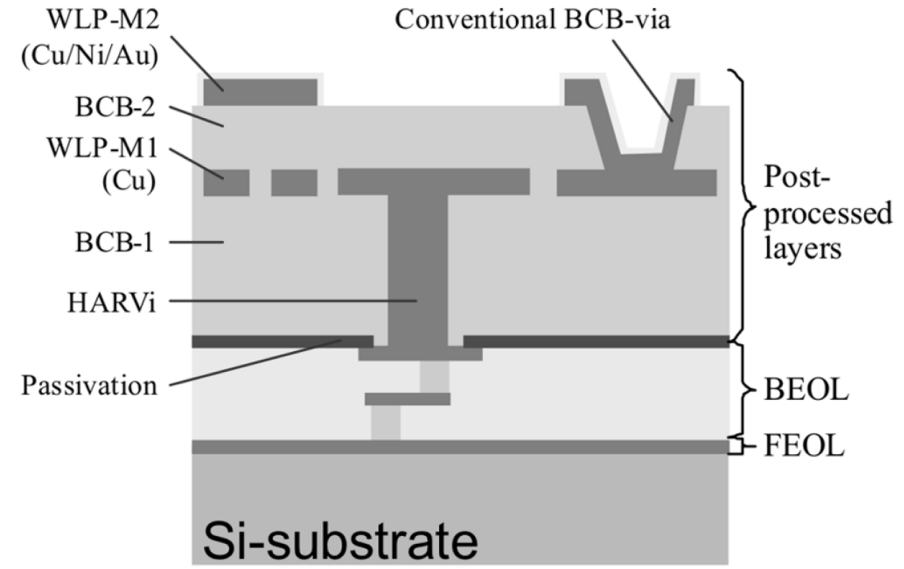
Fig. 4.6 [118] shows a 1.8-nH post-processed symmetrical inductor with and without patterned poly-silicon ground shield. Fig. 4.7 [118] shows the de-embedded measurement and simulation results of a 1.8-nH thin-film post-processed inductor without patterned poly-silicon ground shield, as well as the factor for single-ended (SE) and differential (DIFF) application. A 1.8-nH symmetrical inductor (without ground shield) has a differential Q-factor of 40 at 5 GHz and a single-ended Q-factor of 32 at 3 GHz. When a front-end-of-line (FEOL) is present, a patterned poly-silicon ground shield will terminate the inductor's electric field before reaching the silicon substrate, hereby reducing the substrate losses, such that the Q-factor increase. As shown in Fig. 4.8 [118], Q-factors of the 1.8-nH symmetrical inductor with and without patterned poly-silicon ground shield are compared. With the shield, the differential Q-factor can reach 47 around 9 GHz with a resonance frequency of 25 GHz. Also, it is above 30 from 2.8 GHz to 18 GHz, which guarantees a good performance in a wide frequency range. The differential quality factor Q_{DIFF} and single-ended quality factor Q_{SE} are defined as [187]

$$Q_{DIFF} \equiv \frac{\Im\{Z_{11} - Z_{12} - Z_{21} + Z_{22}\}}{\Re\{Z_{11} - Z_{12} - Z_{21} + Z_{22}\}} \tag{4.1}$$

$$Q_{SE} \equiv \frac{-\Im\{Y_{11}\}}{\Re\{Y_{11}\}} \tag{4.2}$$

where Z_{11}, Z_{12}, Z_{21} and Z_{22} are the Z-parameters of the two-port network of inductor, and Y_{11}, Y_{12}, Y_{21} and Y_{22} are the Y-parameters of the two-port network of inductor.

The characteristic impedance of the transmission line in WLP process has been extracted through HFSS simulation. The design parameters have been shown in Table 5.1. Moreover, the parameters of the equivalent RLGC model of the designed transmission line in WLP process have been shown in Table 5.2.



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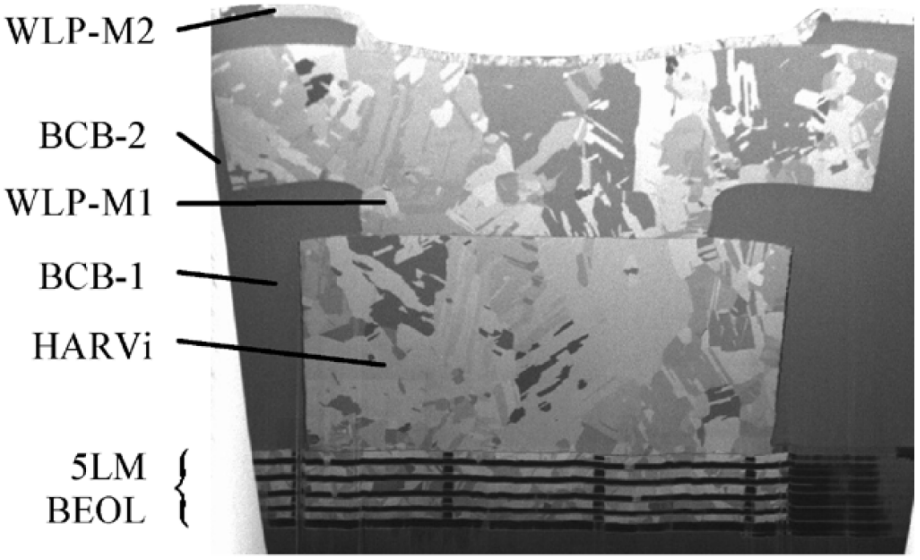


(b)

Figure 4.5 The IMEC WLP technology. (a) Schematic cross section of the äbove ICl̈ayers. (b) SEM cross section of WLP-M1 and WLP-M2 on top of M1-M5 metal levels: conventional via (through BCB-2) and high aspect ratio via (HARVi) through BCB-1 [118].

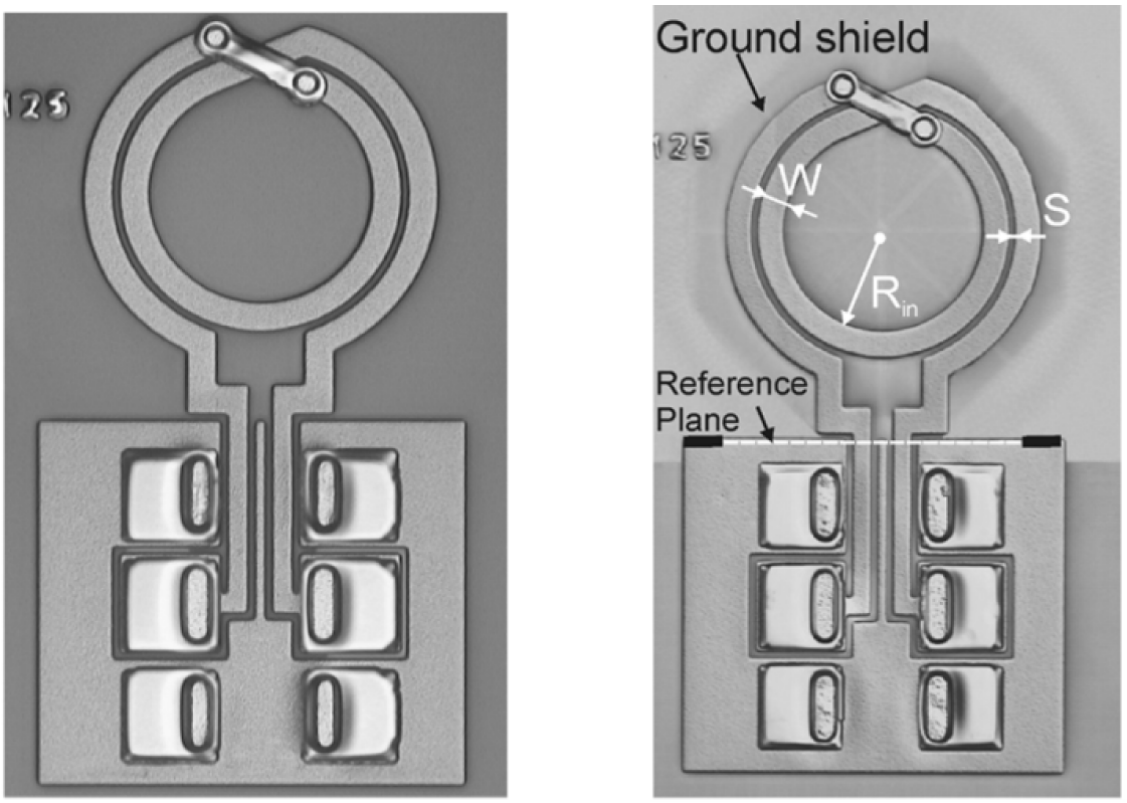


Figure 4.6 Microphotograph of a 1.8-nH thin-film post-processed symmetrical inductor, including the pad connections for wafer probing. The left inductor is without patterned poly-silicon ground shield, and the right inductor is with patterned poly-silicon ground shield. The inductor has two turns (N), an inner radius of 125 μm (R_{in}), 10-μm metal spacing (S), and a metal trace width (W) of 30 μm [118].

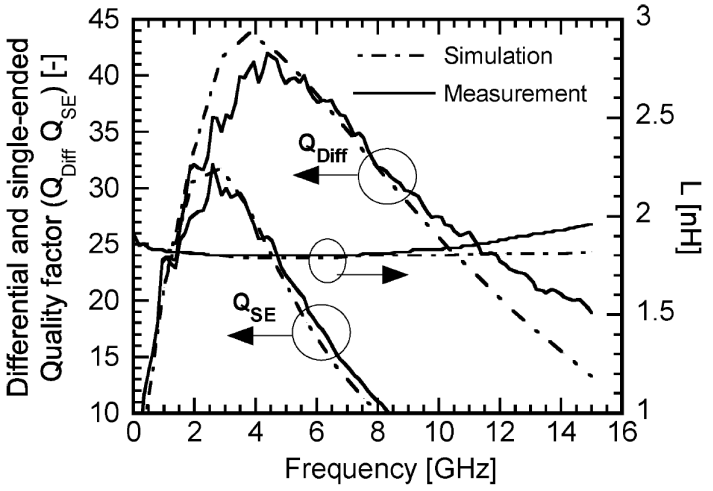


Figure 4.7 Measurement (solid line) and simulation result (dashed line) of the series inductance and the Q factor of thin-film post-processed inductor with a designed inductance of 1.8 nH, both for single-ended (Q_{SE}) and differential (Q_{DIFF}) applications. The inductor has no patterned poly-silicon ground shield: $N = 24$, $S = 10\mu m$, $W = 30\mu m$, and $R_{in} = 125\mu m$ [118].

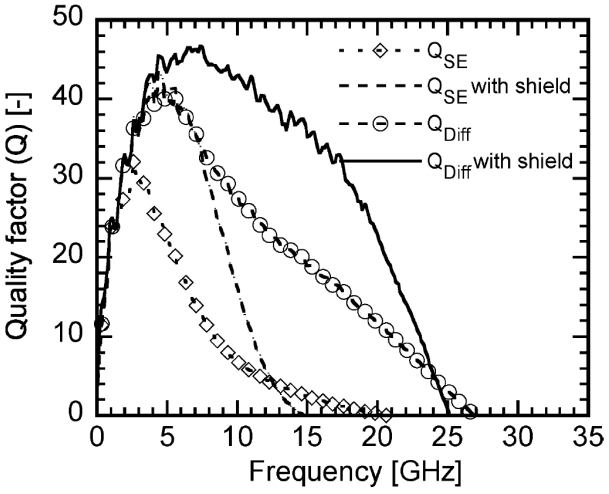


Figure 4.8 The measured quality factor of single-ended Q_{SE} and differential Q_{DIFF} applications of two-turn symmetrical thin-film post-processed 1.8-nH inductors with and without a patterned poly-silicon ground shield: $N = 2$, $S = 10\mu m$, $W = 30\mu m$, and $R_{in} = 125\mu m$ [118].

Table 4.1
CHARACTERISTIC IMPEDANCE OF THE TRANSMISSION LINE EXTRACTED FROM HFSS

			Z_C (Ω)		
TL layer	Shielding layer	TL width (μm)	10 GHz	24 GHz	60 GHz
WLP-M1	M1-to-M5	35	51.5	51.2	51
	M1-to-M2	10	89.9	89.3	88.9
		20	72.4	71.9	71.7
		35	56.2	55.8	55.7
		40	52.6	52.3	52.2
		41	52	51.8	51.6
		43	50.6	50.3	50.2
		45	49.2	48.9	48.8
		60	41.6	41.4	41.4
		80	34.5	34.4	34.3
M5	M1-to-M2	5	50.4	48.4	47.1
		10	33.2	32	31.1
		20	20.4	19.6	19

4.2 Circuit Designs

The CMOS technology is especially attractive for its potential of integration of RF, IF and baseband DSP functions, enabling true systems-on-chip. As CMOS technology is scaled into deca-nanometer range, the transistor $I_D - V_{GS}$ characteristics in the saturation region become linear while the transconductance, minimum noise figure (NF_{MIN}), f_T, and f_{MAX} improve. Additionally, when biased the MOS transistor at the current densities between 0.15 mA/μm and 0.4 mA/μm, these figures of merits become almost insensitive to the variations of I_D and V_{GS}. The application of constant-field scaling rules to every new generation of CMOS since the 0.5-μm node has resulted in constant peak f_T and f_{MAX} current densities of 0.3 – 0.35 mA/μm and 0.2 mA/μm, respectively [187]–[193]. This is in contrast to SiGe HBTs where the peak f_T and f_{MAX} current bias is technology dependent. The peak f_T current density remains constant for different finger widths and for both the common source and cascode configurations. The minimum noise figure bias of MOSFET is $J_{OPT} = 0.15mA/\mu m$, irrespective of frequency and technology nodes.

Table 4.2
EQUIVALENT RLGC MODEL PARAMETERS FROM HFSS

TL layer	Shielding layer	TL width	$\Re\{Z_C\}$	$\Im\{Z_C\}$	$\Re\{\Gamma\}$	$\Im\{\Gamma\}$	R	L	G	C
–	–	[μm]	[Ω]	[Ω]	[Np/m]	[Rad/m]	[Ω/m]	(H/m)	(S/m)	(F/m)
WLP-M1	M1-to-M5	35	51.1	–0.63	10.35	774.5	1014.6	2.6×10^{-7}	0.017	10.0×10^{-11}
	M1-to-M2	10	89.3	–1.19	11.05	778.9	1910	4.6×10^{-7}	0.008	5.6×10^{-11}
		20	71.9	–0.83	9.79	780.9	1350.2	3.7×10^{-7}	0.011	7.2×10^{-11}
		35	55.9	–0.60	9.21	782.8	985.2	2.9×10^{-7}	0.014	9.3×10^{-11}
		40	52.3	–0.54	9.05	785.2	900.5	2.7×10^{-7}	0.017	10.0×10^{-11}
		41	51.7	–0.56	9.25	785.6	918.3	2.7×10^{-7}	0.014	10.1×10^{-11}
		43	50.3	–0.53	9.05	785.9	868.1	2.6×10^{-7}	0.017	10.4×10^{-11}
		45	48.9	–0.52	9.10	786.4	854.8	2.6×10^{-7}	0.015	10.7×10^{-11}
		60	41.3	–0.42	8.91	789.5	700.7	2.2×10^{-7}	0.021	12.7×10^{-11}
		80	34.3	–0.34	8.82	793.1	571.7	1.8×10^{-7}	0.029	15.3×10^{-11}
M5	M1-to-M2	5	48.4	–3.13	66.16	1035.3	6439.2	3.3×10^{-7}	–0.018	14.2×10^{-11}
		10	32.1	–2.02	64.84	1041	4186.6	2.2×10^{-7}	–0.027	21.5×10^{-11}
		20	19.6	–1.29	67.25	1051.3	2671	1.4×10^{-7}	–0.084	35.5×10^{-11}

This current density is very close to the peak f_{MAX} current density of 0.2 mA/μm and there is practically no degradation of power gain when MOSFET is biased for optimum noise.

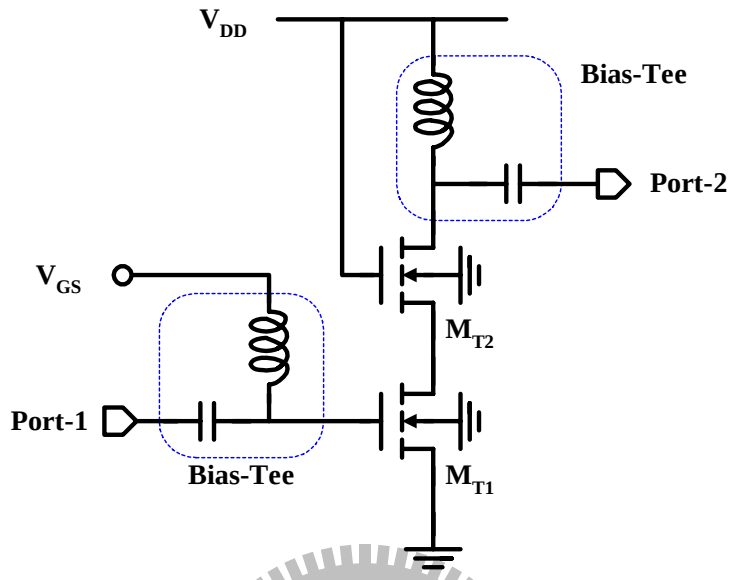
In this IMEC 45-nm planar bulk-CMOS technology, the transistor has been demonstrated that f_T is around 300 GHz with the achievable transconductance efficiency g_m/I_D of $2.5V^{-1}$. In the back-end process, this 45-nm bulk-CMOS technology offers five layers of metal in the damascene process and metal-insulator-metal (MIM) capacitor.

4.2.1 One-stage cascode LNA

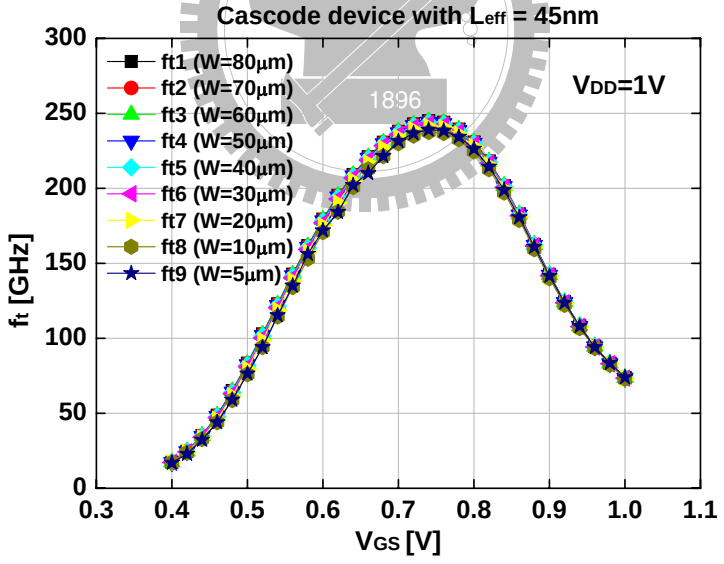
The configuration of the one-stage LNA in this work is cascode structure. The cascode structure has the advantage of reduced Miller Effect because input impedance of the common-gate stage will result in low voltage gain for the common-source stage. In addition to attain high gain, excellent reverse isolation will be achieved so that better stability is guaranteed when operating frequency is pushed up to 24 GHz. Because the input impedance of the common-gate stage in the cascode structure is in general higher than the output impedance of the common-source stage, the noise contributed from the common-gate stage can be ignored.

Fig. 4.9 illustrates the simulated relation between f_T and bias voltage of cascode device. The channel length is set at the minimum value of 45 nm. The channel width is varied from 5 μm to 80 μm. The peak f_T approaches 250 GHz as the gate bias voltage is about 0.7–0.8 V. The one-stage LNA is constrained to power consumption smaller than 5 mW under the supply voltage of 1 V. Based on the aforementioned relation that the minimum noise figure bias of MOSFET is about 0.15 mA/μm, the channel width of the cascode device is about 30 μm. Fig. 4.10 shows the simulated relation among f_T, g_m, and bias voltage of the cascode device. As the bias voltage equal to about 0.85 V, the cascode device will have best linearity. However, with such high bias voltage, the transistors will enter linear region and therefore the f_T will degrade dramatically. Because the performance of the NF is the most important, the bias voltage is set at 0.7 V to get the best f_T, but at the cost of linearity degradation.

The circuit diagram of the presented one-stage LNA is shown in Fig. 4.11. M_1 and



(a)



(b)

Figure 4.9 The simulated relation between f_T and bias voltage of cascode device with the channel width which is varied from 5 μm to 80 μm, and the minimum channel length of 45 nm.

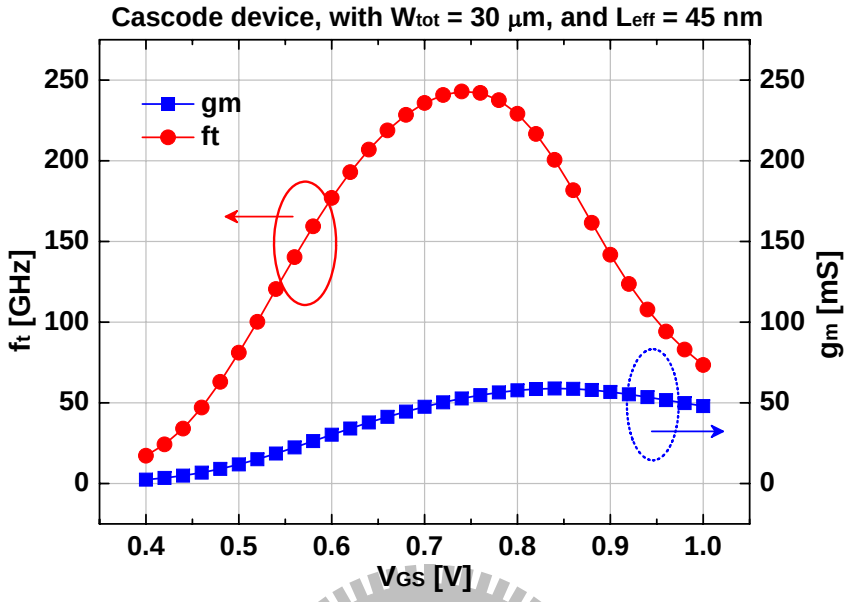


Figure 4.10 The simulated relation among f_T, g_m, and bias voltage of cascode device.

M_2 is the cascode device with W/L equal to 30μm/45nm. The gate bias voltage V_G of the M_1 is fed through the inductor L_g. The gate of M_2 is connected to V_{DD}. C_5 and C_6 are the bypass capacitors that stabilize the dc bias of V_G and V_{DD}. The inductive load L_d is used to resonate out the parasitic. The output of the LNA is designed to match 50 Ω by the capacitive impedance divider formed by the MIM capacitor C_3, C_4, and the parasitic capacitor C_{pad2} contributed from output pad. The input matching is achieved by L_s, L_g, C_1, C_2, and the parasitic capacitor $Cpad1$ contributed from input pad. Ignoring the gate-to-drain parasitic capacitance of M_1 and the parasitic capacitance of input pad C_{pad1}, the input impedance Z_{in} is given by

$$Z_{in}(s) \approx \frac{1}{sC_1} + sL_g \parallel \left(\frac{1}{sC_{gs,M_1}} + sL_s + \frac{g_{m1}L_s}{C_{gs,M_1}} \right) \tag{4.3}$$

where g_{m1} and C_{gs,M_1} is the transconductance and gate-to-source parasitic capacitance of M_1. $\Im\{Z_{in}\}$ is tuned out at the center frequency $\omega_0 = [(L_g + L_s) \cdot C_{gs,M_1}]^{-1/2}$, and $\Re\{Z_{in}\}$ is designed to approach 50 Ω. Hence, the following two conditions should be satisfied.

$$\left[g_{m1} \frac{L_s}{L_g} \left(1 + \frac{L_s}{L_g} \right) \right]^{-1} = 50 \tag{4.4}$$

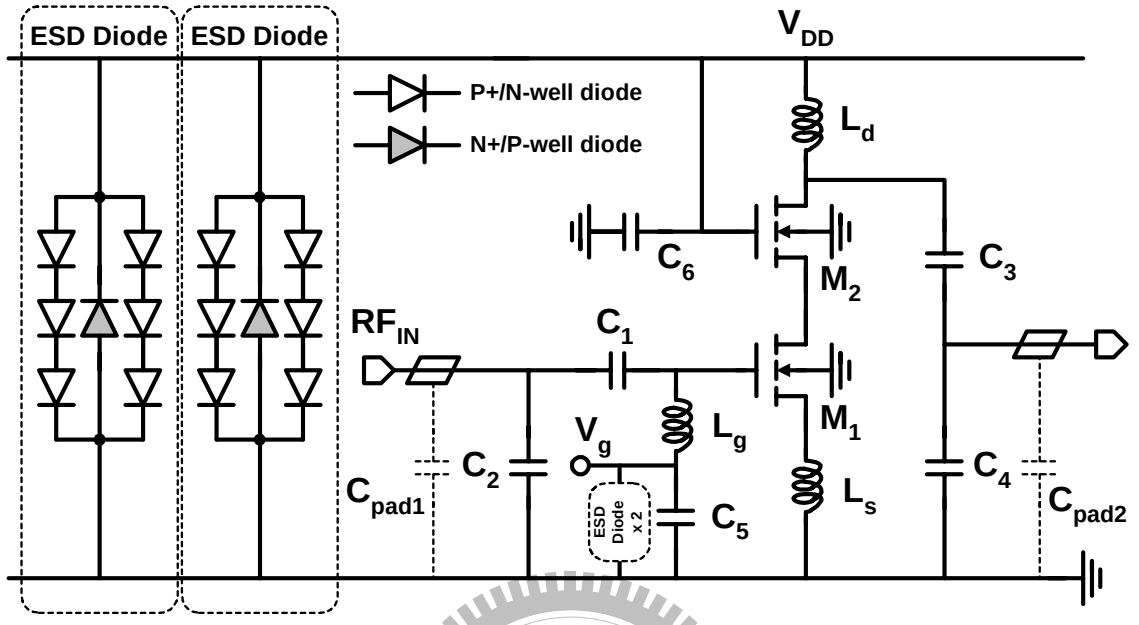


Figure 4.11 Circuit diagram of the one-stage cascode LNA.

$$C_1 = C_{gs,M_1}\left(1 + \frac{L_s}{L_g}\right) \tag{4.5}$$

For simultaneous impedance and noise matching, C_1, L_s, and L_g should be selected properly with an appropriate bias condition such that $\Re\{Z_{opt}^*\} = \Re\{Z_{in}\} = 50\Omega$ and $\Im\{Z_{opt}^*\} = \Im\{Z_{in}\} = 0$ at the center frequency. There exists an optimum L_s for the simultaneous impedance and noise matching without significant degradation of F_{min}. To lower the noise figure, M_1 is biased closed to maximum f_T at a certain gate bias voltage. At higher gate bias voltage, the f_T will drop due to high-electrical-field mobility degradation, and more power will be consumed. Thus, less noise degradation and more power saving will be achieved by biasing M_1 slightly before reaching its maximum f_T point.

In this one-stage LNA design, the WLP technology is used to realize the low-cost high-Q above-IC inductors L_d, L_g, and L_s. L_d and L_g are one-turn sprial inductors. L_s is a microstrip transmission line inductor, where the signal path is realized in the WLP process, and the ground path is realized by the metal-1 and metal-2 of the back-end process in this 45-nm gate length planar bulk-CMOS tehcnology. In the WLP process, the 5-μm

thick metal layer of Cu on the 20-μm low-k dielectric of BCB has been postprocessed on top of the 45-nm planar bulk-CMOS process. From the HFSS simulation, the Q factors of L_d, L_g, and L_s at 23 GHz can be extracted as 48, 39, and 39, respectively. In addition, the values of L_d, L_g, and L_s are 0.38 nH, 0.45nH, and 0.2 nH, respectively. The shallow trench isolation (STI) P+/N-Well and N+/P-Well diodes are implemented between supply/bias (V_{DD} and V_g) and ground for ESD protection. The drawing dimension of each STI diode is 19.35 μm by 1.85 μm. The small input matching capacitors C_2 and C_4 are possible to be replaced with the STI diodes. However, the size of these STI diodes will not large enough to provide enough ESD protection. Moreover, the nonlinear effect of the STI diodes at the input will degrade the linearity performance of LNA. To prevent from degrading the RF performance, the input and output pads are not protected by these STI ESD diodes in this design.

The layout diagram of the one-stage cascode LNA is depicted in Fig. 4.12. The design parameters of the one-stage cascode LNA is shown in Table 5.3. As shown in Fig. 4.13(a), the center frequency of the LNA is at 24.5 GHz, and the LNA has a simulated S_{21} of 12 dB. Shown in Fig. 4.13(b) is the input and output matching characteristics. The simulated S_{11} is below –10 dB within the frequency range from 23.4 GHz to 26 GHz, which is 10.6 % of the center frequency. The simulated S_{22} is below –10 dB within the frequency range from 22.7 GHz to 26.9 GHz, which is 17 % of the center frequency. The bandwidth is designed to larger than 10 % of the center frequency to cover the process variations. As shown in Fig. 4.14, the simulated NF of the one-stage cascode 1.6 dB. At the operating frequency of 24.5 GHz, the NF approaches NF_{min}, which means that the input matching network is well designed and the optimum noise matching is achieved. The stability analyses are shown in Fig. 4.15 and Fig. 4.16, which indicates that the presented one-stage LNA is unconditionally stable. As shown in Fig. 4.17, the one-stage LNA has a P_{IIP3} of about –0.87 dBm with the two-tone testing signals at 24 GHz and 24.5 GHz. This one-stage LNA drains 4.58 mA from the 1-V power supply voltage. The total power consumption is 4.58 mW.

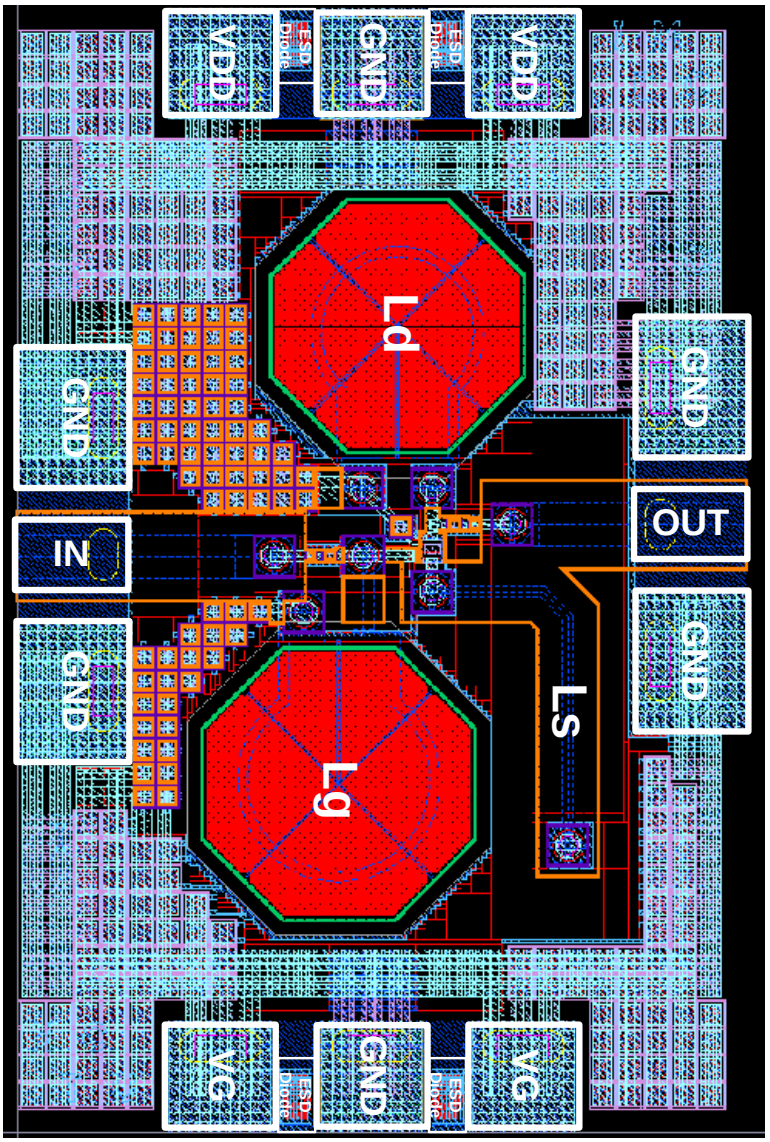


Figure 4.12 Layout diagram of the one-stage cascode LNA.

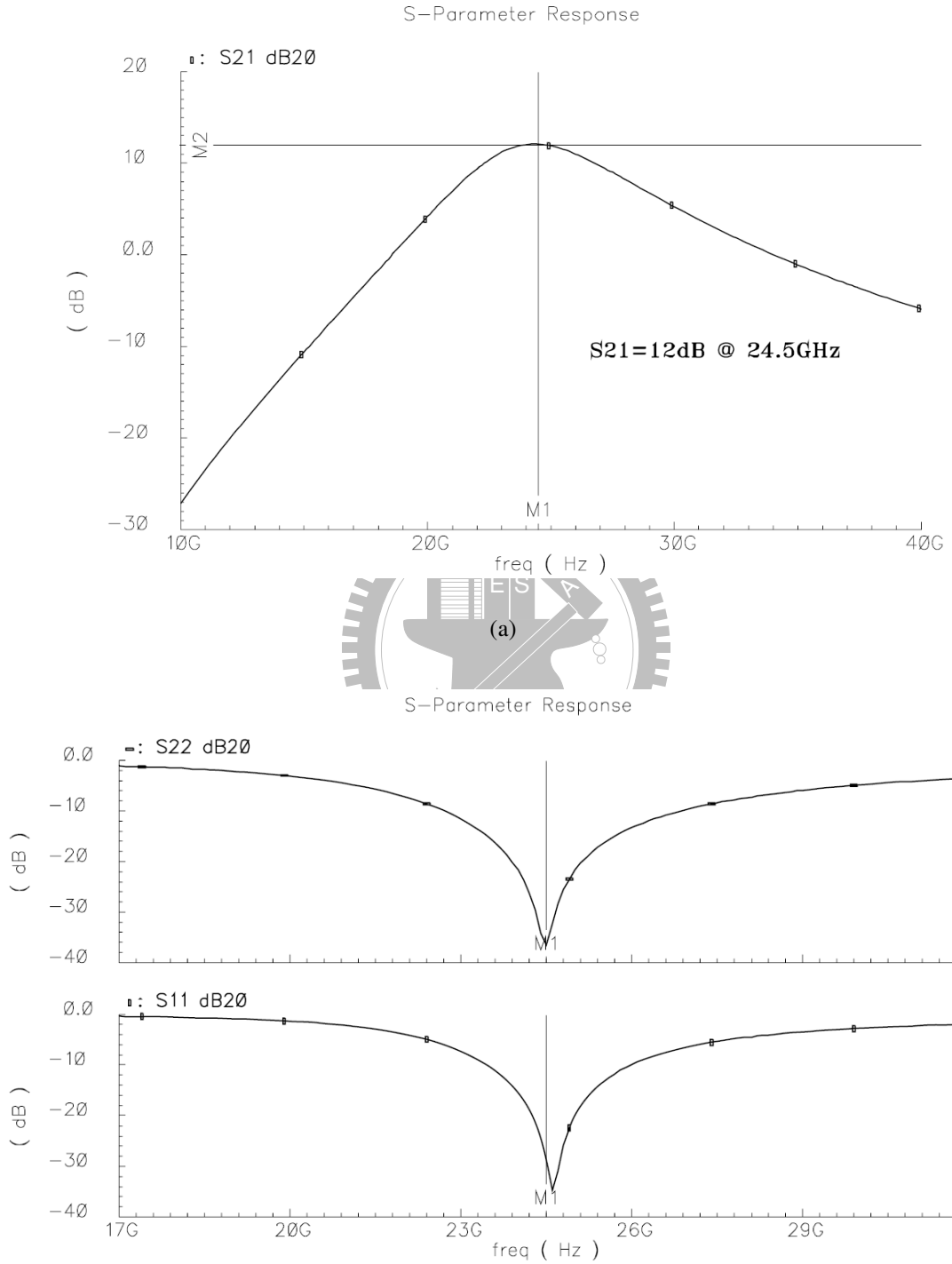


Figure 4.13 Simulated S-parameters of one-stage cascode LNA.

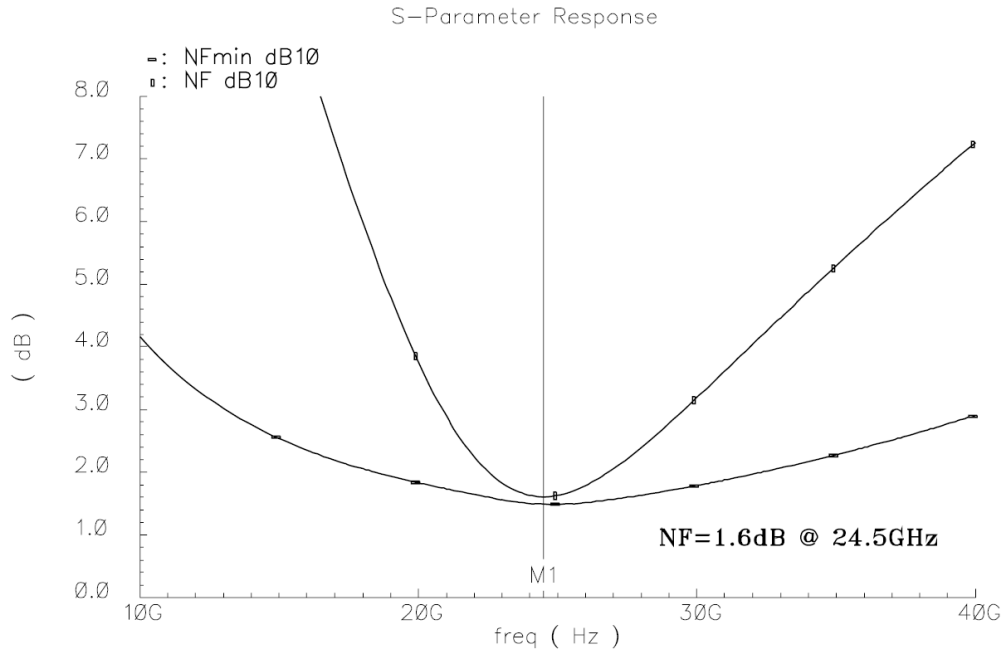


Figure 4.14 Simulated NF and NF_{min} of one-stage cascode LNA.

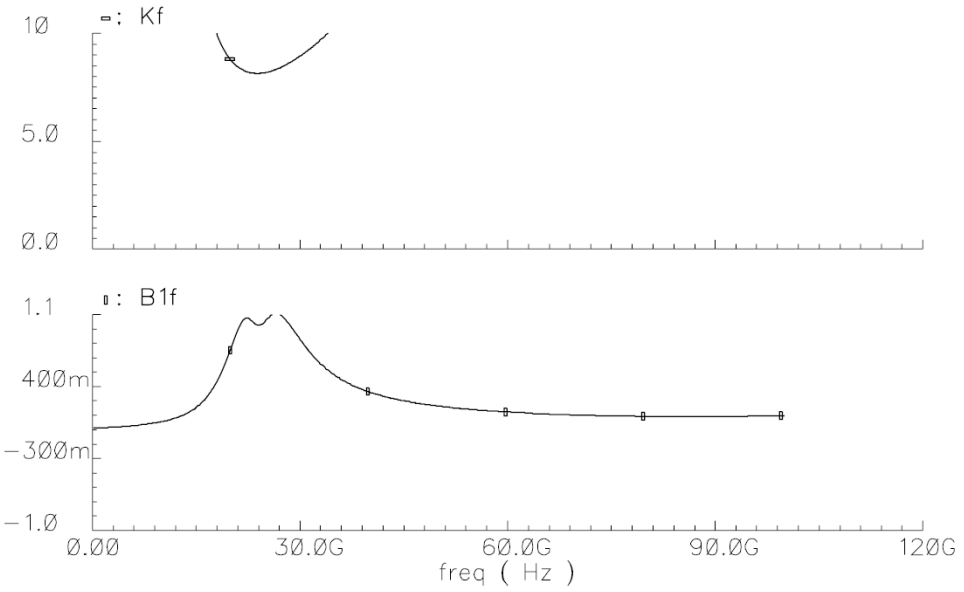


Figure 4.15 Simulated stability factor of one-stage cascode LNA.

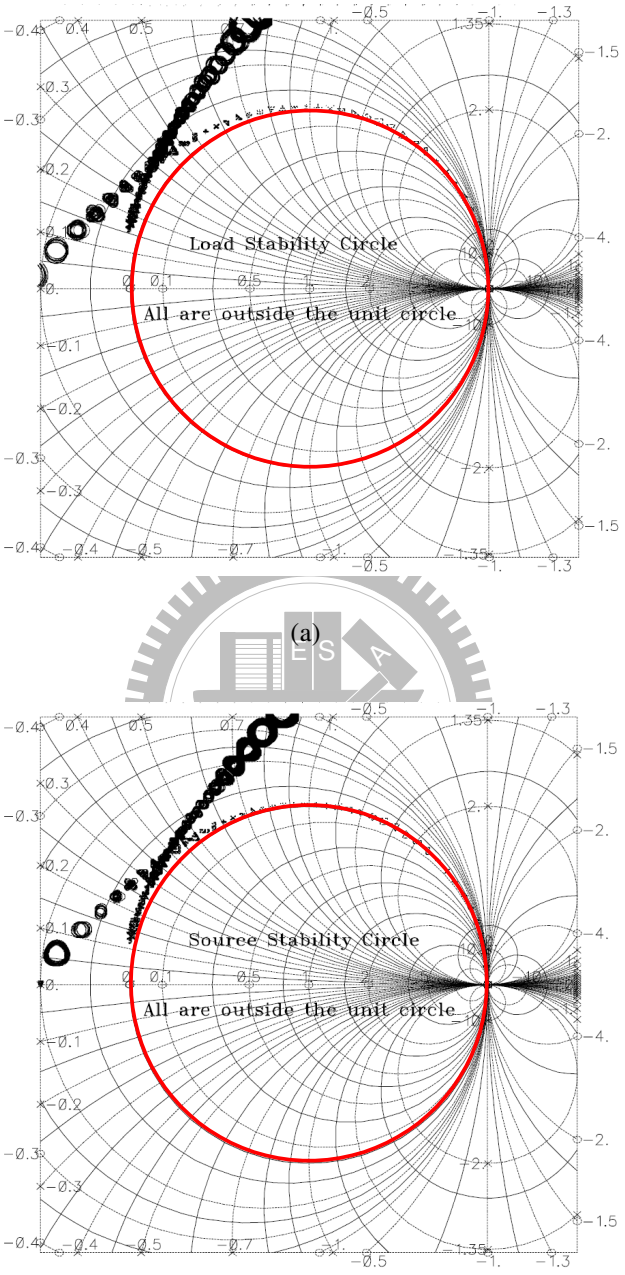


Figure 4.16 Simulated (a) load stability circle, and (b) source stability circle of one-stage cascode LNA.

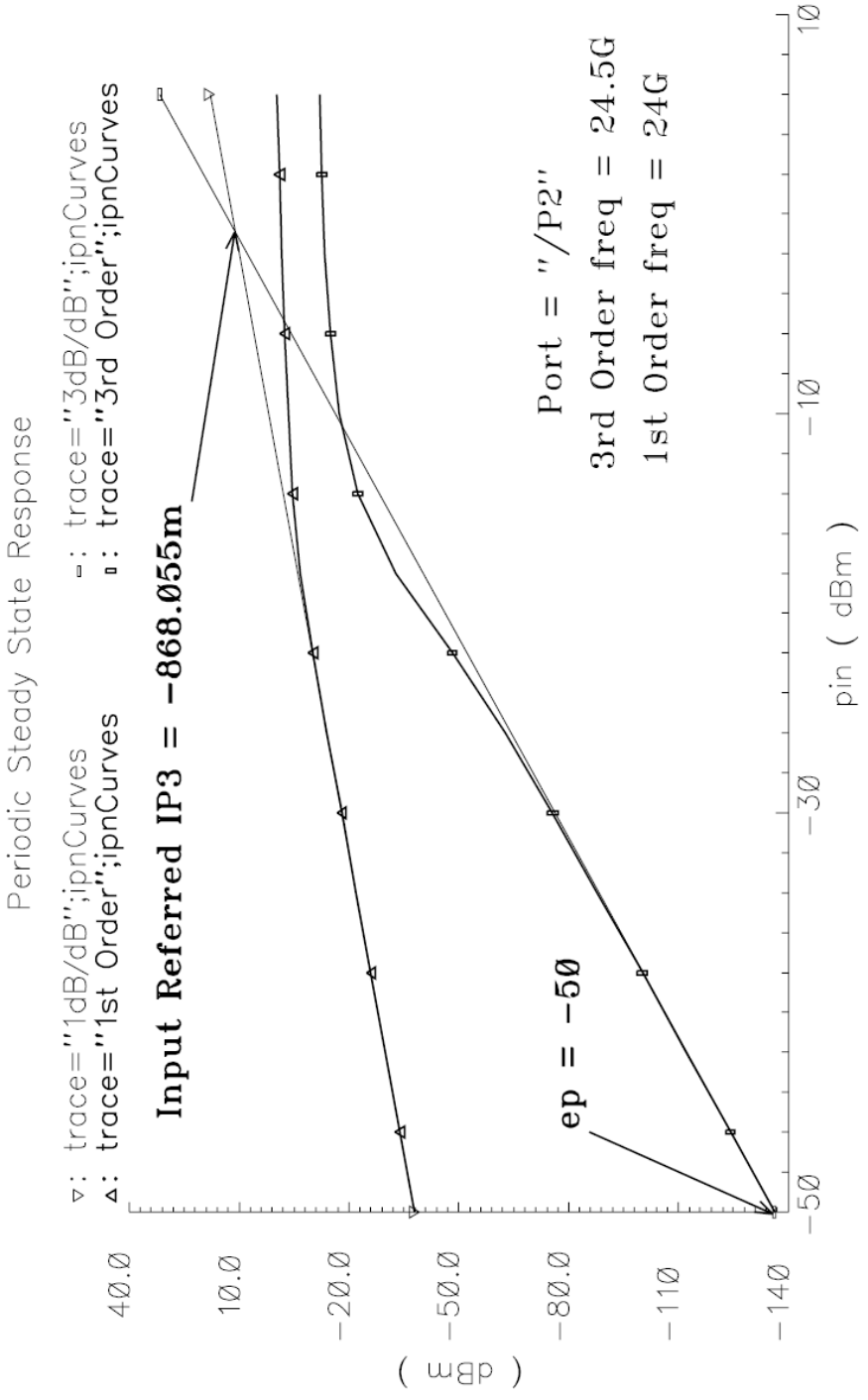


Figure 4.17 Simulated linearity performance of one-stage cascode LNA.

Table 4.3
DESIGN PARAMETERS OF ONE-STAGE CASCODE LNA

One-stage cascode Low Noise Amplifier	
M_1, M_2	30 μm / 45 nm
C_1	50 fF
C_2	40 fF
C_3	80 fF
C_4	60 fF
C_5, C_6	>10 pF
L_g	0.45 nH
L_s	0.2 nH
L_d	0.38 nH
P+\N-well STI Diode (ESD)	19.35 μm × 1.85 μm
N+\P-well STI Diode (ESD)	19.35 μm × 1.85 μm

4.2.2 Two-stage cascaded cascode LNA

The circuit diagram of the presented two-stage cascaded cascode LNA is shown in Fig. 4.18. As for the first stage, M_3 and M_4 is the cascode device of the first stage, and both transistors are with W/L equal to 30μm/45nm. The gate bias voltage V_{g1} of the M_3 is fed through the inductor L_{g1}. The gate of M_4 is connected to V_{DD1}. C_{15} and C_{16} are the bypass capacitors that stabilize the dc biases of V_{g1} and V_{DD1}. The inductive load L_{d1} is used to resonate out the parasitic. The output of the first stage is designed to match 50 Ω by the capacitive impedance divider formed by the MIM capacitor C_9 and C_{10}. The input matching of the first stage is achieved by L_{s1}, L_{g1}, C_7, C_8, and the parasitic capacitor C_{pad3} contributed from input pad. Considering to noise matching and impedance matching at the same time, the values of C_7, C_8, L_{s1}, and L_{g1} are designed based on the discussions in Section 5.4.1.

As for the second stage, M_5 and M_6 form the cascode device of the second stage, and the transistor sizes are with W/L equal to 30μm/45nm and 40μm/45nm, respectively. The gate bias voltage V_{g2} of the M_5 is fed through the inductor L_{g2}. The gate of M_6 is connected to V_{DD2}. C_{17} and C_{18} are the bypass capacitors that stabilize the dc biases of V_{g2}

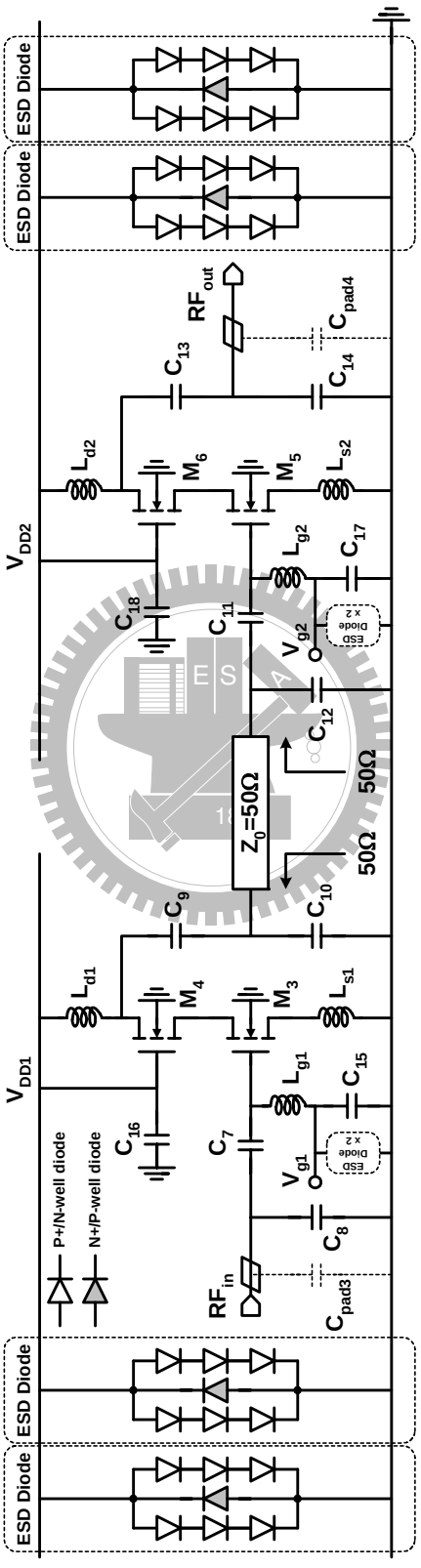


Figure 4.18 Circuit diagram of the two-stage cascaded cascode LNA.

and V_{DD2}. The inductive load L_{d2} is used to resonate out the parasitic. The output of the second stage is designed to match 50 Ω by the capacitive impedance divider formed by the MIM capacitor C_{13}, C_{14}, and the parasitic capacitor C_{pad4} contributed from output pad. The input matching of the second stage is achieved by C_{11}, C_{12}, L_{s2}, and L_{g2}. Because the designed gain of the first stage is not large, the second stage is also required to have low-noise performance. Considering to noise matching and impedance matching at the same time, the values of C_{11}, C_{12}, L_{s2}, and L_{g2} are also designed based on the previous discussions.

Because the input and output impedance of the two stages are all designed to match 50 Ω, the two stages are cascaded directly through the 50-Ω microstrip line which is designed by the WLP-M1 is used to link the two stages.

In this two-stage LNA design, the WLP technology is used to realize the high-Q inductors L_{d1}, L_{d2}, L_{g1}, L_{g2}, L_{s1}, and L_{s2}, where L_{d1}, L_{d2}, L_{g1} and L_{g2} are one turn spiral inductors, and L_{s1} and L_{s2} are microstrip transmission line inductors. The values of L_{d1}, L_{d2}, L_{g1}, L_{g2}, L_{s1}, and L_{s2} are 0.38 nH, 0.2 nH, 0.45 nH, 0.45 nH, 0.2 nH, and 0.2 nH, respectively. The STI P+/N-well and N+/P-well diodes are also implemented between supply/bias (V_{DD1},V_{DD2}, V_{g1}, and V_{g2}) and ground for ESD protection. The drawing dimension of each STI diode is 19.35 μm by 1.85 μm. The small input matching capacitors C_8 and C_{14} are possible to be replaced with the STI diodes. However, the size of these STI diodes will not large enough to provide enough ESD protection. Moreover, the nonlinear effect of the STI diodes at the input will degrade the linearity performance of LNA. To prevent from degrading the RF performance, the input and output pads are not protected by these STI ESD diodes in this design.

The layout diagram of the two-stage cascaded cascode LNA is depicted in Fig. 4.19. The design parameters of the one-stage cascode LNA is shown in Table 5.4. As shown in Fig. 4.20(a), the center frequency of the LNA is at 24.5 GHz, and the LNA has a simulated S_{21} of 22.7 dB. Shown in Fig. 4.20(b) is the input and output matching characteristics. The simulated S_{11} is below –10 dB within the frequency range from 23.3 GHz to 25.86 GHz, which is 10.4 % of the center frequency. The simulated S_{22} is below –10 dB within the frequency range from 23.05 GHz to 26.29 GHz, which is 13 % of the center frequency. The bandwidth is designed to larger than 10 % of the center frequency to cover the process

Table 4.4
DESIGN PARAMETERS OF TWO-STAGE CASCADED CASCODE LNA

Two-stage cascaded cascode Low Noise Amplifier	
M_3, M_4, M_5	30 μm / 45 nm
M_6	40 μm / 45 nm
C_7	50 fF
C_8	40 fF
C_9	75 fF
C_{10}	52 fF
C_{11}	51 fF
C_{12}	52 fF
C_{13}	92.5 fF
C_{14}	40 fF
C_{15}, C_{16}, C_{17}, C_{18}	>10 pF
L_{g1}	0.45 nH
L_{s1}	0.2 nH
L_{d1}	0.38 nH
L_{g2}	0.45 nH
L_{s2}	0.2 nH
L_{d2}	0.2 nH
P+\N-well STI Diode (ESD)	19.35 μm × 1.85 μm
N+\P-well STI Diode (ESD)	19.35 μm × 1.85 μm

variations. As shown in Fig. 4.2.2, the simulated NF of the one-stage cascode 1.62 dB. At the operating frequency of 24.5 GHz, the NF approaches NF_{min}, which means that the input matching network is well designed and the optimum noise matching is achieved. The stability analyses are shown in Fig. 4.22 and Fig. 4.23, which indicates that the presented two-stage LNA is unconditionally stable. As shown in Fig. 4.24, the one-stage LNA has a P_{IIP3} of about –12.43 dBm with the two-tone testing signals at 24 GHz and 24.5 GHz. This one-stage LNA drains 8.79 mA from the 1-V power supply voltage. The total power consumption is 8.79 mW.

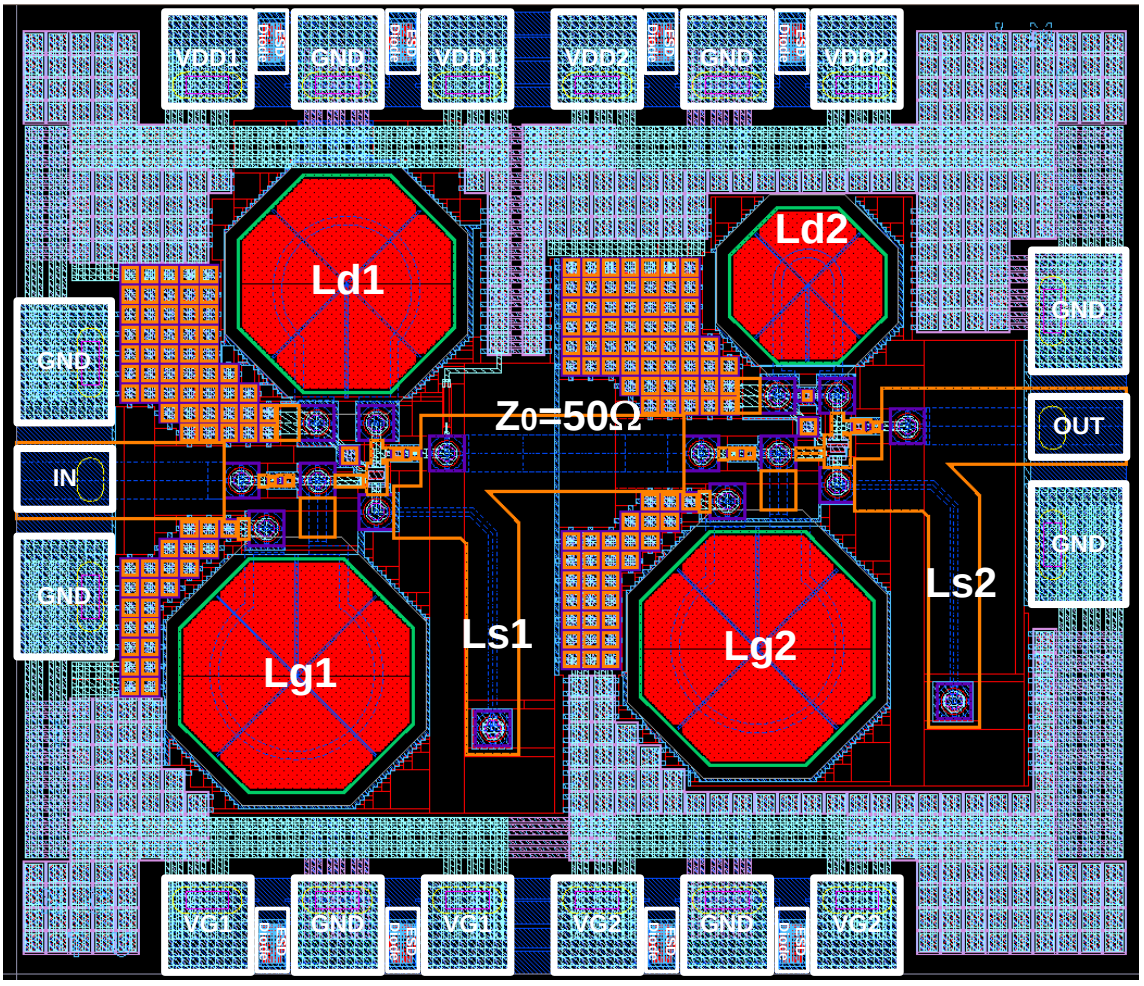


Figure 4.19 Layout diagram of the two-stage cascaded cascode LNA.

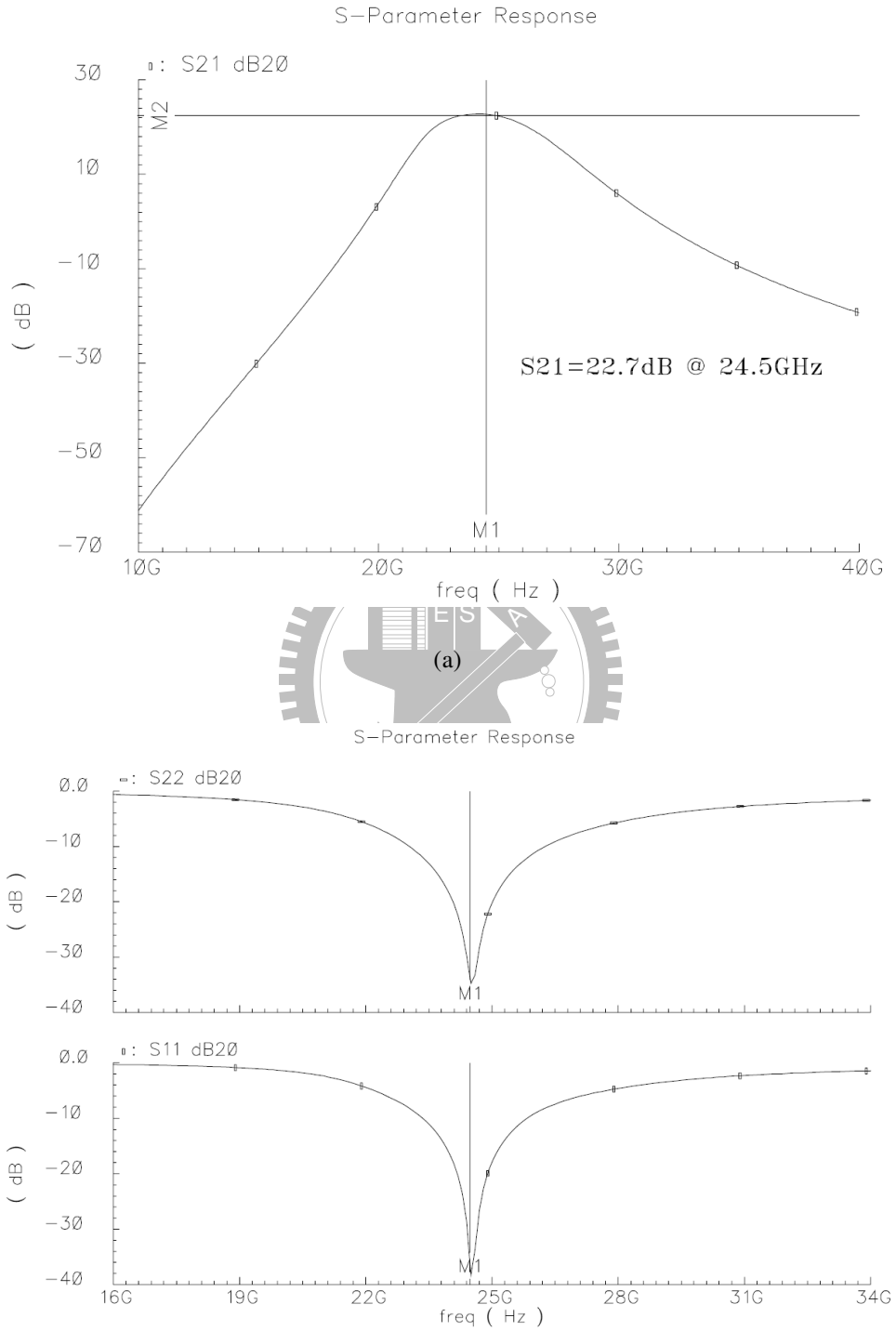


Figure 4.20 Simulated S-parameters of the two-stage cascaded cascode LNA.

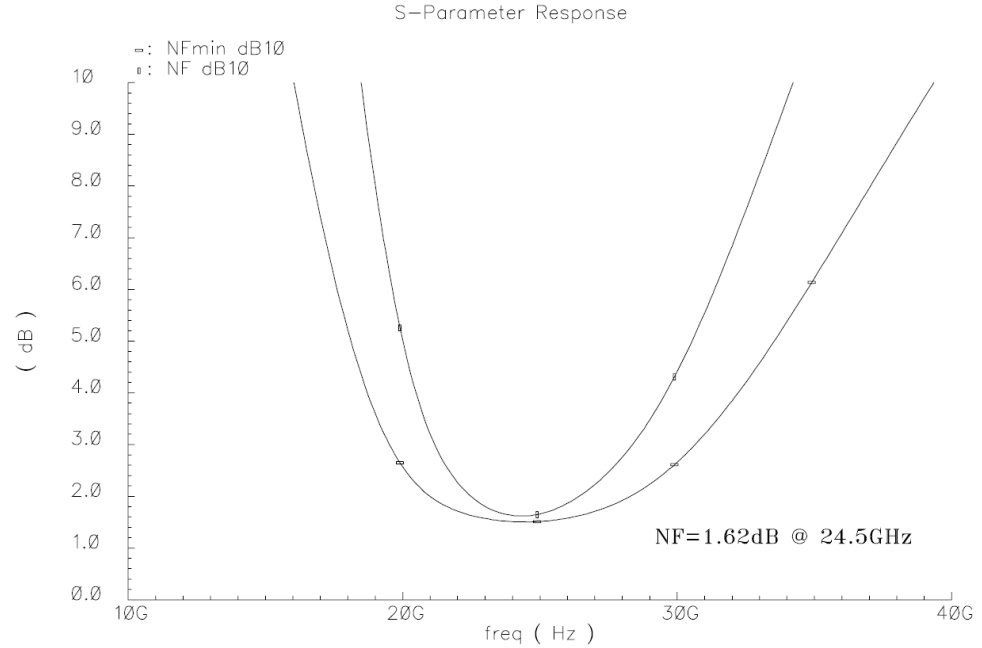


Figure 4.21: Simulated NF and NF_{min} of two-stage cascaded cascode LNA.

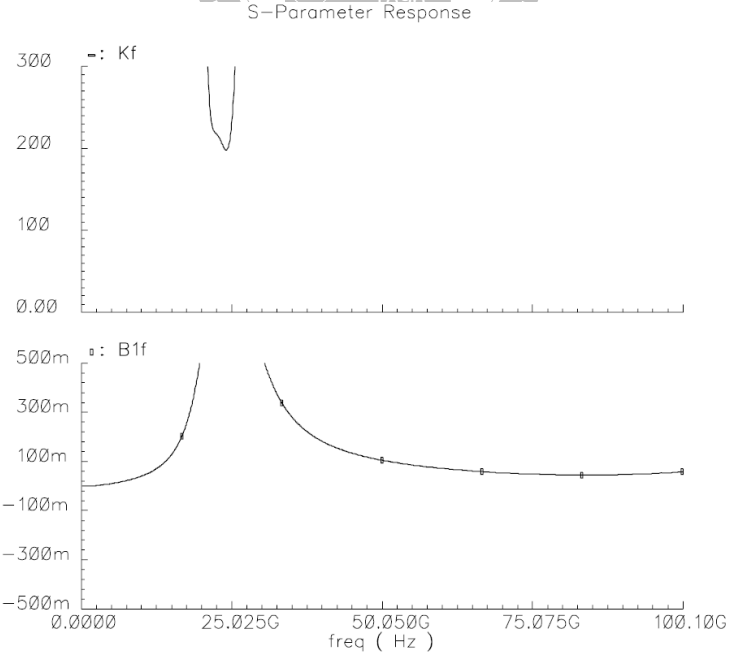
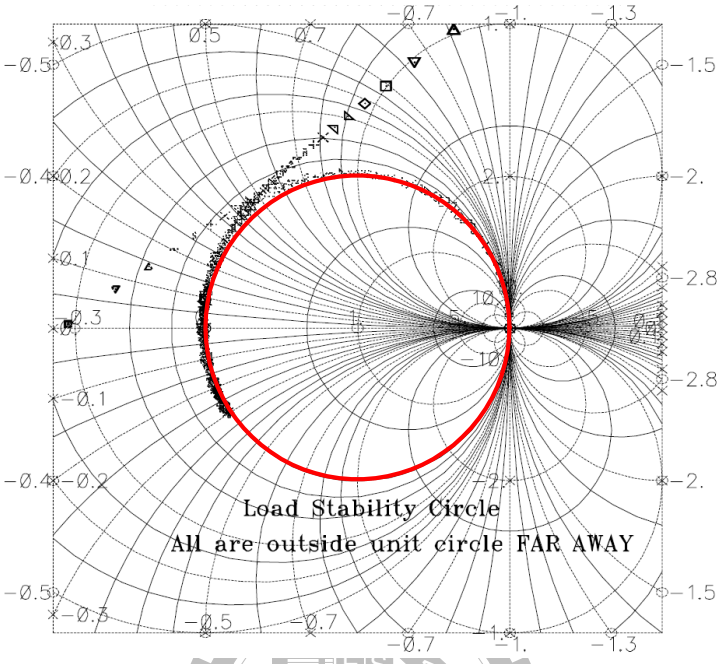
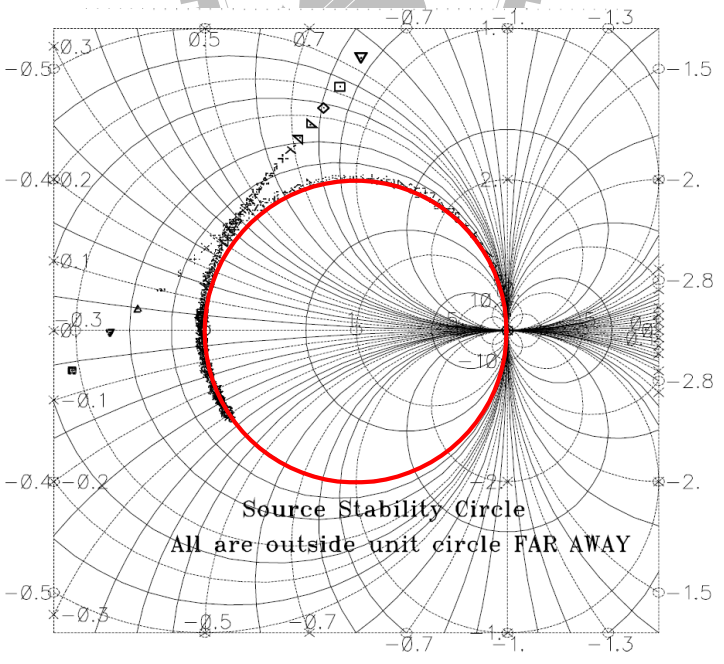


Figure 4.22 Simulated stability factor of two-stage cascaded cascode LNA.



(a)



(b)

Figure 4.23 Simulated (a) load stability circle, and (b) source stability circle of two-stage cascaded cascode LNA.

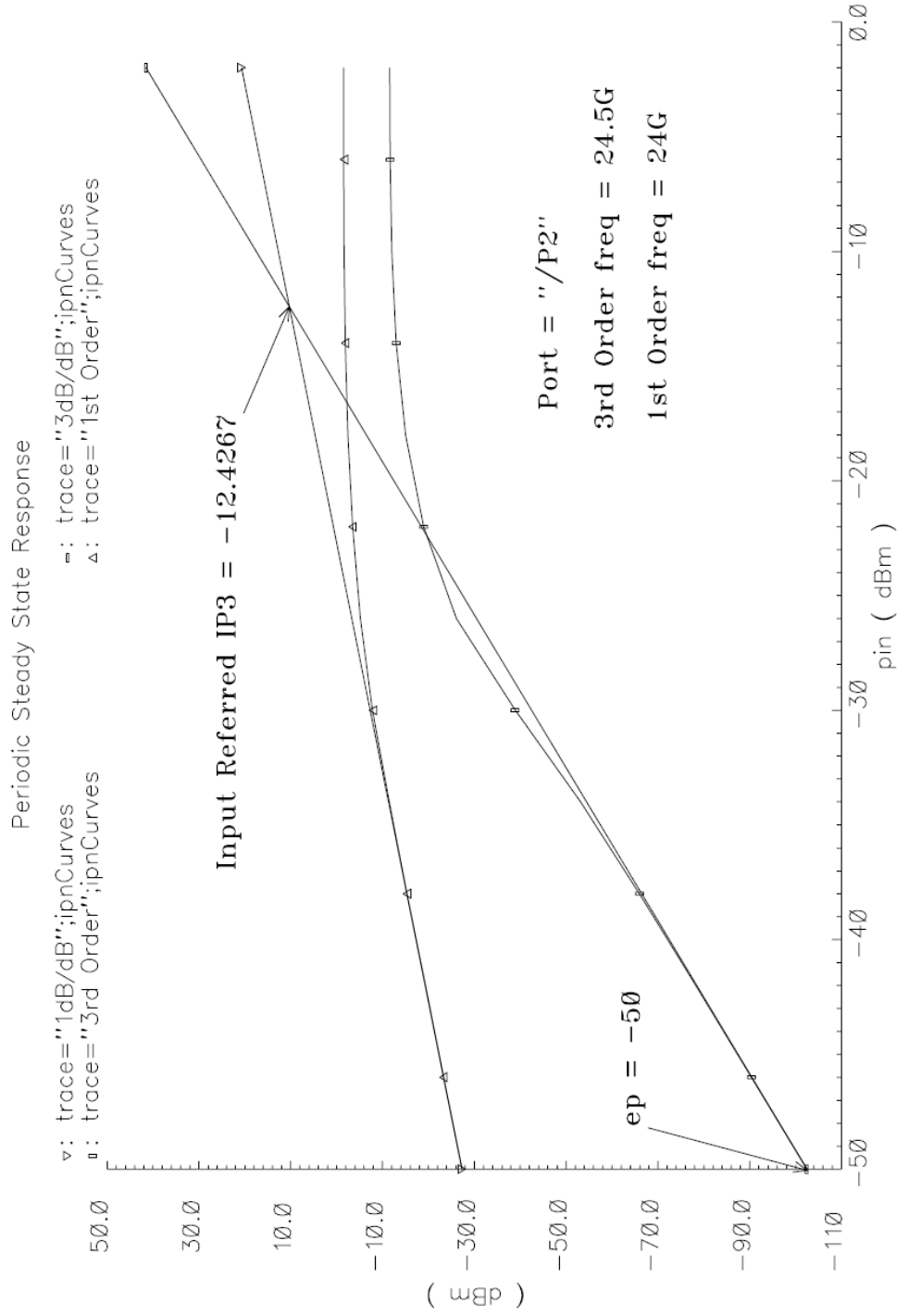


Figure 4.24 Simulated linearity performance of two-stage cascaded cascode LNA.

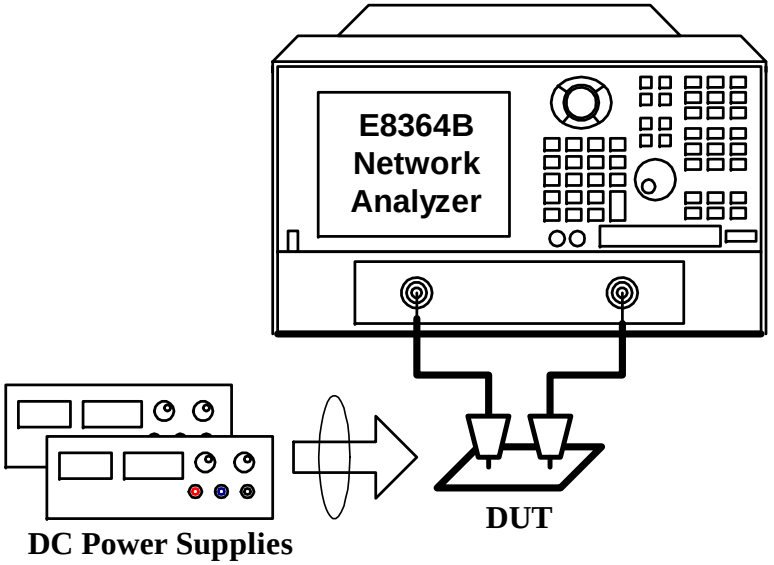


Figure 4.25 Environment setup of S-parameter measurements.

4.3 Experimental Results

The measured environment setups of the presented LNAs are described as follows. On-wafer probing measurement is adopted to verify the performance. Two GSG RF probes with the pitch of 100 μm are used for probing the input and output pads of the LNAs. As for measuring one-stage LNA, two 3-pin dc probes with the pitch of 150 μm are used for probing the testing dc pads. As for measuring two-stage cascaded LNA, two 6-pin dc probes with pitch of 150 μm are used for probing the testing dc pads. As shown in Fig. 4.25, the S-parameters are measured to analyze the matching characteristics of input and output ports by the network analyzer, Agilent E8364B, which can characterize the S-parameter performance from 10 MHz to 50 GHz. To measure the linearity performance of the LNAs, two signal generators Agilent E8257D are used to provide two RF signals for the LNAs. The power combiner Agilent 11616B is used to sum the RF signal in advanced. The signal analyzer Agilent E4448A is used to monitor the spectrum to verify the linearity and power gain of the LNAs. The measurement environment is illustrated in Fig. 4.26.

Furthermore, the NF of the LNAs is measured by the signal analyzer Agilent E4448A

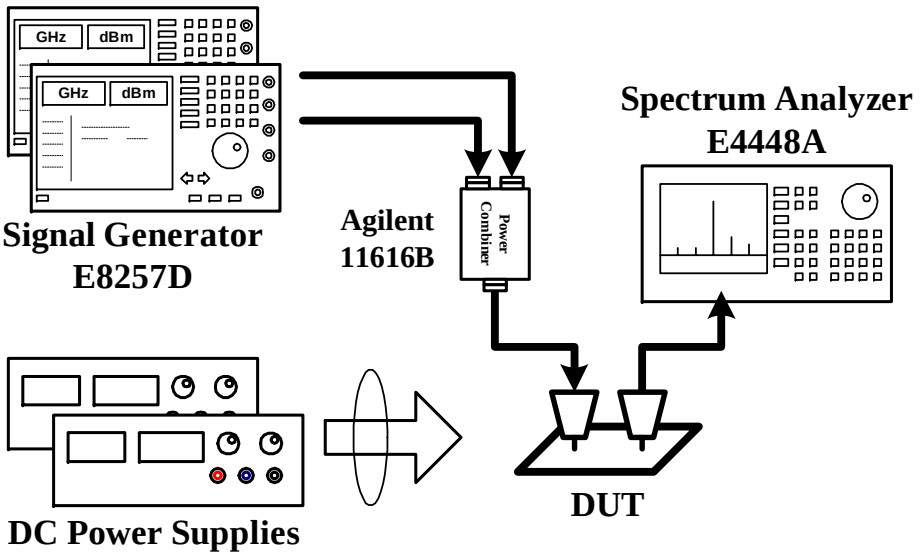


Figure 4.26 Environment setup of linearity measurements.

which is embedded with noise figure option. The broadband noise source of Agilent 346CK01 is used. The measurement environment and measurement steps are illustrated in Fig. 4.27. To measure the NF of the LNAs, the noise characterization through Y-factor technique is used and three separate steps are required. The first step as shown in Fig. 4.27(a) is the calibration of the noise figure analyer (NFA, the signal analyzer Agilent E4448A with noise figure option is used) together with noise source (Agilent 346CK01) and preamplifier (Agilent 83051A). When this setup is completed, the intrinsic NF of NFA and the gain and NF of preamplifier have been calibrated out. After calibrating the NFA, the additional losses can be estimated using the setup of Fig. 4.27(b). A through on the reference calibratioin substrate (the same used to calibrate PNA) is used to estimate the combined losses of two RF GSG probes, two 2.4-mm RF cables, and two 2.4mm-to-3.5mm adaptors which are used to wafer-probe the LNA. Because of the symmetry setup, the total losses are the equally split as *before* and *after* DUT losses as shown in Fig. 4.27(b), and are loaded into the NFA losses compensation table. Finally, as shwon in Fig. 4.27(c), the DUT is inserted to measure its NF.

Fig. 4.28 shows the chip micrograph of the one-stage cascode LNA. It occupies the

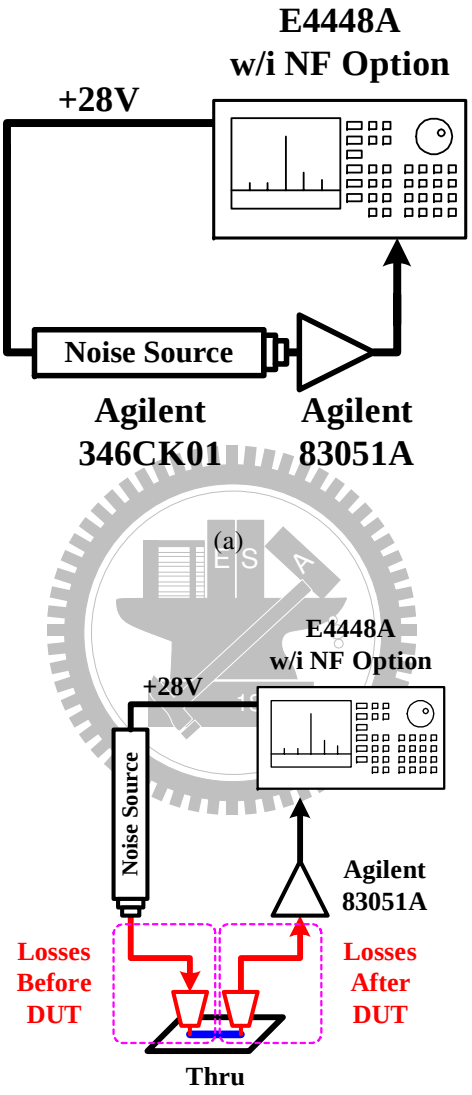
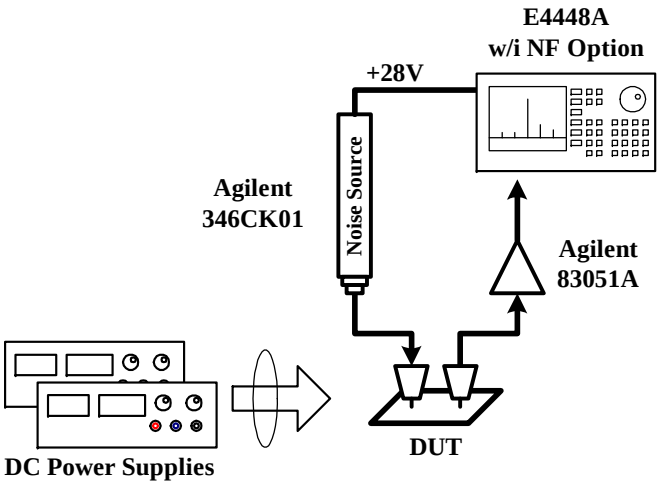


Figure 4.27 Environment setup of noise figure measurements. (a) Calibration, (b) evaluate the losses before and after DUT, and (c) NF measurement.



(c)

Figure 4.27 Environment setup of noise figure measurements. (a) Calibration, (b) evaluate the losses before and after DUT, and (c) NF measurement (*Con't*).

active area of 0.72 × 1.12 mm^2 including the testing pads. Under the supply voltage V_{DD} of 1 V and the gate biasing voltage V_G of 0.45 V, the one-stage LNA draws the currents of 3.6 mA. The measured S-parameters of the LNA are shown in Fig. 4.29(a) and Fig. 4.29(b). The input and output reflection coefficients, S_{11} and S_{22}, are smaller than –5 dB at 23 GHz. Furthermore, the gain, S_{21}, of the one-stage LNA is about 7.1 dB. Due to the cascode configuration, the reverse isolation, S_{12}, can be smaller than –25 dBm over the desired frequency range. In Fig. 4.30, the measured NF at 23 GHz is about 4 dB, under the condition that $V_{DD} = 1V$ and $V_G = 0.45V$. The power gain and NF of the one-stage LNA with different bias conditions are depicted in Fig. 4.31.

The one-tone test results of the one-stage LNA are depicted in Fig. 4.32. With the test signal at the frequency of 23 GHz, it reveals that the one-stage LNA has the IP_{-1dB} of –9 dBm. The measured one-tone test results with different bias conditions are shown in Fig. 4.33. The Fig. 4.34 shows the output spectrum with the two test signals at 23.1 GHz and 23.15 GHz, respectively. The two signals are with the same signal level of –24.3 dBm. It shows that the one-stage LNA has a P_{IIP3} of +2.25 dBm.

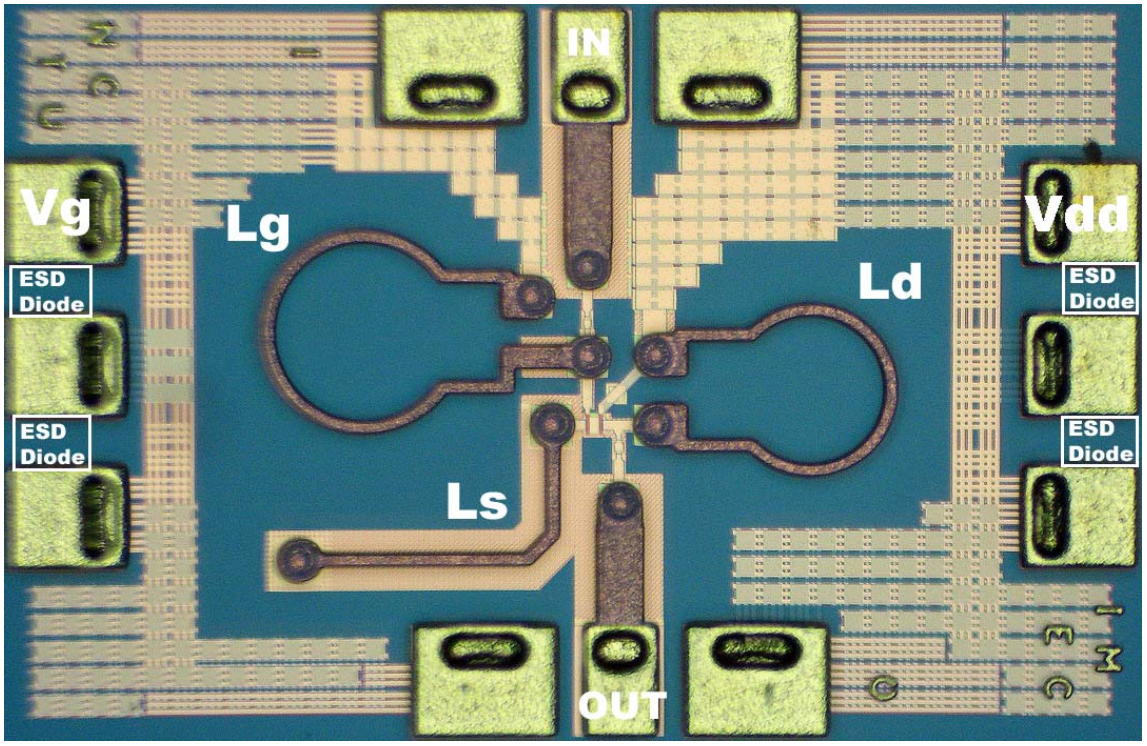


Figure 4.28 Chip microphotography of the one-stage cascode LNA.

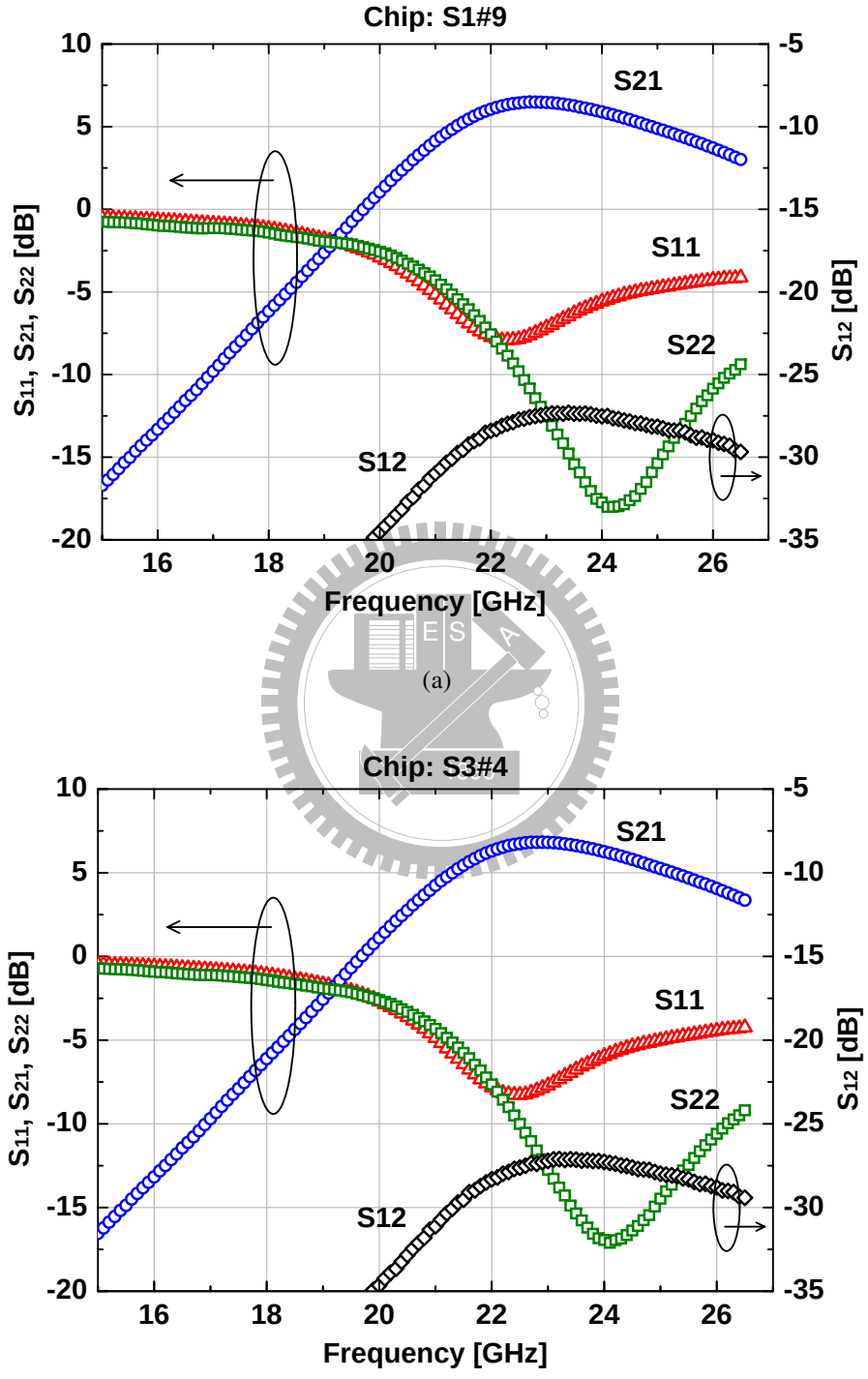


Figure 4.29 Measured S-parameters of the one-stage cascode LNA of (a) Chip S1#9, and (b) Chip S3#4.

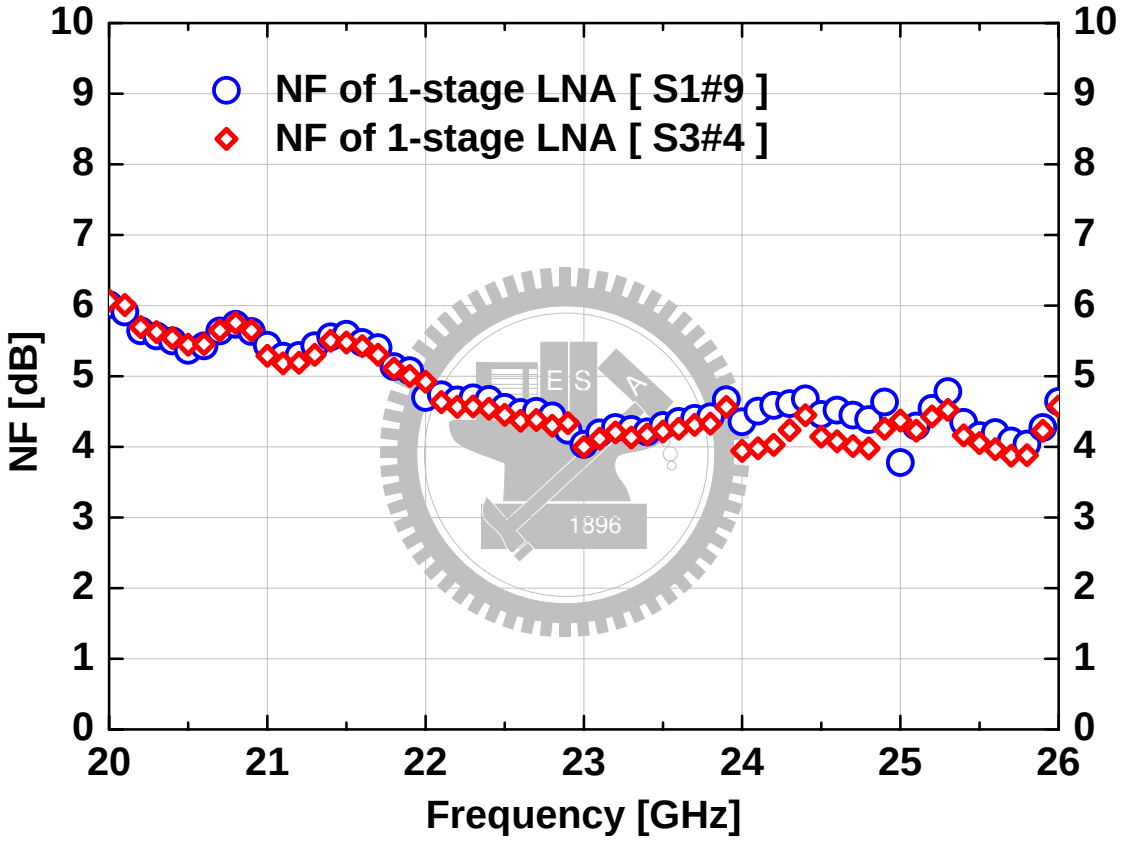
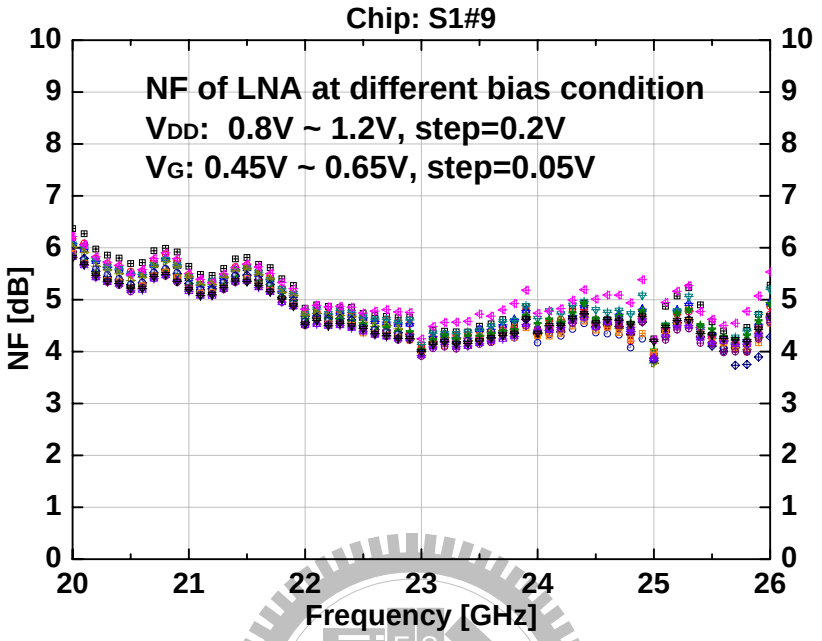
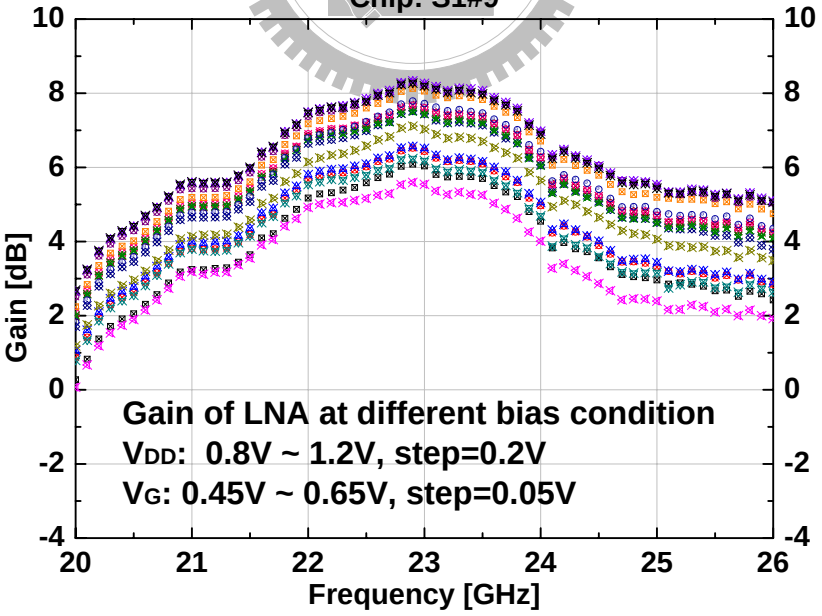


Figure 4.30 Measured NF of the one-stage cascode LNA of Chip S1#9 and Chip S3#4.

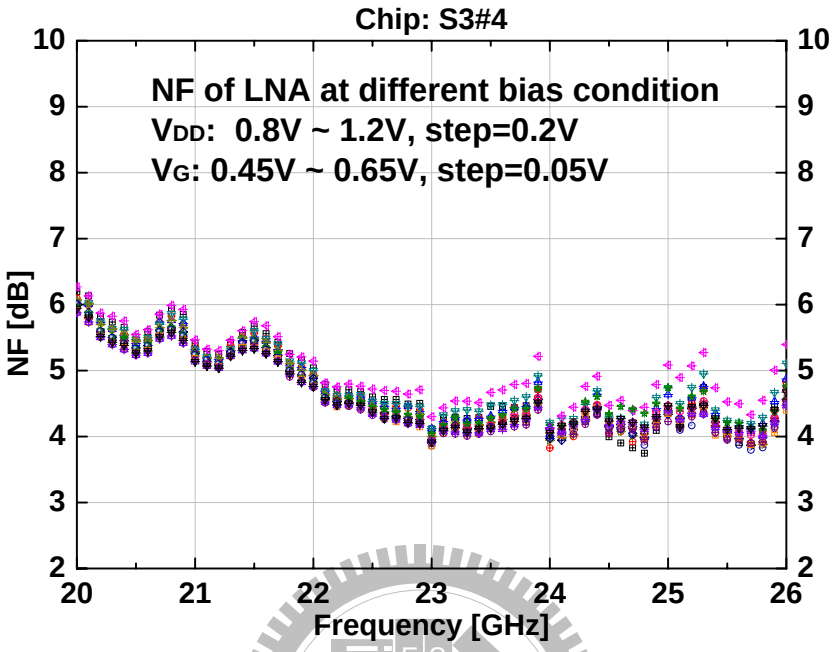


(a)

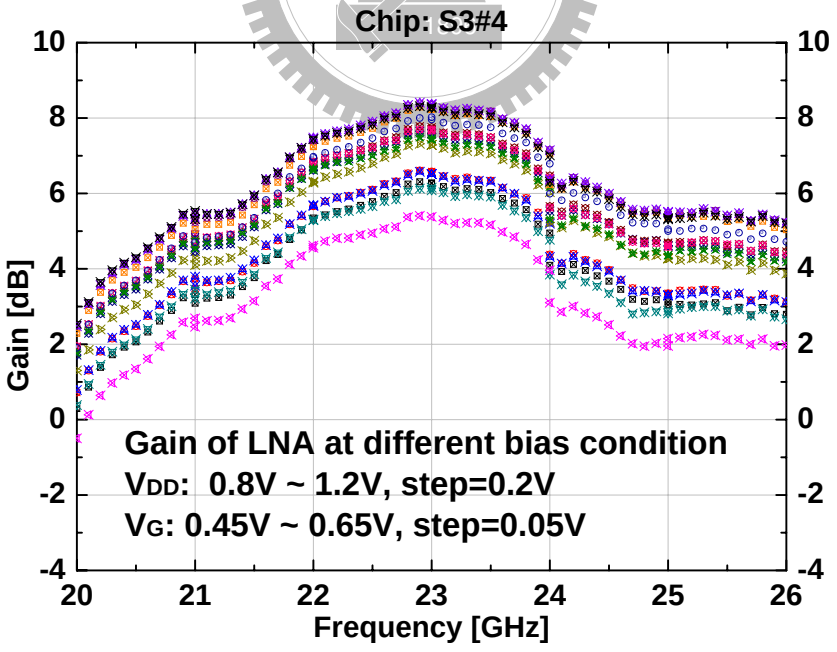


(b)

Figure 4.31 Measured NF and Gain of the one-stage cascode LNA with different bias conditions. (a) NF of Chip S1#9. (b) Gain of Chip S1#9. (c) NF of Chip S3#4. (d) Gain of Chip S3#4.

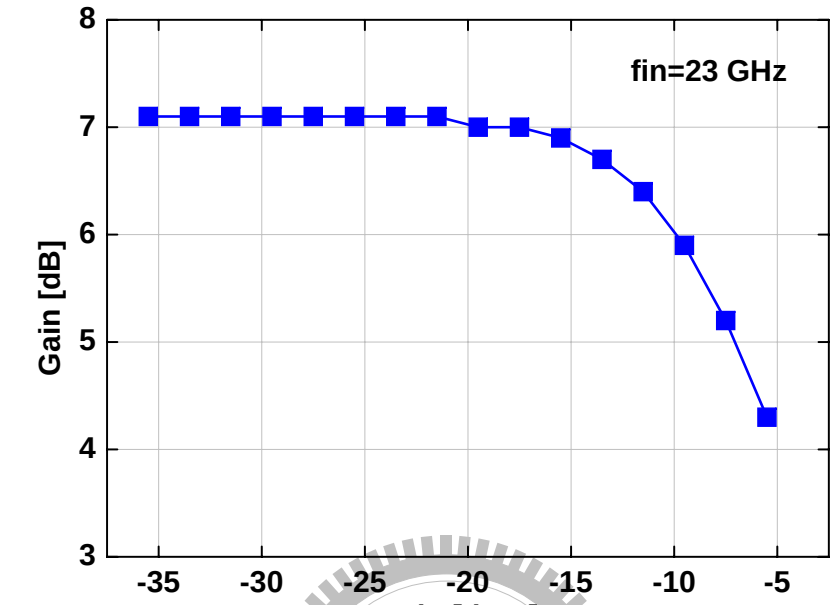


(c)

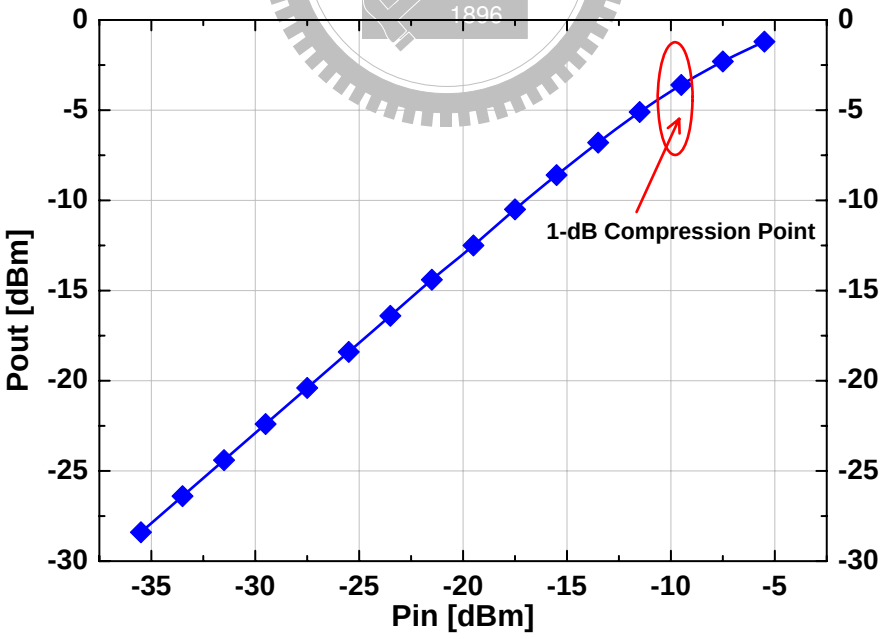


(d)

Figure 4.31 Measured NF and Gain of the one-stage cascode LNA with different bias conditions. (a) NF of Chip S1#9. (b) Gain of Chip S1#9. (c) NF of Chip S3#4. (d) Gain of Chip S3#4 (*Con't*).



(a)



(b)

Figure 4.32 Measured one-tone testing results of the one-stage cascode LNA.

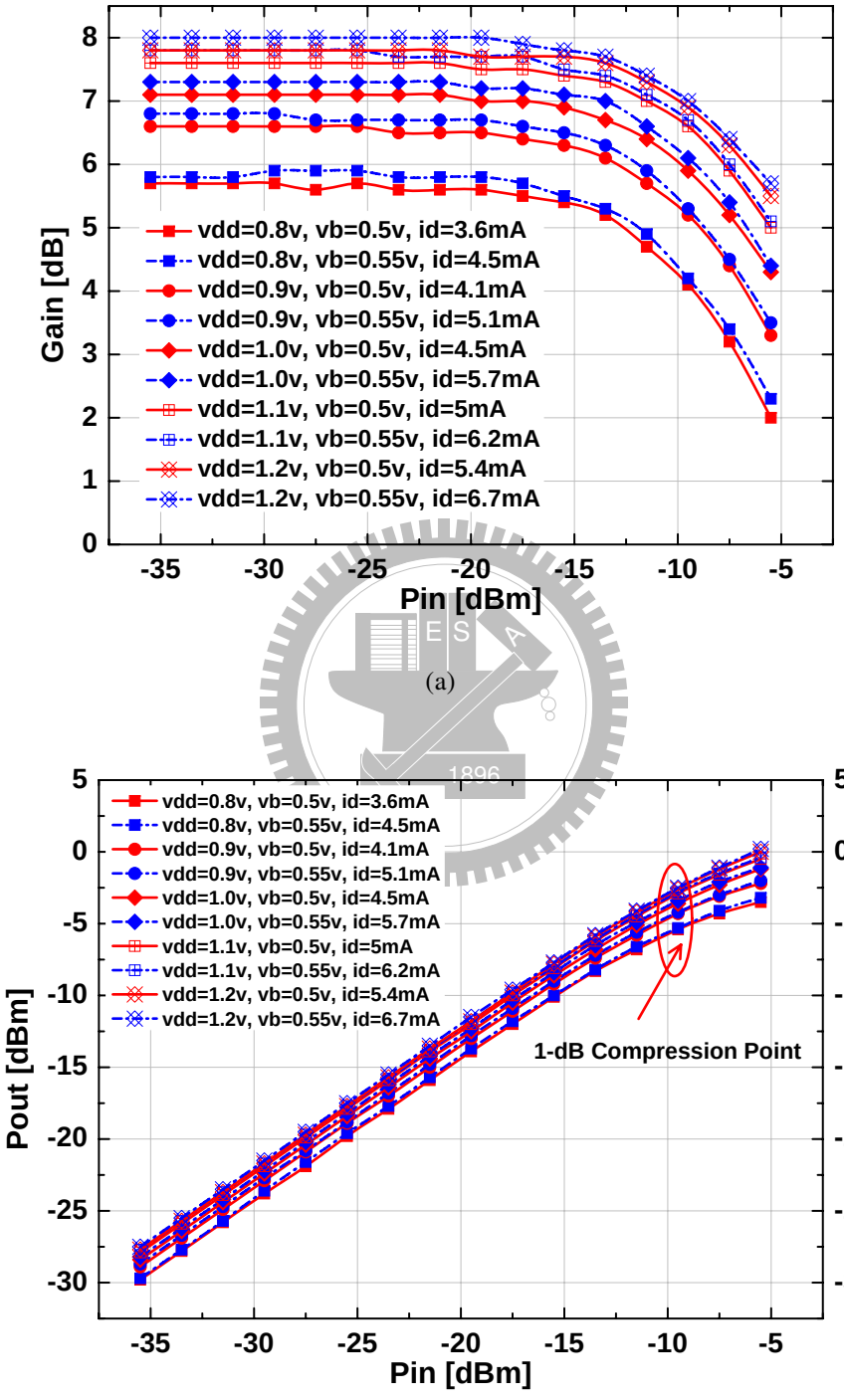


Figure 4.33 Measured one-tone testing results of the one-stage cascode LNA with different bias conditions.

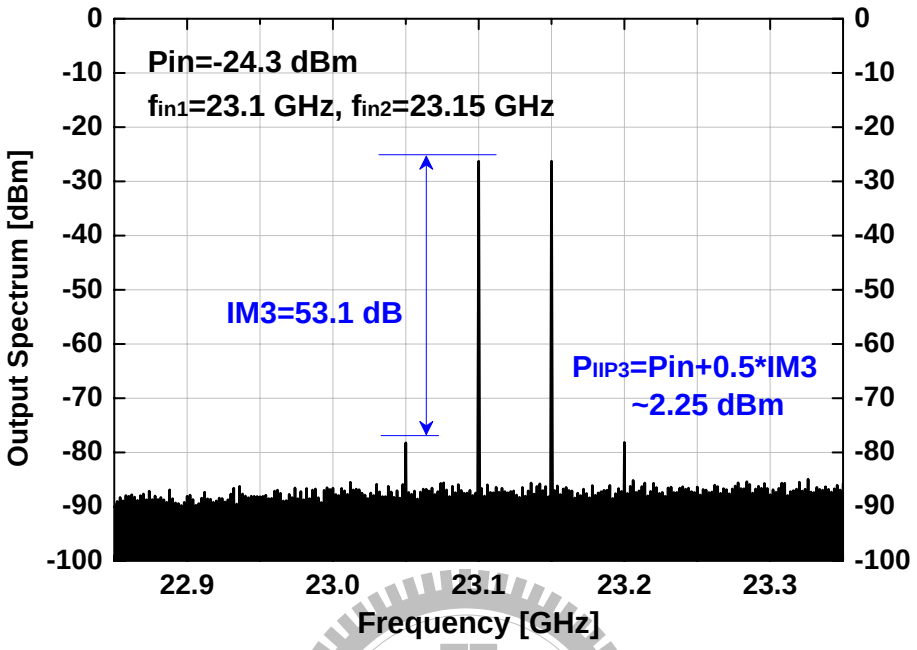


Figure 4.34 Measured two-tone testing results of the one-stage cascode LNA.

Fig. 4.35 shows the chip micrograph of the two-stage cascaded cascode LNA. It occupies the active area of 1.28 × 1.12 mm^2 including the testing pads. Under the conditions of $V_{DD1} = V_{DD2} = 1V$, $V_{g1} = 0.45V$, and $V_{g2} = 0.5V$, the two-stage LNA dissipates the power consumption of 9.3 mW. The measured S-parameters of the two-stage LNA are shown in Fig. 4.36(a) and Fig. 4.36(b). The input and output reflection coefficients, S_{11} and S_{22}, are smaller than –5 dB at 23.4 GHz. Furthermore, the gain, S_{21}, of the two-stage LNA is about 11.6 dB at the frequency of 23.4 GHz. The two-stage LNA has good revere isolation, and the S_{12} is smaller than –45 dB over the desired frequency range. In Fig. 4.37, the measured NF at 23.4 GHz is about 4.4 dB, under the conditions of $V_{DD1} = V_{DD2} = 1V$, $V_{g1} = 0.45V$, and $V_{g2} = 0.5V$. The power gain and NF of the two-stage LNA with different bias conditions are depicted in Fig. 4.38.

The one-tone test results of the two-stage LNA are depicted in Fig. 4.39. With the test signal at the frequency of 23.2 GHz, it reveals that the two-stage LNA has the IP_{-1dB} of –16 dBm. The measured one-tone test results with different bias conditions are shown in Fig. 4.40. The Fig. 4.41 shows the output spectrum with the two test signals at 23.15 GHz

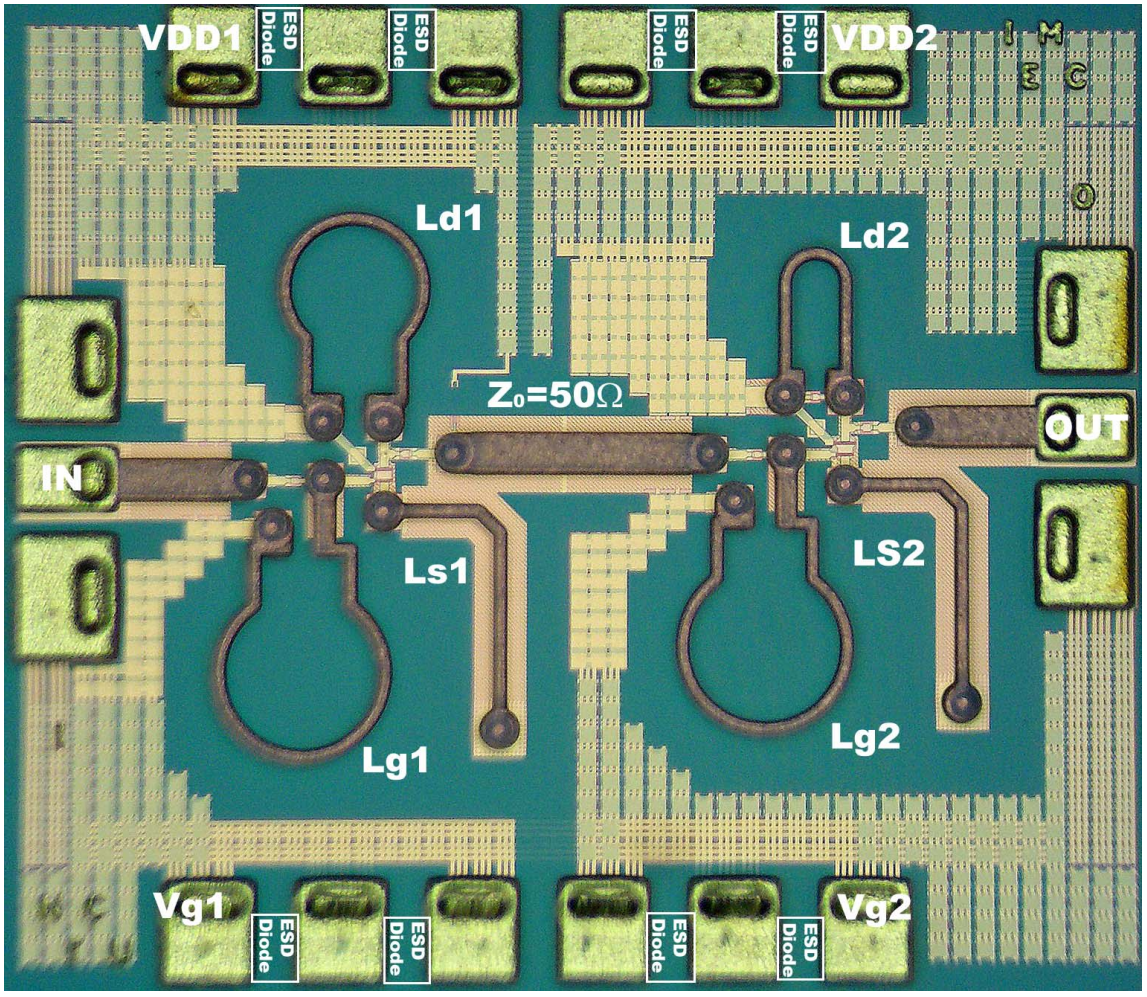
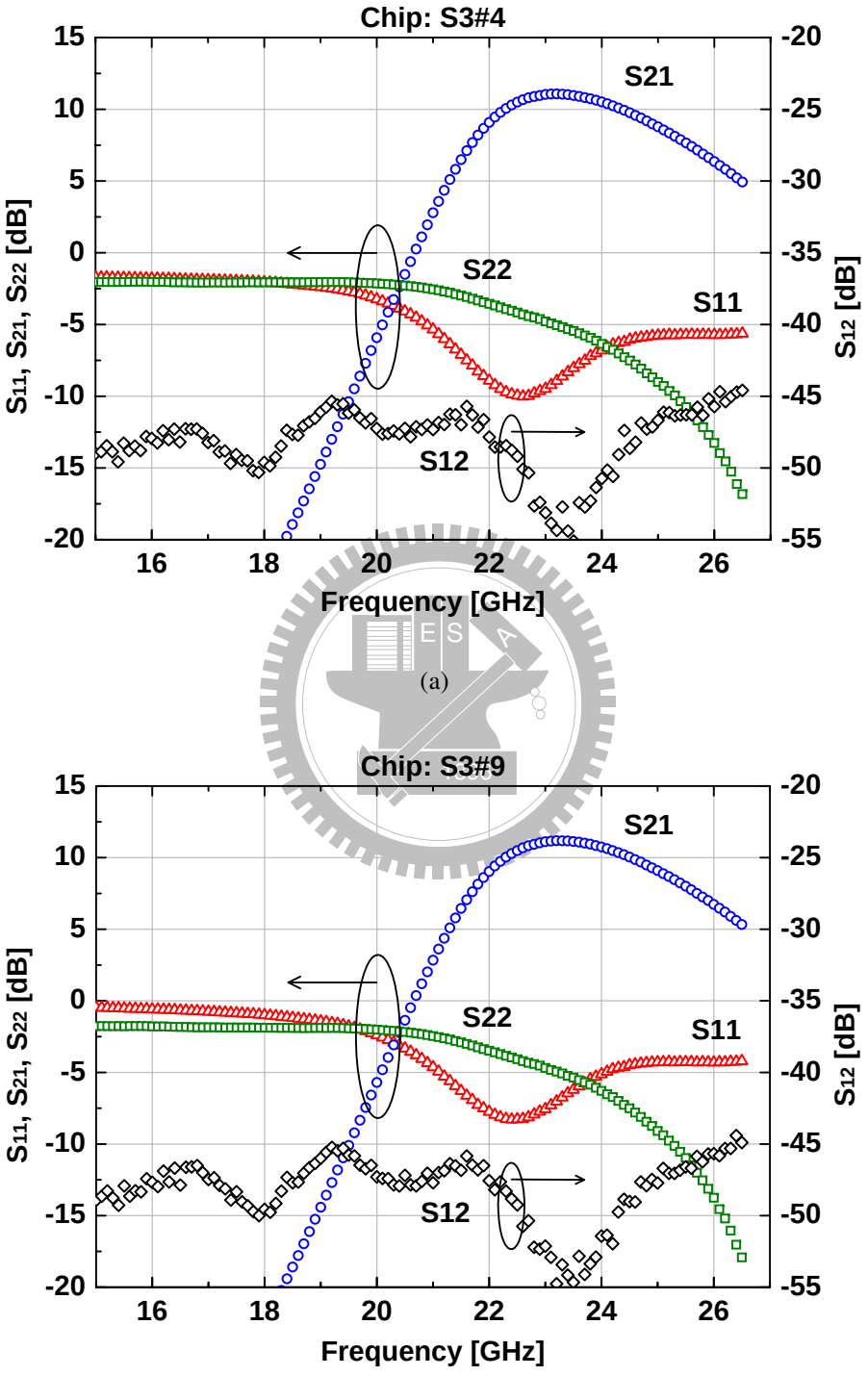


Figure 4.35 Chip microphotography of the two-stage cascaded cascode LNA.



(a)

(b)

Figure 4.36 Measured S-parameters of the two-stage cascaded cascode LNA of (a) Chip S3#4, and (b) Chip S3#9.

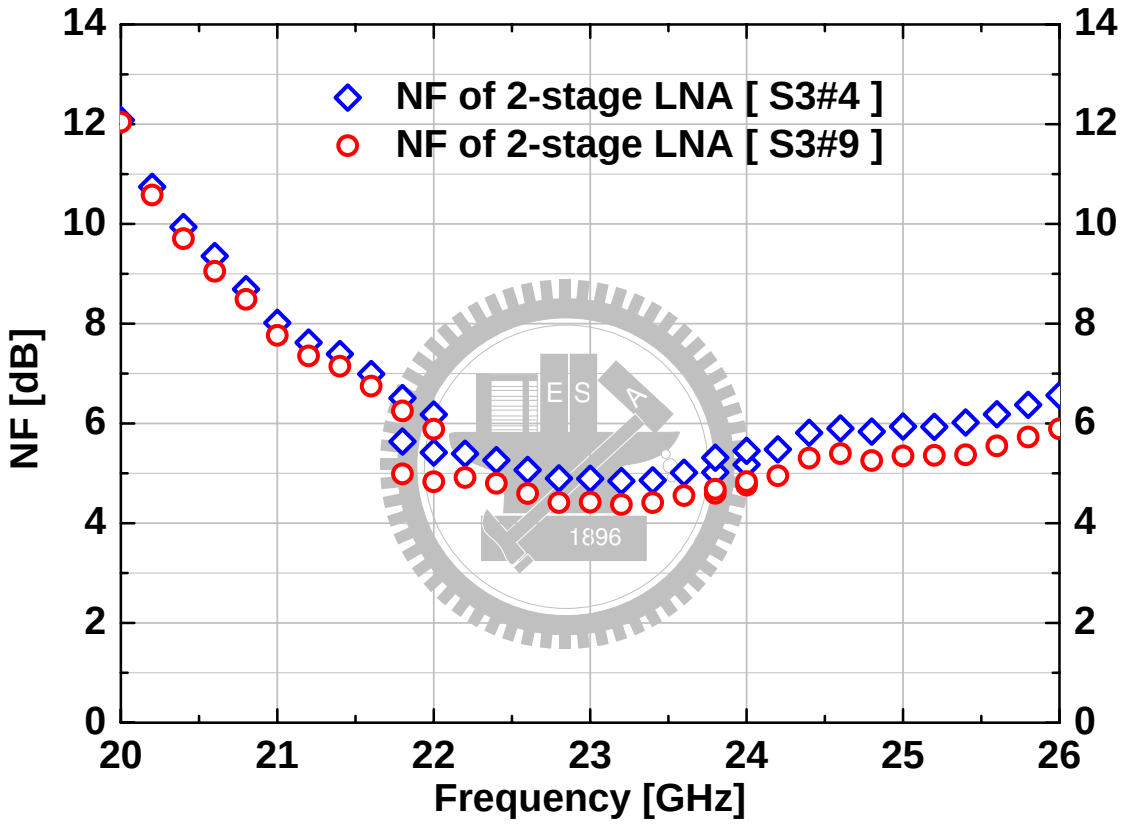
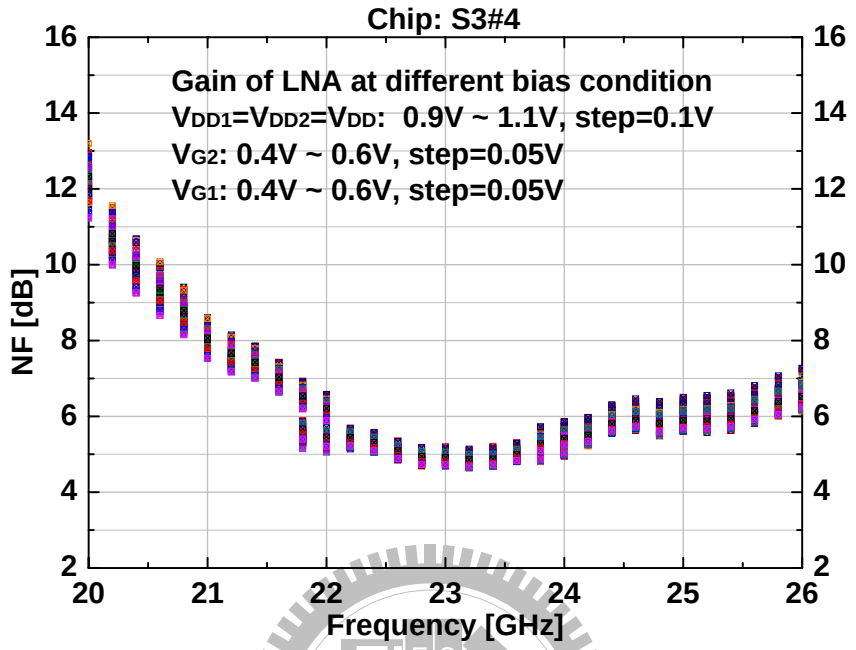
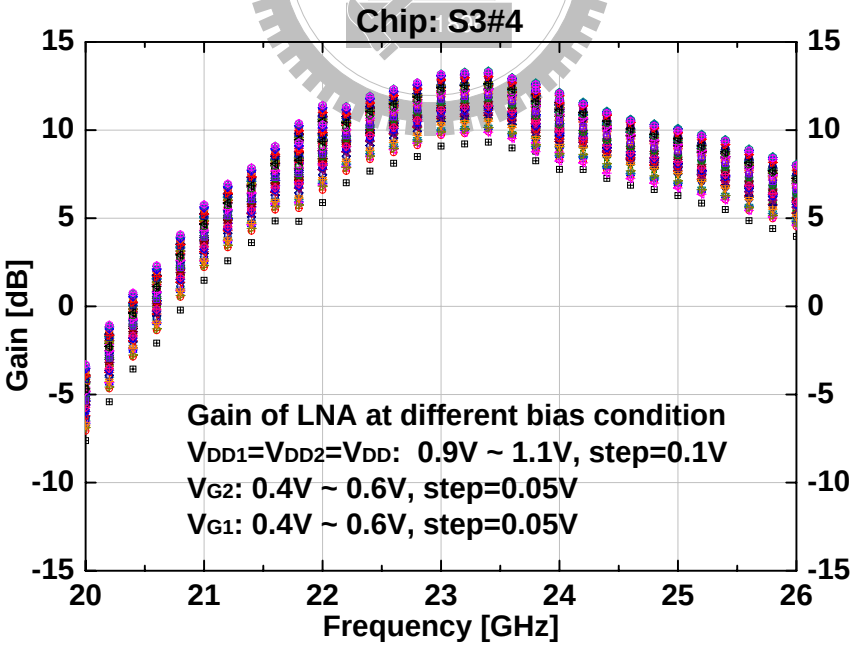


Figure 4.37 Measured NF of the two-stage cascaded cascode LNA of Chip S3#4 and Chip S3#9.

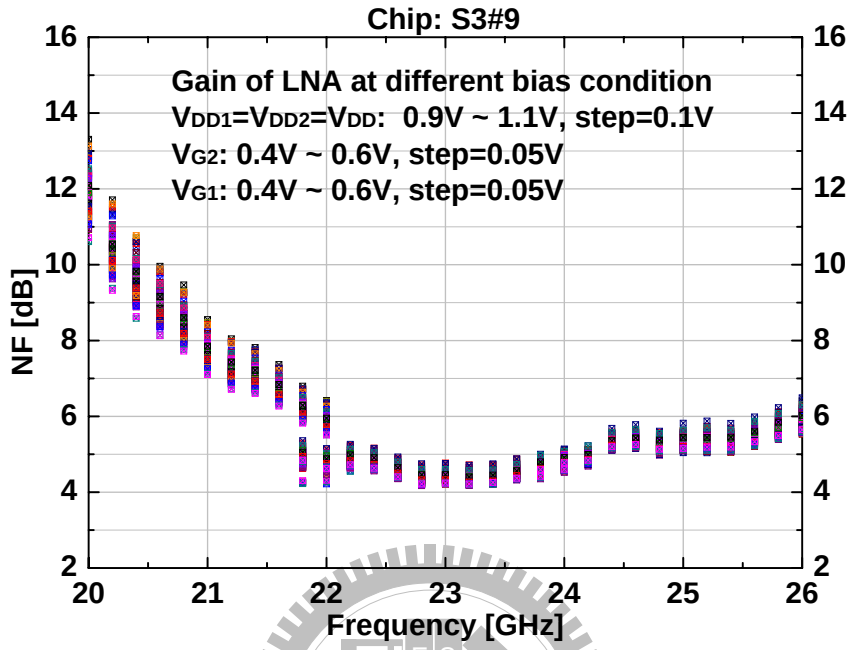


(a)

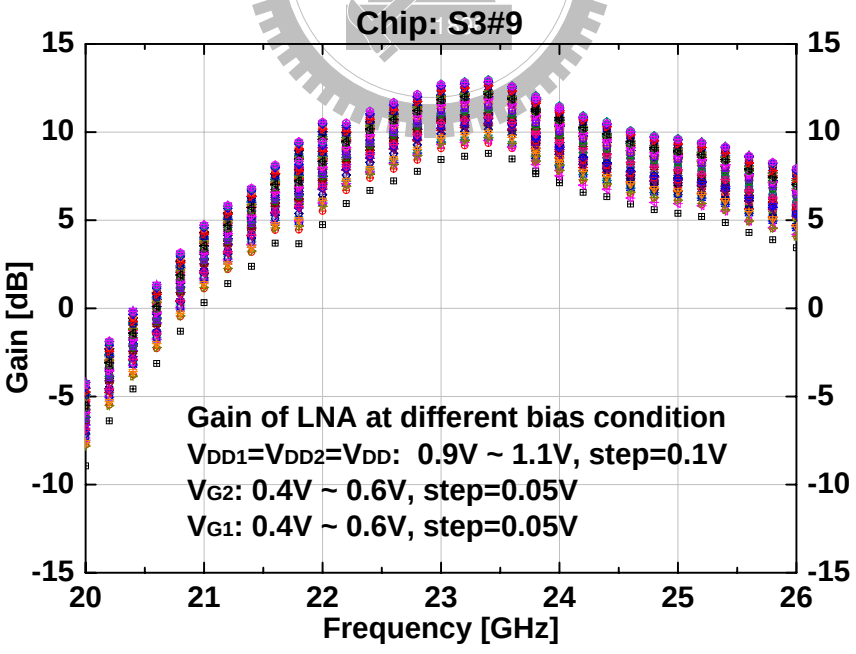


(b)

Figure 4.38 Measured NF and Gain of the two-stage cascaded cascode LNA with different bias conditions. (a) NF of Chip S3#4. (b) Gain of Chip S3#4. (c) NF of Chip S3#9. (d) Gain of Chip S3#9.



(c)



(d)

Figure 4.38 Measured NF and Gain of the two-stage cascaded cascode LNA with different bias conditions. (a) NF of Chip S3#4. (b) Gain of Chip S3#4. (c) NF of Chip S3#9. (d) Gain of Chip S3#9.

and 23.2 GHz, respectively. The two signals are with the same signal level of –30.3 dBm. It shows that the presented two-stage cascaded cascode LNA has a P_{IIP3} of –4.2 dBm.

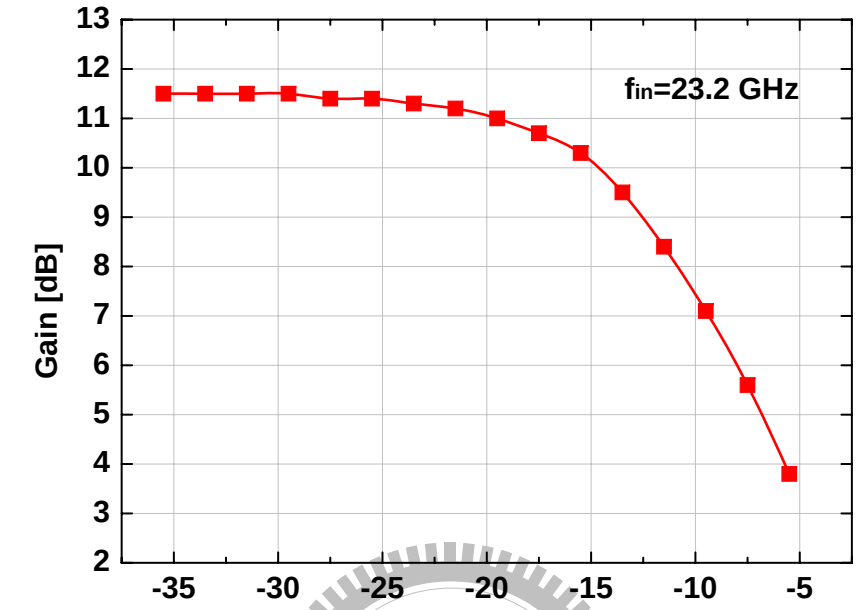
The comparisons of measured and simulated S-parameters of one-stage cascode LNA are shown in Fig. 4.42. The comparisons of measured and simulated S-parameters of two-stage cascaded cascode LNA are shown in Fig. 4.43. Moreover, the comparisons of measured and simulated NF performance of the designed two LNAs are shown in Fig. 4.44.

The difference between simulated and measured NF is because the preliminary version of 45-nm CMOS transistor models is used in the simulation. This transistor model is predicted from 90-nm CMOS spice model, and only the DC characteristics is verified. Moreover, the RF parasitic effects of the transistors are not modeled well, and no process design kits are provided. Different layout results in different parasitic effects. Due to these uncertainties, the simulated and measured results have some differences.

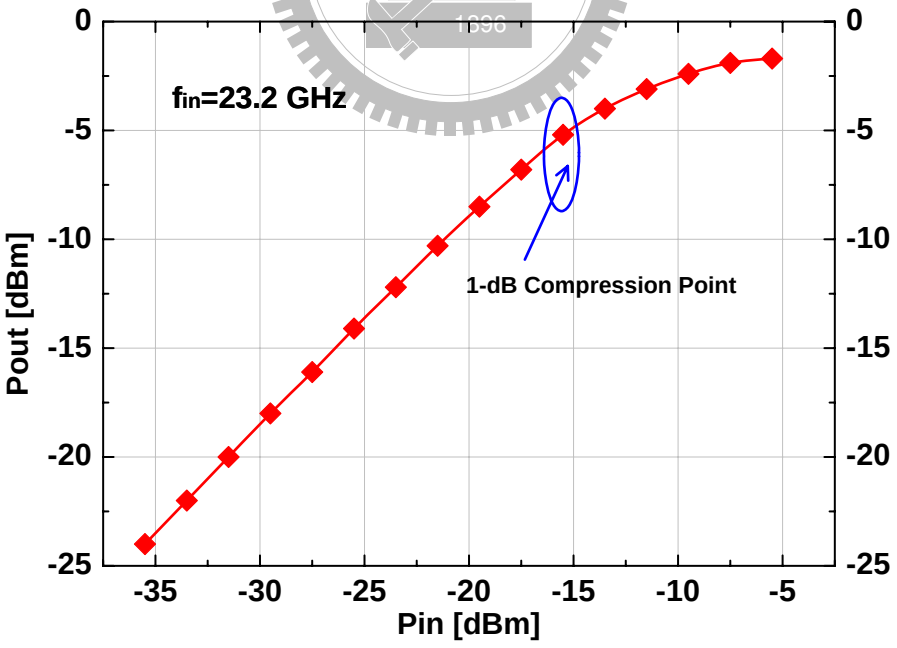
Besides, in the proposed two-stage LNA, the load of the second-stage is not designed well. L_{D2} should be larger than L_{S2} to provide the gain. Therefore, the gain of the two-stage LNA can be improved simply by increasing the value of L_{D2}.

The dc inputs of both one-stage and two-stage LNAs are protected with the power-clamp ESD diodes. Fig. 4.45 shows the test setup of the HBM ESD measurement. The HBM ESD tests are performed between the pad of V_{DD} and the pad of ground with both positive and negative testing voltages. As for the testing case of positive V_{DD}-to-V_{SS}, the measured leakage currents are shown in Fig. 4.46(a) and Fig. 4.46(b). As the ESD level below 3 kV, the $I-V$ curves are not changed too much. However, as the ESD level is increased to 3.5 kV, the $I-V$ curve has dramatically changed. This means fabricated power-clamp diode has the ESD protected level of 3 kV for positive V_{DD}-to-V_{SS}. As for the testing case of negative V_{DD}-to-V_{SS}, the measured leakage currents are shown in Fig. 4.46(c) and Fig. 4.46(d). As the ESD level below 6 kV, the $I-V$ curves are not changed too much. However, as the ESD level is increased to 6.5 kV, the $I-V$ curve has dramatically changed. This means fabricated power-clamp diode has the ESD protected level of 6 kV for negative V_{DD}-to-V_{SS}. The HBM ESD robustness of the fabricated power-clamp diodes are summarized in Table 5.5.

At the 2^{nd}-stage of the two-stage LNA, the performance of the inductor L_{d2} is not



(a)



(b)

Figure 4.39 Measured one-tone testing results of the two-stage cascaded cascode LNA.

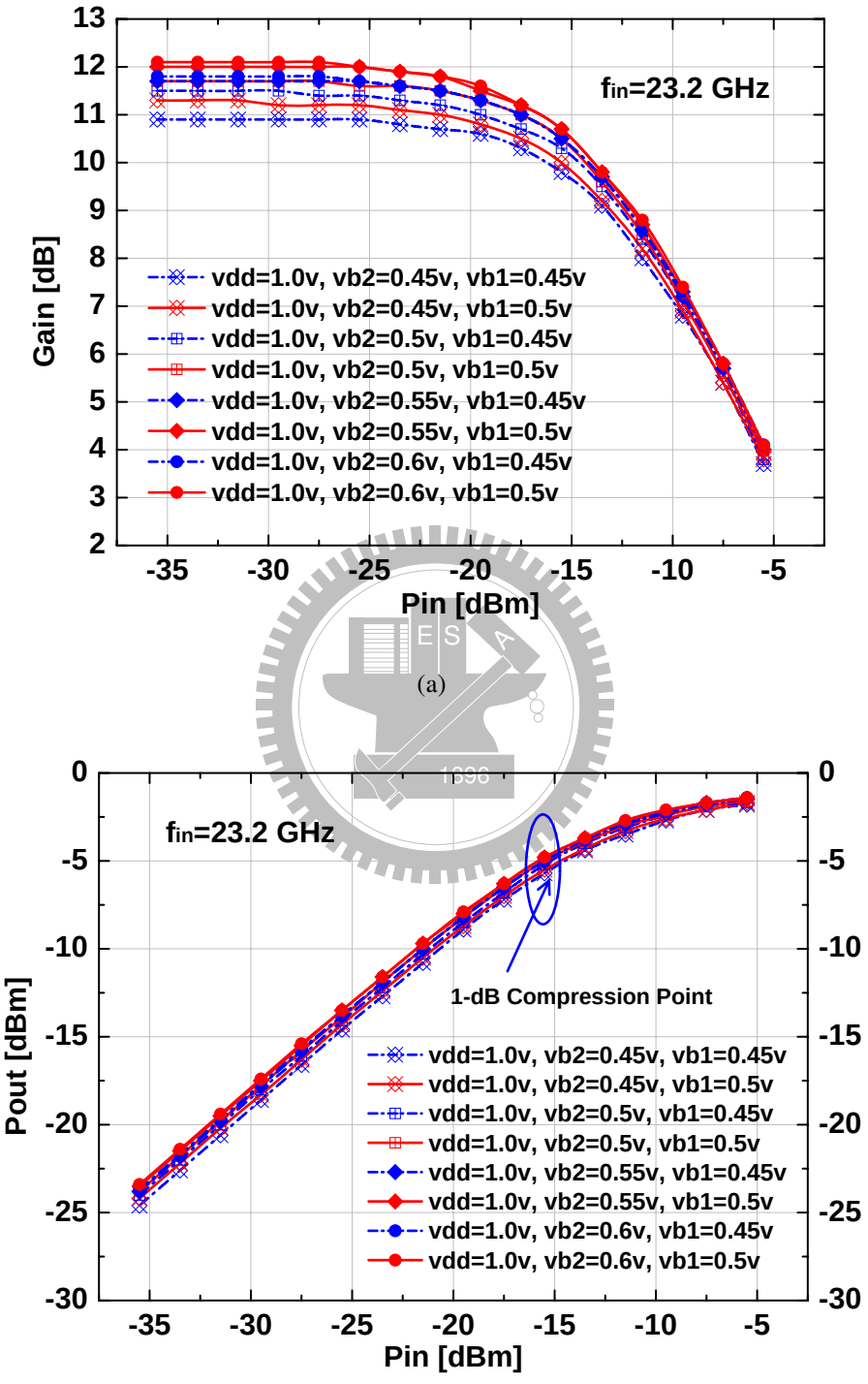


Figure 4.40 Measured one-tone testing results of the two-stage cascaded cascode LNA with different bias conditions.

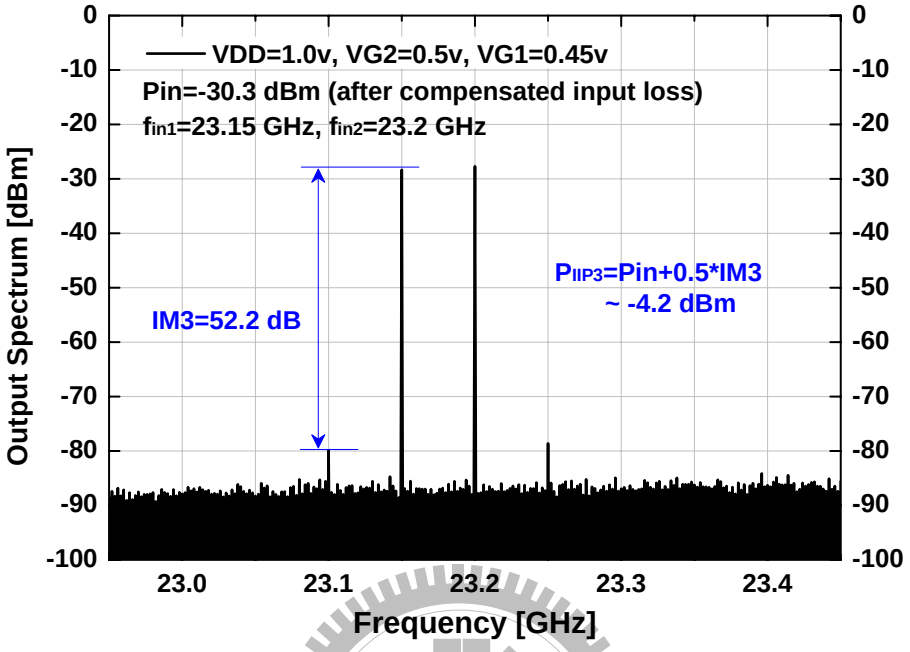


Figure 4.41 Measured two-tone testing results of the two-stage cascaded cascode LNA.

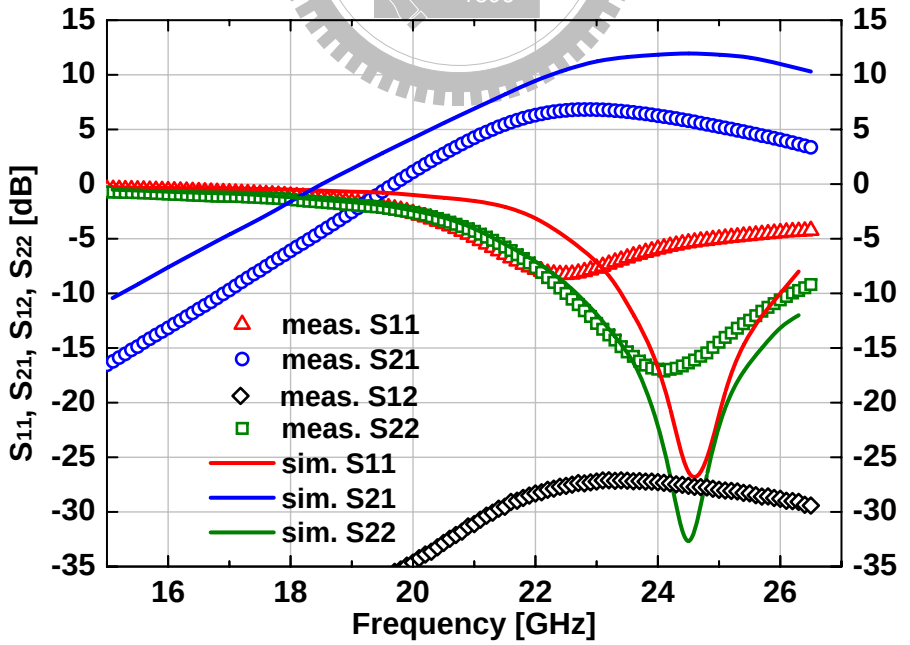


Figure 4.42 Measured and simulated S-parameters of one-stage cascode LNA.

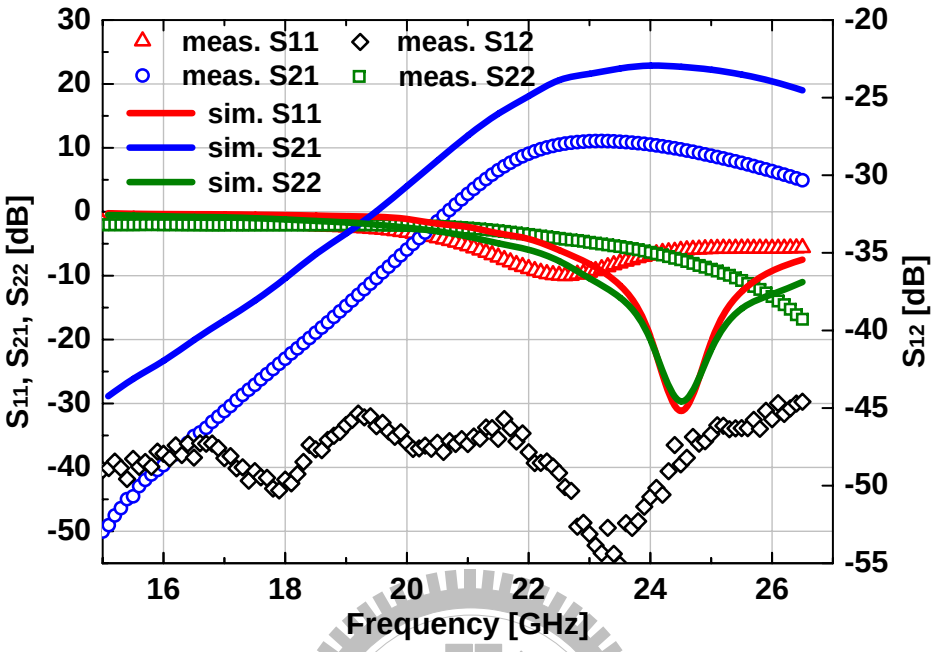


Figure 4.43 Measured and simulated S-parameters of two-stage cascaded cascode LNA.

good. It requires to be modified to a higher value to increase the gain of 2^{nd}-stage. At the operation frequency of K-Band, the on-chip transmission line effect is not noticeable. For the 2-stage LNA, it does not require to do the inter-stage matching to 50 Ohm. Without doing the inter-stage matching to 50 Ohm, the LNA is possible to push the gain higher. The noise contributed from the 2^{nd}-stage or the following stage can be suppressed by the high LNA gain. However, as the LNA is designed to operate at higher frequency, V-band or W-band, on-chip transmission line becomes remarkable. Inter-stage matching of the multi-stage LNA needs to be considered [189].

The measured results of the fabricated one-stage and two-stage 45-nm bulk-CMOS LNA are compared with those of published CMOS LNAs around 20 GHz in Table 5.6. As can be seen from Table 5.6, the fabricated one-stage LNA has good linearity performance as well as low power consumption. The LNAs in [143] and [145] have better linearity performance than these works at the cost of higher power consumption.

To characterize the performance of all bulk-CMOS LNAs around 20 GHz, the FOM

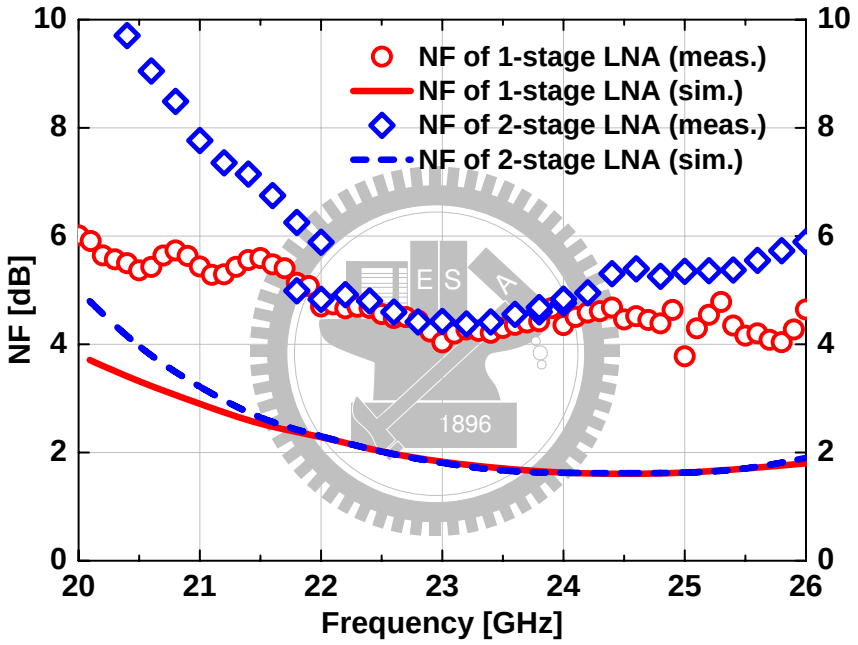


Figure 4.44 Measured and simulated NF of the presented one-stage and two-stage LNAs.

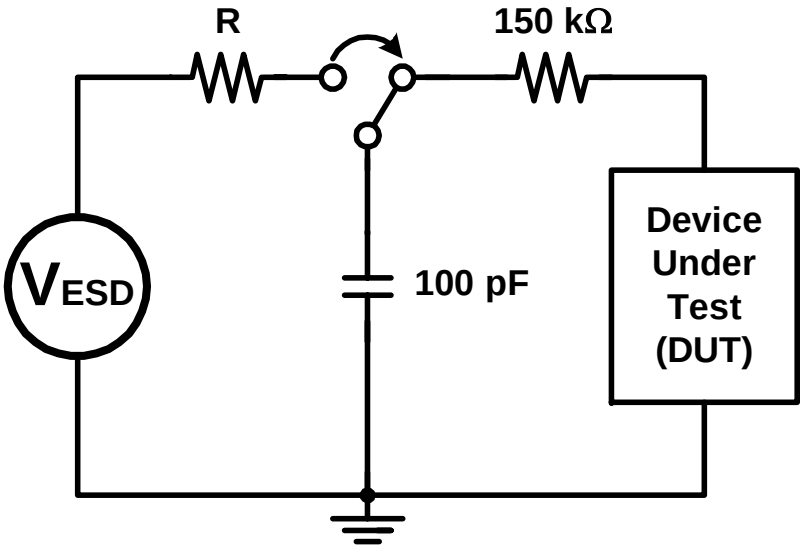


Figure 4.45 Environment setup of HBM ESD measurement.

defined in [194] has been used. It can be written as

$$FOM_{LNA} \equiv \frac{G \times IIP3 \times f_C}{(F-1) \times P} \tag{4.6}$$

where G represents the gain, $IIP3$ denotes the linearity, f_C is the operating frequency, F is the noise factor, and P is the power dissipation. In (4.6), G and F are in absolute values, P and $IIP3$ are in units of mW, and f_C is in the unit of GHz. The values of FOM_{LNA} are calculated for different LNAs and are presented in Table 5.6 and Fig. 4.47. As shown in Fig. 4.47, the fabricated 45-nm CMOS one-stage LNA has the highest FOM_{LNA} as compared with other published bulk-CMOS LNAs around 20 GHz. Furthermore, it is at present the first 45-nm planar bulk-CMOS LNA operated above 10 GHz.

In general, two-stage or multi-stage LNAs will have higher gain than one-stage LNA, but they sacrifices the linearity performance. From (4.6), the product of $G \times IIP3$ nearly keeps the same. However, two-stage or multi-stage LNA will have higher noise figure and consumes more consumption because of more devices used. Therefore, the FOM of two-stage or multi-stage LNA will be smaller than one-stage LNA.

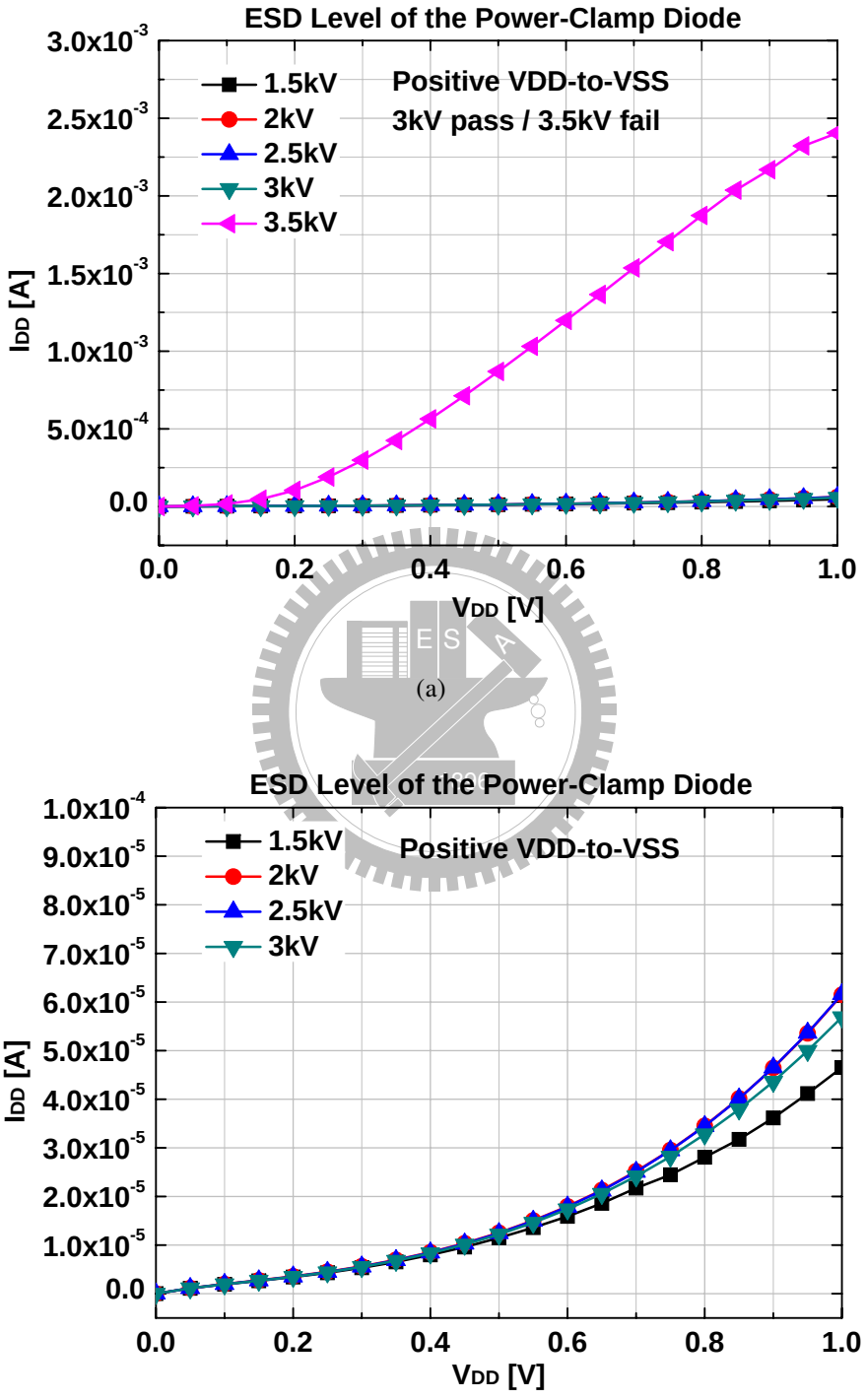
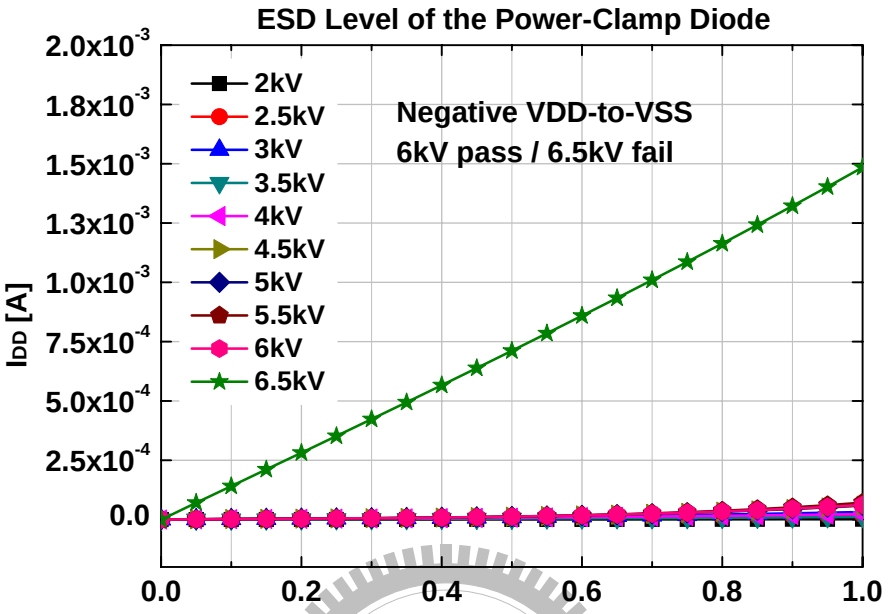
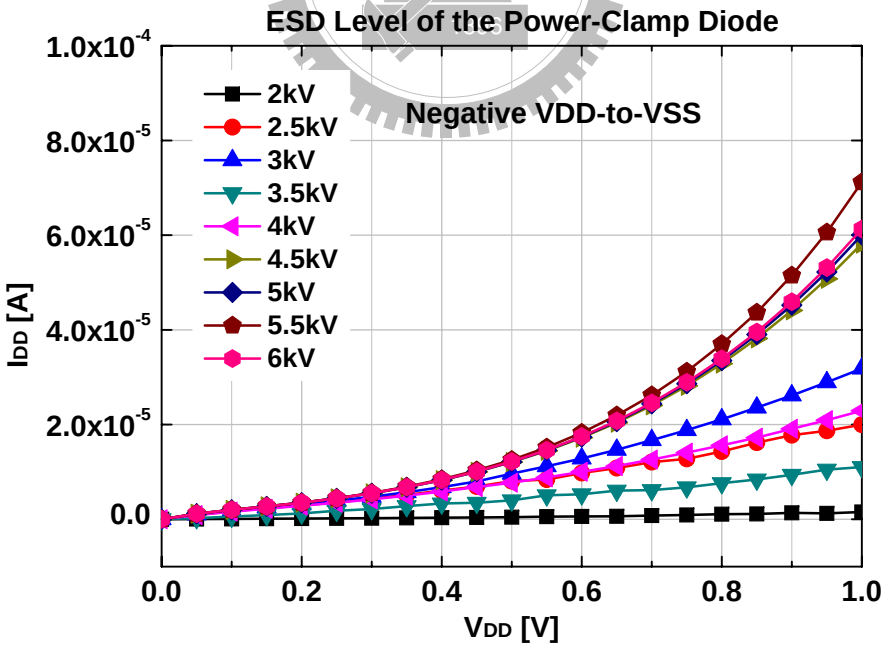


Figure 4.46 Measurement results of HBM ESD testing. (a) Positive V_{DD} to V_{SS}, (b) positive V_{DD} to V_{SS}, (c) negative V_{DD} to V_{SS}, and (d) negative V_{DD} to V_{SS}.



(c)



(d)

Figure 4.46 Measurement results of HBM ESD testing. (a) Positive V_{DD} to V_{SS}, (b) positive V_{DD} to V_{SS}, (c) negative V_{DD} to V_{SS}, and (d) negative V_{DD} to V_{SS} (*Con't*).

Table 4.5
HBM ESD ROBUSTNESS OF POWER-CLAMP STI DIODE

	Positive	Negative
V_{DD} to V_{SS}	3 kV	6 kV

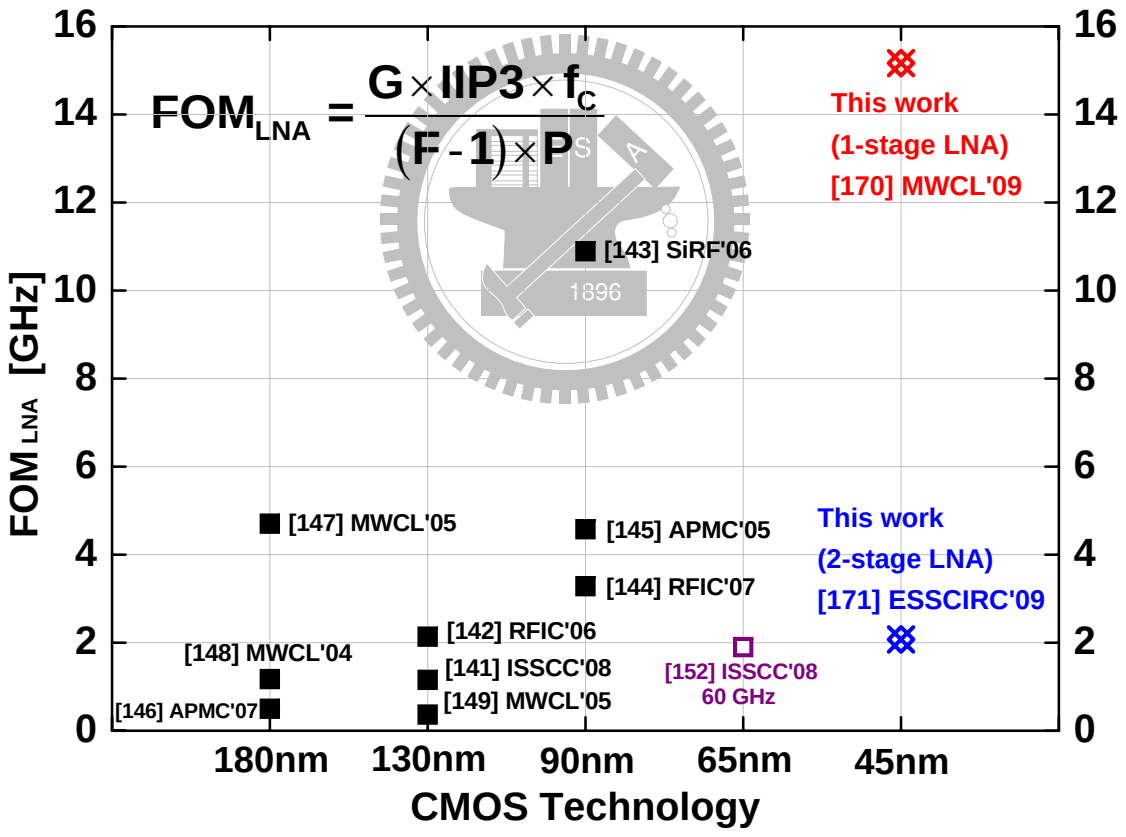


Figure 4.47 Comparisons with published works by FOM_{LNA}.

Table 4.6
PERFORMANCE COMPARISON WITH BULK-CMOS LNAS AROUND 20 GHZ

	Technology	Freq.	Gain	NF	IP_{-1dB}	P_{IIP3}	Supply	Power	Area	FOM_{LNA}	Topology †
Unit	[nm]	[GHz]	[dB]	[dB]	[dBm]	[dBm]	[V]	[mW]	[mm^2]	[GHz]	–
This work (1-stage)	45 nm	23	7.1	4	–9.5	+2.25	1	3.6	0.81	15.2	1-stage cascode
This work (2-stage)	45 nm	23.4	11.6	4.4	–9.5	–16	1	9.3	1.43	2.1	2-stage, cascode+cascode
[141] ISSCC 2008	130 nm	18	22.4	4.1	–	–5.6	1.5	36	0.23	1.2	2-stage, pseudo differential
[142] RFIC 2006	130 nm	26.2	8.4	4.8	–	–13	1	0.8	0.16	2.1	1-stage cascode
[143] SiRF 2006	90 nm	20	8.4	3.1	–	+4.8	1.4	14	0.56	10.9	1-stage cascode
[144] RFIC 2007	90 nm	28.5	20	2.9	–17	–7.5	1	16.25	0.67	3.3	2-stage, CS+Cascode
[145] APMC 2005	90 nm	20	8	5.3	–	+3.8	0.66	11	0.84	4.6	2-stage, CS+CS
[146] APMC 2007	180 nm	25.8	10	4.84	–17.8	–5	1	25.6	0.55	0.5	3-stage, CS+CS+Cascode ††
[147] MWCL 2004	180 nm	24	13.1	3.9	–12.2	–0.54	1	14	0.34	4.7	2-stage, CS+CS
[148] MWCL 2004	180 nm	23.7	12.86	5.6	–11.1	+0.24	1.8	54	0.73	1.2	3-stage, CS+CS+CS
[149] MWCL 2005	130 nm	20	9	5.5	–11	–4	1.2	24	0.8	0.4	2-stage, Cascode ††
[150] ESSCIRC 2005	90 nm	24	7.2	3.5	–	–	1	10.6	2.1	–	1-stage, CS, WLP
[151] RFIC 2008	180 nm	24	12.8	3.3	–	–	1	8	0.55	–	2-stage, CS+CS
[152] ISSCC 2008	65 nm	60	22.6	6.1	–16	–6 ‡	1.2	35	0.21	1.9	3-stage, CS+Cascode+CS ††

† CS: common source.
†† Differential configuration.
‡ Estimated from IP_{-1dB}. $P_{IIP3} \approx IP_{-1dB} + 10$.

4.4 Summary

Two K-band LNAs: a 23-GHz one-stage cascode LNA and a 23.4-GHz two-stage cascaded cascode LNA have been successfully designed and implemented in the IMEC 45-nm planar bulk-CMOS technology. These two LNAs are believed to be the first 45-nm CMOS LNA above 10 GHz and are with silicon-proved. With the advantage of IMEC WLP technology, high-Q above-IC inductors and low-loss microstrip lines are applied into the fabricated LNAs. Furthermore, the power-clamp diodes are used to protected dc inputs.

From the measurement results, the designed one-stage 45-nm bulk-CMOS LNA with high-Q above-IC inductors exhibits a gain of 7.1 dB and a NF of 4 dB at the center frequency of 23 GHz. This LNA has a quite good linearity performance of an IP_{-1dB} of –9.5 dBm, and a P_{IIP3} of +2.25 dBm. The power consumption of the one-stage LNA is 3.6 mW from 1-V supply voltage. The chip area of this one-stage LNA is 0.81 mm^2.

Furthermore, the designed two-stage 45-nm bulk-CMOS LNA with high-Q above-IC inductors exhibits a gain of 11.6 dB and a NF of 4.4 dB at the center frequency of 23.4 GHz. This two-stage LNA also has a good linearity performance of an IP_{-1dB} of –16 dBm, and a P_{IIP3} of –4.2 dBm. The power consumption of the one-stage LNA is 9.3 mW from 1-V supply voltage. The chip area of this one-stage LNA is 1.43 mm^2.

Although the conventional LNA is used, the performance is dramatically improved due to the very high f_T of the 45-nm transistors and very high quality WLP above-IC inductors. The experimental results show that the presented one-stage LNA in IMEC 45-nm planar bulk-CMOS with high-Q above-IC inductors achieve the state-of-the-art as compared to other K-band CMOS LNAs. Moreover, the two-stage LNA has comparable performance. It is also demonstrated that the IMEC 45-nm planar bulk-CMOS technology has great potential for the design of high performance high frequency RF circuits. IMEC WLP technology can successfully provide high-Q above-IC inductors and ultra low-loss microstrip lines, and this technology has the advantage of low cost.

Chapter 5

Conclusion

5.1 Major Contributions of This Dissertation

In this dissertation, the design methodologies and circuit implementation techniques of a current-mode direct-conversion receiver front-end and a current-mode direct-conversion transmitter front-end have been proposed and analyzed. Moreover, two LNAs for the benchmark circuits of IMEC 45-nm planar bulk-CMOS technology have been presented.

Firstly, a low-voltage low-power CMOS 24-GHz (K-band) direct-conversion receiver front-end has been proposed, analyzed, and implemented in TSMC 0.13-μm 1P8M CMOS technology. The CMOS current-mode design techniques for low-voltage, low-power, and high-frequency circuits are developed and applied to the implementation of key building blocks of the proposed K-band direct-conversion receiver. The proposed receiver is of single-balanced structure and integrated with a LNA and a down-conversion mixer. A current-mode LNA by cascading two current-mirror amplifiers is used to amplify the received RF signal. A current-mode mixer which is composed of a current-summing circuit and a current-squaring circuit is used to realize the frequency mixing of RF and LO current signals. With the advantages of current-mode operation, the proposed current-mode K-band receiver is successfully operated with low power consumption of 27.8 mW under the condition that the low supply voltage of LNA is 0.8 V and the low supply voltage of mixer is 1.2 V. The measurement results have shown that the proposed current-mode design techniques have the capability of designing low-voltage, low-power, and high-

frequency RF receiver front-ends in the advanced nanometer CMOS technologies.

Secondly, a low-voltage low-power CMOS 22-GHz (K-band) direct-conversion transmitter front-end has been proposed, analyzed, and implemented in TSMC 0.13-μm 1P8M CMOS technology. The CMOS current-mode design techniques for low-voltage, low-power, and high-frequency RF circuits are developed. The proposed current-mode K-band direct-conversion transmitter front-end is of double-balanced structure and composed of an up-conversion mixer, a VCO, a transformer-based VCO buffer/repeater, and a baseband current buffer/repeater. The current-mode up-conversion mixer which is composed of four current-squaring circuits is used to realize the frequency mixing of baseband and LO current signals. On-chip transformer is used as the inductive load of the current-mode up-conversion mixer and to implement the subtraction of high-frequency and wide-bandwidth current signals. The transformer-based VCO buffer/repeater is adopted to provide two-pair differential LO current signals for the mixer. Moreover, the baseband current buffer/repeater is adopted to provide two-pair differential IF current signals for the mixer. The current-mode circuit has the advantage of easily dealing with the summation of current signals by wire connection. Without additional amplifiers to do summation of current signals, power dissipation can be further reduced. With the advantages of current-mode operation, the proposed current-mode K-band transmitter is successfully operated with low power consumption of only 11.7 mW in low supply voltage of 1 V. In addition to low-power consumption, the proposed current-mode up-conversion mixer has the advantages of requiring very small LO signal power of –4 –12 dBm to achieve the gain of –5 –14 dB. The total power consumption of the integrated transmitter is only 11.7 mW under the low supply voltage of 1 V. Through the experimental results, it reveals that the proposed current-mode design techniques have the capability of designing low-voltage, low-power, and high-frequency RF transmitter front-ends in the advanced nanometer CMOS technologies.

Finally, two 24-GHz (K-band) LNAs have been proposed, analyzed, and implemented in IMEC 45-nm 1P5M planar bulk-CMOS technology. The cascode device is adopted for the LNA design because of its reduced Miller Effect. The benefit of high gain and excellent reverse isolation from cascode structure can be achieved. A one-stage cascode LNA and a two-stage cascaded cascode LNA have been designed for the benchmark circuits

of the advanced 45-nm CMOS process. Moreover, the low-cost and high-performance IMEC WLP technology is adopted to obtain high-Q above-IC inductors and ultra low-loss microstrip lines. The performances of 45-nm bulk-CMOS LNA have been verified through on-wafer measurements of the fabricated chip. The presented 23-GHz one-stage 45-nm bulk-CMOS LNA exhibits the gain of 7.1 dB, the NF of 4 dB, the P_{IIP3} 0f +2.25 dBm, and very small power dissipation of only 3.6 mW. As compared to prior works, it has been shown that the proposed one-stage LNA achieves the highest FOM_{LNA}. The proposed 23.4-GHz two-stage 45-nm bulk-CMOS LNA exhibits the gain of 11.6 dB, the NF of 4.4 dB, the P_{IIP3} of –4.2 dBm, and the power dissipation of 9.3 mW. Although the performance of the proposed two-stage LNA is not as good as the presented one-stage LNA in terms of FOM_{LNA}, the two-stage LNA still has the comparable performances to other work. Moreover, it is at present the first two 45-nm planar bulk-CMOS LNAs that is operated above 10 GHz.

In summary, the continuous scaling of CMOS technology into nanometer or even deca-nanometer nodes, 45 nm and sub-45 nm for examples, has dramatically improved the f_T and f_{MAX} of MOS transistors. It becomes feasible to design high-performance millimeter-wave RF circuits in advanced CMOS technologies. Furthermore, the supply voltage is reduced accordingly along with the scaling of CMOS technologies such that voltage headroom, effective overdrive voltage, and dynamic range of conventional voltage-mode RF circuits are not sufficient enough. It has been successfully demonstrated that the current-mode circuit design techniques proposed in this dissertation are suitable for RF circuits operated in low supply voltage and low-power dissipation. Besides, the direct-conversion architectures of receiver and transmitter front-ends have the advantage of high integration capability. Consequently, it becomes quite feasible to design low-voltage, low-power, high-frequency, high-performance, and high-integration transmitter and receiver front-ends in current-mode design techniques by using advanced CMOS technologies. It can also be easily integrated with the baseband signal processing VLSI.

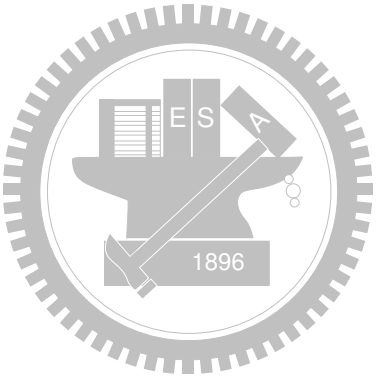
5.2 Future Work

In the implementation of current-mode CMOS K-band receiver front-end circuits, a single-ended LNA and a single-balanced mixer is used. In the future work, differential current-mode LNA and double-balanced current-mode mixer can be adopted to reduce even-order harmonics and inter-modulations and to improve the immunity to common-mode noise. An on-chip transformer before the differential LNA can also be implemented at the same time to provide single-ended to differential transformation. Moreover, the implemented receiver is used to down-converted the RF signal from 24 GHz to the IF frequency at 5 GHz. To prevent from paying much effort that uses a very high speed ADC for digitizing the 5-GHz signals, additional frequency conversion stage that is used to down-convert the 5-GHz signals to the baseband is to be designed. The double-quadrature 5-GHz receiver that exhibits excellent image rejection is a good choice. Besides, the calibration technique of phases and gains of the mixers at I- and Q- paths can be adopted to overcome the process variations and prevent from the degradation of image rejection. It may be possible to apply the proposed CMOS current-mode RF circuit design techniques to much higher operating frequency band, 60-GHz (V-Band) for example, in the advanced nanometer CMOS technologies.

In the implementation of current-mode CMOS K-band transmitter front-end circuits, a double-balanced up-conversion mixer, a differential VCO, a VCO buffer/repeater, and a fully-balanced baseband current buffer/repeater are used. Although the double-balanced up-conversion mixer is used, the LO suppression ability is still not enough. In the future work, much careful layout floor-plan of the differential LO and baseband signal paths should be well considered to improve this. Besides, the layout of the mixer cores should use common centroid layout floor-plan to decrease the cross-chip gradient variations. In addition to this, the calibration technique of phases and gains of the current-squaring circuits can be incorporated. In the calibration phase, the output of the up-conversion mixer is down-converted to DC by mixing with the LO signal through a down-conversion mixer, and is passed through a LPF. Through the negative feedback control, the residue of DC extracted through the LPF can be used to perform differential tuning of the biasing currents of the current-squaring circuits to further improve the LO suppression capability.

Furthermore, the single-sideband (SSB) transmission should be adopted to employ the spectrum efficiently. For this purpose, the quadrature mixing is to be adopted to design the transmitter front-end. The K-band CMOS power amplifier can also be designed and integrated to provide high output power of the transmitter. Finally, it may be possible to apply the proposed CMOS current-mode RF circuit design techniques to 60-GHz (V-Band) transmitter front-end circuits in the advanced nanometer CMOS technologies.

In the implementation of 45-nm planar bulk-CMOS 24-GHz (K-Band) LNAs, only the preliminary models for 45-nm MOS transistors are used. Different transistor layouts result in different parasitic, and consequently influence the performance of the LNA, including matching characteristics of noise and impedance. The operation frequency will be also affected. Tuning the value of the capacitors in the LC loads can be incorporated to alleviate the process variations. By the frequency tuning concept, two resonated frequencies of the two-stage LNA are possible to be tuned to the same frequency such that its gain is possible to be further improved. Besides, to improve the immunity to common-mode noise, the LNA with differential structure can be adopted. The cascode devices can be laid out properly to minimize the parasitic capacitance and so that the signal losses are reduced and the NF is improved. Moreover, the inter-stage matching of the two-stage LNA will be removed to gain higher performance of the proposed CMOS K-band LNA. The 45-nm planar bulk-CMOS process can be used design 60-GHz (V-Band) or W-band LNAs, PAs, and Mixers for benchmark. Furthermore, designing the LNAs, PAs, and Mixers in 24 GHz or 60 GHz in 45-nm or sub-45-nm FinFET devices is also valuable.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Appendix A

In the deep sub-micron CMOS technologies, the relationship between drain current i_{DS} and the gate overdrive voltage $v_{OV} = (v_{GS} - V_{th})$ of CMOS devices in the saturation region is not exactly square due to short channel effects, and the drain current i_{DS} is approximated as [163], [164]

$$i_{DS} \approx \frac{1}{2} k_n \frac{W}{L} \frac{\mu_n}{(1 + \theta v_{OV})} \frac{v_{OV}^2}{\left(1 + \frac{v_{OV}}{E_C L}\right)} (1 + \lambda v_{DS}) \tag{A.1}$$

where E_C is the critical value of the horizontal electric field, θ is inversely proportional to the oxide thickness, and the coefficient λ models the effect of the channel length modulation which is related to v_{DS}. If the transistor in the saturation region is operated with small v_{OV} such that $v_{OV} \ll \theta^{-1}$ and $v_{OV} \ll E_C L$, (A.1) can be simplified approximately as

$$i_{DS} \approx \frac{1}{2} k_n \frac{W}{L} v_{OV}^2 (1 + \lambda v_{DS}) \tag{A.2}$$

The current-squaring circuit of Figure A.1 is proposed in Chapter 3 where the MOS transistors M_{SQ1} and M_{SQ3} are well matched with the same channel width/length (W/L). The drain-to-source voltages of M_{SQ1} and M_{SQ3} are different as the biasing voltage V_G is varied. As a result, the channel length modulation effect should be considered. In Figure A.1, If $\delta = (v_{DS,M_{SQ3}} - v_{DS,M_{SQ1}})/2$ and $\sigma = (v_{DS,M_{SQ3}} + v_{DS,M_{SQ1}})/2 = V_{DD}/2$ are assumed, $v_{DS,M_{SQ3}} = (\sigma + \delta) = (V_{DD}/2 + \delta)$ and $v_{DS,M_{SQ3}} = (\sigma - \delta) = (V_{DD}/2 - \delta)$. The detailed derivations of the relationship between i_{in} and i_{OUT} are shown as the following.

$$i_1 = K(v_A - V_{th})^2 [1 + (\sigma - \delta)] \tag{A.3}$$

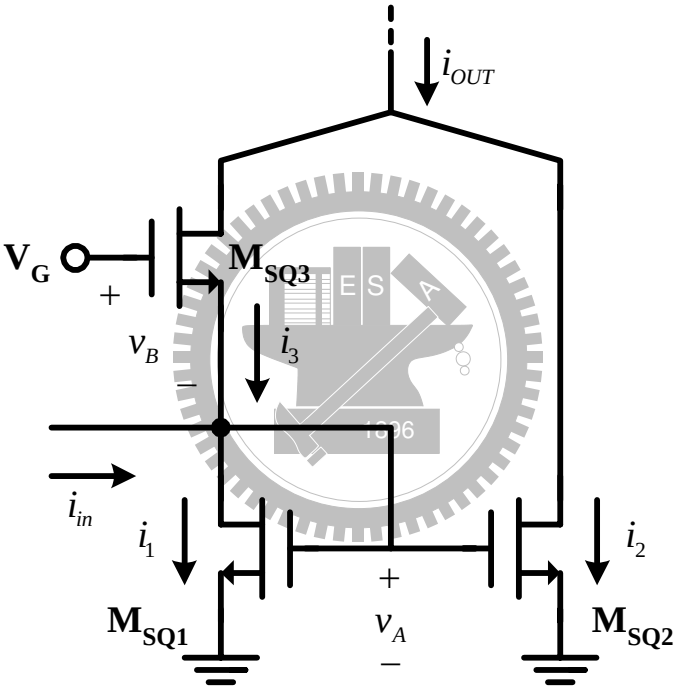


Figure A.1 The current-squaring circuit in down-conversion mixer.

$$i_2 = K\left(v_A - V_{th}\right)^2\left(1 + \lambda V_{DD}\right) = K\left(v_A - V_{th}\right)^2\left(1 + 2\sigma\lambda\right) \tag{A.4}$$

$$i_3 = K\left(v_B - V_{th}\right)^2\left[1 + (\sigma + \delta)\right] \tag{A.5}$$

where

$$K = \frac{1}{2}k_n\frac{W}{L} \tag{A.6}$$

$$v_A = v_{GS,M_{SQ1}}$$

$$v_B = v_{GS,M_{SQ3}}$$

Define

$$I_B = \frac{1}{2}K\left(V_G - 2V_{th}\right)^2 \tag{A.7}$$

From Figure A.1,

$$i_{in} = i_1 - i_3 \tag{A.8}$$

$$i_{OUT} = i_2 + i_3$$

$$i_{in} + i_{OUT} = i_1 + i_2 \tag{A.9}$$

From (A.3), (A.5), and (A.8),

$$i_{in} = K\left(v_A - V_{th}\right)^2\left[1 + \lambda\left(\sigma - \delta\right)\right] - K\left(v_B - V_{th}\right)^2\left[1 + \lambda\left(\sigma + \delta\right)\right]$$

$$\begin{aligned}\frac{i_{in}}{K} &= (v_A + v_B)(v_A - v_B)(1 + \sigma\lambda) - \delta\lambda\left[(v_A + v_B)^2 - 2v_Av_B\right] \\ &\quad -V_{th}(v_A - v_B)(2 + 2\sigma\lambda) + 2V_{th}\delta\lambda(v_A + v_B - V_{th})\end{aligned} \tag{A.10}$$

Due to

$$V_G = v_A + v_B \tag{A.11}$$

(A.10) can be re-arranged by

$$\frac{i_{in}}{K} = -\delta\lambda(V_G^2 - 2v_Av_B) + (v_A - v_B)(V_G - 2V_{th})(1 + \sigma\lambda) + 2V_{th}\delta\lambda(V_G - V_{th}) \tag{A.12}$$

From (A.3), (A.4), and (A.9),

$$\frac{i_{in} + i_{OUT}}{K} = (v_A + V_{th})^2(2 + 3\sigma\lambda - \delta\lambda) \tag{A.13}$$

From (A.13),

$$v_A = V_{th} + \sqrt{\frac{i_{in} + i_{OUT}}{K(2 + 3\sigma\lambda - \delta\lambda)}}$$

$$v_A = V_{th} + \frac{C}{2}\sqrt{i_{in} + i_{OUT}} \tag{A.14}$$

where

$$C = \frac{2}{\sqrt{K(2 + 3\sigma\lambda - \delta\lambda)}} \tag{A.15}$$

Therefore,

$$C^2 = \frac{4}{K(2 + 3\sigma\lambda)\left(1 - \frac{\delta\lambda}{2 + 3\sigma\lambda}\right)}$$

Because

$$\frac{\delta\lambda}{2 + 3\sigma\lambda} \ll 1 \tag{A.16}$$

$$C^2 \approx \frac{4}{K(2 + 3\sigma\lambda)}\left(1 + \frac{\delta\lambda}{2 + 3\sigma\lambda}\right) \approx \frac{4}{K(2 + 3\sigma\lambda)} \tag{A.17}$$

Consequently,

$$\delta\lambda C^2 = \frac{4\delta\lambda}{K(2 + 3\sigma\lambda)} \tag{A.18}$$

From (A.11) and (A.14),

$$v_B = V_G - \left(V_{th} + \frac{C}{2}\sqrt{i_{in} + i_{OUT}}\right) \tag{A.19}$$

From (A.14) and (A.19),

$$v_A - v_B = C\sqrt{i_{in} + i_{OUT}} - (V_G - 2V_{th}) \tag{A.20}$$

From (A.11), (A.14), and (A.15),

$$v_A v_B = v_A(V_G - v_A) = V_G v_A - v_A^2$$

$$v_A v_B = V_G\left(V_{th} + \frac{C}{2}\sqrt{i_{in} + i_{OUT}}\right) - \left(V_{th} + \frac{C}{2}\sqrt{i_{in} + i_{OUT}}\right)^2 \tag{A.21}$$

Substitute (A.20) and (A.21) into (A.12), (A.12) can be expressed as

$$Di_{in} + Ei_{OUT} + F\sqrt{i_{in} + i_{OUT}} + G = 0 \tag{A.22}$$

where

$$D = -\left(\frac{1}{K} + \frac{\delta\lambda C^2}{2}\right) \approx -\frac{1}{K}\left(1 + \frac{2\delta\lambda}{2 + 3\sigma\lambda}\right) \tag{A.23}$$

$$E = -\frac{\delta\lambda C^2}{2} \approx -\frac{2\delta\lambda}{K(2+3\sigma\lambda)} \tag{A.24}$$

$$F = C(V_G - 2V_{th})(1+\sigma\lambda+\delta\lambda) \approx C(V_G - 2V_{th})(1+\sigma\lambda) \tag{A.25}$$

$$G = -(V_G - 2V_{th})^2(1+\sigma\lambda+\delta\lambda) \tag{A.26}$$

From (A.22),

$$Di_{in} + Ei_{OUT} + G = -F\sqrt{i_{in} + i_{OUT}} \tag{A.27}$$

Square both sides of (A.27), we get

$$D^2 i_{in}^2 + E^2 i_{OUT}^2 + G^2 + 2DEi_{in}i_{OUT} + 2DGi_{in} + 2EGi_{OUT} = F^2(i_{in} + i_{OUT}) \tag{A.28}$$

From (A.16) and (A.22),

$$D^2 \approx \frac{1}{K^2}\left[1 + \frac{2\delta\lambda}{2+3\sigma\lambda}\right]^2 \approx \frac{1}{K^2}\left[1 + \frac{4\delta\lambda}{2+3\sigma\lambda}\right] \tag{A.29}$$

From (A.24),

$$E^2 \approx \left[\frac{2\delta\lambda}{K(2+3\sigma\lambda)}\right]^2 \longrightarrow 0 \tag{A.30}$$

From (A.16), (A.23) and (A.24),

$$DE \approx \frac{2\delta\lambda}{K^2(2+3\sigma\lambda)} \longrightarrow 0 \tag{A.31}$$

From (A.26),

$$G^2 = (V_G - 2V_{th})^4(1+\sigma\lambda+\delta\lambda)^2 \tag{A.32}$$

From (A.23) and (A.26),

$$DG \approx \frac{(V_G - 2V_{th})^2}{K}\left[(1+\sigma\lambda+\delta\lambda) + \delta\lambda\left(\frac{2+2\sigma\lambda}{2+3\sigma\lambda}\right)\right]$$

$$DG \approx \frac{(V_G - 2V_{th})^2}{K}\left[(1+\sigma\lambda) + \delta\lambda\left(\frac{4+5\sigma\lambda}{2+3\sigma\lambda}\right)\right] \tag{A.33}$$

From (A.24) and (A.26),

$$EG \approx \frac{2(V_G - 2V_{th})^2}{K}\frac{\delta\lambda(1+\sigma\lambda+\delta\lambda)}{2+3\sigma\lambda} \tag{A.34}$$

From (A.17) and (A.25),

$$F^2 \approx \frac{4(V_G - 2V_{th})^2}{K}\frac{(1+\sigma\lambda)^2}{(2+3\sigma\lambda)} \tag{A.35}$$

Because $E^2 \to 0$ and $DE \to 0$, (A.28) can be simplified as

$$D^2 i_{in}^2 + G^2 + 2DGi_{in} + 2EGi_{OUT} = F^2(i_{in} + i_{OUT})$$

$$\left(F^2 - 2EG\right) i_{OUT} = D^2 i_{in}^2 + \left(2DG - F^2\right) + G^2$$

$$i_{OUT} = \left(\frac{D^2}{F^2 - 2EG}\right) i_{in}^2 + \left(\frac{2DG - F^2}{F^2 - 2EG}\right) i_{in} + \left(\frac{G^2}{F^2 - 2EG}\right) \tag{A.36}$$

From (A.34) and (A.35),

$$F^2 - 2EG \approx \frac{4(V_G - 2V_{th})^2}{K} \left[\frac{(1+\sigma\lambda)^2 - \delta\lambda(1+\sigma\lambda+\delta\lambda)}{2+3\sigma\lambda}\right] \tag{A.37}$$

From (A.33) and (A.35),

$$2DG - F^2 \approx \frac{2(V_G - 2V_{th})^2}{K} \left[\frac{\delta\lambda(4+5\sigma\lambda) + \sigma\lambda(1+\sigma\lambda)}{2+3\sigma\lambda}\right] \tag{A.38}$$

Substitute (A.7), (A.29), (A.32), (A.37), and (A.38) into (A.36),

$$\begin{aligned} i_{OUT} \;=\; & \left[\frac{1}{4K(V_G - 2V_{th})^2} \frac{2+3\sigma\lambda+4\delta\lambda}{(1+\sigma\lambda)^2 - \delta\lambda(1+\sigma\lambda+\delta\lambda)}\right] i_{in}^2 \\ & + \left[\frac{1}{2} \frac{\delta\lambda(4+5\sigma\lambda) + \sigma\lambda(1+\sigma\lambda)}{(1+\sigma\lambda)^2 - \delta\lambda(1+\sigma\lambda+\delta\lambda)}\right] i_{in} \\ & + \left[\frac{K(V_G - 2V_{th})^2}{4} \frac{(1+\sigma\lambda+\delta\lambda)^2(2+3\sigma\lambda)}{(1+\sigma\lambda)^2 - \delta\lambda(1+\sigma\lambda+\delta\lambda)}\right] \end{aligned}$$

$$i_{OUT} = \chi_1 \frac{i_{in}^2}{4I_B} + \chi_2 i_{in} + \chi_3 I_B \tag{A.39}$$

where

$$\chi_1 = \frac{2+3\sigma\lambda+4\delta\lambda}{2\left[(1+\sigma\lambda)^2 - \delta\lambda(1+\sigma\lambda+\delta\lambda)\right]} \tag{A.40}$$

$$\chi_2 = \frac{\delta\lambda(4+5\sigma\lambda) + \sigma\lambda(1+\sigma\lambda)}{2\left[(1+\sigma\lambda)^2 - \delta\lambda(1+\sigma\lambda+\delta\lambda)\right]} \tag{A.41}$$

$$\chi_3 = \frac{(1+\sigma\lambda+\delta\lambda)^2(2+3\sigma\lambda)}{2\left[(1+\sigma\lambda)^2 - \delta\lambda(1+\sigma\lambda+\delta\lambda)\right]} \tag{A.42}$$

Note that χ_1 and χ_2 are less than 1, whereas χ_3 is larger than 1. Furthermore, the above derivations only consider the channel length modulation effect, and the rest of short channel effects are ignored under the condition of small gate overdrive voltage of M_{SQ1}

and M_{SQ3}. If the effect of channel-length modulation effect is neglected as $\lambda = 0$, $\chi_1 = 1$, $\chi_2 = 0$, and $\chi_3 = 1$.

Moreover, even if the drain-to-source voltage differences of M_{SQ1} and M_{SQ3} are the same, the channel length modulation still has effects on the proposed squaring circuit of Figure A.1. In this case where $\delta \neq 0$ and $\lambda = 0$, (A.39) can be simplified to

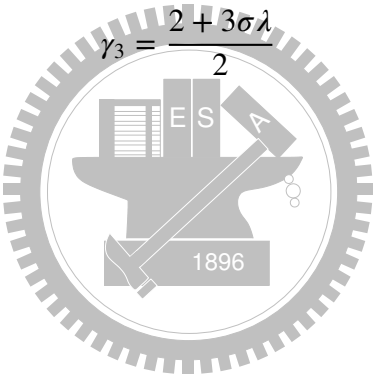
$$i_{OUT} = \gamma_1 \frac{i_{in}^2}{4I_B} + \gamma_2 i_{in} + \gamma_3 I_B \tag{A.43}$$

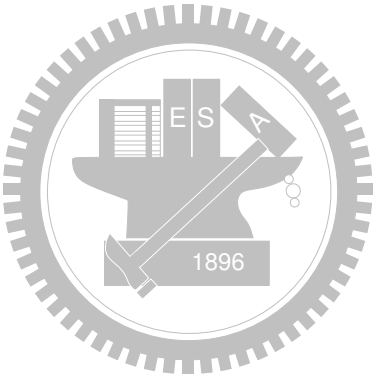
where

$$\gamma_1 = \frac{2 + 3\sigma\lambda}{2(1 + \sigma\lambda)^2} \tag{A.44}$$

$$\gamma_2 = \frac{\sigma\lambda}{2(1 + \sigma\lambda)} \tag{A.45}$$

$$\gamma_3 = \frac{2 + 3\sigma\lambda}{2} \tag{A.46}$$

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Appendix B

In the deep sub-micron CMOS technologies, the relationship between drain current i_{DS} and the gate overdrive voltage $v_{OV} = (v_{GS} - V_{th})$ of CMOS devices in the saturation region is not exactly square due to short channel effects, and the drain current i_{DS} is approximated as [163], [164]

$$i_{DS} \approx \frac{1}{2} k_n \frac{W}{L} \frac{\mu_n}{(1+\theta v_{OV})} \frac{v_{OV}^2}{\left(1 + \frac{v_{OV}}{E_C L}\right)} (1 + \lambda v_{DS}) \tag{B.1}$$

where E_C is the critical value of the horizontal electric field, θ is inversely proportional to the oxide thickness, and the coefficient λ models the effect of the channel length modulation which is related to v_{DS}. If the transistor in the saturation region is operated with small v_{OV} such that $v_{OV} \ll \theta^{-1}$ and $v_{OV} \ll E_C L$, (B.1) can be simplified approximately as

$$i_{DS} \approx \frac{1}{2} k_n \frac{W}{L} v_{OV}^2 (1 + \lambda v_{DS}) \tag{B.2}$$

The current-squaring circuit of Figure B.1 is proposed in Chapter 4 where the aspect ratio of M_3 (M_4) is N times that of M_1 (M_2). Although both M_1 and M_2 are with the same device size and are diode-connected, the drain-to-source voltages of M_1 and M_2 are different due to the fact that the latter suffers from body effect. As a result, the channel length modulation effect should be considered. In Figure B.1, $V_{DD} = (v_{DS,M_1} + v_{DS,M_2})$. If $\delta = (v_{DS,M_2} - v_{DS,M_1})/2$ is assumed, $v_{DS,M_1} = (V_{DD} - 2\delta)/2$ and $v_{DS,M_2} = (V_{DD} + 2\delta)/2$. The detailed derivations of the relationship between i_{in} and i_O are shown as the following.

$$i_1 = K(v_A - V_{th})^2 \left[1 + \lambda \left(\frac{V_{DD}}{2} - \delta\right)\right] \tag{B.3}$$

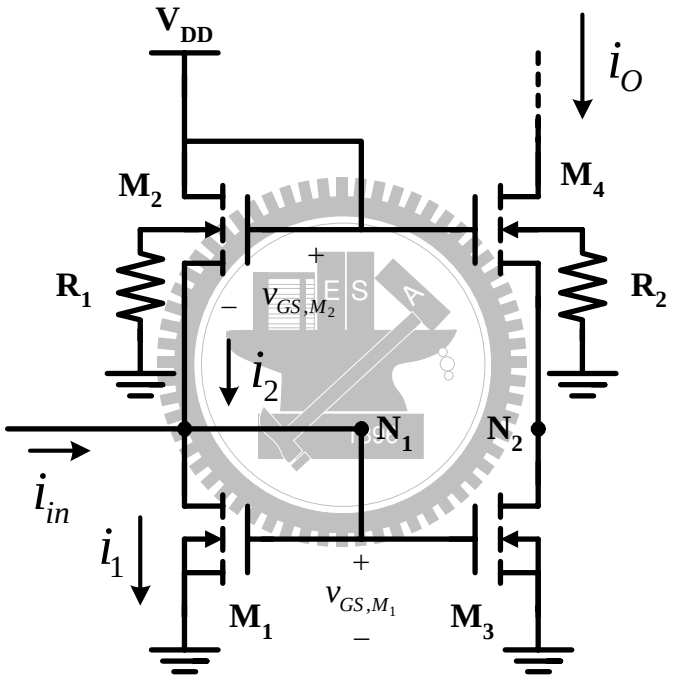


Figure B.1 Current-squaring circuit of up-conversion mixer.

$$i_2 = K(v_B - V_{th})^2 \left[1 + \lambda \left(\frac{V_{DD}}{2} + \delta\right)\right] \tag{B.4}$$

where

$$K = \frac{1}{2} k_n \frac{W}{L}$$

$$v_A = v_{GS,M_1}$$

$$v_B = v_{GS,M_2}$$

$$v_A + v_B = V_{DD} \tag{B.5}$$

Define

$$\begin{aligned} I_B &= \frac{1}{8} k_n \frac{W}{L} (V_{DD} - 2V_{th})^2 \\ &= \frac{1}{4} K (V_{DD} - 2V_{th})^2 \end{aligned} \tag{B.6}$$

From Figure B.1,

$$i_{in} = i_1 - i_2 \tag{B.7}$$

$$i_O = N \times i_1 = N \times (i_{in} + i_2)$$

$$i_O - N i_{in} = N i_2 \tag{B.8}$$

From (B.3), (B.4), and (B.7),

$$i_{in} = K \left[\left(1 + \frac{\lambda V_{DD}}{2}\right)(v_A - v_B)(V_{DD} - 2V_{th}) - \delta\lambda \left(V_{DD}^2 - 2v_A v_B - 2V_{DD}V_{th} + 2V_{th}^2\right)\right] \tag{B.9}$$

From (B.4) and (B.8),

$$i_O - N i_{in} = NK(v_B - V_{th})^2 \left(1 + \frac{\lambda V_{DD}}{2} + \delta\lambda\right) \tag{B.10}$$

From (B.10), the v_B can be represented as the follows in terms of i_{in} and i_O.

$$\begin{aligned} v_B &= V_{th} + \sqrt{\frac{i_O - N i_{in}}{NK(1 + \frac{\lambda V_{DD}}{2} + \delta\lambda)}} \\ &= V_{th} + C\sqrt{i_O - N i_{in}} \end{aligned} \tag{B.11}$$

where

$$C = \frac{1}{\sqrt{NK(1 + \frac{\lambda V_{DD}}{2} + \delta\lambda)}} \tag{B.12}$$

From (B.5),

$$v_A = V_{DD} - \left(V_{th} + C\sqrt{i_O - Ni_{in}}\right) \tag{B.13}$$

From (B.11) and (B.13),

$$v_A - v_B = (V_{DD} - 2V_{th}) - 2C\sqrt{i_O - Ni_{in}} \tag{B.14}$$

$$v_A v_B = V_{th}(V_{DD} - V_{th}) + C(V_{DD} - 2V_{th})\sqrt{i_O - Ni_{in}} - C^2(i_O - Ni_{in}) \tag{B.15}$$

Substitute (B.14) and (B.15) into (B.9), (B.9) can be expressed as

$$Di_{in} + Ei_O + F\sqrt{i_O - Ni_{in}} + G = 0 \tag{B.16}$$

where

$$\begin{aligned} D &= \frac{1}{K}\left(2\delta\lambda C^2 NK - 1\right) \\ &= \frac{1}{K}\left[\frac{4\delta\lambda}{2 + \lambda V_{DD} + 2\delta\lambda} - 1\right] \end{aligned} \tag{B.17}$$

$$E = -\frac{4\delta\lambda}{NK(2 + \lambda V_{DD} + 2\delta\lambda)} \tag{B.18}$$

$$F = -C(V_{DD} - 2V_{th})(2 + \lambda V_{DD} - 2\delta\lambda) \tag{B.19}$$

$$G = \frac{1}{2}(V_{DD} - 2V_{th})^2(2 + \lambda V_{DD} - 2\delta\lambda) \tag{B.20}$$

From (B.16),

$$Di_{in} + Ei_O + G = -F\sqrt{i_O - Ni_{in}}$$

$$(Di_{in} + Ei_O + G)^2 = \left(-F\sqrt{i_O - Ni_{in}}\right)^2$$

$$D^2 i_{in}^2 + E^2 i_O^2 + G^2 + 2DEi_{in}i_O + 2EGi_O + 2DGi_{in} = F^2(i_O - Ni_{in}) \tag{B.21}$$

Because $\delta \ll 1$ and $\lambda < 1$, $\delta\lambda \ll 1$. Therefore, DE and E^2 are small and they can be ignored. (B.21) can be rearranged as

$$i_O\left(F^2 - 2EG\right) = D^2 i_{in}^2 + \left(2DG - NF^2\right) i_{in} + G^2$$

Consequently,

$$i_O = \left(\frac{D^2}{F^2 - 2EG}\right) i_{in}^2 + \left(\frac{2DG + NF^2}{F^2 - 2EG}\right) i_{in} + \left(\frac{G^2}{F^2 - 2EG}\right) \tag{B.22}$$

Based on (B.12), (B.17)–(B.20),

$$\begin{aligned} F^2 &= [-C(V_{DD} - 2V_{th})(2 + \lambda V_{DD} - \delta\lambda)]^2 \\ &= C^2(V_{DD} - 2V_{th})^2(2 + \lambda V_{DD})^2 \left(1 - \frac{2\delta\lambda}{2 + \lambda V_{DD}}\right)^2 \end{aligned} \tag{B.23}$$

Because

$$\frac{2\delta\lambda}{2 + \lambda V_{DD}} \ll 1 \tag{B.24}$$

$$\left(1 - \frac{2\delta\lambda}{2 + \lambda V_{DD}}\right)^2 \approx 1 - \frac{4\delta\lambda}{2 + \lambda V_{DD}} \tag{B.25}$$

Substitute (B.12) and (B.25) into (B.23), F^2 can be expressed as

$$F^2 \approx \frac{2(V_{DD} - 2V_{th})^2(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\delta\lambda)}{NK(2 + \lambda V_{DD} + 2\delta\lambda)} \tag{B.26}$$

From (B.17),

$$D^2 = \frac{1}{K^2}\left(\frac{4\delta\lambda}{2 + \lambda V_{DD} + 2\delta\lambda} - 1\right)^2$$

Because

$$\frac{4\delta\lambda}{2 + \lambda V_{DD} + 2\delta\lambda} \ll 1$$

$$D^2 \approx \frac{1}{K^2}\left(1 - \frac{8\delta\lambda}{2 + \lambda V_{DD} + 2\delta\lambda}\right) \tag{B.27}$$

From (B.20) and (B.24),

$$\begin{aligned} G^2 &= \frac{1}{4}(V_{DD} - 2V_{th})^4(2 + \lambda V_{DD})^2 \left(1 - \frac{2\delta\lambda}{2 + \lambda V_{DD}}\right)^2 \\ &\approx \frac{1}{4}(V_{DD} - 2V_{th})^4(2 + \lambda V_{DD})^2 \left(1 - \frac{4\delta\lambda}{2 + \lambda V_{DD}}\right) \\ &\approx \frac{1}{4}(V_{DD} - 2V_{th})^4(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\delta\lambda) \end{aligned} \tag{B.28}$$

From (B.17) and (B.20),

$$DG = \frac{(V_{DD} - 2V_{th})^2}{2K}\left(\frac{4\delta\lambda}{2 + \lambda V_{DD} + 2\delta\lambda} - 1\right)(2 + \lambda V_{DD} - 2\delta\lambda) \tag{B.29}$$

From (B.18) and (B.20),

$$EG = -\frac{2\delta\lambda(V_{DD} - 2V_{th})^2}{NK}\left(\frac{2 + \lambda V_{DD} - 2\delta\lambda}{2 + \lambda V_{DD} + 2\delta\lambda}\right) \tag{B.30}$$

From (B.24), $2\delta\lambda \ll (2 + \lambda V_{DD})$, and therefore (B.30) is approximated as

$$EG \approx -\frac{2\delta\lambda(V_{DD} - 2V_{th})^2}{K} \tag{B.31}$$

From (B.26) and (B.31), $(F^2 - 2EG)$ is calculated as

$$F^2 - 2EG = \frac{2(V_{DD} - 2V_{th})^2\left[(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\delta\lambda) + 2\delta\lambda(2 + \lambda V_{DD} + 2\delta\lambda)\right]}{NK(2 + \lambda V_{DD} + 2\delta\lambda)} \tag{B.32}$$

From (B.6), (B.27), and (B.32),

$$\frac{D^2}{F^2 - 2EG} = \frac{N}{8I_B}\frac{2 + \lambda V_{DD} - 6\delta\lambda}{(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\delta\lambda) + 2\delta\lambda(2 + \lambda V_{DD} + 2\delta\lambda)} \tag{B.33}$$

From (B.26), (B.29), and (B.32),

$$\frac{2DG + NF^2}{F^2 - 2EG} = \frac{N}{2}\frac{2(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\delta\lambda) - (2 + \lambda V_{DD} - 2\delta\lambda)^2}{(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\delta\lambda) + 2\delta\lambda(2 + \lambda V_{DD} + 2\delta\lambda)} \tag{B.34}$$

From (B.28) and (B.32),

$$\frac{G^2}{F^2 - 2EG} = \frac{NI_B}{2}\frac{(2 + \lambda V_{DD})(2 + \lambda V_{DD} + 2\delta\lambda)(2 + \lambda V_{DD} - 4\delta\lambda)}{(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\delta\lambda) + 2\delta\lambda(2 + \lambda V_{DD} + 2\delta\lambda)} \tag{B.35}$$

Substitute (B.33)–(B.35) into (B.22), the relationship between i_O and i_{in} is as follows,

$$\begin{aligned} i_O \;=\; & \frac{Ni_{in}^2}{16I_B}\left[\frac{2(2 + \lambda V_{DD} - 6\delta\lambda)}{(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\delta\lambda) + 2\delta\lambda(2 + \lambda V_{DD} + 2\delta\lambda)}\right] \\ & + \frac{Ni_{in}}{2}\left[\frac{2(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\delta\lambda) - (2 + \lambda V_{DD} - 2\delta\lambda)^2}{(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\delta\lambda) + 2\delta\lambda(2 + \lambda V_{DD} + 2\delta\lambda)}\right] \\ & + \frac{NI_B}{2}\left[\frac{(2 + \lambda V_{DD})(2 + \lambda V_{DD} + 2\delta\lambda)(2 + \lambda V_{DD} - 4\delta\lambda)}{(2 + \lambda V_{DD})(2 + \lambda V_{DD} - 4\delta\lambda) + 2\delta\lambda(2 + \lambda V_{DD} + 2\delta\lambda)}\right] \end{aligned} \tag{B.36}$$

Therefore, considering the channel length modulation effect and body effect, the output current i_O of the current-squaring circuit shown in Figure B.1 can be expressed as the following equation in terms of i_{in}.

$$i_O = N\left(\chi_1\frac{i_{in}^2}{16I_B} + \chi_2\frac{i_{in}}{2} + \chi_3 I_B\right) \tag{B.37}$$

where

$$\chi_1 = \frac{2(2+\lambda V_{DD}-6\delta\lambda)}{(2+\lambda V_{DD})(2+\lambda V_{DD}-4\delta\lambda)+2\delta\lambda(2+\lambda V_{DD}+2\delta\lambda)} \tag{B.38}$$

$$\chi_2 = \frac{2(2+\lambda V_{DD})(2+\lambda V_{DD}-4\delta\lambda)-(2+\lambda V_{DD}-2\delta\lambda)^2}{(2+\lambda V_{DD})(2+\lambda V_{DD}-4\delta\lambda)+2\delta\lambda(2+\lambda V_{DD}+2\delta\lambda)} \tag{B.39}$$

$$\chi_3 = \frac{(2+\lambda V_{DD})(2+\lambda V_{DD}+2\delta\lambda)(2+\lambda V_{DD}-4\delta\lambda)}{(2+\lambda V_{DD})(2+\lambda V_{DD}-4\delta\lambda)+2\delta\lambda(2+\lambda V_{DD}+2\delta\lambda)} \tag{B.40}$$

Note that χ_1 and χ_2 are less than 1, whereas χ_3 is greater than 1. Furthermore, the above derivations only consider body effect and channel length modulation effect, and the rest of short channel effects are ignored under the design condition of small v_{OV} of M_1 and M_2. Moreover, even if the drain-to-source voltage differences of M_1 and M_2 are the same, the channel-length modulation still has effects on the proposed squaring circuit. In this case where $\delta = 0$ and $\lambda \neq 0$, (B.37) is simplified to

$$i_O = N\left(\gamma_1 \frac{i_{in}^2}{16I_B} + \frac{1}{2}i_{in} + \gamma_2 I_B\right) \tag{B.41}$$

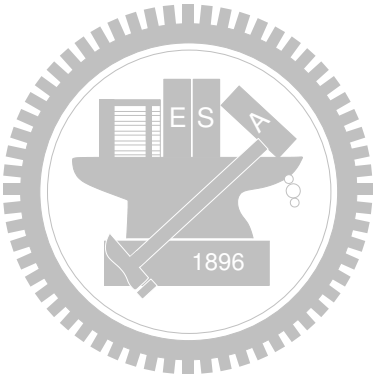
where

$$\gamma_1 = \left(1+\frac{\lambda V_{DD}}{2}\right)^{-1} \tag{B.42}$$

$$\gamma_2 = 1+\frac{\lambda V_{DD}}{2} \tag{B.43}$$

Note that γ_1 is less than 1, whereas γ_2 is greater than 1. However, if the long channel devices of M_1 and M_2 are used, where in ideal case $\lambda = 0$, the drain-to-source voltage differences of M_1 and M_2 will not has effects on the proposed squaring circuit. In this case where $\delta \neq 0$ and $\lambda = 0$, (B.37) is simplified to

$$i_O = N\left(\frac{i_{in}^2}{16I_B} + \frac{1}{2}i_{in} + I_B\right) \tag{B.44}$$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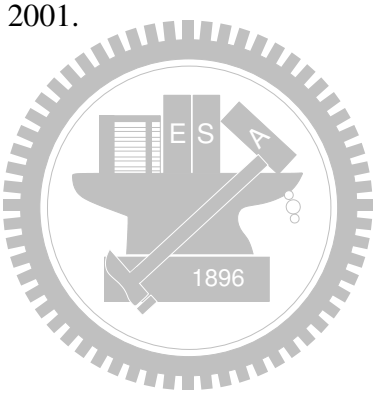

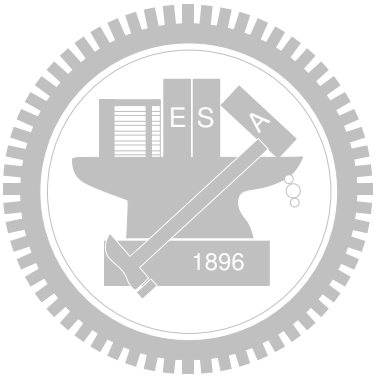
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PUBLICATION LIST

- **REFERRED JOURNAL PAPER**
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