Chapter 1

Introduction

1.1 General Background and Motivation

Copper metallization has become an important topic in the silicon integrated circuit technology ever since IBM announced its success in silicon very large scale integration process [1]-[3]. The advantages of copper metallization for Si VLSI include lower resistivity, higher electromigration resistance and stress voiding as compared to commonly used aluminum. However, copper diffuses very fast into Si when it is in contact with Si substrate without any diffusion barrier [4]-[6]. As in the silicon case, copper also diffuses very fast into GaAs when copper is in direct contact with the GaAs substrate without any diffusion barrier [7]. Even though the use of copper as metallization metal has become very popular in Si devices, there were very few reports of copper metallization of GaAs devices published in the literature and Ta and TaN were used as the diffusion barriers for copper metallization in these reports [8]-[10]. In this work, copper-metallized GaAs and InP heterojunction bipolar transistor devices were studied.

Traditionally, GaAs devices use Au/Ge/Ni/Au for n-type and Pt/Ti/Pt/Au for p-type ohmic contacts, such as metal semiconductor field-effect transistors (MESFETs), high electron mobility transistors (HEMTs), and heterojunction bipolar transistors (HBTs). In addition, GaAs devices use Ti as adhesion layer, and Au as the metallization metal for interconnect metal and transmission lines. The use of copper as the metallization metal has several advantages over gold such as lower resistivity (1.67 μΩ-cm for Cu; 2.2 μΩ-cm for Au), higher thermal conductivity (0.94 cal/cm sec ^{o}C for Cu; 0.7 cal/cm sec ^{o}C for Au), and lower cost. A comparison of the

characteristics of the interconnect metals is list in Table 1.1. If Cu replaces Au as the interconnect metal for the HBTs, then the improvement in the electrical conductivity can increase the transmission speed of the circuits and the heat dissipation will be improved as well. The price of Cu is 5400 times cheaper than that of Au, and therefore the manufacturing cost will be substantially reduced. However, Cu diffuses very fast into most metals, silicon substrate, as well as III-V based substrate. That would induce new phase formation at higher temperature. In addition, diffusion of copper through the ohmic contacts and silicon nitride film into the HBTs will cause the degradation of the electrical properties of the HBT devices. Therefore, the use of copper interconnect for HBTs requires suitable diffusion barrier which is compatible with the HBT processes to prevent the copper inter-diffusion into the GaAs substrate. On the other hand, Cu is easy to oxidation. So a passivation layer is required to prevent the oxide of Cu surface [11]. Besides, copper is difficult to be removed by dry etch due to the lack of volatile compounds. Therefore, lift-off process technology is the solution in this work.

The diffusion barrier between the Cu interconnections and the semiconductor substrate for the GaAs devices should have the following characteristics:

(1) High resistance to diffusion of foreign atoms;

(2) High conductivity, thermal stability and crystallization temperature;

(3) Inert with Cu and underlying metal or substrate;

(4) Good adhesion between Cu and underlying materials;

(5) Smooth surface and low stress;

(6) Lack of grain boundaries and with an amorphous texture;

(7) The loss rate of barrier layer into overlying metal and underlying substrate should be small.

In our previous studies, we have demonstrated backside Cu metallization on

GaAs MESFETs using TaN as the diffusion barrier [10] and Cu air-bridge on low noise GaAs HEMTs using WN_X as the diffusion barrier [12]. In this study, the interconnect copper metallization of InGaP/GaAs HBTs using WN_X as the diffusion barrier was investigated. Further more, the gold-free fully Cu-metallized (from ohmic contact to interconnect metal) InGaP/GaAs and InP/InGaAs HBTs were studied. This is the first time the Cu-metallized HBTs are demonstrated in the literature.

1.2 Outline of the Dissertation

This dissertation covers the study of the copper-metallized GaAs and InP HBTs and is divided into 6 chapters. In Chapter 2, introduction of the GaAs and InP HBTs and the device structures are covered. In addition, the detailed HBT process flow is also present.

In Chapter 3, use of WN_X as the diffusion barrier for interconnect copper metallization of InGaP/GaAs HBTs is investigated. The WN_X (40 nm) and Cu (400 nm) films were deposited sequentially on the InGaP/GaAs HBT wafers as the diffusion barrier and interconnect metallization layer respectively using the sputtering method. The stabilities of WN_X between Cu and Au and between Cu and silicon nitride were investigated. Scanning electron microscopy (SEM), X-ray diffraction (XRD), Auger electron spectroscopy (AES), and sheet resistance were used for phase identification and the study of the interfacial reactions. The HBT devices with gold interconnects and the devices with copper interconnects were stressed using current-accelerated test and high-temperature thermal annealing test for reliability evaluation and comparison. These two kinds of devices showed similar characteristics after the stress tests.

In Chapter 4, gold-free fully copper-metallized InGaP/GaAs HBT using

platinum as the diffusion barrier is presented. The HBT uses Pd/Ge and Pt/Ti/Pt/Cu as the n^+-type and p^+-type ohmic metals, respectively, and uses Ti/Pt/Cu as the interconnect metals with platinum as the diffusion barrier. The thermal stability of the ohmic contact structures and Ti/Pt/Cu structure were studied. SEM, XRD, and sheet resistance were used for the study of the interfacial reactions. The fully copper-metallized InGaP/GaAs HBT devices were stressed using a current-accelerated test and a high-temperature thermal annealing test for reliability evaluation. The high-current test was performed at a high current density of 140 kA/cm^2 for 24 h. The thermal test was carried out by annealing at 250℃ for 24 h in nitrogen ambient. Au-free fully Cu-metallized HBTs using Pt as the diffusion barrier and Pd/Ge and Pt/Ti/Pt/Cu as the ohmic contacts were demonstrated in this study.

In Chapter 5, we present the gold-free fully Cu-metallized InP HBTs using non-alloyed Ti/Pt/Cu and Pt/Ti/Pt/Cu ohmic contact and platinum diffusion barrier. The thermal stability of the ohmic contact structures, InGaAs/Ti/Pt/Cu and InGaAs/SiN/Ti/Pt/Cu structures were studied. The fully copper-metallized InP HBT devices were stressed using a high-temperature thermal annealing test and a current-accelerated test for reliability evaluation. The thermal test was carried out by annealing at 200℃ for 3 hours in nitrogen ambient. The high-current test was performed at a high current density of 80 kA/cm^2 for 24 h. The Au-free, fully Cu-metallized InP HBT was realized using non-alloyed ohmic contacts and Pt diffusion barrier in this study.

Chapter 6 is the conclusion of the dissertation.

TABLE

Property	Cu	Ag	Au	Al
Resistivity(μΩ・cm)	1.67	1.59	2.35	2.66
Young's modulus・10^{-11} dyn/cm^2	12.98	8.27	7.85	7.06
Thermal Conductivity (W/cm)	3.98	4.25	3.15	2.38
CTE・10^6	17	19.1	14.2	23.5
Melting Point (℃)	1085	962	1064	660
Specific heat Capacity (J/Kg•K)	386	234	132	917
Corrosion in air	Poor	Poor	Excellent	Good
Deposion				
Sputtering	Yes	Yes	Yes	Yes
CVD	Yes	No	No	No
Evaporation	Yes	Yes	Yes	Yes
Etching				
Dry	No	No	No	Yes
Wet	Yes	Yes	Yes	Yes
Resistance to Electromigration	High	Very Low	Very High	Low
Delay Time(ps/mm)	2.3	2.2	3.2	3.7

Table 1.1 Properties comparisons of the possible interlayer metals

Chapter 2

Fabrication of Heterojunction Bipolar Transistor

2.1 Introduction of GaAs HBT

The concept of the heterojunction bipolar transistor was first introduced by William Shockley in 1948. A detailed theory related to this device was developed by H. Kroemer in 1957 [13]. Kroemer realized that the use of a wide-band-gap emitter and low-band-gap base would provide band offsets at the heterointerface that would favor the injection of the electrons, in an n-p-n transistor, into the base while retarding hole injection into the emitter. These advantages would be maintained, even when the base is heavily doped, as is required for low base resistance, and the emitter is lightly doped. Thus in an HBT, high emitter injection efficiency would be maintained while parasitic resistances and capacitances would be lower than for a conventional homojunction bipolar transistor.

The cross section of a basic n-p-n AlGaAs/GaAs heterojunction bipolar transistor is shown in Figure 2.1. The n-type emitter is formed in the wide-band-gap AlGaAs while the p-type base is formed in the lower band gap GaAs. The n-type collector, in this basic device, is also formed on GaAs. To facilitate the formation of the ohmic contacts, a heavily doped n^+-GaAs layer is present between the emitter contact and the AlGaAs layer. The energy band diagram of this device is shown in Figure 2.2.

Some inherent advantages of HBTs over silicon bipolar transistors are as follows [14]:

(1) Due to the wide-band-gap emitter, a much higher base doping concentration can be used, decreasing base resistance.

(2) Emitter doping can be lowered and minority carrier storage in the

emitter can be made negligible, reducing base-emitter capacitance.

(3) High electron mobility, built-in drift fields, and velocity overshoot combine to reduce the electron transit time.

(4) Semi-insulating substrates help reduce pad parasitics and allow convenient integration of devices.

(5) Early voltages are higher and high injection effects are negligible due to high base doping.

Figure 2.3 shows the band diagram of a homojunction BJT and HBT. The energy band gap difference between the emitter and the base gives the HBT a substantial edge over BJT. When the base-emitter junction of a BJT is forward biased, both the electrons forward-injection into the base and the hole back-injected into the emitter experience the same amount of energy barrier. For the HBT, when the base-emitter junction is forward biased, the holes, which are back inject from the base into emitter, experience a $\triangle E_g$ larger energy barrier than the electrons, which are injected into the base. So, the HBT provides a design freedom meaning that a HBT structure design can have a heavily base dope to reduce the base resistance, while still maintaining a high current gain. We can quantify the advantage of HBT compared to BJT by calculating the ratio of the collector current to the base current [15].

$$\frac{Ic}{I} = \frac{D_{nB} X_E N_E}{D_{pE} X_B N_B} \frac{{n_{iB}}^2}{{n_{iE}}^2} = \frac{D_{nB} X_E N_E}{D_{pE} X_B N_B} \exp\left(\frac{\Delta E_g}{kT}\right) \qquad (2.1)$$

Equation (2.1), which relates the intrinsic carrier concentration to the energy gap, was used in the derivation. It's defined as the current gain which is one of the most important parameters in bipolar transistors.

Among several HBT device structures, InGaP/GaAs HBTs are becoming

attractive as compared with AlGaAs/GaAs HBTs in the following circuit applications such as high-speed analog-to-digital converters, high-power microwave amplifiers, and high-speed optical communication circuits due to their robust reliability and excellent DC and RF performance. In addition, several advantages have been claimed for this material system, such as large valence-band discontinuity, very low interface recombination velocities with GaAs, significantly less oxidation in comparison with AlGaAs, no DX centers issue, and good selective etch with GaAs [16].

2.2 Introduction of InP HBT

InGaAs/InP single heterojunction bipolar transistors on InP substrate, which exhibit excellent high frequency noise and gain characteristics under low power consumption, are suitable candidates for high-frequency low-noise circuit applications because InP and InGaAs lattice-matched to InP substrate have unique material properties which enable better device performances than in GaAs-based HBT's.

Fabrication of InP-based HBTs is similar to that of the GaAs-based HBTs. There are two differences that have implications to the technology. First, the GaAs HBT is isolated by implantation through the collector. The InGaAs collector used for the InP-based process does not become isolating after implantation due to the low energy bandgap of the material. Therefore, for the InP-based HBT, the mesa is much taller than that for the mesa of the GaAs-based transistor mesa. Second, the surface recombination velocity of GaAs is much higher than InGaAs. This prevents the GaAs HBT from being efficiently scaled to smaller dimensions. Therefore, it can be seen that the GaAs process can be used as a starting point; however, the taller InP mesa and scaling of the emitter must be considered [17].

The advantages of InP-based HBTs over GaAs-based HBTs are as follows:

(1) InGaAs has larger electron mobility and higher values of velocity overshoot than GaAs's, which persist over larger voltage ranges, result in shorter base and collector transit times;

(2) The larger conduction band inter-valley separations, Γ-X and Γ-L, of InGaAs (0.55 eV) over GaAs (0.3 eV) allows electrons to remain in the high velocity Γ valley throughout the base and collector over a larger range of collector reverse-bias voltages;

(3) InGaAs's smaller (than GaAs's) bandgap results in smaller base-emitter voltage drops and permits lower operating voltages and power dissipation;

(4) InGaAs's substantially lower surface recombination velocity improves the scaling of current gain for small emitter size and low current densities and also leads to lower 1/*f* noise [18];

(5) InP substrate's higher thermal conductivity than GaAs substrate's advantages the InP-based HBTs' applications on DHBT.

However, the InP substrates' less mature growth technique results in the small size for the InP wafers. The largest InP wafer of 6-inch was recently released. Besides, the InP substrates are fragile. So, the lack of reliable, reproducible fabrication techniques have limited the implementation of this technology to high level circuit complexity.

There are two kinds of heterojunction for InP-based HBTs with lattice matched to the InP substrate, AlInAs/InGaAs and InP/InGaAs. Figure 2.4 shows the band lineups for the two abrupt (a) InP/$In_{.53}Ga_{.47}As$ and (b) $Al_{.48}In_{.52}As$/ $In_{.53}Ga_{.47}As$ interfaces. Table 2-1 lists the band lineup information for these heterostructure systems and, for comparison, for an $Al_{.3}Ga_{.7}As$/GaAs heterojunction. In the AlInAs/InGaAs heterostructure, most of the discontinuity occurs in the conduction band ($\Delta E_C/\Delta E_V$ = 67/33), whereas in the InP/InGaAs system it is mostly in the

valence band ($\Delta E_C/\Delta E_V$ = 42/58). A larger valence-band offset permits higher base doping level, and the lower conduction-band discontinuity presents a smaller resistance against electron flow at the emitter junction [19].

2.3 Device Structure

For GaAs based HBT, the epitaxial layers of the InGaP/GaAs HBT were grown by metal organic chemical vapor deposition (MOCVD) on semi-insulating (100) GaAs substrate. The typical InGaP/GaAs HBT epitaxial layer structure is shown in Table 2.2. The GaAs subcollector layer was grown on a 3-inch diameter semi-insulating substrate, and it was heavily doped to reduce the n-type ohmic contact resistance. The lightly n-type doped GaAs collector layer and the heavily p-type doped GaAs base layer were grown on it subsequently. The emitter layer is InGaP, and the heavily doped GaAs layer on the top serves as the ohmic cap layer.

On the other hand, for InP based HBT, the epitaxial layers of the InP/InGaAs HBT were grown by MOCVD on the semi-insulating (100) InP substrate. Table 2.3 shows the typical InGaP/GaAs HBT epitaxial layer structure. The InGaAs subcollector layer was grown on a 2-inch diameter semi-insulating substrate, and it was heavily doped to reduce the n-type ohmic contact resistance. The lightly n-type doped InGaAs collector layer and the heavily p-type doped InGaAs base layer were grown on it subsequently. The emitter layer is InP, and the heavily doped InGaAs layer on the top serves as the ohmic cap layer.

2.4 Device Fabrication

The details of the typical GaAs HBT device fabrication are described as follows.

The traditional Au GaAs HBTs which use AuGe/Ni/Au and Pt/Ti/Pt/Au as n-type and p-type ohmic contacts metals and Ti/Au as the interconnect metal were also prepared for comparison. The process sequence for these devices is delineated in Figure 2.5.

2.4.1 Emitter Mesa, Collector Mesa, and Isolation

The InGaP/GaAs HBT devices were fabricated using a standard triple mesa process. The GaAs ohmic contact layer was etched by etchant composed of phosphoric acid, hydrogen peroxide, and D.I. water. And the InGaP layer was etched by a mixture of phosphoric acid and hydrogen chloride acid. After each etching process, the devices were rinsed by D.I. water and blown dry by nitrogen gas. The first step of the fabrication was to define the emitter mesa area. The emitter mesa was etched and stopped on the InGaP emitter layer. The base and collector mesa were etched and stopped on the GaAs subcollector layer. During the isolation etch, the GaAs subcollector was etched to the extent of undercut to separate each devices and to reduce the leakage current from the substrate. The flow diagrams of the triple mesa process are shown in Figure 2.5.1 – Figure 2.5.3.

2.4.2 Emitter and Collector Ohmic Contact Metal

An ohmic contact is a low resistance junction formed between metal and semiconductor to allow electrical current to flow into in the semiconductor device as shown in Fig 2.5.4. Lower resistance of the ohmic contact can lead to better device performance. In order to get good ohmic contact with low parasitic resistance, the semiconductor is usually doped heavily to form good contacts. The heavily doping is essential to form a good ohmic contact. The material usually used to create an

n^+-GaAs ohmic contact is AuGe/Ni/Au metal structure, which is a low resistance, reliable ohmic contact.

In order to remove the unwanted metal, a liftoff process was used, start by the process coating a layer of image reversal photoresist that can form good undercut profile, and after metal deposition using e-gun evaporator, the wafer was soaked in ACE to remove the unwanted metal. The metallization metals in this fabrication were all defined by image reversal AZ-5214E photoresist. After the emitter and collector metals deposition, a high temperature alloying process using RTA was conduced to form the ohmic contacts. To confirm whether the alloyed contact had been done well, the ohmic contact resistance of device was measured in process control monitor by using the transmission line model (TLM) method.

2.4.3 Base Ohmic Contact Metal

For GaAs HBTs, the base layer is formed by GaAs with Carbon doping to form p^+ type doping. In order to form ohmic contact on p^+-GaAs layer, the Pt/Ti/Pt/Au metal was used. To prevent surface oxidation, the emitter ledge method as shown in Figure 2.5.5 was used. Before the deposition of the base metal, the material of InGaP emitter layer under the base ohmic contact photoresist opening was etched to expose the underlying base layer. The base ohmic metal was also deposited by e-gun evaporator and metallization was completed by lift off process.

2.4.4 Device Passivation and Contact Via

HBTs are sensitive to surface effect in the device active region. Plasma enhanced chemical vapor deposition (PECVD) nitride was used on the sample for surface

encapsulation. The major purpose of the silicon nitride protective encapsulation is simply for the surface passivation. This passivation protects the critical area of the originally exposed wafer surface from humidity, chemicals, gases, and particles. The reason why silicon dioxide was not used as the passivation dielectrics in this study is that silicon nitride is less permeable to ions than silicon dioxide, therefore the silicon nitride is relatively reliable material for device passivation. In this study, the silicon nitride film thickness was about 100 nm. Passivation Vias between ohmic contact metals and interconnect metals were etched by reactive ionic etcher (RIE). The schematics of the device passivation and contact via are as shown in Figure 2.5.6 and Figure 2.5.7.

2.4.5 Interconnect Metal Line

The metal line is interconnection between three electrodes (emitter, base, and collector electrodes) and metal pads. After opening the connecting via on the silicon nitride film, the Ti/Au metals were sequentially deposited by e-gun evaporator over patterned resist. The metals were then removed by an ACE wet solvent lift-off process, followed by a high pressure DI water rinse to remove the residues. The schematic of the interconnect metal line is as shown in Figure 2.5.8. After the process described above, the front side processing is completed. The SEM image of the HBT is shown in Figure 2.6. The DC characteristics were measured by HP4142B and Kral Suss semi-automatic probe system.

TABLES

	$E_g(eV)$	$\Delta E_C(eV)$	$\Delta E_V(eV)$
InP/$In_{.53}Ga_{.47}As$	1.35/0.76	0.25	0.34
$Al_{.48}In_{.52}As$/$In_{.53}Ga_{.47}As$	1.48/0.76	0.48	0.24
$In_{.49}Ga_{.51}P$/GaAs	1.92/1.42	0.12	0.38
$Al_{.3}Ga_{.7}As$/GaAs	1.86/1.42	0.28	0.15

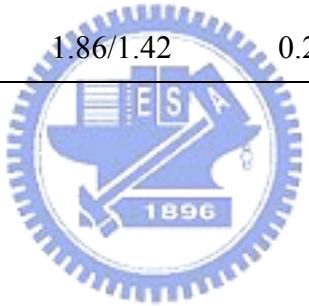


Table 2.1 Band-gap information of different heterostructures [19]

Layer	Material	Type	Doping	Thickness（Å）
Emitter Cap	GaAs	*n*+	5×10^{18}	2000
Emitter	InGaP	*n*	3×10^{17}	500
Base	GaAs	*p*+	4×10^{19}	800
Collector	GaAs s	*n*-	2×10^{16}	7000
Subcollector	GaAs	*n*+	5×10^{18}	5000
Substrate	GaAs			

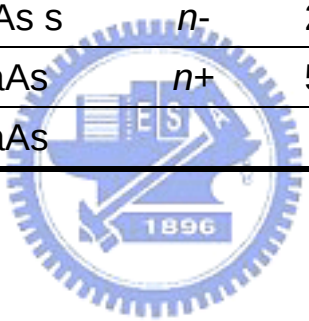


Table 2.2 The typical epitaxial layer structure of the InGaP/GaAs HBT

Layer	Material	Type	Doping	Thickness（Å）
Emitter Cap	InGaAs	*n*+	1×10^{19}	1000
Emitter	InP	*n*	5×10^{17}	1100
Base	InGaAs	*p*+	2×10^{19}	1000
Collector	InGaAs	*n*-	2×10^{16}	6000
Subcollector	InGaAs	*n*+	2×10^{19}	5000
Substrate	InP			

Table 2.3 The typical epitaxial layer structure of the InP/InGaAs HBT

FIGURES

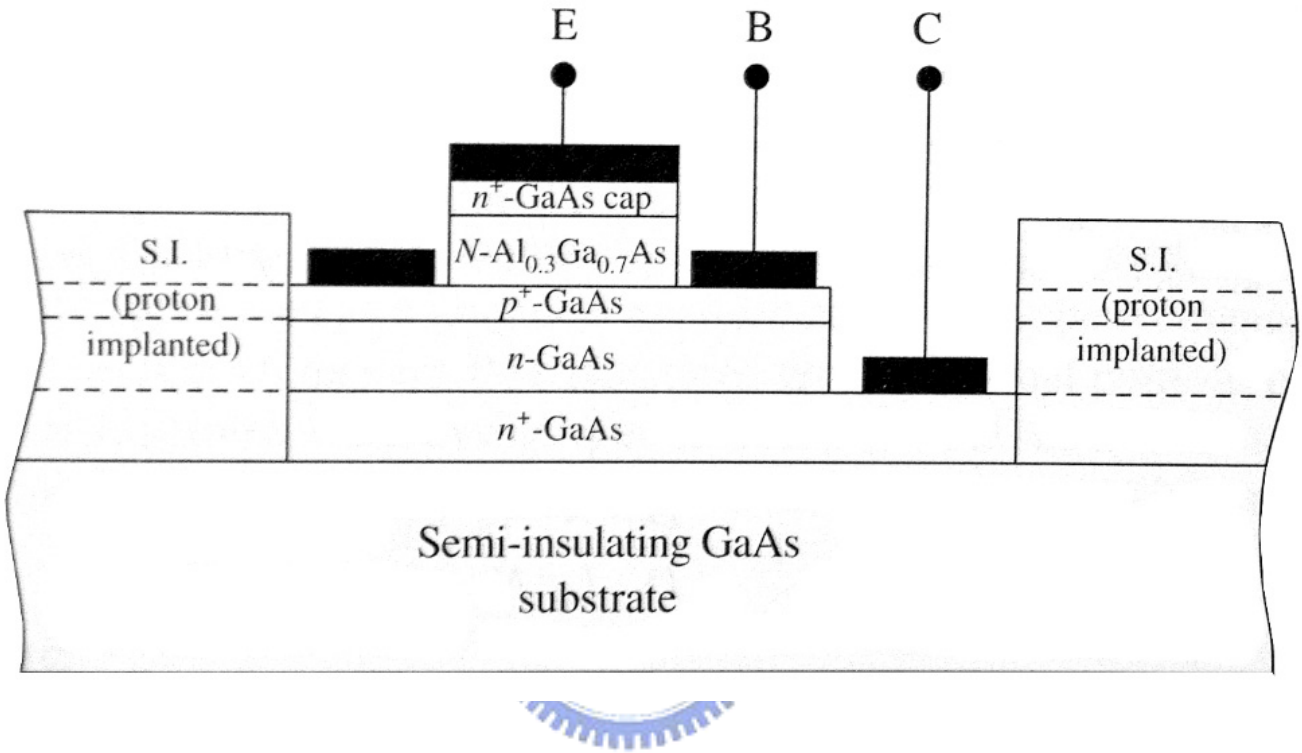


Figure 2.1 Schematic of the cross section of an HBT structure.

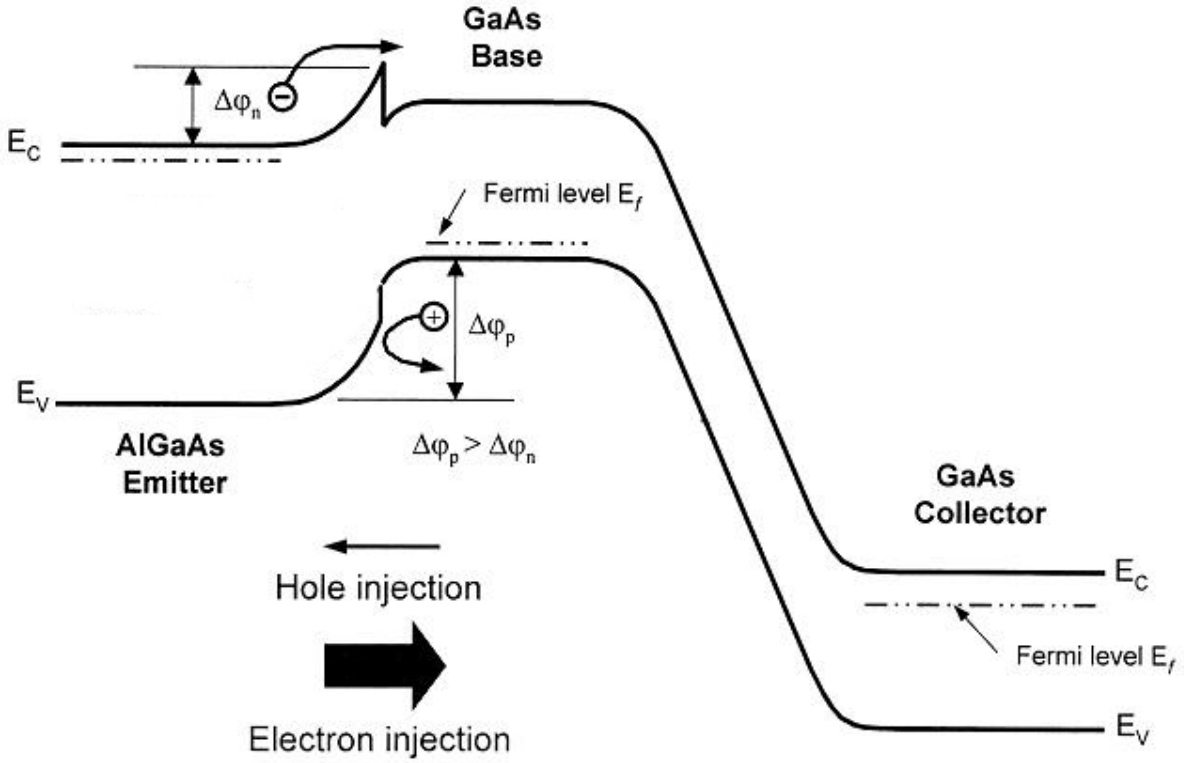


Figure 2.2 Energy band diagram of an HBT structure.

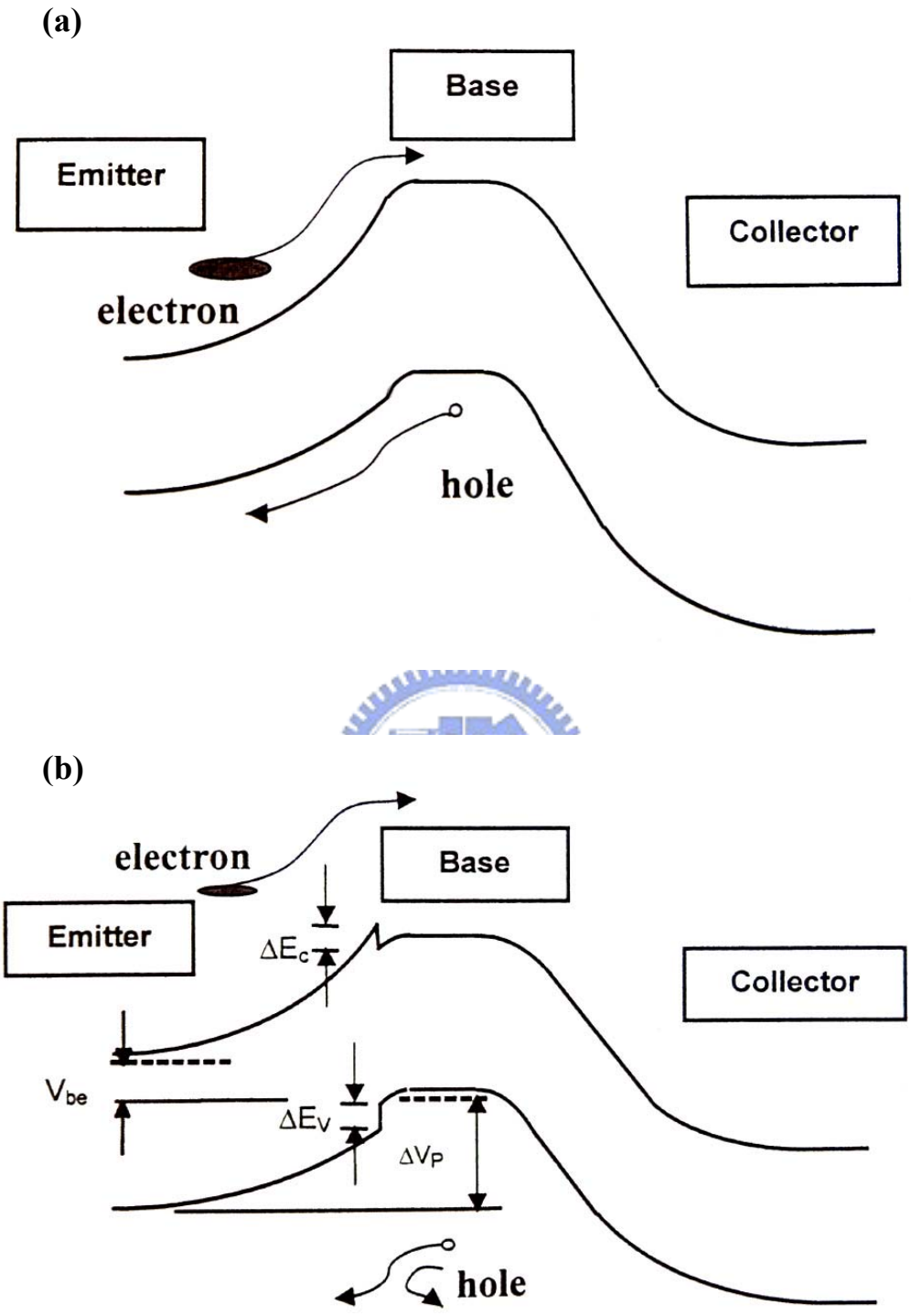


Figure 2.3 The band diagrams of (a) a homojunction bipolar transistor and (b) a heterojunction bipolar transistor.

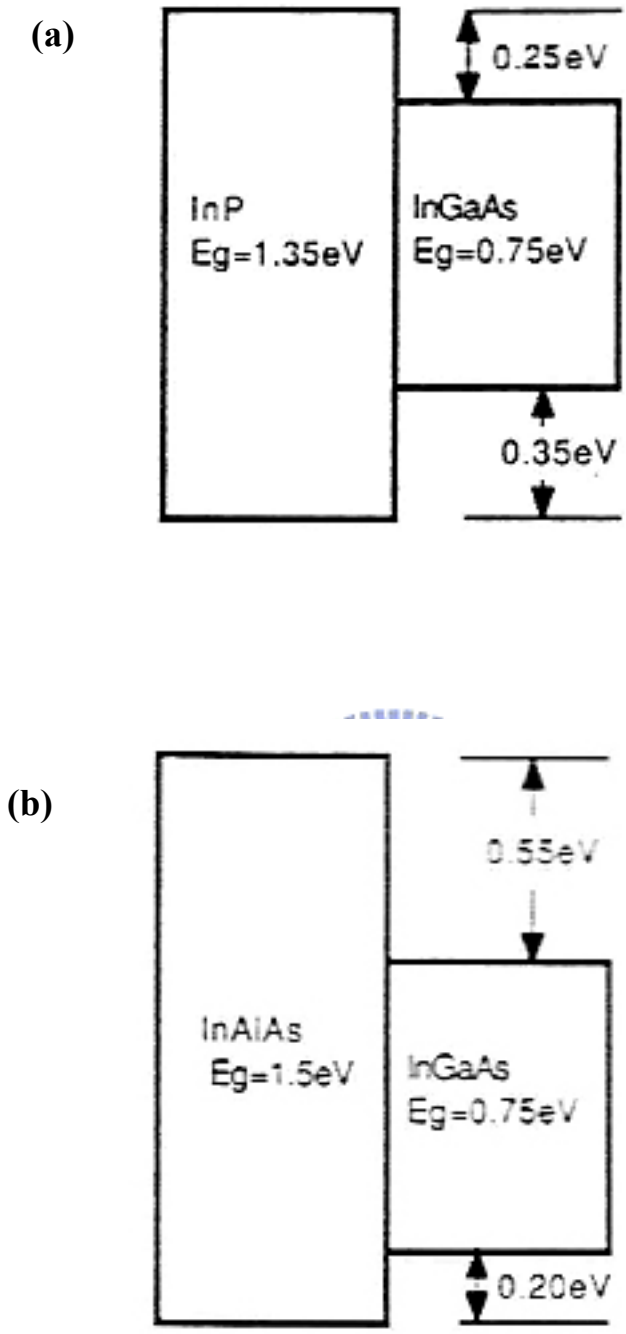


Figure 2.4 Energy-band band lineups for the two abrupt interfaces:

(a) InP/$In_{.53}Ga_{.47}As$ and (b) $Al_{.48}In_{.52}As$/ $In_{.53}Ga_{.47}As$

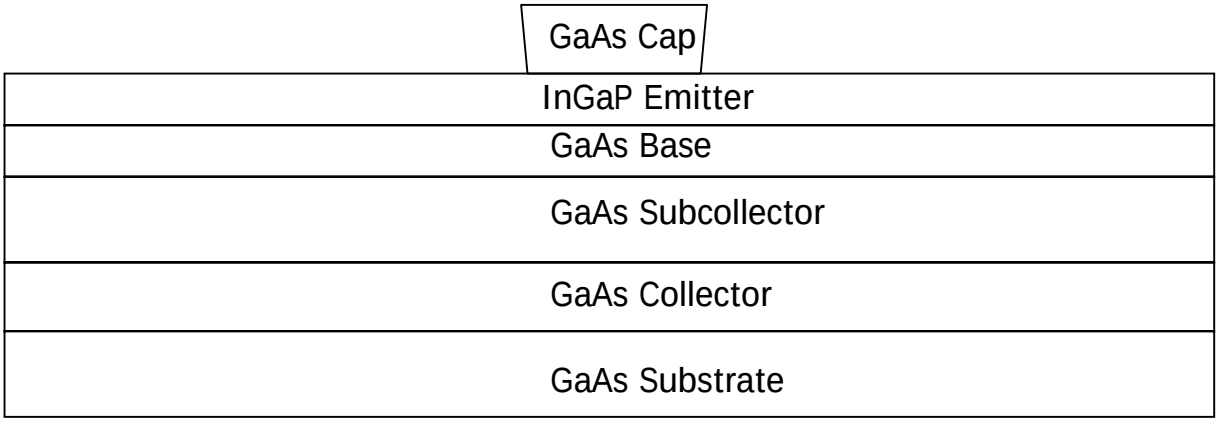


Figure 2.5.1 Emitter mesa etch

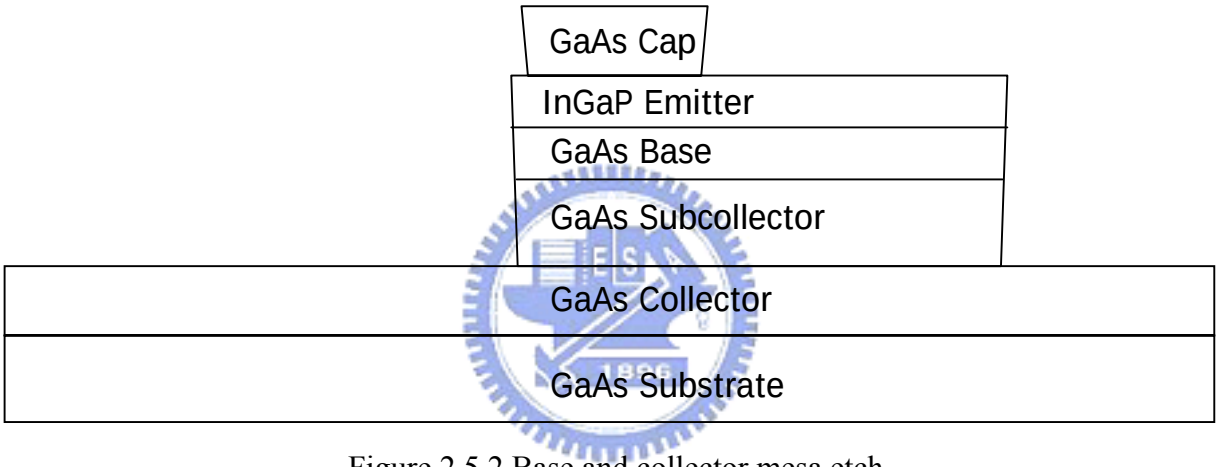


Figure 2.5.2 Base and collector mesa etch

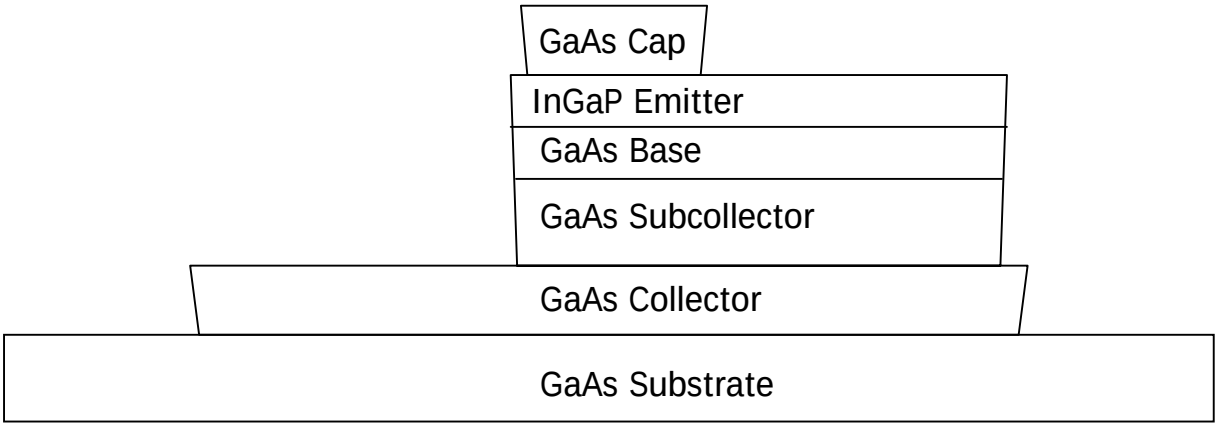


Figure 2.5.3 Mesa isolation

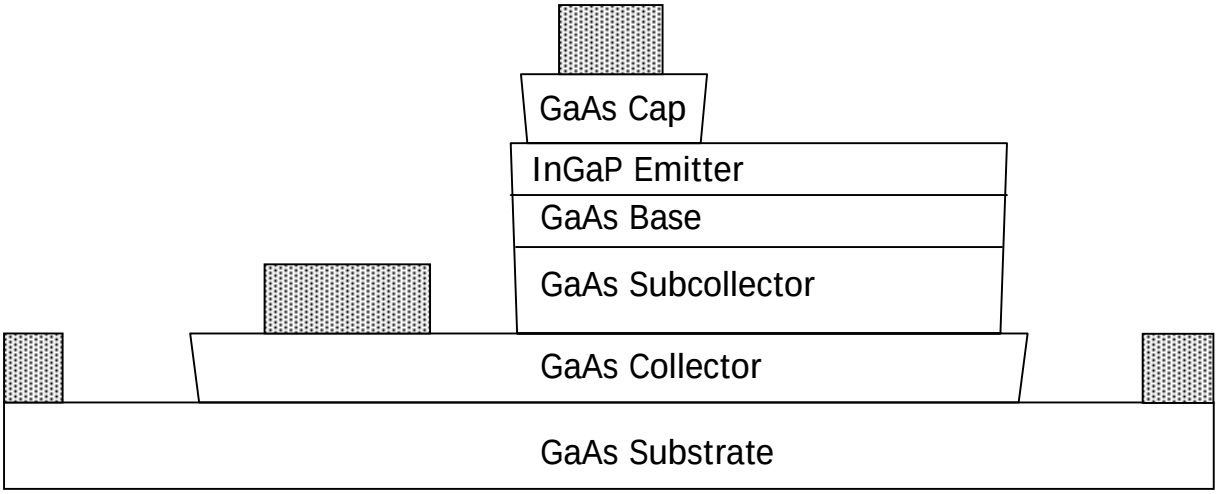


Figure 2.5.4 Emitter and collector ohmic contact metal formation

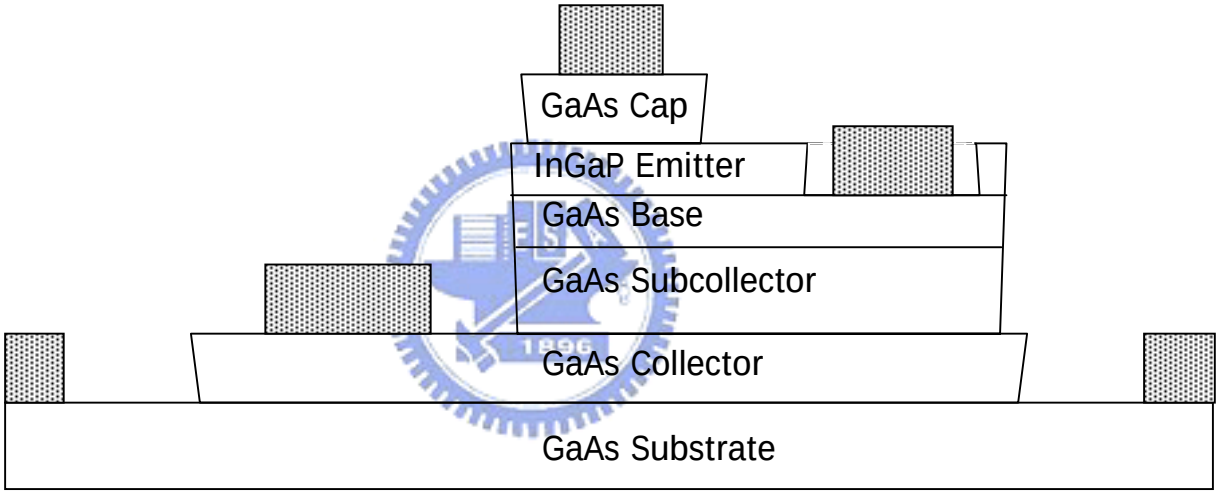


Figure 2.5.5 Base ohmic contact metal formation

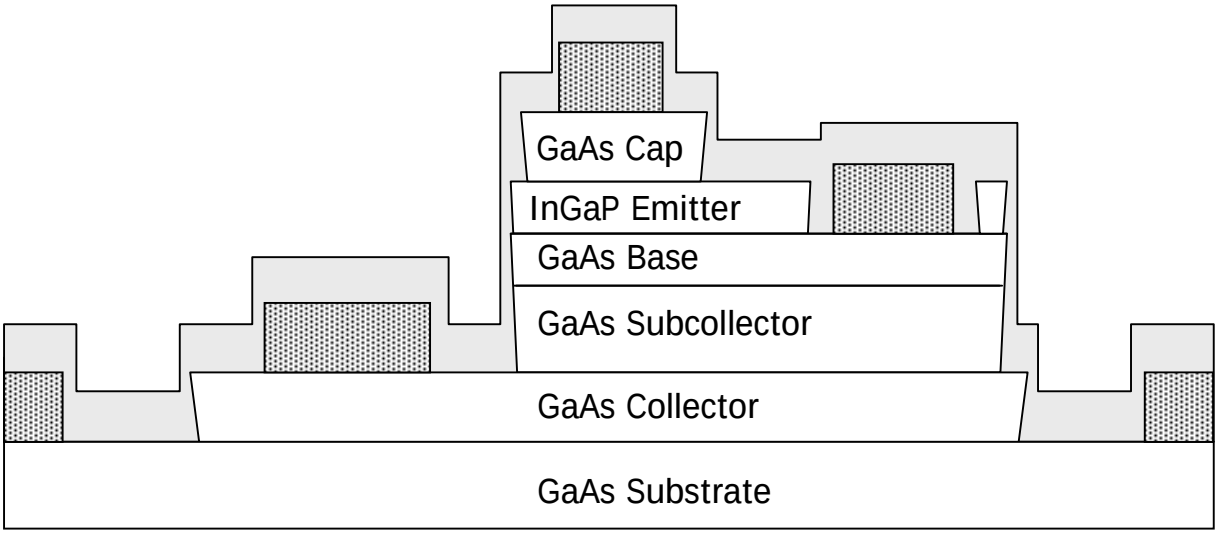


Figure 2.5.6 Silicon Nitride Deposition

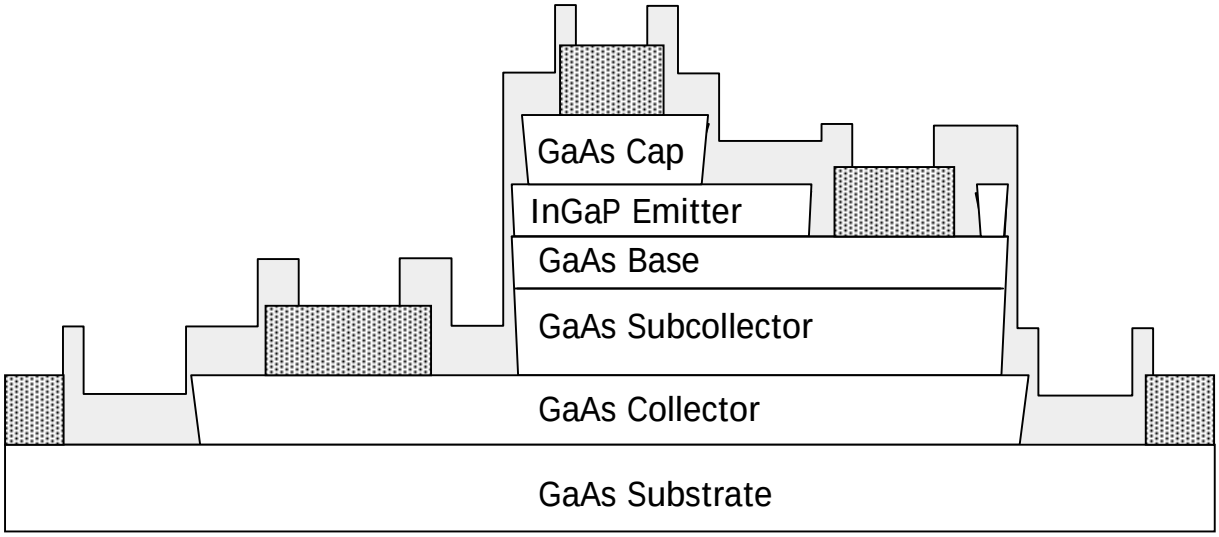


Figure 2.5.7 Nitride via etch

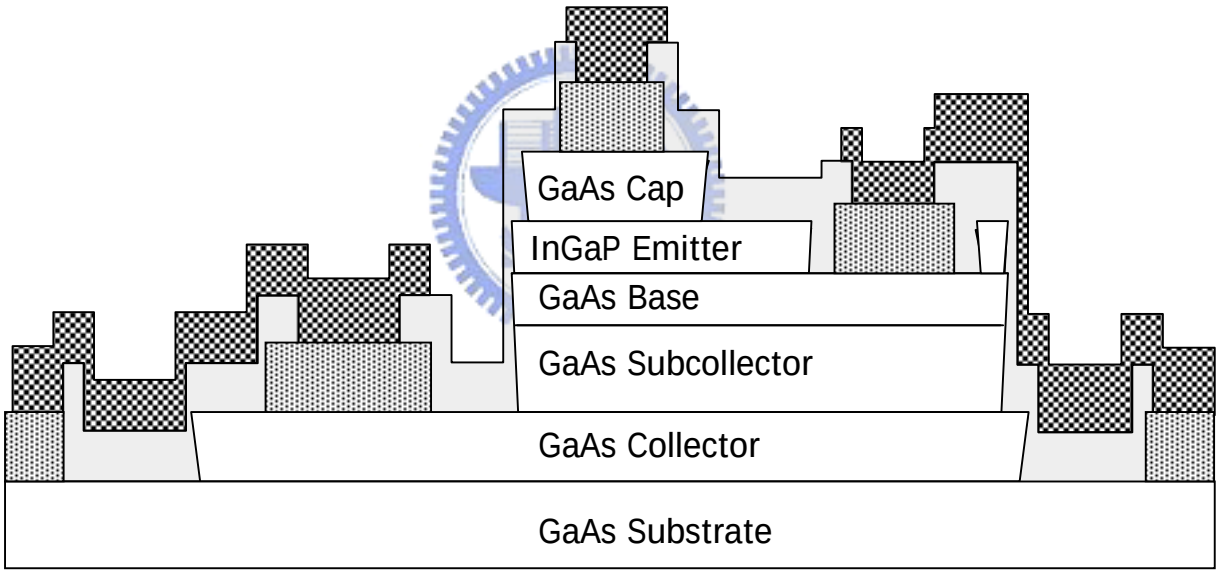


Figure 2.5.8 Interconnect metal line

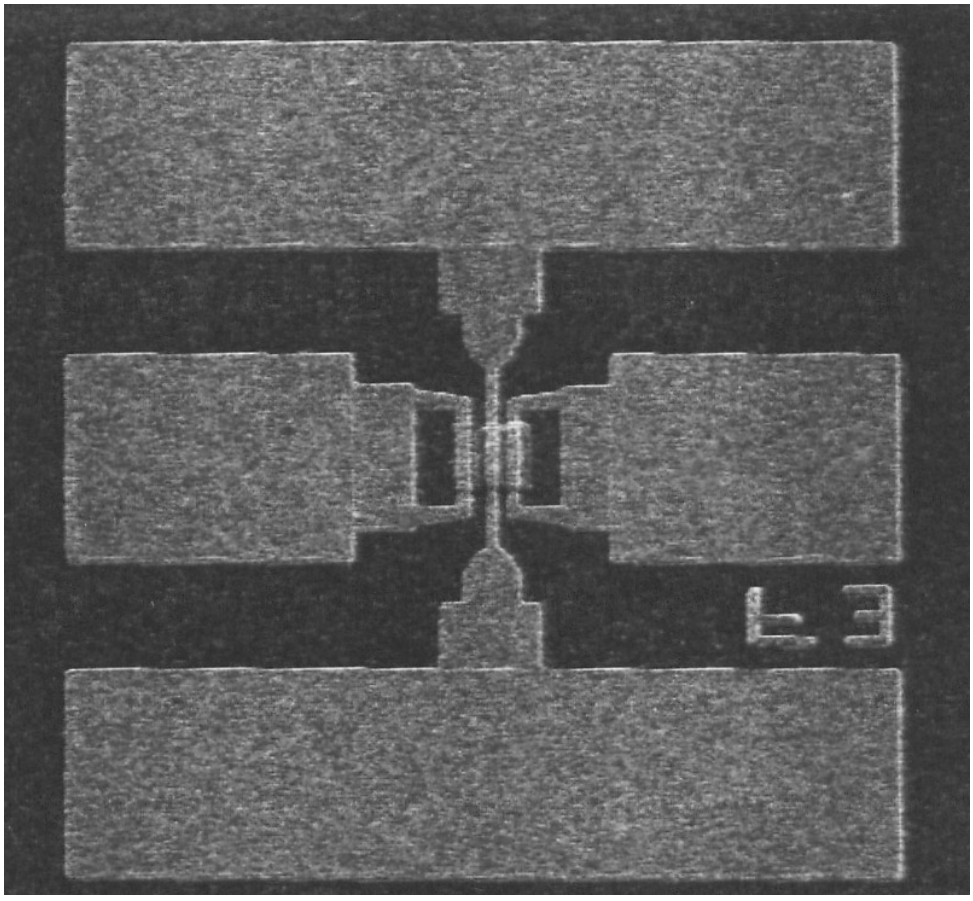


Figure 2.6 SEM image of HBT

Chapter 3

Use of WN_X as the Diffusion Barrier for Interconnect Copper Metallization of InGaP/GaAs HBTs

3.1 Introduction

In this chapter, we try to make interconnect copper metallization of InGaP/GaAs HBTs using WN_X as the diffusion barrier. Traditionally, GaAs devices such as metal semiconductor field-effect transistors (MESFETs), high electron mobility transistors (HEMTs), and heterojunction bipolar transistors (HBTs) use Ti as adhesion layer, and Au as the metallization metal for interconnect metal and transmission lines. The use of copper as the metallization metal has several advantages over gold such as lower resistivity, higher thermal conductivity, and lower cost. If Cu replaces Au as the interconnect metal for the HBTs, then the improvement in the electrical conductivity can increase the transmission speed of the circuits and the manufacturing cost will be substantially reduced. However, the use of copper interconnect for HBTs requires suitable diffusion barrier which is compatible with the HBT processes to prevent copper inter-diffusion into the GaAs substrate.

Generally, the n-type AuGe/Ni/Au and p-type Ti/Pt/Au or Pt/Ti/Pt/Au ohmic contacts are the most widely used structures for the fabrication of the GaAs based HBTs. The top layers of the ohmic structures are Au. From the phase diagrams of these materials systems, there are many possible intermetallic compounds in the Cu/Au binary system. Inter-diffusion of Cu and Au in the Cu/Au structure was observed at a temperature as low as 150 ℃ and a very rapid increase in the resistivity were observed at 250℃ [20]. Meanwhile, HBT is usually passivated with

plasma-enhanced chemical-vapor-deposited silicon nitride (PECVD-SiN) film, if Cu is in direct contact with the silicon nitride film of poor quality, a large amount of copper may diffuse through the microdefects of the PECVD-SiN films during the heat treatment of the metallization process and the leakage current will increase as a result of the copper diffusion [21]. Diffusion of copper through the ohmic contacts and silicon nitride film into the HBTs will cause the degradation of the electrical properties of the HBT devices. Therefore, a diffusion barrier between ohmic metal and copper and between silicon nitride and copper are mandatory for the use of copper as the interconnect metal for the GaAs HBTs. Tungsten nitride has high melting point, good thermal and chemical stability, and is a good diffusion barrier between Si and Cu. In addition, tungsten does not form intermetallic compound with Cu and Au as judged from the phase diagram. In this study, the thermal stabilities of $Cu/WN_X/Au$ and $Cu/WN_X/SiN$ film structures were investigated. And these materials systems were used to fabricate the InGaP/GaAs HBTs with copper interconnects. We are reporting for the first time the fabrication and electrical performance of the Cu-metallized InGaP/GaAs HBTs with WN_X as the diffusion barrier.

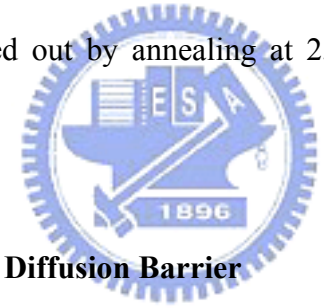
3.2 Experimental

The experiments in this study include two parts. The first part is the thermal stability study of the diffusion barrier. The stabilities of WN_X between Cu and Au and between Cu and silicon nitride were investigated. A WN_X film of 40-nm thickness was sputtered onto the Au/GaAs and SiN/GaAs samples respectively, and then 200-nm Cu film was subsequently sputtered on top of the WN_X films without breaking vacuum in a multitarget magnetron sputtering system to form $Cu/WN_X/Au$ and $Cu/WN_X/SiN$ multilayer structures. The WN_X films were deposited by

dc-magnetron reactive sputtering system using a W (99.99%) target reactively sputtered in the N_2/Ar mixture with 20% N_2 and 80% Ar. Prior to the sputtering, the chamber was pumped down to 1.6×10^{-6} Torr and the target was presputtered for 10 min in Ar gas. The flow rate of Ar gas was 24 sccm, and that of the N_2 gas was 4.8 sccm; the deposition rate of the WN_X films was 2.4 nm/min. The sputtering was performed at 200 W dc power with a total pressure of 7.6×10^{-3} Torr. The thickness of the WN_X film deposited was 40 nm. After sputtering deposition, the Cu/WN_X/Au and Cu/WN_X/SiN multilayer structures were annealed for 30 min at different temperatures in nitrogen ambient for material analysis. Scanning electron microscopy (SEM), X-ray diffraction (XRD), Auger electron spectroscopy (AES), and sheet resistance were used for phase identification and the study of the interfacial reactions.

The second part is the copper metallized HBT device fabrication using WN_X as the diffusion barrier and the electrical performance evaluation of these devices. The InGaP/GaAs HBTs used in this work were grown by metal organic chemical vapor deposition (MOCVD) on semi-insulating (100) GaAs substrates. The layer structure consists of (from bottom to top) a n^+-GaAs subcollector (500 nm, 4×10^{18} cm^{-3}), a n^--GaAs collector (700 nm, 2×10^{16} cm^{-3}), a p^+-GaAs base (83 nm, 3×10^{19} cm^{-3}), an n-InGaP emitter (50 nm, 3×10^{17} cm^{-3}), and an n^+-GaAs cap (200 nm, 3×10^{18} cm^{-3}). The HBT devices were fabricated using a standard triple mesa process. The InGaP and GaAs layers were etched by HCl/H_3PO_4 and $H_3PO_4/H_2O_2/H_2O$ solutions respectively. Alloyed AuGe/Ni/Au, non-alloyed Pt/Ti/Pt/Au, and alloyed AuGe/Ni/Au ohmic metal systems were used for the emitter, base, and collector contacts, respectively. Device passivation was realized with PECVD silicon nitride. After opening the connect via on the nitride film, the diffusion barrier WN_X (40 nm), interconnect Cu (400 nm) metal, and WN_X (10 nm) were sequentially deposited by dc-magnetron reactive sputtering through the collimator over patterned resist. The

bulk of the resist and metal were then removed by a wet solvent lift-off process, followed by a high pressure DI water rinse to remove the residues. The top layer WN_X served as a protective layer to prevent Cu film oxidation. The dimension of the emitter area of the HBT was 3 μm × 20 μm. The HBTs with conventional Ti (50 nm)/Au (400 nm) interconnect metal were also prepared for comparison. The structure of the InGaP/GaAs HBTs in this study is shown in Figure 3.1. The DC current-voltage (I-V) characteristics of the HBT devices were measured by HP4142B. Both the 3 × 20 μm emitter area HBT devices with gold interconnects and the devices with copper interconnects were stressed using current-accelerated test and high-temperature thermal annealing test for reliability evaluation and comparison. The high current test was performed at high current density of 140 kA/cm^2 for 55 hours. The thermal test were carried out by annealing at 250℃ for 25 hours in nitrogen ambient .



3.3 Material Stability of the Diffusion Barrier

There are two WN_X based multilayer structures (Cu/WN_X/Au and Cu/WN_X/SiN/GaAs) in the copper metallized HBTs as shown in Figure 3.1 The stability of these material systems have to be studied before applying them to the device fabrication. The stabilities of these material systems were studied using SEM, AES, XRD and sheet resistances analyses. The first multilayer structure studied was Cu/WN_X/Au. Figure 3.2 shows the AES depth profiles of the Cu/WN_X/Au samples as-deposited and after 400℃ and 450℃ annealing for 30 min. As can be seen from Figure 3.2(b), there was no atomic inter-diffusion between Cu and Au after 400℃ annealing. However, after 450℃ annealing for 30 min, the results in Figure 3.2(c) showed that copper started to diffuse into the gold layer. The SEM micrographs of the

surface morphologies of the Cu/WN_X/Au samples as-deposited and after 450 ℃ annealing were shown in Figure 3.3. As can be seen in Figure 3.3(a), the surface morphology for the as-deposited sample was very smooth, however, after 450℃ 30 min. annealing, the surface morphology started to change and became very rough due to material inter-diffusion and new phase formation as shown in Figure 3.3(b). Additional evidence was obtained from the XRD analysis. Figure 3.4 shows the XRD results of the Cu/WN_X/Au samples as-deposited and after annealing from 350℃ to 450℃ for 30 min. From the XRD data, it is clear that the diffraction peaks of Au, Cu and W_2N remained unchanged after 400 ℃ annealing, suggesting that the Cu/WN_X/Au structure was still quite stable after 400℃ annealing. However, after 450℃ annealing, additional peaks which were identified as Cu_3Au_2 and CuAu diffraction peaks were found. The formation of Cu_3Au_2 and CuAu after 450℃ annealing suggested that Cu atoms had diffused through the WN_X layer into the Au layer.

The second multilayer structure studied was Cu/WN_X/SiN/GaAs. Figure 3.5 shows the sheet resistances of the samples as-deposited and after 400℃ to 600℃ annealing for 30 min. The sheet resistance of the Cu/WN_X/SiN/GaAs film structure decreased after annealed at 400℃~550℃, which was probably due to the grain growth and the decrease of the defect density in the Cu and WN_X films after thermal annealing. After 600 ℃ annealing, the sheet resistance drastically increased, suggesting that atomic diffusion and inter-atomic reactions had occurred between these layers. Additional evidence showing that the Cu/WN_X/SiN/GaAs multiple layer was stable up to 550℃ annealing was obtained from the AES depth profile analysis data shown in Figure 3.6. Figure 3.6(a) is data of the as deposited films, Figure 3.6(b) is the data of these films after 550℃ 30 min annealing. As can be seen from Figure 3.6(b), there was no noticeable diffusion of Cu into the SiN layer after annealing at

550℃ for 30 min. However, after 600℃ annealing for 30 min, Cu atoms started to diffuse through the WN_X layer into the SiN layer as can be seen in Figure 3.6(c). In addition, Figure 3.7 shows the XRD results of the Cu/WN_X/SiN samples as-deposited and after annealed from 500℃ to 600℃ for 30 min. The XRD data clearly shows that the peaks of Cu, W_2N, and SiN remained unchanged up to 550℃ annealing, indicating that the Cu/WN_X/SiN structure remained quite stable up to 550℃. After annealing at 600℃, peaks from new phases of $Cu_{0.83}Si_{0.17}$, $Cu_{16}Si_4$, Cu_5Si , W, and W_2N were identified, suggesting that the reactions between the SiN and the Cu metallization layer had occurred. From the data shown above, it is clear that the Cu/WN_X/Au material system is quite stable up to 400℃ annealing and the Cu/WN_X/SiN material system is quite stable up to 550℃ annealing.

3.4 Device Electrical Characteristics

WN_X diffusion barrier was applied to the InGaP/GaAs HBTs with interconnect copper metallization. InGaP/GaAs HBTs with traditional Ti/Au based interconnect were also processed on half of the same wafer for comparison. The Au thickness for the Au interconnects is the same as the Cu thickness of the Cu interconnects (400 nm). Figure 3.8 shows the typical common emitter characteristics for the small emitter area (3×20 μm^2) HBTs, in this figure, one curve is for the HBT with Cu-metallized interconnects and WN_X diffusion barrier and the other curve is for the HBT with Au metallized interconnects. From Figure 3.8, these two devices show similar knee voltage and offset voltage, which indicates that there was no stress effect for the WN_X/Cu/WN_X films and the quality of the multilayer materials was quite good. The common emitter current gain was around 140 for both cases. Gummel plots of the HBTs with Cu and Au interconnect metallization were also compared. The results are

shown in Figure 3.9. The two HBTs showed similar behavior, but the HBT with Cu interconnect metal showed slightly higher base and collector currents than the HBT with Au interconnect metal in the high current and high base-emitter voltage region.

To test the reliability of the WN_X as the diffusion barrier for the Cu-metallized HBTs, both copper and gold metallized HBTs with 3 × 20 μm emitter area were subjected to current accelerated stress test with high current density of 140 kA/cm^2. It was much higher than 25 kA/cm^2 required for normal device operation and the purpose is to shorten the stress time so that the stress tests could be performed at wafer level without using any package and the results could be obtained in a few hours [22]. Figure 3.10 plots the current gain (β) of the two kinds of HBTs after stressed at the high current density of 140 kA/cm^2 at V_{CE} of 2 V for a period of 55 hours. Under this test condition, the estimated junction temperature, T_j was about 300 ℃. Both measurements were made at an ambient room temperature of T_A = 25 ℃. Figure 3.11 shows the typical Gummel plots before and after the current accelerated stress. It can be seen from Figure 3.11(a) that the Cu-metallized HBT device showed only very little change after stress test and the current gain was still higher than 100 after the stress. Also, almost no significant change in the base and collector ideality factors and no shift in the turn-on voltage were observed. Besides, the collector current (I_C) change was around 3 % at 25 kA/cm^2 after the current accelerated stress for the Cu-metallized HBT. On the other hand, the emitter and base current of the Au metallized HBT showed significant degradation at high base-emitter voltage as can be seen from Figure 3.11(b). The change in the collector current at 25 kA/cm^2 was around 20 %. It was caused by the increase in the emitter resistance after accelerated stress test. This may due to the fact that the heat dissipation of the Cu-metallized HBT is better than that of the Au metallized HBT, so the ohmic structure of the Au metallized HBT is easier to degrade during current accelerated stress. This

phenomenon was not found for the Cu-metallized HBTs.

To study the thermal stability of the WN_X diffusion barrier, the 3 × 20 μm emitter area HBTs with Cu metallization were annealed at 250℃ for 25 hours and tested for the electrical performance. For comparison, the Au metallized HBTs were also annealed at the same conditions and tested. Figure 3.12(a) shows the common emitter I-V curves before and after annealing for the copper metallized HBT with WN_X diffusion barrier and Figure 3.12(b) shows the corresponding common emitter I-V curves before and after annealing for the gold metallized HBT. As can be seen from the data of Figure 3.12, there was no change in the offset voltage, knee voltage, and saturation current after annealing for both types of HBTs. It suggested that there was no ohmic degradation and copper diffusion for the copper metallized HBTs using WN_X as the diffusion barrier. Figure 3.13 shows the Gummel plots before and after 250℃, 25 hours annealing for both the copper metallized and gold metallized devices. The base and collector ideality factors for both HBTs showed little change after the thermal annealing and the base leakage current of the two types of devices remained in the same order. It suggested that no additional degradation mode had occurred and that no copper diffusion into the active device region after the thermal stress, these results were consistent with the material analysis results.

3.5 Conclusion

Use of WN_X as the diffusion barrier for the interconnect copper metallization of InGaP/GaAs HBTs is reported for the first time. In this study, InGaP/GaAs HBTs with Cu/WN_X metallization layers were fabricated and the electrical performance were evaluated. From SEM, XRD, AES depth profile, and sheet resistance studies, the Cu/WN_X/Au and Cu/WN_X/SiN metallization layers were very stable after annealing at

400℃ and 550℃ respectively. After applying the Cu/WN_X metallization layers to the HBTs, the common emitter I-V curves of these copper metallized HBTs showed similar electrical characteristics as those for HBTs metallized with conventional Ti/Au layers. Both current accelerated stress test (140 kA/cm^2 stress for 55 hours) and thermal stress test (annealing at 250 ℃ for 25 hours) were performed on the Cu/WN_X metallized HBTs, almost no change in the electrical characteristics were observed for these devices after the tests. The results showed that the Cu/WN_X interconnect layers were quite stable and that WN_X can be used as the diffusion barrier for the interconnect copper metallization for the InGaP/GaAs HBTs.

FIGURES

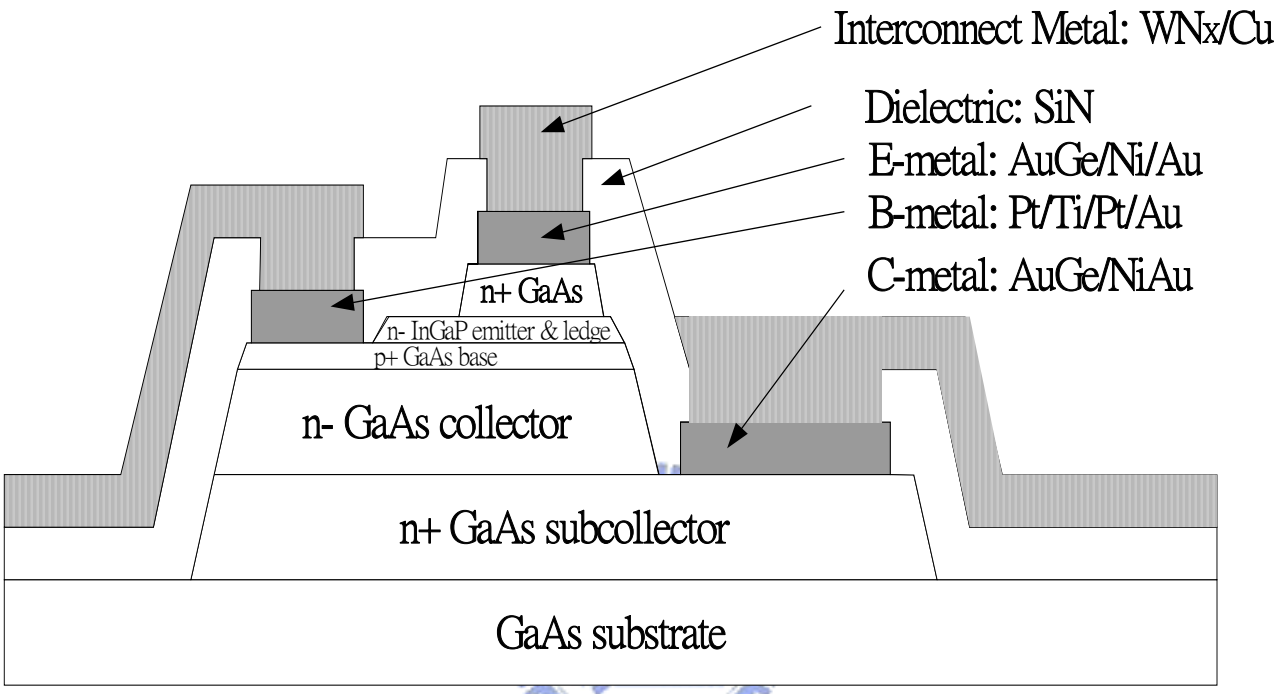


Figure 3.1 Cross section of the InGaP/GaAs HBT with interconnect Cu metallization.

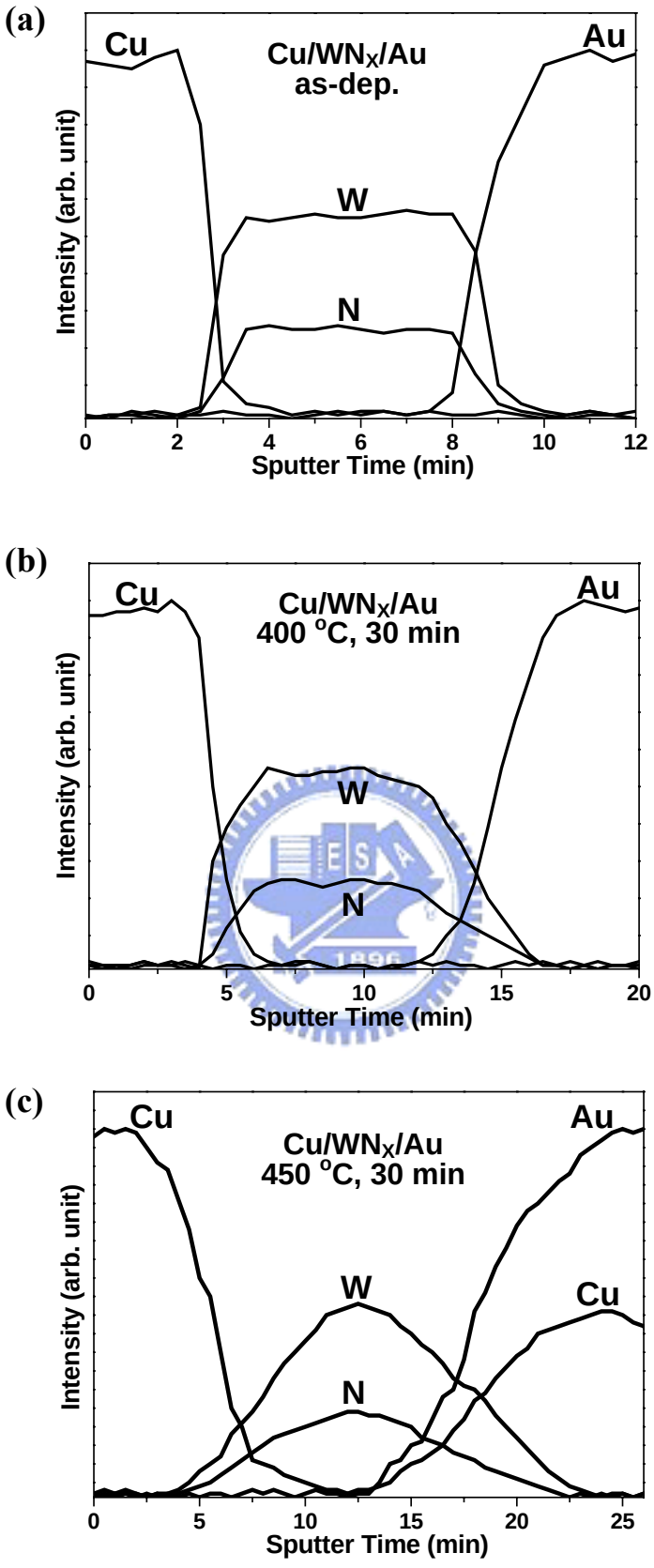


Figure 3.2 AES depth profiles of the $Cu/WN_X/Au$ samples (a) as deposited; (b) after 400 ℃ annealing; and (c) after 450 ℃ annealing.

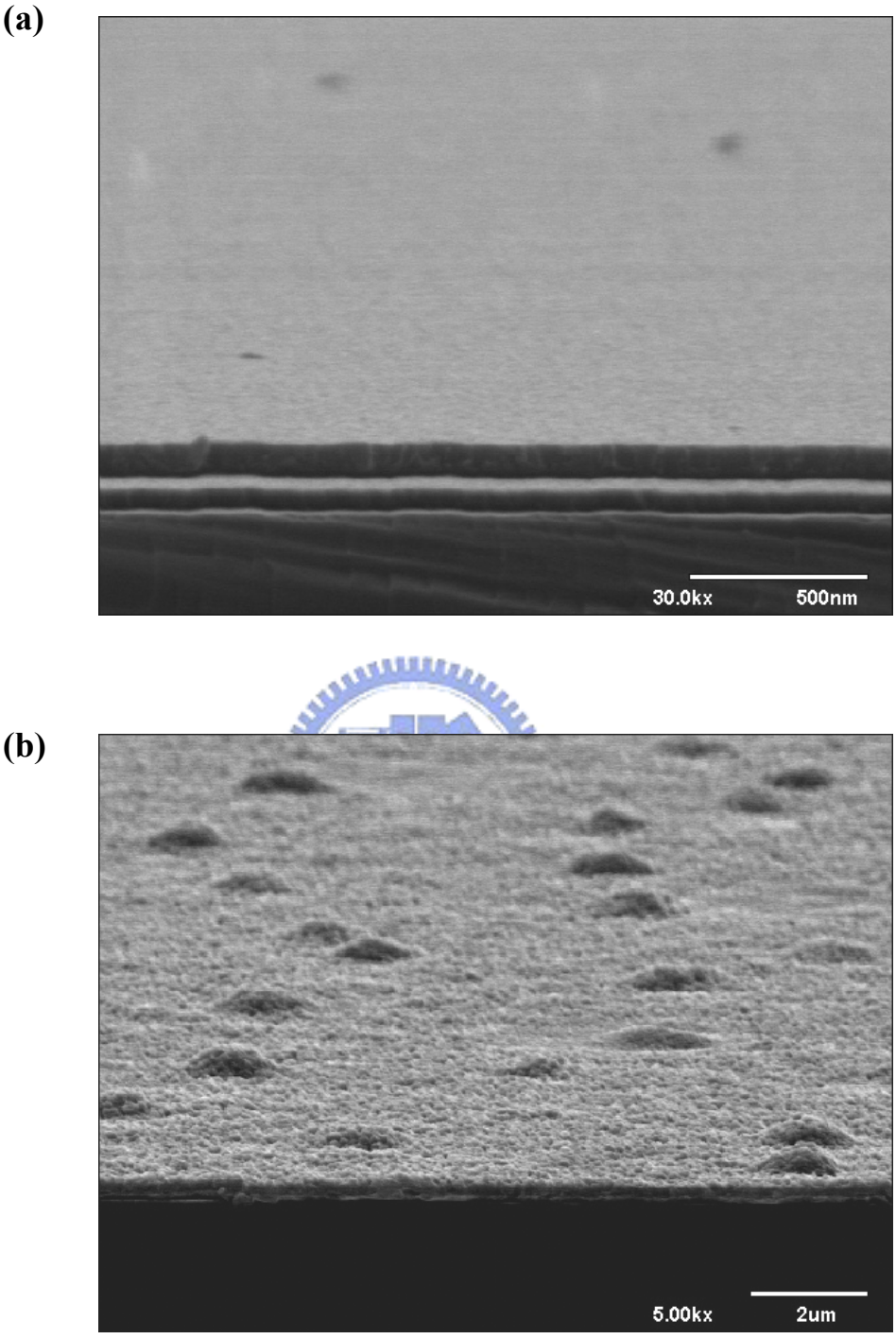


Figure 3.3 SEM images of the Cu/WN_X/Au samples (a) as deposited and (b) after 450 ℃ annealing.

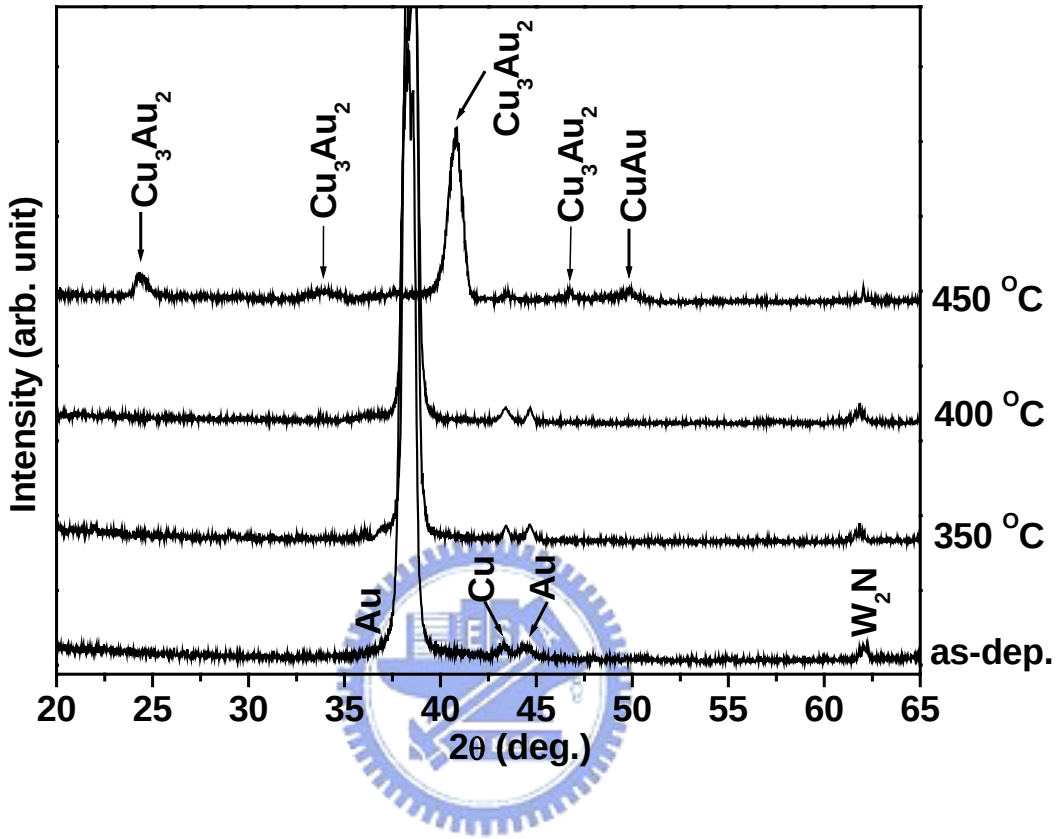


Figure 3.4 XRD patterns of the Cu/WN_X/Au samples as deposited and after annealing at various temperatures.

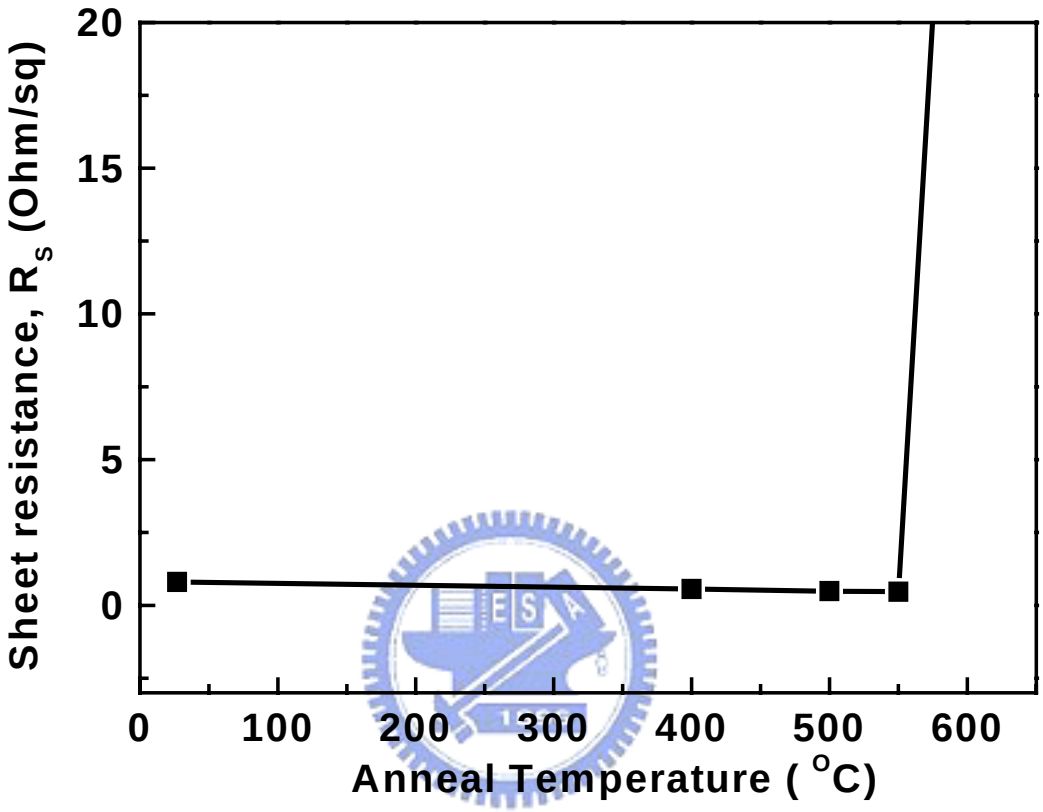


Figure 3.5 Sheet resistance of the Cu/WN_X/SiN/GaAs samples as deposited and after annealing at various temperatures.

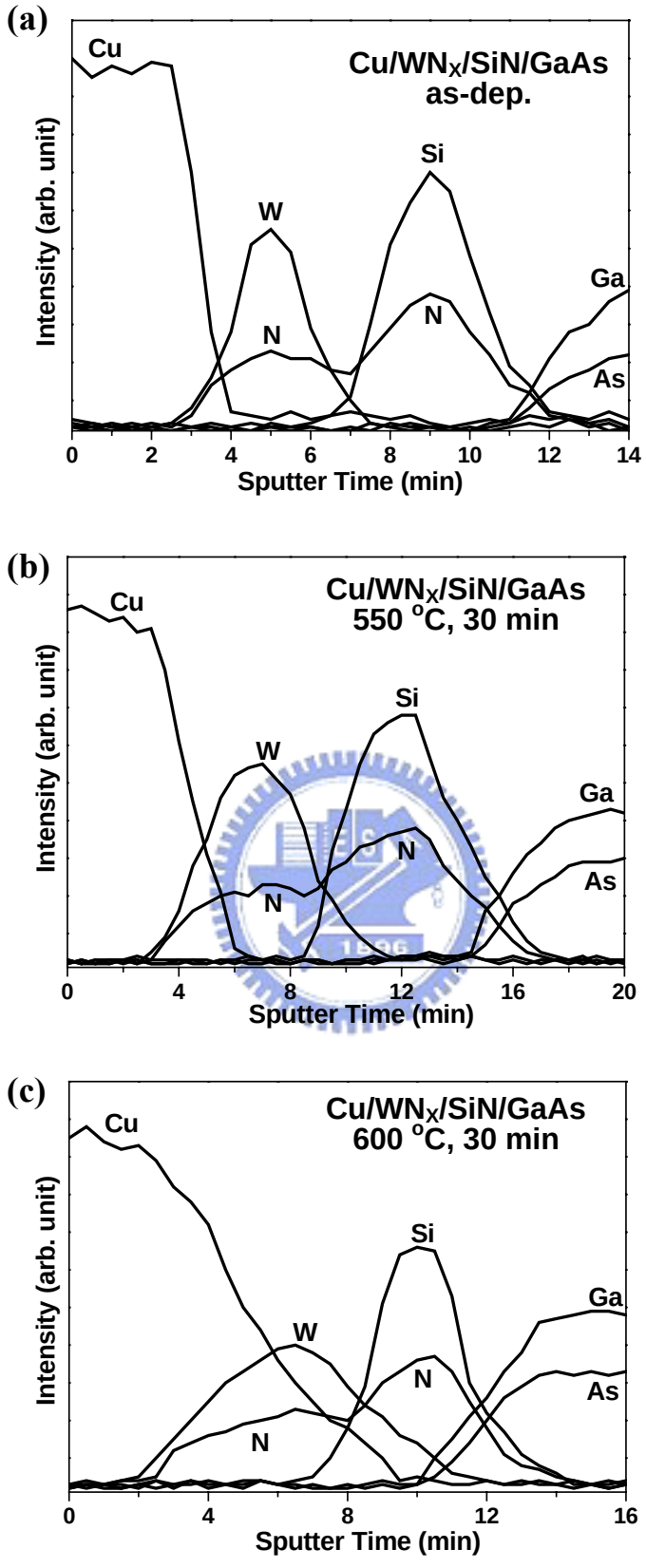


Figure 3.6 AES depth profiles of the Cu/WN_X/SiN/GaAs samples (a) as deposited; (b) after 550 ℃ annealing; and (c) after 600 ℃ annealing.

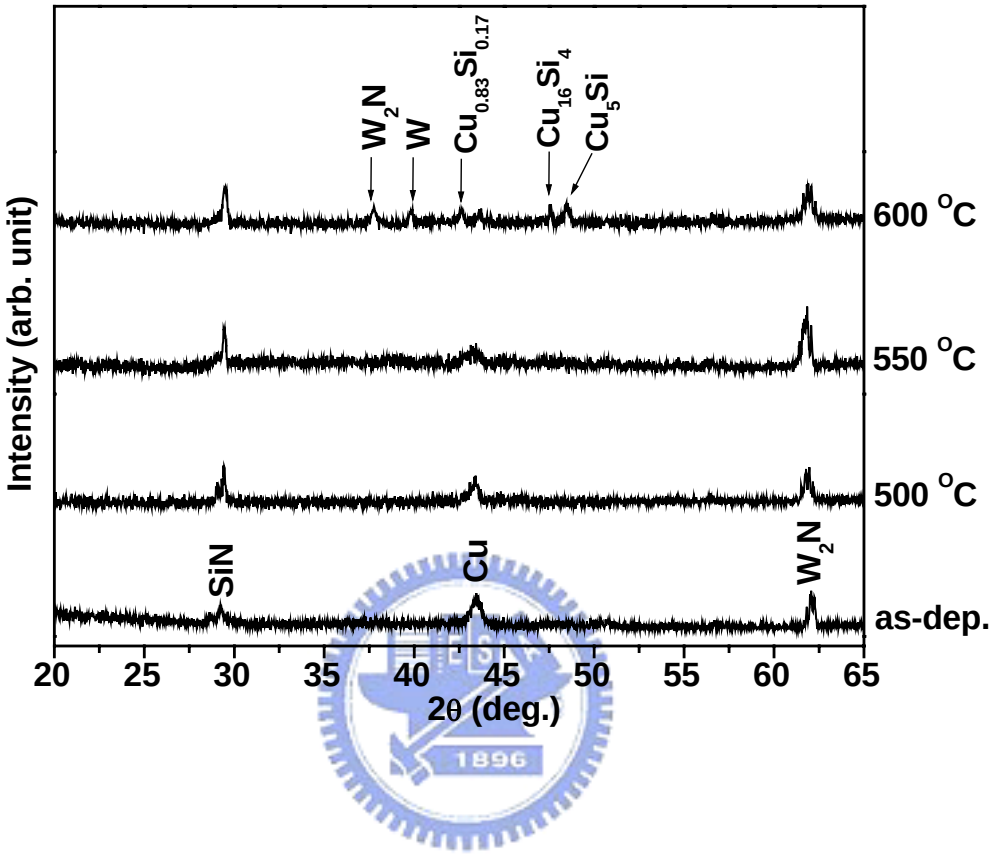


Figure 3.7 XRD patterns of the Cu/WN_X/SiN samples as deposited and after annealing at various temperatures.

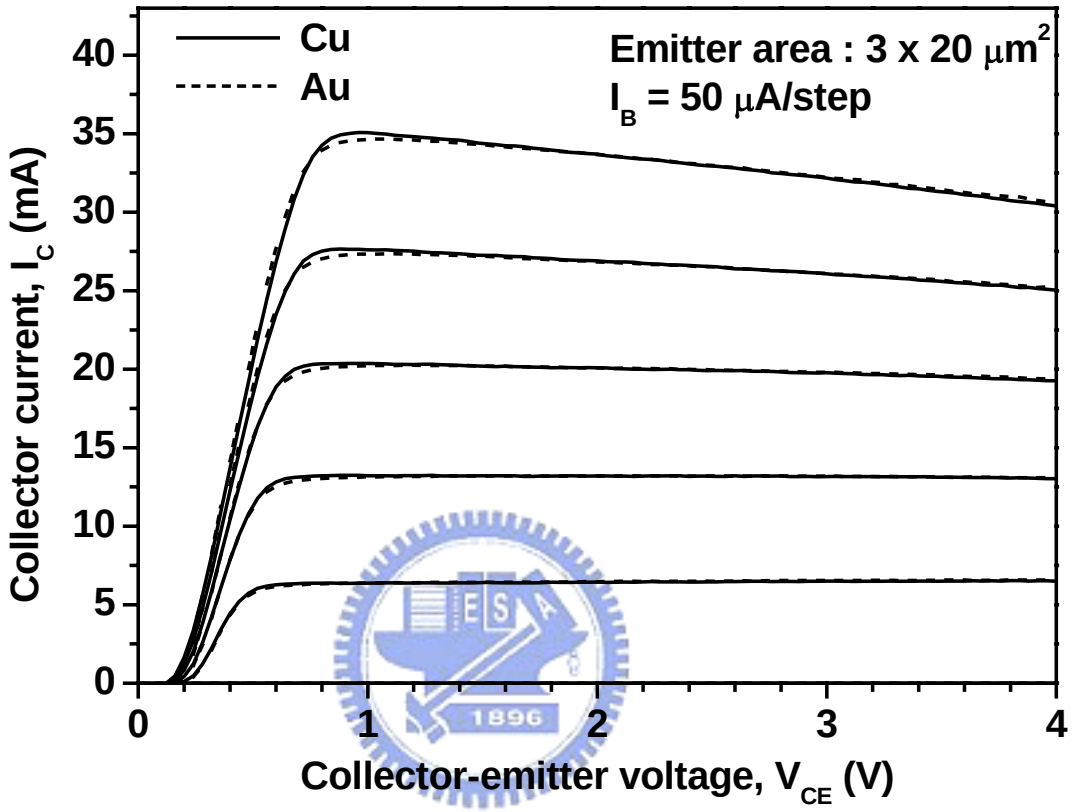


Figure 3.8 Comparison of the typical I_C-V_{CE} characteristics for the emitter area (3×20 μm^2) HBTs with Cu and with Au interconnect metallizations.

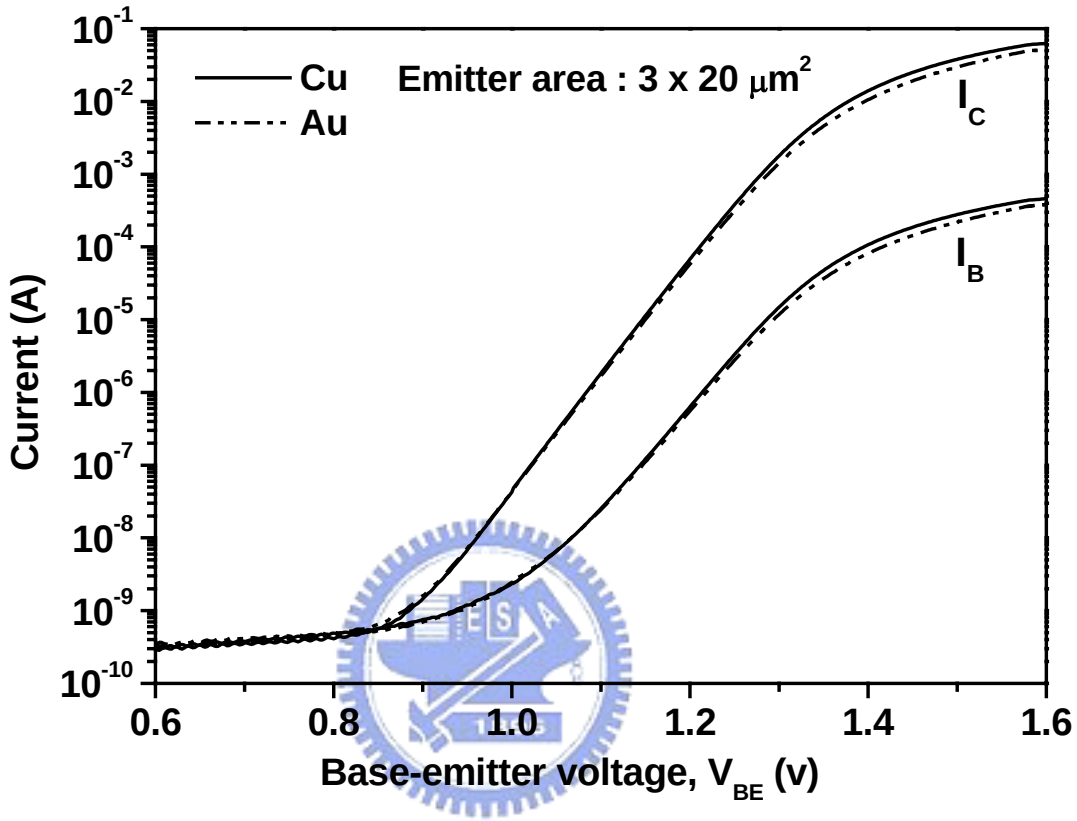


Figure 3.9 Comparison of the Gummel plots for the emitter area (3×20 μm^2) HBT with Cu and with Au interconnect metallization.

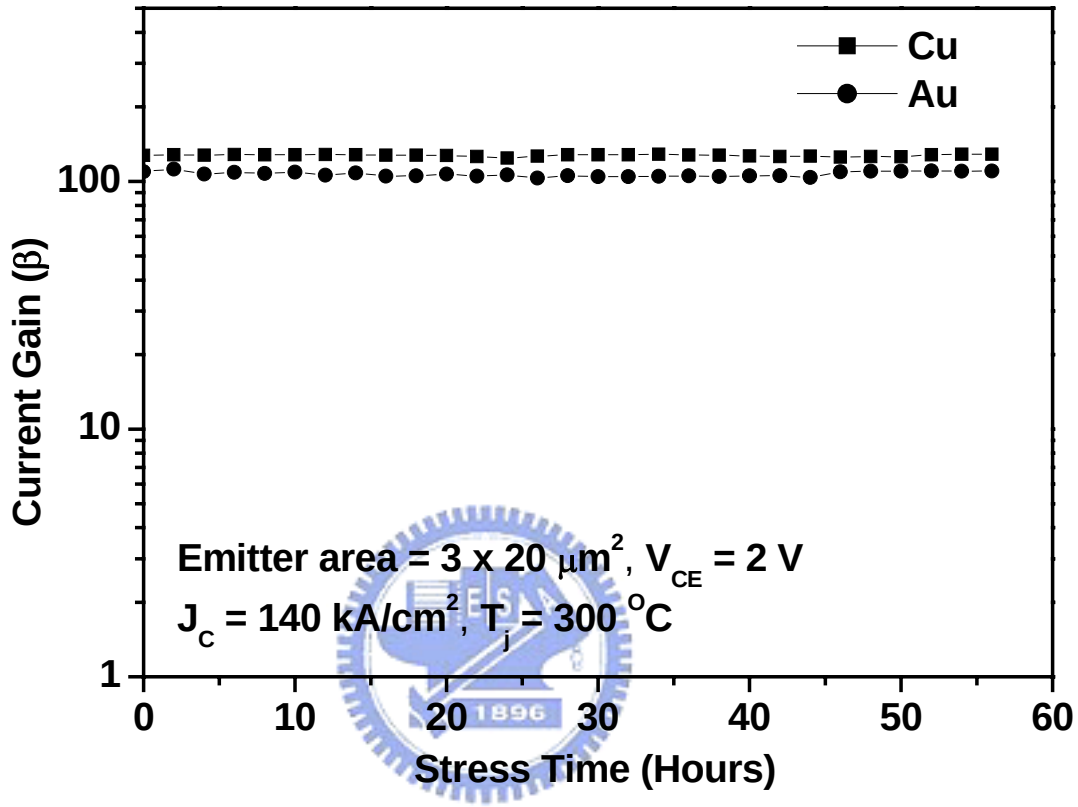


Figure 3.10 Current gain as a function of the stress time at a constant I_B for the emitter area (3×20 μm^2) HBTs with Cu and Au interconnect metallization.

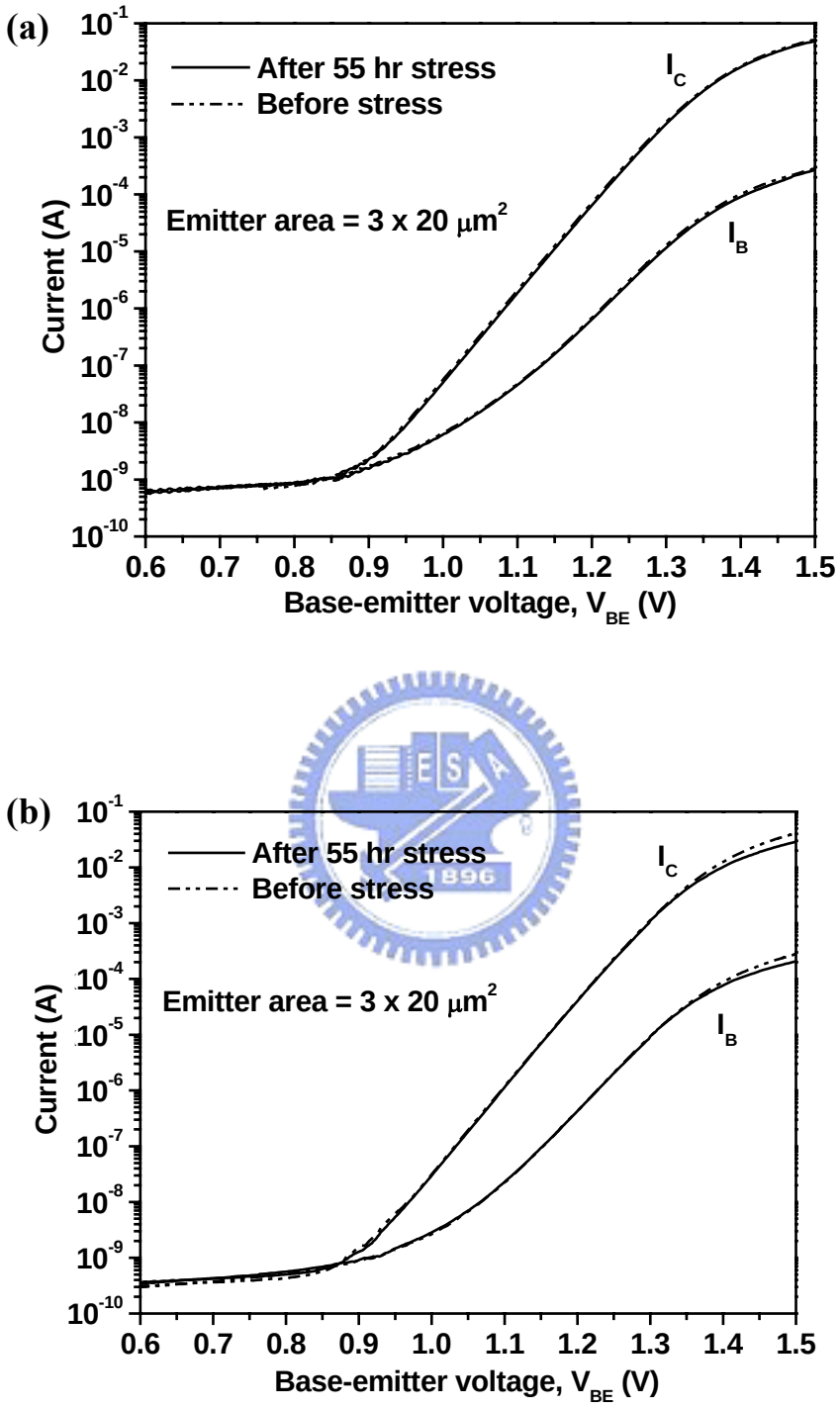


Figure 3.11 Gummel plots measured before and after 55 hours current accelerated stress test with high current density of 140 kA/cm^2 for the emitter area 3×20 μm^2 HBT devices (a) with Cu interconnect metallization and (b) with Au interconnect metallization.

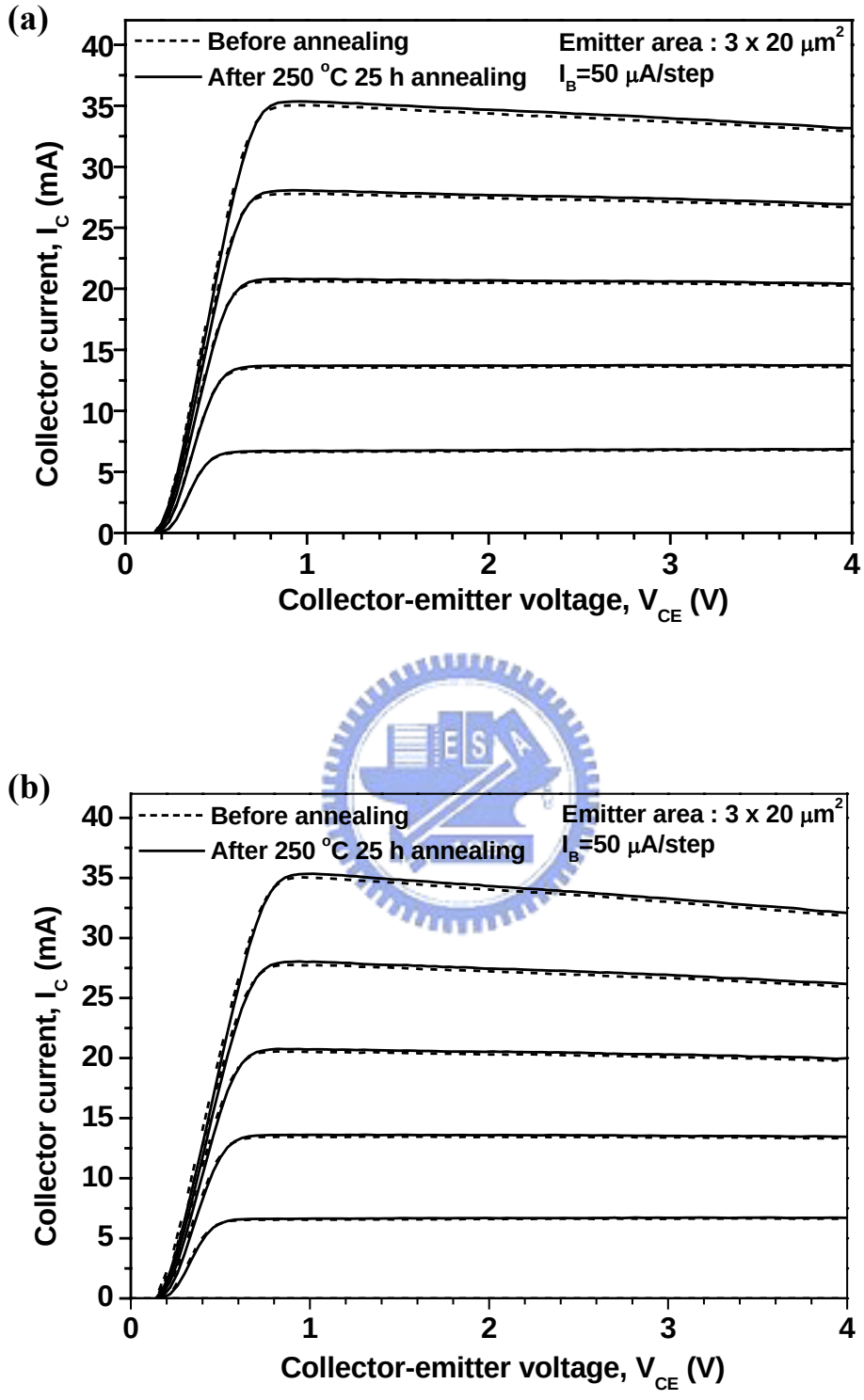


Figure 3.12 Common emitter I-V curves measured before and after 250 ℃ 25 hours annealing for the emitter area 3×20 μm^2 HBT devices (a) with Cu interconnect metallization and (b) with Au interconnect metallization.

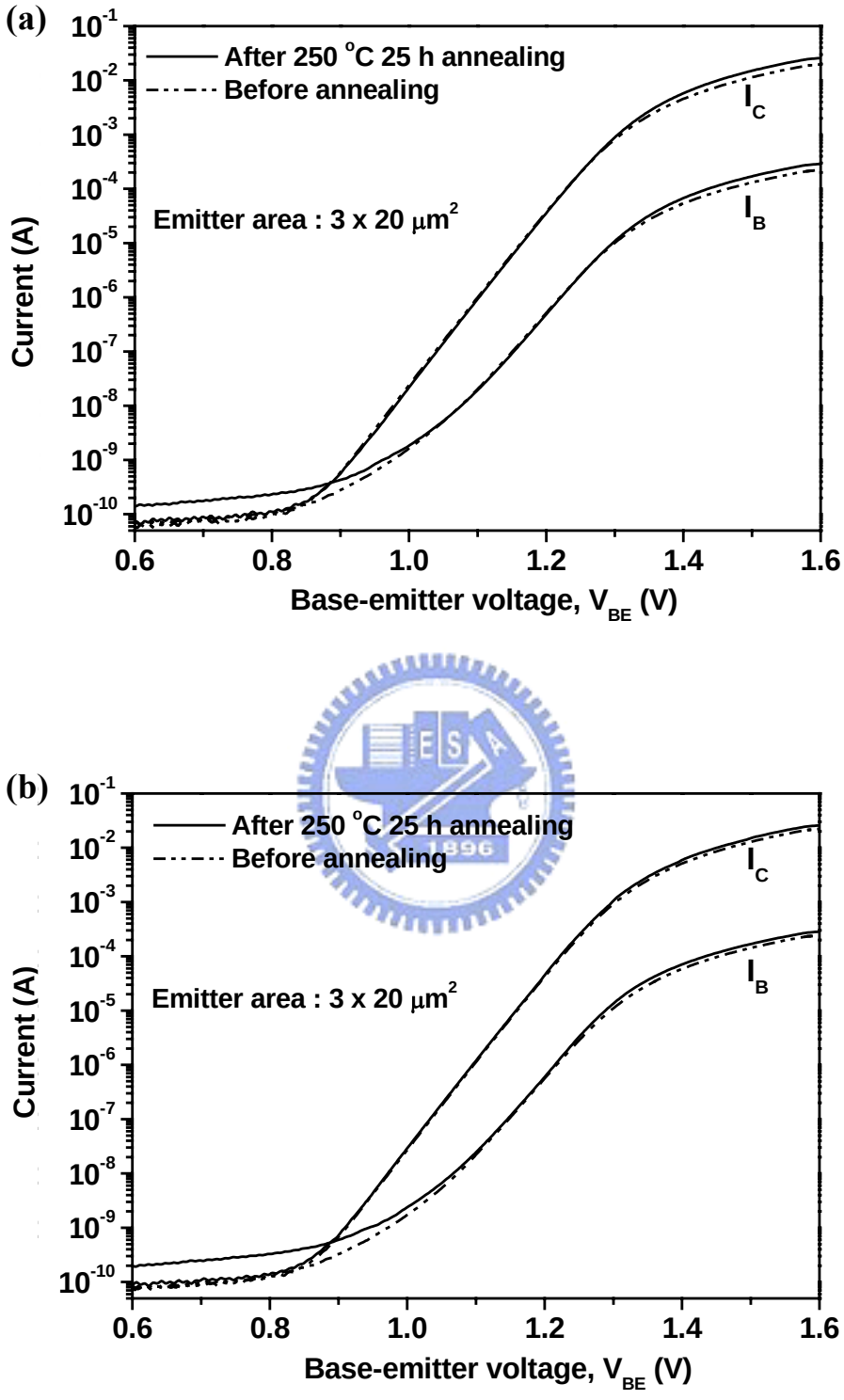


Figure 3.13 Gummel plots measured before and after 250 ℃ 25 hours annealing for the emitter area 3×20 μm^2 HBT devices (a) with Cu interconnect metallization and (b) with Au interconnect metallization.

Chapter 4

Gold-Free Fully Cu-Metallized InGaP/GaAs Heterojunction Bipolar Transistor

4.1 Introduction

In the last chapter, we have demonstrated interconnect copper metallization of InGaP/GaAs HBTs using WN_X as the diffusion barrier. In this chapter, we try to make gold-free fully Cu-metallized InGAP/GaAs HBTs. And this is the first time fully Cu metallized GaAs HBT is demonstrated.

Conventionally, n-type AuGe/Ni/Au and p-type Pt/Ti/Pt/Au ohmic contacts, and Ti/Au interconnect metals have been the most widely used metallization structures for the fabrication of GaAs-based heterojunction bipolar transistors. If Cu is replaced with Au as the metallization metal for HBTs, then the resulting improvement in the electrical conductivity can increase the transmission speed of the circuits and the heat will also be dissipated. In our previous studies, we demonstrated "back-surface" copper metallization in GaAs metal semiconductor field-effect transistors (MESFETs) using TaN as the diffusion barrier [10] and the use of a copper air-bridge in low-noise GaAs high-electron-mobility transistors (HEMTs) using WN_X as the diffusion barrier [12]. On the other hand, copper is difficult to dry etch due to the lack of volatile compounds. To make fully Cu GaAs HBTs, there were two items must take into consideration. One is the n-type and p-type ohmic contacts, the other is the thermal stability of the diffusion barrier. In this study, we use PdGe and Pt/Ti/Pt/Cu as n^+-type and p^+-type ohmic contact metals, respectively, and use Ti/Pt/Cu as interconnect metals with platinum as the diffusion barrier to fabricate the Au-free, fully Cu-metallized HBTs using lift-off technology. Platinum has a high melting point, and

it is a good diffusion barrier for preventing Au from diffusing into the conventional GaAs Schottky (Ti/Pt/Au) and ohmic (Pt/Ti/Pt/Au) structures. In this study, the thermal stabilities of the Ti/Pt/Cu structures were investigated. Furthermore, this material system was used to fabricate InGaP/GaAs HBTs. Here, we are reporting for the first time the fabrication and electrical performance of Au-free, fully Cu-metallized InGaP/GaAs HBTs with platinum as the diffusion barrier.

4.2 Experimental

The experiments in this study include three parts. First, the n-type and p-type multilayer ohmic contacts on heavily doped GaAs should be studied. Second, the thermal stability of the diffusion barrier was discussed. After the completion of the ohmic contact and the diffusion barrier thermal stability studies, the Cu multilayer structures were applied on the GaAs HBTs, and the Au-free fully Cu-metallized GaAs HBTs were realized.

The first part is the ohmic contact study. The specific contact resistances of n^+-GaAs/Pd (50 nm)/Ge (125 nm) and p^+-GaAs/Pt (5 nm)/Ti (50 nm)/Pt (60 nm)/Cu (150 nm) were carried out by transmission line method (TLM). The TLM patterns were fabricated by I-line photolithography. After the metal evaporation, the samples were immersed into ACE and IPA with the common lift-off process. The n^+-GaAs/Pd/Ge samples were than annealed at various temperatures from 300^{o}C to 400 ℃ by rapid thermal annealing (RTA) method for 30 seconds, and the p^+-GaAs/Pt/Ti/Pt/Cu samples were annealed at various temperatures in an Ar-ambient tube furnace for 10 minutes.

The second part is the thermal stability study of the diffusion barrier. The thermal stability of the Ti/Pt/Cu structure must to be studied prior to applying it to the GaAs

HBTs fabrication. The Ti/Pt/Cu multilayer structure was deposited by e-gun evaporator. After deposition, the multilayer structures were annealed for 30 min at different temperatures in Ar-ambient for material analysis. Scanning electron microscopy (SEM), X-ray diffraction (XRD), and sheet resistance were used for the study of the interfacial reactions.

The third part is the fabrication of the gold-free fully copper-metallized GaAs HBT. The InGaP/GaAs HBTs used in this work were grown by metal organic chemical vapor deposition (MOCVD) on semi-insulating (100) GaAs substrates. The layer structure consists of (from bottom to top) an n^+-GaAs subcollector (600 nm, 5×10^{18} cm^{-3}), an n^--GaAs collector (650 nm, 4×10^{16} cm^{-3}), a p^+-GaAs base (120 nm, 2×10^{19} cm^{-3}), an n-InGaP emitter (85 nm, 2×10^{17} cm^{-3}), and an n^+-GaAs cap (100 nm, 5×10^{18} cm^{-3}). The HBT devices were fabricated using a standard triple mesa process. The InGaP and GaAs layers were etched with HCl/H_3PO_4 and $H_3PO_4/H_2O_2/H_2O$ solutions, respectively. Alloyed PdGe, non-alloyed Pt/Ti/Pt/Cu, and alloyed PdGe gold-free ohmic metal systems were used for the emitter, base, and collector contacts, respectively. Device passivation was realized with PECVD silicon nitride. After opening the connecting via on the nitride film, the Ti adhesion layer (30 nm), the Pt diffusion barrier (60 nm), and the Cu interconnect metal (400 nm) were sequentially deposited using an e-gun evaporator over a patterned resist. The bulk of the resist and metal were then removed by a wet-solvent lift-off process, followed by a high-pressure DI water rinse to remove the residues. Finally, silicon nitride (10 nm) was deposited as a protective layer on the top of the device to prevent Cu film oxidation. The dimensions of the emitter area of the HBT are 4 μm × 20 μm. The structure of the InGaP/GaAs HBTs in this study is shown in Figure 4.1. The DC current-voltage (I-V) characteristics of the HBT devices were measured using a HP4142B. The devices were stressed using a current-accelerated test and a

high-temperature thermal annealing test for reliability evaluation. The high-current test was performed at a high current density of 140 kA/cm^2 for 24 h. The thermal test was carried out by annealing at 250℃ for 24 h in nitrogen ambient .

4.3 Ohmic Contact Result

The specific contact resistances of the n^+-GaAs/Pd/Ge annealed at 300℃ to 400 ℃ for 30 seconds by RTA method was shown in Figures 4.2. It can be seen from Figure 4.2 that the contact resistance of n^+-GaAs/Pd/Ge structure reached the lowest value 1×10^{-6} Ω-cm^2 at annealing temperature of 350℃ 30s. For the p-type ohmic contact, the specific contact resistance of p^+-GaAs/Pt/Ti/Pt/Cu was shown in Figure 4.3. As can be seen in figure 4.3, the resistance for the as-deposited sample was 1.08×10^{-6} Ω-cm^2. After 350℃ 10 min annealing, the contact resistance reached the lowest value 9.37×10^{-7} Ω-cm^2. The contact resistance of the n^+-GaAs/Pd/Ge and p^+-GaAs/Pt/Ti/Pt/Cu were of the same order as that of the traditional n^+-GaAs/AuGe/Ni/Au and p^+-GaAs/Pt/Ti/Pt/Au ohmic structure.

4.4 Thermal Stability of Ti/Pt/Cu Multilayers

To study the diffusion barrier properties of platinum, the Ti (50 nm)/Pt (60 nm)/ Cu (400 nm) films were first evaporated onto a blank GaAs wafer using an e-gun evaporator and then annealed for 30 min at different temperatures in nitrogen ambient for material analysis. X-ray diffraction (XRD) analysis, and sheet resistance measurements were used to monitor the interfacial reactions. Figure 4.4 shows the sheet resistances of the samples as-deposited and after annealing at 300℃ to 450℃ for 30 min. The sheet resistance of the GaAs/Ti/Pt/Cu film structure increased

markedly after annealing at 400℃, suggesting that atomic diffusion and interatomic reactions had occurred between these layers at this temperature. Additional evidence showing that the GaAs/Ti/Pt/Cu multiple layers were stable during annealing up to 350℃ was obtained from the XRD data. Figure 4.5 shows the XRD results of the Ti/Pt/Cu samples as-deposited and after annealing from 300℃ to 400℃ for 30 min. The XRD data clearly shows that the peaks corresponding to Cu, Pt, and Ti remained unchanged during annealing up to 350℃, indicating that the Ti/Pt/Cu structure remained quite stable up to 350℃. However, after annealing at 400℃, additional peaks which were identified as Cu_4Ti diffraction peaks appeared and the Ti and Pt peaks disappeared. The disappearance of the Ti and Pt layers was due to the inter-diffusion of atoms. The Ti layer (50 nm) and the Pt layer (60 nm) were destroyed by the inter-diffusion which resulted in the disappearance of the Ti and Pt peaks. The formation of Cu_4Ti after annealing at 400℃ suggested that Cu atoms had diffused through the Pt layer and reacted with the Ti layer. From the data shown above, it was evident that the Ti/Pt/Cu material system was quite stable during annealing up to 350 ℃.

4.5 Device Electrical Characteristics

HBTs with conventional n-type ohmic metal (AuGe/Ni/Au), and p-type ohmic metal (Pt/Ti/Pt/Au) contacts, and interconnect metal (Ti/Au) were also processed on half of the same wafer for a comparative understanding of the material system. The specific contact resistance of the as-deposited nonalloyed p^+-GaAs/Pt/Ti/Pt/Cu HBT was 1.08×10^{-6} Ω-cm^2 and that of the conventional p-GaAs/Pt/Ti/Pt/Au HBT was 1.92×10^{-6} Ω-cm^2. The contact resistance of the Cu based electrode was of the same order as that of the Au-based electrode. Figure 4.6 shows the typical common emitter

characteristics for the 4×20-μm-emitter-area HBTs in this figure, one curve corresponds to an Au-free, fully-Cu-metallized HBT and the other curve corresponds to a conventional Au-metallized HBT. In Figure 4.6, these two devices showed similar knee voltages and offset voltages. We did not observe an increase in the knee voltage or the decay of the collector current, and neither did we observe any film peeling problem, which indicates that there was no stress effect in the Cu-metallized films and the quality of the multilayer materials was reasonably good. The common emitter current gain was approximately 150 for both cases. Figure 4.7 shows the Gummel plots of the HBTs with the traditional Au HBT and Au free fully Cu HBT. The two HBTs also showed similar behavior.

To test the reliability of the Au-free, fully Cu-metallized HBT, the device with the 4 × 20 μm emitter area as subjected to a current-accelerated stress test at a high current density of 140 kA/cm^2. Figure 4.8 plots the measured current gain (β) of the Au-free, fully Cu-metallized HBT after being stressed at the high current density of 140 kA/cm^2 at a V_{CE} of 1.5 V for 24 h. The measurement was carried out at an ambient room temperature of 25℃. Under these test conditions, the estimated junction temperature, T_j was approximately 280℃. It can be seen from the data plotted in Figure 4.8 that the current gain of the device showed no significant change with time and was still higher than 140 after 24 h of the current-accelerated stress test. In the life test, five devices were evaluated, and showed similar characteristics; the change in the ratio of the final/initial current gain is less than 0.5% for these devices. None of the fully Cu-metallized HBTs failed in the test.

To study the thermal stability of the Pt diffusion barrier, the 4 × 20-μm-emitter-area Au-free fully Cu-metallized HBT was annealed at 250℃ for 24 h and tested for electrical performance. Also, the copper oxidation was studied. Silicon nitride (10 nm) protective layer was deposited on the top of the device to prevent Cu

film oxidation. The device without silicon nitride protective layer was also processed the same wafer for comparison. Figure 4.9 shows the common emitter I-V curves before and after annealing for the fully Cu-metallized HBT without silicon nitride protective layer. As can be seen from the data plotted in Figure 4.9, the knee voltage was increase after annealing. It was caused by the copper oxidation when the device without silicon nitride protective layer after annealing, so the resistance of the copper was increased. Figure 4.10 shows the common emitter I-V curves before and after annealing for the fully Cu-metallized HBT with silicon nitride protective layer. As can be seen from the data plotted in Figure 4.10, there was no change in the offset voltage, knee voltage, or saturation current after annealing. It is suggested that there was no ohmic degradation, copper oxidation, or copper diffusion in the fully Cu-metallized HBTs using Pt as a diffusion barrier.

The microwave performance of the fully Cu-metallized HBT was also characterized by on-wafer S-parameter measurements using a network analyzer. Figure 4.11 shows the h_{21} curve of the 4 × 20-μm-emitter-area device before and after annealing at 250℃ for 24 h. As can be seen from the data plotted in Figure 4.11, the H_{21} curve showed less than 3% change after thermal annealing. The cutoff frequency (f_T) of both devices was approximately 38 GHz. It is suggested that no additional degradation, no copper diffusion into the active region of the device and no copper oxidation after the thermal stress; these results were consistent with the material analysis results.

4.6 Conclusion

An Au-free, fully Cu-metallized HBT using Pt as the diffusion barrier was fabricated and reported for the first time. From the XRD data and the sheet resistance

study, the Ti/Pt/Cu HBT was determined to be very stable after annealing at 350℃. The common emitter I-V curves of the Au-free fully Cu-metallized HBTs showed similar electrical characteristics to those of HBTs with conventional Au-metallized layers. During both the current-accelerated stress test (140 kA/cm^2 stress for 24 h) and the thermal stress test (annealing at 250℃ for 24 h), for the fully Cu-metallized HBTs showed almost no change in electrical characteristics. The results show that it is possible to fabricate fully Cu-metallized InGaP/GaAs HBTs using PdGe and Pt/Ti/Pt/Cu as contact metals and Pt as the diffusion barrier metal.

FIGURES

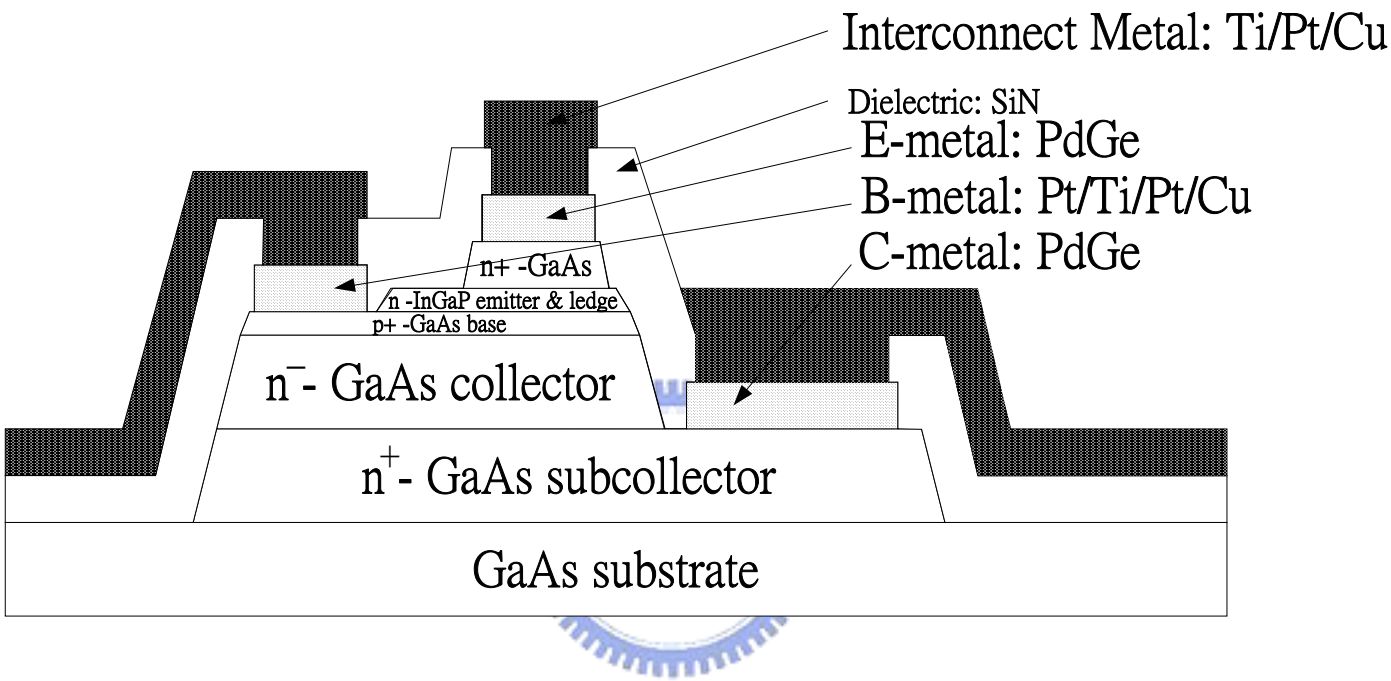


Figure 4.1 Cross section of the Au-free fully Cu-metallized InGaP/GaAs HBT.

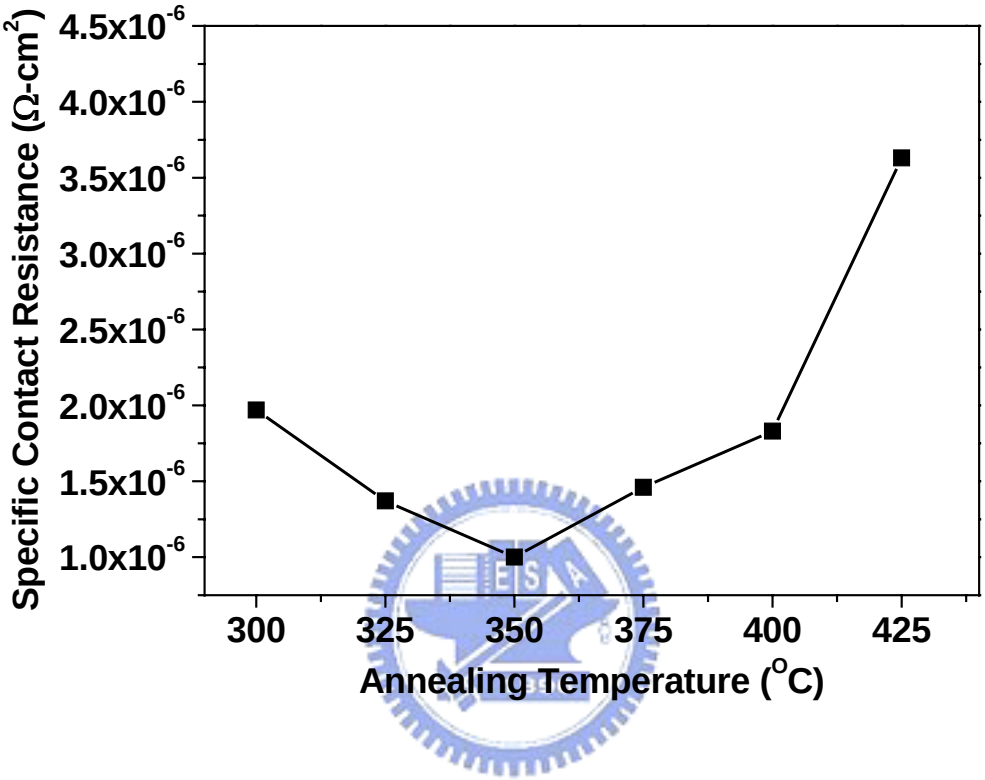


Figure 4.2 Specific ohmic contact resistance for the n^+-GaAs/Pd/Ge structure

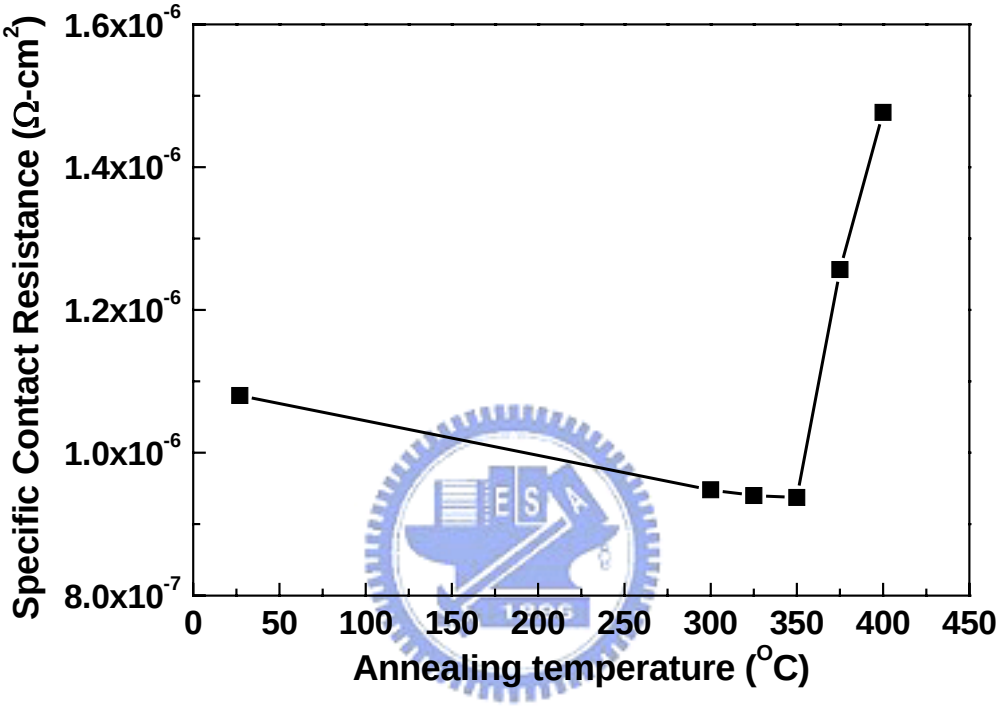


Figure 4.3 Specific ohmic contact resistance for the p^+-GaAs/Pt/Ti/Pt/Cu structure

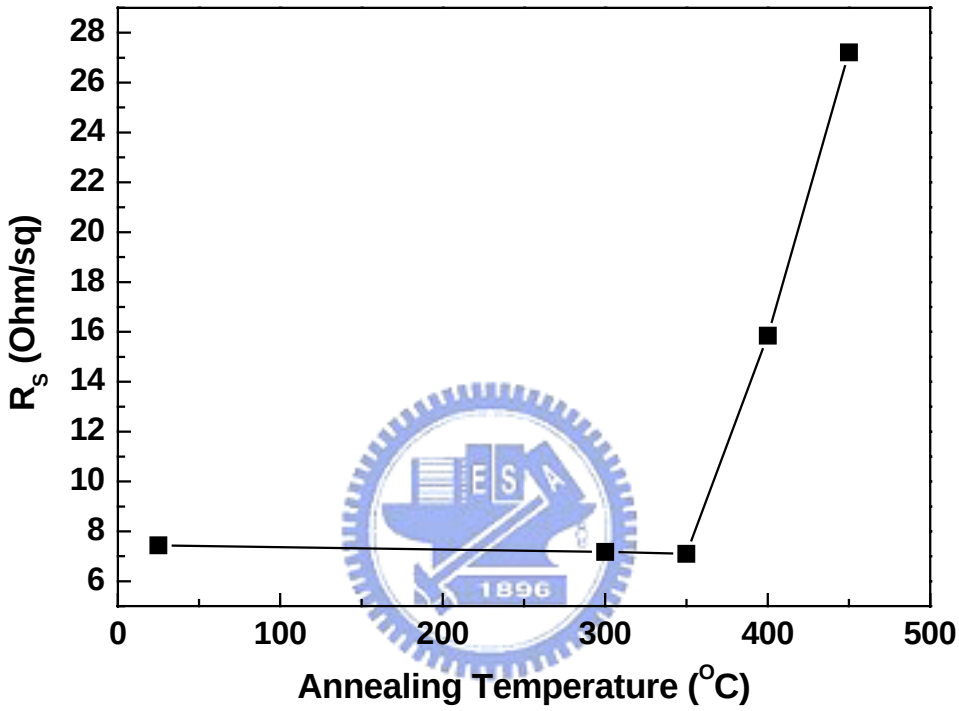


Figure 4.4 Sheet resistance of the GaAs/Ti/Pt/Cu samples as-deposited and after annealing at various temperatures.

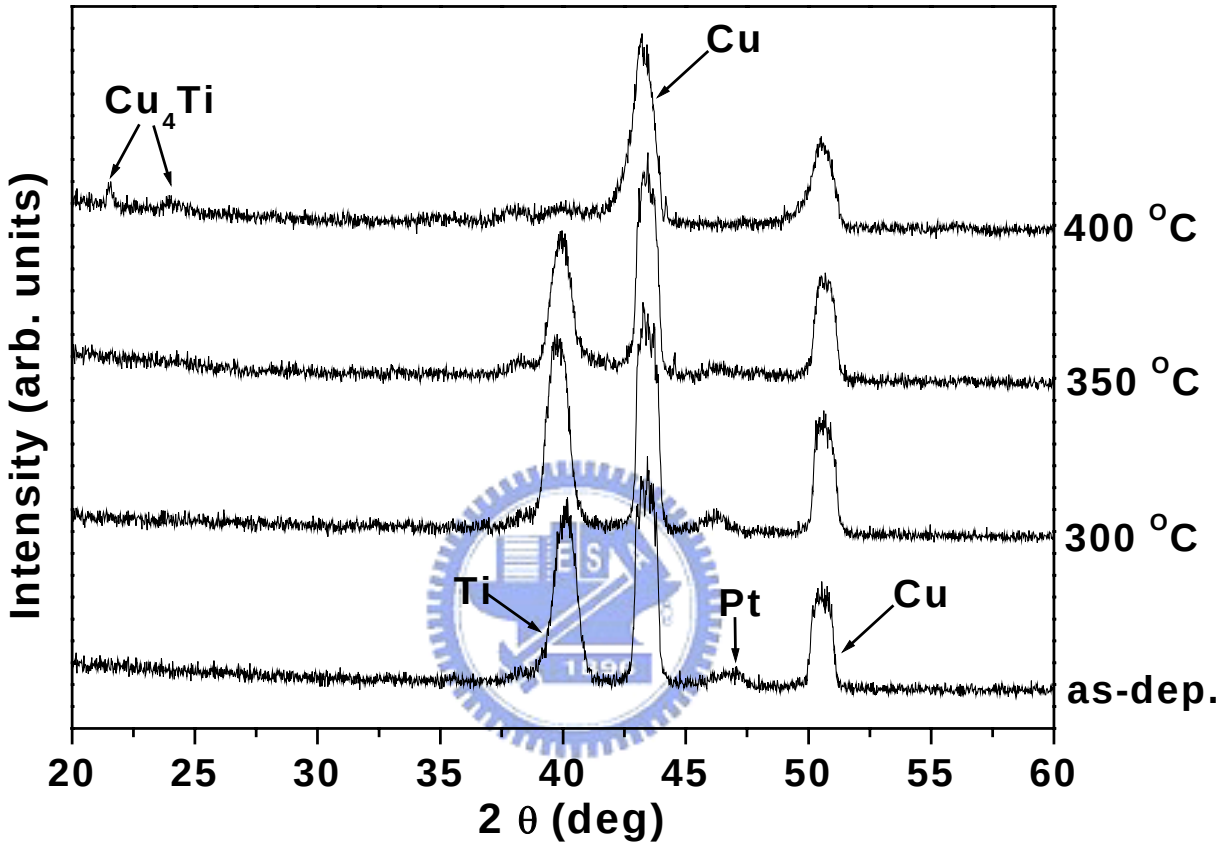


Figure 4.5 XRD patterns of the Ti/Pt/Cu samples as-deposited and after annealing at various temperatures.

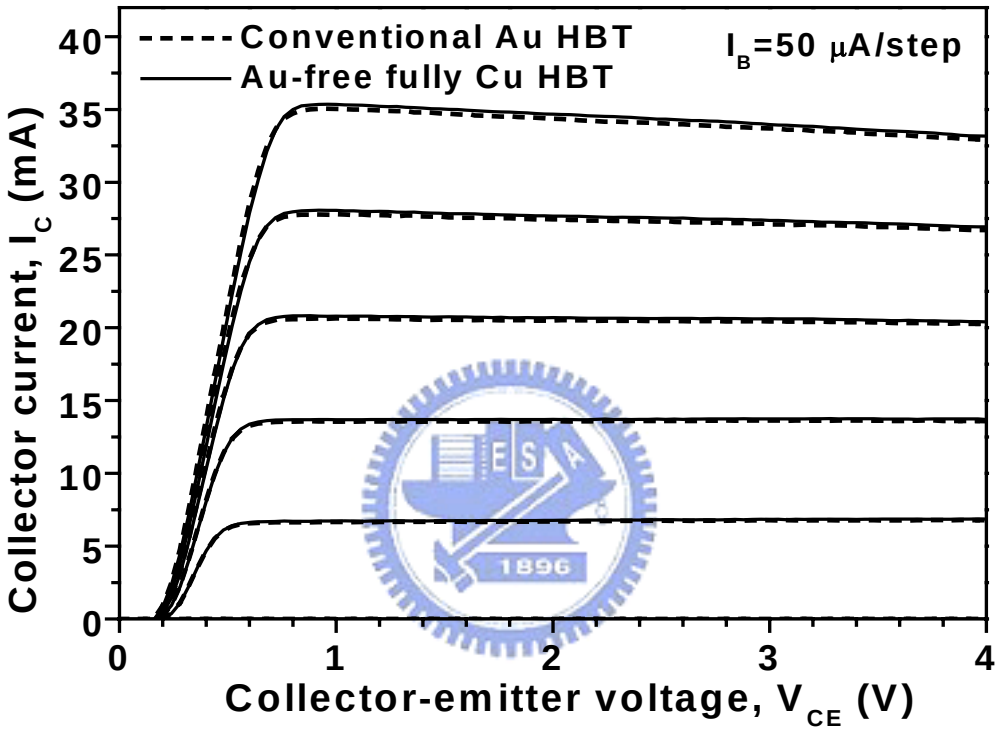


Figure 4.6 Comparison of the typical I_C-V_{CE} characteristics of the fully Cu-metallized and the conventional Au-metallized 4×20-μm-emitter-area HBTs.

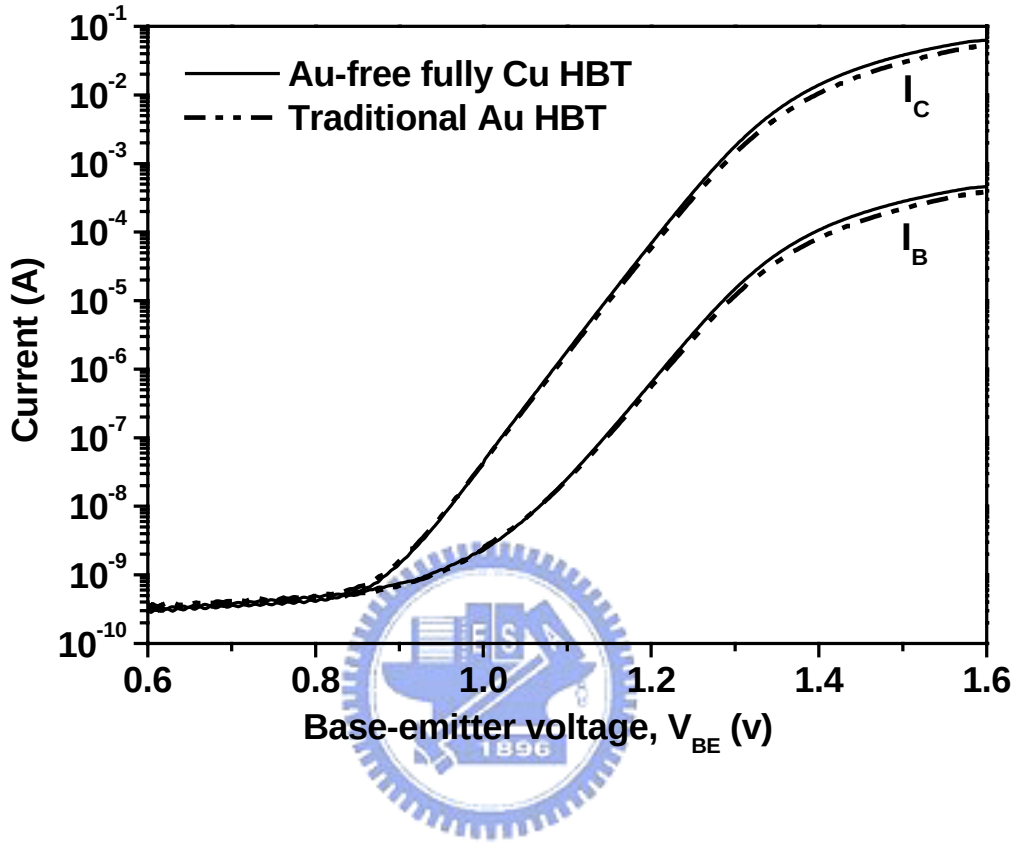


Fig. 4.7 Comparison of the Gummel plots for the emitter area (3×20 μm^2) HBT with Cu and with Au interconnect metallizations.

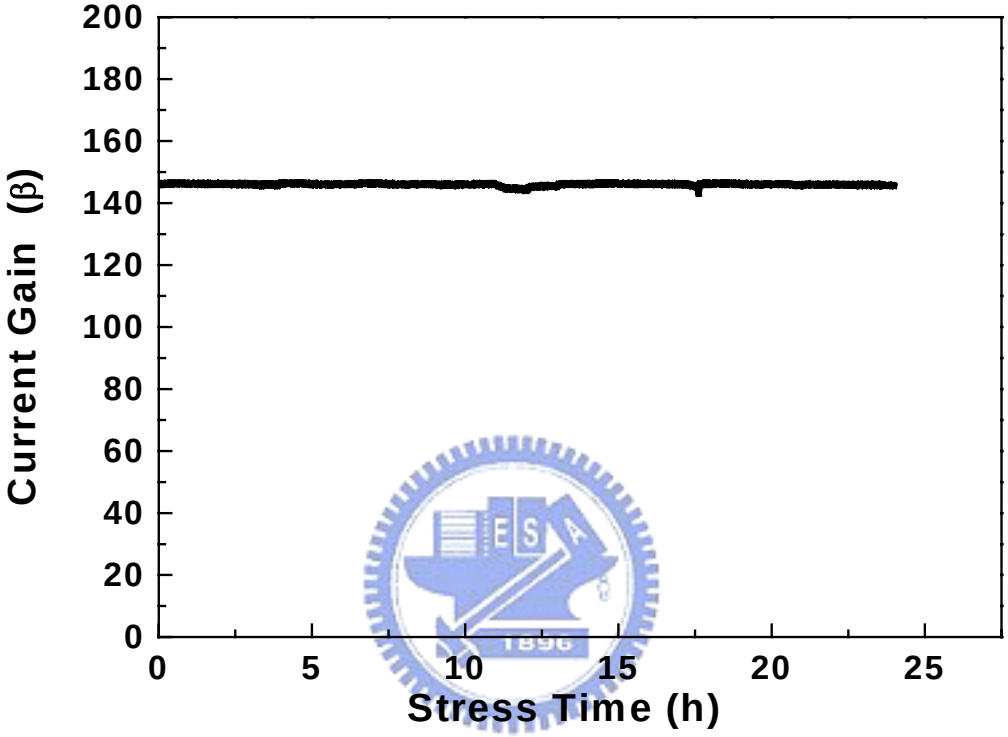


Figure 4.8 Current gain as a function of stress time at constant I_B for the 4× 20-μm-emitter-area fully Cu-metallized HBT.

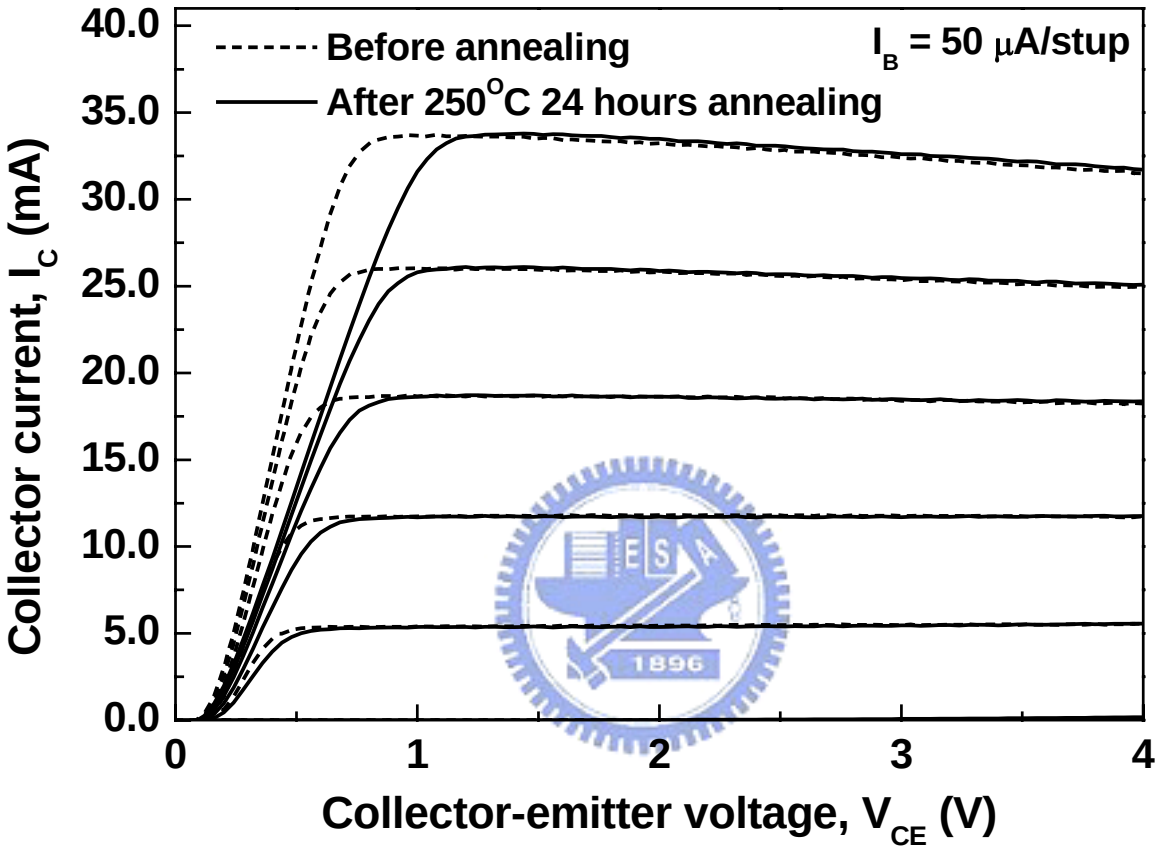


Figure 4.9 Common emitter I-V curves measured before and after annealing at 250℃ for 24 h for the 4×20-μm-emitter-area fully Cu-metallized HBT without silicon nitride protective layer.

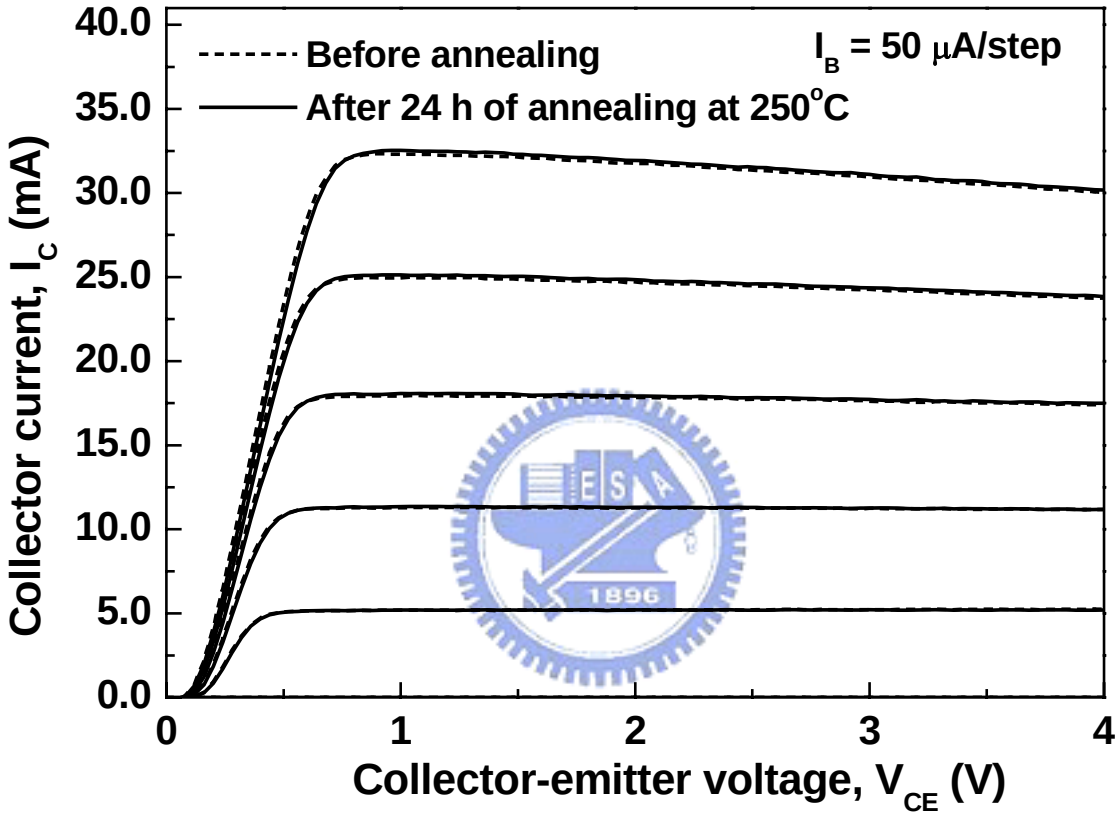


Figure 4.10 Common emitter I-V curves measured before and after annealing at 250 ℃ for 24 h for the 4×20-μm-emitter-area fully Cu-metallized HBT with silicon nitride protective layer.

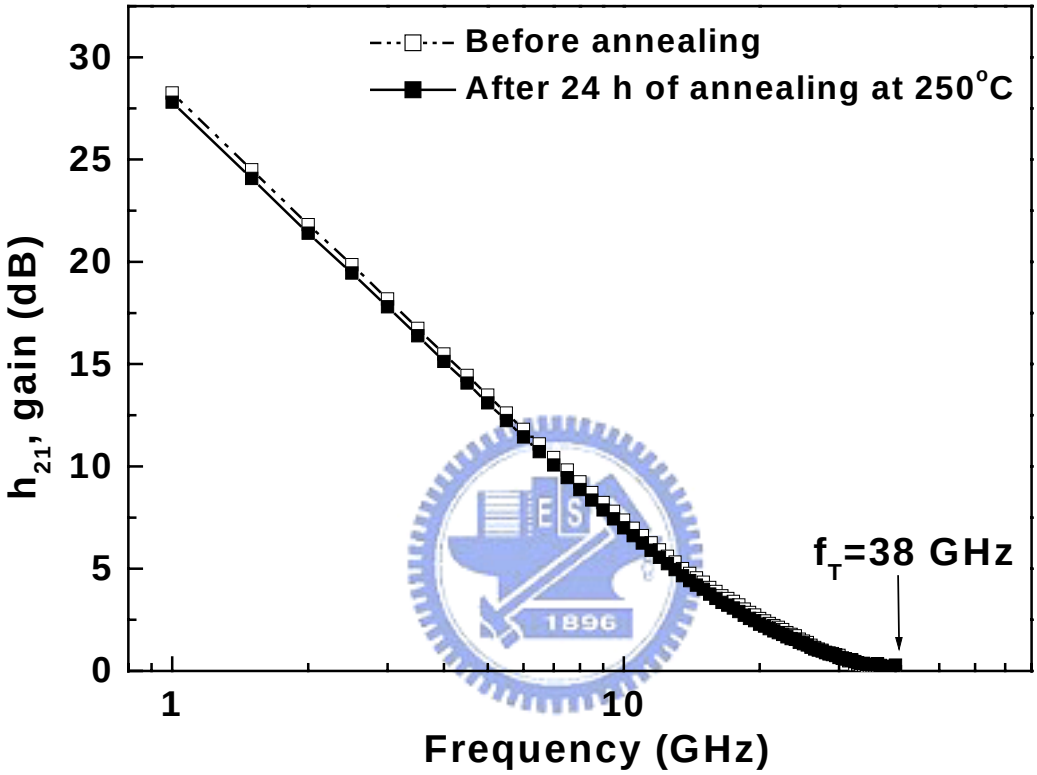


Figure 4.11 Current gain H_{21} curves measured before and after annealing at 250℃ for 24 h for the 4×20-μm-emitter-area fully Cu-metallized HBT.

Chapter 5

A Gold-Free Fully Copper-Metallized InP HBT Using Non-Alloyed Ohmic Contact and Platinum Diffusion Barrier

5.1 Introduction

In our previous studies, we have demonstrated interconnect copper metallization of InGaP/GaAs HBTs using WN_X as the diffusion barrier [23] and gold-free fully copper-metallized InGaP/GaAs HBTs using Pt as the diffusion barrier [24]. In this study, we try to make fully Cu (from ohmic contact to interconnect metal) metallized InP HBTs. And this is the first time fully Cu-metallized InP HBTs are demonstrated.

InGaAs/InP single heterojunction bipolar transistors on InP substrate exhibit excellent high frequency noise and gain characteristics under low power consumption. The InP and InGaAs lattice-matched to InP substrate have unique material properties such as higher electron mobility, lower surface recombination rate, better bandgap alignment, and higher thermal conductivity, which enable better device performances than in GaAs-based HBT's. Conventionally, n-type Ti/Pt/Au and p^+-type Pt/Ti/Pt/Au ohmic contacts, and Ti/Au interconnect metals have been the most widely used metallization structures for the fabrication of InP-based heterojunction bipolar transistors. If Cu replaces Au as the metallization metal for InP HBTs, then the reduction in RC delay can increase the transmission speed of the HBT circuits and the heat dissipation will also be improved.

To make fully Cu InP HBTs, there were two items must take into consideration. First, the n-type and p-type ohmic contact with Cu metallization should be examined. Second, the thermal stability of the diffusion barrier should be carried out. In this study, Ti/Pt/Cu and Pt/Ti/Pt/Cu metals are used for the n-type and p-type ohmic

contacts, respectively, and Ti/Pt/Cu is used as the interconnect metals with platinum as the diffusion barrier to fabricate the Au-free, fully Cu-metallized InP HBTs. Platinum is used as the diffusion barrier because it has a high melting point, is compatible with the lift off process, and is a good diffusion barrier for preventing Au from diffusing into the conventional GaAs Schottky (Ti/Pt/Au) and ohmic (Pt/Ti/Pt/Au) structures [25]. Therefore, the capability of Pt here was the diffusion barrier to make the Au-free, fully Cu-metallized HBTs using lift-off technology.

On the other hand, HBT is usually passivated with plasma-enhanced chemical vapor deposited silicon nitride (PECVD-SiN) film, if Cu is in direct contact with the silicon nitride film of poor quality, a large amount of Cu may diffuse through the micro-defects of the PECVD-SiN films during the heat treatment of the metallization process and the leakage current will increase as a result of the Cu diffusion [4]. In this study, the thermal stabilities of the InGaAs/SiN/Ti/Pt/Cu, and InGaAs/Ti/Pt/Cu multilayer structures were investigated. Moreover, these material systems were used to fabricate the InP/InGaAs HBTs. Here, we are reporting for the first time the fabrication and electrical performance of the Au-free, fully Cu-metallized InP HBTs.

5.2 Experimental

The experiments in this study include three parts. First, the n-type and p-type multilayer ohmic contacts on heavily doped InGaAs should be studied prior to manufacturing fully Cu InP HBTs. Second, the thermal stability of the diffusion barrier was discussed. After the completion of the ohmic contact multilayer and the diffusion barrier thermal stability studies, the Cu multilayer structure was applied on the InP HBTs, and the fully Cu InP HBTs are realized.

The first part is the ohmic contact study. The specific contact resistances of

n^+-InGaAs/Ti (50 nm)/Pt (60 nm)/Cu (150 nm) and p^+-InGaAs/Pt (5 nm)/Ti (50 nm)/Pt (60 nm)/Cu (150 nm) were carried out by transmission line method (TLM). The TLM patterns were fabricated by I-line photolithography. After the metal evaporation, the samples were immersed into ACE and IPA with the common lift-off process. The samples of traditional n^+-InGaAs/Ti (50 nm)/Pt (60 nm)/Au (150nm) and p^+-InGaAs/Pt (5 nm)/Ti (50 nm)/Pt (60 nm)/Au (150 nm) ohmic contact were also fabricated and measured for the purpose of comparison. The samples were then annealed at various temperatures from 300^{o}C to 400 ^{o}C in an Ar-ambient tube furnace for 10 minutes.

The second part is the thermal stability study of the diffusion barrier. There were two types of multilayer structures (InGaAs/Ti/Pt/Cu and InGaAs/SiN/Ti/Pt/Cu) using Pt as diffusion barrier in the Cu-metallized InP HBTs as shown in Figure 5.1. The multilayer structures and thickness of each metal layer were shown in Figure 5.2. The thermal stability of these structures must to be studied prior to applying them to the InP HBTs fabrication. The SiN film was used for the passivation of the devices, and it was formed by PECVD. The Ti/Pt/Cu multilayer structure was deposited using an e-gun evaporator. After deposition, the InGaAs/Ti/Pt/Cu and InGaAs/SiN/Ti/Pt/Cu multilayer structures were annealed for 30 min at different temperatures in Ar-ambient for material analysis. Scanning electron microscopy (SEM), Auger electron spectroscopy (AES), and sheet resistance were used for the study of the interfacial reactions.

The third part is the fabrication of the gold-free fully copper-metallized InP HBT using non-alloyed ohmic contact and platinum diffusion barrier. The InP HBTs used in this work were grown by metal organic chemical vapor deposition (MOCVD) on the semi-insulating InP substrates. The layer structure consists of (from bottom to top) an

n^+-InGaAs subcollector (500 nm, 2×10^{19} cm^{-3}), an n^--InGaAs collector (600 nm, 2×10^{16} cm^{-3}), a p^+-InGaAs base (100 nm, 2×10^{19} cm^{-3}), an n-InP emitter (110 nm, 5×10^{17} cm^{-3}), and an n^+-InGaAs cap (100 nm, 1×10^{19} cm^{-3}). The HBT devices were fabricated using a standard triple mesa process. The InGaAs and InP layers were etched with $H_3PO_4/H_2O_2/H_2O$ and HCl/H_3PO_4 solutions, respectively. Nonalloyed Ti/Pt/Cu, Pt/Ti/Pt/Cu, and Ti/Pt/Cu gold-free ohmic metal systems were used for the emitter, base, and collector contacts, respectively. Device passivation was realized with PECVD silicon nitride. After opening the connecting via on the nitride film, the Ti adhesion layer (30 nm), the Pt diffusion barrier (60 nm), and the Cu interconnect metal (400 nm) were sequentially deposited using an e-gun evaporator. Finally, silicon nitride (10 nm) was deposited as a protective layer on the top of the device to prevent Cu film oxidation. The dimension of the emitter area of the HBT was 3 μm × 20 μm. The structure of the InP/InGaAs HBTs in this study is shown in Figure 5.1. The DC current-voltage (I-V) characteristics of the HBT devices were measured using an HP4142B I-V analyzer. The devices were stressed using a high-temperature thermal annealing test and a current-accelerated test for reliability evaluation. The thermal test was carried out by annealing at 200℃ for 3 hours in nitrogen ambient. The high-current test was performed at a high current density of 80 kA/cm^2 for 24 h.

5.3 Ohmic Contact Result

The specific contact resistances of the traditional n^+-InGaAs/Ti/Pt/Au, p^+-InGaAs/Pt/Ti/Pt/Au, and the fully Cu n^+-InGaAs/Ti/Pt/Cu, p^+-InGaAs/Pt/Ti/Pt/Cu annealed at 300℃ to 400℃ for 10 minutes are shown in Figures 5.3(a) and (b). It can be seen from Figure 5.3(a) that the specific contact resistance of

n^+-InGaAs/Ti/Pt/Cu structure reached the lowest value at annealing temperature of 300℃ whereas that of the n^+-InGaAs/Ti/Pt/Au structure reached a lowest value at annealing temperature of 325℃. For the p-type ohmic contact from Figure 5.3(b), the specific contact resistance of p^+-InGaAs/Pt/Ti/Pt/Cu also reached the lowest value after annealing at temperature of 300℃, but that of the p^+-InGaAs/Pt/Ti/Pt/Au reached a lowest value after annealing at temperature of 350℃. The lowest values of the specific contact resistances of the four structures are listed in Table 5.1. It can be seen from the table that both the n-type and p-type Cu ohmic contacts had similar specific contact resistance with those of the traditional Au ohmic contacts. The contact resistances of the Cu based electrodes were of the same order as that of the Au-based electrodes.

5.4 Thermal Stability of the Pt Diffusion Barrier

Figures 5.4 (a) to (c) show the AES depth profiles of the InGaAs/Ti/Pt/Cu samples as-deposited, after 350℃, and 400℃ annealing for 30 minutes. As can be seen from Figure 5.4(b), there was no atomic inter-diffusions between Cu and the InGaAs layer after annealing at temperature of 350℃ for 30 min, which means Pt can effectively prevent Cu from diffusing into the InGaAs layer. However, as shown in Figure 5.4(c), after annealing at temperature of 400°C, the Cu atoms penetrated the Pt layer and diffused into the InGaAs layer, and the figure shows the serious intermixing of Cu, Pt, Ti, and the InGaAs layer.

Figures 5.5 (a) to (d) are the SEM images of the InGaAs/Ti/Pt/Cu samples as-deposited, after 300℃, 350℃, and 400℃ annealing for 30 minutes. As can be seen in Figure 5.5 (a), the surface morphology of the as-deposited sample was very smooth. The images of Figure 5.5 (b) and (c) were almost the same, there were few

micro-pores in the surface of the samples annealed at 300℃ and 350℃. But as can be seen in Figure 5.5 (d), there were a lot of micro-pores in the surface of the sample subjected to 400℃ annealing. It was suggested that as the sample was subjected to the annealing temperature of 400℃, the serious inter-diffusion of the multilayer not only induced new phases formation and coarsened the surface of the metal film, but also seriously damaged the metal films. The results of AES and SEM could respond to each other and proved that the thermal stability of the InGaAs/Ti/Pt/Cu could reach annealing temperature of 350℃ for 30 min.

For the InGaAs/SiN/Ti/Pt/Cu structure, the sheet resistance measurement was used to monitor the interfacial reactions. Figure 5.6 shows the sheet resistances of the samples as-deposited and after annealing at temperature of 300℃ to 450℃ for 30 min. The sheet resistance of the InGaAs/SiN/Ti/Pt/Cu film structure decreased after annealed at 300℃ to 350℃, which was probably due to the grain growth and the decrease of the defect density in the multilayer films after thermal annealing. After 400℃ annealing, the sheet resistance drastically increased, suggesting that atomic diffusion and inter-atomic reactions had occurred between these layers. From the data shown above, it was clear that the InGaAs/Ti/Pt/Cu and InGaAs/SiN/Ti/Pt/Cu material system was quite stable up to 350℃ annealing.

5.5 Device Electrical Characteristics

The typical common emitter current I-V characteristics of the 3 × 20-μm-emitter-area Au free fully Cu-metallized InP HBT was shown in Figure 5.7. As shown in the figure, the offset voltage was about 0.1 V and the common emitter current gain (β) was approximately 52.

To test the reliability of the Cu multilayer for the Au free fully Cu-metallized

HBTs, the devices with 3 × 20 μm emitter area were subjected to current-accelerated stress test with high current density of 80 kA/cm^2. The measurement was made at an ambient room temperature of T_A = 25℃. Figure 5.8 shows the measured current gain (β) of the Au-free, fully Cu-metallized InP HBT after been stressed at the high current density of 80 kA/cm^2 at a collector-emitter voltage (V_{CE}) of 1.5 V for a period of 24 h. It can be seen from the data plotted in Figure 5.8 that the current gain of the fully Cu device showed no significant change and was still around 59 after 24 hours current accelerated stress test. No additional degradation mode was found for the fully Cu-metallized HBT.

To study the thermal stability of the Cu multilayer, the 3 × 20 μm emitter area Au free fully Cu-metallized HBTs were annealed at 200℃ for 3 hours and tested for the electrical performance. Figure 5.9 shows the common emitter I-V curves before and after annealing. As can be seen from the data plotted in Figure 5.9, there was no change in the offset voltage, knee voltage, or saturation current after annealing. It suggests that there was no ohmic degradation, copper oxidation, or copper diffusion in the fully Cu-metallized InP HBTs using non-alloyed ohmic contacts and with Pt as the diffusion barrier.

The microwave performance of the fully Cu-metallized InP HBT was also characterized by on-wafer S-parameter measurements using a network analyzer. Figure 5.10 (a) and (b) showed the f_T-I_C plots of the fully Cu InP HBT before annealing and after 3 hours annealing at 200℃. It can be seen that the device without heat treatment can operate at higher cutoff frequency at V_{CE} voltage of 1.8 V with higher collector current. If we compare the f_T of the devices operated at V_{CE} of 1.8 V and collector current of 45 mA, the cutoff frequencies of the devices before annealing and after 200℃ annealing for 3 hours are 44 GHz and 41 GHz respectively, indicating that the change of the f_T operating at this condition is less than 7%. The RF

performance shows little change of the fully Cu InP HBT, which is identical with the DC characteristics measurement. These electrical characteristics results were consistent with the material analysis results.

5.6 Conclusion

An Au-free, fully Cu-metallized InP HBT using non-alloyed ohmic contacts and with Pt as the diffusion barrier was fabricated and reported for the first time. From the AES data, the InGaAs/Ti/Pt/Cu HBT was very stable after annealing at 350℃. The common emitter current gain for the 3×20-μm-emitter-area Au-free fully Cu-metallized InP HBT was around 52. During both the thermal stress test (annealing at 200℃ for 3 h) and the current-accelerated stress test (80 kA/cm^2 stress for 24 h), the fully Cu-metallized InP HBTs showed almost no change in the electrical characteristics. The results show that it is possible to fabricate fully Cu-metallized InP HBTs using non-alloyed Ti/Pt/Cu and Pt/Ti/Pt/Cu as the contact metals and Pt as the diffusion barrier metal.

TABLES

Ohmic Contact	Nonalloyed (Ω-cm^2)	Alloyed Lowest Value (Ω-cm^2)
n-type InGaAs		
Ti/Pt/Cu,	7.46×10^{-7}	4.10×10^{-7} (at 300℃)
Ti/Pt/Au,	1.01×10^{-6}	5.67×10^{-7} (at 325℃)
p-type InGaAs		
Pt/Ti/Pt/Cu	1.21×10^{-6}	6.73×10^{-7} (at 300℃)
Pt/Ti/Pt/Au	1.71×10^{-6}	1.12×10^{-6} (at 350℃)

Table 5.1 Comparisons of the ohmic contacts on n-type and p-type InGaAs materials

FIGURES

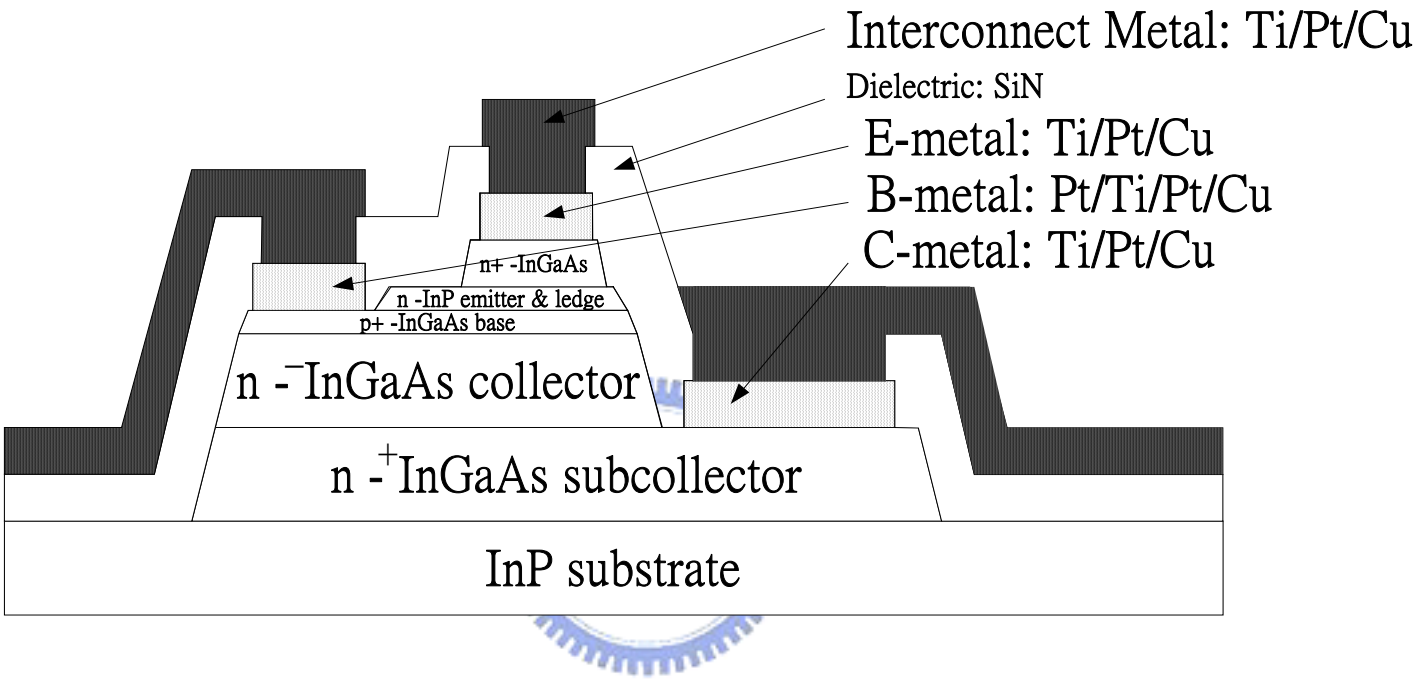
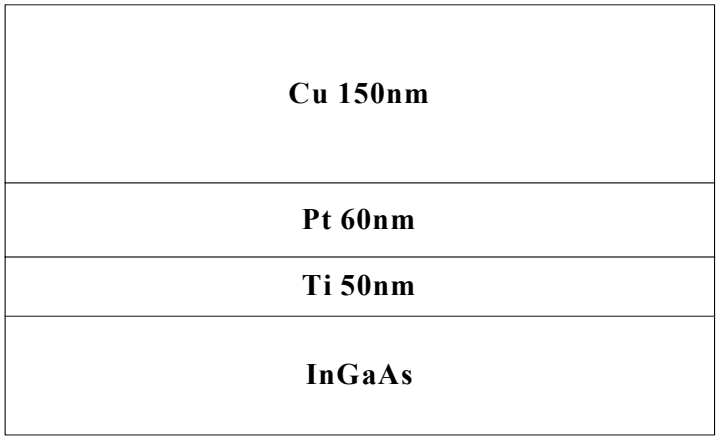


Figure 5.1 Cross section of Au-free fully Cu-metallized InP/InGaAs HBT.

(a)



(b)

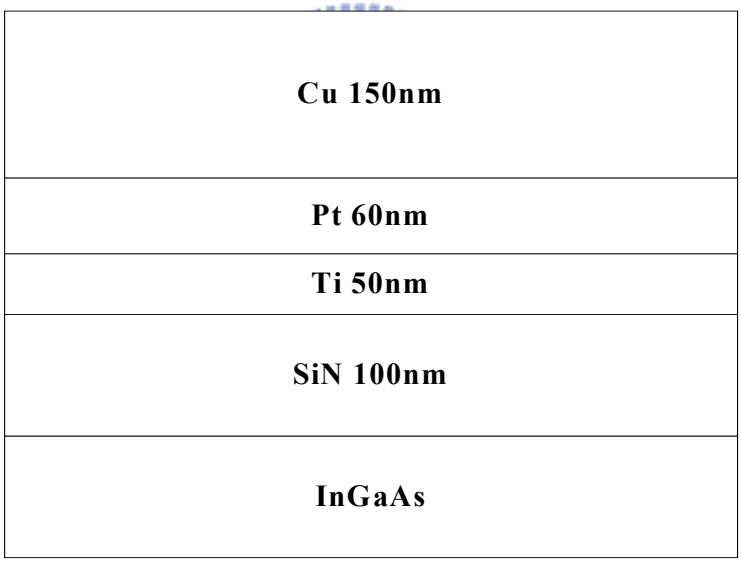


Figure 5.2 Multilayer structures of (a)InGaAs/Ti/Pt/Cu and (b)InGaAs/SiN/Ti/Pt/Cu

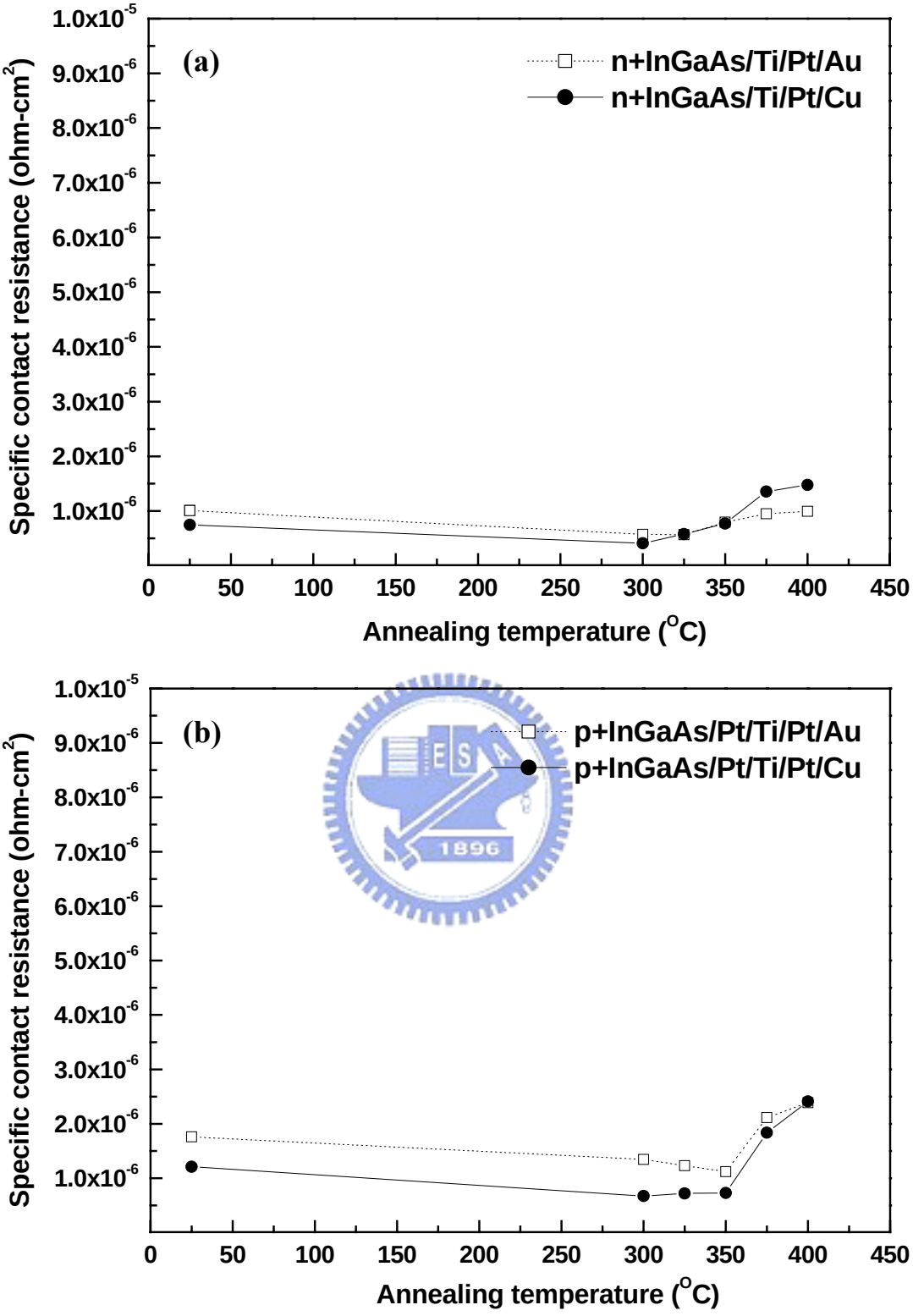
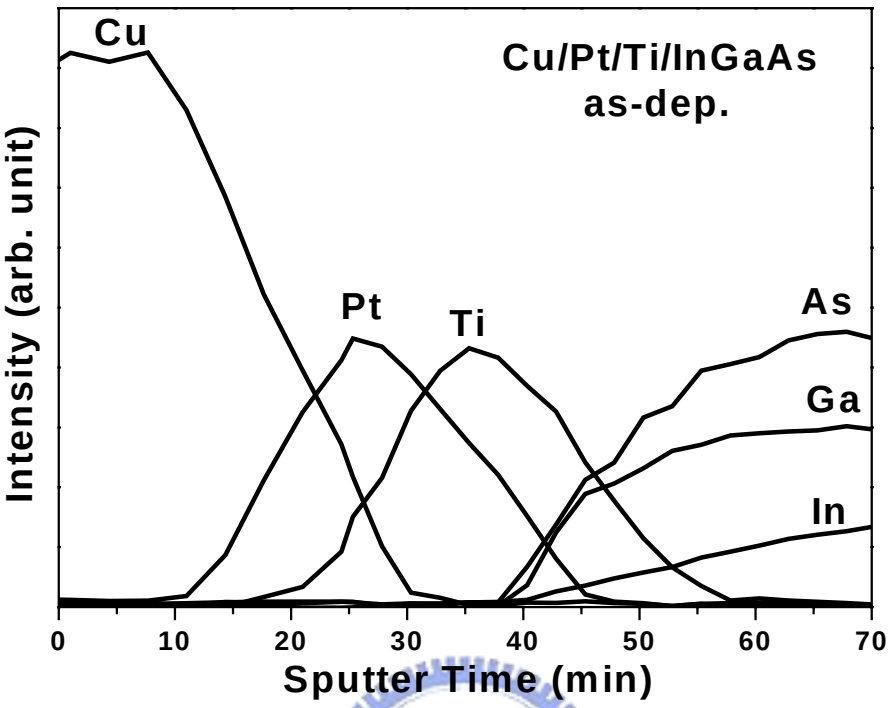
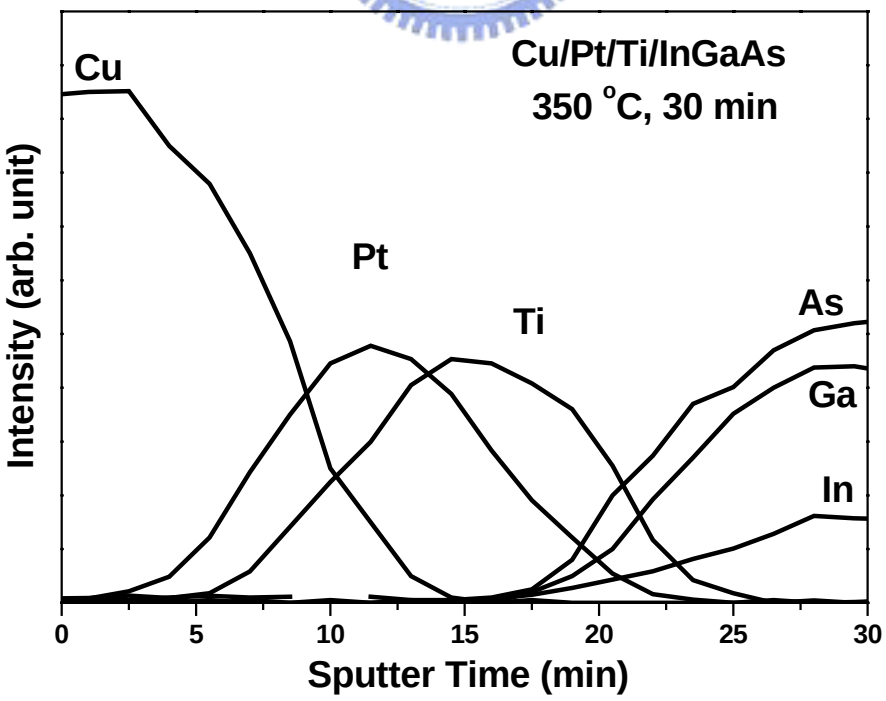


Figure 5.3 Specific ohmic contact resistances (a) on n+-InGaAs (b) on p+-InGaAs after annealing at various temperatures

(a)


Cu
Cu/Pt/Ti/InGaAs
as-dep.
Pt
Ti
As
Ga
In
Intensity (arb. unit)
0
10
20
30
40
50
60
70
Sputter Time (min)

(b)


Cu
Cu/Pt/Ti/InGaAs
350 °C, 30 min
Pt
Ti
As
Ga
In
Intensity (arb. unit)
0
5
10
15
20
25
30
Sputter Time (min)

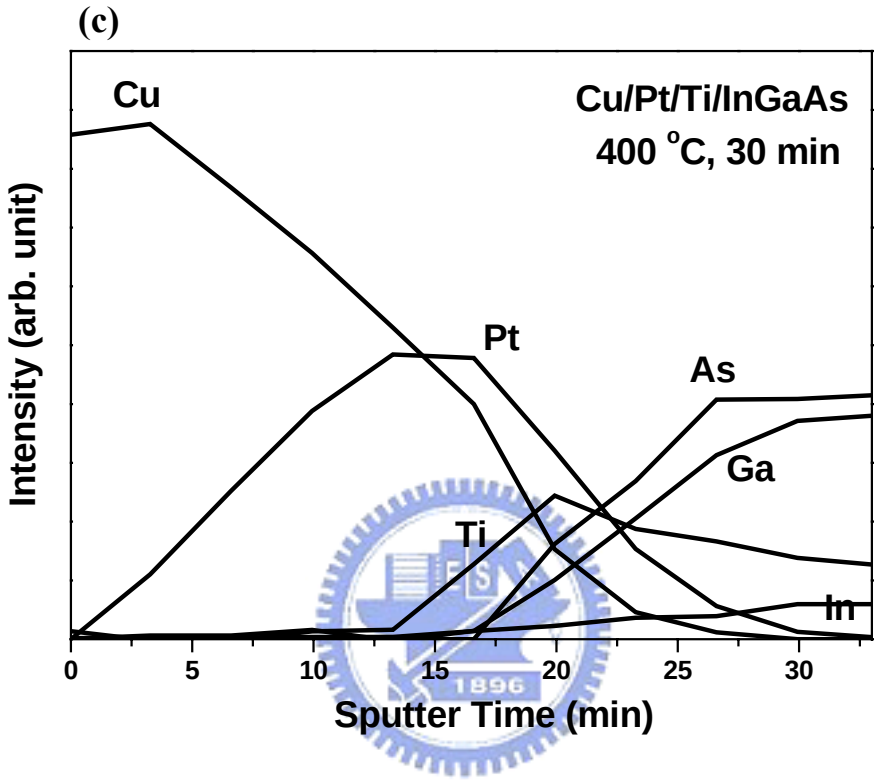
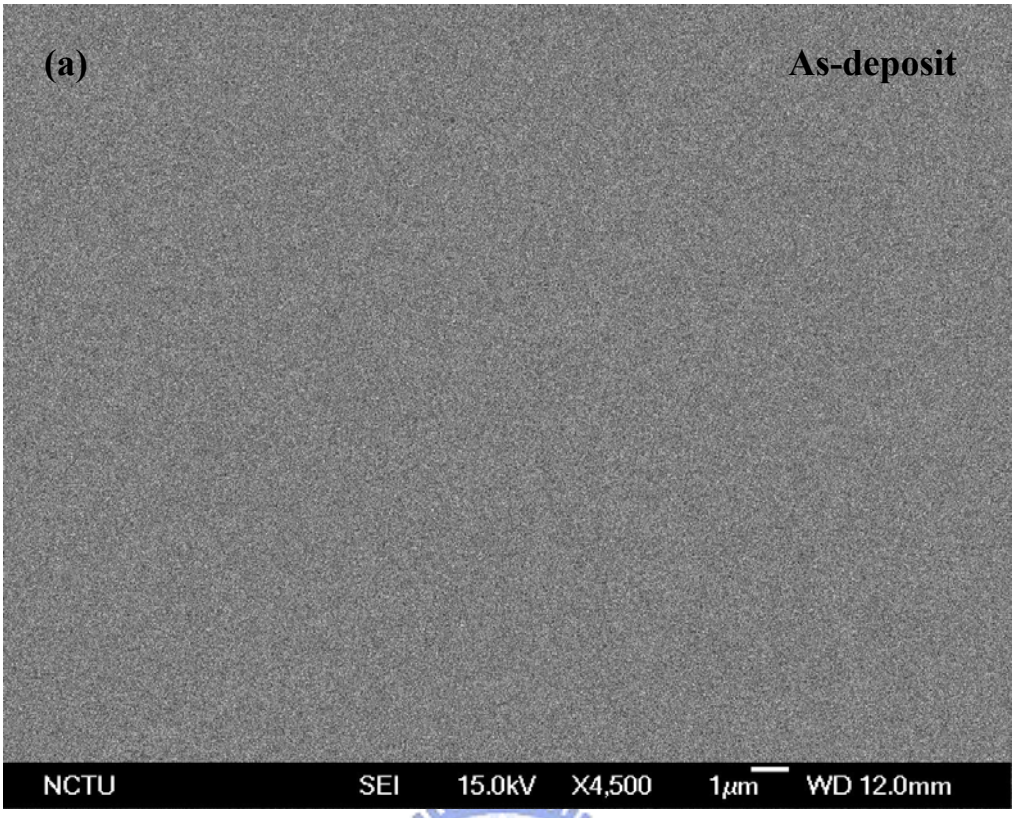
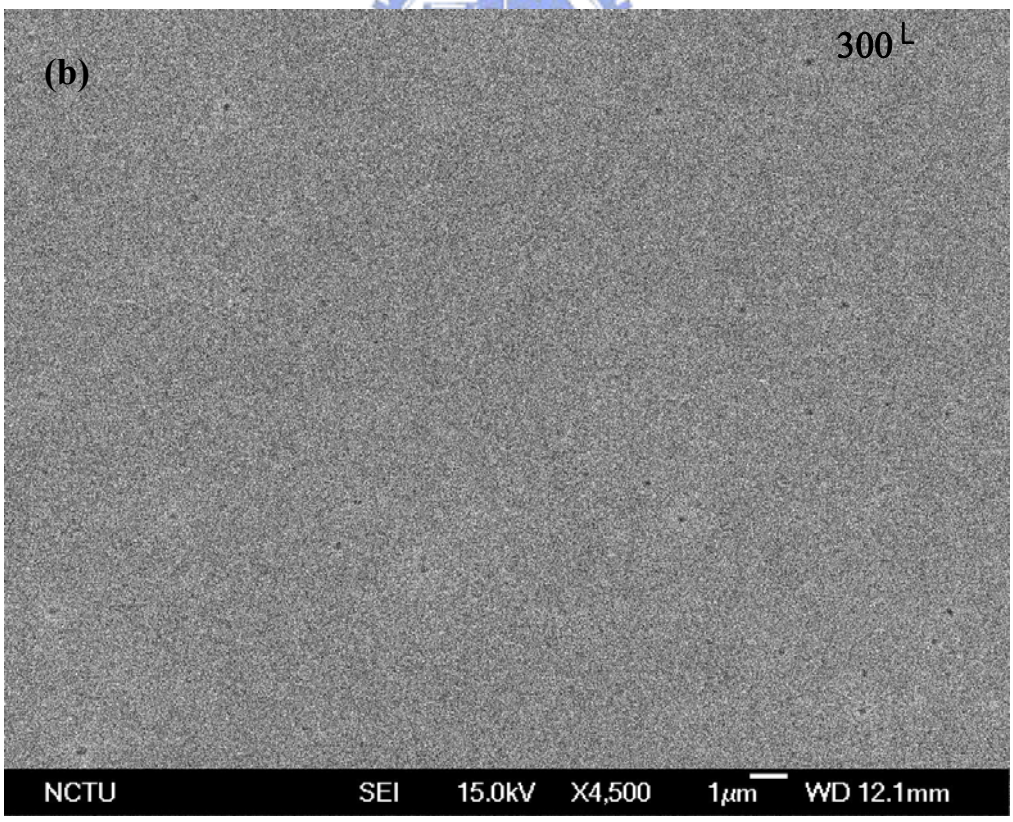


Figure 5.4 AES depth profiles of the Cu/Pt/Ti/InGaAs sample (a) as deposited; (b) after 350 °C 30 min annealing; (c) after 400 °C 30 min annealing


(a)
As-deposit
NCTU SEI 15.0kV X4,500 1μm WD 12.0mm


(b)
300 L
NCTU SEI 15.0kV X4,500 1μm WD 12.1mm

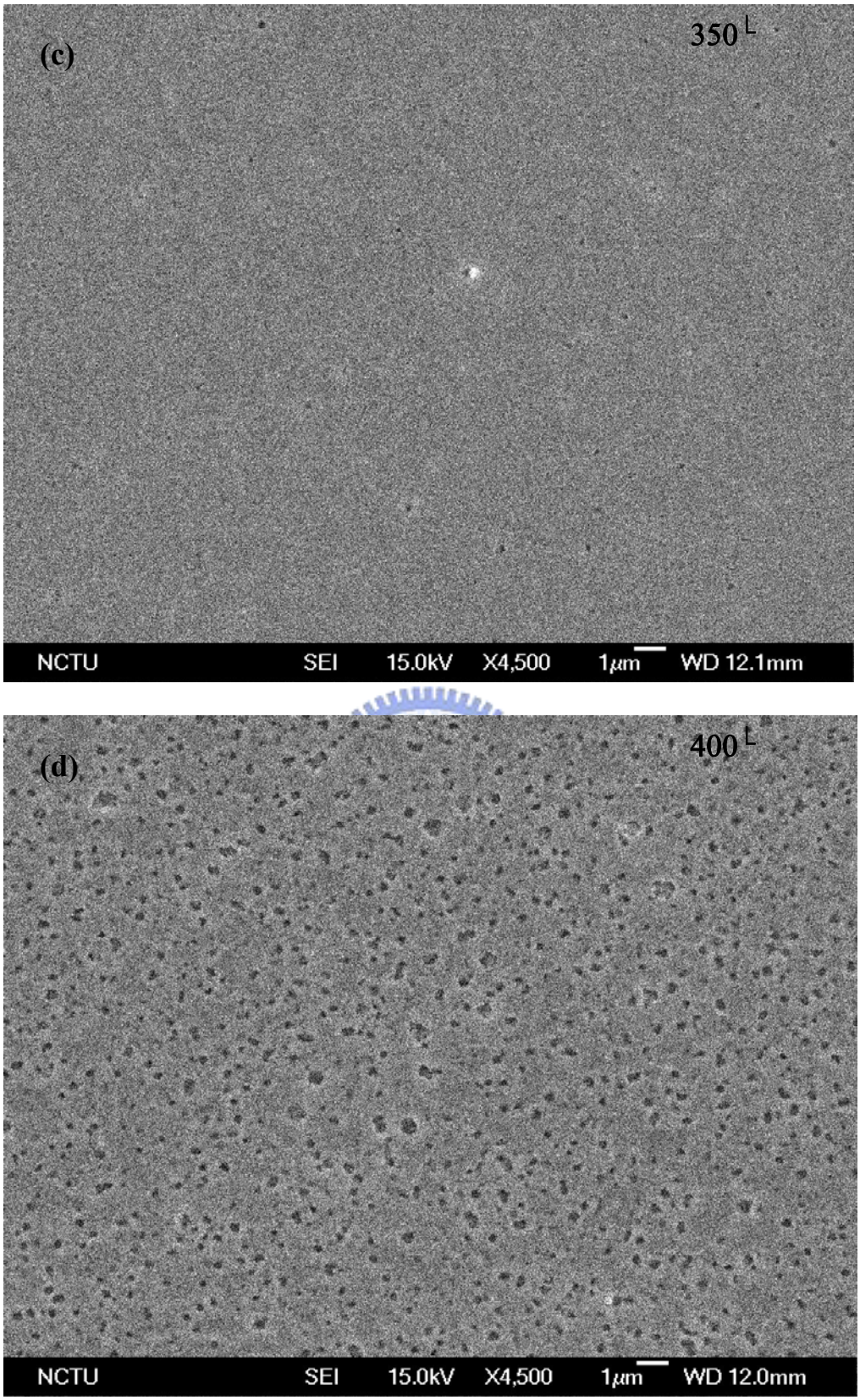


Figure 5.5 SEM micrographs of the samples (a) as-deposit, and annealing at temperatures of (b) 300°C, (c) 350°C, and (d) 400°C

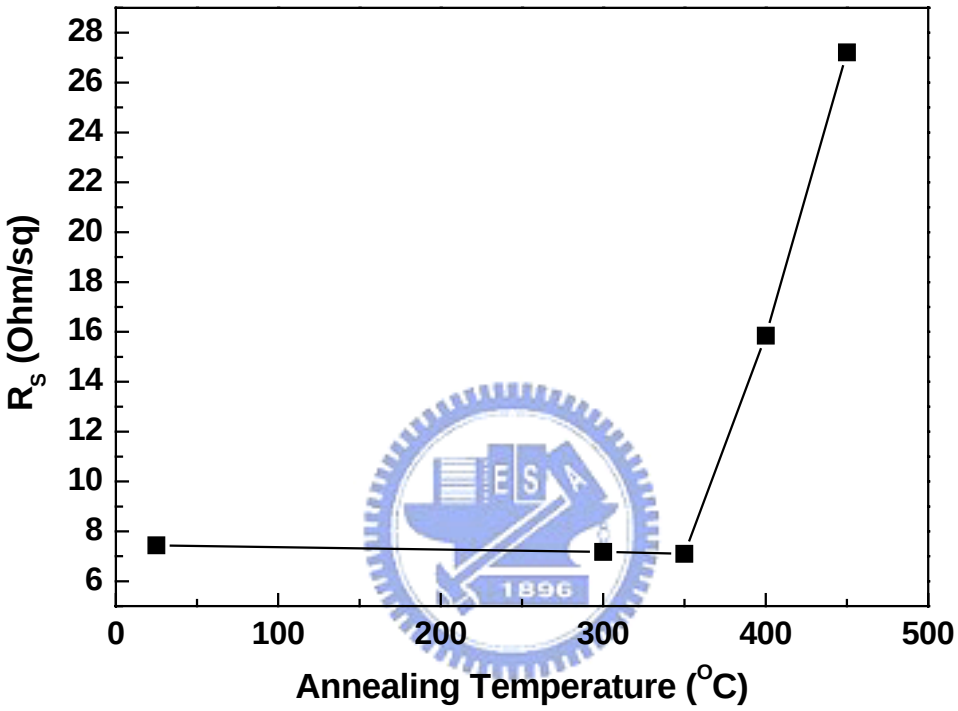


Figure 5.6 Sheet resistance results of the InGaAs/SiN/Ti/Pt/Cu multilayer samples as-deposit and after annealing at various temperatures

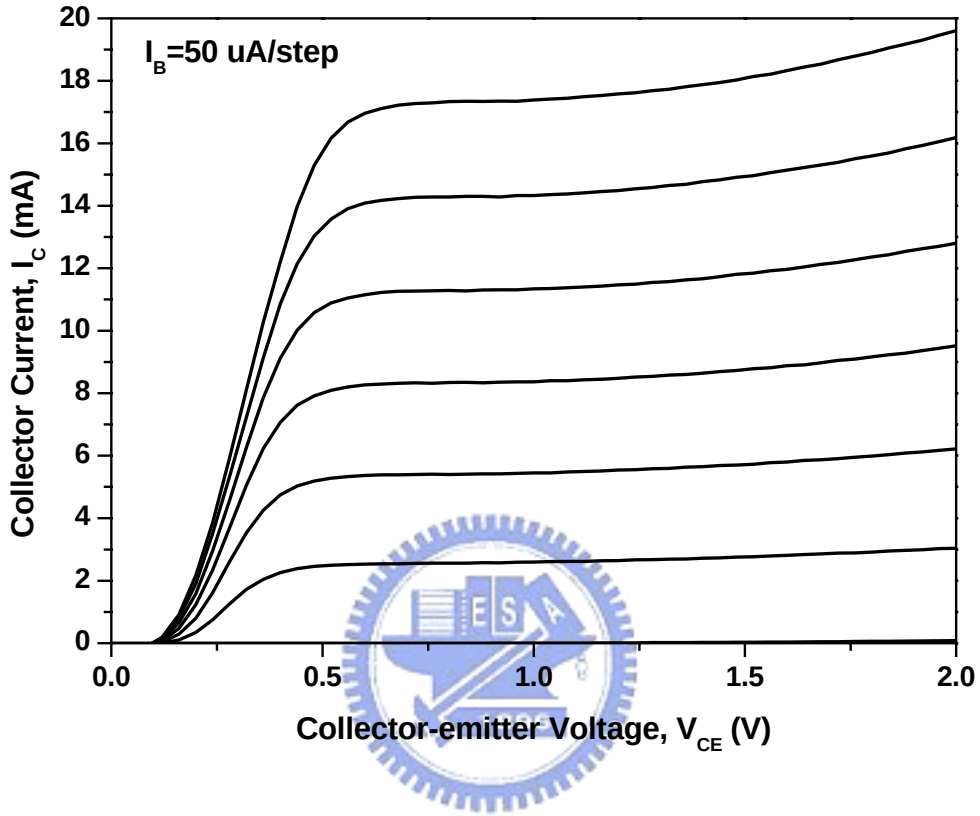


Figure 5.7 The typical common emitter current I-V characteristics of the 3×

20-μm-emitter-area Au free fully Cu-metallized InP HBT

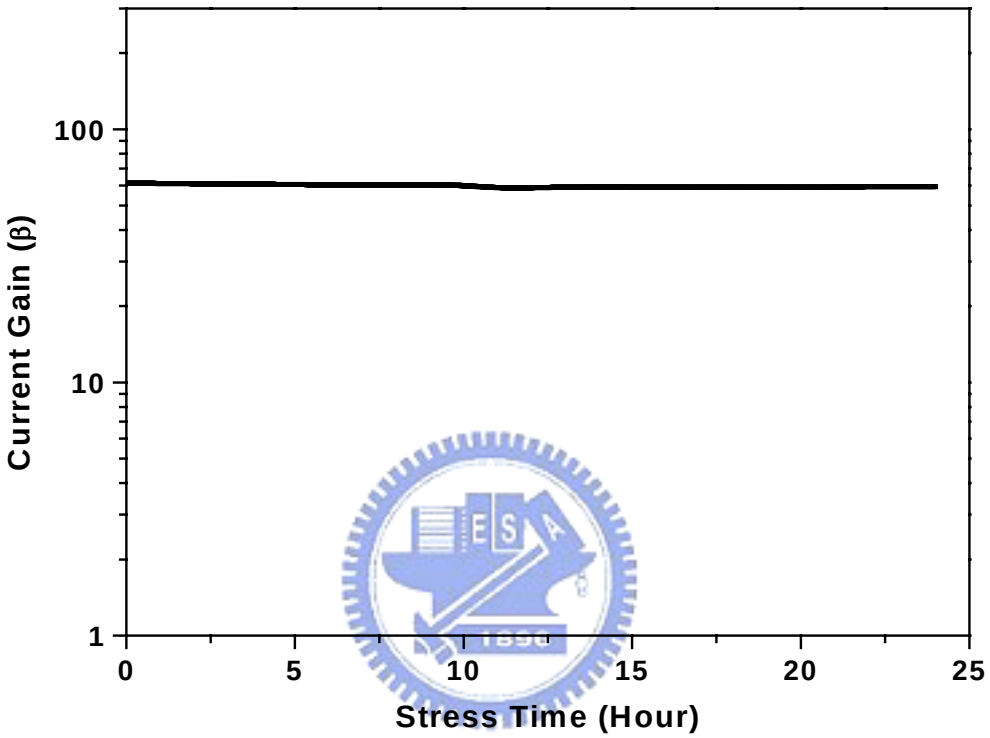


Figure 5.8 Current gain as a function of stress time at constant I_B for 3×

20-μm-emitter-area fully Cu-metallized InP HBT.

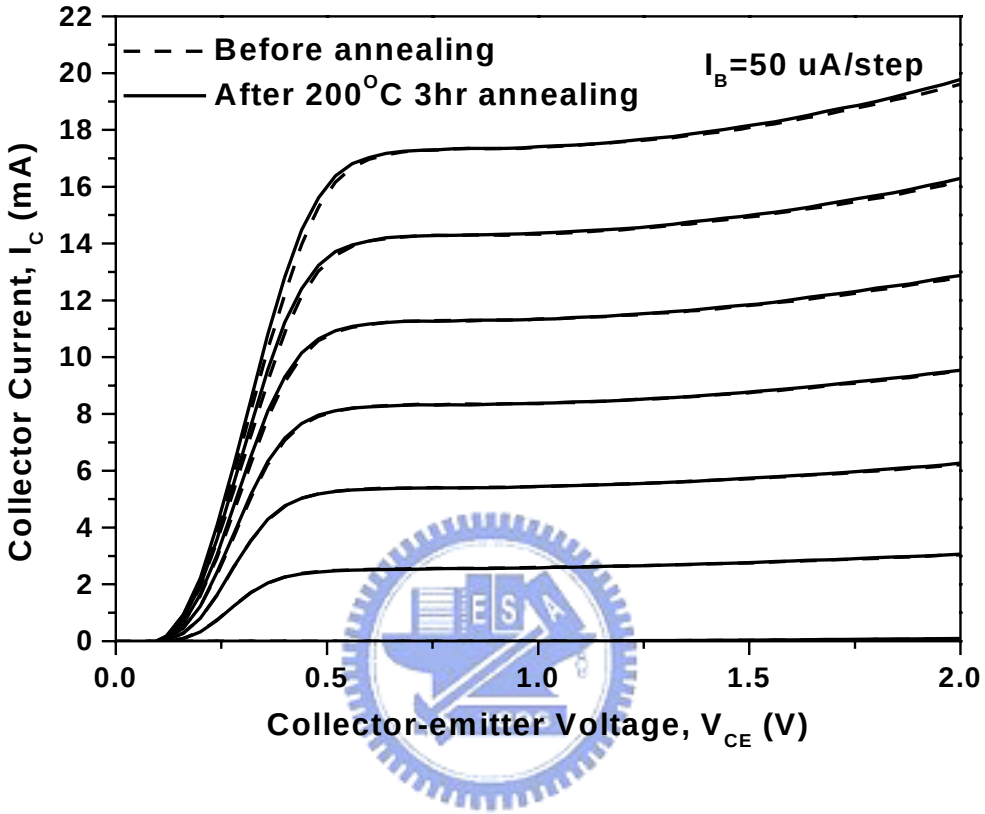


Figure 5.9 Common emitter I-V curves measured before and after annealing at 200 °C for 3 h for the 3×20-μm-emitter-area fully Cu-metallized InP HBT.

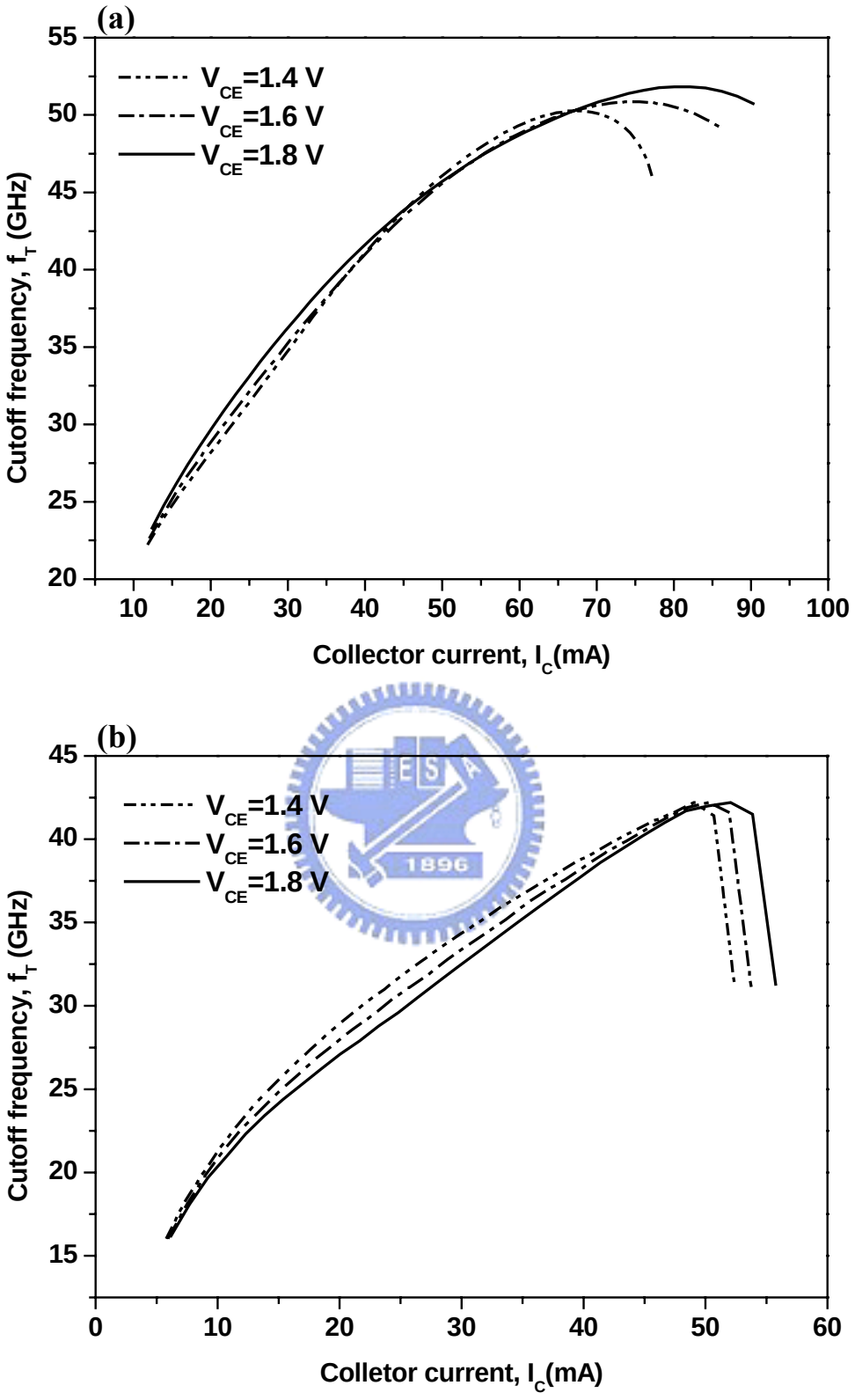


Figure 5.10 Cutoff frequency (f_T) as a function of base current (I_C) for the 3×20 μm^2 emitter area InP HBTs with fully Cu metallization (a) before annealing and (b) after 3 hours annealing

Chapter 6

Conclusions

In this dissertation, we are reporting for the first time the fabrication and electrical performance of the copper-metallized GaAs and InP HBTs. InGaP/GaAs HBTs with Cu/WN_X metallization layers were fabricated and the electrical performance were evaluated. From SEM, XRD, AES depth profile, and sheet resistance studies, the Cu/WN_X/Au and Cu/WN_X/SiN metallization layers were very stable after annealing at 400℃ and 550℃ respectively. After applying the Cu/WN_X metallization layers to the HBTs, the common emitter I-V curves of these copper metallized HBTs showed similar electrical characteristics as those HBTs metallized with the conventional Ti/Au layers. Both current-accelerated stress test (140 kA/cm^2 stress for 55 hours) and thermal stress test (annealing at 250 ℃ for 25 hours) were performed on the Cu/WN_X metallized HBTs, and almost no change in the electrical characteristics was observed for these devices after the tests. The results showed that the Cu/WN_X interconnect layers are quite stable and that WN_X can be used as the diffusion barrier for the interconnect copper metallization for the InGaP/GaAs HBTs.

Gold-free fully copper-metallized InGaP/GaAs HBT using platinum as the diffusion barrier was presented. The GaAs HBT uses Pd/Ge and Pt/Ti/Pt/Cu as n-type and p^+-type ohmic contact metals, respectively, and uses Ti/Pt/Cu as the interconnect metals with platinum as the diffusion barrier. From the XRD data and the sheet resistance study, the Ti/Pt/Cu HBT was very stable after annealing at 350℃. The common emitter I-V curves of the Au-free fully Cu-metallized HBTs showed similar electrical characteristics to those of HBTs with conventional Au-metallized layers. During both the current-accelerated stress test (140 kA/cm^2 stress for 24 h) and the

thermal stress test (annealing at 250℃ for 24 h), the fully Cu-metallized HBTs show almost no change in the electrical characteristics. The results showed that it is possible to fabricate the fully Cu-metallized InGaP/GaAs HBTs using PdGe and Pt/Ti/Pt/Cu as the contact metals and Pt as the diffusion barrier metal.

In addition, an Au-free, fully Cu-metallized InP HBTs using non-alloyed ohmic contacts and with Pt as the diffusion barrier were fabricated. The InP HBT uses Ti/Pt/Cu and Pt/Ti/Pt/Cu as n-type and p^+-type ohmic contact metals, respectively, and uses Ti/Pt/Cu as interconnect metals with platinum as the diffusion barrier. From the AES data, the InGaAs/Ti/Pt/Cu HBT was very stable after annealing at 350℃. The common emitter current gain for the 3×20-μm-emitter-area Au-free fully Cu-metallized InP HBT was around 52. During both the thermal stress test (annealing at 200 °C for 3 h) and the current-accelerated stress test (80 kA/cm^2 stress for 24 h), the fully Cu-metallized InP HBTs showed almost no change in the electrical characteristics. The results showed that it is possible to fabricate fully Cu-metallized InP HBTs using non-alloyed Ti/Pt/Cu and Pt/Ti/Pt/Cu as the contact metals and Pt as the diffusion barrier metal.

REFERENCE

[1] K. Holloway and P. M. Fryer, "Tantalum as a diffusion barrier between copper and silicon," *Appl. Phys. Lett.* **57**, 1736 (1990).

[2] K. Holloway, P. M. Fryer, C. Cabral, Jr., J. M. E. Harper, P. J. Bailey, and K. H. Kelleher, "Tantalum as a diffusion barrier between copper and silicon: failure mechanism and effect of nitrogen additions," *J. Appl. Phys.* **71**, 5433 (1992).

[3] D. S. Yoon, H. K. Baik, and S. M. Lee, "Effect on thermal stability of a Cu/Ta/Si heterostructure of the incorporation of cerium oxide into the Ta barrier," *J. Appl. Phys.* **83**, 8074 (1998).

[4] E. R. Weber, "Transition metals in silicon," *Appl. Phys. A, Solids Surf.* **1**, 1 (1983).

[5] A. Cros, M. O. Aboelfofotoh, and K. N. Tu, "Formation, oxidation, electronic, and electrical properties of copper silicides," *J. Appl. Phys.* **67**, 3328, (1990).

[6] C. A. Chang, "Formation of copper silicides from Cu(100)/Si(100) and Cu(111)/Si(111) structures," *J. Appl. Phys.* **67**, 556 (1990).

[7] P. H. Wohlbier, *Diffusion and Defect Data*. Zürich, Switzerland: Trans Tech **10**, 89 (1975).

[8] C. Y. Chen, L. Chang, E. Y. Chang, S. H. Chen, and D. F. Chang, "Thermal stability of Cu/Ta/GaAs multilayers," *Appl. Phys. Lett.* **77**, 3367 (2000).

[9] C. Y. Chen, E. Y Chang, L. Chang, and S. H. Chen, "Backside copper metallisation of GaAs MESFETs," *Electronics Lett.* **36**, 1318 (2000).

[10] C. Y. Chen, E. Y. Chang, L. Chang, and S. H. Chen, "Backside copper metallization of GaAs MESFETs using TaN as the diffusion barrier", *IEEE Trans. Electron Devices* **48**, 1033 (2001).

[11] Kazuyoshi Ueno, Koichi Ohto, and Kinji Tsunenari, "A HALF-MICRON

PITCH Cu INTERCONNECTION TECHNOLOGY", *VLSI Technology, Digest of Technical Paper,* 27 (1995).

[12] H. C. Chang, E. Y. Chang, Y. C. Lien, L. H. Chu, S. W. Chang, R. C. Huang and H. M. Lee, "Use of WN_X as diffusion barrier for copper airbridged low noise GAAs PHEMT" *Electron. Lett.* **39,** 1763 (2003).

[13] H. Kroemer, "Theory of a wide-gap emitter for transistors", *Proc. IRE* **45**, 1535, (1957).

[14] P. Asbeck et al., "Heterojunction bipolar transistors for microwave and millimeter-wave integrated circuits", *IEEE Trans. Microwave Theory Tech.* **vil**, 1462 (1987).

[15] D. K. Schroder, Semiconductor Material and Device Characterization, Wiley-Interscience, Canada (1998).

[16] W. C. Liu, J. H. Tsai, and S. L. Liu, *IEEE Electron Device Lett.* **13,** 418 (1992).

[17] S. Thomas III, C. H. Fields, M. Sokolich, K. Kiziloglu, and D. Chow: *IEEE Indium Phosphide and Related Materials Conf. Proc*., 286 (2000).

[18] J. F. Jensen, W. E. Stanchina, R. A. Metzger, D. B. Rensch, R. F. Lohr, R. W. Quen, M. W. Pierce, Y. K. Allen, and P. F. Lou, **"**AlInAs/GaInAs HBT IC technology", *IEEE J. Solid-state Circuits* **26**, 415 (1991).

[19] B. Jalali and S. J. Pearton Editors, "InP HBTs: Growth, Processing, and Applications," Artech House, INC (1995).

[20] Peter Madakson, and Joyce C. Liu, "Interdiffusion and resistivity of Cu/Au, Cu/Co, Co/Au and Cu/Co/Au thin films at 25-550 ℃," *J. Appl. Phys.* **68**, 2121 (1990).

[21] H. Miyazaki, H. Kojima, and K. Hinode, "Passivation effect of silicon nitride against copper diffusion", *J. Appl. Phys.* **81**, 7746 (1997).

[22] A. Gupta, A. Young and B. Bayraktaroglu, "InGaP makes HBT reliability a

non-issue", in *GaAs Mantech Tech. Dig.*, 203 (2001).

[23] S. W. Chang, E. Y. Chang, C. S. Lee, K. S. Chen, C. W. Tseng, and T. L. Hsieh, "Use of WN_X as the Diffusion Barrier for Interconnect Copper Metallization of InGaP–GaAs HBTs", *IEEE Trans. Electron Device*s **51**, 1053 (2004).

[24] S. W. Chang, E. Y. Chang, D. BISWAS, C. S. Lee, K. S. Chen, C. W. Tseng, T. L. Hsieh, and W. C. WU, "Gold-Free Fully Cu-Metallized InGaP/GaAs Heterojunction Bipolar Transistor", *Jpn. J. Appl. Phys.* **44**, 8 (2005).

[25] G. Stareev and H. Künzel, G. Dortmann, **"**A controllable mechanism of forming extremely low-resistance nonalloyed ohmic contacts to group III-V compound semiconductors", *J. Appl. Phys*. **74**, 7344 (1993).