24-GHz 互補式金氧半導體電流操作模式射頻前端接受器之設計

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摘　要

本論文提出一個創新的高頻電路設計概念，電流操作模式。並且設計一個操作頻率在 24-GHz 電流操作模式射頻前端接收器，透過國家晶片系統設計中心委託台灣積體電路製造股份有限公司以 0.13 微米互補式金氧半導體製程技術來實現。此射頻前端接收器包含的電路有電流操作模式的低雜訊放大器和電流操作模式的降頻器。整個電流操作模式的射頻接收器已經被完整的設計、製造與量測完成。

量測結果顯示，此射頻前端電路可良好地工作在 24-GHz 的操作頻率，但由於電路佈局上的疏失，量測結果的效能不如當初所預期。在經由雙束型聚焦離子束的補救之後，射頻前端接收器的功率增易為 12.5dB，雜訊指數為 13.3dB，1dB 增易壓縮點為-15dBm，在 1.2V 的操作電壓下共消耗了 41.5mA。

THE DESIGN OF 24-GHz CMOS CURRENT-MODE RECEIVER FRONT-END

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Abstract

A new 24-GHz RF CMOS current-mode receiver integrated with a current-mode LNA and a current-mode downconverter has been proposed and fabricated in a 0.13-um CMOS technology supported by Taiwan Semiconductor Manufacturing Company via Chip Implementation Center. The proposed receiver is completely designed, fabricated and measured.

The measured results exhibit that the receiver can operate well at 24-GHz frequency range. But is doesn't achieve adequate performance due to the oversight of layout. After the FIB solution, the fabricated current-mode receiver has conversion gain of 12.5dB, noise figure of 13.3 dB, a 1-dB compression point of -15 dBm, and drains 41.5mA under 1.2 supply voltage with chip area of 1mm^2.

誌 謝

能夠順利畢業，要感謝的人真的很多。首先，我要對我的指導教授吳重雨老師致上最誠摯的感謝。感謝老師在這兩年中，不論在硬體或軟體資源提供我一個最佳學習環境。並且在學習上，老師適時指導與啟發，使我不在錯誤中打轉，更教導了我許多做事的方法與態度。

再來我要感謝實驗室的學長蕭碩源、周忠昀、王文傑、余繼堯、蘇烜毅、陳旻珓、黃祖德、歐欣華、粘家熒，在這兩年中給予了我許多研究上的幫助與指導，使得我的論文能更佳的出色。還有我要實驗室的同學與學弟們：怡凱、志遠、汝玉、必超、仲朋、允賓、豐維、昌平、泰翔、芳綾、佳惠、資閔、志賢、立龍、國慶、柏宏、順維、晏維、 國忠.....等，在這兩年中我們一起研究功課、遊山玩水，使我的碩士兩年的生活更多采多姿。

最後我要感謝我的女朋友靖雯，謝謝你在這兩年碩士生活中陪伴我走過許多人生的低潮。在我研究上遇到瓶頸時，你的鼓勵與支持讓我走過種種一切的不如意;在我忙碌於研究時，你總是默默的陪伴在我身邊替我加油，讓我能無後顧之憂的向成功邁進。

其他要感謝的人還有很多，無法一一列出，在此一併謝過。

豪傑

于　風城交大

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CHAPTER 1

INTRODUCTION

1.1 Background

In the last two decades, the demand for wireless communication technologies has grown significantly due to the convenient for human life. Wireless communication systems have made great process from bulky to handy as well as from costly to widespread. The main driving force toward building high performance radio-frequency integrated circuits (RFIC) in silicon is the evolution of integrated-circuits techniques.

The Silicon-based technologies, including CMOS and SiGe BiCMOS technology, can integrate the baseband digital, IF analog, and RF front-end circuits on the same die to reduce the cost. Compared to GaAs processes, the inherent semiconductor properties of the silicon substrate have the higher parasitic capacitance and the higher loss with increasing operating frequency and difficult prediction of passive elements at high frequency. In despite of these difficulties, Silicon-based RFIC is still a popular solution for SOC design for wireless communication systems. Because the CMOS technology has the advantages of low cost, high level integration capabilities, low power and short time-to-market, the CMOS have become a competitive technology for RFIC implementation of various wireless communication systems.[1]

Due to the growing demand for larger bandwidth and higher data rate motivates integrated circuits to move toward higher frequencies. RFIC plays the leading roles in high frequency circuits design. In the past decades, high-frequency circuits, such as low-noise amplifiers, mixers and power amplifiers, are usually implemented in Ⅲ/Ⅴ-based technologies or bipolar processes due to their superior device characteristics in high frequency range. However, these processes are usually high-priced and cannot be integrated with general silicon processes that are adopted to fabricate

digital integrated circuits. For this reason, over recent years, CMOS technology is gradually in widespread use to implement an entire communication systems, including RF receiver front-end and baseband circuits.

K-band is a portion of the electromagnetic spectrum in the microwave range of frequencies ranging between 12-GHz and 93-GHz. The frequency range of K-band is between 18-GHz and 26.5-GHz due to the absorbed easily by water vapor (H_2O resonance peak at 22.24-GHz, 1.35 cm). In the recent year, the desires for fixed point-to-point multi-Gigabit wireless communication links and short-range vehicular radar have sparked significant research interest in the 22-29-GHz frequency band. In this thesis, we focus on 24-GHz circuit design application.

In recent year, some of the RF front-end circuit design has been reported with silicon-base or Ⅲ/V-based technologies. All of them are operated as voltage-mode or partial voltage-mode operation. Since the current-mode operation has the advantages of simple structure, lower voltage, lower power consumption and high frequency operation, we attempt to design a 24-GHz RF CMOS current-mode receiver front-end including a current-mode LNA integrated with a current-mode downconverter for K-band applications.

1.2 A Review of CMOS RF Receiver Front-End

A radio-frequency receiver front-end generally consists of a low-noise amplifier (LNA), down-conversion mixer and filters. The LNA amplifies the desired weakly RF signal which received from antenna while introducing a minimum amount of noise to the signal. Since the LNA is the first stage in most receiver front-ends, its noise figure will directly add to that of the system. Mixers perform frequency translation by multiplying signals. The down-conversion mixers employed in the receive path have two distinctly different inputs, called RF port and LO port. The RF port senses the

signal amplified by the LNA to be downconverted and LO port senses the periodic waveform generated by the voltage-controlled oscillator (VCO) and output a lower-frequency signal to feed subsequent stages. Thus, the RF port of the down-conversion mixers must exhibit sufficiently lower noise and high linearity. The latter nearby interferers are amplified by the LNA and hence can produce stronger intermodulation products [2]. The frequency of most RF oscillators must be adjustable. For example, the front-end down-conversion and up-conversion functions must select one of many channels because a given transceiver is assigned different carrier times. Thus, the LO frequency in each case must vary in well-defined steps. If the output frequency of an oscillator can be varied by a voltage, then the circuit is called a voltage-controlled oscillator (VCO) [2]. The filters will suppress the undesired signals for baseband circuits receiving messages with sufficiently low error rate. Fig. 1 shows the common receiver architecture for example.

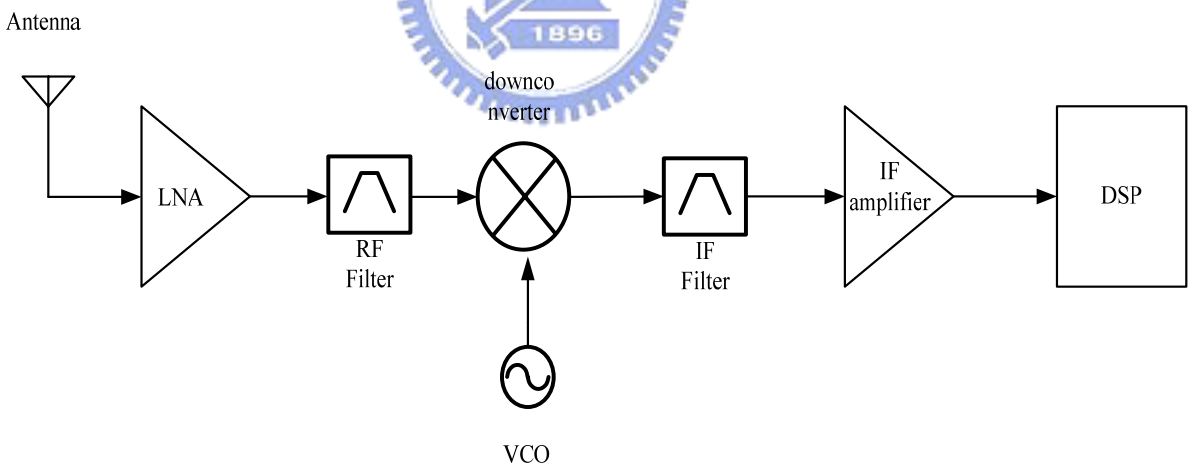


Fig. 1 Common receiver architecture.

1.2.1 High-Frequency CMOS LNA circuit

The LNA is the first block of the RF receiver front-end. Thus, LNA must provide sufficient gain to suppress the noise distribution form the subsequent stages and 50Ohm input impedance matching. Gain can be provided by a single transistor. There are three topologies for a single transistor, as shown in Fig. 2. Each one of the basic amplifiers has many common uses and each is particularly suited to some tasks and not to others.

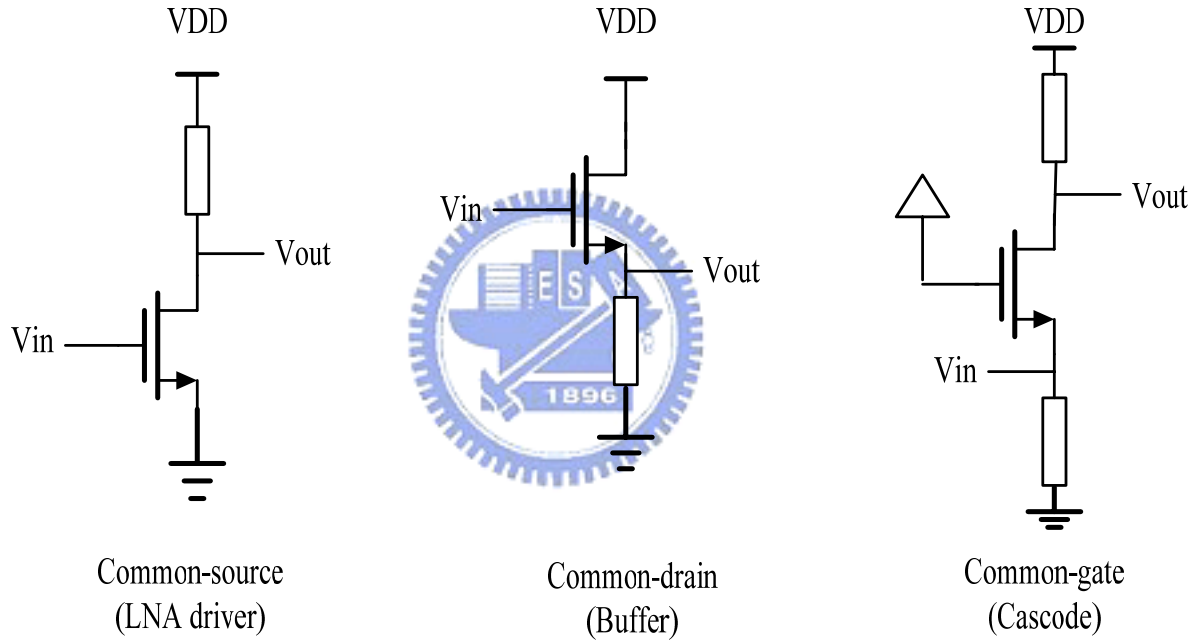


Fig. 2 Single transistor amplifier [3].

The common-source amplifier is most often used as a driver for LNA to provide gain. The common-drain amplifier, with high input impedance and low output impedance, makes an excellent buffer between stages or before the output driver. The common-gate amplifier is often used as a cascade in the combination with the common-source to form an LNA stage with gain to high frequency, but it can be used by itself as well. Since the common-gate amplifier has low input impedance when it is

driven from a current source, it can pass current through it with near unity gain frequency. Therefore, with an appropriate choice of impedance levels, it can also provide voltage gain [3]. The cascode LNA is shown in Fig. 3 and Fig. 4 is the small signal analysis of cascode LNA.

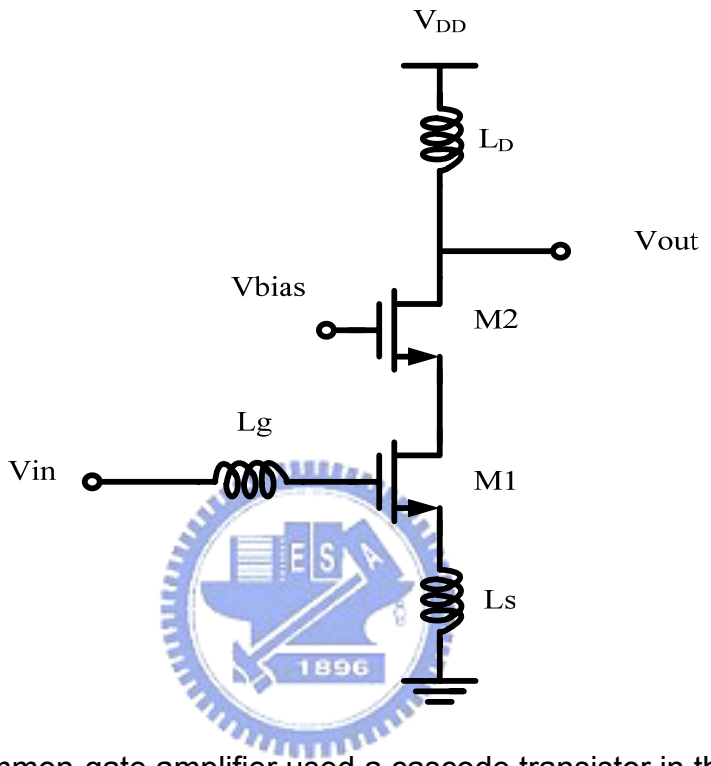


Fig. 3 Common-gate amplifier used a cascode transistor in the LNA [4] .

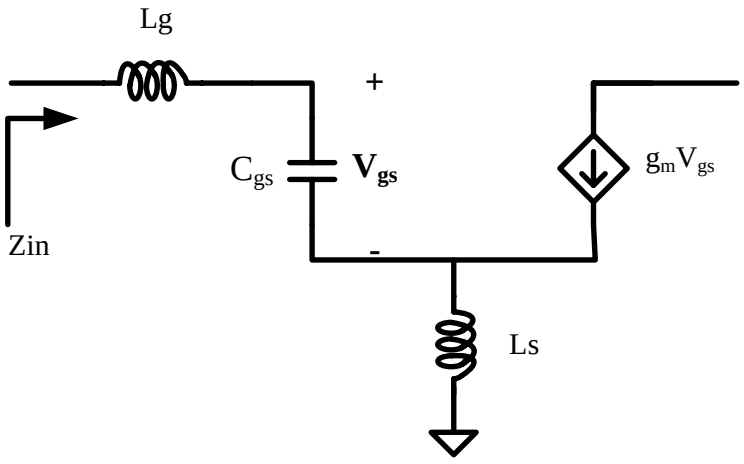
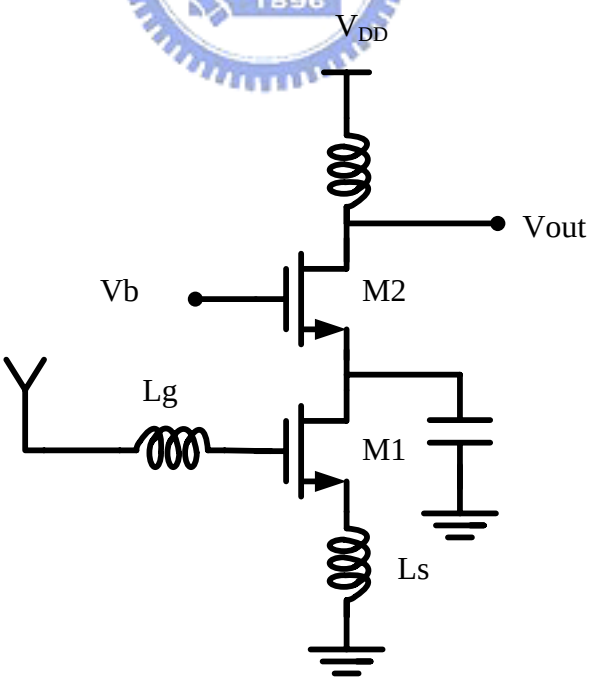


Fig. 4 The input impedance analysis of cascode LNA.

From the Fig. 4, we can easily straightforward analyze the input impedance of the cascode LNA.

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \frac{g_{m1}}{C_{gs}} L_s . \quad (1)$$

Note that L_s contributes a real term to the input impedance through interaction with C_{gs} and g_{m1}. By choosing L_g+L_s to resonate with C_{gs} to create conjugate matching at the input. The inductor L_D provides significant voltage gain. The common-gate transistor of the cascode LNA, M2, plays two important roles by increasing the reverse isolation of LNA: (1) it lowers the LO leakage produced by the follower mixer and (2) it improves the stability of the circuit by minimizing the feedback from the output to input [2]. But the topology of the common-source with inductive degeneration will degrade it performance substantially at higher frequency comparable to ω_T due to the noise factor, F_{min} and effective transconductance, G_m, are linearly related to the working frequency, ω_o and $1/\omega_o$, respectively [5].



(a)

Fig. 5 The high frequency effect of the cascode LNA topology [6].

Above 20GHz, the pole at the drain of M_1 of the cascode LNA showing in Fig. 5 shunts a considerable portion of the RF current to ground, thereby lowering the gain and raising the noise contributed by M_2. Furthermore, the small degeneration and gate series inductances (50-150 pH) required for the input matching make the circuit very sensitive to package parasitic. The above observations suggest that the LNA must contain a single transistor before voltage amplification occurs [6]. Therefore, all of the high frequency LNA circuit design for applications at high-gigahertz range must use a single stage transistor as a first stage amplifier to provide sufficient gain amplification. For example, the 3-stage common-source amplifier is also a popular topology of LNA [7].

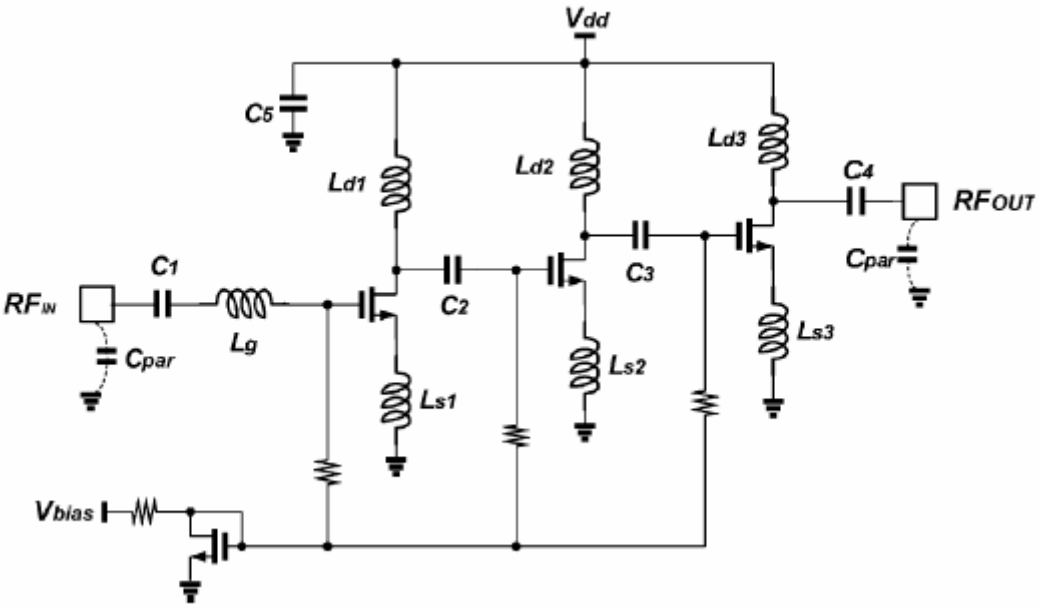


Fig. 6 The simplified schematic of 3-stage common-source LNA [7].

Because the gate-source and gate-drain parasitic capacitances of the common-gate (CG) LNA are absorbed into the LC tank and resonated out at operation

frequency. Due to the constraints of input matching, the CG LNA has a lower bound of $1+\gamma$ for perfect input match, where γ is the channel thermal noise coefficient. Therefore, to the first order, the noise and gain performance of the common-gate stage are independent of the operation frequency, which is a desirable feature for high frequency design [6], [8]. For example in the [8], a 24-GHz CMOS LNA is designed with common-gate with resistive feedback (CGRF) topology. It adds an external resistor, R_p, to the traditional CG LNA in parallel with the input transistor to improve its noise performance, as Fig. 7 shows.

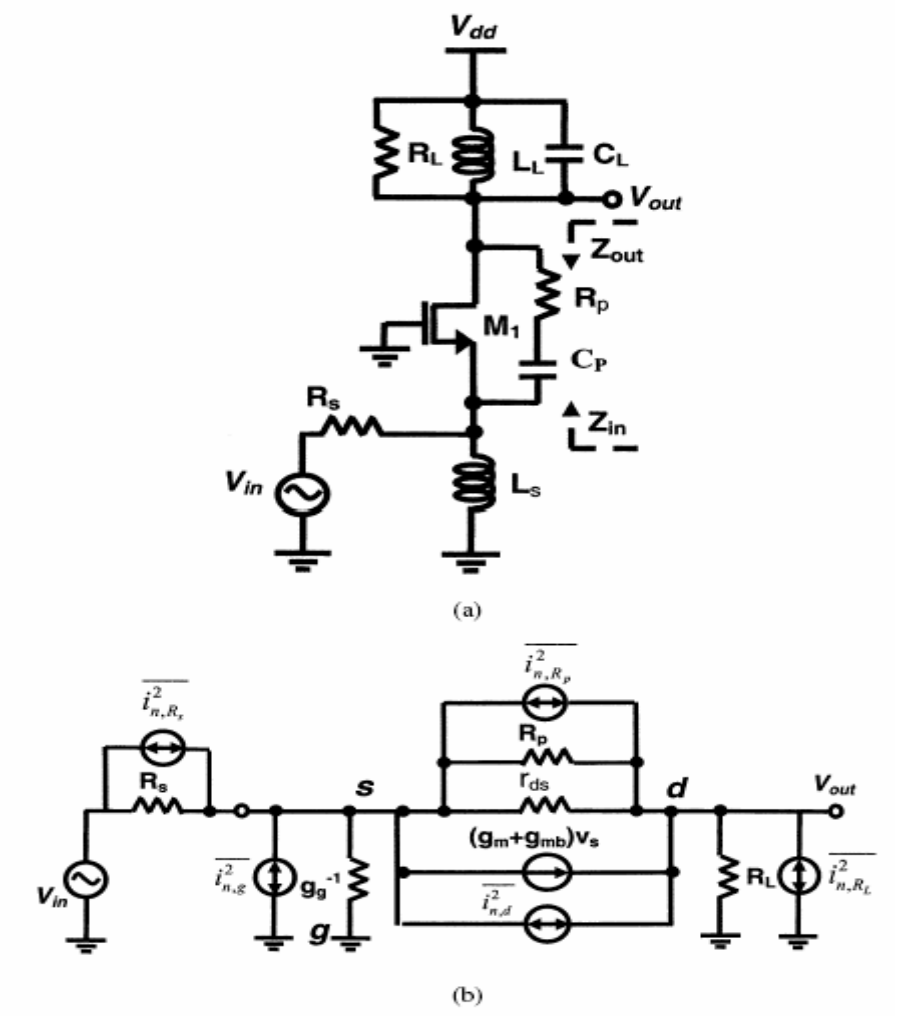


Fig. 7　Common-gate with resistive feedthrough LNA. (a) Schematic. (b) Small-signal equivalent circuits [8].

Fig. 8 shows the 24-GHz CMOS three stage LNA with a CGRF topology as the first stage [8]. The first stage employs CGRF topology, where shunt inductor L_2 resonates the capacitive coupling while introduces a feed-through resistance between drain and source of M_1. A capacitor C_2 isolates the dc level of source and drain. The second and third stages are both common-source with inductive degeneration amplifiers which are used to enhance the overall gain.

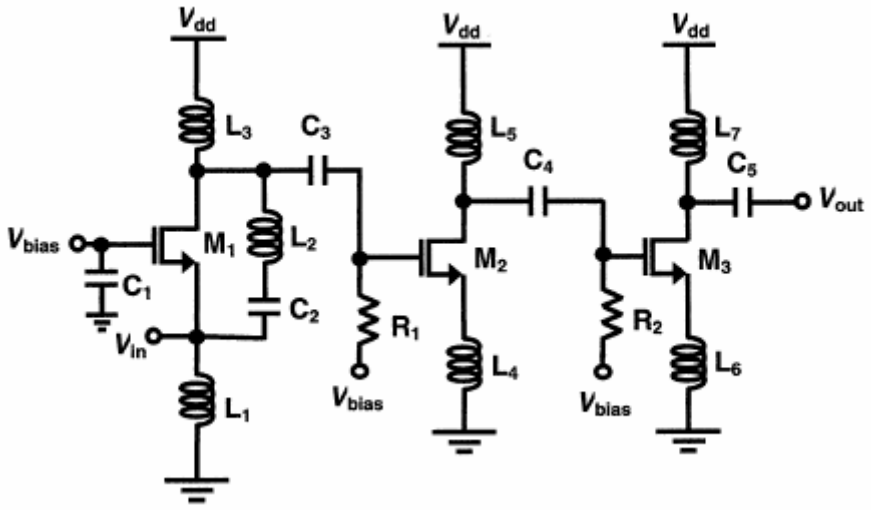


Fig. 8 Three stage LNA with a CGRF topology as the first stage [8]

In recent report about high frequency LNA topology, all of them use a single transistor as the first stage and are realize by voltage-mode or partial-voltage operation. Therefore, we make an attempt to use the current-mirror amplifier to perform a LNA. The current-mirror is also a single stage transistor, not a cascode topology. Because it can bias itself, it doesn't need extra biasing voltage point. Therefore, we use two stage current-mirror amplifiers to realize a LNA. The first stage is a current-mirror with an inductor shunt feedback to provide an input matching and lower the noise figure. The second stage is also a current-mirror amplifier which is

used to enhance the overall gain level. The current-mode LNA with a current mirror topology would be described in chapter 2 particularly. And it has a power gain of 17.1 dB and a noise figure of 3.4dB consuming 9mA from 1.2V supply voltage in the post-simulation result.

1.2.2 CMOS Down-Conversion Mixer

The purpose of the mixer is to convert a signal from one frequency to another. In a receiver path, this conversion is from radio frequency to intermediate frequency. Mixing requires a circuit with a nonlinear transfer function, since nonlinearity is fundamentally necessary to generate new frequencies. Therefore, if an RF input signal and a LO signal are passed through a system with second-order nonlinearity, the output signals will have components at the sum and difference frequencies. A circuit realizing such nonlinearity could be as a simple as a diode followed by some filter to remove unwanted signals. On the other hand, it could be more complex, such as the double-balanced cross-coupled circuit, commonly called the Gilbert cell. In this section, we will focus on CMOS Mixer.

The simple switch used as mixer is shown in Fig. 9. Fig. 9 shows that the output is equal to the RF input when S_1 is on and zero when S_1 is off. Note that the circuit is a linear, time-variant system with respect to RF port and a nonlinear, time-variant system with respect to the LO port. The Fig. 9(b) incorporates a MOS switch to implement the Fig. 9(a). As the RF input signal varies, the gate-source overdrive voltage of M_1 and hence its on-resistance change, introducing nonlinearity in the voltage division between M_1 and R_L.

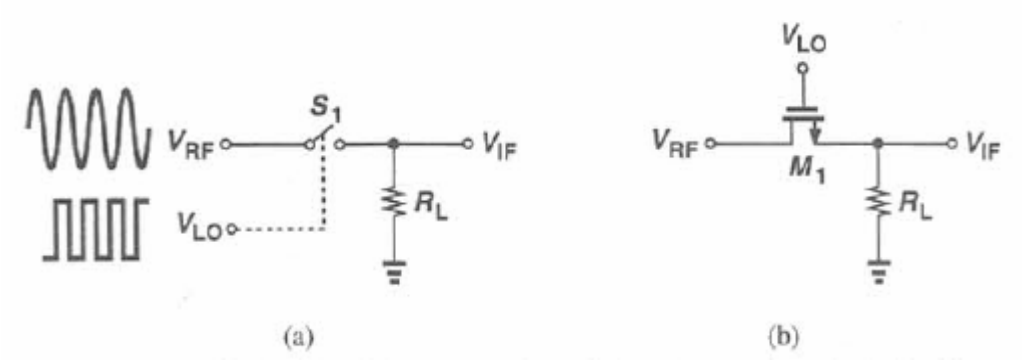


Fig. 9 (a) A simple switch used as a mixer, (b) implementation of switch with a NMOS device.

The most popular mixer topology in the low-gigahertz range is the double-balanced cross-coupled circuit, Gilbert cell as shown in Fig. 10. The Gilbert cell consists of transconductance stage, differential switching pair and load. The transconductance stage generates current in proportional to RF signal. The differential switching pairs perform the chopping operation of the current output of the transconductance stage and thus down-convert the RF signal into the IF band. In order to drive differential pairs sufficiently to turn on and turn off, the LO signal strength should be large enough. If the LO signal is a square wave signal, the IF output current and conversion gain is found easily as the equation (2).

$$I_{IF} = g_{m1}V_{RF}\sin\omega_{RF} * (\frac{4}{\pi})(\sin\omega_{LO}t + \frac{1}{3}\sin\omega_{LO}t + ...) \approx \frac{2}{\pi}g_{m1}V_{RF}\cos(\omega_{RF} - \omega_{LO})t \qquad (2)$$

Thus, the conversion gain is equal to $2/\pi * g_{m1}R_L$.

The double-balance mixer shown in Fig. 10 (b) can eliminate the even-order distortion but its power consumption is also double.

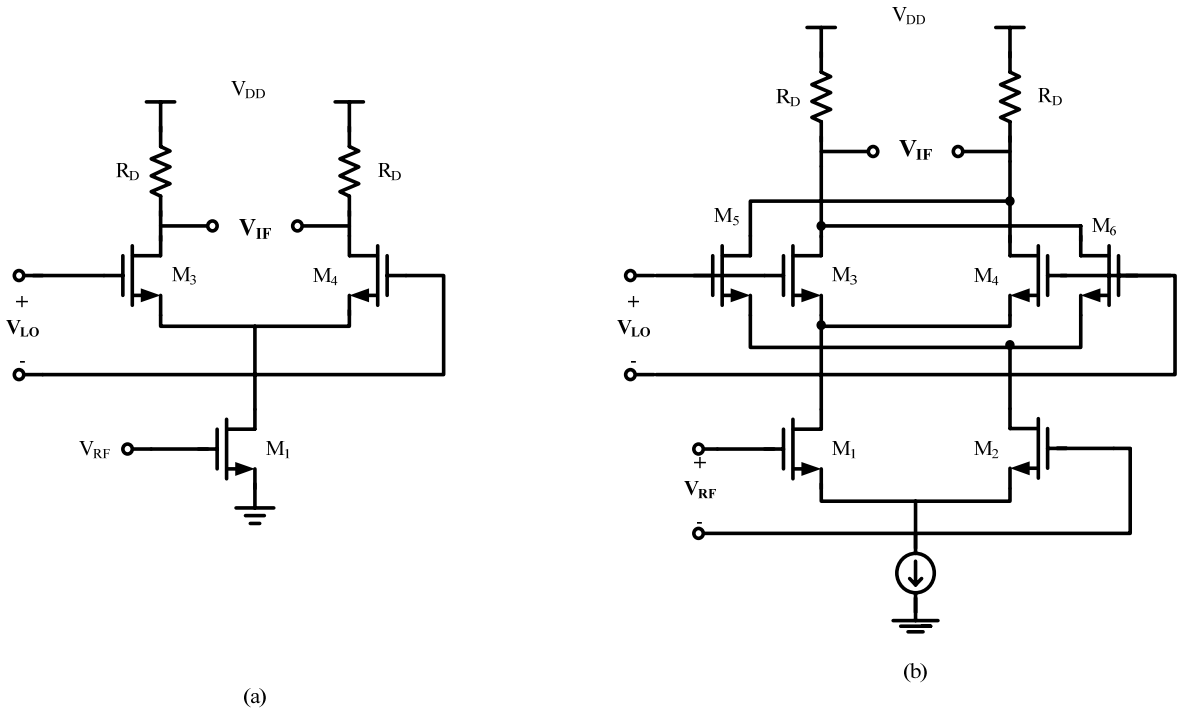


Fig. 10 Gilbert cell mixer. (a) single-balanced, (b) double-balanced.

The conversion gain of Gilbert cell mixer is proportional to R_L. If RL is larger, its conversion gain would be larger with a larger voltage drop. Thus, the current-reuse bleeding mixer [9] bleeds the driver stage current with a current source, the current source being used as part of the driver stage. This topology would provide the better performance in terms of conversion gain, linearity, noise figure and LO isolation. The detailed schematic of current-reuse bleeding mixer is shown in Fig. 11.

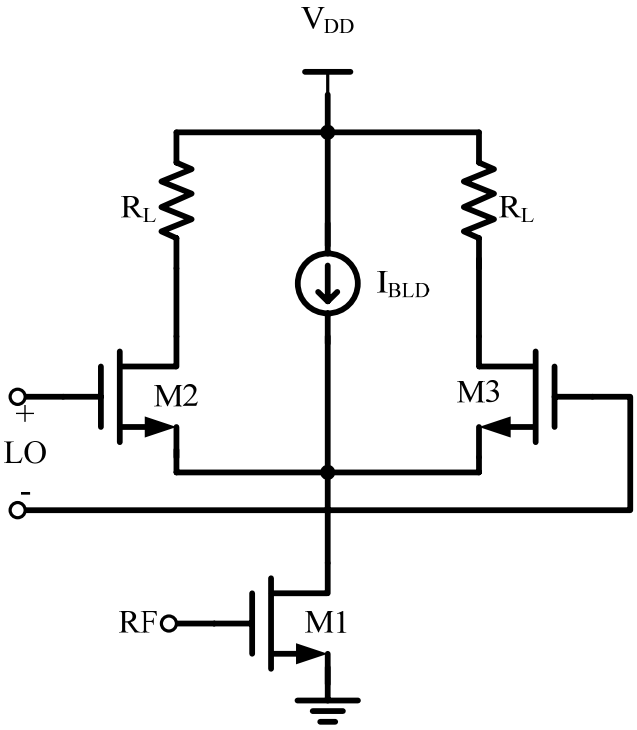


Fig. 11 Schematic diagram of single-balanced mixer with current bleeding

For high frequency mixer, the single-end transconductance mixer is very popular. All of the single-end transconductance mixer could approximately be divided into two portions shown in Fig. 12, gate-pumped and drain pumped mixer respectively.

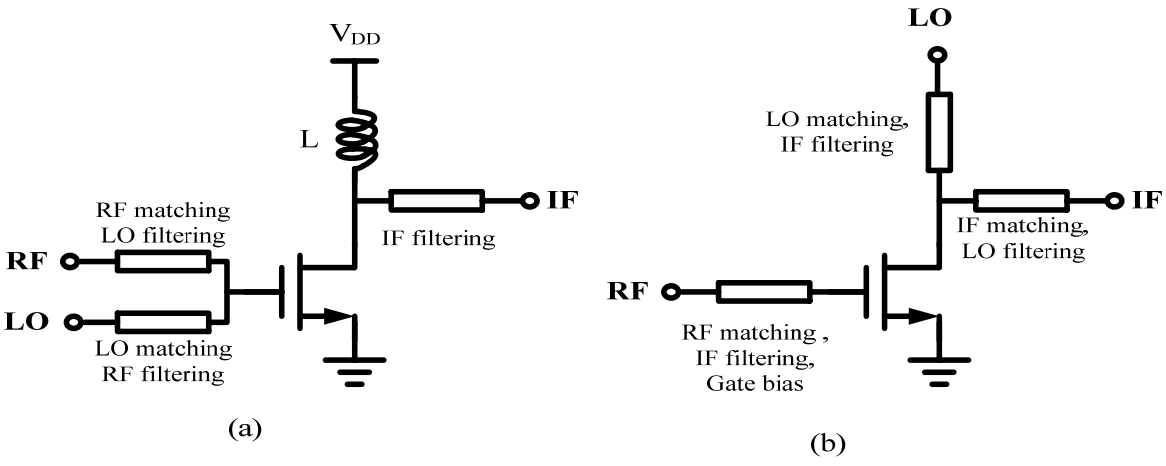


Fig. 12 The simplified schematic of single-end transconductance mixers. (a) gate-pumped mixer. (b) drain-pumped mixer.

The gate-pumped mixer operates in the saturation region with V_{gs} close to the threshold voltage V_{th}, where maximum nonlinearity variations of gm are achieved. Since the LO power would apply with RF signal together and the LO and RF frequency are close for down conversion mixer, the LO to RF and RF to LO isolation are very poor. Typically, the single-gate mixer have one major practical implementation problem which requiring a hybrid power combining circuit to combine the LO and RF signals. Due to the high frequency operation, the hybrid can be easily integrated on-chip. The quadrature balanced mixer that consists of two unit single-end gate-pumped mixer and a 90° branch-line hybrid is shown in Fig. 1.

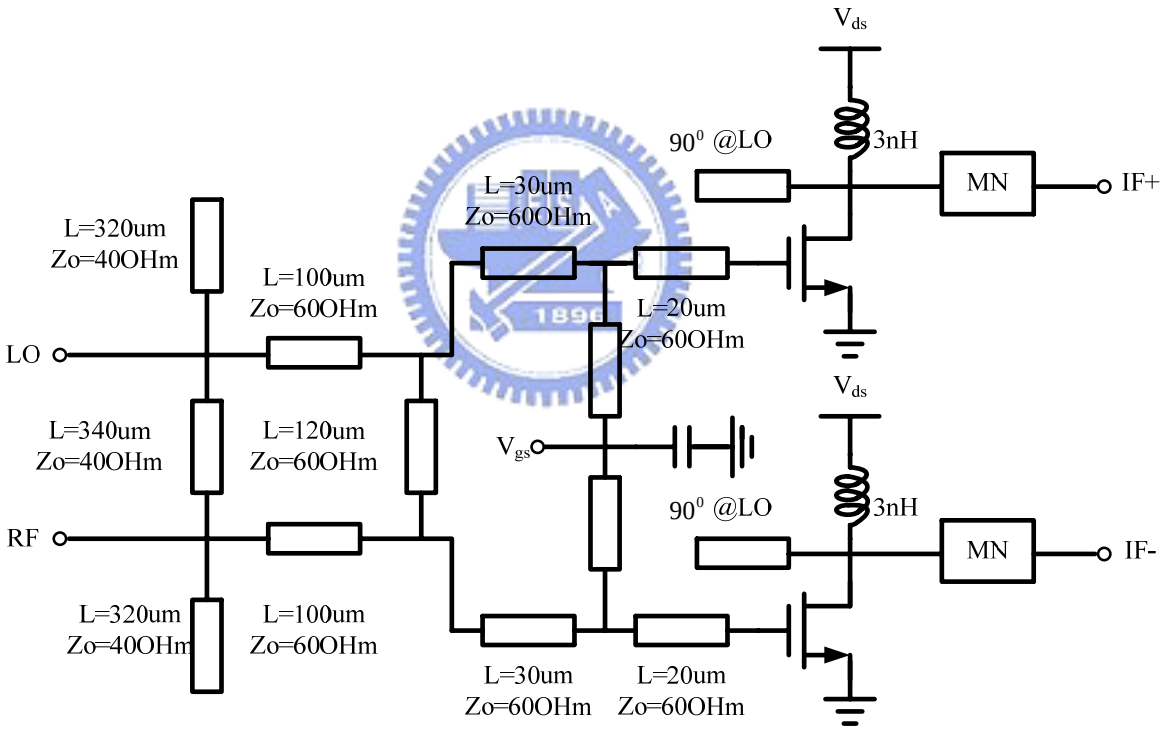


Fig. 13 Simplified circuit diagram of the single-gate quadrature balanced mixer [10]

For drain-pumped mixers, it's LO power is fed at the drain of the transistor. Consequently, gm is a nonlinear function of V_{ds}. The drain-pumped down-conversion mixers have a significant advantage compared to the gate-pumped approach. The RF and LO frequency, which are close to together, are injected at different ports. Thus, the

simplifying the filtering circuit would improve the LO to RF and RF to LO isolation [11].

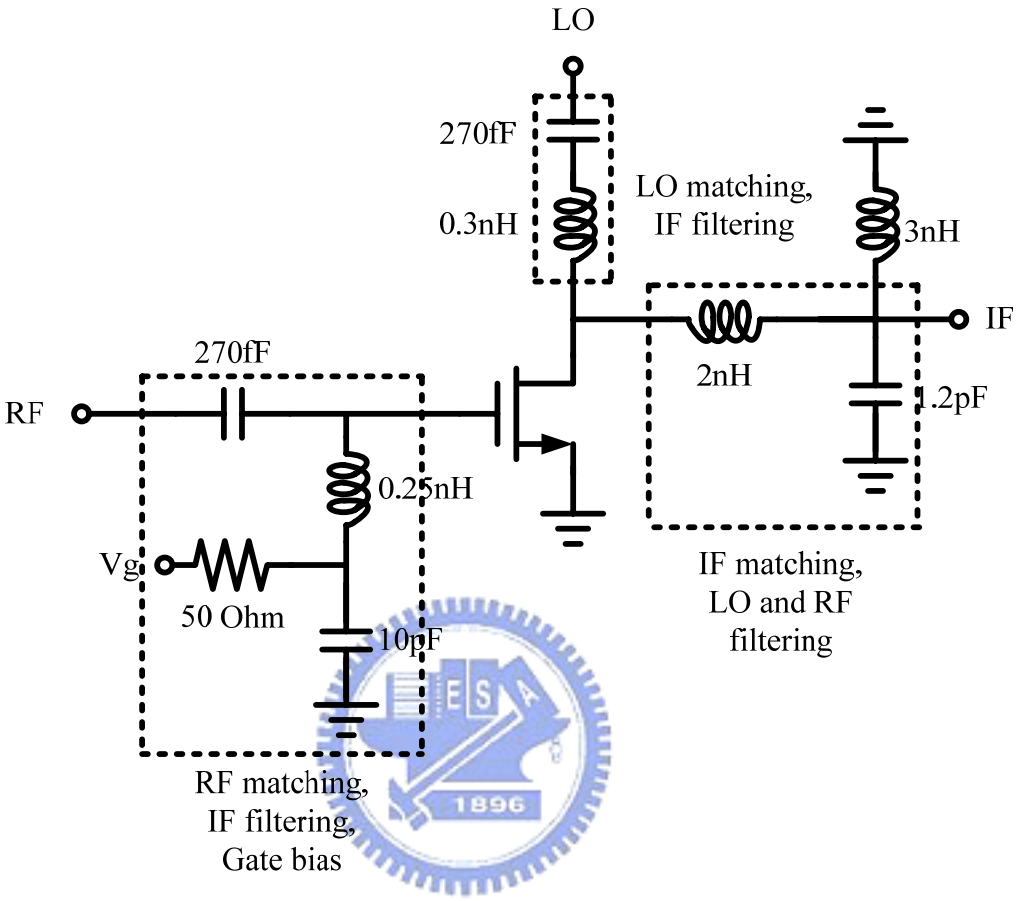


Fig. 14 Simplified circuit schematics of the passive drain-pumped resistive mixer [11]

In above discussion, the most of the CMOS RF mixers are realized by voltage or partial-voltage method. No current-mode approach is discussed for mixer design in high frequency domain. Therefore, a new approach of current-mode mixer is proposed in this thesis. The current-mode mixer is realized the down-conversion function with the multiplication between the RF and LO current signal. The operation method would be introduced in chapter 2 in detail.

1.3 Motivation

Early circuit design principles and techniques for current-mode processing, such as the translinear circuit principal introduced by Barrie Gilbert in 1972 is becoming powerful tools for the development of high performance analogue circuits and systems. The current conveyor is an extremely powerful analogue building block, combining voltage and current mode capability. In recent year, the current-mode circuits and sub-systems have a better performance in much application such as continuous-time and sampled-data filters, A/D and D/A converters, and current-mode neural networks. From above descriptions, we believe that current-mode system would also have the better performance in radio-frequency system. Thus, we would develop a new approach, current-mode operation, to design a 24GHz front-end circuit design with TSMC CMOS 0.13um technology.

1.4 Thesis Organization

Chapter 2 proposes a new approach of current-mode receiver front-end, including the current-mode low-noise amplifier and current-mode mixer, and simulation results. Chapter 3 would illustrate the layout considerations, measurement considerations and setup and experimental results. Finally, the conclusions and future works are described in chapter 4.

CHAPTER 2

CIRCUIT DESIGN AND SIMULATION RESULTS

A new design approach, current-mode operation, will be proposed in this chapter. Using such approach, a low-noise amplifier and a down-conversion mixer are designed and implemented in TSMC 0.13um technology. This chapter is organized as following. In first two sections, the operational principles and design considerations of the current-mode LNA and mixer will be described in detail. Then, the post-simulation results would be illustrated in the last section. Fig. 15 shows the block diagram of the receiver front-end and the circuit blocks implemented in this work also are marked in this figure.

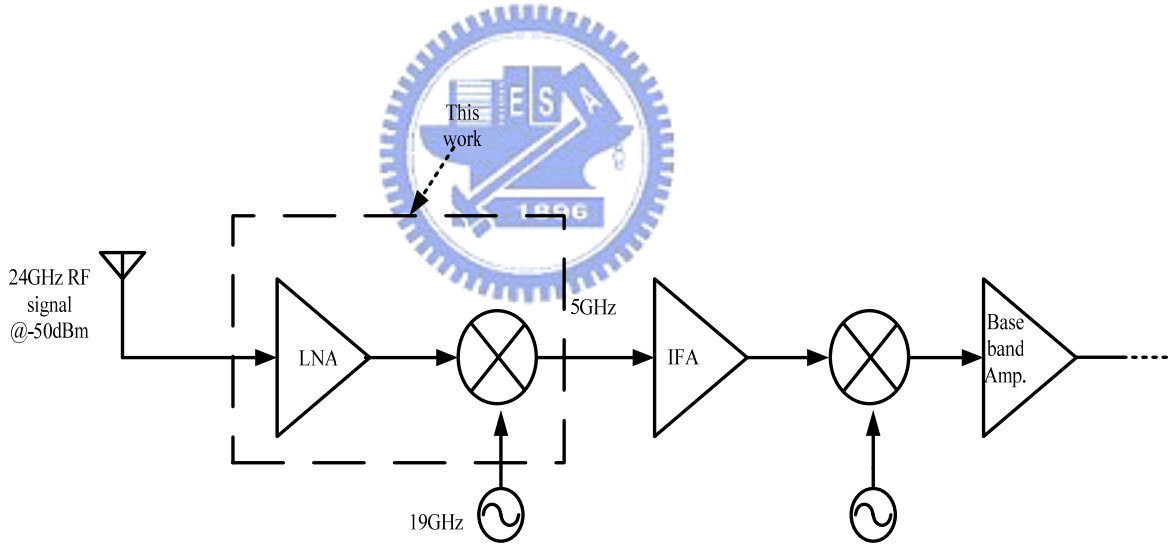


Fig. 15 Block diagram of the current-mode receiver front-end

The current-mode LNA consists of two stages and each is a current-mirror amplifier. The first stage uses a feedback inductor for input impedance and noise matching. The second stage is used to enhance the overall gain performance. The current-mode mixer consists both of I-sum and I-square circuit. The RF frequency is 24-GHz and 5-GHz is selected as the IF frequency.

2.1 Current-Mode Low-Noise Amplifier

Due to the leakage current of parasitic capacitance, the LNA must contain a single transistor before voltage amplification occurs [6]. Therefore, most of LNA in recent report above 20-GHz would use a single transistor as the first input stage [8][21][22][23]. However, all of them are realized by voltage-mode or partial-voltage mode operation. Therefore, a new approach of current-mode operation is proposed and performs a LNA. The current-mirror amplifier is also a single stage transistor, thus the current-mirror amplifier could also avoid the leakage current of parasitic capacitance. The 2-stage cascade current-mirror amplifiers are employed to implement a current-mode LNA.

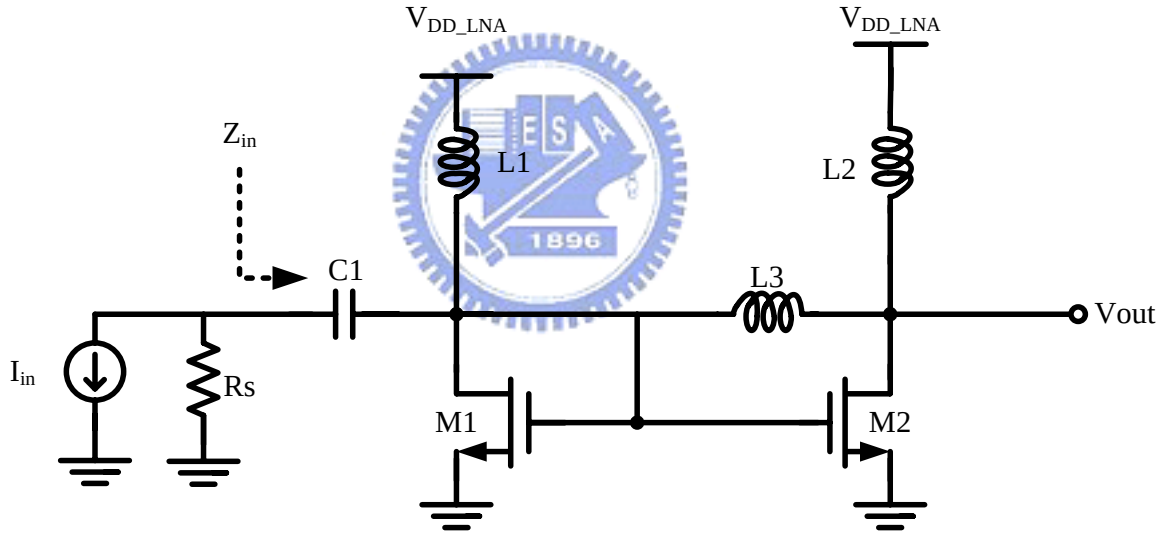
2.1.1 Operational Principle and Design Consideration

The LNA amplifies the desired weakly RF signal received from an antenna while introducing a minimum amount of noise to the signal. Since the LNA is the first stage in the most receiver front-ends, its noise figure would directly add to the noise figure of the system and it must provide an input impedance matching for the maximum power transference.

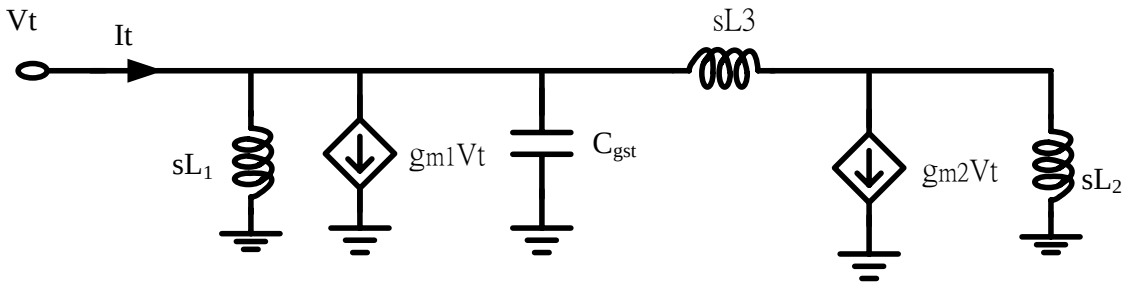
The first stage of current-mode LNA is a current-mirror amplifier with a feedback inductor to improve the input matching and isolation. The second stage is also a current-mirror amplifier which is used to enhance the overall gain level. Thus, the current-mode LNA could be fed the desired RF current signal and generate a greater output current signal with a minimum amount of noise. And the output current signal of current-mode LNA can be injected into the current-mode down-conversion mixer directly.

2.1.1.1 Input Matching Network

The first input stage of current-mode LNA is shown in the Fig. 16(a) and Fig. 16(b) is the small signal equivalent circuits. The value of inductor L_1 is chosen to resonate with the total capacitance seen at the drain terminal of M_1. Therefore, the input current signal can be fed into the transistor of M_1 and use the current mirror pair of M_1 and M_2 to amplify the current signal. For the same reason, the value of inductor L2 is chosen to resonate with the total capacitance seen at the drain terminal of M2. Thus, the output current signal can be fed into next stage. The inductor L_3 provides the shunt feedback loop to improve the input impedance and isolation.



(a)



(b)

Fig. 16 Current-mirror amplifier with inductor feedback. (a) schematic (b) small signal equivalent circuits.

From Fig. 16(b), we could directly derive the value of input impedance of this stage.

$$Z_{in} = \frac{V_t}{I_t} = \frac{sL_3 + sL_2}{1 + \frac{L_2 + L_3}{L_1} + s(g_{m1}L_1 + g_{m2}L_2 + g_{m1}L_3) + s^2 C_{gst}(L_2 + L_3)} \tag{3}$$

When $1 + \frac{L_2 + L_3}{L_1} - \omega^2 C_{gst}(L_2 + L_3) = 0$, the above equation can be simplified to equation (4).

$$Z_{in} = \frac{L_3 + L_2}{g_{m1}L_1 + g_{m2}L_2 + g_{m1}L_3} = \frac{1}{g_{m1} + \frac{L_2}{L_2 + L_3} g_{m2}} \tag{4}$$

Because the size ratio between the transistor of M_1 and M_2 is chosen to decide the ratio of current amplification, the suggestion is to choose the minimum size of transistor M_1. Because the value of inductor L_2 is chosen to resonate with total

capacitance seen at the drain terminal of M_2, the inductor value of L_2 is fixed. Therefore, the value of input impedance can be modulated by change the value both of the transconductance of M_2 and the value of inductor L_3. But, the value of transconductance g_{m2} is involved with the gain, noise figure and power consumption performance. So, the choice of size value of transistor M2 needs to be considered in detail. Therefore, the value of inductor L_3 is the most important key element to adjust the input impedance. The feedback inductor is used to improve the isolation and input matching. Therefore, only one feedback inductor is needed to use in the first stage of current-mode LNA to provide input matching and fine isolation.

2.1.1.2 Noise and Linearity

Low noise figure, low power consumption, high linearity and high gain are the fundamental characteristic in LNA circuit design. But the noise figure, linearity and gain are trade-off with each other for the fixed power consumption. Hence, the optimum value of noise figure, gain and linearity can not be achieved at the same time.

Due to the cascade topology of current-mode LNA, it is significant to understand the effects of cascading on figure-of-merit, such as noise figure and linearity. It is known as Friis's equation [12] that the noise figure of a cascade of signal blocks can easily be shown in the following equation.

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{A_{p1}} + \ldots + \frac{NF_m - 1}{A_{p1} \ldots A_{p(m-1)}} \quad (5)$$

where NF_m is the noise figure of the mth stage evaluated with respect to the driving impedance of the preceding stage and A_{pm} is the power gain if mth stage. Therefore,

the noise contributed by each stage decreases as the gain preceding the stage increases, implying that the first few stage in a cascade are most critical. Similarly, we could estimate the linearity of two stage current-mirror amplifier. The production if intermodulation distortion in each stage is complicated. With some simplifying assumption, we could obtain the following equation [2].

$$\frac{1}{A_{IP3}^2} \approx \frac{1}{A_{IP3,1}^2} + \frac{A_{p1}^2}{A_{IP3,2}^2} + \frac{A_{p1}^2 A_{p2}^2}{A_{IP3,3}^2} + \dots \quad (6)$$

Where $A_{IP3,n}$ denotes the input-referred third-order intercept point of the nth stage and A_{pn} is the power gain of the nth stage. According to the equation (5) and (6), the trade-off between noise figure and linearity are involved with power gain. For example, the noise figure would reduce and linearity worse with a greater power gain. Therefore, the maximal power gain is not the best value. The design issue of the current-mode LNA is to achieve the lower noise figure and a greater power gain with a suitable linearity.

Since the noise figure in the first stage of current mode LNA would directly add to the system. Thus, the first stage of LNA would be performed with a low noise figure and greater gain. Then, the second stage would enhance the overall gain and achieve high linearity performance. However, the biasing voltage and transistor size would be involved with both of the power gain and noise figure performance. Therefore, the biasing voltage and transistor size need to choose carefully.

The noise contribution would be discussed in detail in the first instance. The dominant noise contribution brings from the MOS transistor. Therefore, the noise contribution of the CMOS device would be introduced clearly. The standard CMOS small signal noise model is shown in Fig. 17 [13] and the noise calculation would

adopt this noise model.

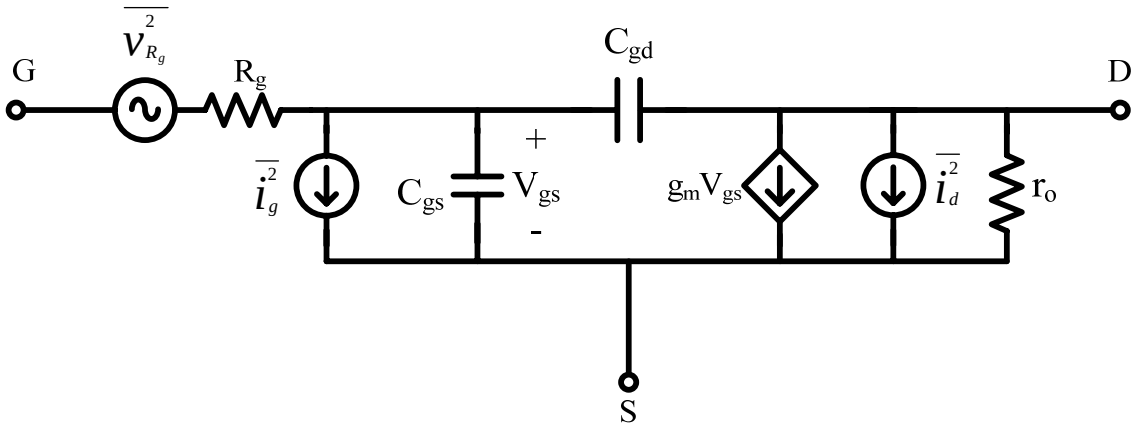


Fig. 17 The standard CMOS small signal noise model [13].

The dominant noise source in the CMOS device is channel thermal noise. This source of noise is commonly modeled as a shunt current source in the output circuit of the device. The channel noise is white with a power spectral density given by

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\gamma g_{d0} \tag{7}$$

The parameter of g_{d0} is the zero-bias drain conductance of the device and γ is a bias-dependent factor that, for long-channel devices, satisfies the inequality

$$\frac{2}{3} \le \gamma \le 1 \tag{8}$$

The value of 2/3 holds when the device is saturated and the value of 1 is valid when the drain-source voltage is zero. For short-channel devices, however, γ does not satisfy equation (8). In fact, γ can be much greater the 2/3 for short-channel devices operating in saturation [14].

This excess noise may be attributed to the presence of hot electrons in the channel. The high electric fields in sub-micron MOS devices cause the electron temperature, T_e, to exceed the lattice temperature. The excess noise due to carrier

heating was anticipated by van der Ziel as early as 1970 [15].

Then, an additional source of noise in MOS devices is the noise generated by the distributed gate resistance [16]. This noise source could be modeled by a series resistance in the gate circuit and an accompanying white noise generator. By interdigitating the device, the contribution of this noise source could be reduced to insignificant levels. For noise purposes, the effective gate resistance is given by [17]

$$R_g = \frac{R_{\square} W}{3n^2 L} \tag{9}$$

where $R_{\square}$ is the sheet resistance of the polysilicon, W is the total gate width of the device, L is the gate length and n is the number of gate fingers used to layout the device. The factor of 1/3 arises from a distributed analysis of the gate, assuming that each gate finger is contacted only at one end. By contacting at both ends, this term reduces to 1/12. In addition, this expression neglects the interconnect resistance used to connect the multiple gate fingers together. Interconnect can be routed in a metal layer that possesses significantly lower sheet resistance and hence is easily rendered insignificant. Its significance is further reduced in silicided CMOS process which possess a greatly reduced sheet resistance, $R_{\square}$. Due to the TSMC CMOS 0.13um technology which is a silicided CMOS process, the noise source of gate resistance would be neglected when calculating the noise contribution.

The gate-induced noise is proceeded to introduce. When the device is biased so that the channel is inverted, fluctuations in the channel charge would induce a physical current in the gate due to the capacitive coupling. At frequencies approaching ω_T, the gate impedance of the device exhibits a significant phase shift from its purely capacitive value at lower frequencies. This shift could be accounted by including a real conductance, g_g, and a shunt noise current, $\overline{i_g^2}$. Mathematical expressions for these sources are

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g \tag{10}$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \tag{11}$$

where δ is the coefficient of gate noise, classically equal to 4/3 for long-channel devices. The equations of (10) and (11) are valid when the device is operated in saturation. However, in the gate noise expression, g_g is proportional to ω^2 and hence the gate noise is not a white noise source. Therefore, Fig. 18 is the simplified small signal noise model which neglected the C_{gd} capacitance for convenient estimation. The Fig. 18 would apply to estimate the noise contribution of current-mode LNA.

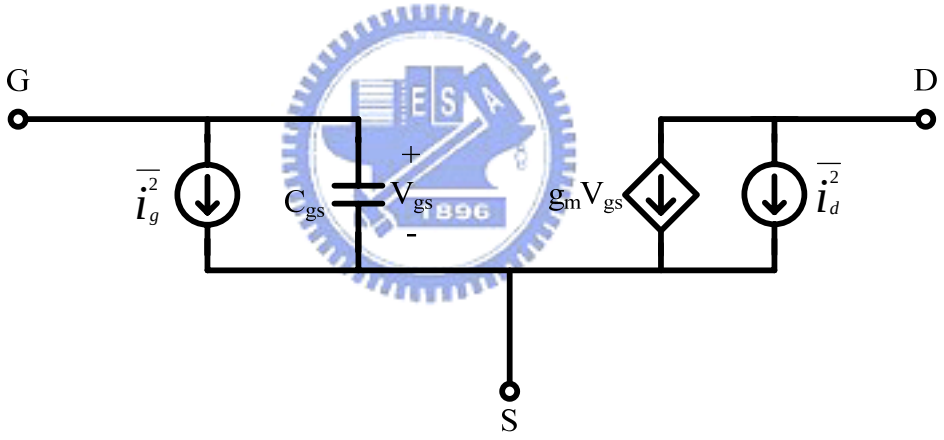


Fig. 18 The simplified small signal noise model.

The noise performance of a circuit is usually characterized by a parameter called noise factor (*F*) or noise figure ($NF \equiv 10\log F$) that represents how much the given system degrades the signal-to-noise ratio [18].

$$F \equiv \frac{SNR_{in}}{SNR_{out}} \tag{12}$$

$$F = \frac{Total \quad output \quad noise \quad power}{Total \quad output \quad noise \quad power \quad due \quad to \quad souece \quad only} \tag{13}$$

The simplified schematic diagram of noise source distribution of input stage is shown in Fig. 19. And the small signal equivalent circuit for noise calculation is shown in Fig. 20 where the channel thermal noise power of the m[th] MOS device is $\overline{i_{n,m}^2}$ equal to $4kT\gamma g_{do,m}$, the gated-induced noise power of the m[th] MOS device is $\overline{i_{g,m}^2}$ equal to $\frac{\omega^2 C_{gs,m}^2}{5g_{d0,m}}$ and the thermal noise power of R_S is $\overline{i_{R_S}^2}$ equal to $\frac{4kT}{R_s}$.

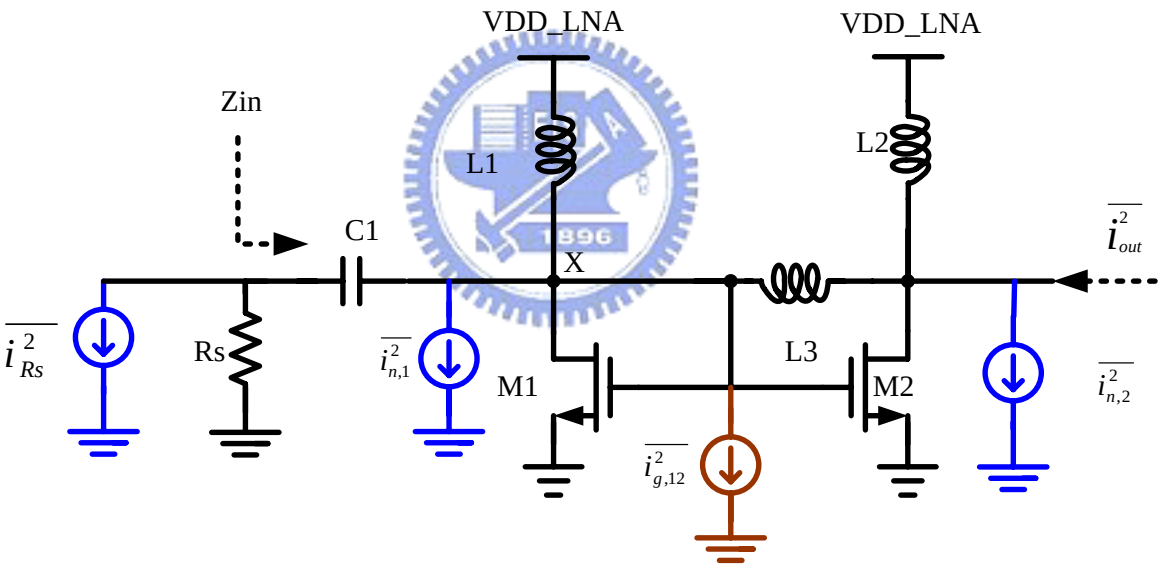


Fig. 19 The noise source distribution of the input stage.

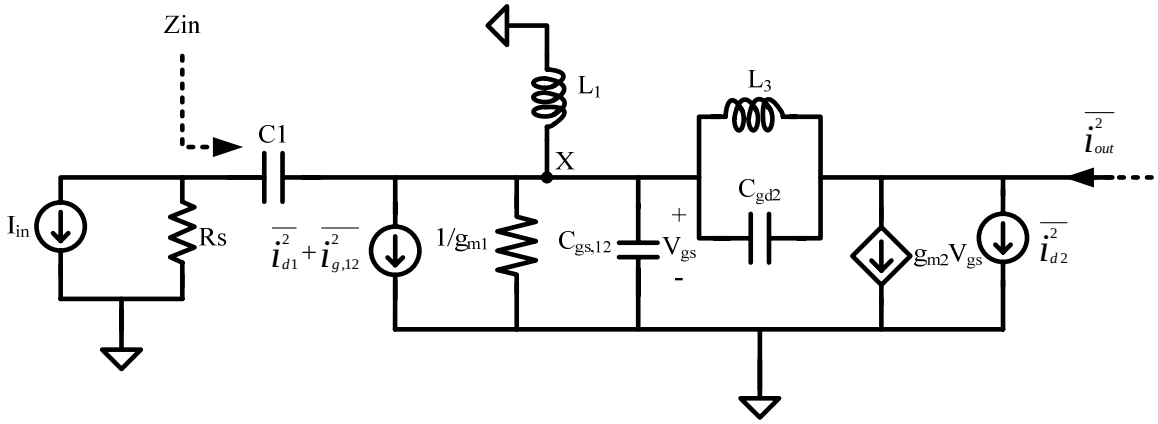


Fig. 20 The small-signal circuit of input stage for noise calculations.

For noise calculation, the output noise power is estimated with some of the reasonable assumption. First, the inductor, L1, would resonate with the total parasitic capacitance at X node including the $C_{gs,12}$. Second, the inductor, L3, would resonate with C_{gd2}. From the diagram of Fig. 20, the output noise power $\overline{i_{n,out}^2}$ could be driven as following equation (14).

$$\overline{i_{n,out}^2} \approx (\overline{i_{R_S}^2} + \overline{i_{d1}^2} + \overline{i_{g,12}^2}) * (R_s // Z_{in})^2 * g_{m2}^2 + \overline{i_{d2}^2} \tag{14}$$

Due to the definition of equation (13), the noise factor of input stage of the current-mode LNA is presented as the following equation.

$$\begin{aligned} NF &= \frac{\overline{i_{n,out}^2}}{\overline{i_{R_S}^2} * (R_s // Z_{in})^2 * g_{m2}^2} \\ &\approx 1 + R_s(\gamma g_{d0,1} + \delta \frac{\omega^2 C_{gs2}^2}{5 g_{d0,2}}) + R_s * \frac{\gamma g_{d0,2}}{(R_s // Z_{in})^2 * g_{m2}^2} \end{aligned} \tag{15}$$

From above equation, the noise figure performance is involved with the C_{gs}, g_{do},

operating frequency and input impedance, Z_{in}. However, the value of C_{gs} is proportional to the size value of transistor. The biasing voltage would influence the value both of g_{d0} and Z_{in}. In order to obtain the minimum noise figure, the optimum value both of transistor size and biasing voltage would be chosen with the simulator tools. The setup of NF_{mim} versus V_{GS} simulation is shown in Fig. 21.

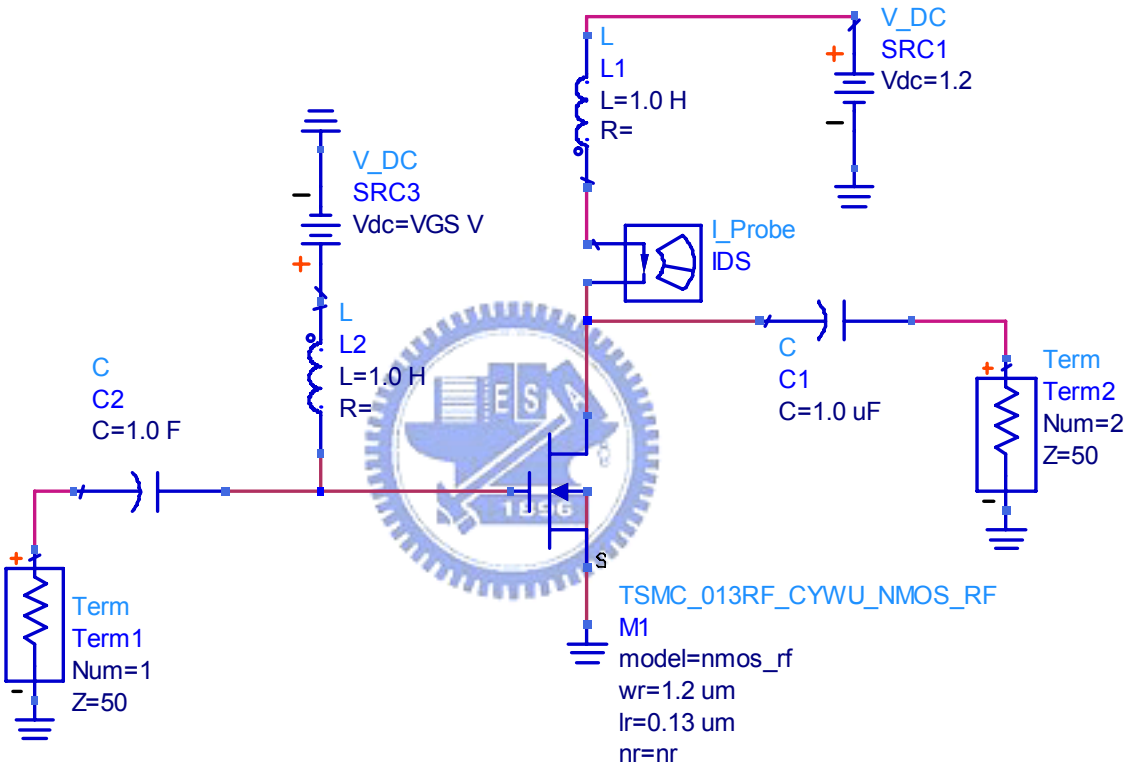


Fig. 21 The setup of NF_{min} versus V_{GS} simulation.

The parameter of nr is the finger number of transistor. The simulation results are shown in Fig. 22, the diagram of minimum noise figure versus biasing voltage, V_{GS}, with different transistor size. Then, the simulation result of the power gain, dB(S(2,1)), versus V_{GS} with different transistor is shown in Fig. 23.

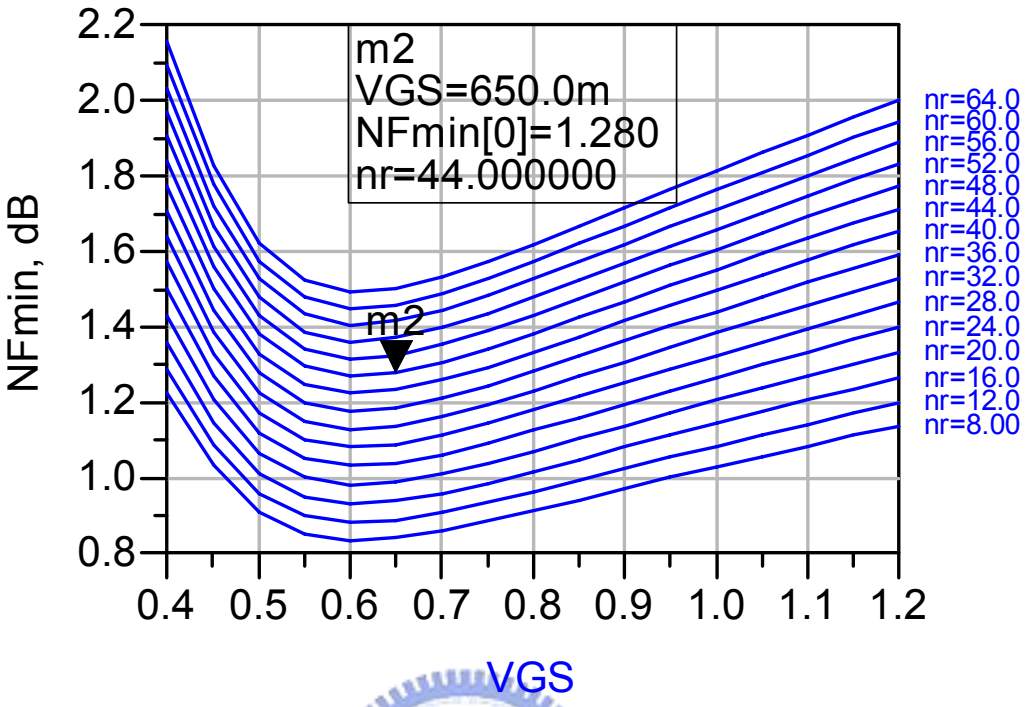


Fig. 22 The simulation result of minimum noise figure versus V_{GS}.

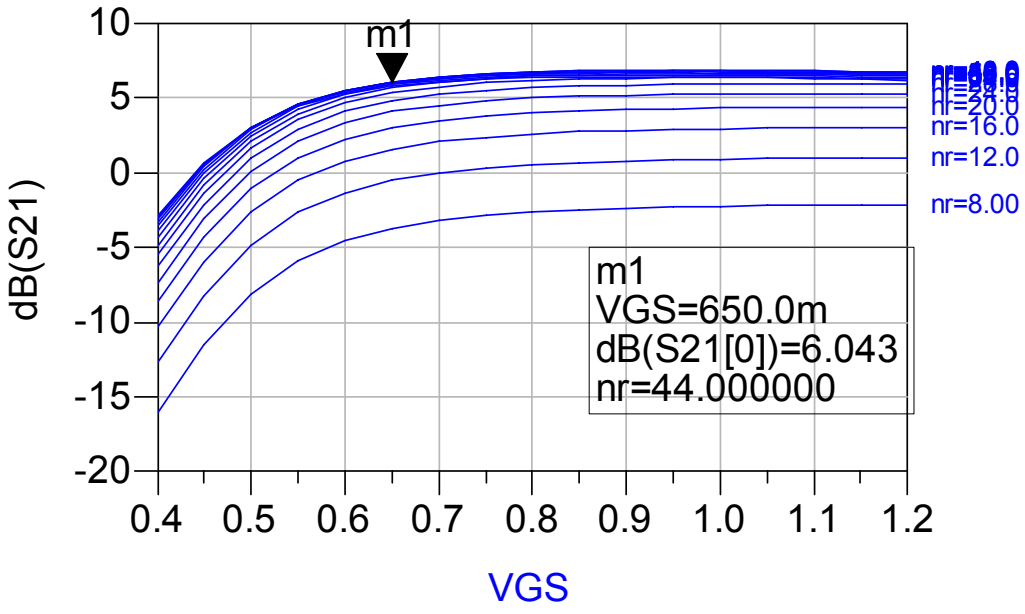


Fig. 23 The simulation result of dB(S(2,1)) versus V_{GS}.

From the simulation results, the noise figure would be worse with both of the larger transistor size and higher biasing voltage. But the power gain performance is greater with larger transistor size and biasing voltage. Thus, the minimum noise figure, power gain and power consumption are a trade-off. The design issue in this thesis is to achieve the lower noise figure with a suitable power gain and acceptable power consumption.

The linearity of the transistor is also involved with biasing voltage. Unfortunately, in the condition of the best noise figure performance is always the worst case of linearity performance. The Taylor series is used to expand the drain current. The drain current in Taylor expansions could be expressed as following:

$$i_{ds}(v_{GS}) \approx I_{DS}(V_{GS}) + g_m v_{gs} + g_m^{'} v_{gs}^2 + g_m^{''} v_{gs}^3 + \ldots \quad (16)$$

The third-order intercept point (A_{IP3}) of gate voltage amplitude is shown as the following equation.

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{g_m}{g_m^{''}}\right|} \quad (17)$$

where g_m is the transconductance of transistor and $g_m^{''}$ is the second-order differential of transconductance. And the simulation results about g_m and $g_m^{''}$ are shown in Fig. 24.

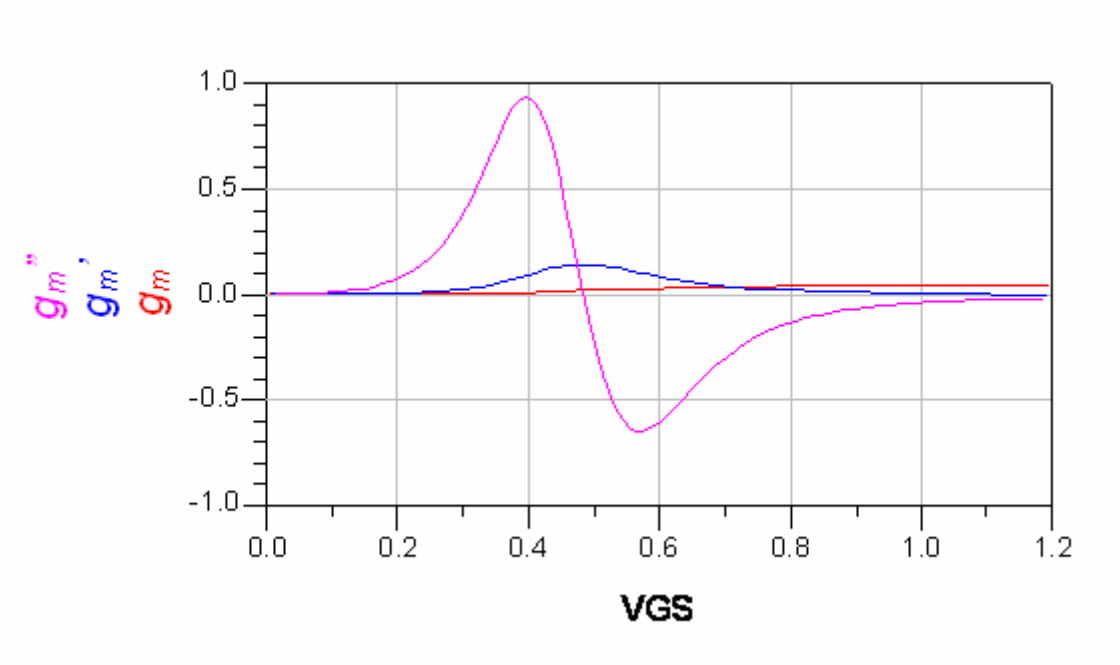


Fig. 24 The transconductance of transistor device.

From the simulation result of Fig. 24, the worst case of the third-order intercept point occurs at the biasing voltage of 550mV. But, the biasing voltage of 550mV is the best value of noise figure performance. From the simulation results of Fig. 22, Fig. 23 and Fig. 24, the value of biasing voltage is chosen as 650mV with a lower noise figure, suitable power gain, acceptable power consumption and linearity.

2.1.2 Circuit Implementation

Fig. 25 shows the schematic of current-mode LNA in the receiver and Table(i) list the detailed parameters of each device. In the schematics, the MOS transistor pairs of $M_{1,2}$ and $M_{3,4}$ operate as the current-mirror amplifier. Due to the different power supply voltage between LNA and Mixer, the MOS transistors of M_5, M_6 and M_7 are the diode connected MOS transistors employed to provide a suitable voltage drop for the same supply voltage in LNA and downconverter circuit. The inductors of L_1, L_2 and L_3 would resonate with the total capacitance seen from the drain node of M_1, M_2 and M_4,

respectively, to present high impedance for the RF signal. Also, the inductors of L_1, L_2 and L_3 behave as DC current source. They provide the necessary DC bias current without requiring extra voltage headroom. Besides, an additional advantage is to nullify the parasitic capacitances of the MOS transistors, resulting in an improvement of the noise figure [19]. The inductor of L_4 is used to provide an inductor shunt feedback to improve the isolation and the input matching. Therefore, only one feedback inductor is needed to use in the first stage of current-mode LNA to provide input matching and fine isolation. The capacitor of C_1 and C_2 are used as the block capacitors at input and output terminals, respectively. The capacitor of C_3 is used to provide a stable AC ground.

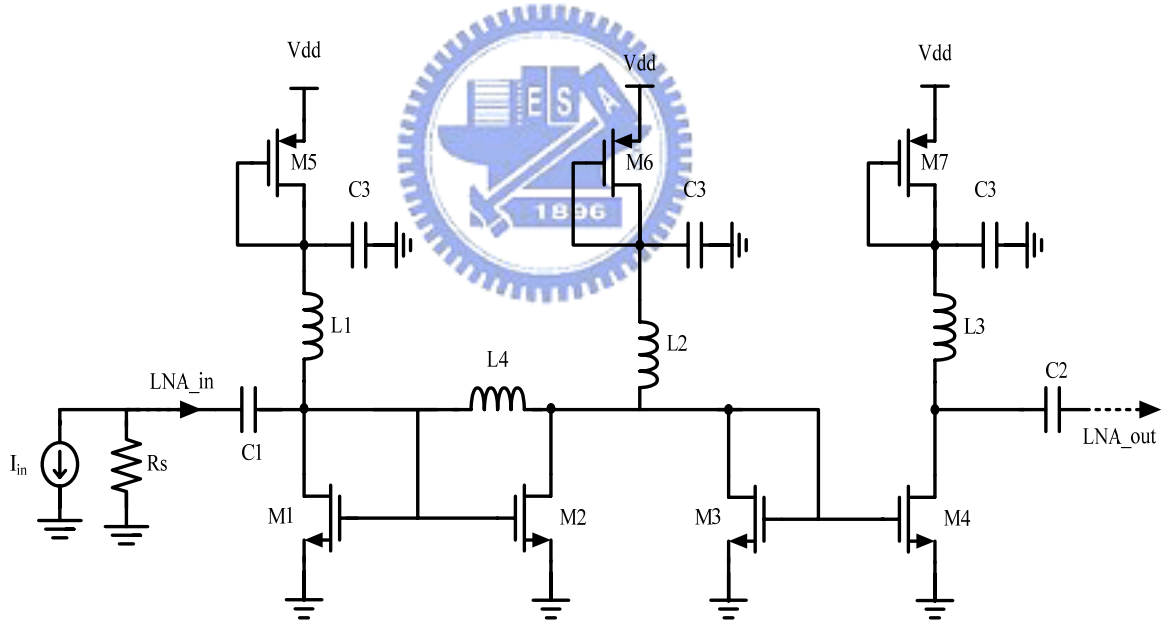


Fig. 25 The complete schematic of current-mode LNA.

Table(i) Detailed parameters of the current-mode LNA

$M_{1,3}$	RF_MOS	1.2um*1/ 0.13um
M_2	RF_MOS	1.2um*44 / 0.13um
M_4	RF_MOS	1.2um*26 / 0.13um
M_5	RF_MOS	5.0um*30 / 0.13um
$M_{6,7}$	RF_MOS	8.0um*30 / 0.13um
C_1	Mmcap_um	9.0um*9.0um (89.4 fF)
C_2	Mmcap_um	7.5um*7.5um (62.996 fF)
L_1	Spiral_std	rad= 15um w=9 nr=1.5 (297.81 pH)
$L_{2,3}$	Spiral_std	rad= 15um w=3 nr=1.5 (314.5 pH)
L_4	Spiral_std	rad= 32.5um w=3 nr=1.5 (506.7 pH)

2.2 Current-Mode Down-Conversion Mixer

The purpose of the mixer is to convert a signal from one frequency to another. In a receiver path, this conversion is from radio frequency to intermediate frequency. Frequency mixing requires a circuit with a nonlinear transfer function, since nonlinearity is fundamentally necessary to generate new frequencies. Therefore, if an RF input signal and a LO signal are passed through a system with second-order nonlinearity, the output signals will have components at the sum and difference frequencies. In the past research, most of the CMOS RF mixers are realized by voltage or partial-voltage method. No current-mode approach is discussed for mixer design in high frequency domain. Therefore, a novel aspect of current-mode mixer is proposed in this section.

2.2.1 Operational Principle and Design Consideration

Most of the high frequency CMOS mixers are realized the down-conversion function with the multiplications between RF and LO voltage signal. The Gilbert cell mixers and single-end transistor mixers are the most popular topologies. In this section, a new approach of current operation mixer is proposed. In opposite to the voltage mode or partial-voltage mode mixer, the current-mode mixer is realized the down-conversion function with the multiplication of the RF and LO current signal. Therefore, the I-sum and I-square circuits are necessary to perform the current-mode mixer. The I-Sum circuit would sum the current both of RF and LO ports and feed the output summing current into the I-square circuit to perform the current multiplication of RF and LO current signal. Fig. 26 shows the block diagram of current-mode mixer and the operation of circuit blocks in this work also are marked in this figure.

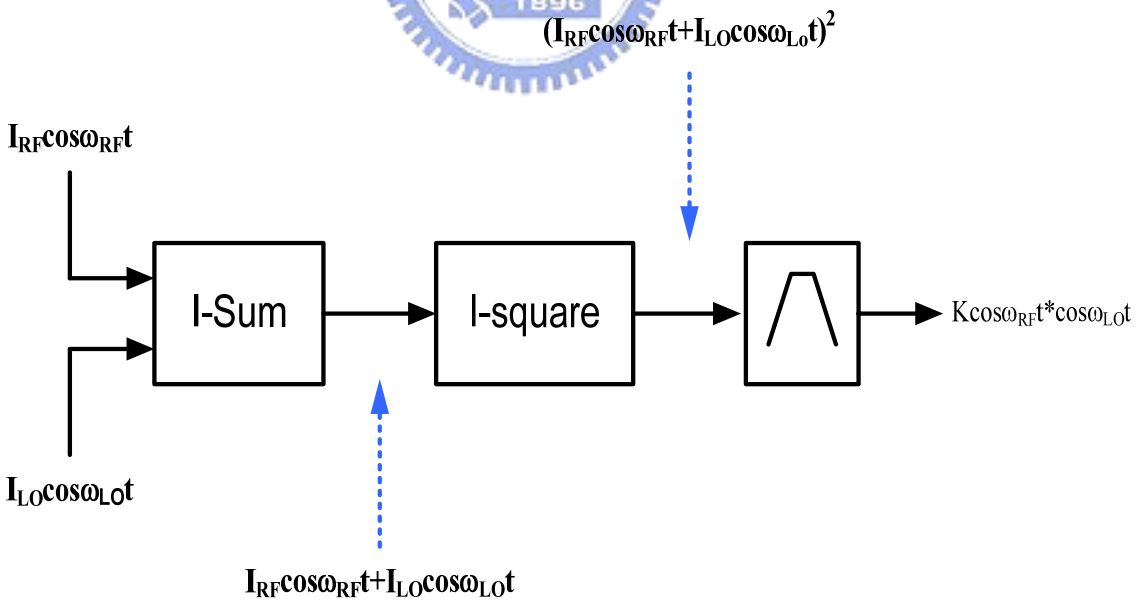


Fig. 26 The block diagram of current-mode mixer

2.2.1.1 Current-summing circuit

For the operation of current mixing, the I-sum circuit is used to sum the RF and LO current signal. Then, the summing current both of the RF and LO port would be fed into the I-square circuit to perform the current multiplication as the down-conversion function. The current summing function is operated with two common-gate transistors connected the drain terminal together. Fig. 27 shows the I-sum circuit. The L_{s1} and L_{s2} resonate with the total parasitic capacitance seen at the source of the transistor M_{s1} and M_{s2}, respectively. The resonance would provide high impedance. Therefore, the current signal both of the RF and LO port would be fed into common-gate transistors to perform the current summing operation. The inductor L_{s3} resonates with the total parasitic capacitance seen at the output node of current summing circuit. For the same reason, the output current signal of I-sum circuit would be fed into the current squaring circuit to perform the operation of current multiplication.

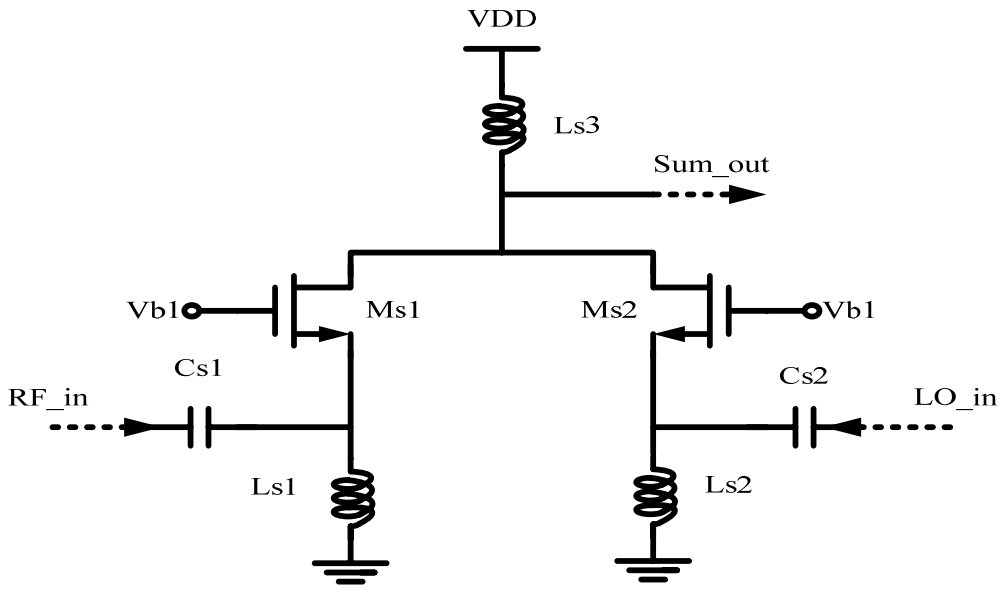


Fig. 27 The current summing circuit.

2.2.1.2 I-square circuit

In this section, the I-square circuit would be discussed in detail. Fig. 28 is the simplified circuit of the current squaring.

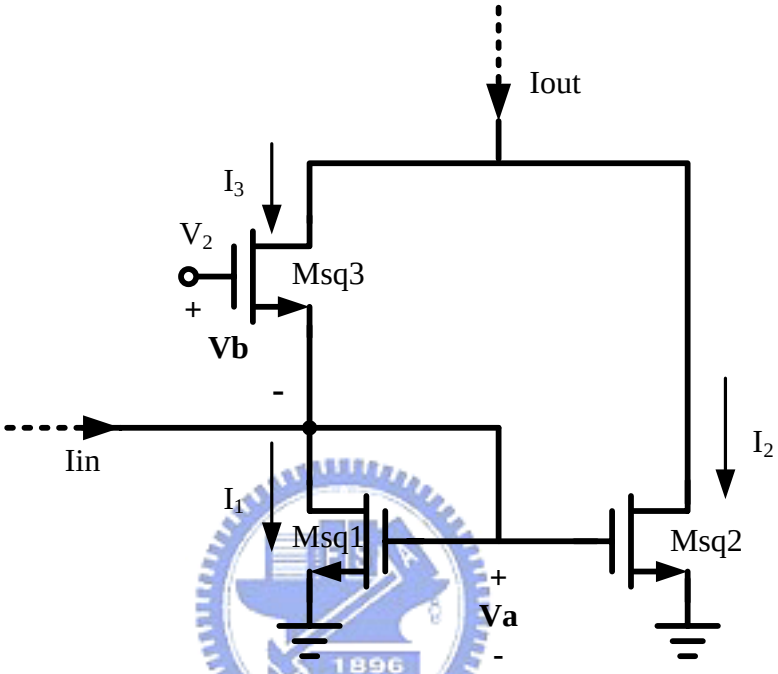


Fig. 28 The simplified current squaring circuit.

Before the derivation of the current squaring function, some of the assumptions would be considered. First, the transistors of M_{sq1}, M_{sq2} and M_{sq3} are operated in the saturation region and all of threshold voltage is the same. Second, the value of $k_1(W/L)_1$ is equal to the value of $k_2(W/L)_2$ and $k_3(W/L)_3$. Thus, all of them are respected as the symbol of K. The I_{in} is the ac signal of input current. From the Fig. 28, some of the equality could be obtained easily.

$$I_{in} = I_3 - I_1 \tag{18}$$

$$I_1 = K(V_a - V_t)^2 \tag{19}$$

$$I_3 = K(V_b - V_t)^2 \tag{20}$$

$$V_2 = V_a + V_b \tag{21}$$

From the above equation, the equation of I_{in} could be derived as following:

$$I_{in} = I_3 - I_1 = K(V_2 - 2V_t)(V_b - V_a) \tag{22}$$

$$\Rightarrow V_b - V_a = \frac{I_{in}}{K(V_2 - 2V_t)} \tag{23}$$

Thus, the correlation between V_a, V_b and I_{in} could be obtained. From the correlation between equation (21) and (23), the value of *Va* and *Vb* could attain.

$$V_b = \frac{V_2}{2} + \frac{I_{in}}{2K(V_2 - 2V_t)} \tag{24}$$

$$V_a = \frac{V_2}{2} - \frac{I_{in}}{2K(V_2 - 2V_t)} \tag{25}$$

Intuitively, the summing current of I_1 and I_3 would have the current squared the input current, I_{in},

$$I_1 + I_3 = \frac{1}{2}K(V_2 - 2V_t)^2 + \frac{I_{in}^2}{2K(V_2 - 2V_t)^2} \tag{26}$$

Due to the current mirror pair of M_{sq1} and M_{sq2}, the current I_1 is similar with I_2. Therefore, the output current of the I-square circuit is equal to the current of I_1+I_3.

$$I_{out} = I_1 + I_3 = I_2 + I_3 = \frac{1}{2}K(V_2 - 2V_t)^2 + \frac{I_{in}^2}{2K(V_2 - 2V_t)^2} \tag{27}$$

From the equation (27), some of the correlations would be obtained. The value of output current of current squaring circuit would be in reverse proportional to the value of V_2-$2V_t$. For the same reason, the conversion gain of current mode down-conversion mixer is in reverse proportional to the value of V_2-$2V_t$. Due to the fixed value of V_t, the conversion gain would be decided by the biasing voltage, V_2. However, the performance of linearity is proportional to the biasing voltage. Therefore, the performance of conversion gain and linearity are trade-off in the design consideration of I-square circuit. Fig. 29 presents the simulated results about conversion gain and linearity. From the simulated results, the optimal value of bias voltage V_2 is about 1V.

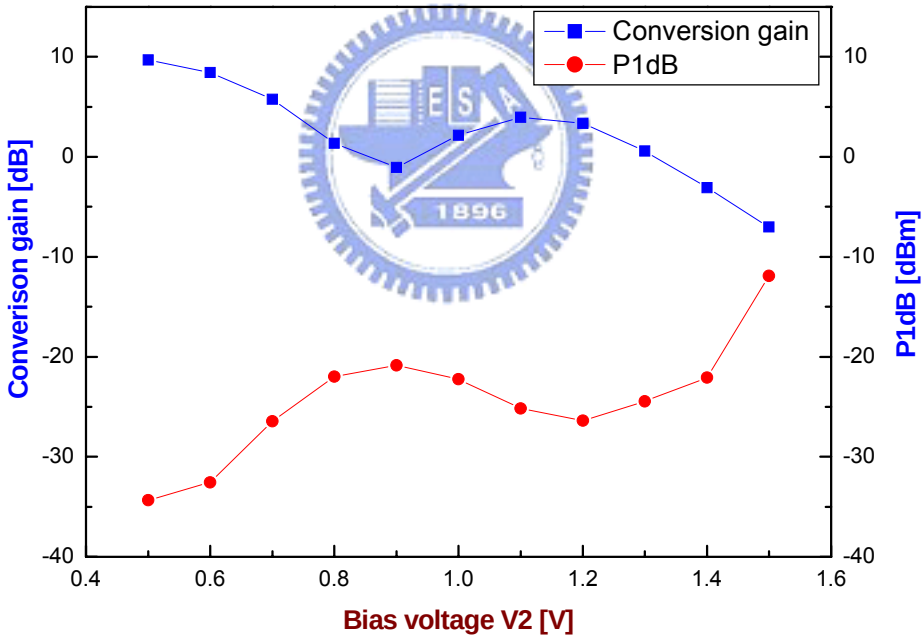


Fig. 29 Conversion gain and 1dB compression point of current-mode downconverter

Due to the short-channel effect of MOS device, the drain current I_D is shown as following.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^m(1+\lambda V_{DS}) \qquad (28)$$

The velocity saturation effect makes the drain current I_D proportional to $(V_{GS}-V_T)^m$ where $1 \le m < 2$. The drain current is correlated with V_{DS} in the short-channel MOS devices. For the different VDS voltage of VDS1 and VDS3, the function of current square circuit would be worsened. The equation of I_{out} is shown as (29) and all of the detailed analysis would be introduced in the appendix I.

$$I_{out} = \frac{I_{in}^2}{2K(V_2-2V_t)^2} * [1 + \frac{1}{(1+\frac{\lambda^2 V_{DD}^2}{4}+\lambda V_{DD})} * (\frac{\frac{\Delta\lambda}{2}+\frac{\Delta\lambda^2 V_{DD}}{4}}{1+\frac{\lambda^2 V_{DD}^2}{4}+\lambda V_{DD}} - \frac{\lambda^2 V_{DD}^2}{4} - \frac{\lambda V_{DD}}{4})]$$

$$+ [\frac{\frac{2\Delta\lambda}{K} + (V_2-2V_t)^2 * (\frac{1}{2}\lambda V_{DD} + \frac{\lambda^2 V_{DD}^2}{4} + \frac{-2\Delta\lambda - \Delta\lambda^2 V_{DD} + \frac{27}{4}\Delta\lambda^3 V_{DD}^2}{2+\frac{3}{2}\lambda V_{DD}})}{(1+\frac{\lambda^2 V_{DD}^2}{4}+\lambda V_{DD})}$$

$$- (V_2-2V_t)^2 * \frac{\frac{3\lambda V_{DD}}{2} + \frac{5\lambda^2 V_{DD}^2}{2} + \frac{11\lambda^3 V_{DD}^3}{8} + \frac{\lambda^4 V_{DD}^4}{4}}{(2+\frac{3}{2}\lambda V_{DD}) * (1+\frac{\lambda^2 V_{DD}^2}{4}+\lambda V_{DD})^2} * \Delta\lambda] * I_{in}$$

$$+ \frac{K(V_2 - 2V_t)^2 * (1+\lambda V_{DD}+2\Delta\lambda) * (2+\frac{3}{2}\lambda V_{DD})}{4(1+\frac{\lambda^2 V_{DD}^2}{4}+\lambda V_{DD}+\frac{3\Delta\lambda+\frac{7}{2}\Delta\lambda^2 V_{DD}+\Delta\lambda^3 V_{DD}^2}{2+\frac{3}{2}\lambda V_{DD}})} \qquad (29)$$

$$\Rightarrow I_{out} \propto \frac{I_{in}^2}{2K(V_2-2V_t)^2} * \{1 - \frac{1}{(1+\frac{\lambda^2 V_{DD}^2}{4}+\lambda V_{DD})} * [(1+\lambda V_{DD}) * \frac{\lambda V_{DD}}{4}] - (\frac{\frac{\Delta\lambda}{2}+\frac{\Delta\lambda^2 V_{DD}}{4}}{1+\frac{\lambda^2 V_{DD}^2}{4}+\lambda V_{DD}})\}$$

$$= \frac{I_{in}^2}{2K(V_2-2V_t)^2}(1-\delta)$$

$$where \quad \delta = \frac{1}{(1+\frac{\lambda^2 V_{DD}^2}{4}+\lambda V_{DD})} * [(1+\lambda V_{DD}) * \frac{\lambda V_{DD}}{4}] - (\frac{\frac{\Delta\lambda}{2}+\frac{\Delta\lambda^2 V_{DD}}{4}}{1+\frac{\lambda^2 V_{DD}^2}{4}+\lambda V_{DD}}) \qquad (30)$$

Thus, the smaller difference between V_{DS1} and V_{DS3} is the better for the current square operation. The following figure represents the impact of difference V_{DS} voltage. The smaller difference of V_{DS} voltage will have the greater conversion gain of current-mode mixer. Therefore, there are two important issues about the current square circuit. First, the channel length of MOS devices in the current square circuit should be chosen as larger channel length to alleviate the short channel effect. Second, the biasing voltage of current square circuit should be chosen with the smallest difference of V_{DS} between M1 and M3 MOS devices. While the V_2 is equal to V_{DD}, the voltage of V_{DS1} is very close to V_{DS3}.

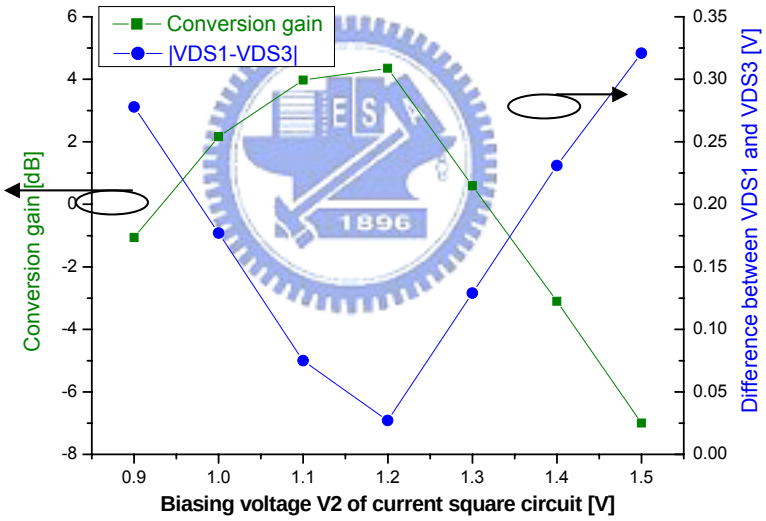


Fig. 30 The impact of difference of V_{DS} voltage

The drain current I_D of MOS devices may not a quadratic equation of V_{GS}. Fig. 31 compares the difference of drain current between the modified quadratic equation of V_{GS}-V_t and model definition. Below the bias voltage of 0.8V, the differences are very slight. The operated voltage of MOS device in the current squaring circuit is below 0.8V. Therefore, the drain current equation is closed to the quadratic equation of V_{GS}.

The functionality of current squaring is acceptable.

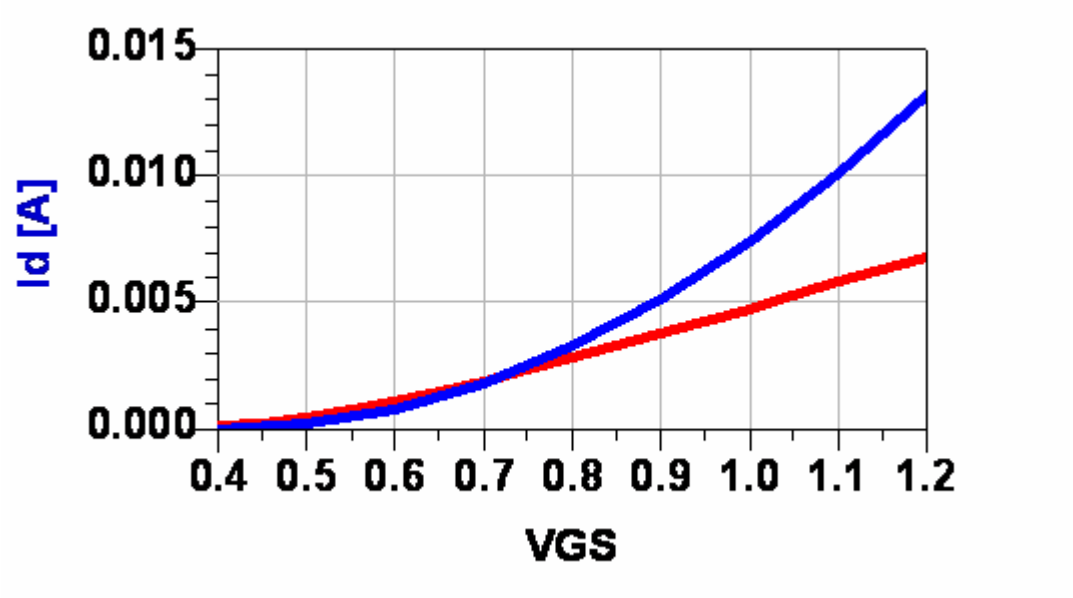


Fig. 31 The difference of drain current of between the modified quadratic equation of V_{GS}-V_t and model definition.

While the input current of I-square circuit is the summing current between I_{LO} and I_{RF}, the output current of I-square circuit could obtain the mixing frequency between ω_{RF} and ω_{LO}. Therefore, the operation of down-conversion mixing can be accomplished. The Fig. 32 shows the complete whole circuit implement.

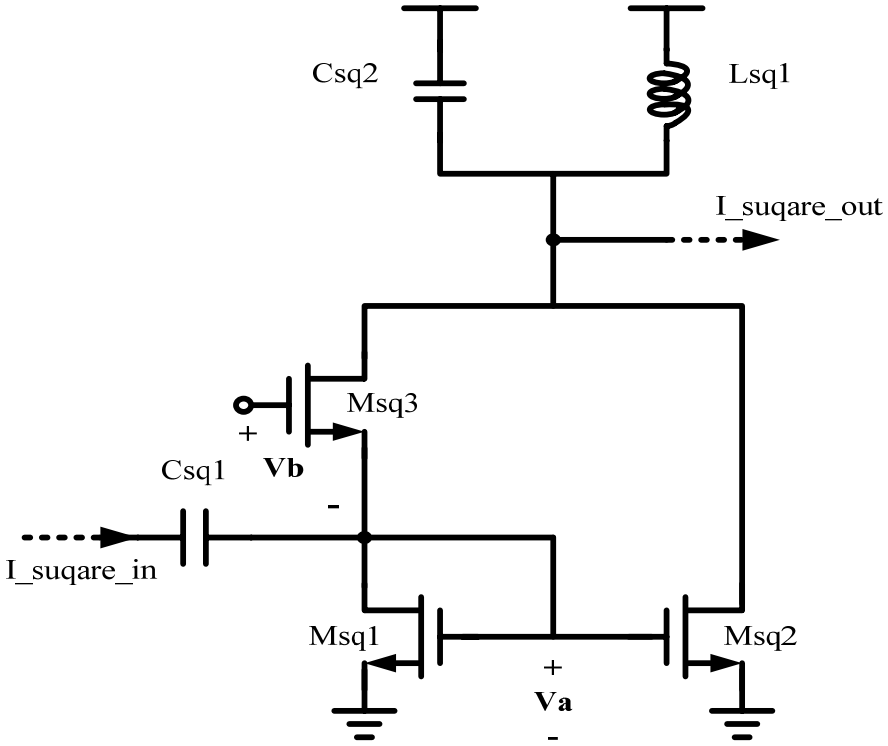


Fig. 32 The complete whole circuit of I-square circuit.

The capacitance of C_{sq1} is the block capacitance between I-sum and I-square circuit. The inductor of L_{sq1} resonates with the capacitance of C_{sq2} at the intermediate frequency of 5-GHz and provide high impedances at output terminal of I-square circuit. Therefore, the L_{sq1} and C_{sq2} could be used as the filter to percolate the leakage signal of LO frequency (19-GHz), RF frequency (24-GHz), up-conversion frequency (19-GHz+24-GHz), the double frequency of RF and LO frequency (48-GHz and 38-GHz) and third frequency of RF and LO frequency (72-GHz and 57-GHz).

2.2.2 Circuit Implementation

The complete schematic of current-mode mixer is shown in Fig. 33 and Table(ii) lists the detailed parameters of each device. The current-mode mixer is composed of three blocks, the I-sum circuit, I-square circuit and output current buffer. First, the I-sum circuit consists of transistors, M_{s1} and $M_{s2,}$ and the inductors, L_{s1}, L_{s2} and L_{s3}.

The transistors of M_{s1} and M_{s2} are the common-gate topology connected the drain terminal together. The inductor of L_{s1} and L_{s2} resonate with the total parasitic capacitance seen at source node of M_{s1} and M_{s2}, respectively. Thus, the LC resonance would provide the high impedance to feed the RF and LO current signal into the common-gate transistor connected the drain terminal together. Then, the inductor L_{s3} resonates with the total parasitic capacitance seen at the output node of current summing circuit. Thus, the resonation of L_{s3} would provide high impedance to feed the output current of summing circuit into the current squaring circuit. Second, the I-square circuit is composed of transistor of M_{sq1}, M_{sq2} and M_{sq3}, capacitance of C_{sq1} and C_{sq2}, and the inductor of L_{sq1}. The transistor of M_{sq1}, M_{sq2} and M_{sq3} would perform the operation of current squaring. The inductor resonates with Csq2 at intermediate frequency of 5-GHz. The resonation between L_{sq1} and C_{sq2} would provide high impedance to feed the output current of current squaring into output current buffer. Finally, the output current buffer provided the performance of 0-dB consists of the transistor of M_{b1}, M_{b2} and inductor, L_{b1}. Table(ii) lists the detailed parameters of current-mode downconverter.

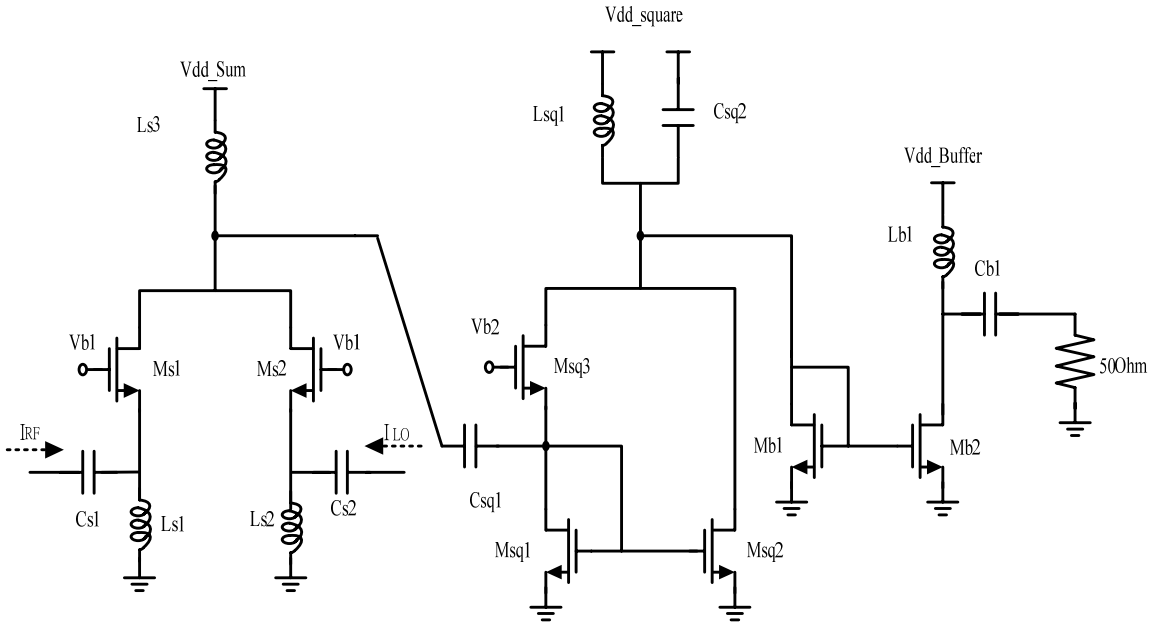


Fig. 33 The complete circuit of the current-mode circuit.

Table(ii) Detailed parameters of current-mod downconverter.

$M_{s1,2}$	RF_MOS	1.2um*32 / 0.13um
$M_{sq1,2,3}$	RF_MOS	1.2um*12 / 0.13um
M_{b1}	RF_MOS	1.2um*1 / 0.13um
M_{b2}	RF_MOS	5.0um*30 / 0.13um
C_{s1}	Mmcap_um	7.5um*7.5um (62.996 fF)
C_{s2}	Mmcap_um	16um*16um (273.95 fF)
C_{sq1}	Mmcap_um	11um*11um (131.881 fF)
C_{sq2}	Mmcap_um	31um*31um (1.0 pF)
C_{b1}	Mmcap_um	23.5um*23.5um (583.4 fF)
L_{s1}	Spiral_std	rad= 20um w=3 nr=3.25 (945.25 pH)
L_{s2}	Spiral_std	rad= 26um w=3 nr=2.75 (916.56 pH)
L_{s3}	Spiral_std	rad= 27.0um w=3 nr=1.5 (443.21 pH)
L_{sq1}	Spiral_std	rad= 15.5um w=3 nr=3.5 (884.52 pH)
L_{b1}	Spiral_std	rad= 20.0um w=3 nr=4.5 (1.693 nH)

2.3 Simulation Results

The post-simulation is completed by ADS simulator for whole simulation with process parameters of TSMC 0.13-um CMOS MS/RF general purpose 1P8M salicide Cu-FSG 1.2V/2.5V RF SPICE models. The following diagrams are the post-simulation results of thorough receiver circuits.

■ LNA

Because the first stage of receiver is LNA, it must provide input matching, power gain and low-noise contribution in a specific frequency band. The figures from Fig. 34 to Fig. 37 are the port-simulation results of S-parameters, S11, S22, S21 and S12, respectively. The input and output matching are lower than -10dB indicated a power transfer greater than 90%. Fig. 38 exhibits that the noise figure is lower 3.5dB at the frequency of 24-GHz. The resultant noise figure is close to the minimum noise figure. The simulation results of linearity are shown in Fig. 39, Fig. 40 and Fig. 41. The linearity performance of input 1-dB compression (P_{1dB}) is about -21.3dBm. The input third-intercept point (IIP3) is about -11.7dBm. The transient simulation results of input and output current amplitude are shown in Fig. 42. The stability simulation results of stability factor and stability measure are shown in Fig. 43 and Fig. 44. The necessary and sufficient conditions for unconditional stability are that the stability factor is greater then unit and the stability measure are positive. The Table(iii) is the comparison with previously reported LNA for frequencies around 20-GHz. The conversion gain of current-mode LNA is dominant with the device size ratio of current-mirror amplifier. Thus, the supply voltage has slight effect on the conversion gain. But the supply voltage would have great effects on the power consumption.

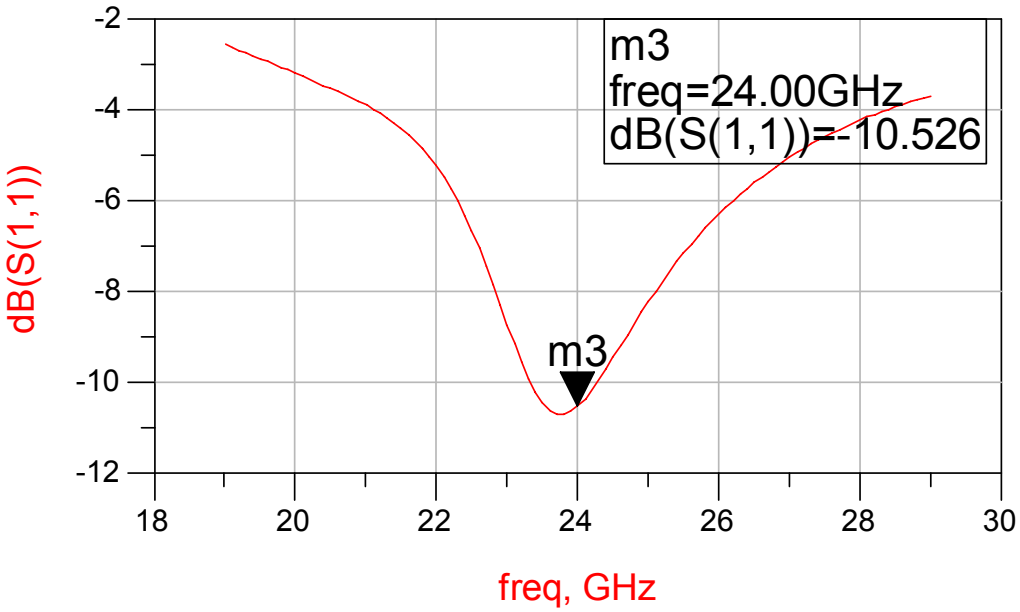


Fig. 34 Simulation result S11 of LNA.

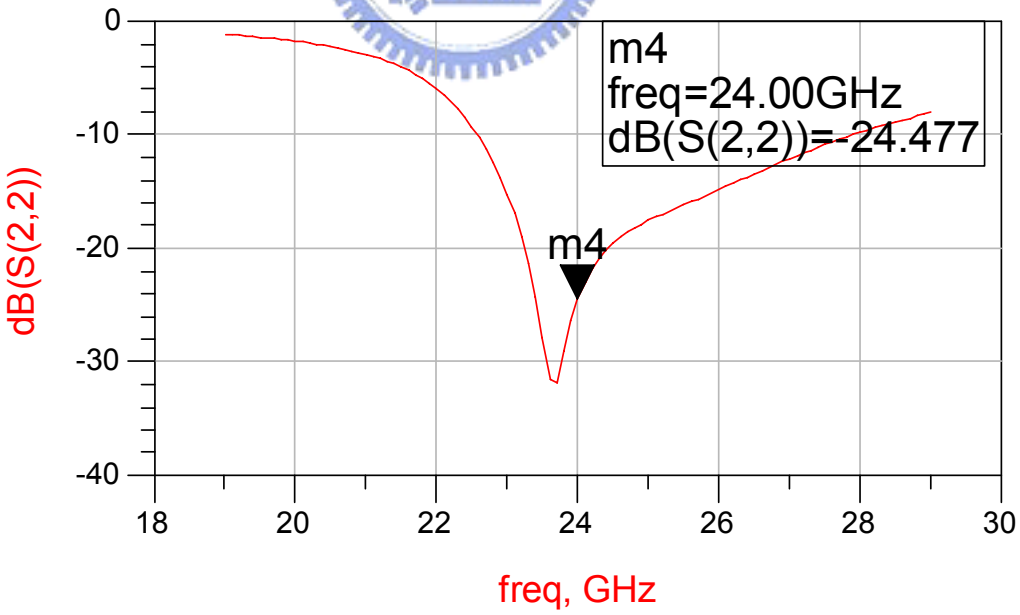


Fig. 35 Simulation result S22 of LNA.

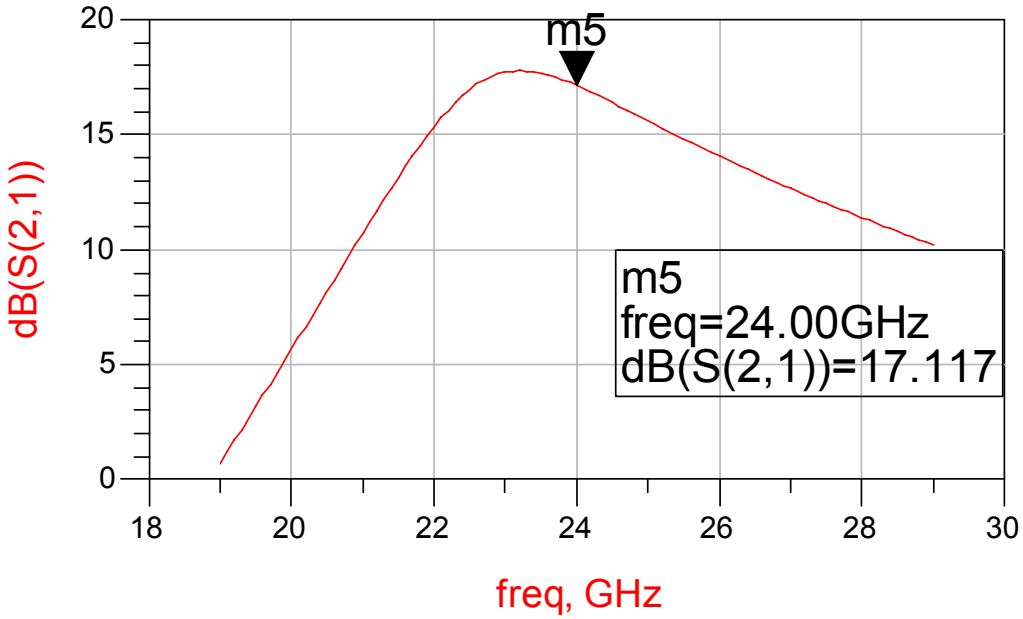


Fig. 36 Simulation result S21 of LNA.

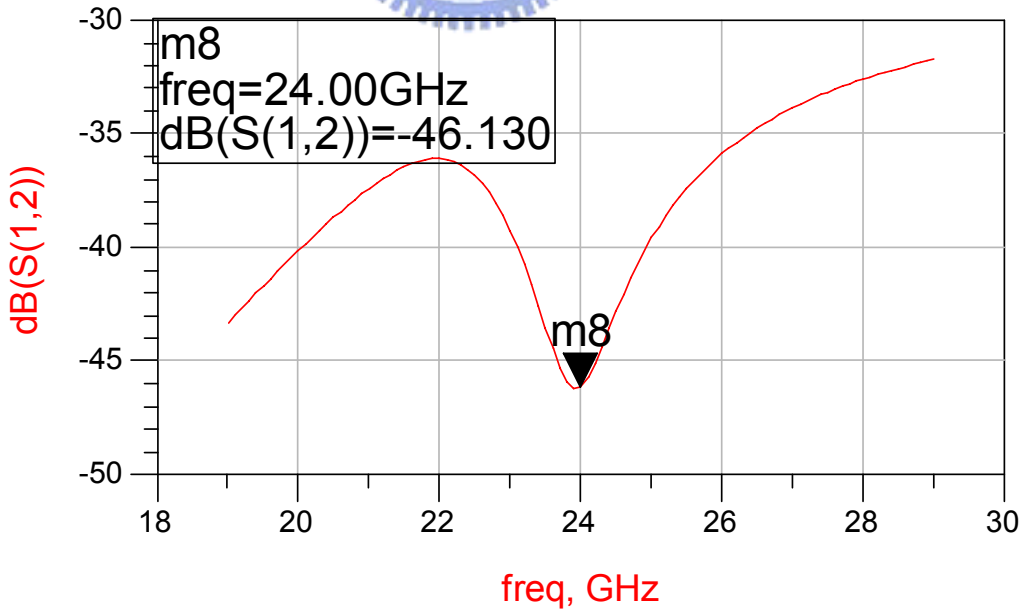


Fig. 37 Simulation result S12 of LNA.

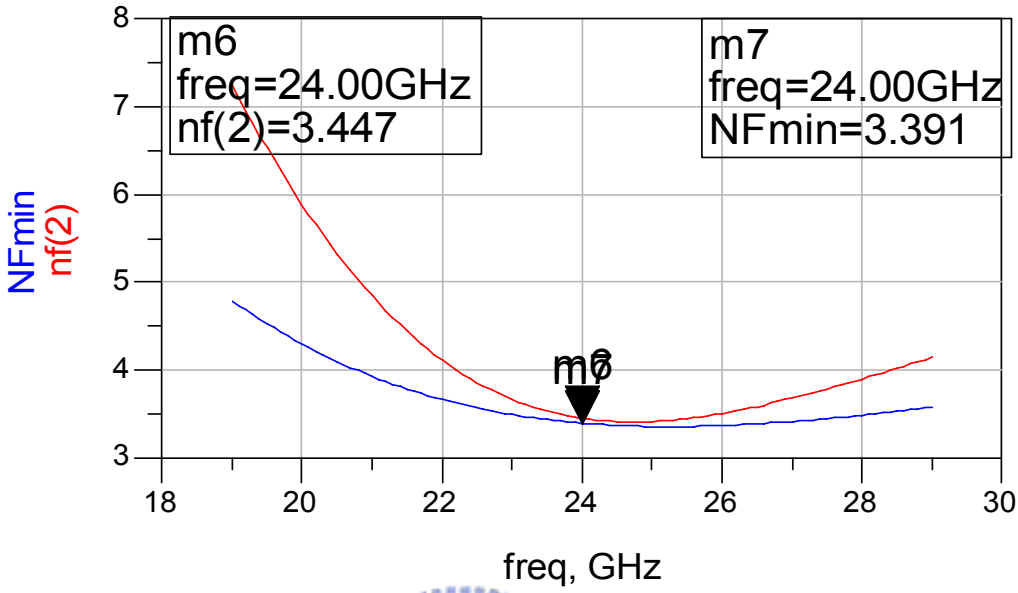


Fig. 38 Simulation result NF_{min} of LNA.

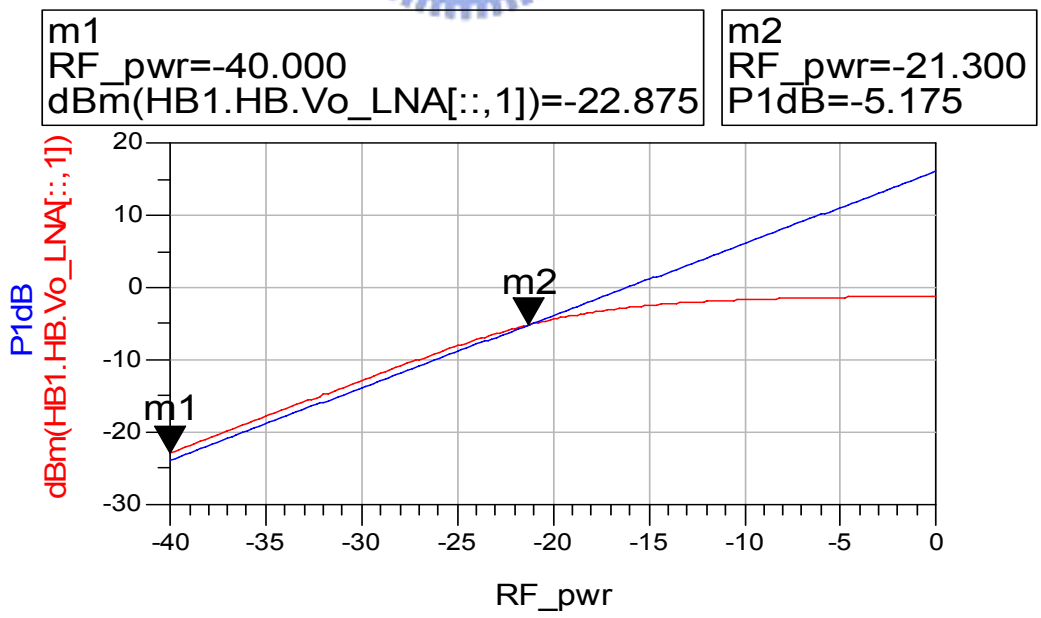


Fig. 39 Linearity simulation result P_{1dB} of LNA.

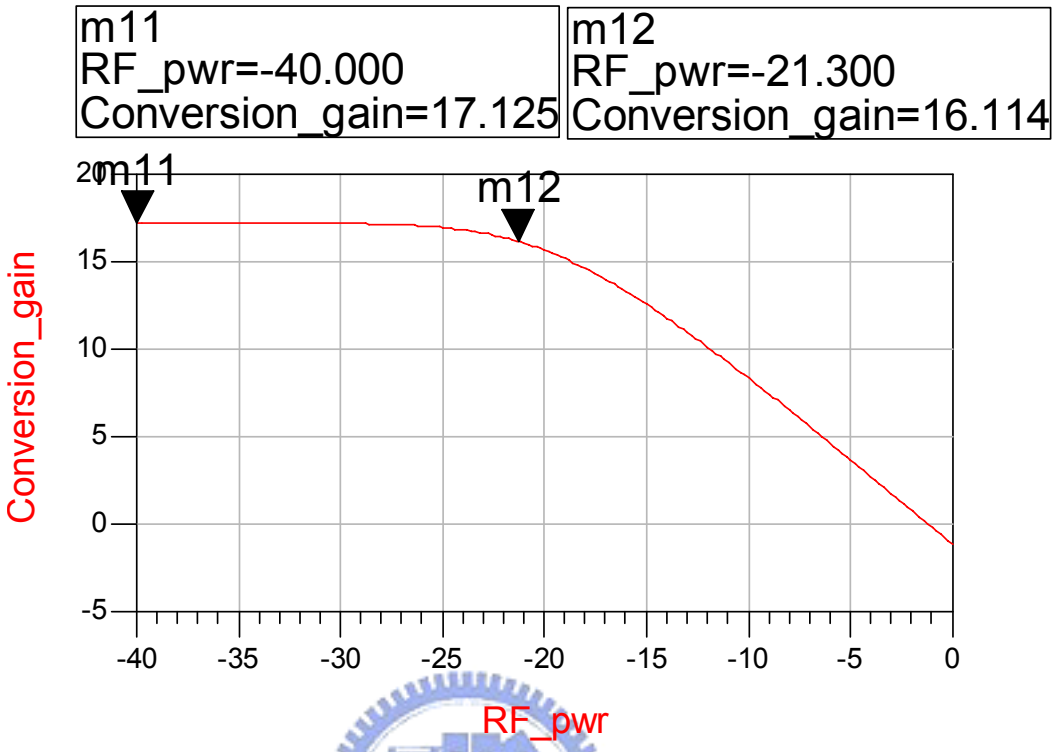


Fig. 40 Simulation result of conversion gain of LNA.

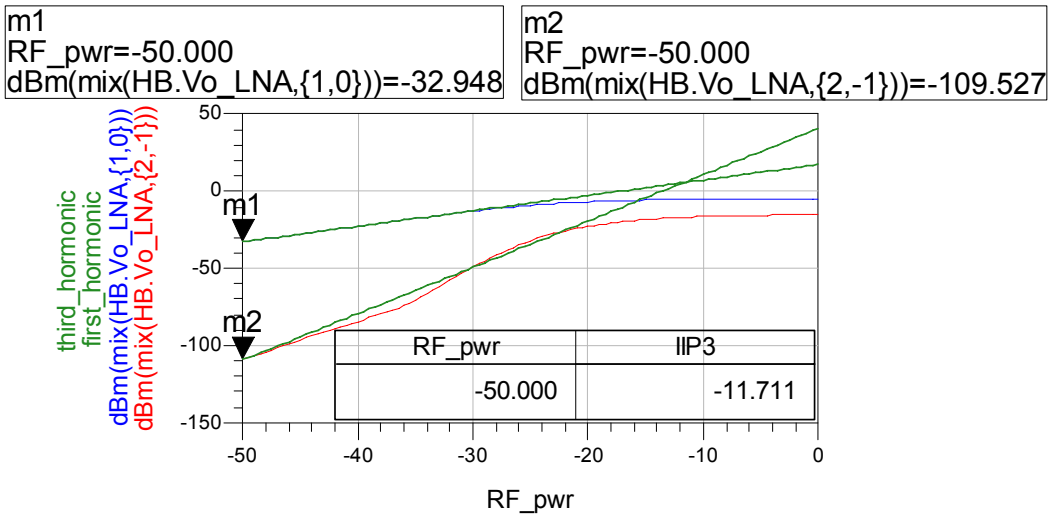


Fig. 41 Simulation result IIP3 of LNA.

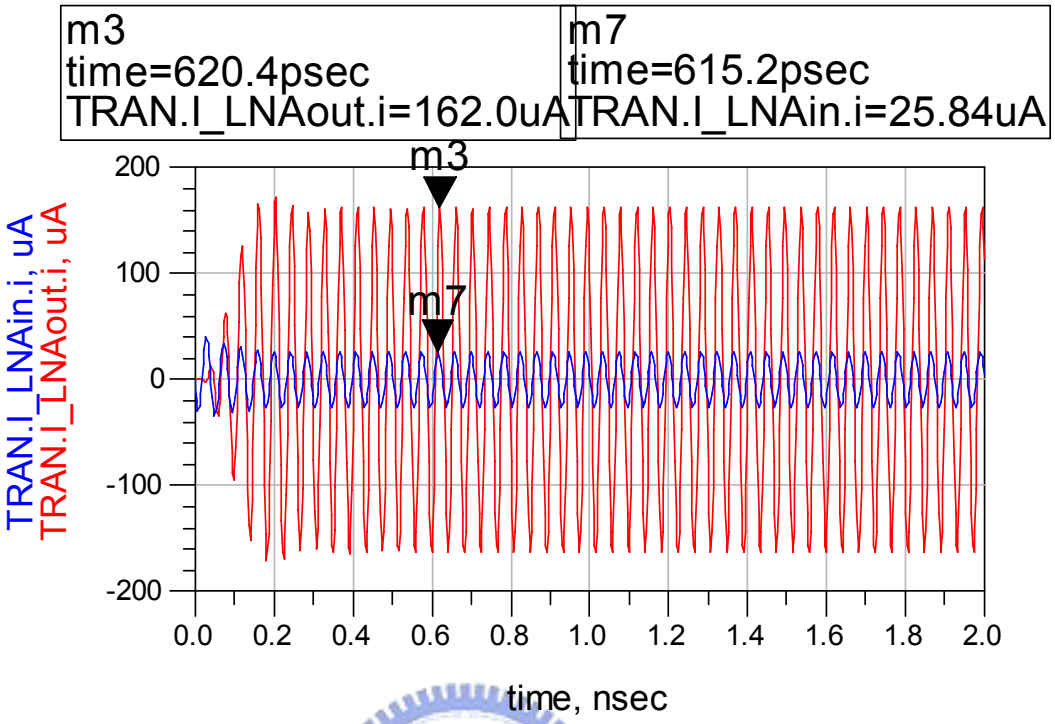


Fig. 42 Transient simulation result of LNA.

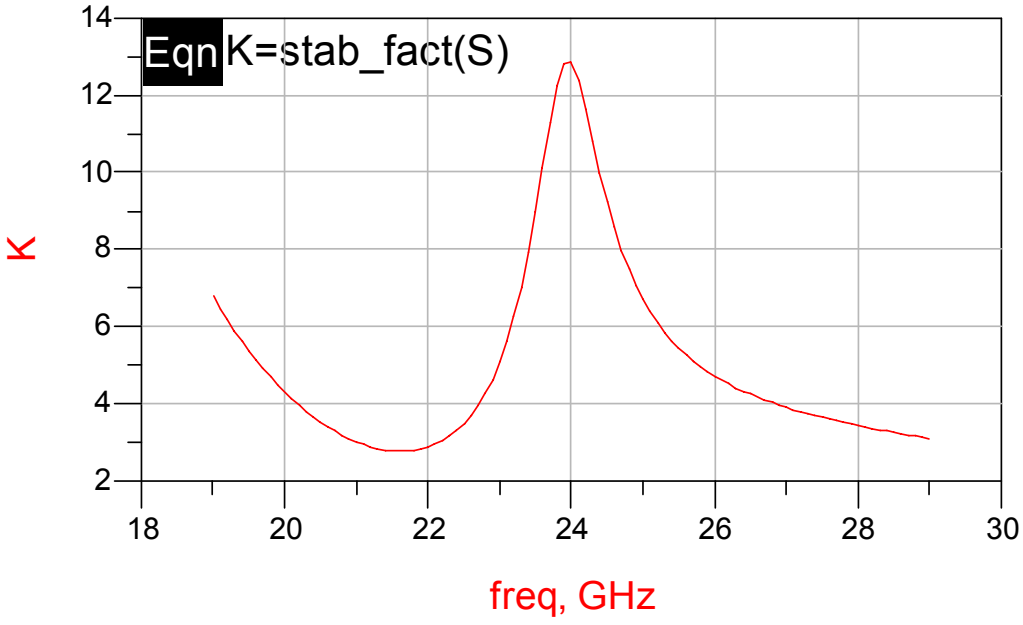


Fig. 43　Simulation result K-factor of LNA.

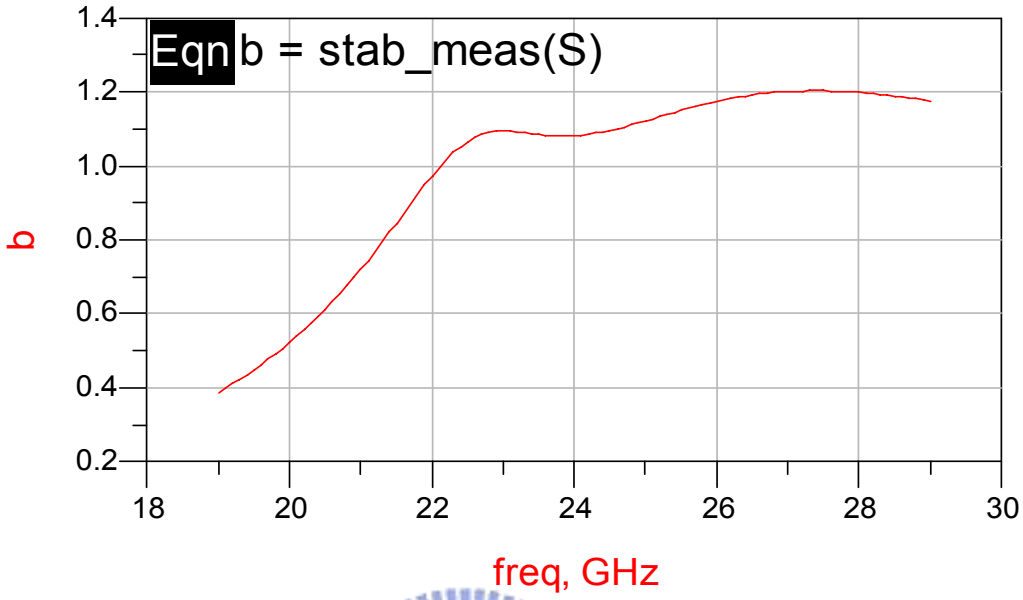


Fig. 44　Simulation result stability measure of LNA.

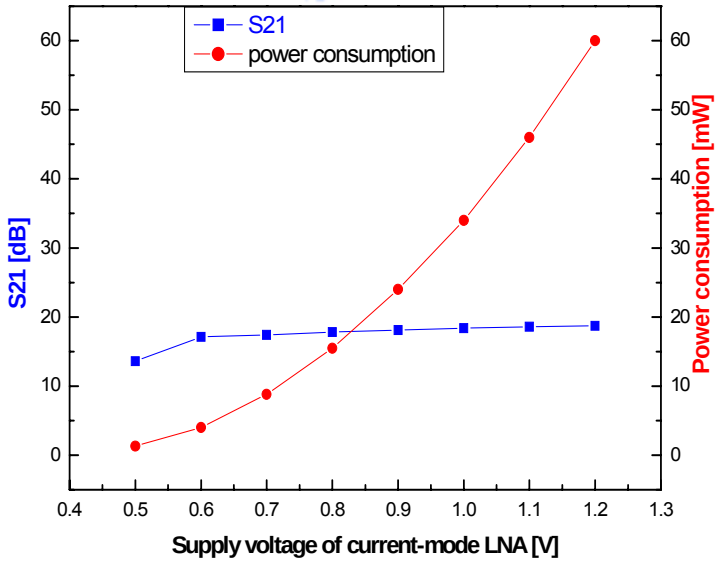
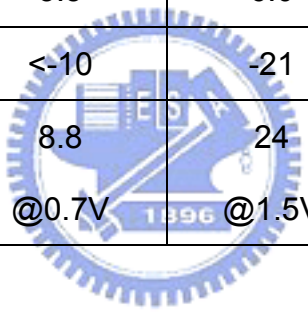


Fig. 45　The S21 and power consumption of LNA in the different supply voltage.

Table(iii) The comparison with previously reported LNA for frequencies around 20-GHz.

Reference	This work	This work	[8]	[21]	[7]	[22]
Freq. [GHz]	24	24	21.8	20	23.7	24
Technology	0.13um	0.13um	0.18um	0.13um	0.18um	0.18um
Topology	2 stage Current-mode	2 stage Current-mode	3 stage CGRF+CS+CS	2 stage CS+CS	3 stage CS+CS+CS	2 stage CS+CS
Gain [dB]	17.1	17.5	15	12.9	12.86	13.1
P_{1dB} [dBm]	-21.3	-19.7	--	--	--	--
IIP3 [dBm]	-11.7	-10.8	--	--	--	--
NF [dB]	3.4	3.5	6.0	4.4	5.6	3.9
S11 [dB]	<-10	<-10	-21	-14	-11	-15
Total power [mW]	10.6 @1.2V	8.8 @0.7V	24 @1.5V	16.8 @1.2V	54 @1.8V	14 @1V



■ overall

The Fig. 46, Fig. 47 and Fig. 48 plot the S-parameter simulation results at RF, LO and output port in the whole receiver, respectively. The harmonic simulation is shown in Fig. 49. The input spectrum at RF (24-GHz) and LO port (19-GHz) are about -49dBm and -3dBm, respectively. The output spectrum of receiver at 5-GHz is about -27.898dBm. Thus, the conversion gain of overall receiver at 24-GHz is about 20.913dB. From the Fig. 49(c), some of sub-harmonic the isolation performance can be found. The spectrum at LO frequency (19-GHz), RF frequency (24-GHz), up-conversion frequency (19-GHz+24-GHz), the double frequency of RF and LO frequency (48-GHz and 38-GHz) and third frequency of RF and LO frequency

(72-GHz and 57-GHz) can be suppressed with resonating at 5-GHz between L_{sq1} and C_{sq2}. The conversion gain and noise figure versus frequency of overall receiver path are shown in Fig. 50 and Fig. 51. The frequency range of K-band applications is from 18GHz to 26.5GHz. The frequency bandwidth of ISM band is about 1GHz. The 3-dB bandwidth of current-mode receiver is about 1.75 GHz (21.5GHz~23.25 GHz) and conversion gain of current-mode receiver is about 26.4 dB at the peak frequency of 22.5GHz. The 3-dB bandwidth is dominant with the Q value of inductor. For the higher conversion gain, the higher Q of the inductor will be used. Therefore, the wider 3dB bandwidth and higher conversion gain are trade-off. Finally, the diagram of Fig. 52 and Fig. 53 present the simulation results of linearity performance. The summary table of post-simulation with corner variations presents as Table(iv). The Table(v) is a summary table of post-simulation with temperature variation.

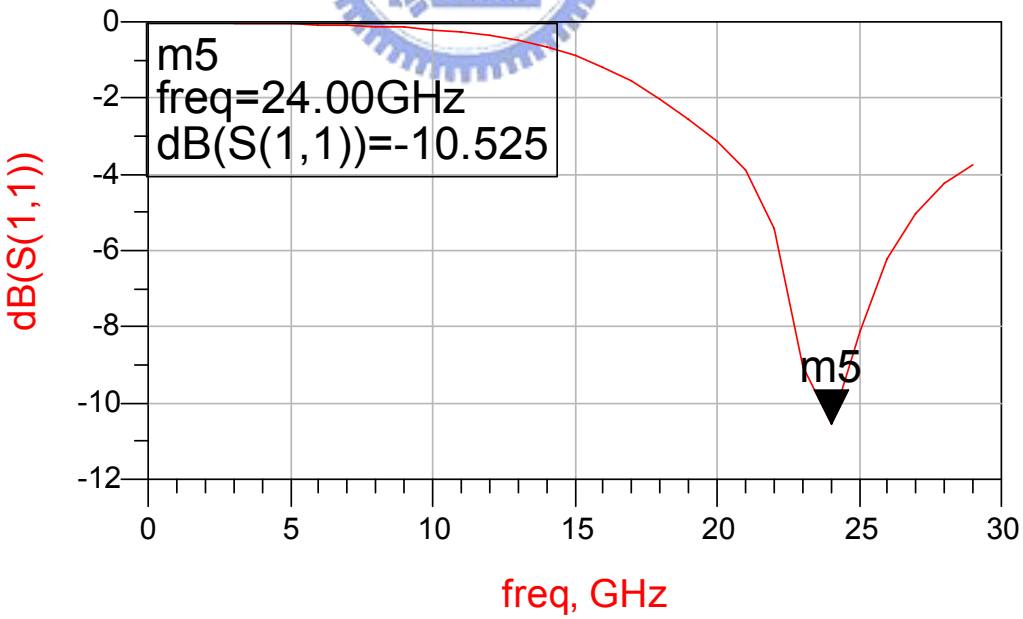


Fig. 46 S-parameter simulation result at RF input of the overall receiver.

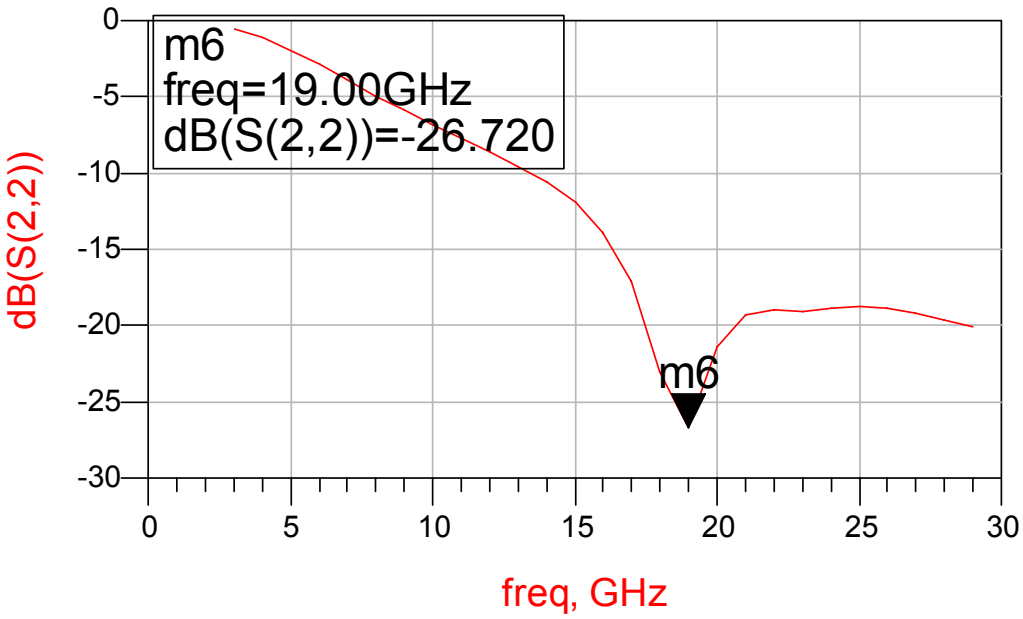


Fig. 47 S-parameter simulation result at LO port of the overall receiver.

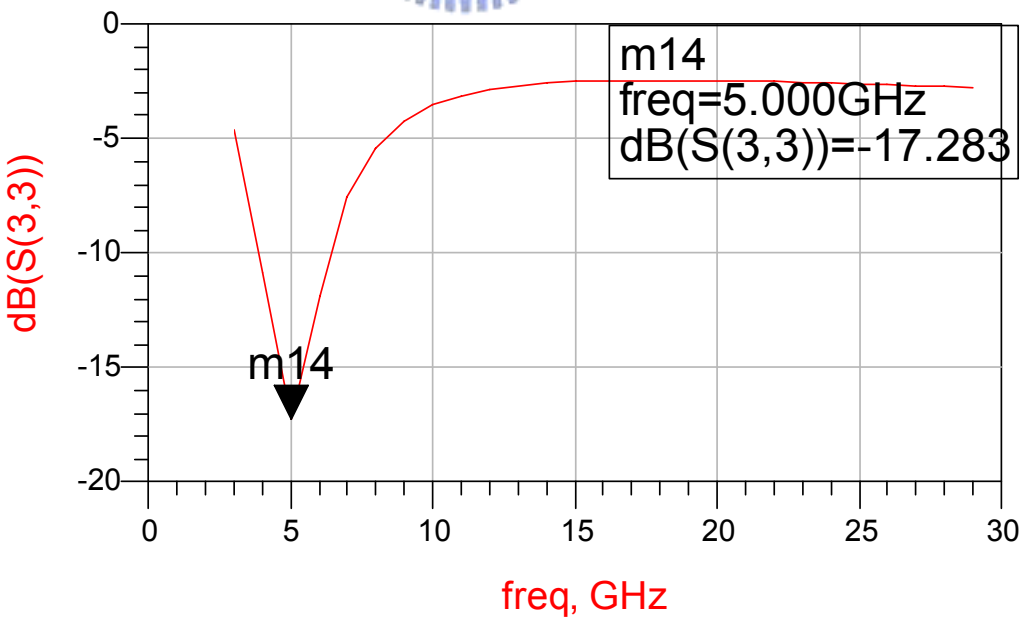
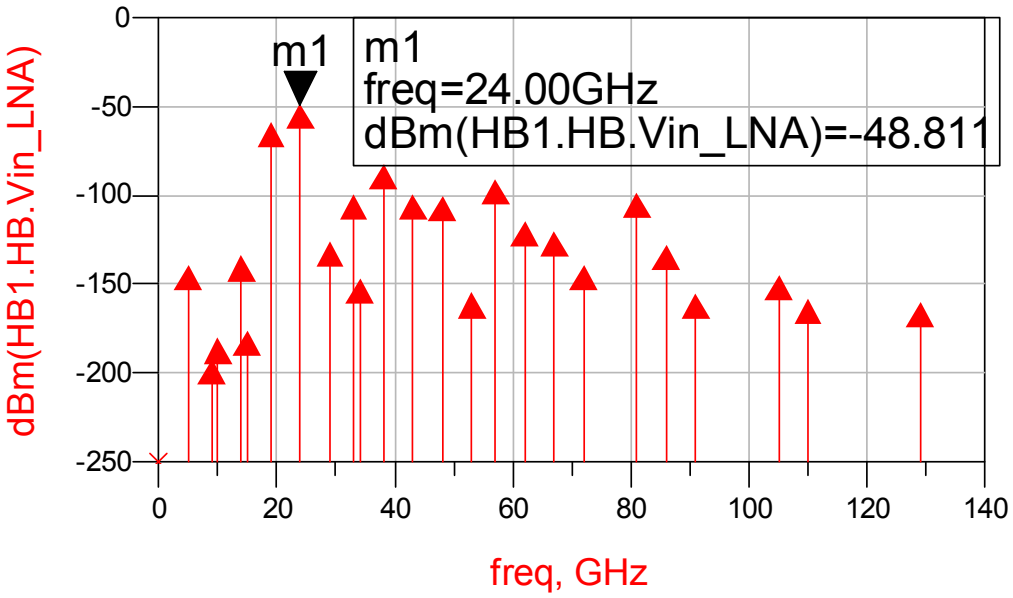
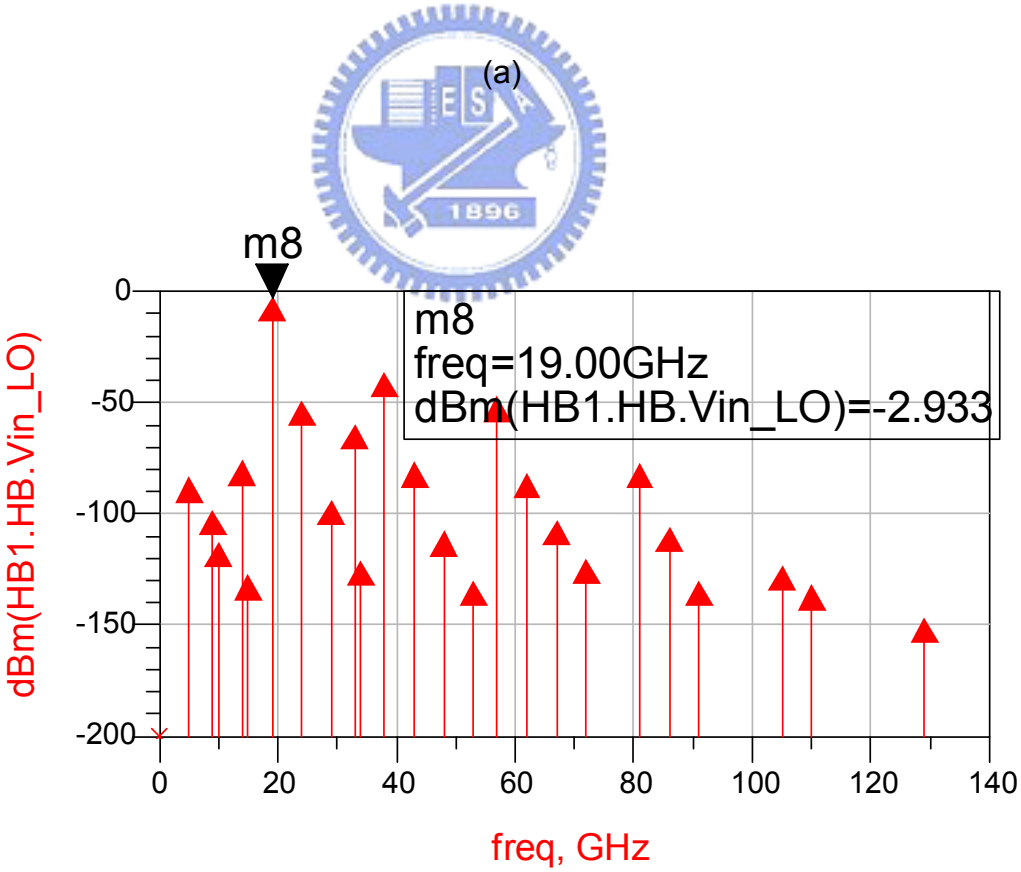


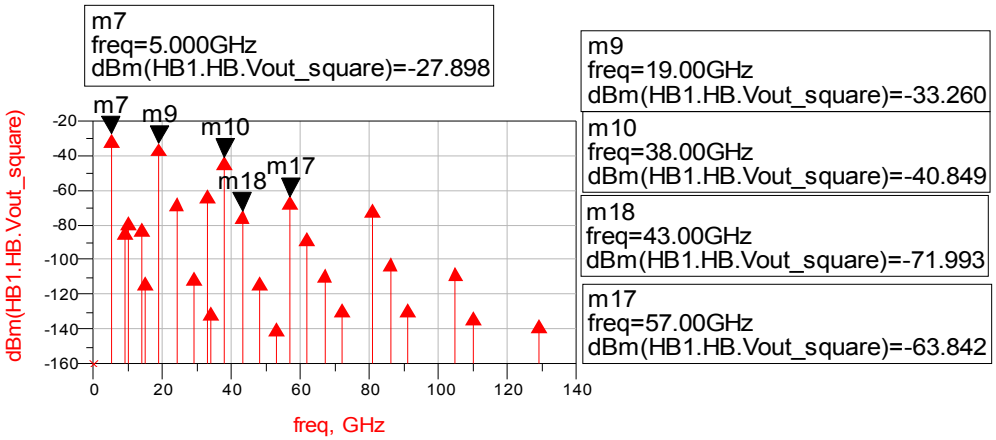
Fig. 48 S-parameter simulation result at output of the overall receiver.


m1
m1
freq=24.00GHz
dBm(HB1.HB.Vin_LNA)=-48.811
dBm(HB1.HB.Vin_LNA)
freq, GHz
0
-50
-100
-150
-200
-250
0
20
40
60
80
100
120
140

(a)


m8
m8
freq=19.00GHz
dBm(HB1.HB.Vin_LO)=-2.933
dBm(HB1.HB.Vin_LO)
freq, GHz
0
-50
-100
-150
-200
0
20
40
60
80
100
120
140

(b)



(c)

Fig. 49 The harmonic simulation results of the receiver. (a) The spectrum diagram at RF input port. (b) The spectrum diagram at LO port. (c) The spectrum diagram at output port.

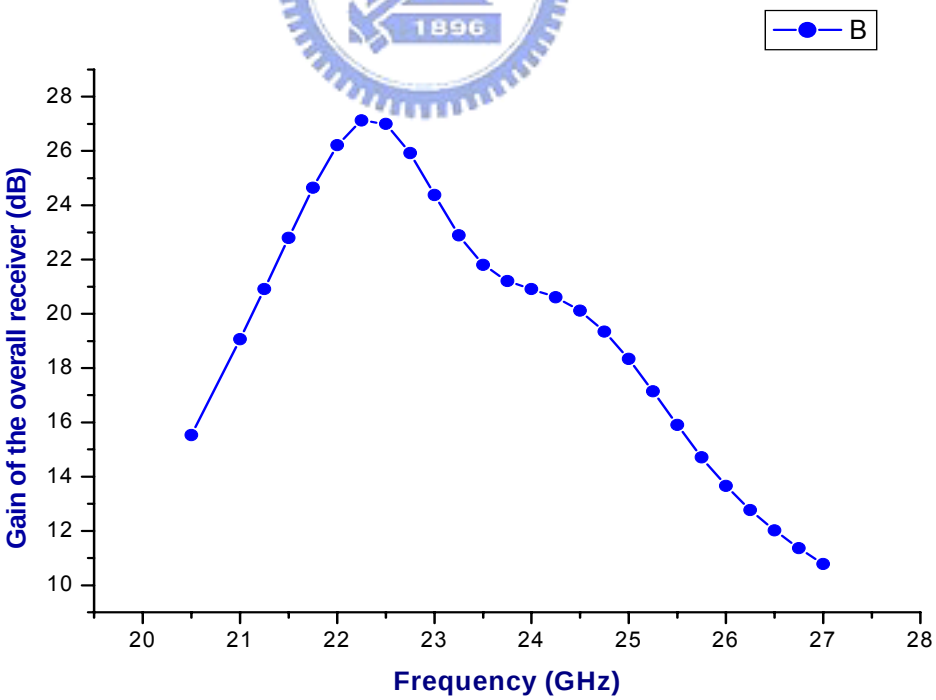


Fig. 50 The conversion gain of the overall receiver.

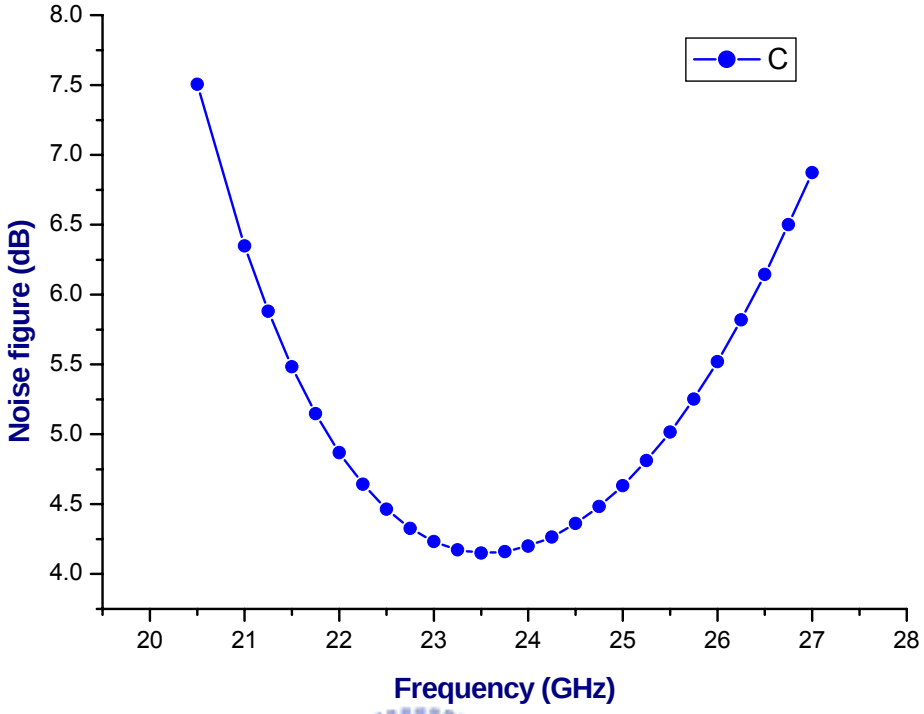


Fig. 51 The noise figure of the overall receiver.

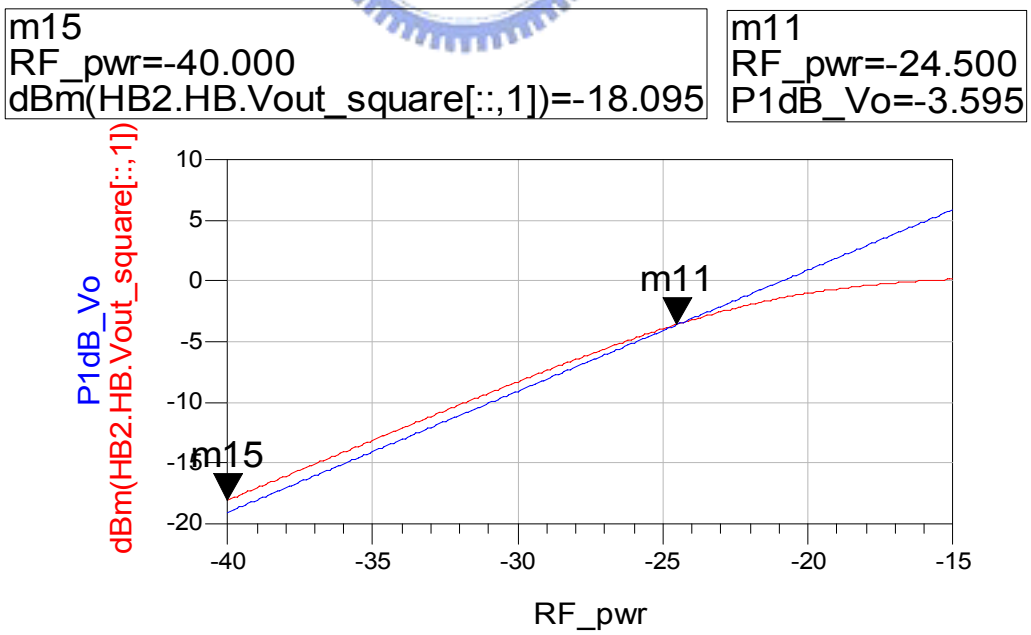


Fig. 52 The simulation result P1dB of the overall receiver.

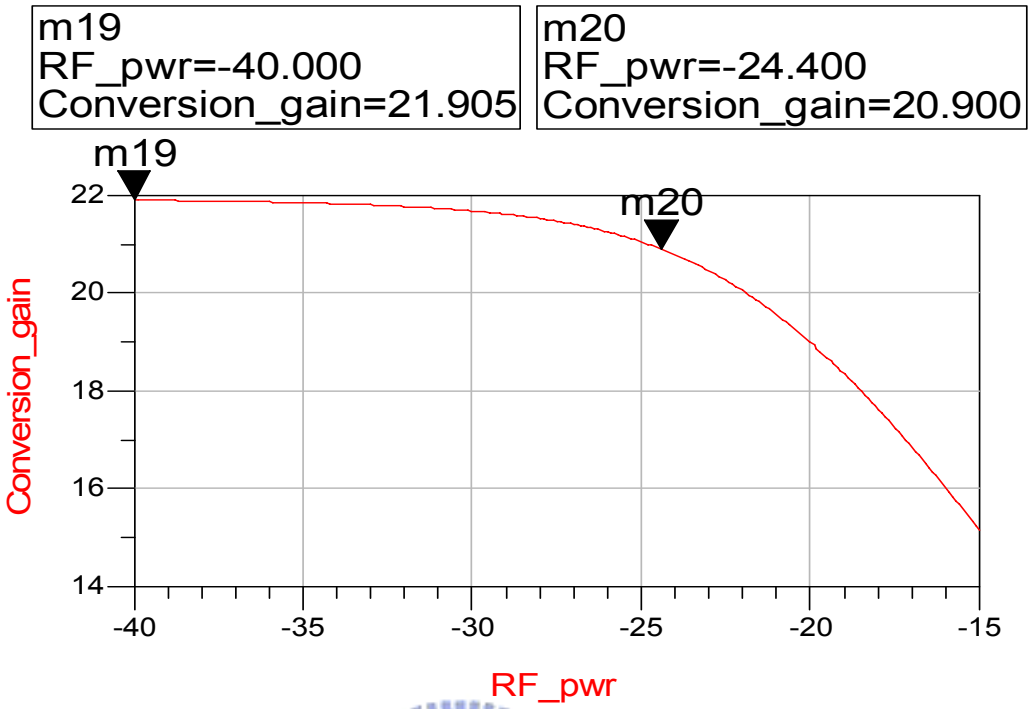


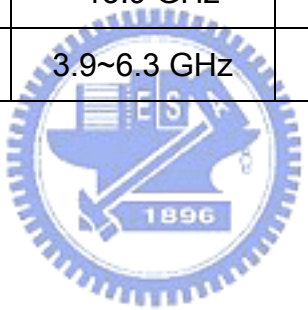
Fig. 53 The linearity simulation result of overall receiver.

Table(iv) The corner of the post-simulation summary.

	FF	TT	SS
$Gain_{LNA}$ [dB]	18.5	17.1	13.9
NF_{LNA} [dB]	3.5	3.4	3.6
$Gain_{RX}$ [dB]	24.7	20.9	14.5
NF_{RX} [dB]	4.1	4.2	5.2
P_{1dB} [dBm]	-26.2	-24.4	-25.7
Power dissipation [mW]	37.4	24.3	14.7
S_{11} (<10 dB)	23.5~25.5 GHz	23.2~24.3 GHz	22.9~23.6 GHz
S_{22} (<10 dB)	>14.8 GHz	>13.5 GHz	>10.1 GHz
S_{33} (<10 dB)	4.2~7.0 GHz	4.0~6.3 GHz	3.5~5.9 GHz

Table(v) Post-simulation summary with temperature variation.

Temperature	0	25	100
$Gain_{LNA}$ [dB]	16.7	17.1	17.4
NF_{LNA} [dB]	3.2	3.4	4.0
$Gain_{RX}$ [dB]	21.7	20.9	18.0
NF_{RX} [dB]	4.0	4.2	4.9
P_{1dB} [dBm]	-23.8	-24.4	-26.9
Power dissipation [mW]	23.6	24.3	26.2
S_{11} (<10 dB)	23.2~24.1 GHz	23.2~24.3 GHz	23.2~24.8 GHz
S_{22} (<10 dB)	>13.9 GHz	>13.5 GHz	>12.5 GHz
S_{33} (<10 dB)	3.9~6.3 GHz	4.0~6.3 GHz	3.8~6.4 GHz



CHAPTER 3 EXPERIMENTAL RESULTS

A current-mode receiver front-end is designed and fabricated in TSMC 0.13-um 1P8M CMOS technology. The descriptions and considerations of chip layout are presented in first section. The measurement setup and considerations are discussed in second section. The measurement performance summaries are taken into discussions and comparisons in the last section.

3.1 Layout Description

For any high frequency design, the layout plays a very important role in the circuit performance. Thus, the fundamental issues of layout should take care.

The input signals of the receiver are taken in the topmost metal available in the technology. And the input lines from the pad are kept short to minimize the parasitic capacitance resulting from the layout traces [20]. Because the LNA noise figure is sensitive to the deviation in the input impedance, hence, if the layout traces contribute much parasitic capacitance, the noise figure of LNA would degrade. Since, the signal paths are as short as possible in the metal route to alleviate transmission line effect. All of the NMOS devices are arranged with deep n-well technique. The technique allows the source and bulk node to connect together to avoid the body effect. Dummy gates and dummy resistors are equipped at the margins of every MOS devices and resistor, respectively, to cope with process variation. The each sub-circuit is surrounded with guard rings for stable electric potential on substrate. Every spiral inductor keeps proper distances with the others and the core circuit to minimum any coupling effect, mutual inductance and disturbance on circuit working. The high frequency interconnect lengths should be kept as small as possible to reduce resistance, capacitance and inductance. Sometimes, shielding of the layout traces

becomes very important. If the metal line connecting the gate goes underneath the metal line connecting the drain, it gives rise to additional Miller capacitance, which might degrade the high frequency performance. Hence, another metal layer could be used as shielding for the two traces. Large DC blocking capacitors are provided between the power supply and ground to minimize noise perturbation from the supply voltages as well as to prevent any kind of ringing effect from DC supplies. The Fig. 54 shows the layout of receiver front-end, covering an area of 1.45*0.72 mm^2.

From the layout photo, there are many the long distance interconnection metal lines between the inductor devices. In RF/analog circuit design, the parasitic effects on the metal lines are critical issues. The parasitic of interconnections affect seriously the performance of circuits. Therefore, the parasitic effects of interconnection metal lines should be taken completely into considerations during post-simulation. The ADS momentum is used to modify the parasitic effects of interconnection metal lines in the post-simulation.

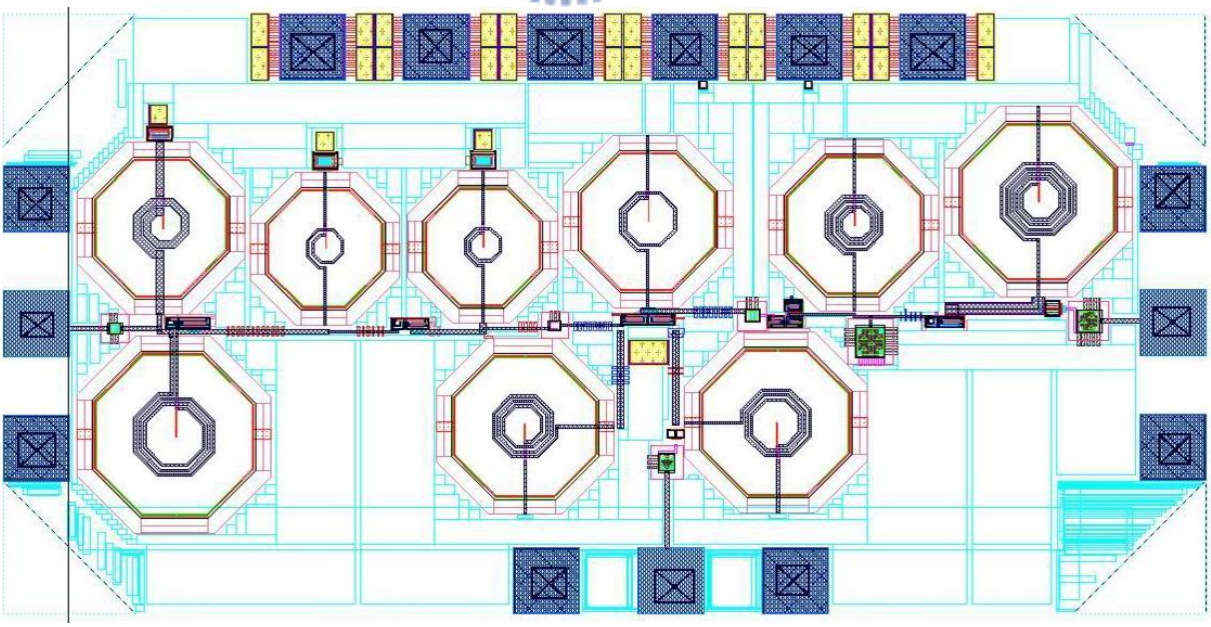


Fig. 54 Layout configuration of the receiver.

3.2 Measurement Considerations and Setup

The fabricated ICs are characterized using the on-wafer characterization technique. Two types of testing methods have been used for measurements: (1) probe cards and (2) wedge probes. Probe cards are custom made with a number of power supply signals and RF ports. But, the probe cards need to consider the effect of bond wire inductors and custom made and the pad frame must be laid out accordingly. Wedge probe offers flexibility in terms of their positioning and four probes have been used for testing the integrated receiver [20]. Due to the flexibility and the effect of bond wire inductors, the testing method of wedge probe is adopted for high frequency measurement. The chip microphotograph and measurement setup are shown in Fig. 55 and Fig. 56.

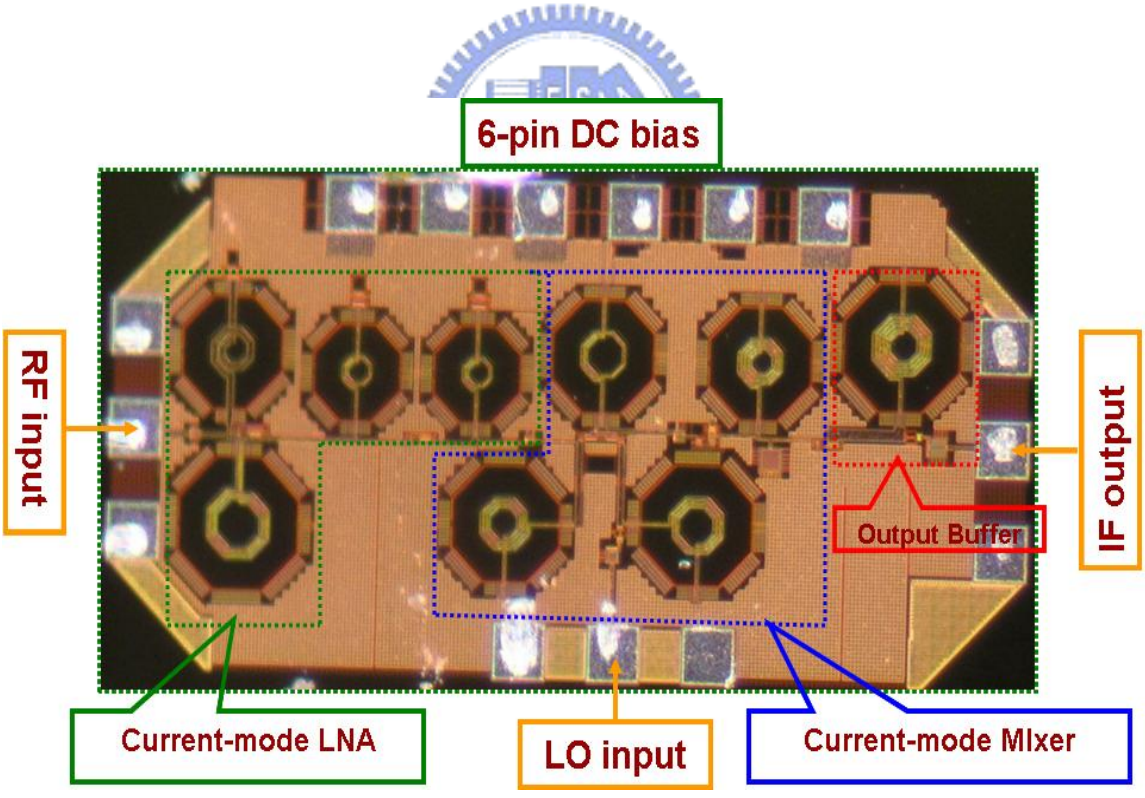


Fig. 55 Chip microphotograph.

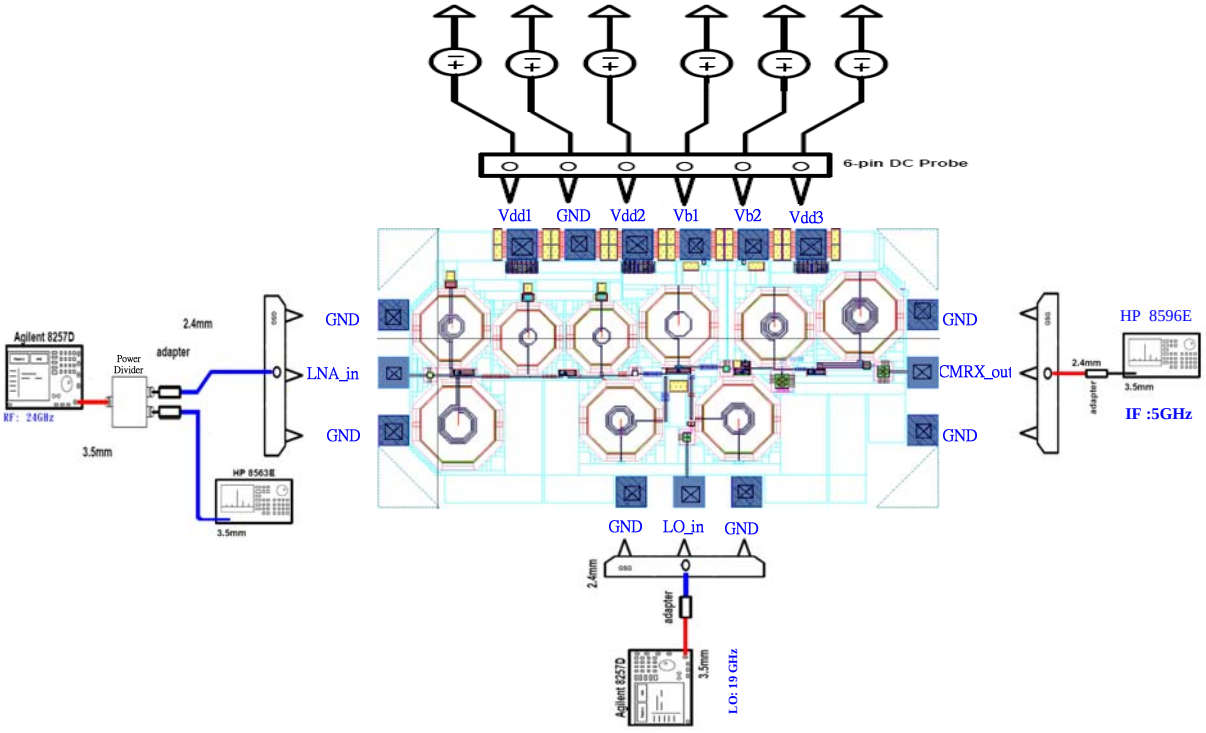


Fig. 56 Measurement setup for the receiver.

Three of the RF-GSG probes are used for RF, LO and output port, respectively. A 6-pin DC-probe is used for DC port. The power divider and spectrum analyzer are used to measure the magnitude of spectrum in the RF input pad distinctly. Since the single ended topology is adopted in this chip, the balun and transformers are not necessary in measurement. Thus, it doesn't involve the extra signal attenuation.

The measurement setups were performed in exactly the same way the front-end was simulated. The receiver front-end in this thesis is characterized by S-parameters, conversion gain, linearity (IIP3 and P_{1dB}) and noise figure (NF). A flow chart for complete receiver testing is demonstrated in Fig. 57.

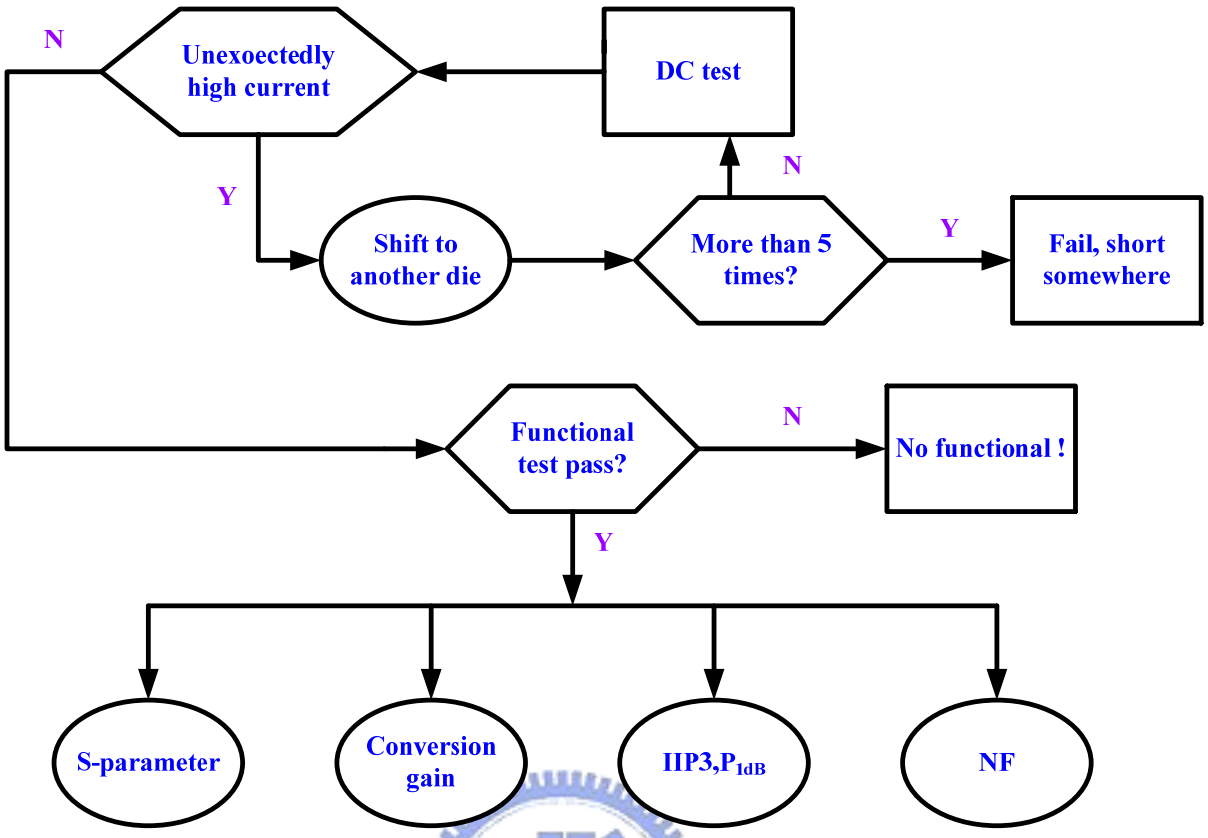


Fig. 57 The complete flow chart for receiver testing.

The first step to characterize any circuit is to set up the DC bias points for the circuit under test and observe the DC current currents flowing through the IC. The supply voltage in the circuit should be adjusted to the nominal value as in simulation. If the current through the circuit is much higher than expected, there might be a short in the circuit. In this case, the probe should be shifted to another IC sample. However, if the circuit passes this test, then other performance tests should be carried out.

After the DC biasing points have been set up, a test should also be carried out to determine whether the circuit is functional. If the circuit does not pass this test, no further tests should be carried out. However, if the circuit passes this test, the S-parameter, conversion gain, linearity and noise figure test would be performed. Therefore, the testing of measurement setups is shown in Fig. 58, Fig. 59 and Fig. 60 for the S-parameter, receiver gain and noise figure, respectively.

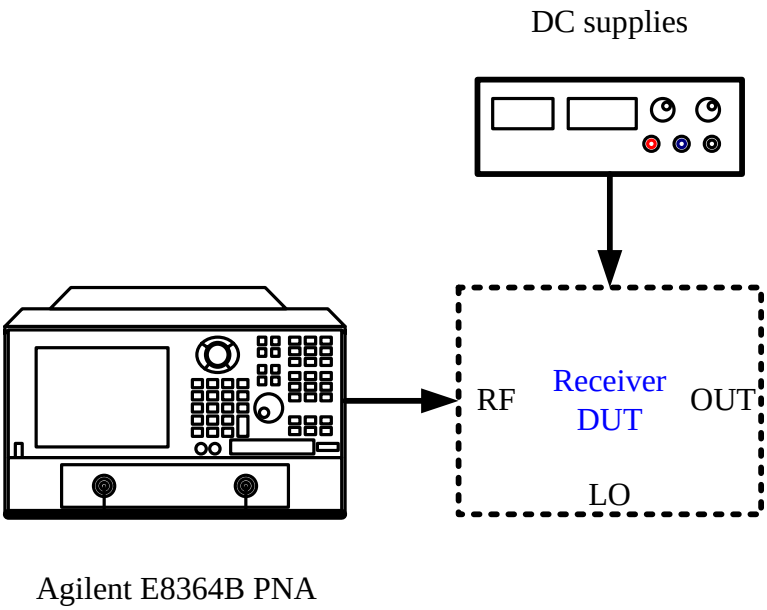


Fig. 58 Test setup for S-parameter measurement.

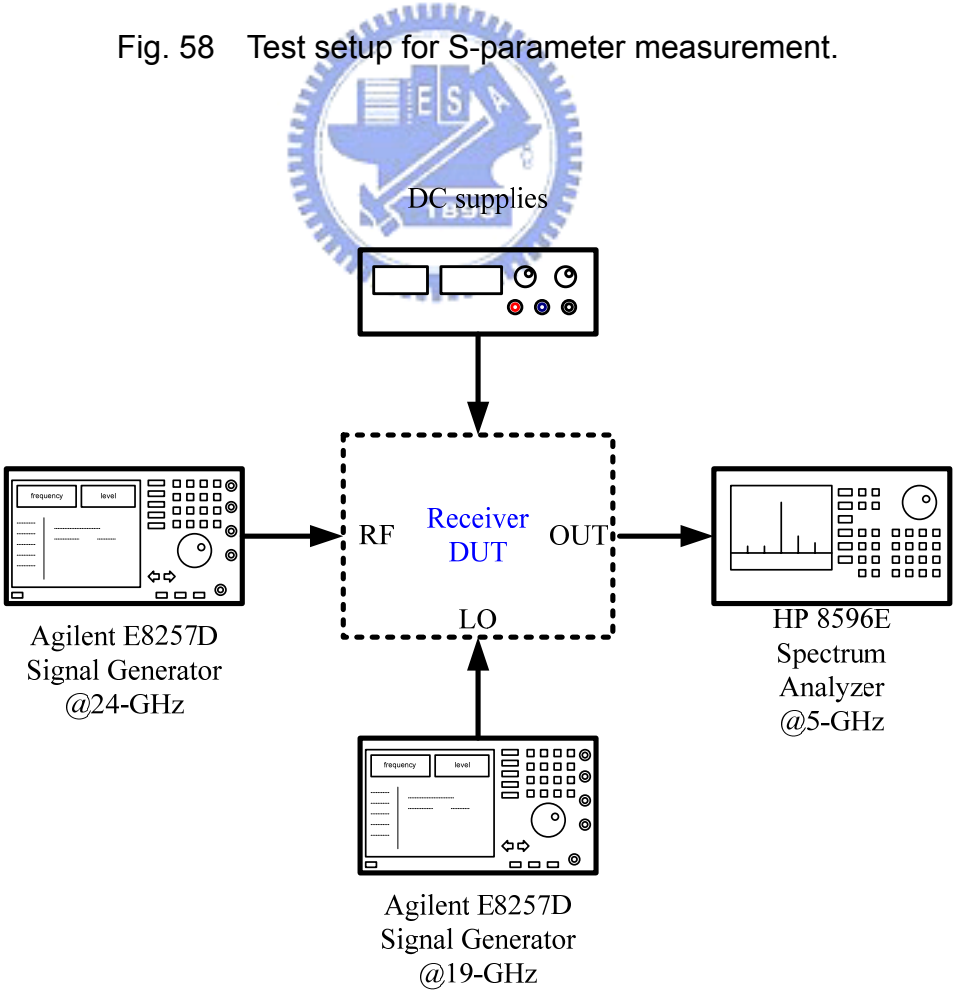


Fig. 59 Test setup for receiver gain measurement.

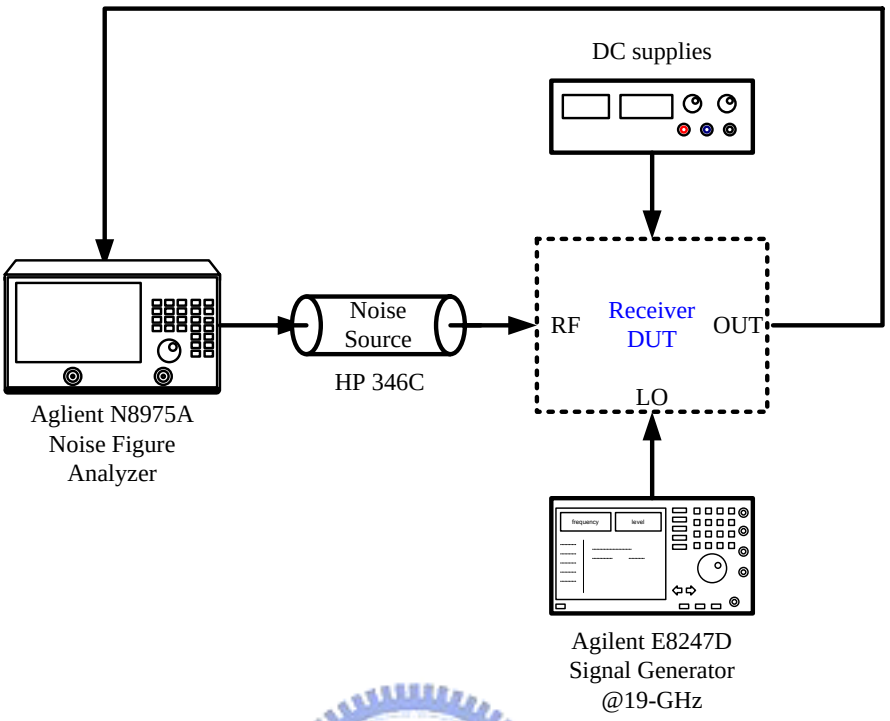


Fig. 60 Test setup for noise figure measurement.

3.3 Experimental Results

Before measuring the receiver, the loss of passive components should be measured in the first place. The loss of cable line and instrument is about 4.5 dBm at 24-GHz and 2 dBm at 5-GHz measured by spectrum analyzer. The two-port network of S-parameter analysis cannot be applied for gain measurement because the frequencies of input and output terminals are different. Therefore, the spectrum observation is a substitutive way.

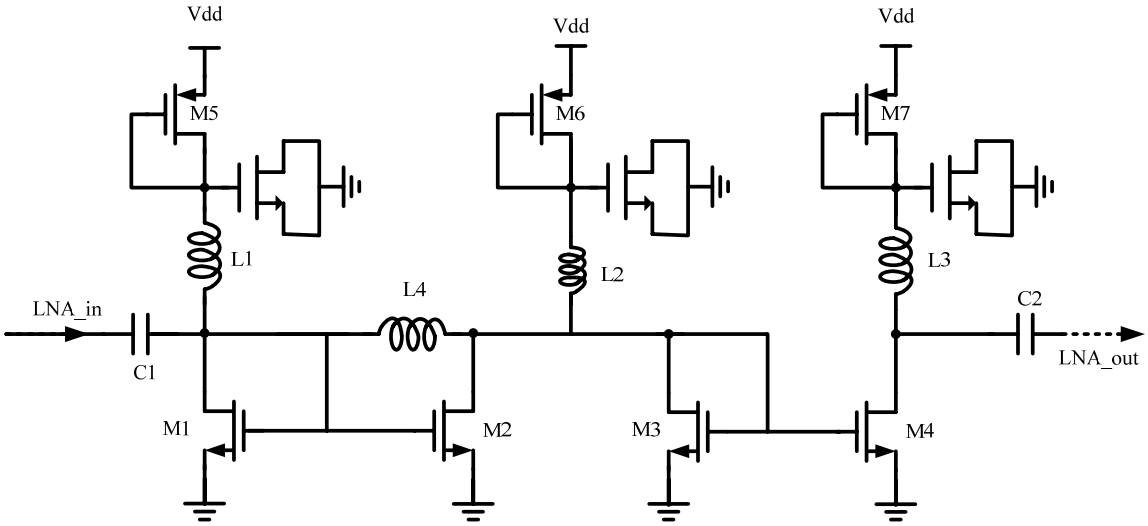


Fig. 61 The MOS capacitance in the LNA circuit.

A large value of capacitor should be used in the current-mode LNA. Because occupied area of MOS capacitors are smaller than ones of MIM capacitance. For the considerations of chip areas, the MOS capacitor is chosen. Unfortunately, due to the poly-gate resistor of MOS capacitor in the LNA circuit shown in the Fig. 61, the Q value of inductor would be decreased. Therefore, the gain performance of LNA circuit is seriously decreased. The gain performance of overall receiver decreases 14dB compared with post-simulation result. This is a serious mistake in the circuit design and the mistake should be found in the post-simulation. Unfortunately, the design Kit of ADS simulator does not provide the model of MOS capacitor and the ideal capacitance is chosen instead of the MOS capacitor. In order to measure the performance of receiver, the Focus Ion Beam (FIB) technology is adopted to grow a metal line and connected the gate terminal of MOS capacitor to Vdd node shown as the Fig. 62. The capacitor from the DC pad could restore the Q value of inductor in the LNA circuit. Therefore, the gain performance could be improved. After the remedy of FIB solution, the gain of overall receiver is about 12.5 dB increased 6dB compared with original measurement result.

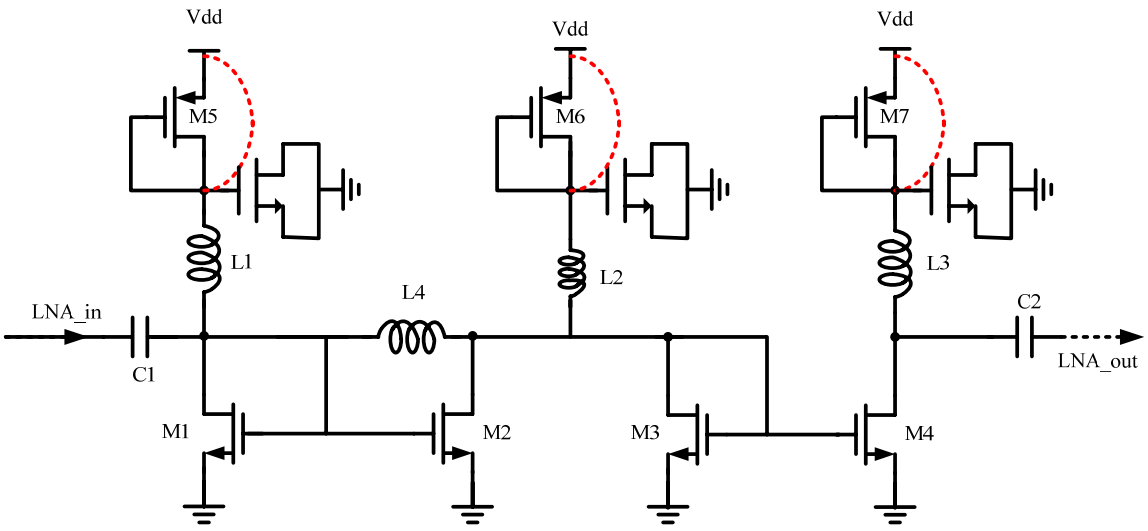


Fig. 62 The solution of FIB.

The Fig. 63 presents an output spectrum at IF port with a power of -40dBm RF (23.6-GHz) signal and a power of 5dBm LO (18.8-GHz) signal. Compensating back with the loss of cable line, the receiver performs a conversion gain of 12.5dBm under 1.2V supply voltage. In the Fig. 63, the LO to IF isolation could be calculated with the value of -39dBm. Fig. 65 plots the IF output power related to RF input power and the input 1-dB compression point is obtained with value of -18dBm. Fig. 66 shows the results of a two-tone third-order intercept point (IP3) measurement performed on the signal path. The value of IIP3 is about -3dBm. The measurement setup for noise figure is shown in Fig. 60. The SSB noise figure is obtained with the value of 13.3dB. The measured noise performance is so terrible due to the decrease of conversion gain. There are many factors to influence the performance of noise figure. Even though the calibration of noise performance has been used to modify the noise contributions from the instrument (noise figure analyzer), cable line, and the assembly of measurement setup, some of the noise contributions can not still be avoided. For example, the noise contributions from the DC supply voltage, substrate noise of the

MOS device, the noise contribution of dummy metal, dummy poly and dummy oxide layer and the external LO power signal can not be expected and simulated in advance. Therefore, the noise performance of measurement has a little difference to the simulation results.

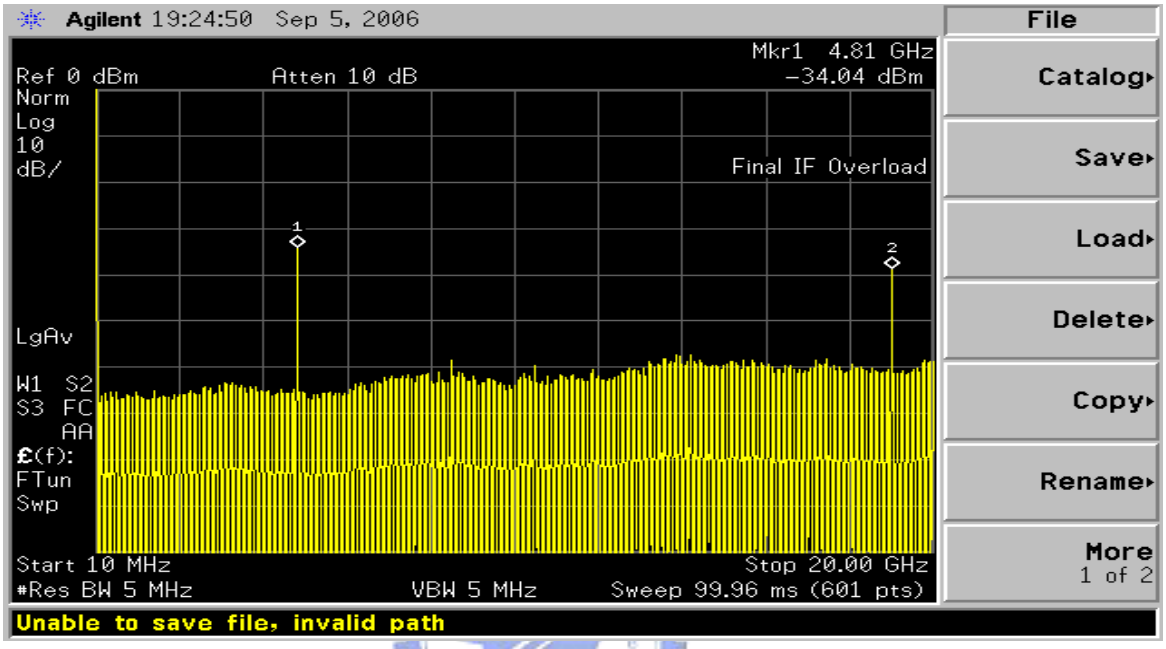


Fig. 63 The measured spectrum at IF output terminal.

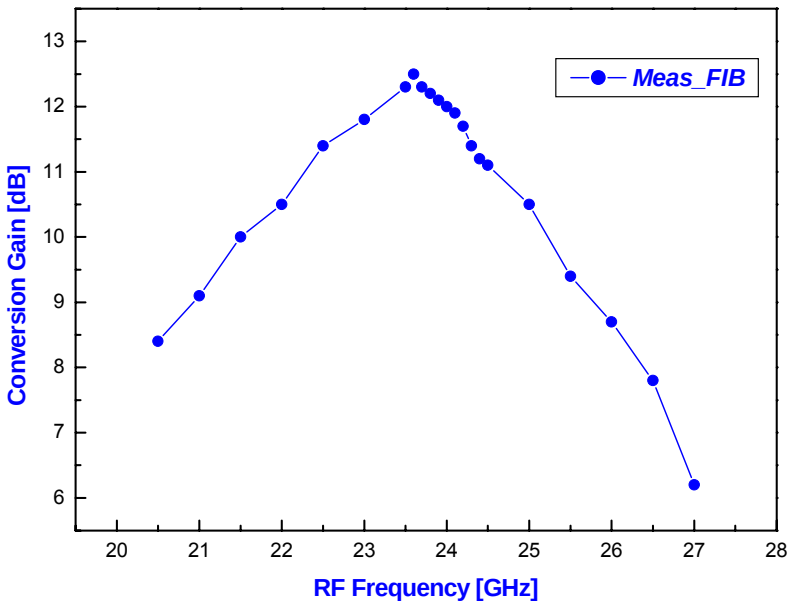


Fig. 64 Measured conversion gain of the receiver

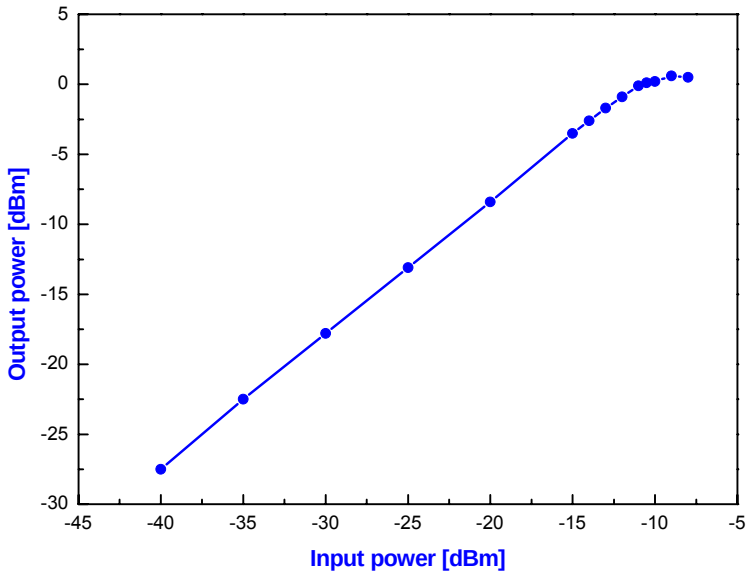


Fig. 65 Measured 1-dB compression point of the receiver.

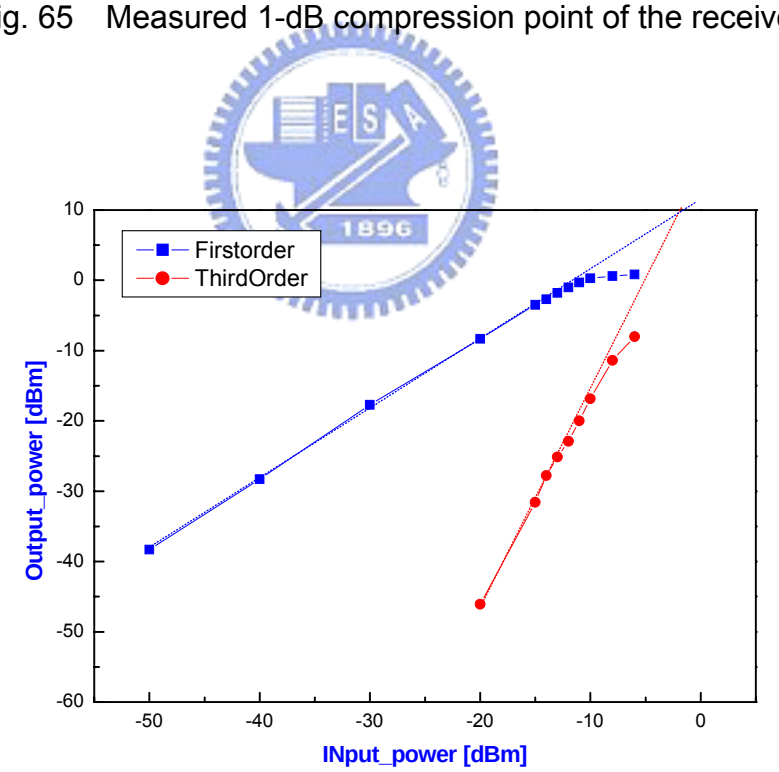


Fig. 66 Two-tone IIP3 measurement for the receiver

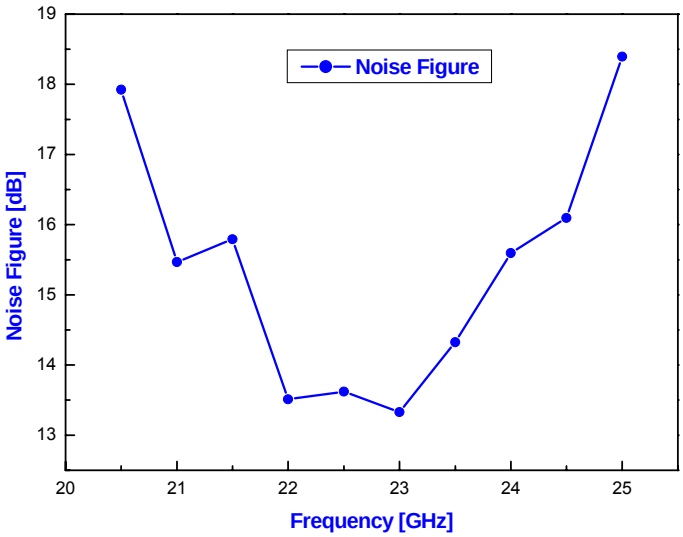


Fig. 67 Measured noise figure of the receiver

The value of fine-tuned supply voltage and biasing voltage are listed and compared with post-simulation in the Table(vi). The power consumption of the tested receiver is about 49.8mW. The power consumption is higher than post-simulation due to the raise of operated voltage of each LNA MOS device. Table(vii) lists the summary of the measurement results of the tested receiver. Table(viii) presents the measurement results in the different supply voltage of LNA circuit.

Table(vi) Comparison on bias status between post-simulation and measurement

	post-simulation	Meas_FIB
VDD1	1.2 V	1.2 V
VDD2	1.2 V	1.2 V
VDD3	1.2 V	1.2 V
Vb1	0.65 V	0.75 V
Vb2	1.1 V	1.0 V

Table(vii) Summary of the measurement results

	post-simulation	Meas_FIB
Frequency[GHz]	24	23.6
$Gain_{LNA}$[dB]	17.1	N/A
NF_{LNA}[dB]	3.4	N/A
$Gain_{RX}$[dB]	20.9	12.5
NF_{RX}[dB]	4.2	13.3
IIP3[dBm]	-14	-3
P_{1dB}[dBm]	-24.5	-15
Image rejection[dB]	32.1	33.2
Total power [mW]	24.3	49.8
S11(<10dB)	23.2~24.3 GHz	23.8~28.1 GHz
S22(<10dB)	>13.5 GHz	>9.8 GHz
S33(<10dB)	4.0~6.3 GHz	3.2~7.4 GHz

Table(viii) Summary of the measurement results with different supply voltage.

	Meas_FIB	Meas_FIB
Supply voltage	1.2	0.8
Peak frequency[GHz]	23.6	23.6
$Gain_{RX}$[dB]	12.5	11.3
NF_{RX}[dB]	13.3	14.2
IIP3[dBm]	-3	-2
P_{1dB}[dBm]	-15	-13.5
Image rejection[dB]	33.2	33.5
Total power [mW]	49.8	27.8
S11(<10dB)	23.8~28.1 GHz	23.6~27.8 GHz
S22(<10dB)	>9.8 GHz	>9.8 GHz
S33(<10dB)	3.2~7.4 GHz	3.2~7.4 GHz

3.4 Discussions and Comparisons

First, the problem of conversion gain decrease is discussed. A large value of capacitor is used in the current-mode LNA. Because occupied area of MOS capacitor are smaller than ones of MIM capacitance. For the considerations of chip areas, the MOS capacitor is chosen. Unfortunately, there is an unexpected resistor from the polygate of MOS capacitor and the Q of the inductor in the current-mode LNA would be debased. The performance of conversion gain would also be debased. Therefore, The MOS capacitors used in the current-mode LNA can be replaced with MIM capacitors for better performance. For the measurement, the FIB technology is adopted to grow a metal line and connected the gate terminal of MOS capacitor to Vdd termination shown as the Fig. 62. After the remedy of FIB solution, the fabricated

current-mode receiver has conversion gain of 12.5dB. Because the metal line of FIB has 3 Ohm/square sheet resistance, the Q value of inductor in the LNA circuit can not restore well. The photo of FIB solution presents in the Fig. 68. A resistance of16.7 Ohm is used to estimate the resistance of metal line in the revised post-simulation. Fig. 69 plots the revised post-simulation result of conversion gain. The revised post simulation result of noise performance is shown in Fig. 70. The noise figure is about 8.5dB at 24-GHz frequency range. The noise figure of overall current-mode receiver is shown as the following equation.

$$NF_{tot} = NF_{LNA} + \frac{NF_{Mixer} - 1}{A_{LNA}} + \dots$$

The operating frequency of NF_{mim} of current-mode LNA, maximum power gain of current-mode LNA and NF_{mim} of current-mode downcoverter are about 24-GHz, 22.5-GHz and 25-GHz, respectively. Therefore, the noise figure of overall current-mode receiver is flat. Fig. 71 plots the IF output power related to RF input power. The revised simulated 1-dB compression point is obtained with a value of -18 dBm. Table(ix) lists a summary table comparing the revised post-simulation results. Table(x) compares the proposed 24-GHz CMOS receiver [8].

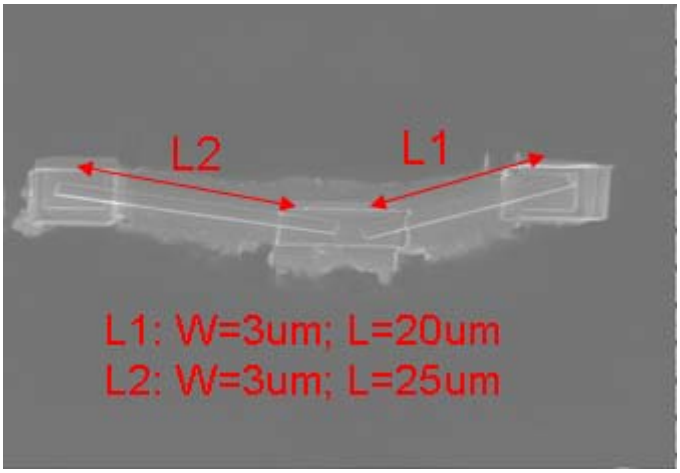


Fig. 68 The photo of FIB solution.

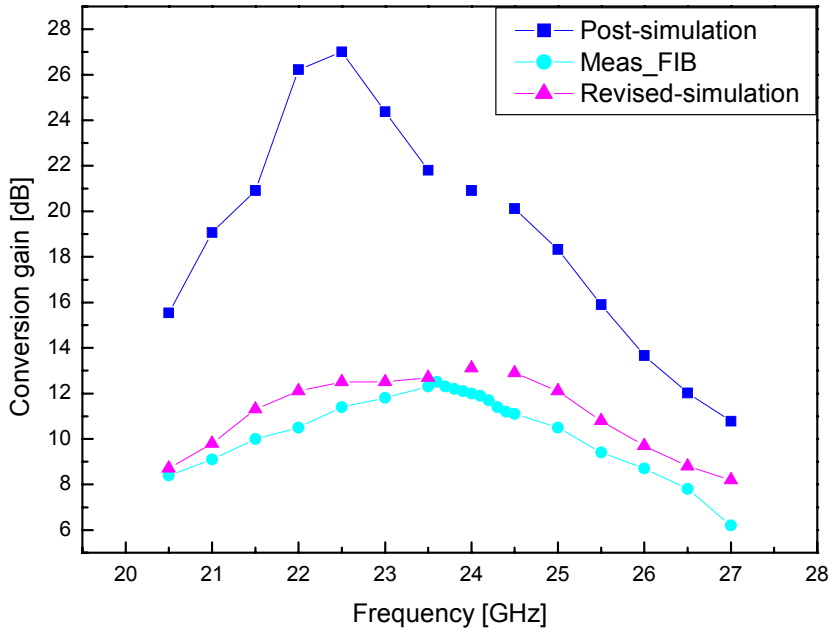


Fig. 69 Revised post-simulation of conversion gain.

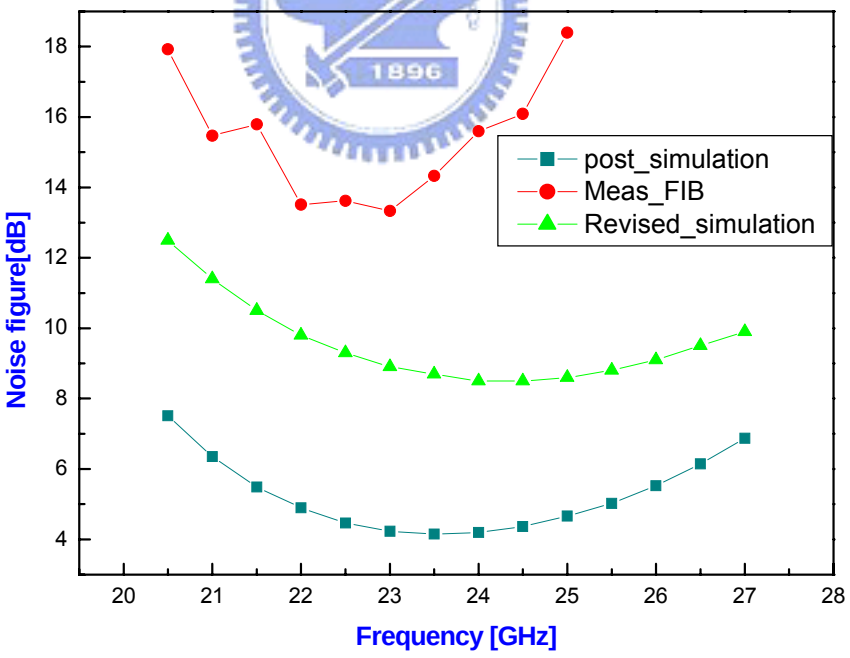


Fig. 70 Revised post-simulation of noise figure.

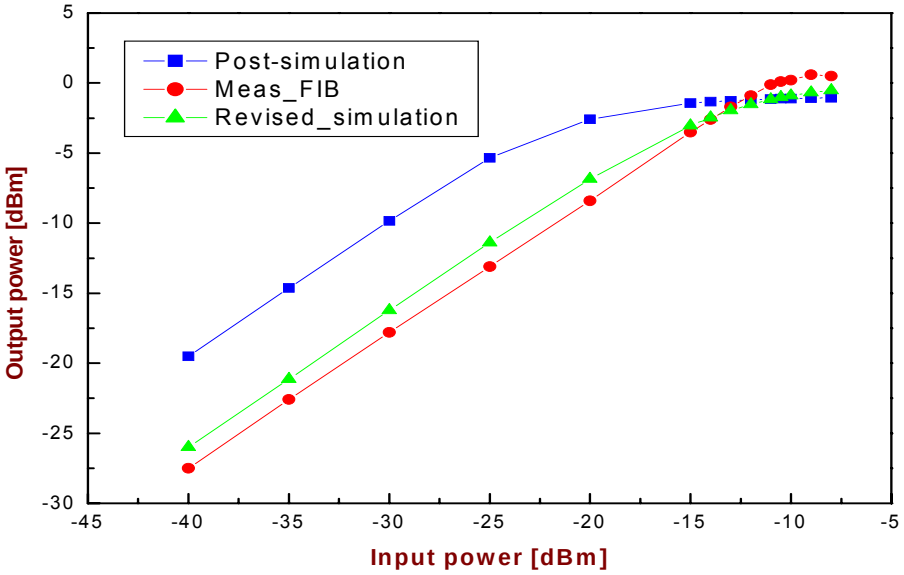


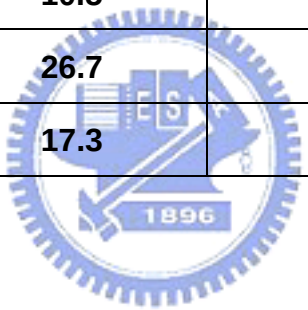
Fig. 71 Revised post-simulation of 1-dB compression point.

Table(ix) Summary of revised post-simulation results

	Post-simulation	Meas_FIB	Revised post simulation
$Gain_{LNA}$[dB]	17.1	N/A	9.8
NF_{LNA}[dB]	3.4	N/A	6.7
$Gain_{RX}$[dB]	20.9	12.5	13.1
NF_{RX}[dB]	4.2	13.3	8.5
IIP3[dBm]	-14	-3	-7.3
P_{1dB}[dBm]	-24.5	-15	-18
Image rejection[dB]	32.1	33.2	31
Total power [mW]	24.3	49.8	55.4
S11(<10dB)	23.2~24.3 GHz	23.8~28.1 GHz	22~25.3 GHz
S22(<10dB)	>13.5 GHz	>9.8 GHz	>13.5 GHz
S33(<10dB)	4.0~6.3 GHz	3.2~7.4 GHz	3.9~6.3 GHz

Table(x) Comparison of performance with other proposed 24-GHz Receiver.

	Post-simulation	Meas_FIB	[8]
$Gain_{LNA}$[dB]	17.1	N/A	15
NF_{LNA}[dB]	3.4	N/A	6
$Gain_{RX}$[dB]	20.9	12.5	27.5
NF_{RX}[dB]	4.2	13.3	7.7
IIP3[dBm]	-14	-3	N/A
P_{1dB}[dBm]	-24.5	-15	-23
Image rejection[dB]	32.1	33.2	31
Total power [mW]	24.3	49.8	30
S11(<10dB)	10.5	12.1	-21
S22(<10dB)	26.7	-26	N/A
S33(<10dB)	17.3	-21.6	-10



CHAPTER 4 CONCLUSIONS AND FUTURE WORK

4.1 Conclusions

A new 24-GHz RF CMOS current-mode receiver front-end integrated with a current-mode low-noise amplifier and a current-mode downconverter is completely designed, fabricated in 0.13-um CMOS technology and measured. A new LNA and downconverter with current-mode operation have been proposed. The 2-stage cascade current-mirror amplifiers are employed to implement a current-mode LNA and only four inductors are used. Current summing and current squaring circuits are adopted to form a current multiplier in the current-mode downconverter. The measured results exhibit that the receiver can operate well at 24-GHz frequency range. But is doesn't achieve adequate performance due to the oversight of layout. After the remedy of FIB solution, the fabricated current-mode receiver front-end has conversion gain of 12.5dB, noise figure of 13.3 dB, and drains 41.5mA under 1.2V supply voltage with chip area of 1mm^2.

4.2 Future Work

The MOS capacitors used in the current-mode LNA circuit can be replaced with MIM capacitor for better performance. The current-mode downconverter can be re-designed for low supply voltage operation. For the integrity of current-mode receiver front-end, the current-mode VCO could been included. Finally, a frequency synthesizer also can be included to obtain a stable LO signal.

REFERENCES

[1] B. Razavi, “CMOS technology characterization for analog and RF design,” IEEE J. Solid-State Circuits, vol. 34, pp. 268-276, Mar. 1999.

[2] B. Razavi, RF Microelectronics, Upper Saddle River, NJ: Prentice Hall, 1998.

[3] John Rogers and Calvin Plett, Radio Frequency Integrated Circuit Design, Boston. London, MA: Artech House, April 2003.

[4] D. K. Shaeffer and T. H. Lee, “A 1.5V 1.5-GHz CMOS Low Noise Amplifier,” VLSI Circuits Symp. Dig. Tech. Papers, pp. 32-33, June 1996.

[5] D. K. Shaeffer and T. H. Lee, The Design and Implementation of Low Power CMOS Radio Receivers. Boston, MA: Kluwer, 1999.

[6] B. Razavi, IEEE Fellow, “A 60-GHz CMOS Receiver Front-End,” IEEE Journal of Solid-State Circuits, vol. 41, no. 1, January 2006.

[7] K.-W. Yu, Y.-L. Lu, D.-C. Chang, V. Liang, and M. F. Chang, “K-band low-noise amplifiers using 0.18-um CMOS technology,” *IEEE Microw. Wireless Compon. Lett.*, vol. 14, no. 3, pp. 106–108, Mar. 2004.

[8] X. Guan and A. Hajimiri, “A 24 GHz CMOS front-end,” IEEE Journal of Solid-State Circuits, vol.38, Feb. 2004, pp.368-373

[9] S.G Lee and L.K Choi, “Current-reuse bleeding mixer,” Electronics letters, vol.36, no.8, 13th April 2000.

[10] S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Brodersen, “A 60-GHz down-converting CMOS single-gate mixer,” in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, Jun. 2005, pp.163–166.

[11] F. Ellinger, L. C. Rodoni, G. Sialm, C. Kromer, G. von Buren, M.L.Schmatz, C. Menolfi, T. Toifl, T. Morf, M. Kossel, and H. Jackel,“30–40-GHz drain-pumped

passive-mixer MMIC fabricated on VLSISOI CMOS technology," IEEE Trans. Microw. Theory Tech., vol.52, no.5, pp. 1382-1391, May 2004.

[12] H. T. Friis, "Noise Figure of Radio Receivers," in proc. IRE, vol. 32, pp.419-422, jul. 1994.

[13] T. H. Lee, the design of CMOS radio-frequency integrated circuits, second edition, Boston , MA: Cambridge, 2004

[14] A. A. Abidi, "High-frequency noise measurement on FET's with small dimensions," *IEEE Transactions in Electron Devices*, vol. ED-33, no.11, pp. 1801-1805, Nov. 1986.

[15] Aldert van der Ziel, "Noise in solid-state devices and lasers," *Proceeding of the IEEE,* vol. 58, no. 8, pp. 1178-1206, Aug. 1970.

[16] R. P. Jindal, "Noise associated with distributed resistance of MOSFET gate structures in integrated circuits," *IEEE Transactions on Electron Devices*, vol. ED-31, no. 10, pp. 1505-1509, Oct.1984

[17] Behzad Razavi, Run-Hong Yan and Kwing F. Lee, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, vol. 41, no. 11, pp.750-754, Nov.1994.

[18] "Fundamentals of RF and microwave noise figure measurements," Aglient Technologies, Palo Alto, CA, Application note 57-1.

[19] H. Samavati, H. R. Rategh and T. H. Lee, "A 5-GHz CMOS Wireless LAN receiver Front-End," *IEEE J. Solid-State Circuits*, vol. 35, pp. 765-772, May 2000.

[20] Joy Laskar, Babak Matinpour and Sudipto Chakraborty, Modern Receiver Front-End, Upper Saddle River, MA: John Wiley & Sons, Inc. (US), 2004.

[21] Huei Wang, Shih-Chieh Shin, "18-26 GHz Low-Noise amplifier Using 130- and 90-nm Bulk CMOS technologies", *Symposium on Radio Frequency Integrated*

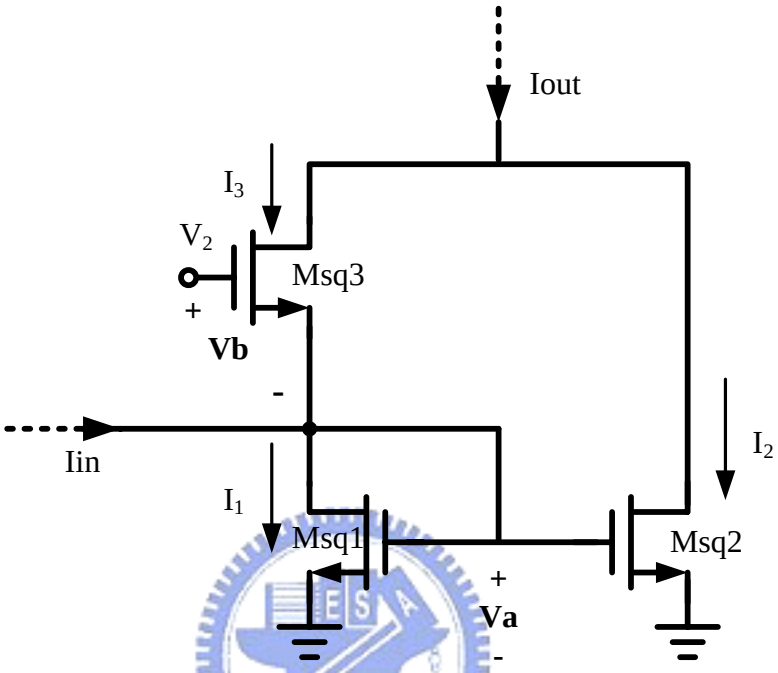
Circuits (RFIC), 2005

[22] Shih-Chieh Shin, Ming-Da Tsai, Ren-Chieh Liu, Kun-You Lin, and Huei Wang," A 24GHz 3.9-dB NF Low-Noise Amplifier Using 0.18um CMOS Technology," IEEE Microwave and Wireless Components Letters,Vol.15, NO. 7, July 2005

[23] Olivier Dupuis, Xiao Sun, Geert Carchon, Philippe Soussan, Mattias Frendahl, Stefaan Decoutere and Walter Raedt, "24 GHz LNA in 90nm RF-CMOS with High-Q Above-IC Inductors", Proceedings of ESSCIRC, Grenoble, France, 2005

APPENDIX

I. Current-square circuit for short channel effect:



The simplified current squaring circuit

From the above figure, the correlation between Iin and Iout can be calculated as the following equation with different V_{DS} voltage.

$$K = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$$

$$I_1 = K(V_a - V_t)^2[1+\lambda(\frac{V_{DD}}{2}-\Delta)]$$

$$I_3 = K(V_b - V_t)^2[1+\lambda(\frac{V_{DD}}{2}+\Delta)]$$

$$I_{in} = I_1 - I_3 = K(V_a - V_t)^2[1+\lambda(\frac{V_{DD}}{2}-\Delta)] - K(V_b - V_t)^2[1+\lambda(\frac{V_{DD}}{2}+\Delta)]$$

$$\Rightarrow (V_a^2 - 2V_aV_t + V_t^2)(1+\frac{\lambda V_{DD}}{2}-\Delta\lambda) - (V_b^2 - 2V_bV_t + V_t^2)(1+\frac{\lambda V_{DD}}{2}+\Delta\lambda) = \frac{I_{in}}{K}$$

$$\Rightarrow (V_a^2 + \frac{\lambda V_{DD}}{2}V_a^2 - \Delta\lambda V_a^2 - 2V_aV_t - \lambda V_{DD}V_aV_t + 2V_aV_t\Delta\lambda + V_t^2 + \frac{\lambda V_{DD}}{2}V_t^2 - \Delta\lambda V_t^2)$$

$$-(V_b^2 + \frac{\lambda V_{DD}}{2}V_b^2 + \Delta\lambda V_b^2 - 2V_bV_t - \lambda V_{DD}V_bV_t - 2V_bV_t\Delta\lambda + V_t^2 + \frac{\lambda V_{DD}}{2}V_t^2 + \Delta\lambda V_t^2) = \frac{I_{in}}{K}$$

$$\Rightarrow (V_a^2+\frac{\lambda V_{DD}}{2}V_a^2-\Delta\lambda V_a^2-2V_aV_t-\lambda V_{DD}V_aV_t+2V_aV_t\Delta\lambda+V_t^2+\frac{\lambda V_{DD}}{2}V_t^2-\Delta\lambda V_t^2)$$
$$-(V_b^2+\frac{\lambda V_{DD}}{2}V_b^2+\Delta\lambda V_b^2-2V_bV_t-\lambda V_{DD}V_bV_t-2V_bV_t\Delta\lambda+V_t^2+\frac{\lambda V_{DD}}{2}V_t^2+\Delta\lambda V_t^2)=\frac{I_{in}}{K}$$
$$\Rightarrow (V_a^2-V_b^2)+\frac{\lambda V_{DD}}{2}(V_a^2-V_b^2)-\Delta\lambda(V_a^2+V_b^2)-2V_t(V_a-V_b)$$
$$-\lambda V_{DD}V_t(V_a-V_b)+2V_t\Delta\lambda(V_a+V_b)-2\Delta\lambda V_t^2=\frac{I_{in}}{K}$$
$$\Rightarrow (V_a^2-V_b^2)(1+\frac{\lambda V_{DD}}{2})-\Delta\lambda(V_a^2+V_b^2)-(V_a-V_b)(2V_t+\lambda V_{DD}V_t)+2V_t\Delta\lambda(V_a+V_b)-2\Delta\lambda V_t^2=\frac{I_{in}}{K}$$
$$\Rightarrow V_2(V_a-V_b)(1+\frac{\lambda V_{DD}}{2})-\Delta\lambda[(V_a+V_b)^2-2V_aV_b]-(V_a-V_b)V_t(2+\lambda V_{DD})+2V_t\Delta\lambda(V_a+V_b)-2\Delta\lambda V_t^2=\frac{I_{in}}{K}$$
$$\Rightarrow -\Delta\lambda(V_2^2-2V_aV_b)+(V_a-V_b)[V_2(1+\frac{\lambda V_{DD}}{2})-(2+\lambda V_{DD})V_t]+2V_t\Delta\lambda(V_2-V_t)=\frac{I_{in}}{K}$$
$$\Rightarrow -\Delta\lambda(V_2^2-2V_aV_b)+(V_a-V_b)(1+\frac{\lambda V_{DD}}{2})(V_2-2V_t)+2V_t\Delta\lambda(V_2-V_t)=\frac{I_{in}}{K}.....(1)$$

From the correlation of output current I_{out} and I_{in} , we can find the equation of (V_a-V_b) and V_a*V_b.

$$I_{in}=I_1-I_3\ \&\ I_2+I_3=I_{out}$$
$$\Rightarrow I_1+I_2=I_{in}+I_{out}$$
$$\Rightarrow (V_a-V_t)^2(1+\frac{\lambda V_{DD}}{2}-\Delta\lambda)+(V_a-V_t)^2(1+\lambda V_{DD})=\frac{I_{in}+I_{out}}{K}$$
$$\Rightarrow (V_a-V_t)^2(2+\frac{3}{2}\lambda V_{DD}-\Delta\lambda)=\frac{I_{in}+I_{out}}{K}$$
$$\Rightarrow V_a=V_t+\sqrt{\frac{I_{in}+I_{out}}{K(2+\frac{3}{2}\lambda V_{DD}-\Delta\lambda)}}\ ;\ V_b=V_2-V_a=V_2-V_t-\sqrt{\frac{I_{in}+I_{out}}{K(2+\frac{3}{2}\lambda V_{DD}-\Delta\lambda)}}$$
$$\therefore V_a-V_b=2\sqrt{\frac{I_{in}+I_{out}}{K(2+\frac{3}{2}\lambda V_{DD}-\Delta\lambda)}}+2V_t-V_2=C\sqrt{I_{in}+I_{out}}+2V_t-V_2$$
$$C=\frac{2}{\sqrt{K(2+\frac{3}{2}\lambda V_{DD}-\Delta\lambda)}}$$
$$V_aV_b=V_a(V_2-V_a)=V_aV_2-V_a^2=V_2(V_t+\frac{C}{2}\sqrt{I_{in}+I_{out}})-(V_t+\frac{C}{2}\sqrt{I_{in}+I_{out}})^2$$

Take the equation of $(V_a-V_{b)}$ and V_a*V_b into equation (1).

$$\Rightarrow -\Delta\lambda[V_2^2 - 2V_2(V_t + \frac{C}{2}\sqrt{I_{in}+I_{out}}) + 2V_t^2 + 2CV_t\sqrt{I_{in}+I_{out}} + \frac{C^2}{2}(I_{in}+I_{out})]$$

$$+ (1+\frac{\lambda V_{DD}}{2})(V_2 - 2V_t)(C\sqrt{I_{in}+I_{out}} + 2V_t - V_2) + 2\Delta\lambda V_t(V_2 - V_t) = \frac{I_{in}}{K}$$

$$\Rightarrow (-\frac{1}{K} - \Delta\lambda\frac{C^2}{2})I_{in} - \Delta\lambda\frac{C^2}{2}I_{out} + C[\Delta\lambda V_2 - 2\Delta\lambda V_t + (1+\frac{\lambda V_{DD}}{2})(V_2 - 2V_t)]\sqrt{I_{in}+I_{out}}$$

$$+ [\Delta\lambda(-V_2^2 + 2V_2V_t - 2V_t^2) - (V_2 - 2V_t)^2(1+\frac{\lambda V_{DD}}{2}) + 2\Delta V_t(V_2 - V_t)] = 0$$

$$\Rightarrow DI_{in} + EI_{out} + F\sqrt{I_{in}+I_{out}} + G = 0$$

where $D = (-\frac{1}{K} - \Delta\lambda\frac{C^2}{2})$; $E = -\Delta\lambda\frac{C^2}{2}$; $F = C(V_2 - 2V_t)(1+\frac{\lambda V_{DD}}{2} + \Delta\lambda)$;

$$G = \Delta\lambda(-V_2^2 + 2V_2V_t - 2V_t^2) - (V_2 - 2V_t)^2(1+\frac{\lambda V_{DD}}{2}) + 2\Delta V_t(V_2 - V_t)$$

$$= -(V_2 - 2V_t)^2(1+\frac{\lambda V_{DD}}{2} + \Delta\lambda)$$

$$\Rightarrow DI_{in} + EI_{out} + G = -F\sqrt{I_{in}+I_{out}}$$

$$\Rightarrow D^2I_{in}^2 + E^2I_{out}^2 + G^2 + 2DEI_{out}I_{in} + 2DGI_{in} + 2EGI_{out} = F^2(I_{out}+I_{in}).....(2)$$

$$\because C^2 = \frac{4}{K(2+\frac{3}{2}\lambda V_{DD} - \Delta\lambda)} \approx \frac{4}{K(2+\frac{3}{2}\lambda V_{DD})}(1+\frac{\Delta\lambda}{2+\frac{3}{2}\lambda V_{DD}})$$

$$\Delta\lambda C^2 \approx \frac{4\Delta\lambda}{K(2+\frac{3}{2}\lambda V_{DD})}$$

$$D^2 = (-\frac{1}{K} - \Delta\lambda\frac{C^2}{2})^2 \approx \frac{1}{K^2} + \frac{C^2}{K}\Delta\lambda \approx \frac{1}{K^2}(1+\frac{4\Delta\lambda}{2+\frac{3}{2}\lambda V_{DD}})$$

$$E^2 = (-\Delta\lambda\frac{C^2}{2})^2 \approx 0$$

$$G^2 = (V_2 - 2V_t)^4 * (1+\frac{\lambda V_{DD}}{2} + \Delta\lambda)^2 \approx (V_2 - 2V_t)^4 * (1+\frac{\lambda^2V_{DD}^2}{4} + \lambda V_{DD} + 2\Delta\lambda + \Delta\lambda^2V_{DD})$$

$$DE = (-\frac{1}{K} - \Delta\lambda\frac{C^2}{2}) * (-\Delta\lambda\frac{C^2}{2}) \approx \frac{\Delta\lambda C^2}{2K} = \frac{2\Delta\lambda}{K^2(2+\frac{3}{2}\lambda V_{DD})}$$

$$DG = (-\frac{1}{K} - \Delta\lambda\frac{C^2}{2}) * (-1) * (V_2 - 2V_t)^2 (1 + \frac{\lambda V_{DD}}{2} + \Delta\lambda)$$

$$= (V_2 - 2V_t)^2 (\frac{1}{K} + \frac{\Delta\lambda C^2}{2})(1 + \frac{\lambda V_{DD}}{2} + \Delta\lambda)$$

$$= (V_2 - 2V_t)^2 [\frac{1}{K}(1 + \frac{\lambda V_{DD}}{2} + \Delta\lambda) + \frac{\Delta\lambda C^2}{2} * (1 + \frac{\lambda V_{DD}}{2})]$$

$$\approx (V_2 - 2V_t)^2 [\frac{1}{K}(1 + \frac{\lambda V_{DD}}{2} + \Delta\lambda) + \frac{(2 + \lambda V_{DD}) * \Delta\lambda}{K(2 + \frac{3}{2}\lambda V_{DD})}]$$

$$= \frac{(V_2 - 2V_t)^2}{K}(1 + \frac{\lambda V_{DD}}{2} + \Delta\lambda + \frac{(2 + \lambda V_{DD}) * \Delta\lambda}{(2 + \frac{3}{2}\lambda V_{DD})})$$

$$= \frac{(V_2 - 2V_t)^2}{K}(1 + \frac{\lambda V_{DD}}{2} + \frac{4 + \frac{5}{2}\lambda V_{DD}}{2 + \frac{3}{2}\lambda V_{DD}}\Delta\lambda)$$

$$EG = (-\Delta\lambda\frac{C^2}{2}) * [-(V_2 - 2V_t)^2 (1 + \frac{\lambda V_{DD}}{2} + \Delta\lambda)] \approx \frac{\Delta\lambda C^2}{2} * (V_2 - 2V_t)^2 * (1 + \frac{\lambda V_{DD}}{2})$$

$$= \frac{2(V_2 - 2V_t)^2 \Delta\lambda}{K(2 + \frac{3}{2}\lambda V_{DD})}(1 + \frac{\lambda V_{DD}}{2})$$

$$F^2 = C^2 * (V_2 - 2V_t)^2 * (1 + \frac{\lambda V_{DD}}{2} + \Delta\lambda)^2 \approx \frac{4(V_2 - 2V_t)^2}{K(2 + \frac{3}{2}\lambda V_{DD})} * (1 + \frac{\Delta\lambda}{2 + \frac{3}{2}\lambda V_{DD}}) * (1 + \frac{\lambda^2 V_{DD}^2}{4} + \lambda V_{DD} + 2\Delta\lambda + \Delta\lambda^2 V_{DD})$$

$$\approx \frac{4(V_2 - 2V_t)^2}{K(2 + \frac{3}{2}\lambda V_{DD})} * [(1 + \frac{\lambda^2 V_{DD}^2}{4} + \lambda V_{DD} + 2\Delta\lambda + \Delta\lambda^2 V_{DD}) + \frac{1}{2 + \frac{3}{2}\lambda V_{DD}}(\Delta\lambda + \Delta\lambda^2 V_{DD})]$$

$$\approx \frac{4 * (V_2 - 2V_t)^2}{K(2 + \frac{3}{2}\lambda V_{DD})}[1 + \frac{\lambda^2 V_{DD}^2}{4} + \lambda V_{DD} + \Delta\lambda * (2 + \frac{1}{2 + \frac{3}{2}\lambda V_{DD}}) + \Delta\lambda^2 V_{DD} * (1 + \frac{1}{2 + \frac{3}{2}\lambda V_{DD}}) + \frac{\frac{\Delta\lambda^3 V_{DD}^2}{4}}{2 + \frac{3}{2}\lambda V_{DD}}]$$

$$= \frac{4 * (V_2 - 2V_t)^2}{K(2 + \frac{3}{2}\lambda V_{DD})}[1 + \frac{\lambda^2 V_{DD}^2}{4} + \lambda V_{DD} + (\frac{5 + 3\lambda V_{DD}}{2 + \frac{3}{2}\lambda V_{DD}}) * \Delta\lambda + (\frac{3 + \frac{3}{2}\lambda V_{DD}}{2 + \frac{3}{2}\lambda V_{DD}}) * \Delta\lambda^2 V_{DD} + \frac{\frac{1}{4}}{2 + \frac{3}{2}\lambda V_{DD}} * \Delta\lambda^3 V_{DD}^2]$$

$$= \frac{4 * (V_2 - 2V_t)^2}{K(2 + \frac{3}{2}\lambda V_{DD})}(1 + \frac{\lambda^2 V_{DD}^2}{4} + \lambda V_{DD} + \frac{5\Delta\lambda + 6\Delta\lambda^2 V_{DD} + \frac{7}{4}\Delta\lambda^3 V_{DD}^2}{2 + \frac{3}{2}\lambda V_{DD}})$$

Thus, the equation (2) can be simplified as the following equation.

$$D^2 I_{in}^2 + G^2 + 2DEI_{in} + 2DGI_{in} + 2EGI_{out} = F^2(I_{out} + I_{in})$$

$$\Rightarrow (F^2 - 2EG)I_{out} = D^2 I_{in}^2 + 2DEI_{in} + 2DGI_{in} - F^2 I_{in} + G^2$$

$$\Rightarrow I_{out} = \frac{D^2 I_{in}^2 + (2DE + 2DG - F^2)I_{in} + G^2}{F^2 - 2EG}$$

$$= \frac{D^2}{F^2 - 2EG} I_{in}^2 + \frac{2DE + 2DG - F^2}{F^2 - 2EG} I_{in} + \frac{G^2}{F^2 - 2EG}$$

$$= \frac{\frac{1}{K^2}(1 + \frac{4\Delta\lambda}{2 + \frac{3}{2}\lambda V_{DD}})}{\frac{4(V_2 - 2V_t)^2}{K(2 + \frac{3}{2}\lambda V_{DD})}(1 + \frac{\lambda^2 V_{DD}^2}{4} + \lambda V_{DD} + \frac{3\Delta\lambda + \frac{7}{2}\Delta\lambda^2 V_{DD} + \Delta\lambda^3 V_{DD}^2}{2 + \frac{3}{2}\lambda V_{DD}})} I_{in}^2$$

$$+ \frac{\frac{2}{K(2 + \frac{3}{2}\lambda V_{DD})}[\frac{2\Delta\lambda}{K} + (V_2 - 2V_t)^2 * (\frac{1}{2}\lambda V_{DD} + \frac{\lambda^2 V_{DD}^2}{4} + \frac{-2\Delta\lambda - \Delta\lambda^2 V_{DD} + \frac{27}{4}\Delta\lambda^3 V_{DD}^2}{2 + \frac{3}{2}\lambda V_{DD}})]}{\frac{4(V_2 - 2V_t)^2}{K(2 + \frac{3}{2}\lambda V_{DD})}(1 + \frac{\lambda^2 V_{DD}^2}{4} + \lambda V_{DD} + \frac{3\Delta\lambda + \frac{7}{2}\Delta\lambda^2 V_{DD} + \Delta\lambda^3 V_{DD}^2}{2 + \frac{3}{2}\lambda V_{DD}})} I_{in}$$

$$+ \frac{(V_2 - 2V_t)^4 * (1 + \lambda V_{DD} + 2\Delta\lambda)}{\frac{4(V_2 - 2V_t)^2}{K(2 + \frac{3}{2}\lambda V_{DD})}(1 + \frac{\lambda^2 V_{DD}^2}{4} + \lambda V_{DD} + \frac{3\Delta\lambda + \frac{7}{2}\Delta\lambda^2 V_{DD} + \Delta\lambda^3 V_{DD}^2}{2 + \frac{3}{2}\lambda V_{DD}})}$$

$$= \frac{(1+\frac{3\lambda V_{DD}}{4})*(1+\frac{4\Delta\lambda}{2+\frac{3}{2}\lambda V_{DD}})*I_{in}^2}{2K(V_2-2V_t)^2*(1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD})}*[1-\frac{(3+\frac{7}{2}\lambda V_{DD}+\lambda^2V_{DD}^2)\Delta\lambda}{(2+\frac{3}{2}\lambda V_{DD})*(1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD})}]$$

$$+\frac{[\frac{2\Delta\lambda}{K}+(V_2-2V_t)^2*(\frac{1}{2}\lambda V_{DD}+\frac{\lambda^2V_{DD}^2}{4}+\frac{-2\Delta\lambda-\Delta\lambda^2V_{DD}+\frac{27}{4}\Delta\lambda^3V_{DD}^2}{2+\frac{3}{2}\lambda V_{DD}})]}{2(V_2-2V_t)^2(1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD}+\frac{3\Delta\lambda+\frac{7}{2}\Delta\lambda^2V_{DD}+\Delta\lambda^3V_{DD}^2}{2+\frac{3}{2}\lambda V_{DD}})}I_{in}$$

$$+\frac{K(V_2-2V_t)^2*(1+\lambda V_{DD}+2\Delta\lambda)*(2+\frac{3}{2}\lambda V_{DD})}{4(1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD}+\frac{3\Delta\lambda+\frac{7}{2}\Delta\lambda^2V_{DD}+\Delta\lambda^3V_{DD}^2}{2+\frac{3}{2}\lambda V_{DD}})}$$

$$= \frac{I_{in}^2}{2K(V_2-2V_t)^2}*[1+\frac{1}{(1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD})}*(\frac{\frac{\Delta\lambda}{2}+\frac{\Delta\lambda^2V_{DD}}{4}}{1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD}}-\frac{\lambda^2V_{DD}^2}{4}-\frac{\lambda V_{DD}}{4})]$$

$$+[\frac{\frac{2\Delta\lambda}{K}+(V_2-2V_t)^2*(\frac{1}{2}\lambda V_{DD}+\frac{\lambda^2V_{DD}^2}{4}+\frac{-2\Delta\lambda-\Delta\lambda^2V_{DD}+\frac{27}{4}\Delta\lambda^3V_{DD}^2}{2+\frac{3}{2}\lambda V_{DD}})}{(1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD})}$$

$$-(V_2-2V_t)^2*\frac{\frac{3\lambda V_{DD}}{2}+\frac{5\lambda^2V_{DD}^2}{2}+\frac{11\lambda^3V_{DD}^3}{8}+\frac{\lambda^4V_{DD}^4}{4}}{(2+\frac{3}{2}\lambda V_{DD})*(1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD})^2}*\Delta\lambda]I_{in}$$

$$+\frac{K(V_2-2V_t)^2*(1+\lambda V_{DD}+2\Delta\lambda)*(2+\frac{3}{2}\lambda V_{DD})}{4(1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD}+\frac{3\Delta\lambda+\frac{7}{2}\Delta\lambda^2V_{DD}+\Delta\lambda^3V_{DD}^2}{2+\frac{3}{2}\lambda V_{DD}})}$$

$$\Rightarrow I_{out} \propto \frac{I_{in}^2}{2K(V_2-2V_t)^2}*\{1-\frac{1}{(1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD})}*[(1+\lambda V_{DD})*\frac{\lambda V_{DD}}{4}]-(\frac{\frac{\Delta\lambda}{2}+\frac{\Delta\lambda^2V_{DD}}{4}}{1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD}})\}$$

$$= \frac{I_{in}^2}{2K(V_2-2V_t)^2}(1-\delta);\ \text{where}\ \delta = \frac{1}{(1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD})}*[(1+\lambda V_{DD})*\frac{\lambda V_{DD}}{4}]-(\frac{\frac{\Delta\lambda}{2}+\frac{\Delta\lambda^2V_{DD}}{4}}{1+\frac{\lambda^2V_{DD}^2}{4}+\lambda V_{DD}})$$

Due to the LC tank of current squaring circuit resonated at 5-GHz, it could be used as a filter to percolate the leakage signal of LO frequency (19-GHz), RF frequency (24-GHz), up-conversion frequency (19-GHz+24-GHz), the double frequency of RF and LO frequency (48-GHz and 38-GHz) and third frequency of RF and LO frequency (72-GHz and 57-GHz).

if $\Delta \to 0$:

$$I_{out} \approx \frac{I_{in}^2}{2K(V_2 - 2V_t)^2} * (1 - \frac{\frac{\lambda^2 V_{DD}^2}{4} + \frac{\lambda V_{DD}}{4}}{1 + \frac{\lambda^2 V_{DD}^2}{4} + \lambda V_{DD}})$$

$$+ \frac{(V_2 - 2V_t)^2 * (\frac{1}{2}\lambda V_{DD} + \frac{\lambda^2 V_{DD}^2}{4})}{2(V_2 - 2V_t)^2 (1 + \frac{\lambda^2 V_{DD}^2}{4} + \lambda V_{DD})} I_{in}$$

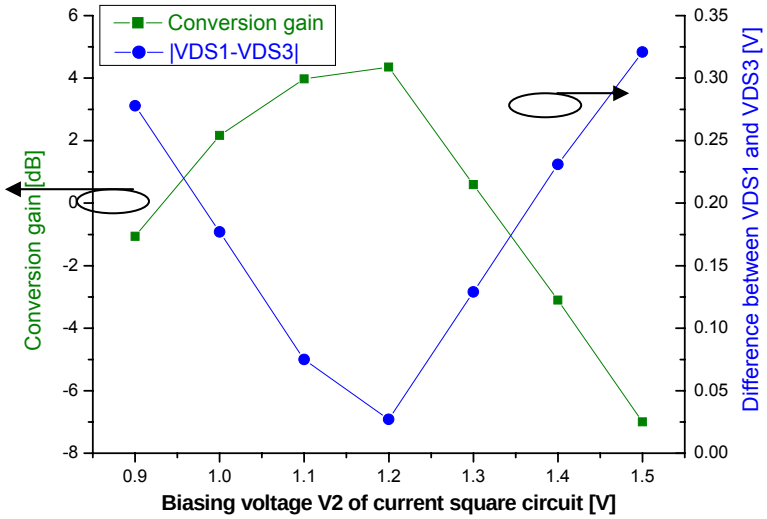
$$+ \frac{K(V_2 - 2V_t)^2 * (1 + \lambda V_{DD}) * (2 + \frac{3}{2}\lambda V_{DD})}{4(1 + \frac{\lambda^2 V_{DD}^2}{4} + \lambda V_{DD})}$$

if $\lambda \to 0$:

$$I_{out} \approx \frac{I_{in}^2}{2K(V_2 - 2V_t)^2} + \frac{K(V_2 - 2V_t)^2 *}{2}$$

Thus, the smaller difference between V_{DS1} and V_{DS3} is the better for the current square operation. The following figure represents the impact of difference V_{DS} voltage. The smaller difference of V_{DS} voltage will have the greater conversion gain of current-mode mixer. Therefore, there are two important issues about the current square circuit. First, the channel length of MOS devices in the current square circuit should be chosen as larger channel length to alleviate the short channel effect. Second, the biasing voltage of current square circuit should be chosen with the smallest difference of V_{DS} between M1 and M3 MOS devices. While the V_2 is equal to

V_{DD}, the voltage of V_{DS1} is very close to V_{DS3}.



The impact of difference of V_{DS} voltage

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