國　立　交　通　大　學

電子工程學系　　電子研究所碩士班

碩　士　論　文

矽鍺奈米線的製作和電性探討

A Fabrication and Electrical Properties Studies of SiGe Nanowire

學生：曾文賢　　Student: Wen-Hsien Tzeng

指導教授：張國明 博士　　Advisor: Dr. Kow-Ming Chang

中華民國九十五年七月

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A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Electronics Engineering

July 2006

Hsinchu, Taiwan, Republic of China

中華民國九十五年七月

矽鍺奈米線的製作和電性探討

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摘要：

近年來，由於元件的微縮，使得 nanowire 和 nanostructure 變得相當的熱門。Nanowire 主要被拿來應用於 biological sensor 或 nanoelectronics，因和傳統元件相比，其具有較快速的元件轉換速度和低功率消耗之優點。Nanowire 的側壁相當的敏感，可用來偵測相當細微的變化。

在這篇研究中，我們引入了 SiGe 的應用，來製作出 SiGe nanowire，利用 Ge 有比較高的 mobility，故將其以不同比例的摻入 Si 中，而所成長出的 SiGe 層，會隨著 Ge 的濃度增加，使我們的元件具有較高的電流傳導力。起先我們先用濕氧化製程長氧化層，再用 TEL 5000 乾式蝕刻機台把氧化層蝕刻成一個個階梯狀。利用 UHV-CVD 機台來成長 SiGe，將其疊在 oxide step 上，再利用 TCP 9400 乾式蝕刻機台把所疊的 SiGe film 蝕刻掉，則 SiGe nanowire 會被精巧的製作在剩餘的 spacer 上。之後欲得到更大的電流，我們再將 Source/Drain 打入離子佈植，由於降低了 Al/SiGe 之間的接觸電阻，使電流加大的提高。之後再整個 nanowire 都打入離子佈植，由於在通道中提供了更多的導通載子，以致於電流更大大的被提升，更加的利於我們日後拿來做為 sensor 方面的應用。

A Fabrication and Electrical Properties Studies of SiGe Nanowire

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Abstract

Due to the scaling down of devices, nanowire and nanostructure attracts many interests recently. Nanowire is mainly used in biological sensor or nanoelectronics, because it has the advantages of faster switching speeds and lower power consumption than conventional devices. The sidewall of nanowire is very sensitive and this could be used to detect the slight variation of the condition.

In this thesis, we involve the application of SiGe to fabricate SiGe nanowire. Ulitize the higher mobility of Ge, and formed different SiGe alloy concentration. The grown SiGe layer will enhance current with the Ge content increases. First, we oxidized the Si bulk by wet oxidation. By lithography, we fabricated each step of the oxide. An then, We deposited SiGe layer on the oxide step by Ultra High Vaccum-Chemical Vapor Deposition (UHV-CVD), and then etched the SiGe film. The SiGe nanowire will elaborately formed in the side-wall spacer. Later we treated the Source/Drain with ion implanation to get the higher current due to the reduction the Al/SiGe contact resistance. The current was more improved by implanted the channel. It favored the application for the nanowire to be a sensor later.

誌　謝

首先，感謝張國明老師這兩年來的指導，使我在研究或做人處世上都獲益良多，並且對我們日常生活也非常的照顧和關心。

其次，感謝實驗室的學長和同學們，當我實驗遇到問題時，總是能給予我適時的幫助和指導，特別要感謝郭俊銘學長，幫我設計了整個實驗的流程與架構，並且從旁參與整個實驗，並適時的提出保貴的經驗指導我。另外要感謝林建宏學長，在實驗的過程中，遇到問題時，能給予意見並提出看法，也因此幫我克服不少問題。

再者，感謝國立交通大學奈米中心和國家奈米元件實驗室（NDL）提供了完整的機台讓我可以順利的完成實驗，

最後，要感謝爸媽不斷的支持與鼓勵，讓我在追求學問的過程中並不孤獨。同時也要感謝女友總是在我背後默默的替我加油和打氣，在我遭遇壓力和困境時陪我解悶讓我開心，給予我新的力量以面臨更大的挑戰！謝謝你們！

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Chapter 1

Introduction

1.1 Revolution of VLSI device technology

From the first used of the VLSI application in the 1980, an excellent amount of evolution of the metal-oxide-semiconductor field effect transistor had been presented. The recent trend was to scale down the transistor and pack them more in the same chip area. Lithography and etching technology was the two most important key issue to decide which limitation of the device could be scale down. The scaling down of the devices, it's advantages are lower power consumption and improving the operating speed, and its could reduce cost and increasing many logic calculating ability. With the fabrication process into nano-structure, many problem like lithography and physical limitation should be worked out. Here we present a fabrication of nanowire with the material of SiGe.

Recently, the band gap enginnering in the SiGe/Si material system has been studied and used for the fabriction of heterojunction bipolar transistors[1][2], superlattice devices[3], modulation field effect devices[4]. In Fig 1.1 shows the energy-band diagram of the Si/SiGe HBT. The improvement in epitaxial technology makes it possible to grown pseudomorphic SiGe layers with good crystallinity and electronic properties on an Si substrate. The SiGe and Si material combination is particularly attractive due to its compatibility with the conventional Si technology. However, in order to use SiGe alloys in Si-based devices, there is plenty of primary importance to study, since the lattice mismatch between the silicon and germanium

is a major step in Si technology. Moreover, since Si structure has been studied for many years, but for SiGe nanostructures, it's quite neonatal. It is physical interest to compare the basic physical phenomena involved in both silicon and SiGe even in the nano-scale dimension.

1.2 The introduction of SiGe

Many groups have show great interest in SiGe for modern device preparation due to the capability of band gap engineering, and the increased mobility of charge carriers by the incorporation of Ge into the Si lattice. SiGe alloy has higher mobility and better electrical properties, compare to bulk Si, which speed is higher than that of Si device with same technology. Higher mobility means that higher driving current could be afforded. Si and Ge have a 4.17 % lattice mismatch (the lattice constant of Si and Ge is 5.43 and 5.66 Å), when SiGe was deposited on Si-based wafer, it would pseudomorphic growth of Si and SiGe layers leads to compressive strain (Shown in Fig.1.2 and 1.3), which modifies the band structure of the SiGe material thus changing electronic transport properties [5][6][8].

Considering the mobility term μ, the carrier mobility is the most important transport parameter of a semiconducting material. It describes the linear relation between an electric field E and the carrier drift velocity Vd, in the limit of low electric and negligible magnetic fields in homogeneous, isothermal semiconductors:

$$Vd = \mu \times E$$

μ is a function of the elctron charge e, the transport effective mass m^* and the transport scattering time τ

$$\mu = \left(\frac{e}{m^*} \right) \times \tau_t$$

τ_t, and thus μ is a fundamental material parameter that represents all scattering mechanisms a carrier experiences when moving through a semiconductor in the presence of an electric field. Within the limits of the wave-vector-independent relaxation time approximation $1/\tau_t$ is the sum of all reciprocal scattering times associated with the respective scattering mechanism [7].

$$\frac{1}{\tau_t} = \sum_i \frac{1}{\tau_i}$$

The SiGe/Si heterojunction has much to be investigated, like strained-Si, compressively-strained-SiGe. Use the Vegard's rule, we can calculate the lattice constant of SiGe alloy

$$a_{Si_{1-x}Ge_x} = a_{Si} + x(a_{Ge} - a_{Si})$$

In Table 1, we can know the basic properties of Si and Ge. The Ge mobility is higher than Si in electron and hole and this is due to the Ge has lower effective mass (Both in electron and hole). The electron mobility of Si and Ge is 1500 and 3900 $cm^2/V \cdot s$. Due to the idea, we can fabricate devices with $Si_{1-x}Ge_x$ material, which x is the proportion of the Ge concentration. With the Ge content x increases, the mobility will increase, and the current will also be increased[9][10]. Fig 1.6 show the effective carrier mobility in the $Si_{0.17}Ge_{0.83}$ channel p MOSFET and in conventional Si n and p MOSFETs as a function of the vertical electric field at room temperature. It is apparent that the current was improved than the conventional one. The band alignment of pseudomorphic $Si/Si_{1-x}Ge_x$ was recently clearly identified. The second way to more improve the current was using Strained-SiGe or Strained-Si. With the main band offset in the valence band (VB) and only a very small offset of about 10 meV in the conduction band (CB) as schematically illustrated on the Fig 1.4. Compressive in-plane strain in SiGe lifts degeneracy and splits the VB into heavy

hole (hh) and light hole (lh) states with the hh defining the VB maxima. This was shown in Fig 1.5. The mechanism of the strained-Si is the six-fold degenerate CB split into $\Delta(2)$ and $\Delta(4)$valleys with the $\Delta(4)$ states being the CB minima. More electron state in the energy state of the $\Delta(2)$ and the $\Delta(2)$ valley have lower effective mass (Shown in Fig 1.7). So the current will be increased. When the Si layer which is grown on the relaxed SiGe uniform layer, is supposed to be completely strained if it is below the equilibrium critical thickness[11][12][13]. However, we find that in the presence of ~10^5 /cm^2 threading dislocations, strained Si layers start to partially relax even when the layer thickness is well below the predicted critical thickness (Shown in Fig 1.8). Device processing subjects the strained Si layer to temperatures beyond the growth temperature for varying time periods which can relax some of the strain. Strain relaxation is also accompanied by the formation of misfit and threading dislocations which can increase leakage currents, and reduce carrier mobility by scattering. Some groups experiment that grow relaxed graded SiGe buffer layers in order to prevent the strain relaxation [14][15]. But the strained-Si devices can enhance the electron mobility[16], but hole mobility is similar to control Si at the high field [17]. Furthermore, strained-Si suffers from the threading defect density and high cost.

Knowing the correlationship between Ge concentration and device performance, the control of Ge concentration will be a capital issue.

1.3 The introduction of nanowire

1.3.1 The application of nanowire

Silicon-based nanostructured materials are highly attractive due to their unique semiconducting, electronics, mechanical, optical properties, biochemistry and their

compatibility with conventional Si technology. Due to their large specific surface area and high surface free energy, nanostructured materials can be used in the detection of biomolecules[18]. The surface properties become important because of the large surface-to-volume ratio, which makes them specially appealing for use as chemical and biomedical sensor. It was shown in Fig 1.9.

Silicon nanowire (SiNWs) show quantum effects, a large piezoresistance coefficient, and a diameter-dependent thermal conductivity. SiNWs are semiconducting, and their dopant type and concentration can be controlled. Moreover, it is possible to exploit the vast knowledge of the chemical modification of oxide surfaces to realize semiconductor nanowires modified with receptors for many applications.

Many groups have demonstrated nanosensors based on Si nanowires. There are many ways to fabricate a nanowire listed following.

1.3.2 The ways to fabricate nanowires

(a) Scanning Probe Lithography

Scanning probe devices were first developed by Binnig et al. in 1982 [19] and since that time have been used primarily as tools for obtaining topographical and electronic surface maps. They can also be used to directly modify the chemical or physical structure of surface [20][21][22]. The ability to organize matter on the nanometer scale is one of the major enabling principles in the field of nanotechnology. Scanning probe lithography (SPL) has been a key tool in achieving this goal.

It is natural to marry the nano-scale visualization and manipulation capabilities of SPM/SPL with the chemical definition and opportunities for creating patterns afforded by SAMs. This combination is the subject of this review. From a

fundamental manufacturing standpoint, simultaneous utilization of these two elements can also be considered as a hybridization of top-down (SPL) and bottom-up (self-assembly) approaches[23]. As there are no general paradigms for the artificial construction of arbitrary objects exclusively via self-assembled structures has enabled their use in nanosynthesis. Fig 1.10 shows the schematic of fabrication using SPL technique.

(b) Vapor-Liquid-Solid (VLS)

Research in the past few years, most of the silicon nanowire was fabricated by Vapor-liquid-solid technology[24][25][26]. In the VLS technique, a gold thin film or particle is used to catalyze the decomposition of a gas source (SiH_4) at elevated temperature. Silicon diffuses into the gold, forming a liquid Au-Si alloy, provided that the growth temperature is greater than the eutectic temperature of the alloy. (~363 ℃ for Au-Si). Upon supersaturation, a single crystal silicon nanowire is precipitated from the liquid and grows in length. Since the diameters of the nanowires are determined by the size of the metal particles, gold particles with nanometer dimensions are required in order to fabricate nanowires [27].

(c) Laser Ablation

A method combining laser ablation cluster formation and VLS growth was developed for the synthesis of semiconductor nanowires [28]. In this process, laser ablation was used to prepare nanometer diameter catalyst clusters that define the size of wires produced by VLS growth. This approach was used to prepare bulk quantities of uniform single-crystal Si and Ge nanowires with diameters of 6 to 20 and 3 to 9 nm, respectively, and lengths ranging from 1 to 30 micrometers. The schematics are shown in Fig 1.11. In the Laser ablation technique, (1) Laser ablation with photons of

energy h ν of the SiFe target creates a dense, hot vapor of Si and Fe species. (2) The hot vapor condenses into small clusters as the Si and Fe species cool through collisions with the buffer gas. The furnace temperature is controlled to maintain the Si-Fe nanocluster in a liquid state. (3) Nanowire growth begins after the liquid becomes supersaturated in Si and continues as long as the Si-Fe nanoclusters remain in a liquid state and Si reactant is available. (d) Growth terminates when the nanowire passes out of the hot reaction zone onto the cold finger and the Si-Fe nanoclusters solidify.

(d) Electron Beam Lithography

Electronic is a very small particles, and it can be seen as a wave. The wavelength of electron depends on its momentum and energy-related. The higher the energy of the electron is, the shorter the wavelength be. An electron beam with high energy even shorter than the wavelength of the ultraviolet, thus the electron beam lithography has higher spatial resolution and a wider process range than optical lithography. The Electron beam lithography technology has been widely used for the semiconductor factories to fabricate masks.

The designed pattern was stored in the computer initially. Electron beam lithography technology uses very thin scanning beams reading from the computer to directly write to the design of electronic photosensitive material. The energy stored in the electron will alter the solubility of the photoresist after the electron beam scanning. For the positive PR, it would become soluble. Owing to the consecutive series of moves of the electron beam system, the efficiency is too low for the electron beam directly writing in the semiconductor wafer production. So it becomes economically feasible in the large-scale production.

(e) Solid-Liquid-Solid

The SLS growth process has been previously demonstrated for group Ⅲ element phosphides and arsenides, which are thermally stable at conventional growth temperatures. However, indium nitride is not. The SSLS mechanism operates at very low temperatures in comparison to conventional materials-synthesis methods, presumably because it is catalytic and lowers energy barriers for both precursor decomposition and the interfacial steps required for nonmolecular crystal growth. The crystal lattice is assemble. SLS synthesis of other thermally unstable compounds and crystal structures should be possible [29]~[31]. The VLS and SLS grown mechanisms was explained in Fig 1.12.

(f) Atomic Force Microscope (AFM)

The atomic force microscope shown in Fig 1.13 is a sensitive profilometer that maintains a constant contact force with a surface, not necessarily conducting. The tip is located at the end of a cantilever, and the constant force is maintained by optically detecting the cantilever's deflection as the sample is scanned. Metallizing the tip allows a current and electric field to be applied to the region of contact [32].

1.4 Electrical properties of SiGe nanowire

There are several kinds electric properties of nanowires. Here we will demonstrate them together to help us understanding the properties.

Contact is a key issue in studying the electrical properties of semiconductor nanotubes (NTs) and nanowires (NWs). In many experiments, a Schottky barrier is

believed to exist at the contact [33][34][35][36]. The electrode metal plays an important role in device performance[35]. To study the intrinsic properties of nanowires, ohmic contacts are necessary. Whether a contact is a Schottky or ohmic depends on the work-function (ϕ) difference between the electrode and the semiconducting NW, and also on the type of majority carriers (electrons or holes). For a p-type semiconductor, if the work function of the metal (ϕ_M) used for contact is smaller than that of the semiconductor (ϕ p), a Schottky barrier will be formed; otherwise, if $\phi_M > \phi$ p, an ohmic contact will be formed. The diagrams of the Schottky barrier and Ohmic contact is shown in Fig 1.14

Another testing way was shown here. As known, the scanning probe microscope (SPM) has high spatial resolution, and can be used to probe the local electronic properties of materials shown in Fig 1.15. Therefore, the combination of the SPM technique and the current transport study could assist in characterizing the nanostructures microscopically. Z. Fan et al. [37] had shown that using the scanning surface potential microscopy (SSPM) to analyzed the potential drop at Schottky barrier contact and contact resistances. The schematic of scanning tip gating applied a negatively biased conductive tip is scanning the nanowire is shown in Fig 1.16. The Operation principles are using the conductive SPM tip as a movable local gate and a comparison between tip gating effect and back gating effect is made. It is found that local gating can modify the effective Schottky barrier heights when applied at the contact region. A negative tip bias results in a local potential barrier which obstructs the elctron transport when applied in the middle of the nanowire. So, a scanning tip gating effect is demonstrated in which the conductance of the nanowire is modulated periodically by the negatively biased scanning tip.

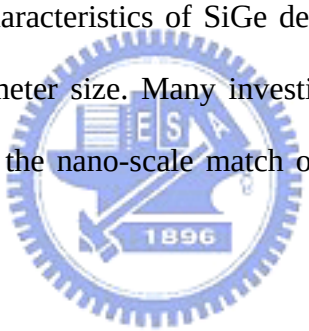
There are two important features of nanostructures. Firstly, size can be used as a variable to modulate the structure and properties. Secondly, due to the small size, quantum effects are dominant, and therefore quantum mechanical methods should be used to elucidate their behaviours and properties. At low temperature measurement, some quantum effects might be observed such as Coulomb Blockade or Coulomb Oscillation.

Chapter 2

Experiment

2.1 Motivation

An easy process to fabricate a nanostructure with high-yield and low-cost is the main issue to be concerned. The fabrication only using the combination of the conventional lithography and process technology was demonstrated without using EBL, SPL, VLS, etc. in the thesis. Use the side wall spacer technology on our experiment, only by etching the film then nanowires would be formed. This method was shown is Fig 2.1. The characteristics of SiGe device in the large size was well known, but not for the nanometer size. Many investigations still have to do to see whether the characteristics of the nano-scale match or not. So its our motivation to design the fabrication process.



2.2 Detail experiments

In the thesis, we will introduce our new fabrication technique of the SiGe Nanowire. The processes used sidewall spacer technique to fabricate the SiGe nanowires on Si wafer.

A p-type (100)-oriented bare silicon wafer. The resistivity of the silicon substrate is about 1-10 Ω-cm.

1. Zero layer formation – Zero mask dry etch to form the alignment mark.
2. Standard RCA cleaning, 980 ℃Wet Oxidation for 1 hr to grow the bottom oxide

as a gate oxide by *ASM/LB45 Furnace system*. The thickness of the oxide is 2000 ~3000 Å. It was shown in Fig 2.2.

3. Mask #01 : Define the AA region, we etch the oxide film to form each step by *TEL oxide etcher – TEL 5000*. It was shown in Fig 2.3. In mask #01, the residue thickness of the oxide is around 300~500 Å and this should be precisely controlled (In Fig.2.3) . If the oxide left too thick, the control ability of the oxide would become weak. On the contrary, if the oxide left too thin, the leakage will become serious and the breakdown voltage will be decreased. Thus we use the *P-10 surface profiler* to check whether if the step is the height we want or not. We controlled the height is about 400 Å.
4. Standard RCA cleaning. Before we deposited the SiGe film, we deposited amorphous Si film first by *ASM/LB45 Furnace system*. It was shown in Fig 2.4. This purpose is due to SiGe and SiO_2 has a had adhesion. The grown condition of the amorphous Si is 620 ℃ and the preasure is controlled at 160 mTorr, and its thickness is 150 Å.
5. We treated the wafers for standard RCA cleaning again after the amorphous Si deposition because of the better uniformity compared to the without cleaning one. The SiGe film is deposited with the ultra-high-vaccum chemical vapor deposition (*ANELAVA SiGe UHV-CVD*). The structure was shown in Fig 2.5. The condition of the SiGe film is epitaxially grown at 550 ℃. After deposition, we measure the testing wafer by *N&K Analyzer 1280* to confirm the SiGe thickness and how much the thickness should we etch. The SiGe thickness is about 800 Å.
6. Mask #02 : Defined the S/D region. Etching the whole height of the amorphous Si and SiGe film by *TCP poly etcher – TCP 9400 SE*. Only the S/D and SiGe deposited in the sidewall spacer will be stayed. And the residue SiGe film is what we want – SiGe nanowire. It enclose the step height circularly. The structure is

shown in Fig 2.6. The height of the oxide step was measured by *P-10 surface profiler*.

7. Mask #03 : Etching each pair of the parallel SiGe nanowire to form only a parallel SiGe nanowire by *TCP poly etcher – TCP 9400 SE*. The structure is shown in Fig 2.7.
8. Mask #04 : The mask is used for the Gate contact hole exposure. And etching the oxide in the Gate by BOE solution. The thickness of the oxide is 2000 Å and 3000 Å etched by BOE solution for 50 sec respectively. Later, we diped HF solution for removing the oxide on the Source/Drain before thermal coating to get ohmit contact. The figure was shown in Fig 2.8.
9. Thermal coating the aluminum as contact electrode for the thickness of 5000 Å at 30~40 ℃. This was shown in Fig 2.9.
10. Mask #05 : Aluminum contact pad were then defined by wet etching (HNO_3:CH_3COOH:H_3PO_4:H_2O=2:9:50:10)
11. Sintering at T=430 ℃ for 30 min. The schematics was shown in Fig 2.10.

2.3 The variance of the process flow

The process flow above was the initial, and we will insert some process after the Mask #03 to experiment a series condition. The condition of the ion implantation in our experiments was energy E=15 KeV and dose D=5E15.

(1) The First : The above process flow.

(2) The Second : After Mask #03, we add one Mask #PR. We use PR as hard mask to stop the Gate and channel being ion implanted. The ion implantation was operated with the *Implantation E500HP* . After strip the PR, we treated

the device with thermal annealing at T=950 ℃ for 30 sec for good ohmic contact.

(3) The Third : After Mask #03, we treated the device with ion implantation and then thermal annealing at T=950 ℃ for 30 sec for activate the dopants. Source/Drain and channel were all be implanted.

2.4 Test structure

The test structure we design was used to make sure that the SiGe and Al film was etched completely in the isolation area. The test structure is shown in Fig 2.11. A series test block was used to calculate the contact resistance between the Al electrode and SiGe or Poly-Si film. Fig 2.12 shows the contact resistance test structure. The two test structure was experimented with the process flow. So all the process condition was the same with the devices.

Chapter 3

Results & Discussion

We have successfully fabricated the SiGe nanowire structure on the Si wafer, and measured the electric characteristics.

3.1 SiGe Nanowire Fabrication

We use the side wall spacer technique to fabricate our SiGe nanowires. As we known, the diameter of the nanowire would influence the current, so the control of the nanowire would become a key issue. The most important is the diameter of the nanowire. This was controlled by the Mask #02 when we etched the SiGe film by *TCP poly etcher – TCP 9400 SE*. The surface of the nanowire is quite sensitive so that it's easy influenced by any variances.

3.1.1 $Si_{0.93}Ge_{0.07}$ Nanowire

Electrical-transport measurements were conducted using an *Agilent 4156C semiconductor parametric analyzer*. We sweep the Id-Vd figure from –5 V to 5 V, and change the Vg step from –10 to 10 V. Fig 3.1, 3.2 show the Id-Vd figure of the $Si_{0.93}Ge_{0.07}$ nanowire. The Fig 3.1 is length L=15 μm and the Fig 3.2 is L=50 μm. For comparision, we fabricated the Poly-Si nanowire and the same way to measured. Fig 3.3, 3.4 show the Id-Vd figure of the Poly-Si nanowire. Clearly, higher currents were obtained at negative gate voltages, demonstrating that the SiGe nanowire is a p-type semiconductor. The figure of the Id-Vd is somewhat nonlinear, which indicates nonideal contact between the electrodes and nanowire. The contact problem we will discuss later. The Fig 3.3 is length L=5 μm and the Fig 3.4 is L=15 μm. We directly compared the four figures, it seems that the current of the Poly-Si nanowire would be

larger than $Si_{0.93}Ge_{0.07}$ nanowire. But as we known, there is still some reason will affect the drive current including the diameter of the nanowire, wire length, the dopant condition, heat treatment, and the electrode contact, etc. So, if we want to compare the two structures, we should normalize them. The equation about current I is

$$V = I \times R = I \times \rho \times \left(\frac{L}{A} \right)$$

ρ is the resistivity. We fix the voltage at Vd=5 V and Vg= -10 V to be constant. Rewrite the equation, the σ is

$$\rho = \frac{(A \times V)}{(I \times L)}$$

$$\sigma = I \times \frac{L}{(V \times A)}$$

σ is the conductivity (Ampere per unit length) term and this is proportional to the current I and device length L. The area of the nanowire we could observe from the *TFSEM*. The *JOEL JSM 6500-F – TFSEM* was the equipment we used to measure the diameter of the nanowires. Figure 3.5 (a)(b) show the top view SEM picture and Figure 3.6 (a)(b) show the cross-section view SEM picture. There was fluctuation in each width and height which was controlled by the *TCP dry etcher*. The fluctuation must be decreased because the diameter of the nanowire is directly related to the current. Table 3 (a)(b) show the distogram of the (a)Poly-Si, (b)$Si_{0.93}Ge_{0.07}$ show the distribution of the nanowire width. The average of the $Si_{0.93}Ge_{0.07}$ nanowire is 147.6 nm in height and 76 nm in the half width, we thought that the nanowire was a triangle column shape, so the average area is about 11218 nm^2. The $Si_{0.93}Ge_{0.07}$ nanowire at Vd=5 V and Vg= -10 V the current I=1.76 nA for L=15 μm and I=0.5 nA for L=50 μm. By calculation, the $Si_{0.93}Ge_{0.07}$ nanowire current per unit length is I=0.01773 A/V‧cm for L=15 μm and I=0.01872 A/V‧cm for L=50 μm. For the Poly-Si nanowire, figure 3.7 (a)(b) show the *TFSEM* top view and figure 3.8 (a)(b) show the *TFSEM* cross-section view. The average of the Poly-Si nanowire is 178.8 nm in height and 77.4 nm in the half width, so the average area is about 13839 nm^2. At Vd = 5 V and Vg= -10 V the current I=2.27 nA for L=5 μm and I=1.22 nA for L=15 μm. By normalizing, the Poly-Si current per unit length is I=0.01147 A/V‧cm for L=5 μm and

I=0.01312 A/V・cm for L=15 μm. After normalizing, we could observe that $Si_{0.93}Ge_{0.07}$ nanowire has higher current than Poly-Si nanowire. This matches the theoretical deduction. All the data were summary on the Table 2.

3.1.2 SiGe nanowire with higher Ge concentration (11% and 20%)

In the last paragraph, we observe the SiGe nanowire has higher mobility than Poly-Si one. Subsequently, we try the Ge 11 % and 20 % to see if there will be higher current. Fig 3.9, 3.10 show the Id-Vd figure of the $Si_{0.89}Ge_{0.11}$ nanowire and Fig 3.11, 3.12 show the Id-Vd figure of $Si_{0.8}Ge_{0.2}$ nanowire. And Fig 3.13 (a)(b) show the SEM top view and (c)(d) cross-section view of the $Si_{0.89}Ge_{0.11}$. Fig 3.14 show the $Si_{0.8}Ge_{0.2}$ one. For $Si_{0.89}Ge_{0.11}$ nanowire *TFSEM* figure (shown in fig 3.13), it is obvious that the SiGe nanowire was over-etched. The height of the nanowire was lower than the oxide step height and the nanowire is nearly run out of. From SEM figure, we could read out the average of the $Si_{0.89}Ge_{0.11}$ nanowire is 85 nm in height and 43 nm in the half width, so the average area is about 3528 nm^2. The $Si_{0.89}Ge_{0.11}$ nanowire measured at Vd=5 V and Vg= -10 V the current I=1.36 nA for L=15 μm and I=0.855 nA for L=30 μm. By calculation, the $Si_{0.89}Ge_{0.11}$ nanowire I=0. 1178 A/V・cm for L=15 μm and I=0.1168 A/V・cm for L=30 μm. The results match our deduction for the higher Ge concentration in SiGe the higher current will be for the nanowire structure. The current by normalizing was larger than the $Si_{0.93}Ge_{0.07}$ and Poly-Si nanowires. The Id in the fig 3.15 and 3.16 were normalized at any drain voltage (but fixed Vg = -10 V) that it's apparent that the $Si_{0.89}Ge_{0.11}$ nanowire has higher current than Poly-Si. But for the $Si_{0.8}Ge_{0.2}$ nanowire, it is evident that the SiGe nanowire was over-etched (Shown in fig 3.14) and there is no nanowire residue in the sidewall spacer. So we could find that the current is much smaller than the 7 % and 11 % of the Ge contents. It's hard to know that how much the nanowire would be for us to calculate the current per unit length. The problem was came out that we etch the SiGe film in Mask #02 for too much time. The time of etching 20 % SiGe should be shorter and 17 sec etching was

too long. This was shown in SEM figure in Fig 3.14. All data of the nanowires we measured were listed in Table 1. Table 2. summary the data above we calculated from the equation $\sigma = (I \cdot L) / (V \cdot A)$. The current per unit length was normalized so that we could compare directly. Table 3. compare all the width fluctuation of each nanowire. It shows the Gaussian distribution profile. Though there exists some fluctuation in calculating the conducting area of the nanowire, but the fluctuation is small. For Poly-Si, the average width is 78.9 nm and the fluctuation is 2.631 nm. The variance is only 3.33 %. For Ge 7 %, the average width is 79.5 nm and the fluctuation is 2.78 nm. The variance is only 3.5 %. For Ge 11 %, the average width is 50.1 nm and the fluctuation is 4.96 nm. The variance is 9.9 %. The Ge 11 % fluctuation is higher might due to the nonuniform Ge distribution.

3.2 Thermal annealing

From the paper proposed by Yi Cui. etc., they presented that the relatively low transconductance and carrier mobility were partly due to poor contacts between the SiNWs and source-drain electrodes and are not intrinsic to the single-crystal NW building blocks [38]. By thermal annealing and passivation of oxide defects by chemical modification were found to increase the average transconductance. Due to this idea, we treat our experiment with thermal annealing before etching gate of the Mask #04. The condition we choose is T=950 ℃ for 30 min. For $Si_{0.93}Ge_{0.07}$, $Si_{0.89}Ge_{0.11}$ nanowire and Poly-Si nanowire at the same measurement condition that the current I=0.283 μA for L=20 μm for $Si_{0.93}Ge_{0.07}$, I=0.103 μA for L=20 μm for $Si_{0.89}Ge_{0.11}$ and I=0.107 μA for L=13 μm for Poly-Si nanowire. Fig 3.17, 3.18, 3.19 show the Id-Vd diagram of the $Si_{0.93}Ge_{0.07}$, $Si_{0.89}Ge_{0.11}$ and Poly-Si nanowire respectively after thermal annealing. We think that the area of the nanowire is still the same and not be oxidized during thermal annealing. By calculation, the currenet per unit length is I=0.814 A/V‧cm for $Si_{0.93}Ge_{0.07}$, I=2.845 A/V‧cm for $Si_{0.89}Ge_{0.11}$ and the normalizing of the Poly-Si nanowire is I=0.4 A/V‧cm. The current is greatly improved by thermal annealing. The SiGe have higher current than Poly-Si even after thermal

annealing. This is truly that the more Ge concentration, the more driving current will get. We did not experiment the heat treatment of the $Si_{0.8}Ge_{0.2}$ nanowire because there was no nanowire residue on the sidewall spacer. Fig 3.20 (a) and 3.20 (b) show the Source/Drain leakage current of the $Si_{0.89}Ge_{0.11}$ and Poly-Si nanowire. The low leakage current is acceptable for our device.

3.3 Ion Implantation

As we all know, the conductivity of all the devices can be improved by ion implantation because it could supply more carriers in the channeal [30][31]. So, we also experiment a series of the research incorporation to the ion implantation. The condition of the ion implantation was the same for the following two experiments which the energy E=15 KeV and the dose D=5E15. After ion implantation, we all treat the device for thermal annealing to active the dopants. The temperature of thermal anneal was set at T=950 ℃ for 30 min. It was the same with the previous experiment for the comparison.

3.3.1 Only Source/Drain Ion Implantation

It add one lithography process of the Mask #PR to block the channel being implanted. We use Photo Resist (PR) for hard mask. After implantation, the other processes were all the same with the previous experiment. Fig 3.21, 3.24, 3.27 and 3.22, 3.25, 3.28 show the Id-Vd of the $Si_{0.89}Ge_{0.11}$ and Poly-Si nanowire for the same length respectively. Using the previous way, the current I=2.63 μA in L=4 μm, I=2.35 μA in L=5 μm, and I=2.12 μA in L=6 μm for $Si_{0.89}Ge_{0.11}$ nanowire and I=1.47 μA in

L=5 μm, I=1.57 μA in L=5 μm, I=1.77 μA in L=6 μm, By calculation, the current of the $Si_{0.89}Ge_{0.11}$ nanowire is I=7.256 A/V・cm, 7.201 A/V・cm, 6.732 A/V・cm and the current of the Poly-Si nanowire is I=0.915 A/V・cm, 0.918 A/V・cm, 0.962 A/V・cm. It was evident that the current after normalizing is higher than the without any treatment respectively. Fig 3.23, 3.26 and 3.29 show the normalized Id-Vd at Vg= -10 V. It's clear that the SiGe nanowire has higher current than Poly-Si one. And the current is larger than previous one due to the contact resistance is reduced by the S/D ion implantation. In fig 3.26 and 3.29 show a little zero current at Vd=-1~1 V and this is because there is still Schottky barrier between the Al/SiGe contact. Table 4. summary the current after S/D ion implantation then anneal at T=950 ℃ for 30 min. Each term of the current was improved by the process due to reduce the contact resistance.

3.3.2 S/D and Channel Ion Implantation

The process of ion implantation was done after the Source/Drain of the SiGe were formed in the Mask #03. There was no sacrificial layer grown on the SiGe channel before being ion implantation. The other processes were all the same with the previous experiment. Fig 3.30, 3.33, 3.36, 3.39 show the Id-Vd of the $Si_{0.89}Ge_{0.11}$ nanowires and Fig 3.31, 3.34, 3.37, 3.40 show the Id-Vd of the Poly-Si nanowires. It is obvious that the current of the Poly-Si nanowire is larger than $Si_{0.89}Ge_{0.11}$ ones. So we should normalize the current to compare them. Fig 3.32, 3.35 show two normalized Id-Vd diagram fixed at Vg = -10 V. It was clear that the $Si_{0.89}Ge_{0.11}$ has higher current than Poly-Si at any drain voltages.

The current is much improved in SiGe nanowire. In 3.38 and 3.41, we show both the Vg = 10 V and –10 V at the same time. The $Si_{0.89}Ge_{0.11}$ has higher current than

Poly-Si both at Vg=10 V and –10 V at any drain voltages. The SiGe nanowire is tend to p-type, so the more negative bias we supply, the more larger current we'll get. As we known, the nanowire used as a sensor by dip specific PH solution as the applied gate voltage. For a fixed Vd, the variance range of SiGe current is more widespread from Vg=10 V to –10 V than Poly-Si and this means that the SiGe nanowire is more sensitive than Poly-Si. Fig 3.42, 3.43 show the Id-Vd of the $Si_{0.89}Ge_{0.11}$ and Poly-Si nanowires we measured from –1 V to 1 V with the different Vg change from –20 V to 20 V. It shows the very sensitive properties of the nanowires, and the SiGe nanowire is more sensitive than Poly-Si nanowire.

If we assume that the area of the nanowire are the same with the present values, we will get the current per unit length of the $Si_{0.89}Ge_{0.11}$ nanowire is I=99.1 A/V・cm, 104.59 A/V・cm, 106.8 A/V・cm, and 103.17 A/V・cm and the current of the Poly-Si nanowire is I=63.3 A/V・cm, 71.54 A/V・cm, 73.27 A/V・cm, and 64.96 A/V・cm. Both the SiGe and Poly-Si were improved, but it was obvious that the improvement of the SiGe is lower than Poly-Si one. Table 5. summary the current after S/D and channel ion implantation then anneal at T=950 ℃ for 30 min. Each term of the current was improved by the process. Table 6. list all the average current per unit length we normalized, and table 7 show the comparison of the SiGe and Poly-Si nanowire. The SiGe/Poly-Si ratio is 9.537 in the initial, and is reduced to 7.578 after S/D implantation and 1.515 after S/D, channel implantation. The improvement properties of the $Si_{0.89}Ge_{0.11}$ is getting lower. What is wrong ?

3.4 Discussion

After Source/Drain and Channel being ion implantation, both the current of the $Si_{0.89}Ge_{0.11}$ and Poly-Si nanowires were both improved. But the improvement of $Si_{0.89}Ge_{0.11}$ is lower than Poly-Si. It might divide into two parts to be discussed: (1)

Contact Resistance, (2) Implant Doses.

(1) Contact Resistance :

Fig 3.44 and 3.45 show contact resistance-length figure of the $Si_{0.89}Ge_{0.11}$ and Poly-Si nanowires after S/D implantation. We could read out the contact resistance is R=71.57 Ω for $Si_{0.89}Ge_{0.11}$ and R=31.702 Ω for Poly-Si. The contact resistace of the $Si_{0.89}Ge_{0.11}$ is twice larger than the Poly-Si. This might be due to the Al electrode contact pad does not form good ohmic contact with SiGe film. Choose a comportable metal electrode as contact pad such as or TiN/W for the SiGe film could be tried. Dawei Wang, etc. have experimented that the Ni forms good ohmic contact for the boron nanowires [38]. The contact electrode for the $Si_{0.89}Ge_{0.11}$ might not be the optimum.

(2) Implant Doses

The reduction of the improvement of the SiGe nanowire in our S/D, channel implantation experiment is more serious. The most possible reason might due to the Boron doses in the channel are too much. The nanowire after the channel implantation is almost a boron conducting wire. In the Yi Cui, etc. show it is possible to incorporate high dopant concentrations in the nanowire and to approach the metallic regime [39]. They fabricated the Si nanowire with the SiH_4:B_2H_6 ratios of 1000:1 and 2:1, respectively. Fig 3.46 show the I-V curves of the metallic properties of different nanowire diameters. There are too many dopants in the channel that the improvement by SiGe would be vague.

Chapter 4

Conclusion

In our thesis, We have successfully fabricated the SiGe nanowire on silicon wafer with the conventional lithography process. The electrical properties were measured by 4156C and the structure of the SiGe nanowire on the sidewall spacer were observed by SEM.

The sensitivity is the most important key issue for the nanowire as a sensor, and the higher conductance means that the nanowire is more sensitive. We have improved the current by using SiGe material. With the Ge concentration increases, the current will increase, too. After Source/Drain ion implantation, we can get the higher current due to reduce the contact resistance. When the channel was implanted, the current becomes larger than without any treatment.

The improvement of the SiGe nanowire was lower than Poly-Si after implantation. We have proved that the contact resistance in Al/SiGe is higher than Al/Poly-Si nanowire. In the channel implantation, the reduction of the improvement of SiGe might due to the too higher Boron doses we implanted and then conducting properties was dominated by boron.

Chapter 5

Future Work

The higher Ge concentration of the SiGe, the higher current we might get. So more higher Ge concentration about 30 %, 40 %, 50 % can be try later to find the optimum of the Ge concentration for the device.

Increase the Ge concentration by oxidation may be a feasible way. The Ge segregation would happen when the SiGe film be oxidized. This could lead to higher Ge concentration in the SiGe film.

Metal electrode is also an important issue to be discussed. Another metal contact pad like TiN/W might be tried.

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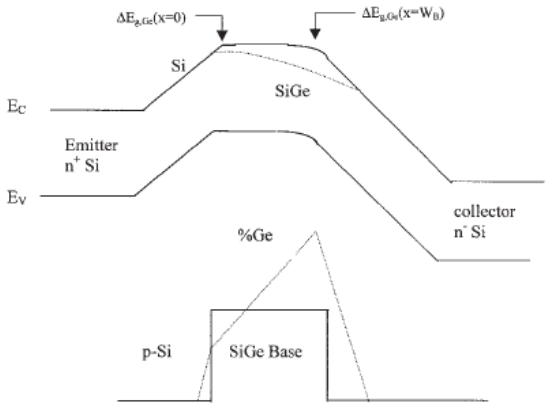


Fig 1.1 Energy-band diagram of the Si/SiGe HBT

	Si	Ge
a_0 (Å)	5.43	5.66
E_g (eV)	1.12	0.66
m^*_e	0.33	0.22
m^*_h	0.55	0.29
μ^*_e ($cm^2V^{-1}s^{-1}$)	1500	3900
μ^*_h ($cm^2V^{-1}s^{-1}$)	450	1900
ε_r	11.7	16.2
Melting point (°C)	1415	937

Transport properties of bulk Si and Ge at 300K

Table 1. Basic Properties of Si and Ge

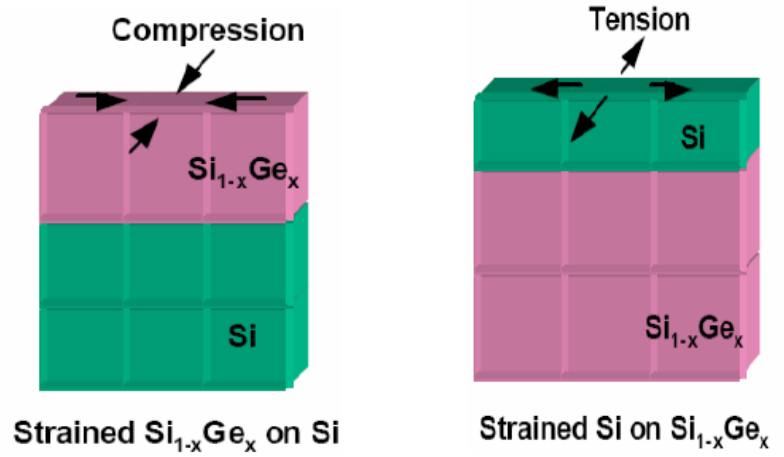


Fig 1.2 The different kinds of strain shown in the diagram

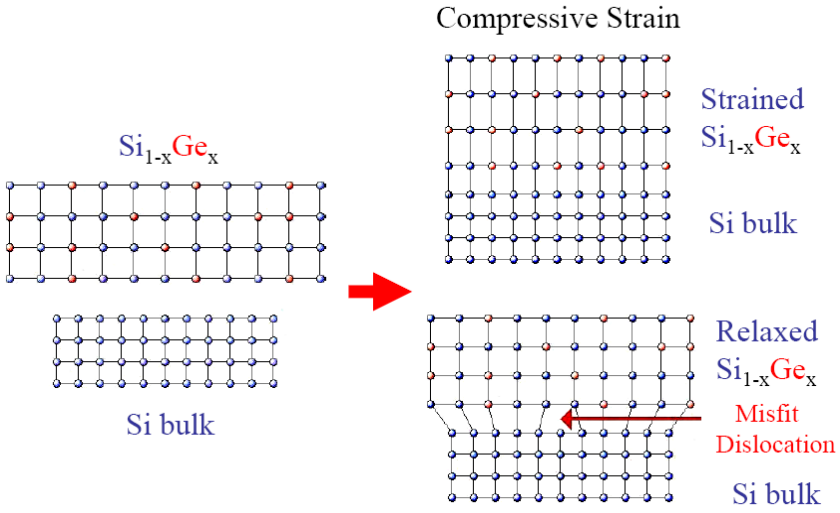


Fig 1.3 $Si_{1-x}Ge_x$ is epitaxially grown on the Si bulk to form the $Si_{1-x}Ge_x$/Si heterojunction.

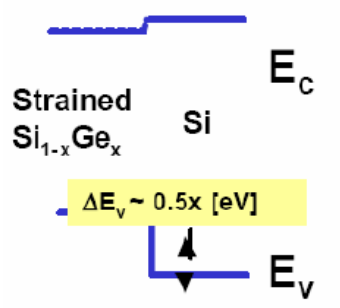


Fig 1.4 The band offset of the valance band and conduction band was schematically illustrated

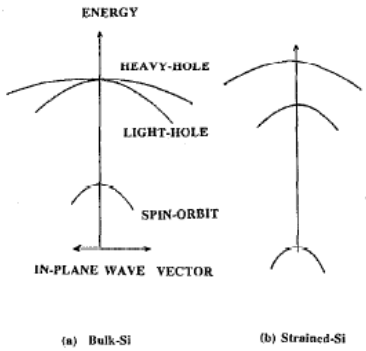


Fig 1.5 The Compressive in-plane strain in SiGe lifts degeneracy and splits the VB into heavy hole (hh) and light hole (lh) states with the hh defining the VB maxima.

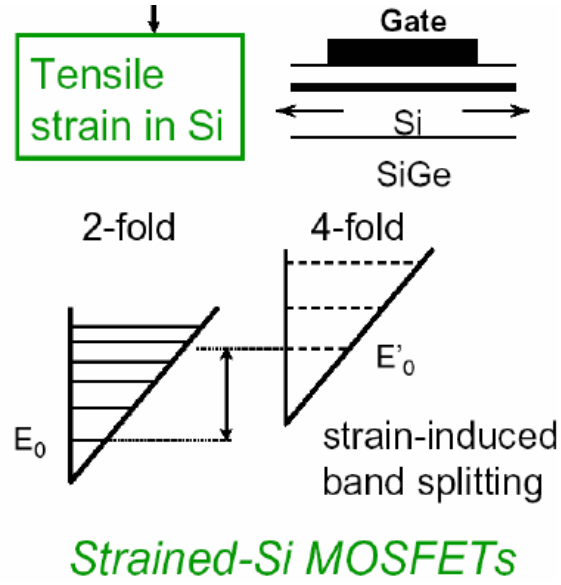


Fig 1.6 The mechanism of the Strained-Si on relaxed SiGe layer.

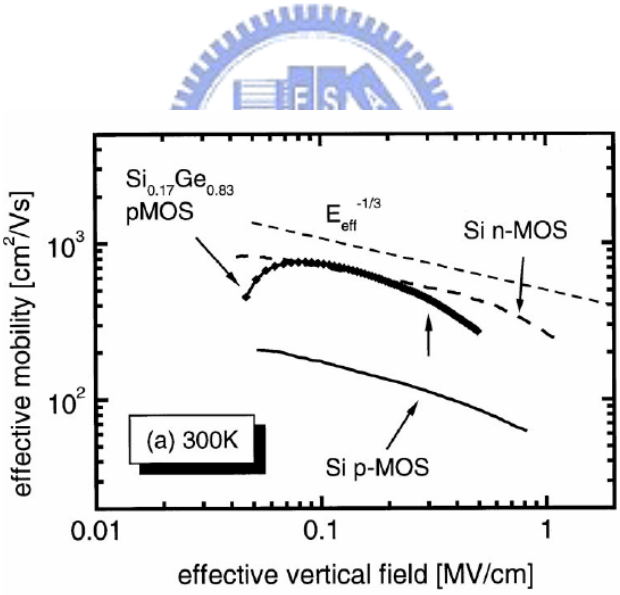


Fig 1.7 Effective carrier mobility in the Si0.17Ge0.83 channel p MOSFET and in conventional Si n and p MOSFETs as a function of the vertical electric field at room temperature

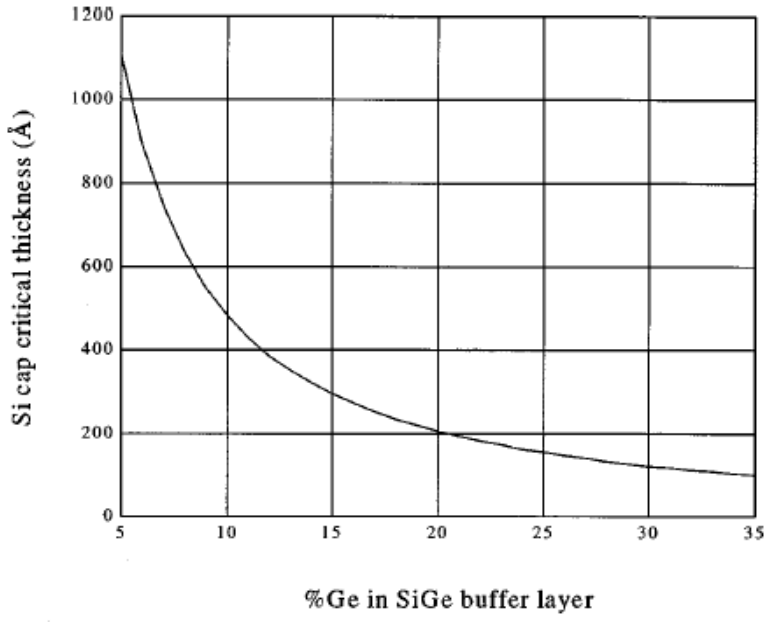


FIG. 2. Si cap critical thickness as a function of Ge% in the uniform SiGe layer.

Fig 1.8 Si cap critical thickness as a function of Ge % in the uniform SiGe layer.

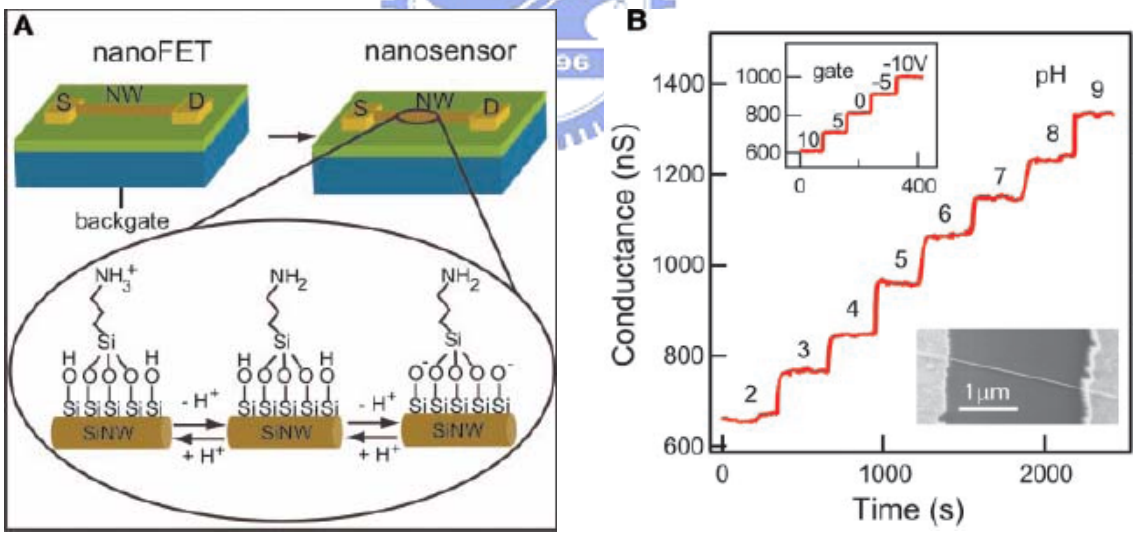


Fig 1.9 NW nanosensor for pH detection. (A) Schematic illustrating the conversion of a NW FET into NW nanosensors for pH sensing. The NW is contacted with two electrodes, a source (S) and drain (D), for measuring conductance. (B) Real-time detection of the conductance for an APTES-modified SiNW for pHs from 2 to 9; the pH values are indicated on the conductance plot.

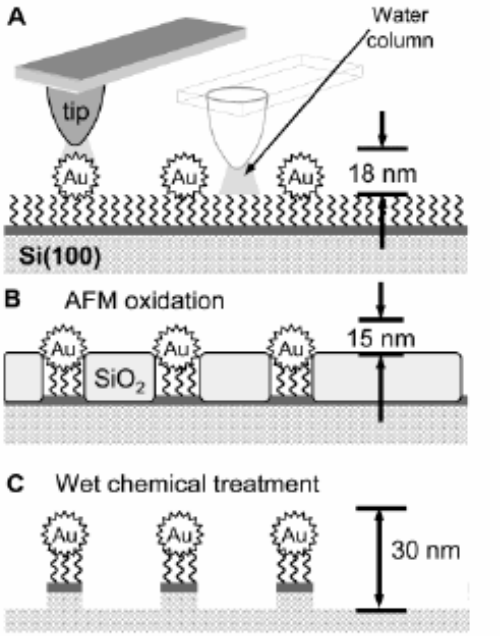


Fig 1.10 Schematic diagram of (A) selective anodization of the silicon regions not masked by nanoparticles. (B) The volume expansion of the silicon led to a decreased height contrast between the particles and the substrate. (C) After a wet etching step, silicon columns capped with a nanoparticle were formed

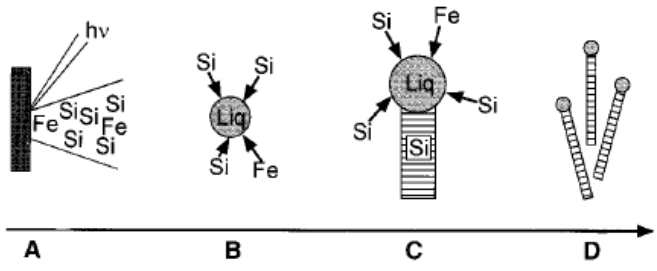


Fig 1.11 The mechanisms of the laser ablation formation technique

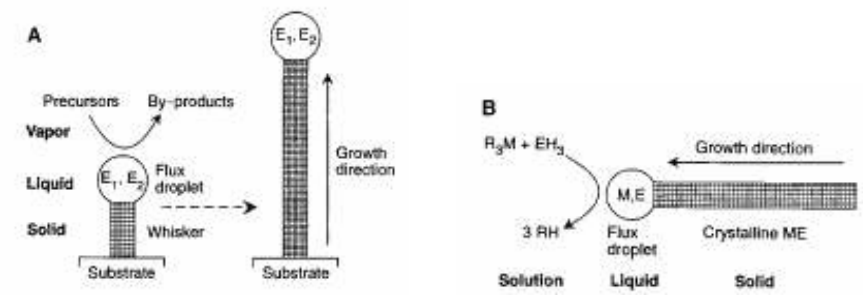


Fig 1.12 (a) VLS mechanism : the flux droplet is a metal such as Au, Ag, Pd, Pt, Ni, or Cu are elements of the crystal phase dissolved in the metallic flux droplet. (b) SLS mechanism : the flux droplet is In, and M and E are elements of the III-V semiconductor dissolved in the flux droplet.

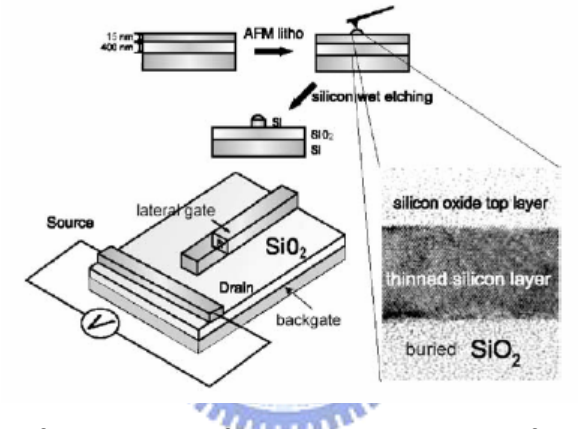


Fig 1.13 Schematics of the process for silicon nanodevice fabrication involving an AFM lithography step. Inset: tranmission electron imcrography of a thinned Unibond SOI substrate showing the good crystalline structure of the Si upper layer.

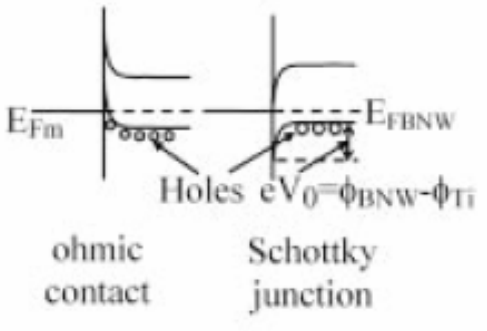


Fig 1.14 (a) Band diagram for ohmic contace
(b) Band diagram for barrier contact; eVo is the built-in potential of the Schottky junction

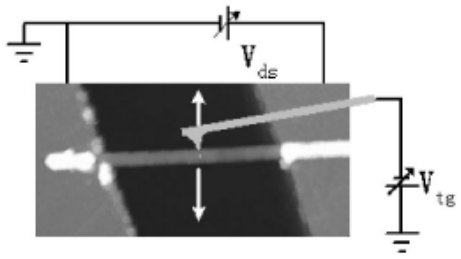


Fig 1.15 A schematic of scanning tip gating, a negatively biased conductive tip is scanned across the nanowire

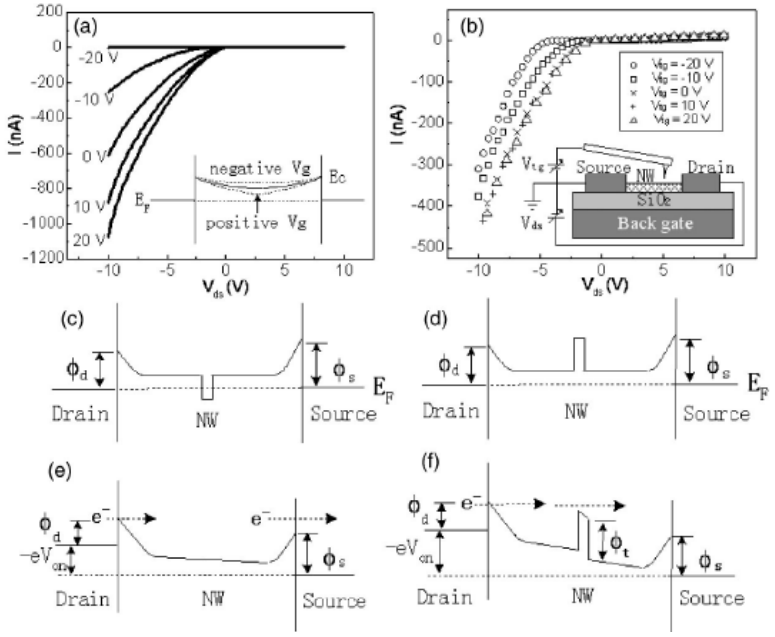


Fig 1.16 (a) I-V curves under different back gate voltages of –20, -10, 0, 10, and 20V. (b) I-V curves under different tip gate voltages. Inset: schematic showing the circuit measurement setup. (c) Local energy band benging caused by positive SPM tip gate voltage, and (d) negative tip gate voltage, (e)At negative drain-source bias, energy diagram for zero bias SPM tip gating and (f) negatively biased tip gating.

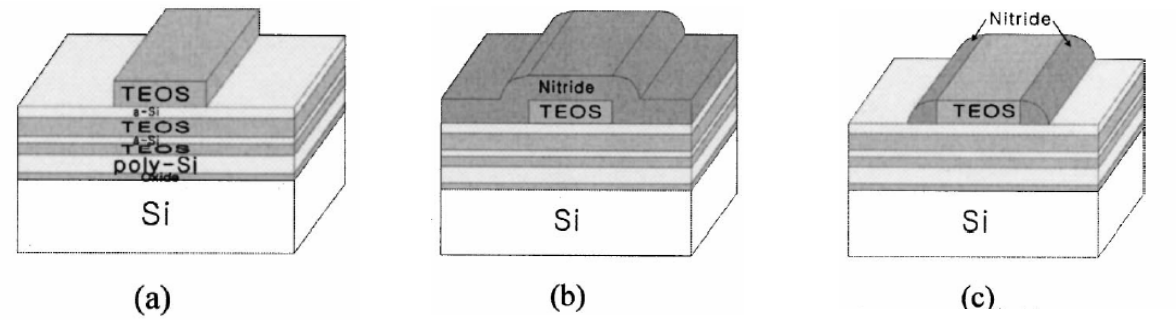


Fig 2.1 The schematic of the sidewall spacer technology.

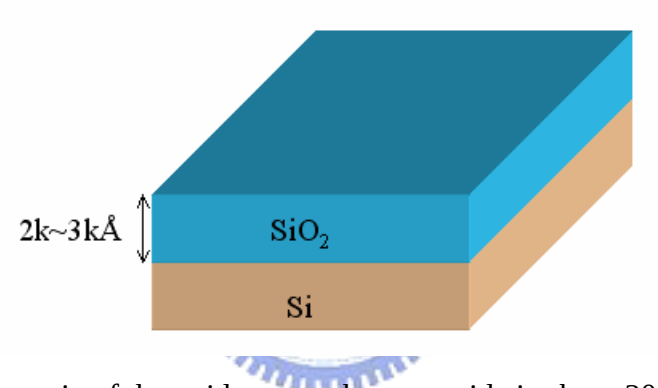
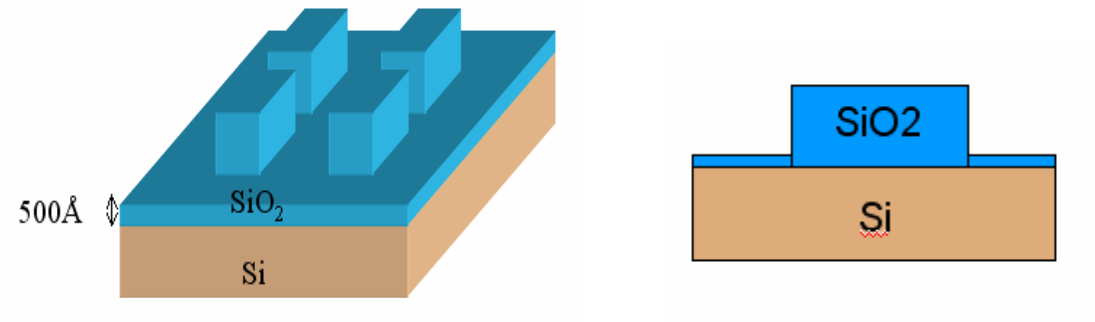


Fig 2.2 The schematic of the oxide grown by wet oxide is about 2000~3000Å.



(a) (b)

Fig 2.3 Define the AA region, we etch the oxide film to form each oxide step by the *TEL 5000*. The residue thickness of the oxide is around 300~500Å and this should be precisely controlled. (a) The top view, (b) The cross-section view

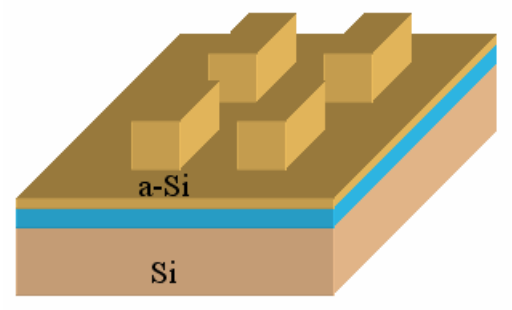
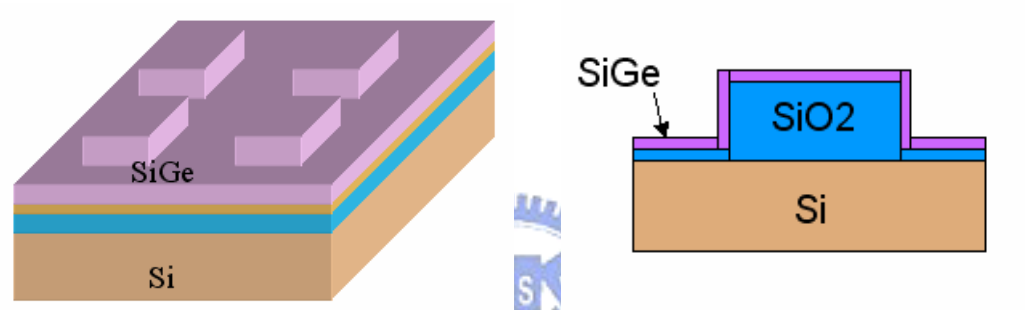
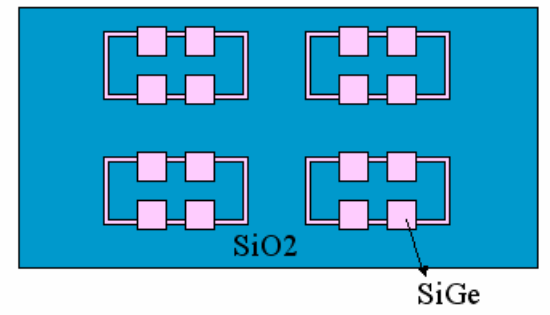


Fig 2.4 Before we deposited the SiGe film, we deposited amorphous Si film first. This purpose is due to SiGe and SiO_2 has a had adhesion. The thickness of the amorphous Si film is about 150Å.



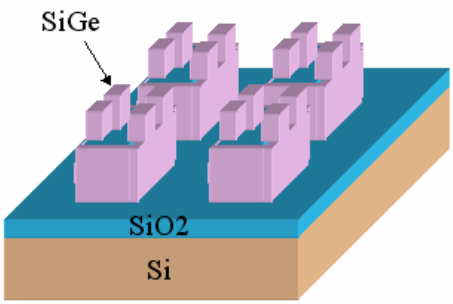
(a) (b)

Fig 2.5 The SiGe film is deposited with the ultra-high-vaccum chemical vapor deposition. The SiGe film is about 800 Å. (a) The top view, (b) The cross-section view



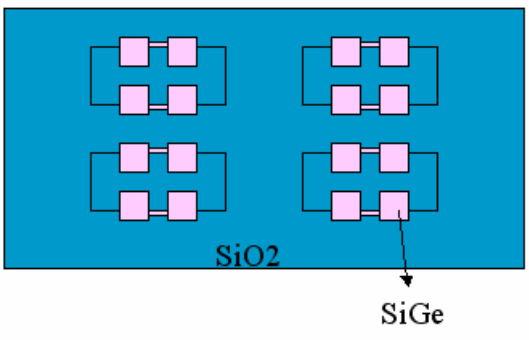
(a)

Fig 2.6 After defining the SiGe pattern by the Mask #2, then etching the whole SiGe up by TCP poly etcher. (a) The schematic shows the top view.

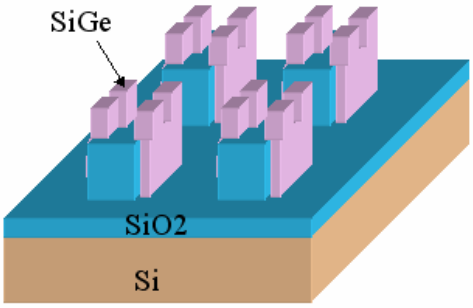


(b)

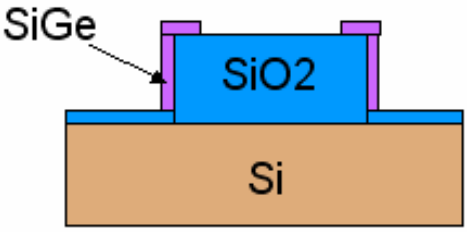
Fig 2.6 (b) The schematics shows the side view, after etching the SiGe film.



(a)



(b)



(c)

Fig 2.7 Remove one side of the parallel SiGe spacer. The schematics of the Mask #3. (a) Top view, (b) Side view, (c) The cross-section view

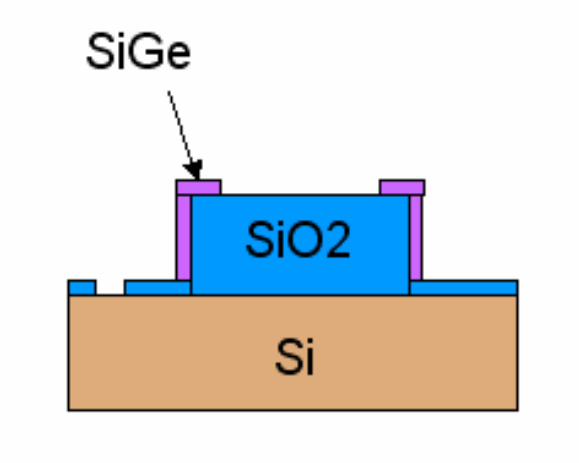


Fig 2.8 The figure show the Gate contact hole etching

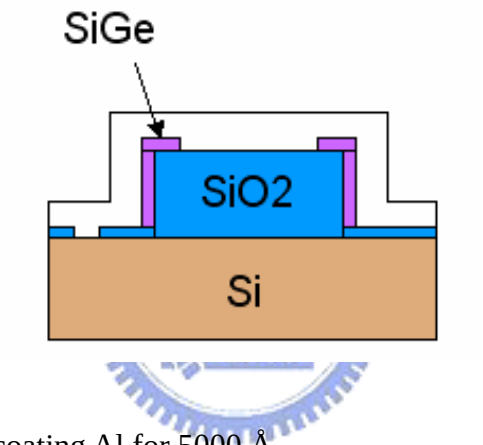


Fig 2.9 After thermal coating Al for 5000 Å

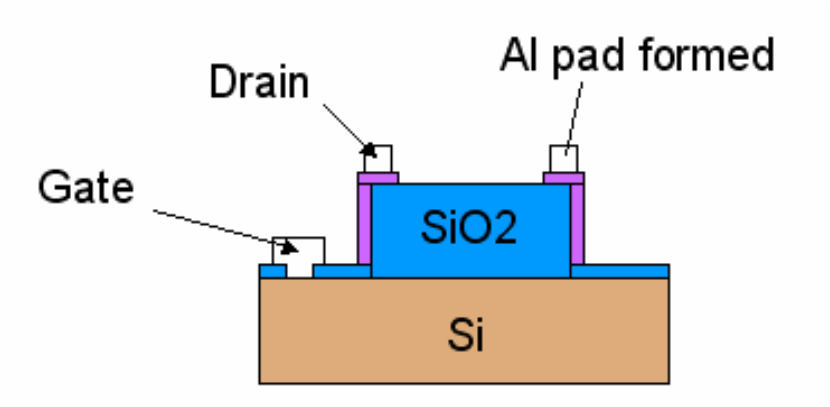


Fig 2.10 Defined the Al contact pad in the Mask #05. And then sintering at T=430℃ for 30 min

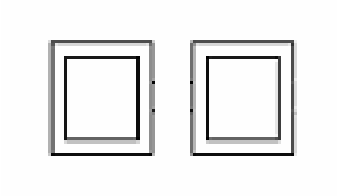


Fig 2.11 The schematics of the two SiGe block film. There is no connection between the two block. This was used to make sure that the SiGe and Al film was etched completely in the isolation area.

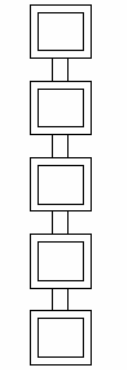


Fig 2.12 The test structure of each block was used to calculate the contact resistance between Al/SiGe and Al/Poly-Si.

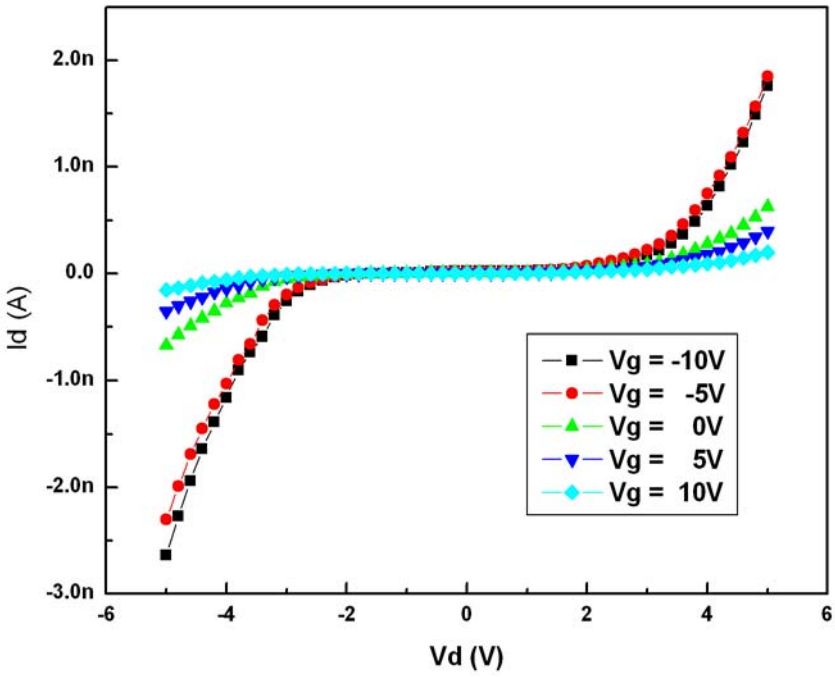


Fig 3.1 The Id-Vd of the **$Si_{0.93}Ge_{0.07}$** nanowire with the length **L=15 μm**.

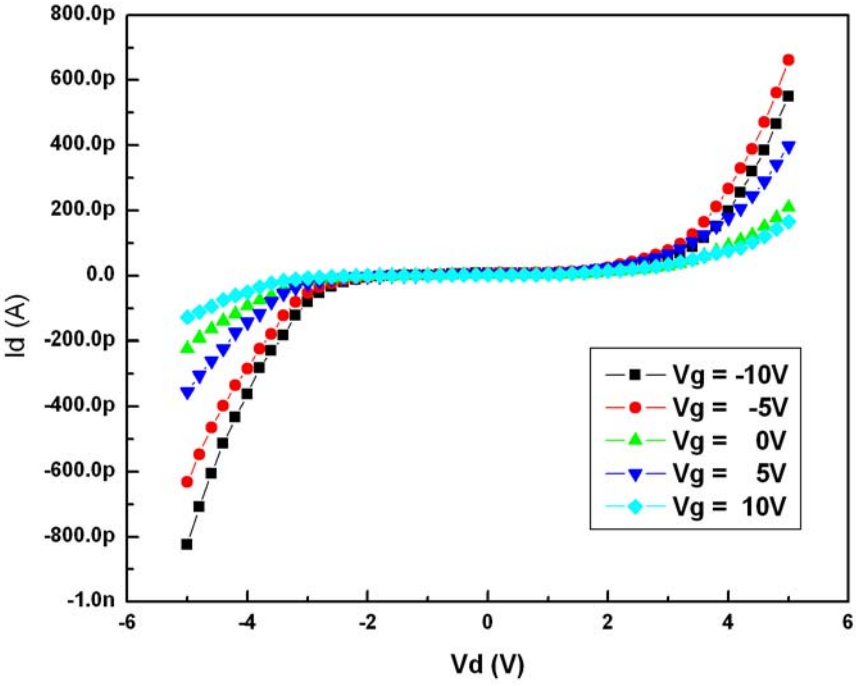


Fig 3.2 The Id-Vd of the **$Si_{0.93}Ge_{0.07}$** nanowire with the length **L=50 μm**.

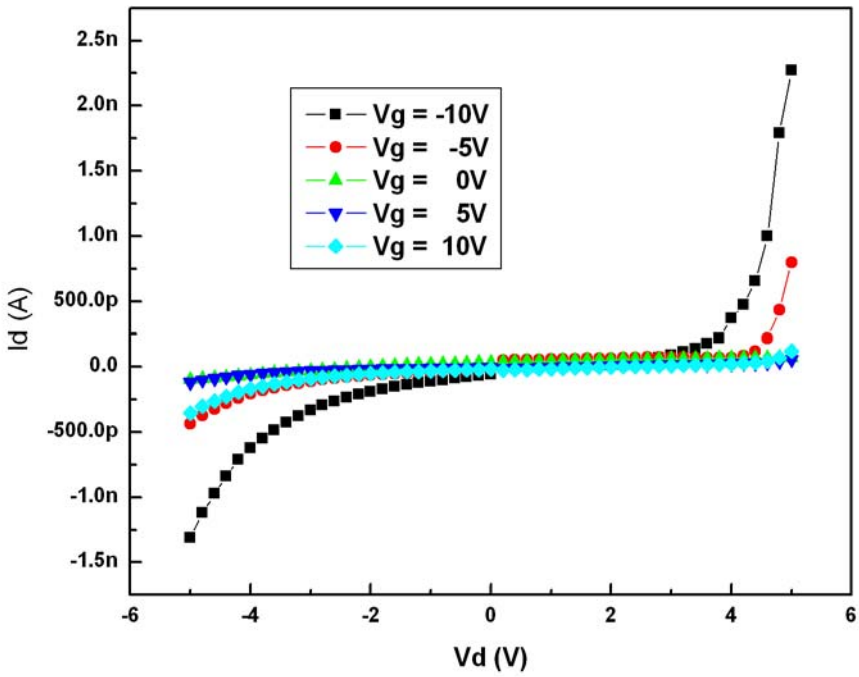


Fig 3.3 The Id-Vd of the **Poly** nanowire with the length **L=5 μm**.

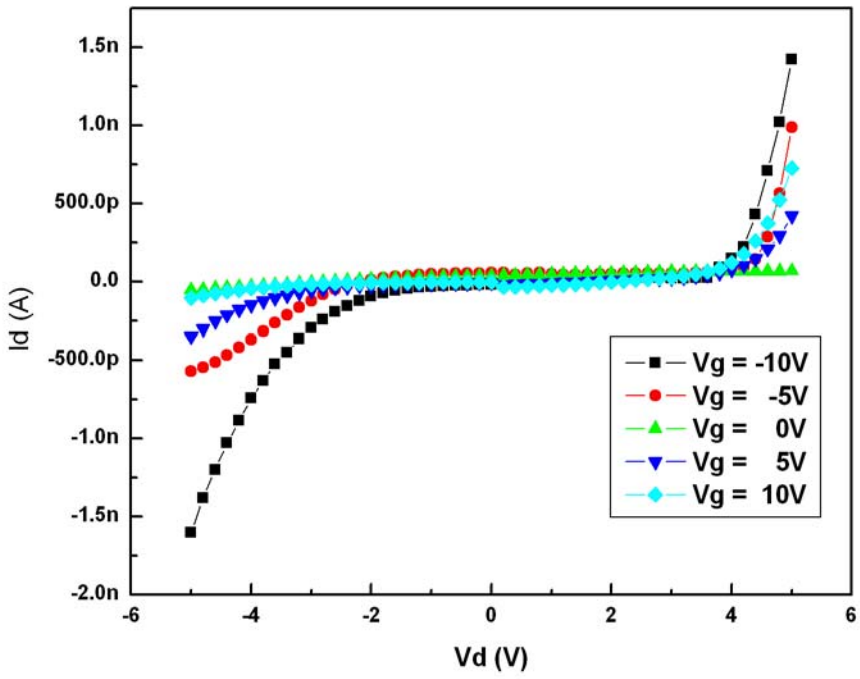
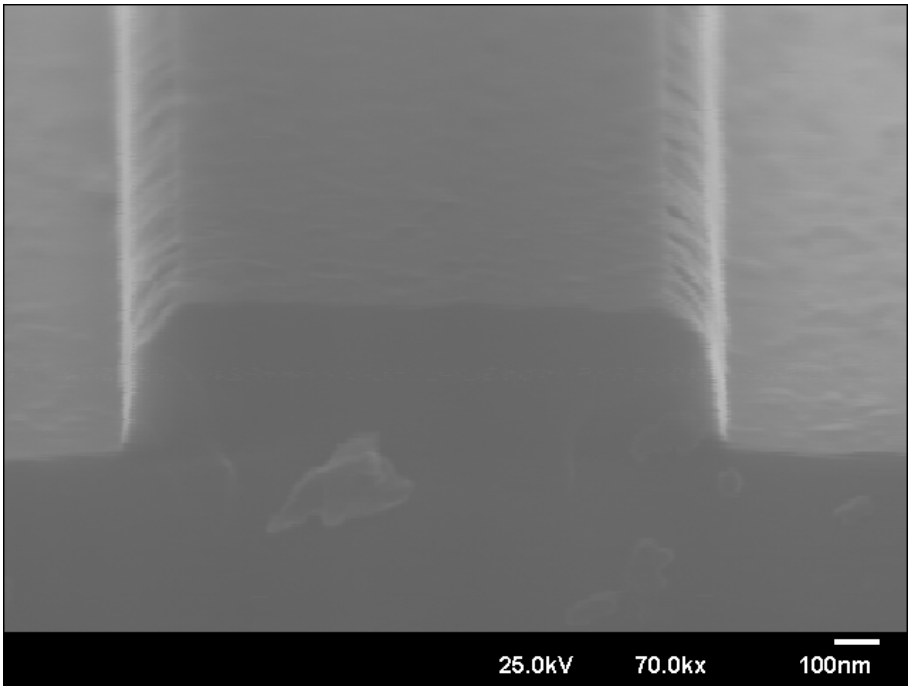
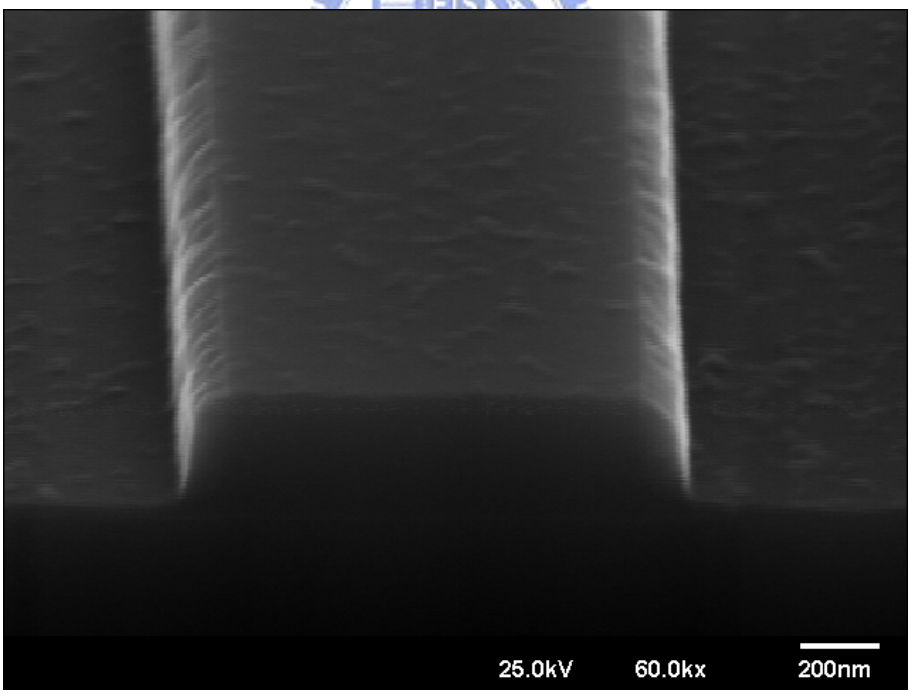


Fig 3.4 The Id-Vd of the **Poly** nanowire with the length **L=15 μm**.

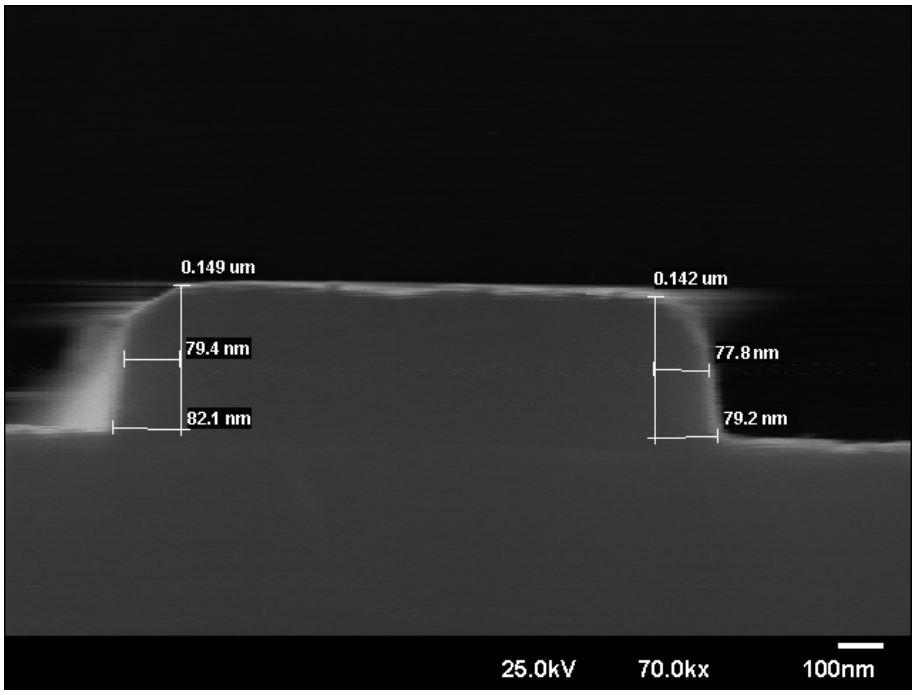


(a)

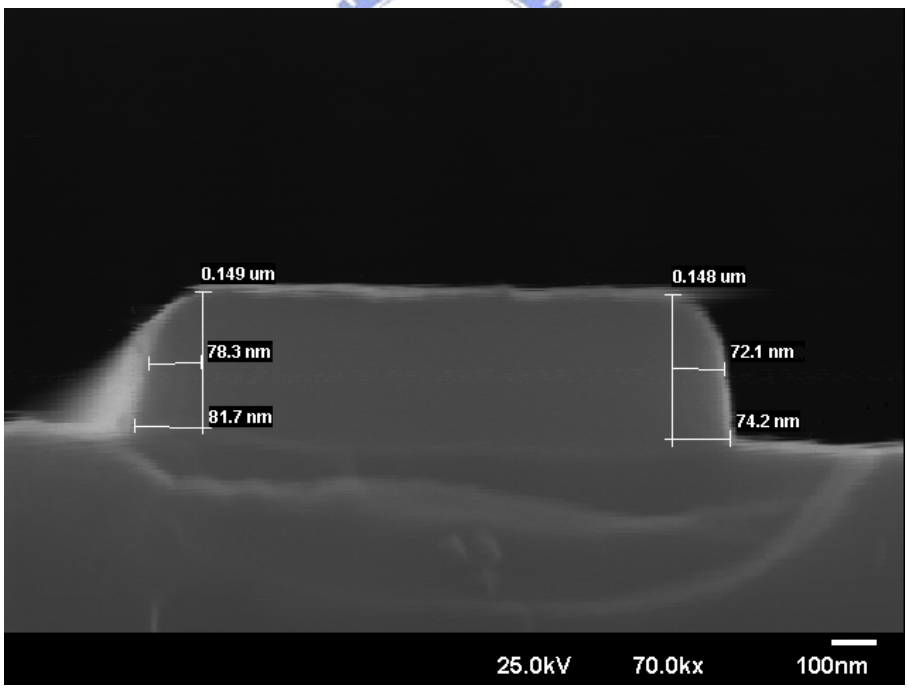


(b)

Fig 3.5 The Top view of the SEM of $Si_{0.93}Ge_{0.07}$ nanowire



(a)

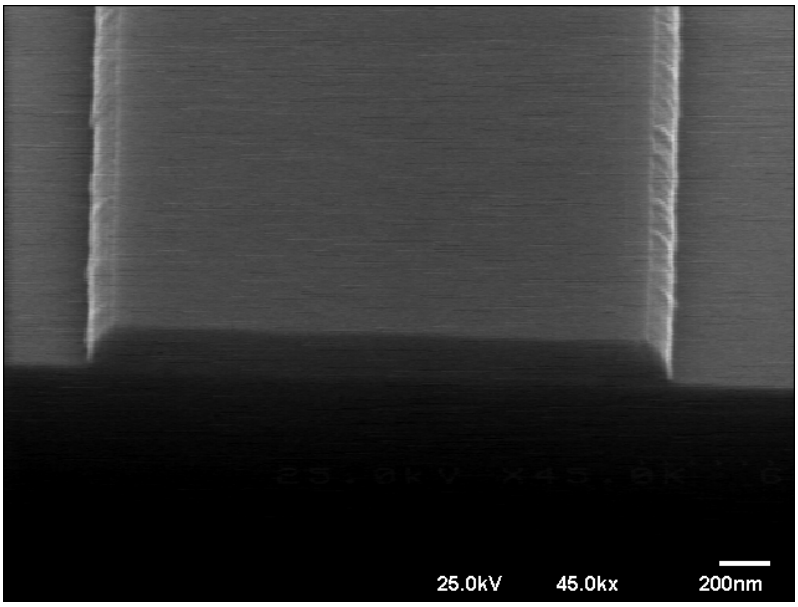


(b)

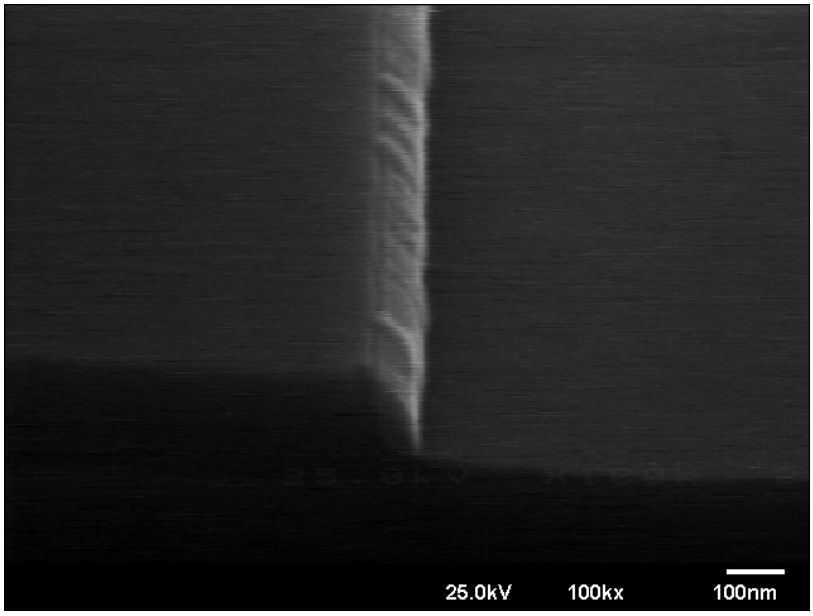
Fig 3.6 The cross-section view of the SEM of $Si_{0.93}Ge_{0.07}$ nanowire

(a) The $Si_{0.93}Ge_{0.07}$ nanowire is 79.4 nm, 77.8 nm in the half width, and 149 nm, 142 nm in height.

(b) The $Si_{0.93}Ge_{0.07}$ nanowire is 78.3 nm, 72.1 nm in the half width and 149 nm, 148 nm in height.

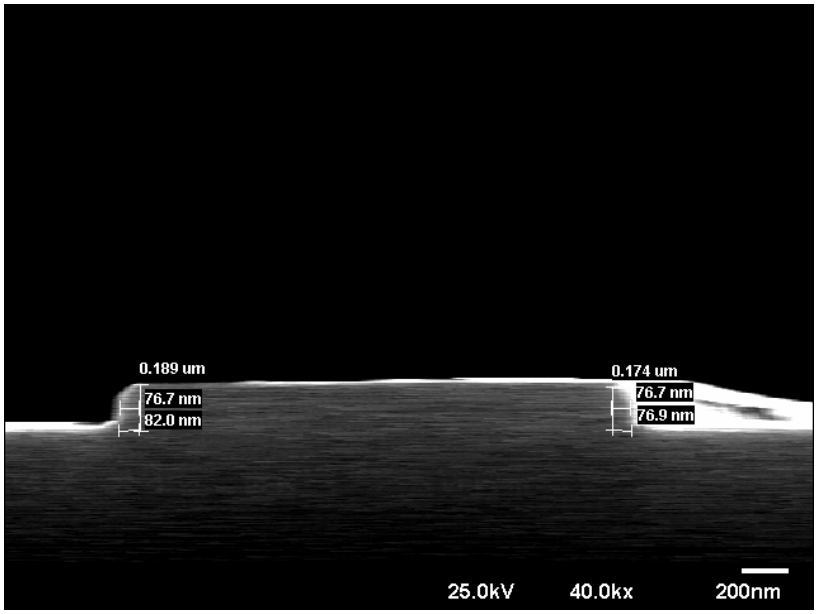


(a)

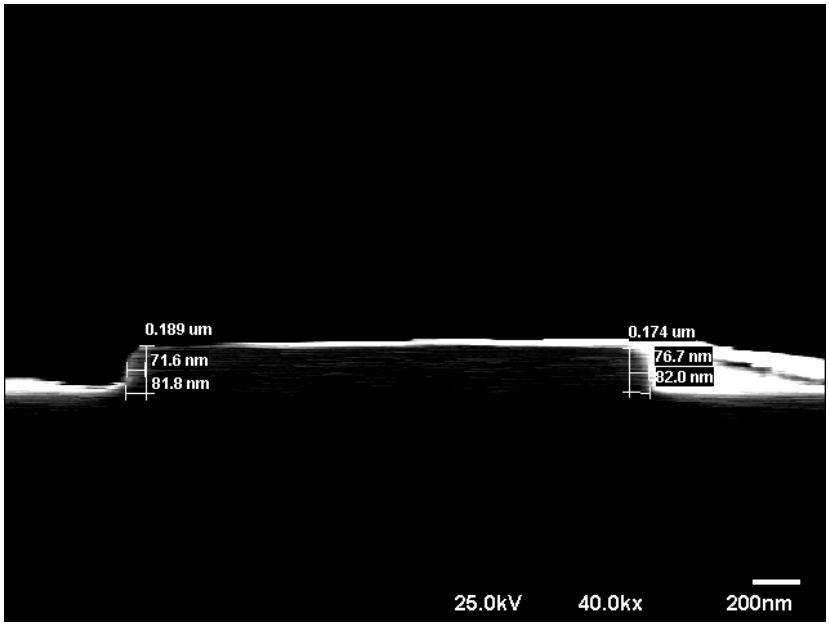


(b)

Fig 3.7 The top view of the SEM of Poly-Si nanowire



(a)



(b)

Fig 3.8 The cross-section view of the SEM of Poly-Si nanowire

(b) The Poly-Si nanowire is 76.7 nm, 76.7 nm in the half width, and 189 nm, 174 nm in height.

(c) The Poly-Si nanowire is 71.6 nm, 76.7 nm in the half width, and 189 nm, 174 nm in height.

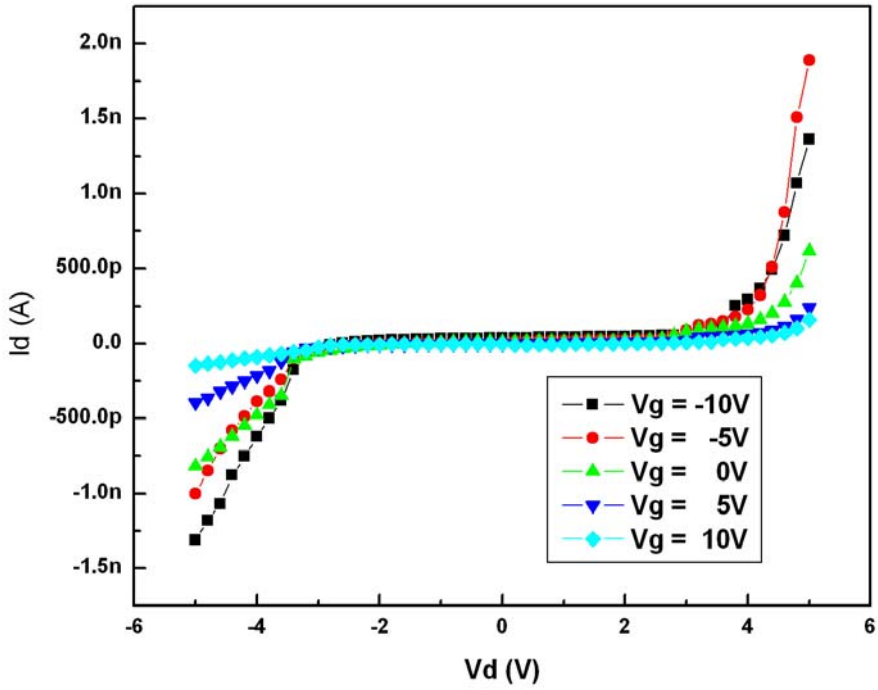


Fig 3.9 The Id-Vd of the $\mathbf{Si_{0.89}Ge_{0.11}}$ nanowire with the length **L=15 μm**.

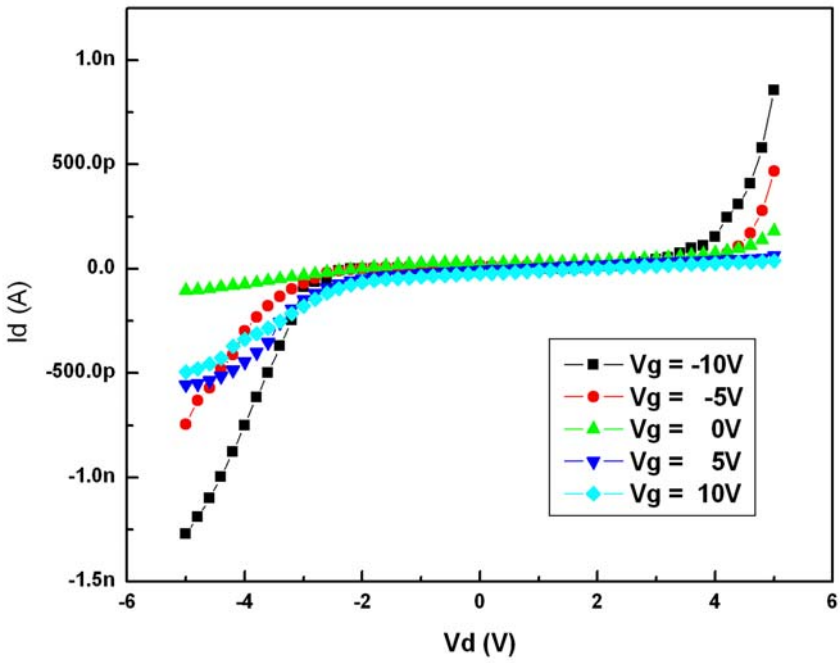


Fig 3.10 The Id-Vd of the $\mathbf{Si_{0.89}Ge_{0.11}}$ nanowire with the length **L=30 μm**.

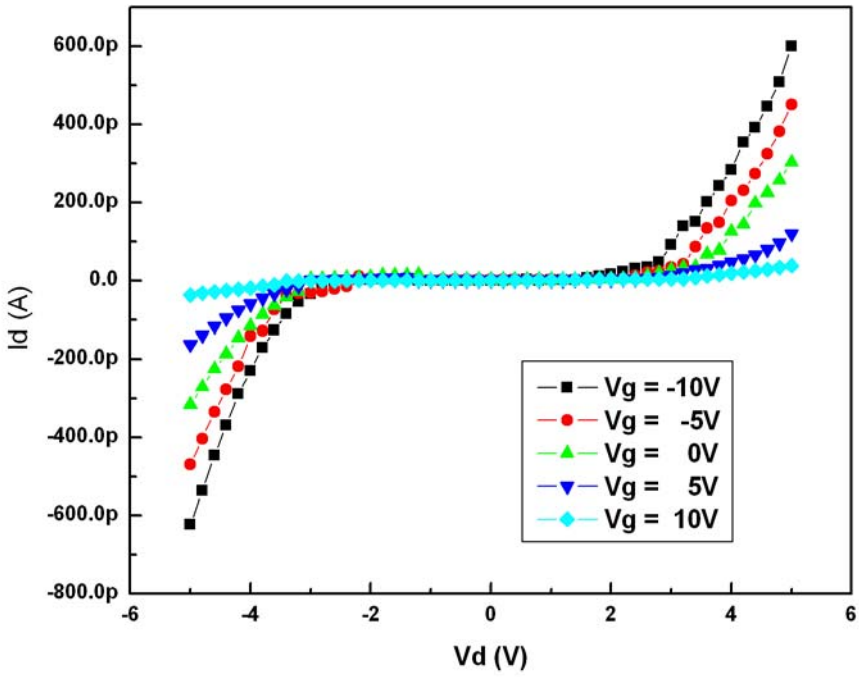


Fig 3.11 The Id-Vd of the $Si_{0.8}Ge_{0.2}$ nanowire with the length **L=15 μ m**.

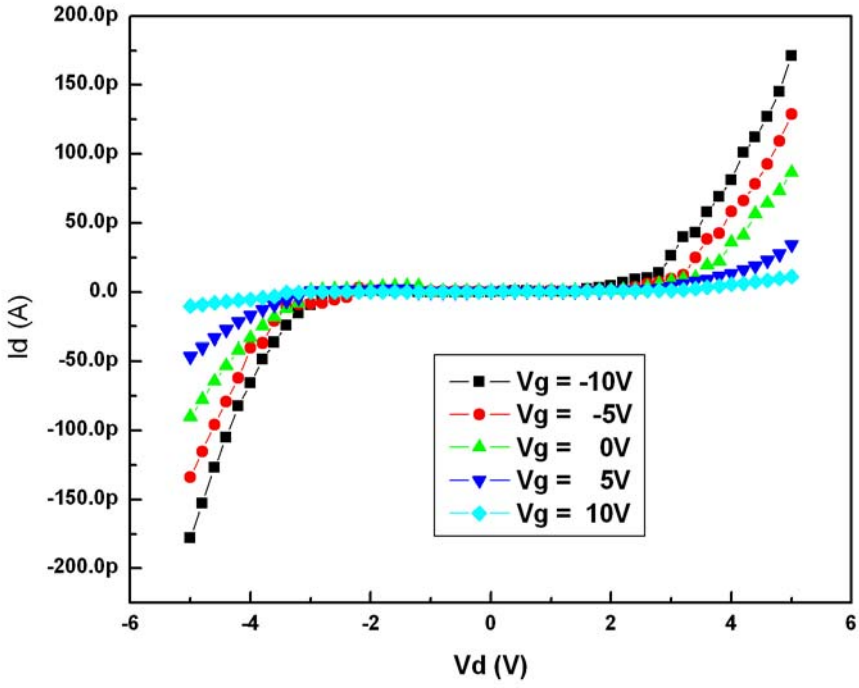
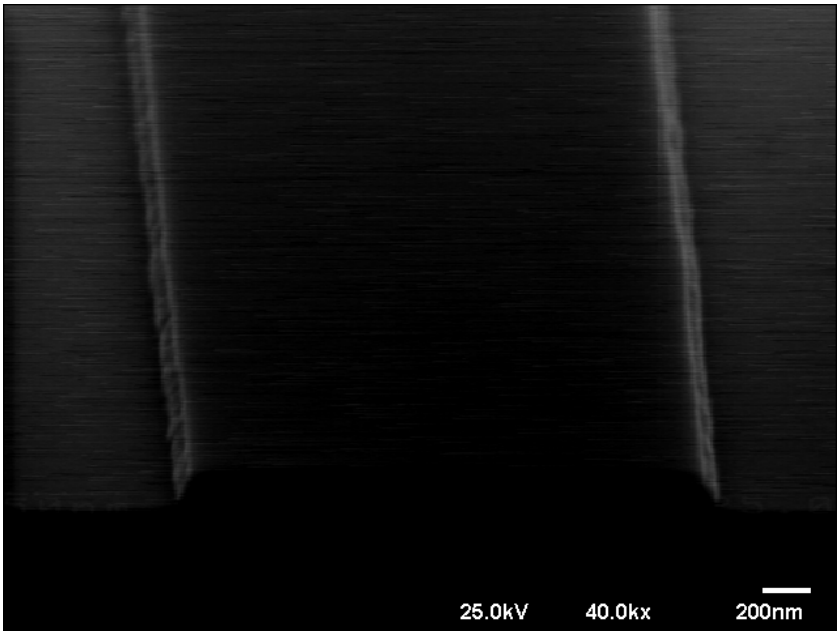
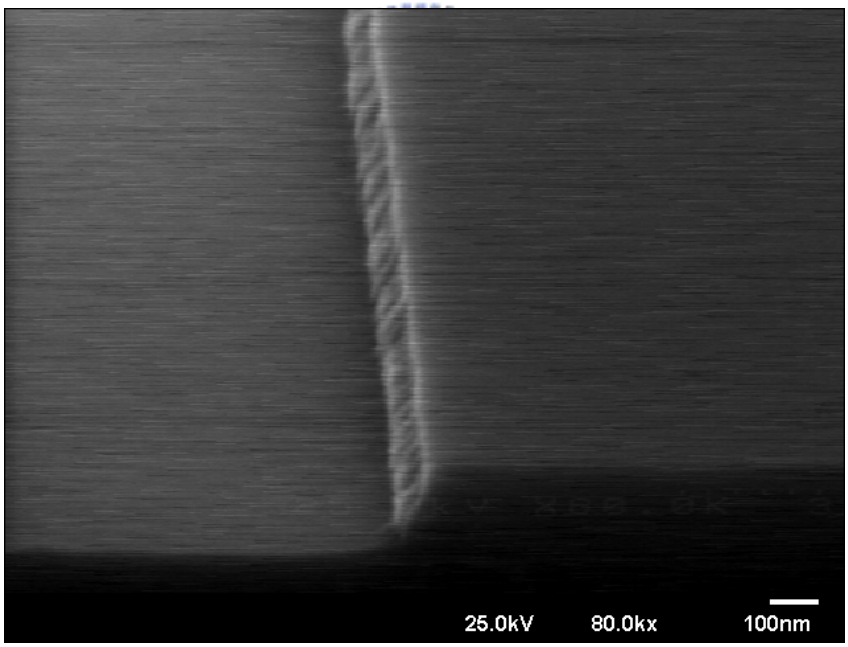


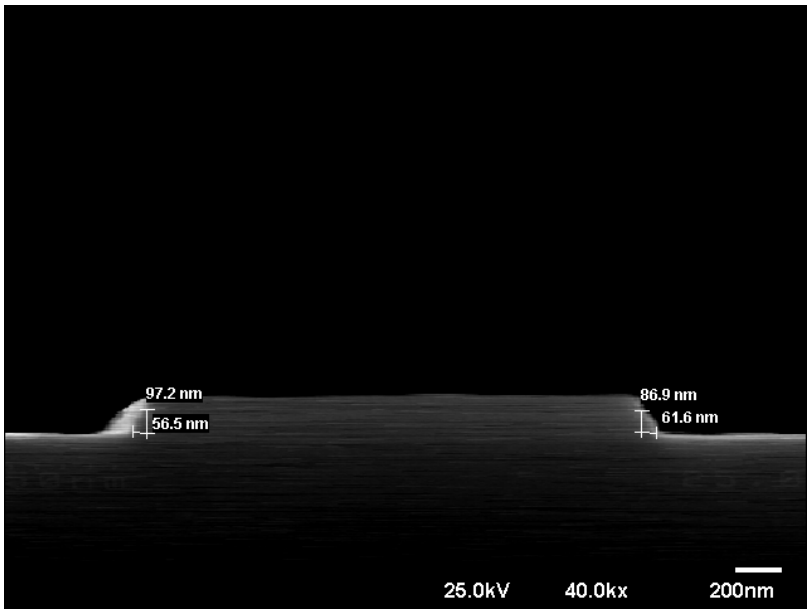
Fig 3.12 The Id-Vd of the $Si_{0.8}Ge_{0.2}$ nanowire with the length **L=30 μ m**.



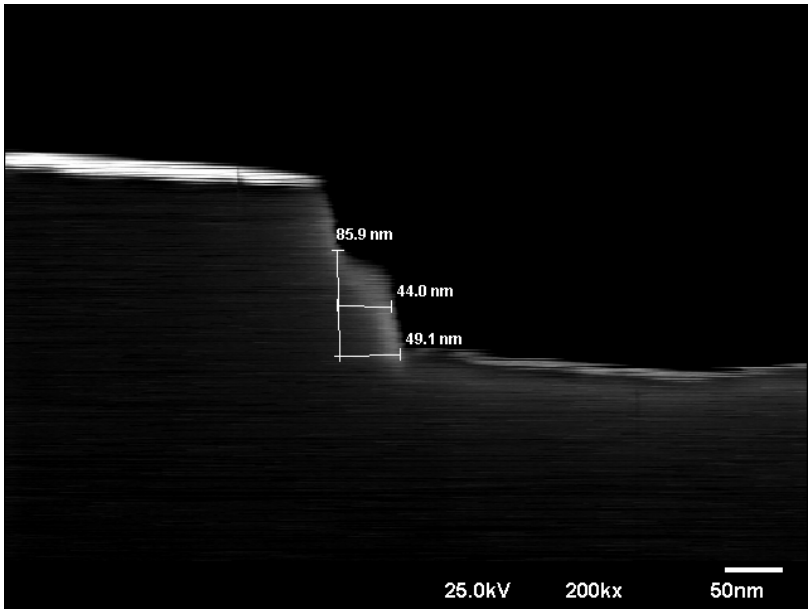
(a)



(b)



(c)



(d)

Fig 3.13(a)(b) The top view of the SEM of $\mathbf{Si_{0.89}Ge_{0.11}}$ nanowire

The cross-section view of the SEM of $\mathbf{Si_{0.89}Ge_{0.11}}$ nanowire

(c) The $\mathbf{Si_{0.89}Ge_{0.11}}$ nanowire is 56.5 nm, 61.6 nm in width, and 86.9 nm, 97.2 nm in height.

(d) The $\mathbf{Si_{0.89}Ge_{0.11}}$ nanowire is 44 nm in the half width, 49.1 nm in width and 85.9 nm in height.

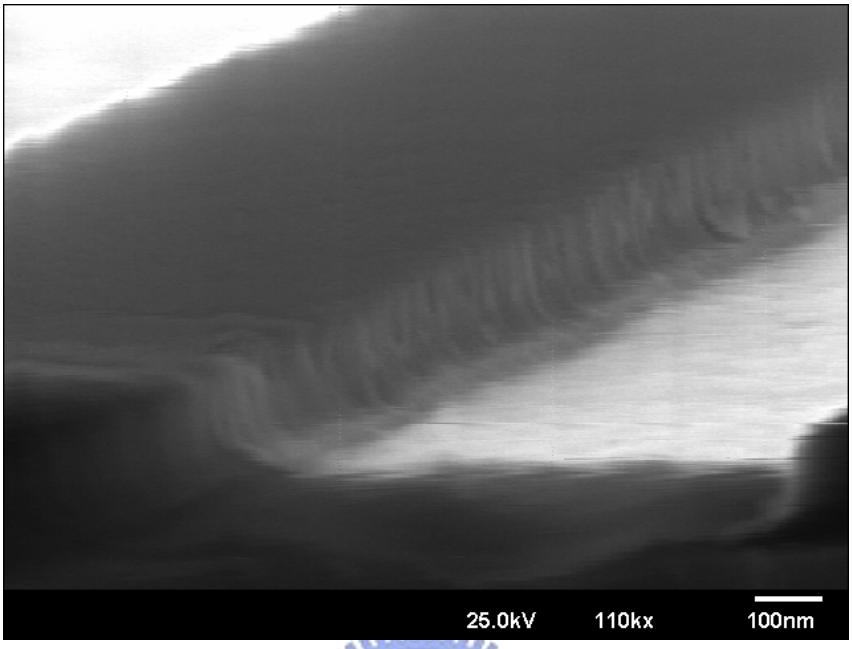


Fig 3.14 The cross-section view of the SEM of $\mathbf{Si_{0.8}Ge_{0.2}}$ nanowire. In this figure, it is evident that there is no nanowire in the side wall spacer

	Poly-Si		**$Si_{0.93}Ge_{0.07}$**		**$Si_{0.89}Ge_{0.11}$**		**$Si_{0.8}Ge_{0.2}$**	
Etching time	32 sec		16 sec		15 sec		17 sec	
	Height	Width	Height	Width	Height	Width	Height	Width
(nm)	189	82	149	81.7	84.1	44.3	150	-
	174	76.9	148	74.2	85.9	49.1	148	-
	159	76.2	144	80.2	90.9	54.7	191	-
	179	77.4	147	82	86.9	59.1	184	-
	181	82	140	78.9	87.3	46	175	-
	175	81.8	151	83.4	81.8	46	143	-
	186	76.2	153	79.9	82	51.4	143	-
	172	-	148	76.4	-		132	-
	179	-	148	77.6	-		126	-
	174	-	-	-	-		171	-
Ave.	176	78.9	147.6	79.5	85	50.1	156.3	-
Half	176	77.4	147.6	76	85	43		
Diameter	**13839 nm^2**		**11218 nm^2**		**3528 nm^2**		-	

Table 1. The diagram show all the lists of the nanowires we measured by SEM and the etching time of etching Poly-Si and SiGe on Mask #02

(The unit of the normalized current was A/V・cm)

	Current	Length	Area	Current
Poly-Si	2.27 nA	5 μm	13839 nm^2	**0.01147**
	1.22 nA	15 μm	13839 nm^2	**0.01312**
$Si_{0.93}Ge_{0.07}$	1.76 nA	15 μm	11218 nm^2	**0.01773**
	0.5 nA	50 μm	11218 nm^2	**0.01872**
$Si_{0.89}Ge_{0.11}$	1.36 nA	15 μm	3528 nm^2	**0.1178**
	0.855 nA	30 μm	3528 nm^2	**0.1168**

Table 2. The diagram show the lists of the normalized current we calculated. It is obvious that the $Si_{0.89}Ge_{0.11}$ has higher current

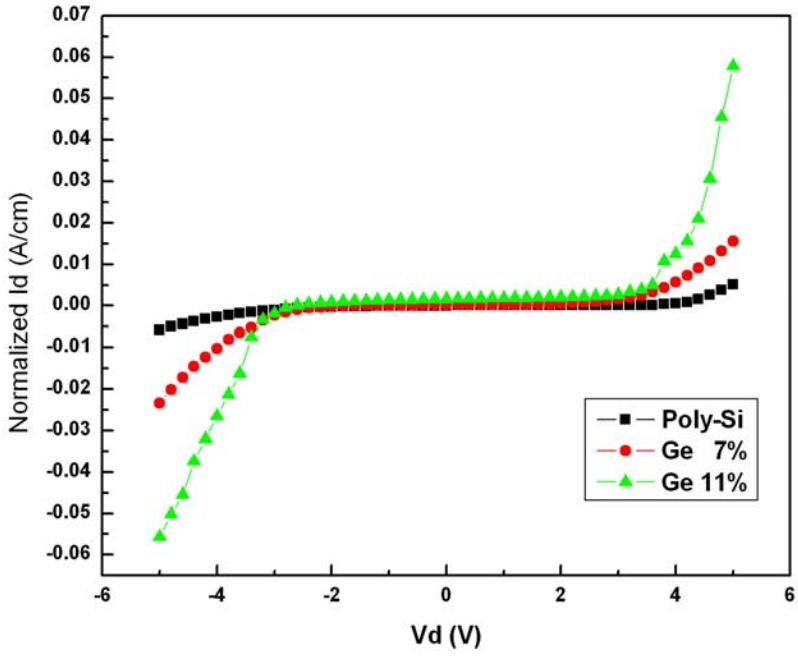


Fig 3.15 Show the normalized Id-Vd. It is obvious that the SiGe nanowire has higher current than Poly-Si one.

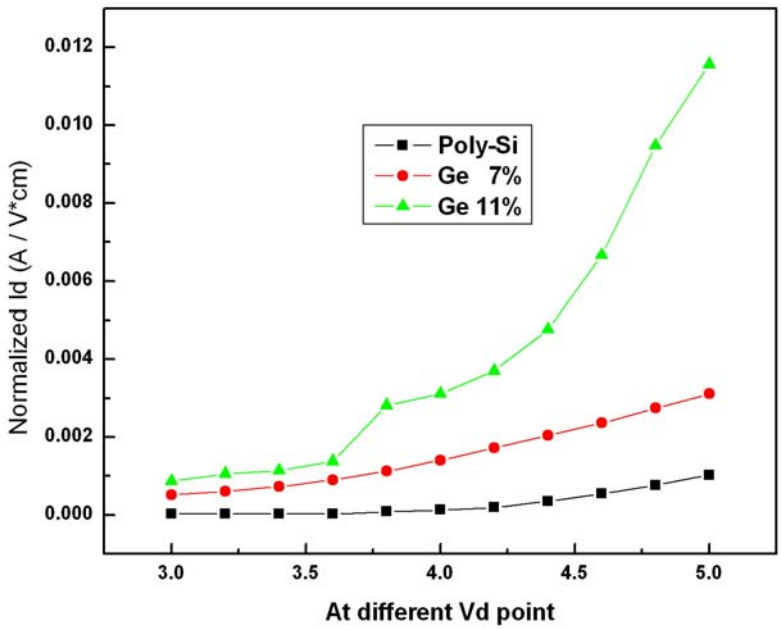
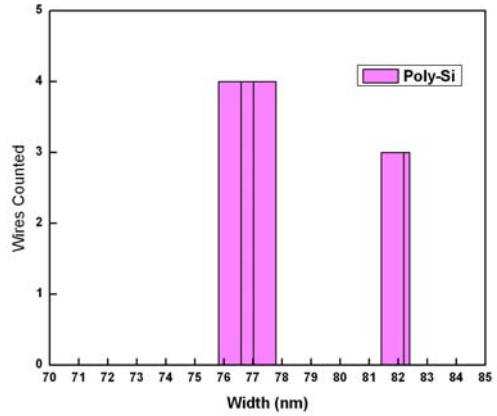
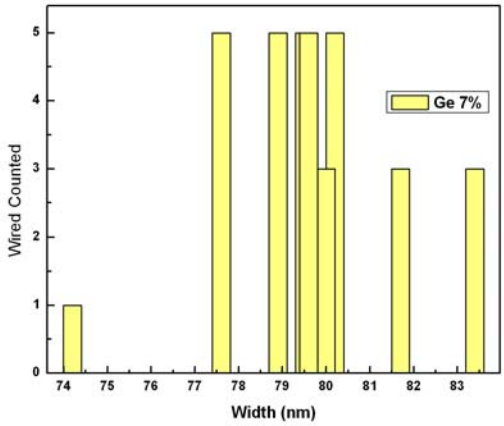


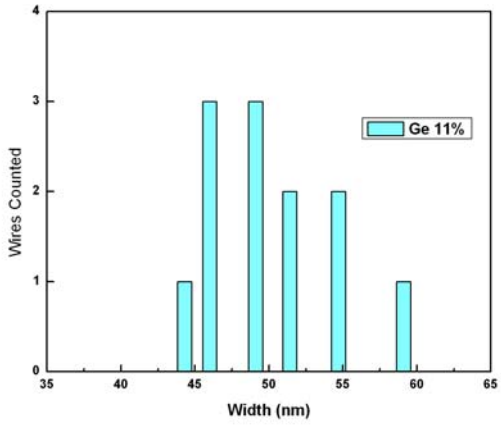
Fig 3.16 Show the normalized Id-Vd from 3 V to 5 V. It is obvious that the SiGe nanowire has higher current than Poly-Si one at the conducting region.



(a) Poly-Si



(b) Ge 7%



(c) Ge 11%

Table 3. Histograms of the (a) Poly-Si, (b) $Si_{0.93}Ge_{0.07}$, (c) $Si_{0.89}Ge_{0.11}$ show the nanowire diameters. The bar chart show a little Gaussian Distributions.

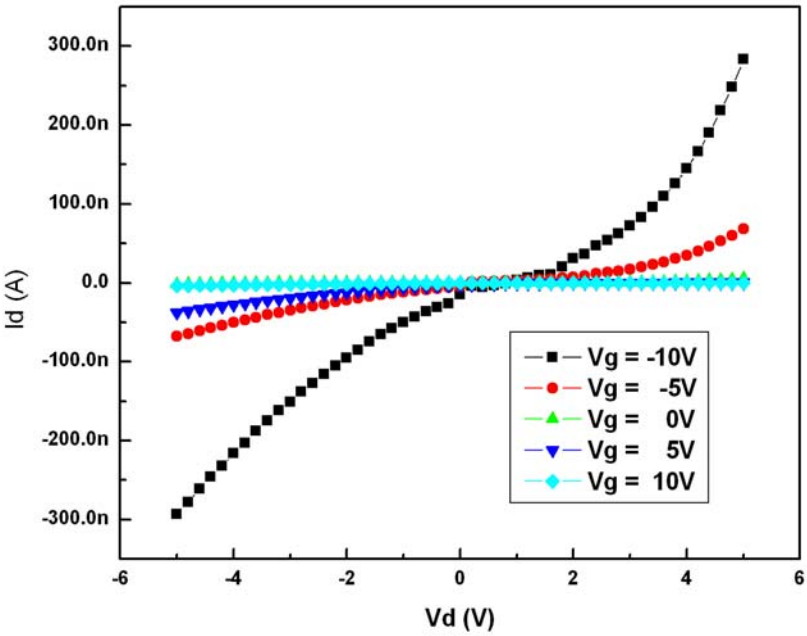


Fig 3.17 The Id-Vd of the **$Si_{0.93}Ge_{0.07}$** nanowire with the length **L=20 μm** after thermal annealing.

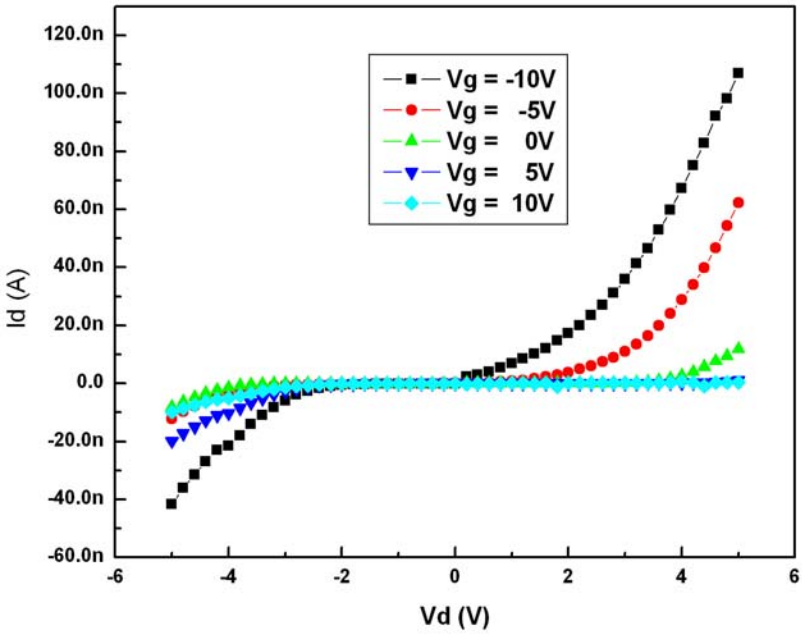


Fig 3.18 The Id-Vd of the **Poly-Si** nanowire with the length **L=13 μm** after thermal annealing.

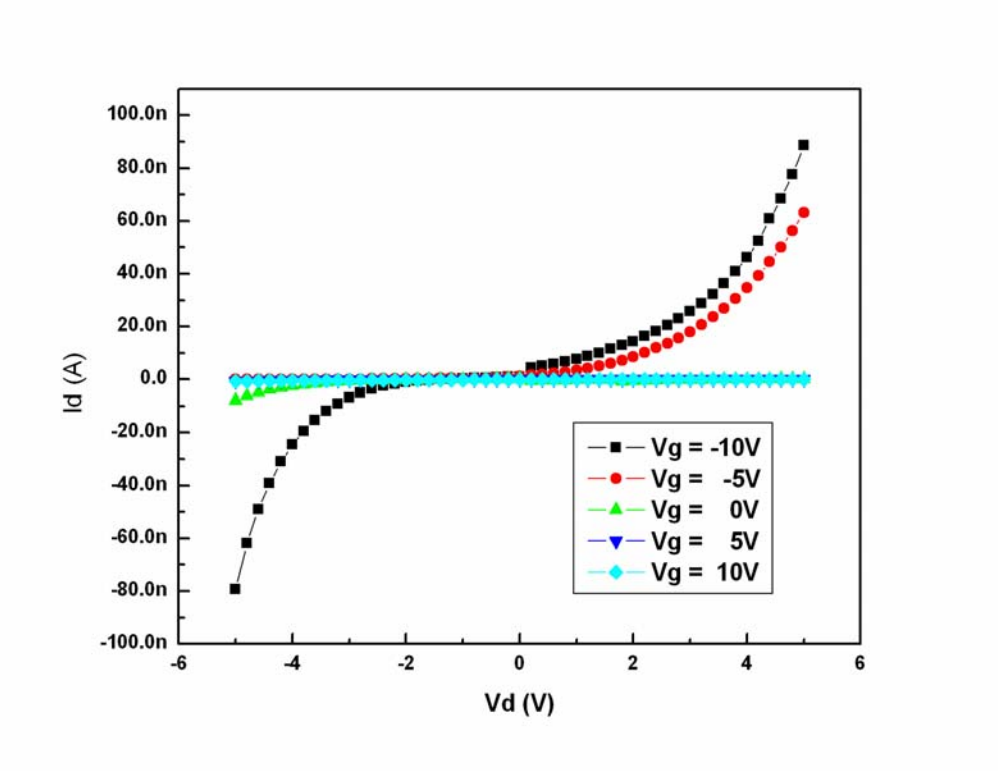
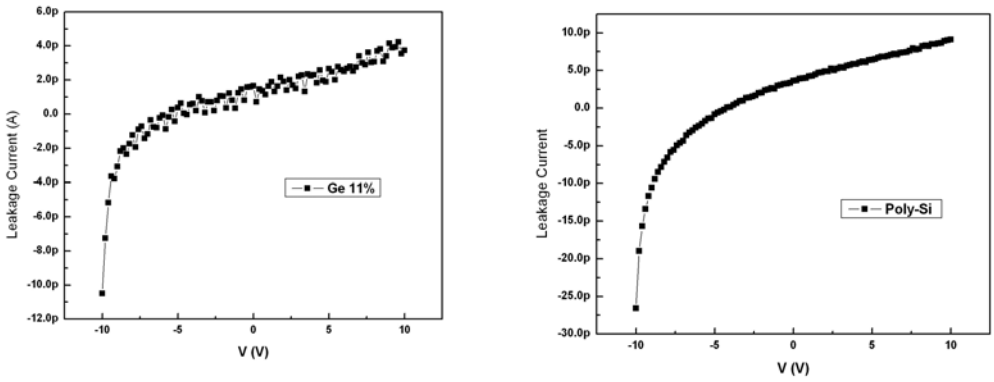


Fig 3.19 The Id-Vd of the $\mathbf{Si_{0.89}Ge_{0.11}}$ nanowire with the length **L=20 μm** after thermal annealing.



(a) $\mathbf{Si_{0.89}Ge_{0.11}}$ (b) **Poly-Si**

Fig 3.20 Show the Source/Drain leakage current of the structure of (a) $\mathbf{Si_{0.89}Ge_{0.11}}$, (b) Poly-Si.

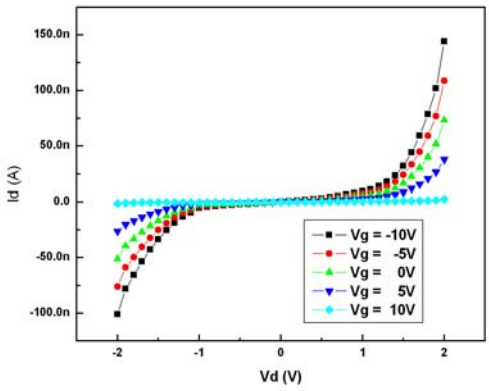


Fig 3.21 The Id-Vd of the **$Si_{0.89}Ge_{0.11}$** nanowire with the length **L=4 μm** after S/D Ion Implantation.

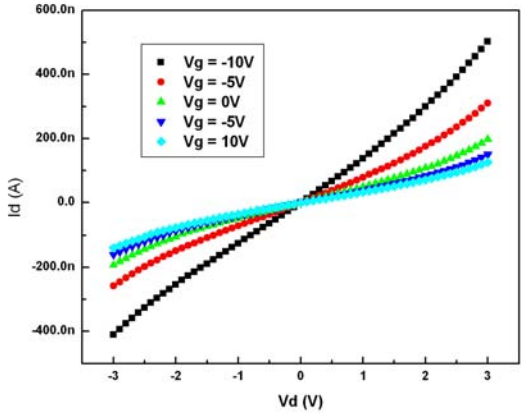


Fig 3.22 The Id-Vd of the **Poly-Si** nanowire with the length **L=5 μm** after S/D Ion Implantation.

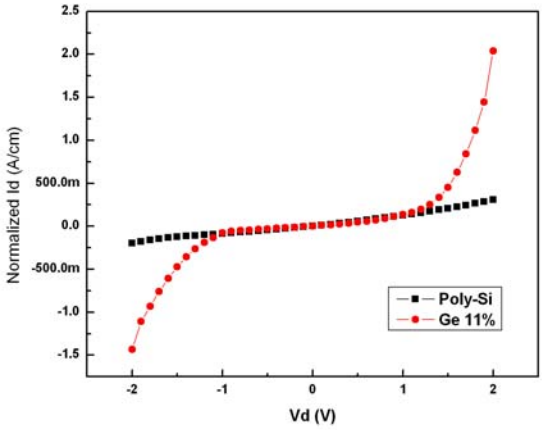


Fig 3.23 The Id-Vd is normalized of the L=5 μm which the Vg is fixed at –10V.

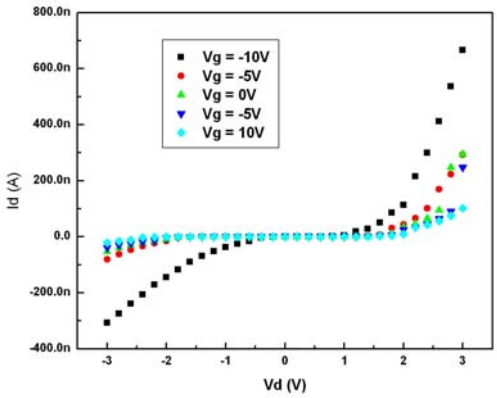


Fig 3.24 The Id-Vd of the **$Si_{0.89}Ge_{0.11}$** nanowire with the length **L=5 μ m** after S/D Ion Implantation.

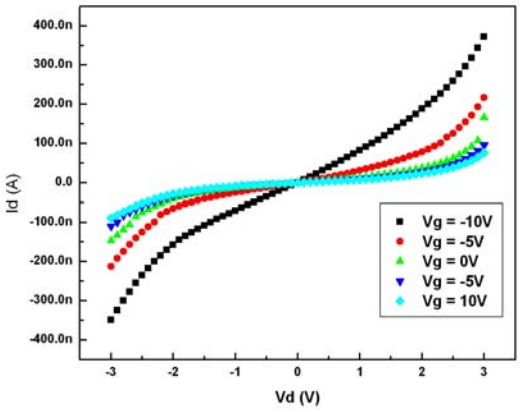


Fig 3.25 The Id-Vd of the **Poly-Si** nanowire with the length **L=5 μ m** after S/D Ion Implantation.

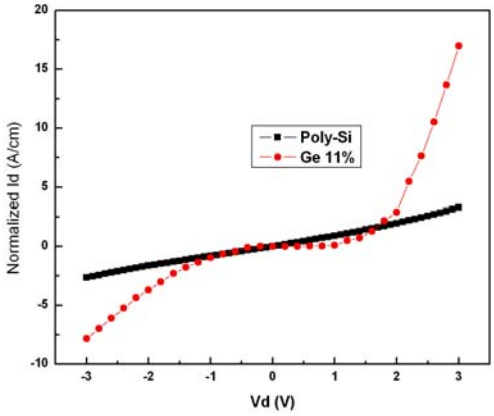


Fig 3.26 The Id-Vd is normalized of the L=4 μ m which the Vg is fixed at –10V. It is obvious that the current of SiGe nanowire is higher.

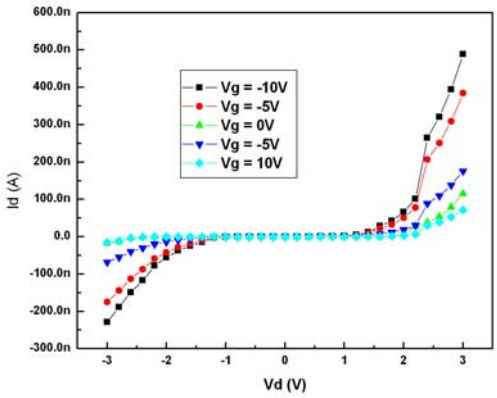


Fig 3.27 The Id-Vd of the **$Si_{0.89}Ge_{0.11}$** nanowire with the length **L=6 μm** after S/D Ion Implantation.

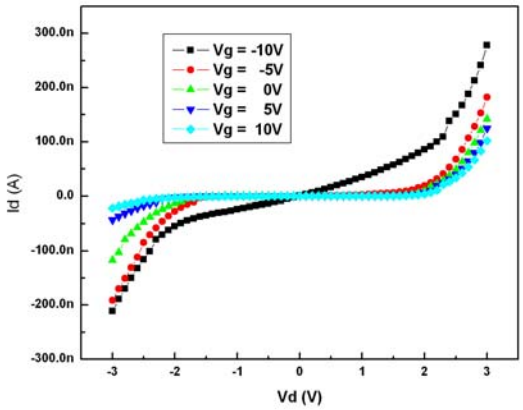


Fig 3.28 The Id-Vd of the **Poly-Si** nanowire with the length **L=6 μm** after S/D Ion Implantation.

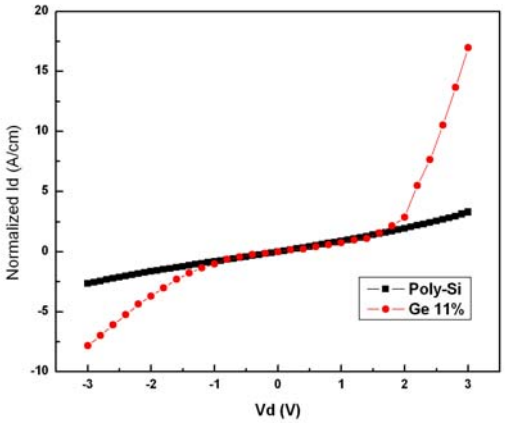


Fig 3.29 The Id-Vd is normalized which the Vg is fixed at –10V. It is obvious that the current of SiGe nanowire is higher.

(The unit of the normalized current was A/V・cm)

	Length	Area	S/D Implant	Initial
Poly-Si	L=5 μ m	13839 nm^2	0.915	0.01147
	L=5 μ m	13839 nm^2	0.918	0.01312
	L=6 μ m	13839 nm^2	0.962	-
$Si_{0.89}Ge_{0.11}$	L=4 μ m	3528 nm^2	7.256	0.1178
	L=5 μ m	3528 nm^2	7.201	0.1168
	L=6 μ m	3528 nm^2	6.732	-

Table 4. The diagram list the current after S/D ion implantation then anneal at T=950 ℃ for 30 min. Each term of the current was improved by the process due to reduce the contact resistance

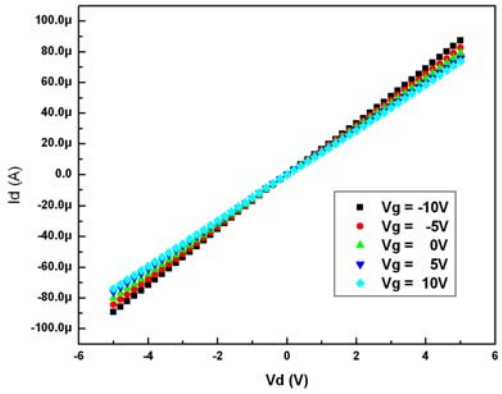


Fig 3.30 The Id-Vd of the **$Si_{0.89}Ge_{0.11}$** nanowire with the length **L=2 μ m** after S/D and Channel Ion Implantation.

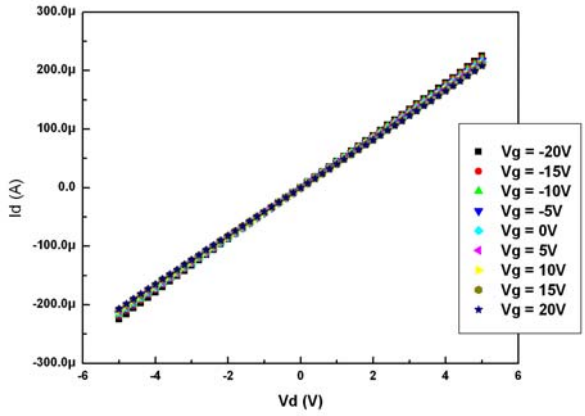


Fig 3.31 The Id-Vd of the **Poly-Si** nanowire with the length **L=2 μ m** after S/D and Channel Ion Implantation.

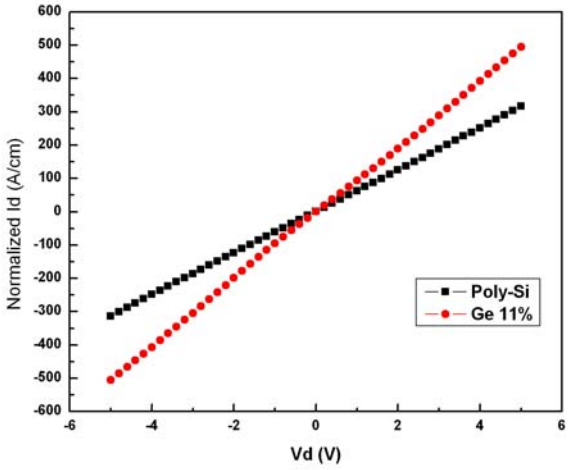


Fig 3.32 The Id-Vd is normalized of the L=2 μ m which the Vg is fixed at –10V.

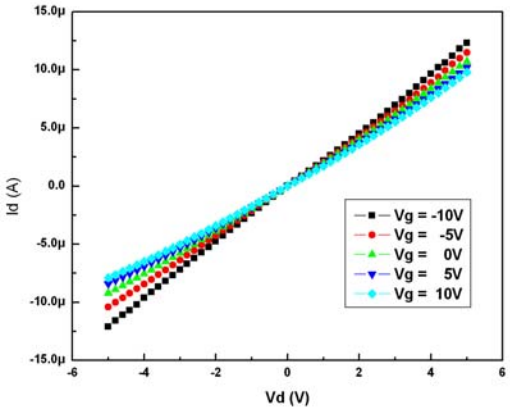


Fig 3.33 The Id-Vd of the **$Si_{0.89}Ge_{0.11}$** nanowire with the length **L=15 μm** after S/D and Channel Ion Implantation.

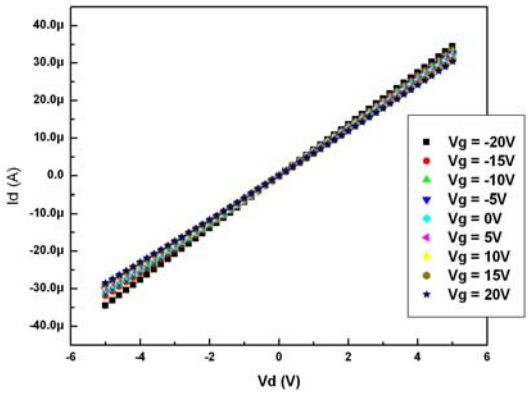


Fig 3.34 The Id-Vd of the **Poly-Si** nanowire with the length **L=15 μm** after S/D and Channel Ion Implantation.

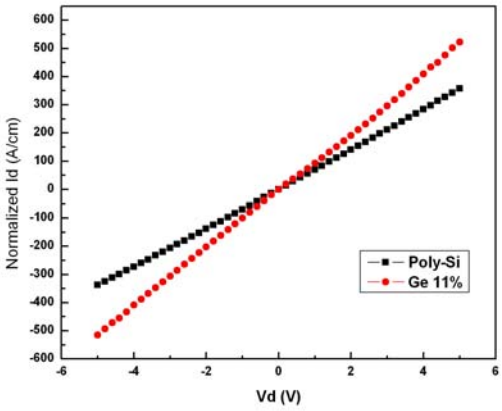


Fig 3.35 The Id-Vd is normalized of the L=15 μm which the Vg is fixed at –10V.. It is obvious that the current of SiGe nanowire is higher.

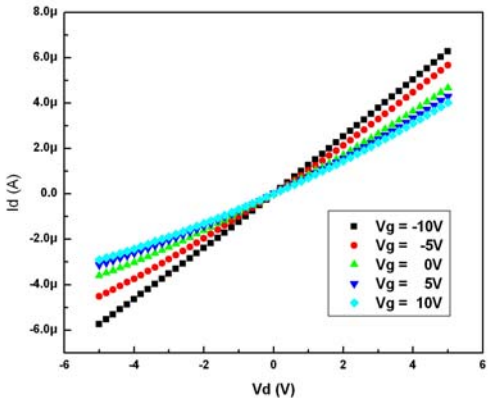


Fig 3.36 The Id-Vd of the **$Si_{0.89}Ge_{0.11}$** nanowire with the length **L=30 μm** after S/D and Channel Ion Implantation.

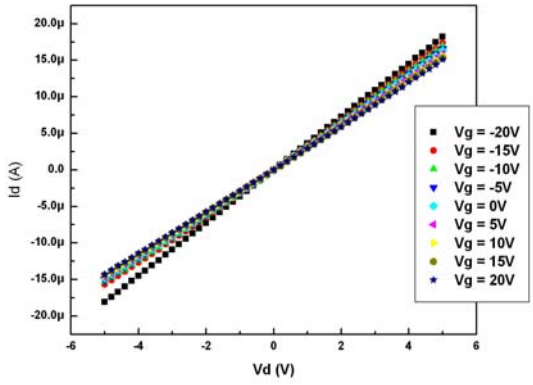


Fig 3.37 The Id-Vd of the **Poly-Si** nanowire with the length **L=30 μm** after S/D and Channel Ion Implantation.

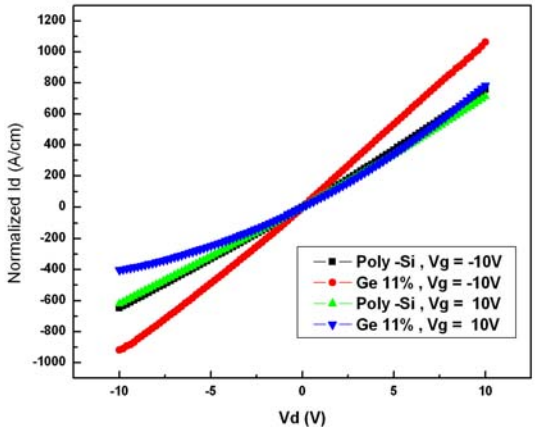


Fig 3.38 The Id-Vd is normalized which the Vg is fixed at 10V and –10V. It is obvious that the current of SiGe nanowire is higher.

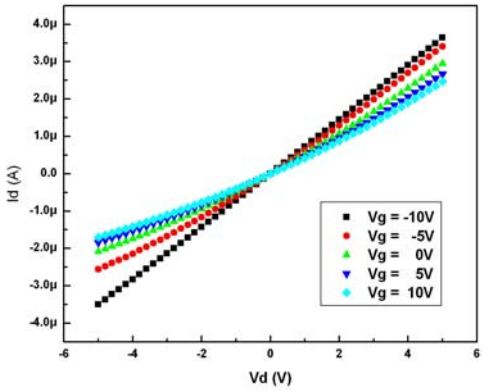


Fig 3.39 The Id-Vd of the **$Si_{0.89}Ge_{0.11}$** nanowire with the length **L=50 μm** after S/D and Channel Ion Implantation.

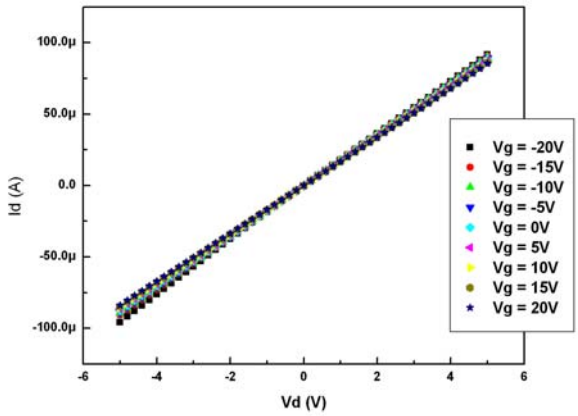


Fig 3.40 The Id-Vd of the **Poly-Si** nanowire with the length **L=5 μm** after S/D and Channel Ion Implantation.

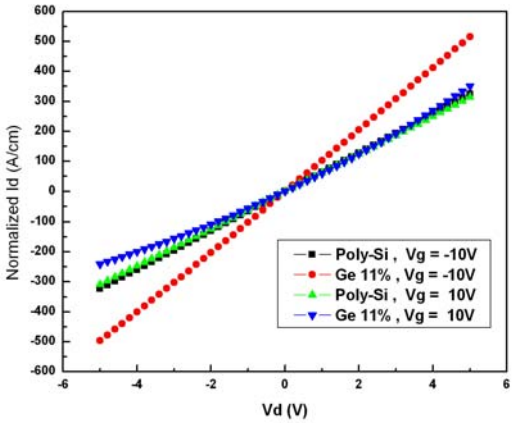


Fig 3.41 The Id-Vd is normalized which the Vg is fixed at 10V and –10V. It is obvious that the current of SiGe nanowire is higher.

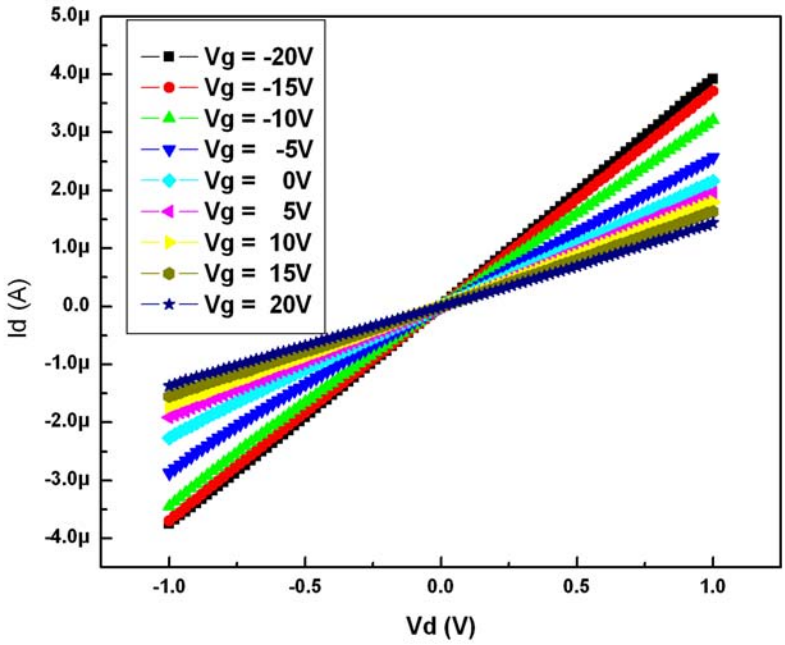


Fig 3.42 The Id-Vd measured from –1V to 1V with different Vg change from –20V to 20V of the **$Si_{0.89}Ge_{0.11}$** nanowire with the length **L=10 μm** after S/D and Channel Ion Implantation.

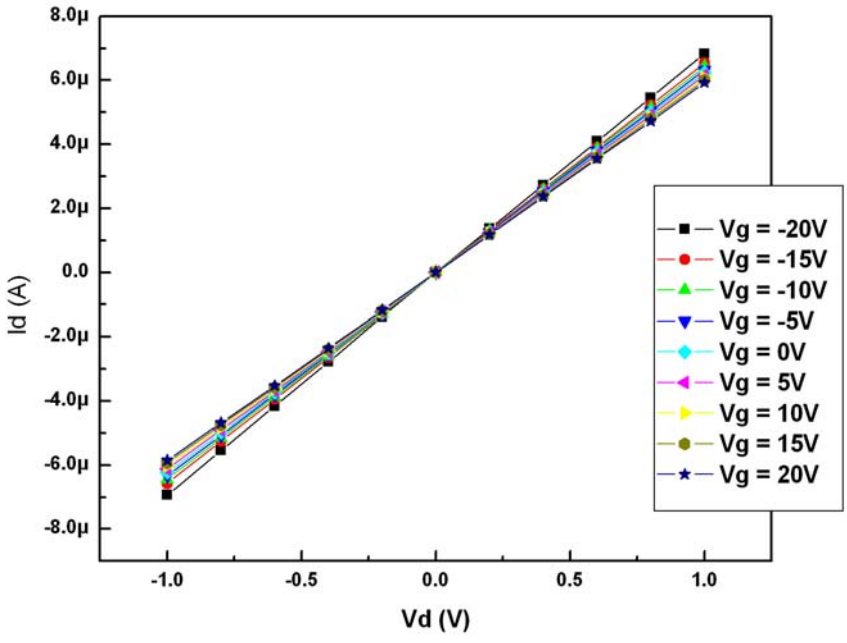


Fig 3.43 The Id-Vd measured from –1V to 1V with different Vg change from –20V to 20V of the Poly nanowire with the length **L=15 μm** after S/D and Channel Ion Implantation.

(The unit of the normalized current was A/V・cm)

	Length	Area	All Implant	S/D Implant
Poly-Si	L=2 μm	13839 nm^2	**63.3**	0.915
	L=15 μm	13839 nm^2	**71.54**	0.918
	L=30 μm	13839 nm^2	**73.27**	0.962
	L=50 μm	13839 nm^2	**64.96**	-
$Si_{0.89}Ge_{0.11}$	L=2 μm	3528 nm^2	**99.1**	7.256
	L=15 μm	3528 nm^2	**104.59**	7.201
	L=30 μm	3528 nm^2	**106.8**	6.732
	L=5 μm	3828 nm^2	**103.17**	-

Table 5. The diagram list the current after S/D and Channel ion implantation then anneal at T=950℃ for 30 min. Each term of the current was improved by the process

(The unit of the normalized current was A/V・cm)

	Intrinsic	Heat Treatment	Source/Drain Implantation	S/D, channel Implantation
Poly-Si	0.01147	0.4	0.915	63.31
	0.01312	-	0.918	71.54
	-		0.962	73.27
	-		-	64.96
Ave.	**0.0123**	**0.4**	**0.932**	**68.27**
$Si_{0.93}Ge_{0.07}$	0.01773	0.814	-	-
	0.01872		-	-
Ave.	**0.01833**	**0.814**	-	-
$Si_{0.89}Ge_{0.11}$	0.1178	2.845	7.256	99.1
	0.1168		7.201	104.6
	-		6.732	106.8
	-		-	103.17
Ave.	**0.1173**	**2.845**	**7.062**	**103.42**
$Si_{0.8}Ge_{0.2}$	-		-	-

Table 6. The table summary all the all we measured. The worlds in bold line are the average normalized current.

	Intrinsic	Heat Treatment	Source/Drain Implantation	S/D, channel Implantation
$Si_{0.89}Ge_{0.11}$	0.1173	2.845	7.062	103.42
Poly-Si	0.0123	0.4	0.932	68.27
ratio	**9.537**	**7.113**	**7.578**	**1.515**

Table 7 The table compare the two average normalized current. The effect improvement of the SiGe is getting lower.

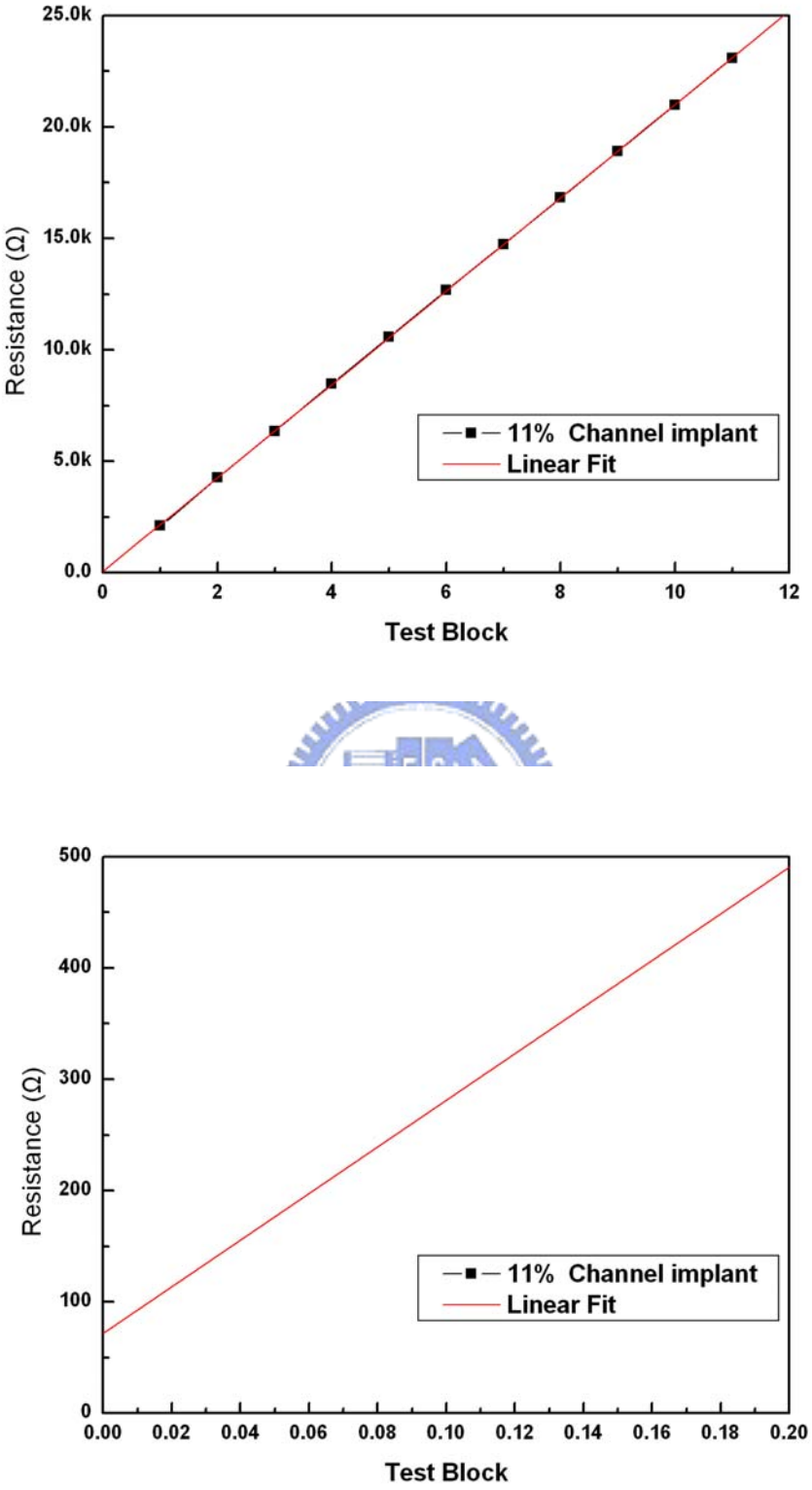


Fig 3.44 The Resistance-Length of the $Si_{0.89}Ge_{0.11}$ nanowire after S/D Ion Implantation. The test block is the which one contact pad. And from the extrapolation, we could get the contact resistance is **71.57Ω**

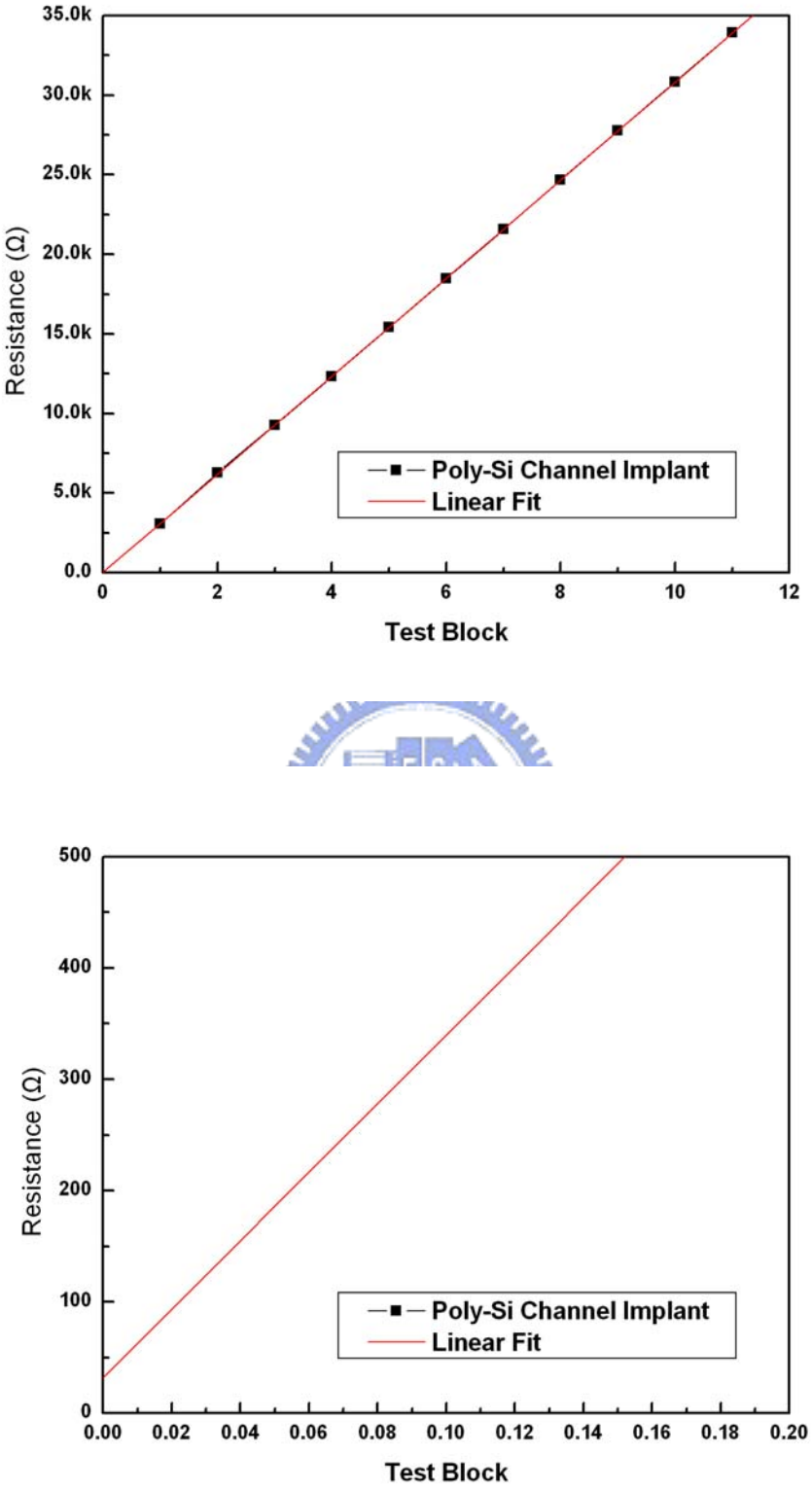


Fig 3.45 The Resistance-Length of the **Poly-Si** nanowire after S/D Ion Implantation. The test block is the which one contact pad. And from the extrapolation, we could get the contact resistance is **31.702Ω**

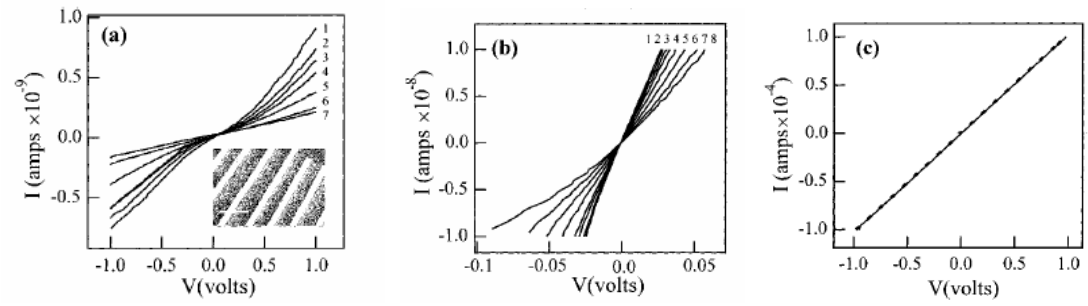


Fig 3.46 (a) I-V on a 70 nm diameter. No doping (sweep –30V to 30V)
(b) I-V on a 150 nm diameter. SiH4:B2H6=1000:1 (sweep -20V to 20V)
(c) I-V on a 150 nm diameter. SiH4:B2H6=2:1 (sweep 20V , 0V)