國 立 交 通 大 學

電子工程學系　電子研究所

碩 士 論 文

1.8伏金氧半低雜訊放大器之設計應用於超寬頻UWB 3.1-10.6GHz無線接收端

Design of a 1.8 -V CMOS LNA applied for Ultra-Wideband 3.1 to 10.6GHz Wireless Receivers

研究生: 邱子倫

指導教授: 荊鳳德 博士

中華民國九十五年六月

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摘要

本論文研製一個應用於超寬頻 3.1-10.6 GHz 的低雜訊放大器。本研究是以 0.18 微米互補式金氧半製程實現。此低雜訊放大器是以共源極和共閘極疊接為放大器主架構，在共源極電晶體的閘極和源極兩端外加電容，在不增加電晶體的大小下，補足濾波器所需電容值，達到低功率消耗的設計原則，並用一電容與源極電感並聯，能減少源極電感對高頻響應的降低，用三階帶通柴比雪夫濾波器做輸入匹配，而在輸出端是用共汲極電壓緩衝器做匹配，為了能在所應用的頻段內達到相對的平坦增益，在疊接放大器中利用 shunt peaking 的方法去實現。供應電壓 V_{DD} 為 1.8 伏特時，整個電路功率消耗約為 18mW，及包含 pad 的情況下整個電路大小約為 0.992 mm^2。本研究的低雜訊放大器所量測的規格，順向增益(S_{21})在 3.1-10.6GHz 時為 6dB-9.7dB，逆向隔離(S_{12})為-20dB 以下，S11 平均為-7dB 以下，S22 平均為-10dB 以下，平均雜訊指數為 7dB，而線性度參數 IIP3 為 6dBm。

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Abstract

A low noise amplifier is applied for ultra-wideband. This research is fabricated in 0.18-μm CMOS process. The three-order band-pass Chebyshev filter can reach the broadband input impedance matching. Owing to the low power consideration, plus the additional gate capacitor C_p. The cacoded structure gain stage provides the gain of the amplifier. The capacitor C_s reduces the gain degradation caused by L_s at high frequency. The inductive shunt peaking maintain the gain flatness. Output buffer is used for output broadband matching. The low noise amplifier introduces the shunt peaking to achieve the flat gain purpose. The total power dissipation of the chip is about 18 mW at power supply 1.8 volt. The chip size included pad is 0.992 mm^2. The measurement result of this study expect that the forward gain S_{21} is 6 to 9.7dB at 3.1-10.6GHz, the reverse isolation S_{12} is under -20dB, the average S_{11} is under -7 dB, the average S_{22} is under -10dB, the noise figure minimum is 6dB, and IIP3 is 6dBm.

誌　謝

謹向指導老師 荊鳳德 教授致上最大謝意，老師對研究的熱誠態度影響了實驗室的每個同學，在老師的指導下，也讓本篇論文得以順利完成。

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最後要感謝我的父母，致上最深的敬意，感謝他們對我的栽培，不斷的在成長的路上鼓勵我，這一路上的支持，才有今天的我。還有我的女友依廷小美仔，是我最大的精神支柱，在我心情鬱悶時，總是及時的給我打氣加油，使我能支撐下去，讓我有完成碩士學業的動力。

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CHAPTER 1

Introduction

1.1 Motivation

Recently , commercial wireless communication systems at gigahertz frequencies have been expanded extensively. Due to the advancement of integrated circuit design technology, circuit size is miniaturized and cost down considerations. Therefore, CMOS technology is attractive due to its advantages of high-level integration, low cost, and enhancing performance by scaling. The prospect of a single chip CMOS system has received considerable interest. Although the SOC is hard to implement at this moment, but a set of separating chips in the same CMOS technology may bring significant economic profit.

The interest in Ultra-wideband (UWB) system for wireless communication application has increased significantly. The US Federal Communications Commission (FCC) approval of UWB has prompted the IEEE 802.15.3a standards committee to establish a new physical layer standard utilizing the frequency spectrum from 3.1-GHz to 10.6GHz for consumer electronics applications. One of the proposed leading standards for UWB spectrum allocation is a multi-band with frequency hopping between these bands. The UWB frequency band is divided into several

sub-bands and each bandwidth has 528MHz. The modulation scheme is Multi band-OFDM [6]. Main application of UWB is short distance about 10 meters and high-speed wireless communication. UWB has very high data rate from 110M to 480M bps (bit per second). Otherwise, another advantage of UWB is the low power consumption.

The direct down-conversion receiver becomes more attractive since it has the advantages of low power, low complexity, and less extra components. And it lets system-on-chip (SOC) become possible. Typical, the first stage of the receiver is a low noise amplifier (LNA), which provides high gain and low noise to suppress the overall system's noise performance. To implement the broadband LNA is the main object of this thesis.

1.2 Thesis Organization

The chapter 2 presents the basic concepts of RF design. These basic concepts which include the introduction of receiver architecture, linearity and noise provide the guidance for RF circuit design. The chapter 3 discusses the basic low-noise amplifiers design for UWB and other broadband amplifiers. In the chapter 4, a UWB LNA with wideband input matching network by using third-order Chebyshev filter is designed. Measurement result of the LNA chip fabricated by TSMC 0.18um CMOS technology is discussed. In the chapter 5, this work is summarized and concluded.

▪ CHAPTER 2

Basic Concepts in RF Design

2.1 Receiver Architecture

2.1.1 Homodyne Receiver

The homodyne receiver is also called “direct-conversion” or “zero-IF” architecture, since the RF signal is directly down-converted to the baseband in the first downconversion. In the homodyne receiver, the LO frequency is equal to the input carrier frequency, and channel selection requires only a low-pass filter with relatively sharp cutoff characteristics. The simple homodyne architecture is shown in Figure 2-1. But quadrature outputs are needed for frequency and phase-modulated signals, since the two sides of FM or QPSK spectra carry different information.

In recent years, this architecture becomes the topic of active research gradually due to the following reasons:

(1) The problem of image is removed due to $\omega_{IF} = 0$. Therefore no image filter is required, and the LNA need not drive a 50-ohm load.

(2) It is attractive for monolithic integration because this architecture needs less external components.

For the above reasons, this architecture is suitable for low-power and single-chip

design. But some extra issues that do not exist or are not as serious in a heterodyne receiver must be entailed, such as channel selection, DC offset, I/Q mismatch, even-order distortion, and flicker noise.

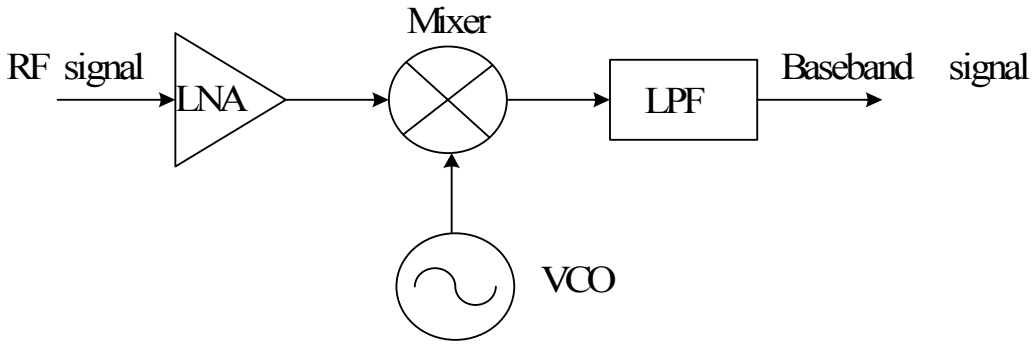


Figure 2-1 Simple homodyne receiver architecture.

2.1.2 Heterodyne Receiver

In heterodyne architectures, the signal band is translated into much lower frequencies by down-conversion mixer, and the filters are used to select the band and channel of the interested signals. In general, the low noise amplifier is placed in front of the down-conversion mixer, since the noise of the down-conversion mixer is high. A simple heterodyne architecture is shown in Figure 2-2. This architecture is the most reliable reception technique today. But if the cost, complexity, integration and power dissipation are the primary criteria, the heterodyne receiver will become unsuitable due to its complexity and the need for a large number of external components.

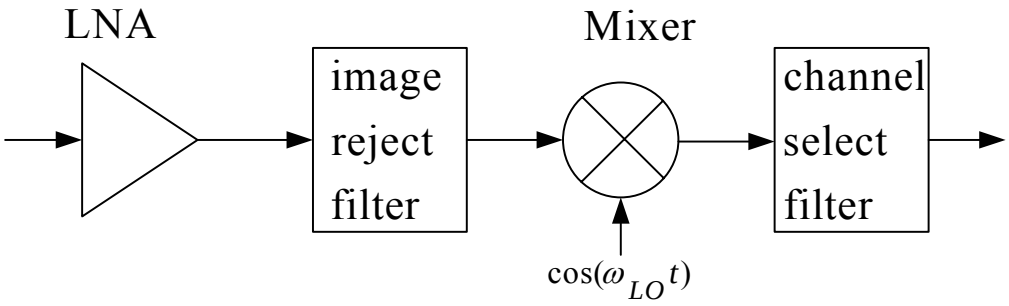


Figure 2-2 Simple heterodyne receiver architecture.

Frequency planning is an important thing in heterodyne receiver. For high-side injection, an undesired signal (image) at a frequency of $\omega_{IM} = \omega_{LO} + (\omega_{LO} - \omega_{RF})$ is translated into the same frequency, intermediate frequency (IF), as the desired signal. Similarly, for low-side injection, the image frequency is at $\omega_{IM} = \omega_{LO} - (\omega_{RF} - \omega_{LO})$. Therefore the image would cause the distortion of the signal at the intermediate frequency. As shown in Figure 2-3, some techniques are necessary to suppress the image, such as image reject filter. How to choose the intermediate frequency? If $2\omega_{IF}$ is sufficiently large, the image reject filter will have a relatively small loss in the signal band and a large attenuation in the image band. But a lower $2\omega_{IF}$ will release the quality factor of the channel select filter to get great suppression of nearby interferers. Therefore we must take a trade-off between image rejection and channel selection.

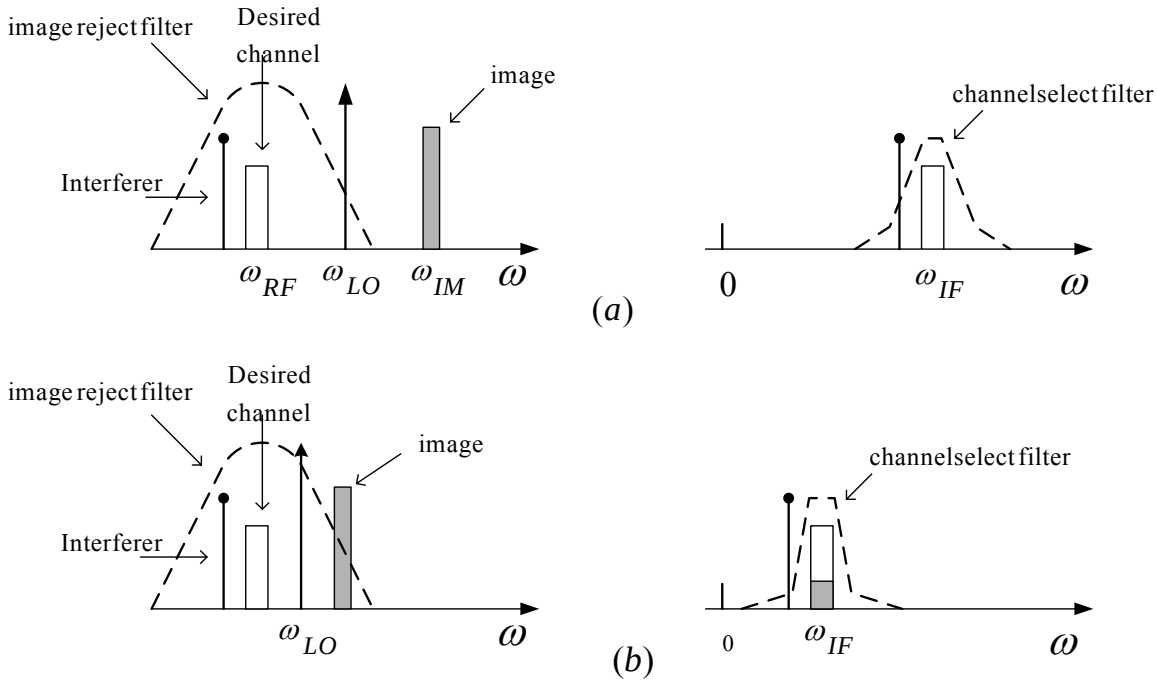


Figure 2-3 Rejection of image versus suppression of interferers.

2.2 Linearity Basic

The nonlinearity of the system often leads to interesting and important phenomena, such as harmonics, gain compression, desensitization, blocking, cross modulation, intermodulation, etc. These distortions will degrade the performance of the system.

When two signals with different frequencies are applied to a nonlinear system, the output exhibits some components that are not harmonics of the input frequencies in general. This is called intermodulation (IM), and this phenomenon arises from multiplication of the two signals when their sum is raised to a power greater than unity. We assume that

$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \tag{2.1}$$

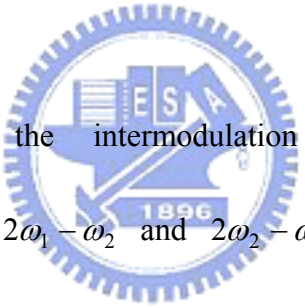
Thus,

$$\begin{aligned} y(t) = {} & \alpha_1 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + \alpha_2 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 \\ & + \alpha 3 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 \end{aligned} \tag{2.2}$$

Expanding the left side and discarding DC terms and harmonics, we obtain the intermodulation products:

$$\omega \to 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 {A_1}^2 A_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 {A_1}^2 A_2}{4} \cos(2\omega_1 - \omega_2)t \tag{2.3}$$

$$\omega \to 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 {A_2}^2 A_1}{4} \cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 {A_2}^2 A_1}{4} \cos(2\omega_2 - \omega_1)t \tag{2.4}$$



Furthermore, among the intermodulation products, the third-order intermodulation products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ is important. Since if the difference between ω_1 and ω_2 is small, the distortions at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ will appear in the vicinity of ω_1 and ω_2.

$$IM_3 = \frac{3}{4} A_2^2 \left| \frac{H_3(-j\omega_1, j\omega_2, j\omega_2)}{H_1(j\omega_1)} \right| \tag{2.5}$$

This effect causes some distortion at our desired frequency and damages desired signals. Therefore third intercept point (IP3) is used to characterize this behavior. This parameter is measured by supplying a two-tone signal to the system. This input signal must be chosen to be sufficiently small in order to remove higher-order nonlinear terms. In a typical test, A_1=A_2=A, hence the magnitude of third-order intermodulation

products grows at three times the rate at which the fundamental signal on a logarithmic scale when input signal increases. The third-order intercept point is defined to be the point at which third-order intermodulation product equals to the fundamental signal, and the corresponding input signal is called input IP3 (IIP3) and the corresponding output signal is called output IP3 (OIP3). The A_{IP3}, therefore, can be obtained by setting $IM_3 = 1$ and expressing as

$$A_{IP3}^2 = \frac{4}{3}\left|\frac{H_1(j\omega_1)}{H_3(-j\omega_1, j\omega_2, j\omega_2)}\right| \tag{2.6}$$

Besides, a quick method of measuring IIP3 is as follows. As shown in Figure 2-4, If the power of the two-tone signal, P_{in}, is small enough to ignore higher order nonlinear terms, then IIP3 can be expressed as

$$IIP_3\,|_{dBm} = \frac{\Delta P\,|_{dB}}{2} + P_{in}\,|_{dBm} \tag{2.7}$$

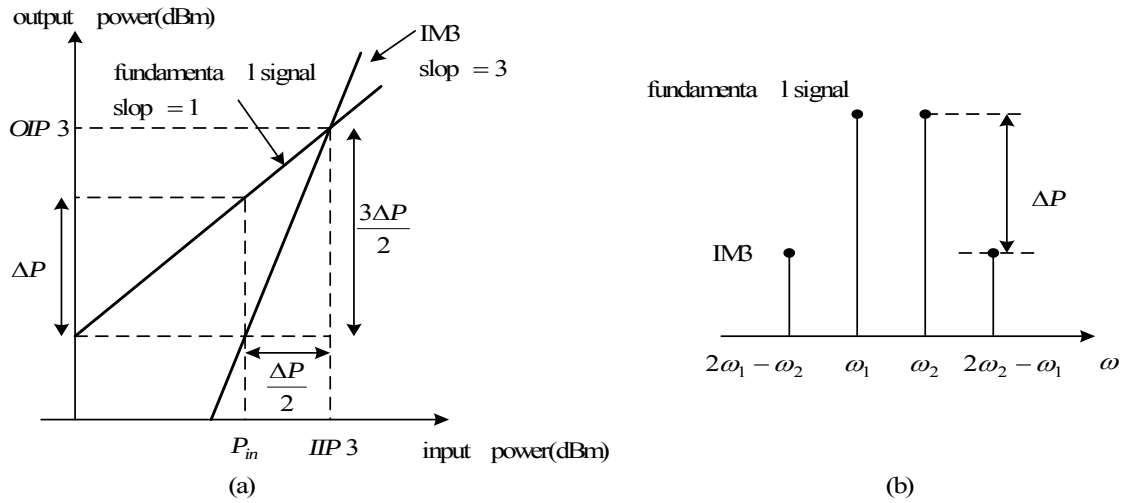


Figure 2-4 (a) Growth of output components in an intermodulation test
(b) Intermodulation distortion.

2.3 Noise Basic

Noise can be loosely defined as any random interference unrelated to the signal of interest, and noise is characterized by a PDF and a PSD. In analog circuits, the signal-to-noise ratio (SNR), defined as the ratio of the signal power to the total noise power, is an important parameter. But in RF design, most of the front-end receiver blocks are characterized in terms of their noise figure, which is a measure of SNR degradation due to the added noise from the circuit/system, rather than the input-referred noise. Noise factor can be expressed as

$$\text{noise factor} = \frac{\text{total output noise power}}{\text{output noise power due to input source}} \tag{2.8}$$

the noise figure (NF) is simply the noise factor expressed in decibels. If a system has no noise, then noise figure is 0 dB regardless of the gain. In reality, the finite noise of a system degrades the SNR, yielding noise figure > 0 dB. For those whose noise factor is quite close to unity, noise temperature, T_N, is an alternative way of expressing the effect of noise contribution due to its higher-resolution description of noise performance, and is defined as the increase in temperature required of the source resistance for it to account for all of the output noise at the reference temperature T_{ref} (which is 290 K). It is related to the noise factor as follows:

$$\text{noise factor} = 1 + \frac{T_N}{T_{ref}} \Rightarrow T_N = T_{ref} \cdot (\text{noise factor} - 1) \tag{2.9}$$

2.3.1 Noise Source

Thermal noise:

Thermally agitated charge carriers in a conductor constitute a randomly varying current that gives rise to a random voltage due to their Brownian motion. Thermal noise is often called Johnson noise or Nyquist noise. The noise voltage has a zero average value, but a nonzero mean-square value.

In a resistor R, thermal noise can be represented by a series noise voltage source $\overline{v_n^2} = 4kTR\Delta f$ or by a shunt noise current source $\overline{i_n^2} = \frac{4kT\Delta f}{R}$, where k is k is Boltzmann's constant (about 1.38×10^{-23} J/K), T is the absolute temperature in Kelvins, and Δf is the noise bandwidth. However, purely reactive elements generate no thermal noise.

Shot Noise:

Shot noise occurs in PN junctions, and two conditions for shot noise to occur:

(1) There must be direct current flow.

(2) There must be energy barrier over which a charge carrier hops.

Charge comes in discrete bundles. The randomness of the arrival time gives rise to the whiteness of shot noise. Therefore the shot noise can be modeled by a shunt noise current source $\overline{i_n^2} = 2qI_{DC}\Delta f$, where q is the electronic charge, I_{DC} is the DC current in amperes, and Δf is the noise bandwidth in hertz.

Flicker Noise:

Flicker noise appears as 1/f character and is found in all active devices, as well as in some discrete passive element such as carbon resistors. In diodes, flicker noise is caused by traps associated with contamination and crystal defects in the depletion regions. The traps capture and release carriers in a random fashion and the time constants associated with the process give rise to the 1/f nature of the noise power density. The flicker noise in diode can be represented as $\overline{i_j^2} = \frac{K}{f} \cdot \frac{I}{A_j} \cdot \Delta f$, where K is the process-dependent constant, A_j is the junction area, and I is the bias current. In MOSFET, charge trapping phenomena are invoked in surface, and his type of noise is much greater than that of the bipolar transistor. The flicker noise in MOSFET can be given by

$$\overline{i_n^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f \approx \frac{K}{f} \cdot \omega_T^2 \cdot A \cdot \Delta f \qquad (2.10)$$

where K is the process-dependent constant, and A is the area of the gate.

2.3.2 Noise Model of MOSFET

The dominant noise source in CMOS devices is channel noise, which basically is thermal noise originated from the voltage-controlled resistor mechanism of a MOSFET. This source of noise can be modeled as a shunt current source in the output circuit of the device. The channel noise of MOSFET is given by

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \qquad (2.11)$$

where γ is bias-dependent factor, and g_{d0} is the zero-bias drain conductance of the device. Another source of drain noise is flicker noise and is given by equation 2.10. Hence, the total drain noise source is given by

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f + \frac{K}{f}\cdot\frac{g_m^2}{WLC_{ox}^2}\cdot\Delta f \tag{2.12}$$

At RF frequencies, the thermal agitation of channel charge leads to a noisy gate current because the fluctuations in the channel charge induce a physical current in the gate terminal due to capacitive coupling. This source of noise can be modeled as a shunt current source between gate and source terminal with a shunt conductance g_g, and may be expressed as

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \tag{2.13}$$

where the parameter g_g is shown as

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \tag{2.14}$$

and δ is the gate noise coefficient. This gate noise is partially correlated with the channel thermal noise because both noise currents stem from thermal fluctuations in the channel, and the magnitude of the correlation can be expressed as

$$c \equiv \frac{\overline{i_g \cdot i_d^*}}{\sqrt{\overline{i_g^2}\cdot\overline{i_d^2}}} \approx 0.395\,j \tag{2.15}$$

where the value of 0.395j is exact for long channel devices. Hence, the gate noise can be re-expressed as

$$\overline{i_{ng}^2} = \overline{(i_{ngc} + i_{ngu})^2} = 4kT\delta g_g \Delta f \mid c \mid^2 + 4kT\delta g_g \Delta f (1 - \mid c \mid^2) \qquad (2.16)$$

where the first term is correlated and the second term is uncorrelated to channel noise. From previous introduction of MOSFET noise source, a standard MOSFET noise model can be presented in Figure 2-5, where $\overline{i_{nd}^2}$ is the drain noise source, $\overline{i_{ng}^2}$ is the gate noise source, and $\overline{v_{rg}^2}$ is thermal noise source of gate parasitic resistor r_g.

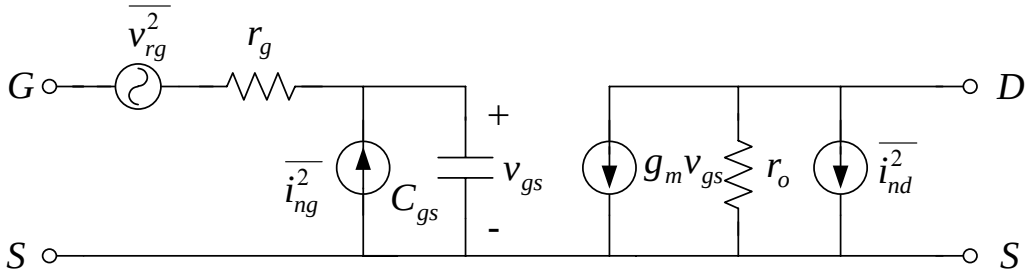


Figure 2-5 A standard noise model of MOSFET.

2.3.3 Noise Figure of Cascaded Stages

For a cascade of m stages, the overall noise figure can be characterized by Friis formula

$$NF_{total} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \ldots + \frac{NF_m - 1}{A_{p(m-1)}} \qquad (2.17)$$

where NF_n is the noise figure of stage n, and A_{pn} denotes the power gain of stage n. This equation indicates that the noise contributed by each stage decreases as the gain preceding the stage increases. Hence, the first few stages in a cascade are the most critical for noise figure. But if a stage exhibits attenuation, then the noise figure of the following circuit is amplified when referred to the input of that stage [5].

CHAPTER 3

General Consideration in LNA Circuit Design

3.1 Low Noise Amplifier Basic

Low noise amplifier is the first gain stage in the receive path so its noise figure directly adds to that of the system. Therefore, there are several common goals in the design of LNA. These include minimizing noise figure of the amplifier, providing enough gain with sufficient linearity and providing a stable 50 ohm input impedance to terminate an unknown length of transmission line which delivers signal from antenna to the amplifier [9]. Among LNA architectures, inductive source degeneration is the most popular method since it can achieve noise and power matching simultaneously, as shown in Figure 3-1. The following analysis after 3.1.3 is based on this architecture. The LNA basic considerations are introduced as follows.

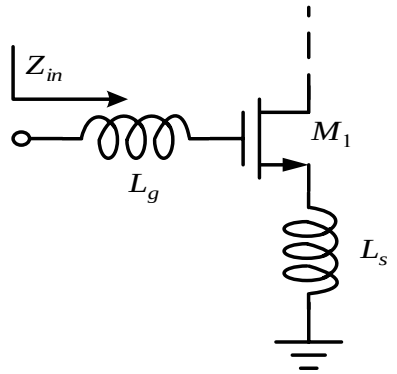


Figure 3-1 Common-source input stage with inductive source degeneration.

3.1.1 Impedance Matching Network

The need for impedance matching network becomes more important. In order to deliver maximum power to a load, must be properly terminated at both the input and the output ports. The input impedance of a circuit can be any values. In order to have the best power transfer into the circuit, it is necessary to match this impedance to the impedance of the source driving the circuit. The output impedance must be similarly matched. In order to deliver maximum power to the 50 ohm load, must have the terminations Z_S and Z_L. The input matching network is designed to transforms the generator impedance to the source impedance Z_S, and the output matching network transforms the 50 ohm termination to the load impedance Z_L. Consider the RF system shown in Figure 3-2. Here the source and load terminations are 50ohm, as are the transmission lines leading up to the circuit for optimum power transfer, prevention of ringing and radiation, and good noise behavior. For example, we needs the circuit input and output impedances matched to the system. In general, some matching circuit must almost always be added to the circuit, as shown in Figure 3-3. Typically, reactive matching circuits are used because they are lossless and because they do not add noise to the circuit. Note that, in general, when an impedance is complex $(R + jX)$. Then to match it, the impedance must be driven from its complex conjugate $(R - jX)$.

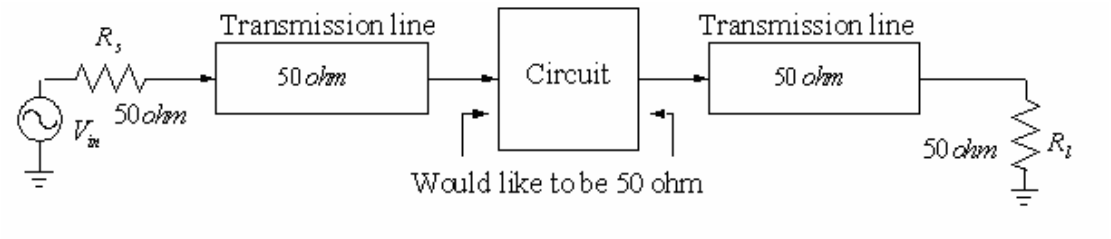


Figure 3-2 Circuit embedded in a 50 ohm system.

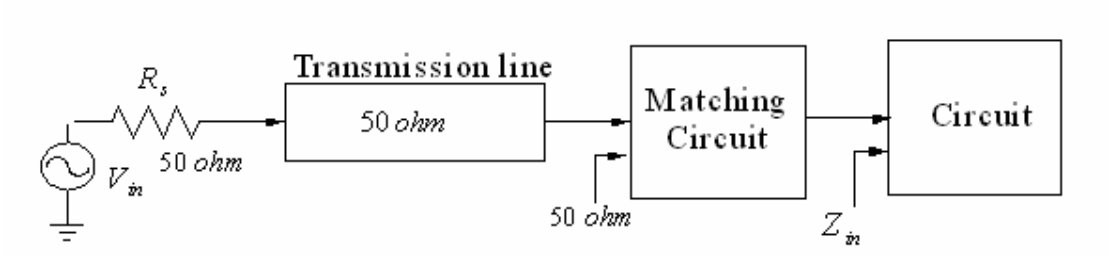


Figure 3-3 Circuit embedded in a 50 ohm system with matching circuit.

3.1.2 Stability

The stability of an amplifier is a very important consideration in a design and can be determined from the S parameters, the matching networks, and the terminations. A two-port network to be unconditionally stable can be derived from (3.1) to (3.4).

$$\left|\Gamma_s\right| < 1 \tag{3.1}$$

$$\left|\Gamma_L\right| < 1 \tag{3.2}$$

$$\left|\Gamma_{IN}\right| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right| < 1 \tag{3.3}$$

$$\left|\Gamma_{OUT}\right| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_S}\right| < 1 \tag{3.4}$$

The two-port network is shown in Figure 3-4. For unconditional stability any passive load or source in the network must produce a stable condition. The solution of (3.1) to (3.4) gives the required conditions for the two-port network to be unconditionally stable. [4]

$$k = \frac{1 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2 + \left|\Delta\right|^2}{2\left|S_{12}S_{21}\right|} \tag{3.5}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.6}$$

A convenient way of expressing the necessary and sufficient conditions for unconditional stability is

$$k > 1 \tag{3.7}$$

$$\left|\Delta\right| < 1 \tag{3.8}$$

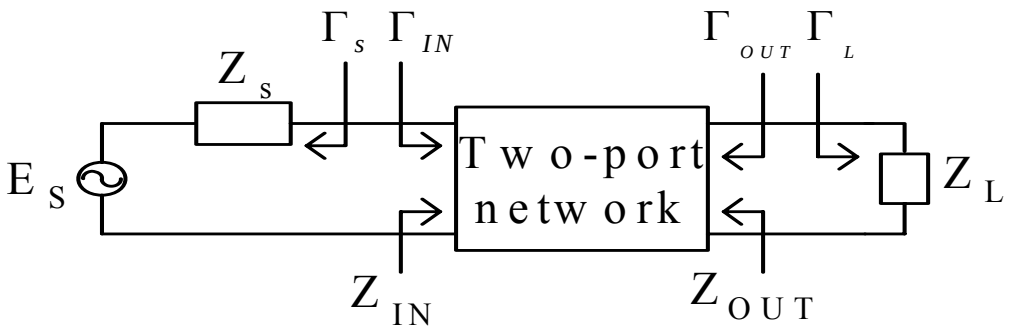


Figure 3-4 Stability of two-port networks.

3.1.3 Low Noise Amplifier Architecture Analysis

In Figure 3-5, the input impedance can be expressed as

$$\begin{aligned} Z_{in} &= s(L_g + L_s) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s \\ &= \left(\frac{g_m}{C_{gs}}\right)L_s \approx \omega_T L_s \quad at \quad \omega = \omega_o = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \end{aligned} \tag{3.9}$$

as shown in equation (3.9), the input impedance is equal to the multiplication of cutoff frequency of the device and source inductance at resonant frequency. Therefore it can be set to 50 ohm for input matching while resonant frequency is designed to be equal to the operating frequency.

According to prior introduction, the equivalent noise model of common-source LNA with inductive source degeneration can be expressed as Figure 3-5, where R_l is the parasitic resistance of the inductor, R_g is the gate resistance of the device. Note that the overlap capacitance C_{gd} has also been neglected in the interest of simplicity. Then the noise figure can be obtained by computing the total output noise power and output noise power due to input source. To find the output noise, we first evaluate the trans-conductance of the input stage. With the output current proportional to the voltage no C_{gs} and noting that the input circuit takes the form of series-resonant network, the transconductance at the resonant frequency can be expressed as

$$G_m = g_m Q_{in} = \frac{g_m}{\omega_o C_{gs}(R_s + \omega_T L_s)} = \frac{\omega_T}{2\omega_o R_s} \tag{3.10}$$

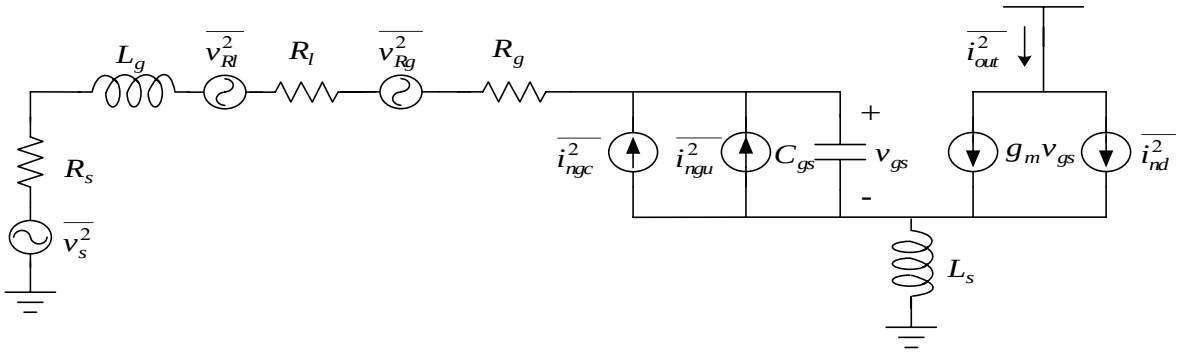


Figure 3-5 Equivalent noise model of Figure 3-1.

where Q_{in} is the effective Q of the amplifier input circuit. So the output noise power density due to the source can be expressed as

$$S_{a,Rs}(\omega_o) = S_{Rs} G_{m.eff}^2 = \frac{4kT\omega_T^2}{\omega_o^2 R_s (1+\frac{\omega_T L_s}{R_s})^2} \tag{3.11}$$

In the similar way, the output noise power density due to R_g and R_l is

$$S_{a,R_g,R_l}(\omega_o) = \frac{4kT(R_g + R_l)\omega_T^2}{\omega_o^2 R_s^2 (1+\frac{\omega_T L_s}{R_s})^2} \tag{3.12}$$

Furthermore, channel current noise of the device is the dominant noise contributor, and its noise power density associated with the correlated portion of the gate noise can be expressed as

$$S_{a,i_{nd},i_{ngc}}(\omega_o) = \frac{4kT\gamma\kappa g_{do}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{3.13}$$

where γ is the coefficient of channel thermal noise, $\alpha = g_m / g_{d0}$ and

$$\kappa = \frac{\delta\alpha^2}{5\gamma}|c|^2 + \left[1 + |c| Q_L \sqrt{\frac{\delta\alpha 2}{5\gamma}}\right]^2 \tag{3.14}$$

$$Q_L = \frac{1}{\omega_o R_s C_{gs}} \tag{3.15}$$

The last noise term is the contribution of the uncorrelated portion of the gate noise, and its output noise power density can be expressed as

$$S_{a,i_{ngu}}(\omega_o) = \frac{4kT\gamma\xi g_{do}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{3.16}$$

where

$$\xi = \frac{\delta\alpha^2}{5\gamma}(1-|c|^2)(1+Q_L^2) \tag{3.17}$$

According to equations (3.11), (3.12), (3.13) and (3.16), the noise figure at the resonant frequency can be expressed as

$$F = 1+\frac{R_l}{R_s}+\frac{R_g}{R_s}+\frac{\gamma\chi}{\alpha Q_L}\left(\frac{\omega_o}{\omega_T}\right) \tag{3.18}$$

where

$$\chi = 1+2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}+\frac{\delta\alpha^2}{5\gamma}(1+Q_L^2) \tag{3.19}$$

From equation (3.19), we observe that χ includes the terms which are constant, proportional to Q_L, and proportional to Q_L^2. It follows that equation (3.19) will contain terms which are proportional to Q_L as well as inversely proportional to Q_L. A minimum noise figure, therefore, exits for a particular Q_L.

3.1.4 Optimizations of Low Noise Amplifier Design Flow

The analysis of the previous section can now be drawn upon in designing the LNA. In order to pick the appropriate device size and bias point to optimize noise performance given specific objectives for gain and power dissipation, a simple second-order model of the MOSFET transconductance can be employed which accounts for high-field effects in short channel devices. Assume that the drain current, I_d, has the form

$$I_{DS} = WC_{ox}v_{sat}\frac{(V_{gs}-V_T)}{1+\frac{V_{gs}-V_T}{LE_{sat}}} = WC_{ox}v_{sat}LE_{sat}\frac{\rho^2}{1+\rho} \tag{3.20}$$

where $\rho \equiv \frac{V_{gs}-V_T}{LE_{sat}}$. And the equation (3.15) can be replace as

$$Q_L = \frac{3}{2\omega_o WLC_{ox}R_s} \Rightarrow C_{ox} = \frac{3}{2R_sQ_L\omega_o WL} \tag{3.21}$$

The power consumption of the LNA, therefore, can be expressed as

$$P_D = V_{DD}I_{DS} = \frac{3}{2}V_{DD}\frac{1}{Q_LR_s\omega_o}v_{sat}E_{sat}\frac{\rho^2}{1+\rho} \tag{3.22}$$

The noise figure can be expressed in terms of P_D and V_{gs}. Two parameters linked to power dissipation need to be accounted for.

$$\omega_T \approx \frac{g_m}{C_{gs}} = f_1(V_{gs}) \tag{3.23}$$

$$Q_L = \frac{3V_{DD}v_{sat}E_{sat}}{2P_D\omega_oR_s}\frac{\rho^2}{1+\rho} = \frac{P_o}{P_D}\frac{\rho^2}{1+\rho} = f_2(V_{gs},P_D) \tag{3.24}$$

where $P_o = \frac{3V_{DD}v_{sat}E_{sat}}{2\omega_o R_s}$.

The noise figure of the LNA, therefore, can be expressed as

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha Q_L}\left(\frac{\omega_o}{\omega_T}\right)\left(1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1+Q_L^2)\right) = f(V_{gs}, P_D) \quad (3.25)$$

In general, there are two approaches to optimize noise figure. The first approach assumes a fixed transconductance, G_m. The second approach assumes fixed power consumption.

(1) Fixed G_m optimization: To fix the value of the transconductance, G_m, we need only assign a constant value to ρ. Once ρ is determined, the optimization of the noise figure can be obtained by equation (3.25):

$$\left.\frac{\partial f(V_{gs}, P_D)}{\partial P_D}\right|_{fixed\,Vgs} = 0 \Rightarrow P_{D.opt} \Rightarrow Q_{L.opt} \Rightarrow F = f(V_{gs}, P_{D.opt}) \quad (3.26)$$

From equation (3.21), we can obtain the optimal width to get the minimal noise figure for a given G_m under the assumption of matched input impedance. In this approach, the designer can achieve high gain and low noise performance by selecting the desired transconductance, but its disadvantage is that we must sacrifice the power consumption to achieve minimum noise figure.

(2) Fixed P_D optimization: An alternative method of optimization fixes the power dissipation and adjusts device size and bias point to minimize the noise figure. Once P_D is determined, the optimization of the noise figure can be obtained by

equation (3.27):

$$\left.\frac{\partial f(V_{gs}, P_D)}{\partial V_{gs}}\right|_{fixed\ P_D} = 0 \Rightarrow V_{gs.opt} \Rightarrow Q_{L.opt} \Rightarrow F = f(V_{gs.opt}, P_D) \quad (3.27)$$

Then the optimum device size can be obtained to get the best noise performance for fixed power dissipation. In this approach, the designer can specify the power dissipation and find the optimal noise performance, but its disadvantage is that the transconductance is held up by the optimal noise condition [5].

3.2 Broadband LNA introductions

Figure 3-6 is the LNA circuit schematic. We discuss this circuit step by step from the first stage. First, to make $1/g_m = 50\,ohm$, the g_m value of common gate amplifier is going to be fixed at certain trans-conductance. An additional stage is required to provide sufficient gain over the desired band. A shunt feedback common source amplifier is used in the second stage for this purpose. The first step is the selection of transistor size and bias condition of the M1 to yield $\mathrm{Re}|Z_{11}| = 1/g_m = 50\,ohm$. This ensures input matching condition for wide-band of frequency. But this condition is violated with optimum noise condition. There is a trade-off between noise and impedance matching in the LNA circuit. One of the major problems in the wide bandwidth amplifier design is the limitation imposed by the gain-bandwidth product of the active device. We know that any active device has a

gain roll off at high frequency because of the gate-drain and gate-source capacitance in the transistor. This effect degrades the forward gain as the frequency increases and eventually the transistor stops functioning as an amplifier at the high frequency. Therefore the second design step is the selection of optimal bias point of second stage of LNA so that it operates at its maximum f_T. In addition to this $|S_{21}|$ degradation with frequency other complications that arises in wide-bandwidth amplifier design includes, increase in reverse gain $|S_{12}|$ and noise figure at high frequency. Negative feedback configuration is used to reduce these effects and increase the bandwidth. An inductor L is connected in series with R_f such that after certain frequency the negative feedback decreases in proportion to the S_{21} roll-off. This technique improves gain flatness at high frequency. The load inductance of L_1 and L_2 replace the resistor load which is used conventionally. The magnitude of the inductor's impedance increases as frequency increases. This increase inductor impedance compensates the active device gain degradation that occurs at high frequency [10].

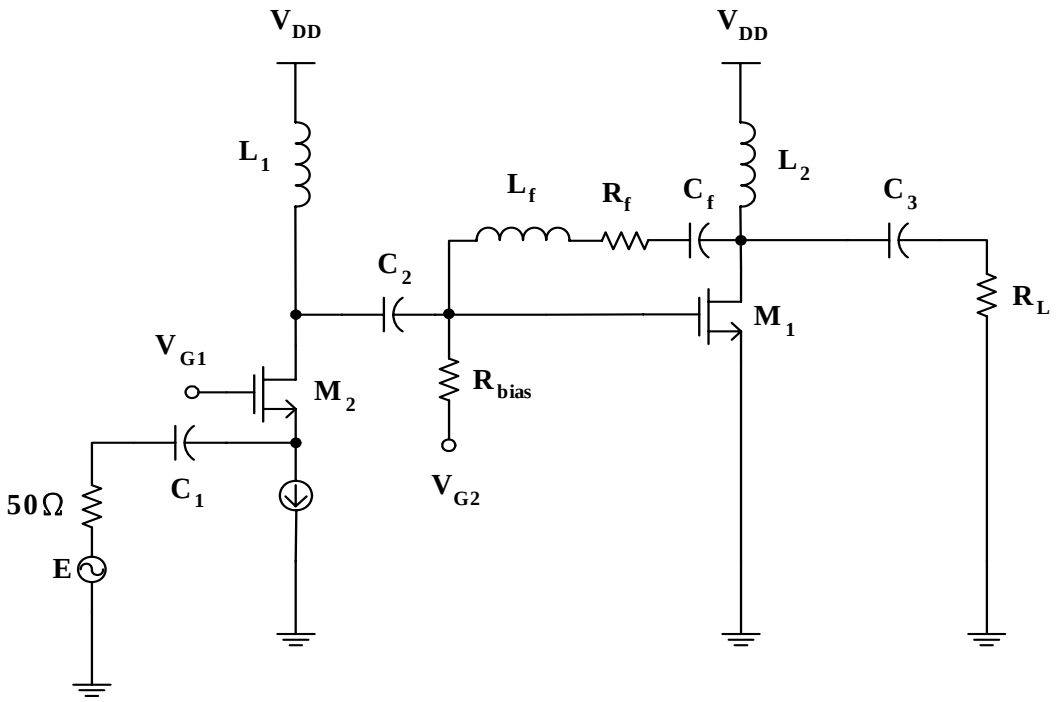


Figure 3-6 Wide-band LNA circuit schematic.

Another circuit topology for wide-band application is distributed amplifier (DA). Distributed amplifier was first introduced by [17]. MMIC DA was mainly implemented using G_aA_s-based or S_iG_e devices. The distributed amplifier schematic is shown in Fig. 3-7. From the Fig. 3-7, we can observe that the power gain of a cascade pair is considerably higher than that of a common-source single transistor. The input signal propagates down the gate line, with each FET tapping off some of the input power. The amplified output signals from the FETs form a traveling wave on the drain line. The propagation constants and lengths of the gate and drain lines are chosen for constructive phasing of the output signals, and the termination impedanc3es on the lines serve to absorb waves traveling in the reverse directions. According to

equivalent circuit of a single unit cell of the gate line and drain line, we can get optimal number of section [3].

$$N_{opt} = \frac{\ln(\alpha_g l_g / \alpha_d l_d)}{\alpha_g l_g - \alpha_d l_d} \tag{3.28}$$

A small resistor R_{gx} is added in the gate of common-gate transistor to improve the entire circuit stability. The input and output impedances of the cascade device are needed. In the DA design, the input and output of the cascade FETs used in the distributed amplifier were terminated by the gate line characteristic impedance Z_{og} and drain line characteristic impedance Z_{od}, respectively. Higher gain can be obtained by choosing higher characteristic impedance of gate (Z_{og}) and drain lines (Z_{od}) but the cutoff frequency will be lower, which will limit the bandwidth. The m-derived matching section is used in our design to overcome the well-known non-constant image impedance from the constant-k sections. A de-embedded m-derived π equivalent circuit is shown in Fig. 3-8. Distributed amplifiers are not capable of very high gains or very low noise figure, however, and generally are larger in size than an amplifier having comparable gain over a narrower bandwidth.

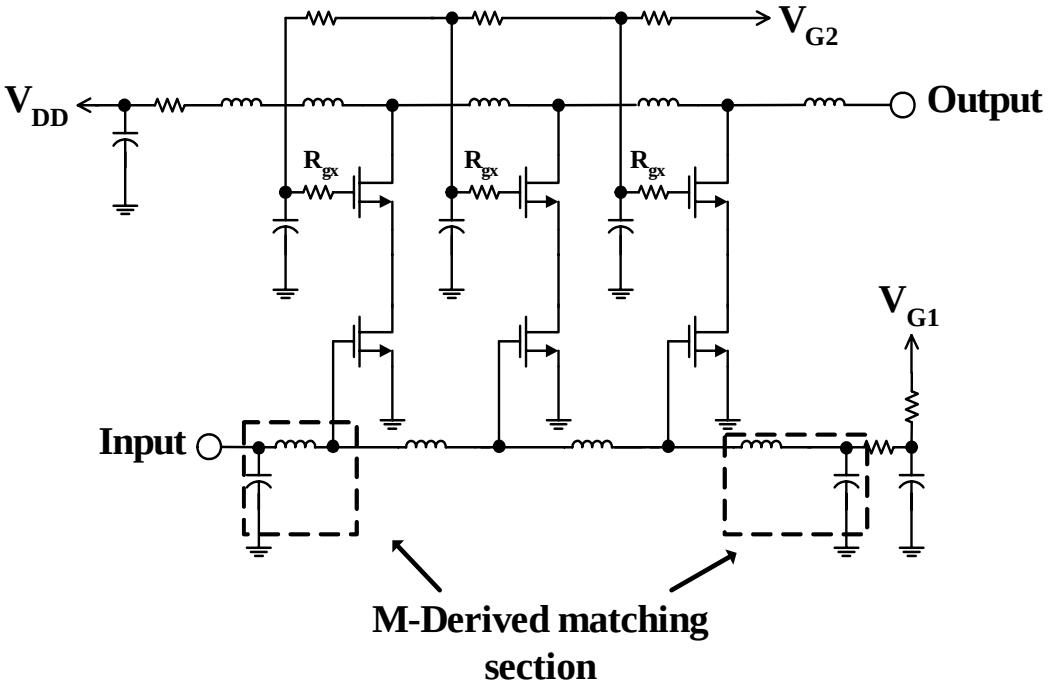


Fig. 3-7. Schematic circuit diagram of the cascade distributed amplifier.

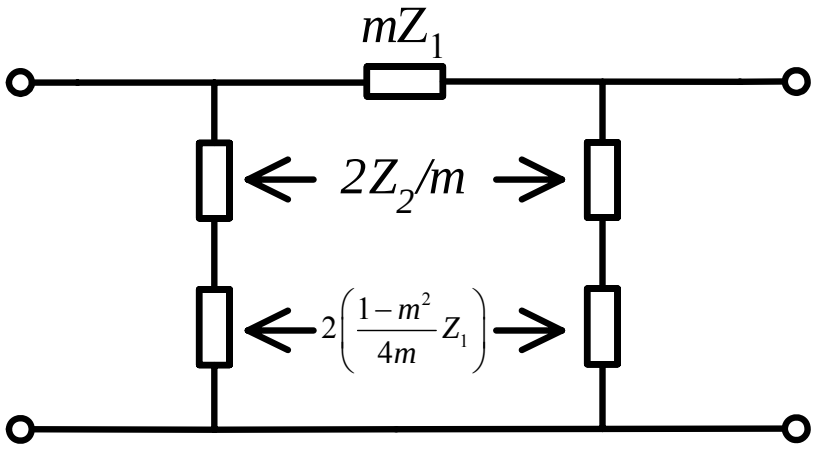


Fig. 3-8. A de-embedded m-derived π -equivalent.

CHAPTER 4

Ultra-Wideband CMOS Low Noise Amplifier Design

4.1 Circuit topology and Design Consideration

We use the three-order band-pass Chebyshev filter to maintain the flat gain at the Ultra Wide-band operating frequency spectrum from 3.1 to 10.6 GHz. Figure 4-1 shows the whole proposed ultra-wideband CMOS LNA circuit schematic. The input impedance Z_{in} is embedded in a three-order band-pass Chebyshev filter to resonate its image part over the entire band. To add flexibility to the design, an inductor (L_g) is placed in series with the gate, and a capacitor (C_p) is placed in parallel with the gate source of the input device. A capacitor (C_s) is placed in parallel with the source degeneration inductor (L_s). The gain stage is cascode structure (M_1, M_2) which improves the reverse isolation and provides the frequency response of the amplifier. The Ultra-wideband is for 3.1 to 10.6 GH_Z application. The flat forward gain over the whole bandwidth is essential. A technique that satisfied this requirement of large bandwidth at low cost is known as inductive peaking. The resistance R_d improves the gain at lower frequency. At high frequency, the L_d can maintain the gain. Source-follower voltage buffer (M_3) is intended to drive an external 50 ohm load. It is for measurement purposes.

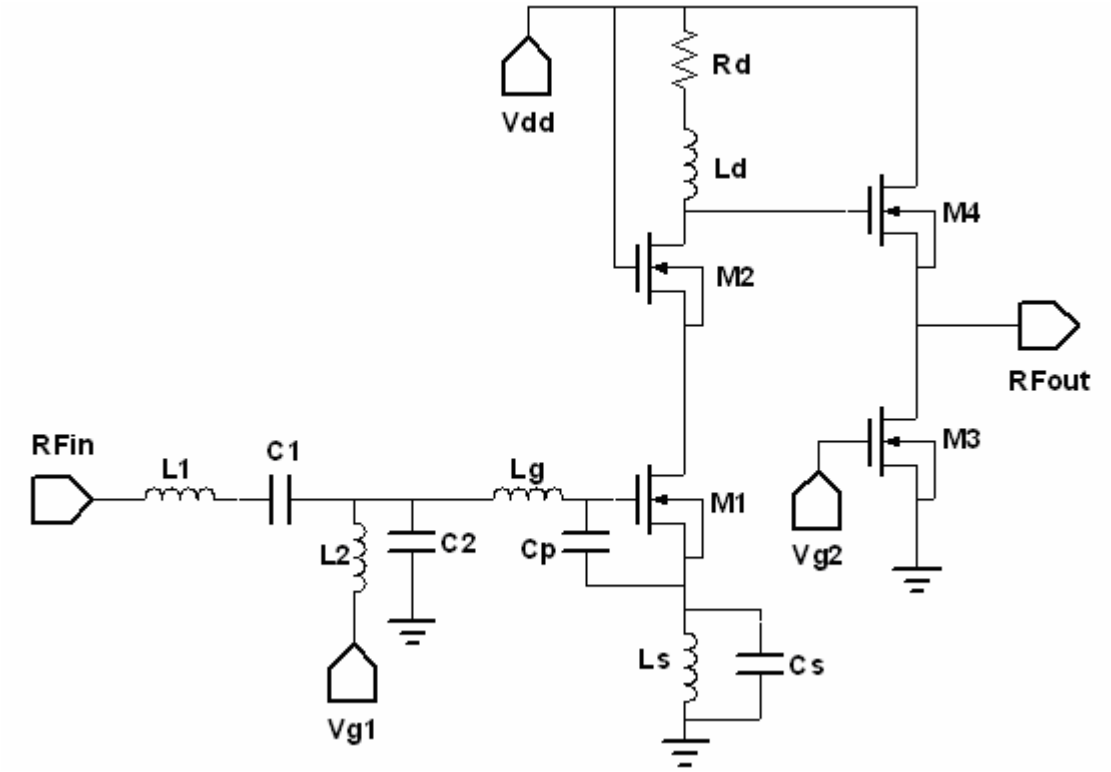


Figure 4-1 Circuit schematic of the UWB LNA.

4.1.1 Input and output impedance matching network

Figure 4-2 is the third-order band-pass Chebyshev filter. Design a band-pass filter having a 0.5 dB equal-ripple response, with three order (N=3) [3]. The center frequency is 5.7 GHz. The termination is 50 ohm. The four parameters g1, g2, g3, g4, are the prototype element values by definition. The reactive devices L1, C1, L2, C2, L3, C3 ($C_3 = C_{gs1} + C_p$, in the next discussion, C_3 is divided into C_{gs1} *and* C_p), are the components of the third-order band-pass Chebyshev filter. ω_b is the beginning frequency, and ω_c is the cutoff frequency, and ω_o is the center frequency. Design flow is as follows. The first thing is choosing the beginning

frequency (ω_b) and cutoff frequency (ω_c), then knows the bandwidth and center frequency (ω_o). Second, we can know the prototype element values g1, g2, g3, g4, from the choosing numbers of ripples and stages. Finally, put the values in the equations (4.1) of L1, C1, L2, C2, L3, C3, and we can get the values of the components we want.

$$g_1 = L_1', \quad g_2 = C_2', \quad g_3 = L_3', \quad g_4 = R_L$$

$$\Delta = \frac{\omega_c - \omega_b\,(BW)}{\omega_o\,(center\ \ freq.)}, \qquad \omega_o = \sqrt{\omega_b \cdot \omega_c}$$

$$L_1 = \frac{L_1' \cdot Z_o}{\omega_o \cdot \Delta}$$

$$C_1 = \frac{\Delta}{\omega_o \cdot L_1' \cdot Z_o}$$

$$L_2 = \frac{\Delta \cdot Z_o}{\omega_o \cdot C_2'}$$

$$C_2 = \frac{C_2'}{\omega_o \cdot \Delta \cdot Z_o}$$

$$L_3 = \frac{L_3' \cdot Z_o}{\omega_o \cdot \Delta}$$

$$C_3 = \frac{\Delta}{\omega_o \cdot L_3' \cdot Z_o}$$

(4.1)

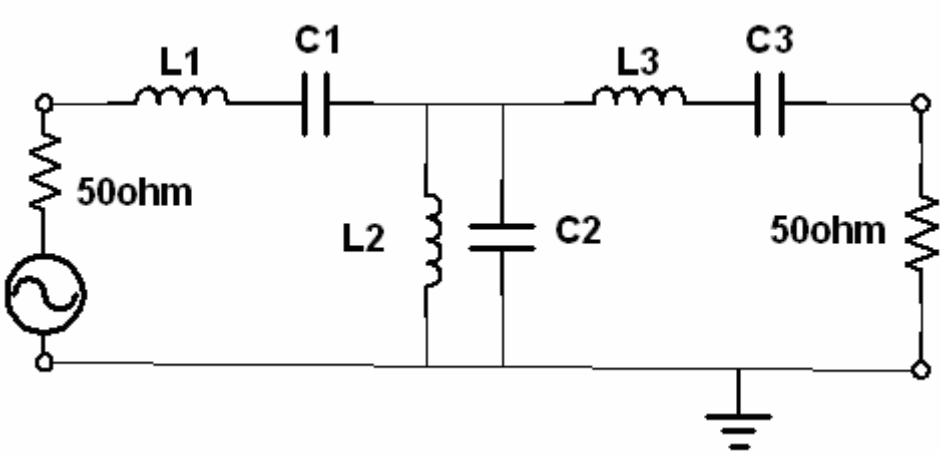


Figure 4-2 Third-order Chebyshev filter.

The input impedance (Zi) of the transistor with inductive source degeneration is a series RLC circuit. The equation (4.2) is Zi. The real part of Zi is chosen to be equal to source resister (filter termination), that is $\omega_T L_s = R_s$. If the two image part of Zi can cancel each other, the input impedance can match Rs. In the filter passband, the power loss is 0 dB, with a ripple ρ_p. The choice of reactive elements in the filter determines the bandwidth and the in-band ripple. The input reflection coefficient Γ is related to ρ_p by $|\Gamma|^2 = 1 - \frac{1}{\rho_p}$ [12]. Use the filter to let $\rho_p = 1$, then $|\Gamma|^2 = 0$. The filter can achieve the input broadband impedance matching. Figure 4-3 shows the input impedance approximation of the source degeneration LNA.

$$Z_i(s) \cong \frac{1}{s(C_{gs1} + C_p + C_s)} + s(L_s + L_g) + \omega_T L_s$$
$$= \frac{s^2(L_s + L_g)(C_{gs1} + C_p + C_s) + s\omega_T L_s(C_{gs} + C_p + C_s) + 1}{s(C_{gs1} + C_p + C_s)} \quad (4.2)$$

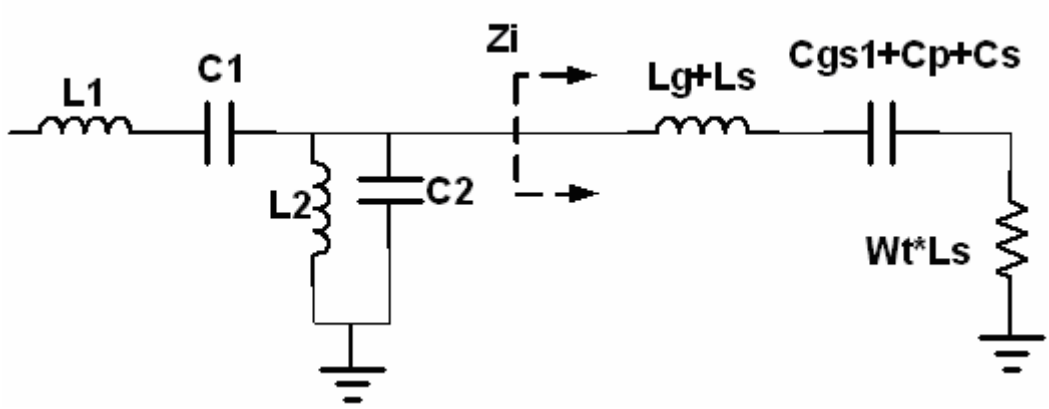


Figure 4-3 Input impedance approximation of the source degeneration LNA.

In the Figure 4-4, it shows the input impedance of the Ultra-Wideband LNA. Equation (4.3) has the detail derivation of the whole input impedance. Z_1 is the impedance of L_1, C_1 series. Z_2 is the impedance of L_2, C_2 parallel. Z_3 is other impedance of original source degeneration LNA, and is similar to Zi. Z_{in} is the combination of the three part impedance. ω_T is the 3dB cutoff frequency.

The noise resistance and minimum noise figure are not effected by the addition of C_p. For low-power design, where C_{gs1} of transistor is small, the required degeneration inductance L_s can be reduced by the addition of C_p [13]. This way can increase capacitance without raising the transistor size, and it can procure the low-power purpose. At dc frequency, L_s provides the dc ground. As frequency increasing, the impedance of L_s degrades the frequency respond, and C_s which reduces the gain degradation caused by L_s provides ac ground at radio-frequency.

$$Z_{in}(s) = Z_1 + \frac{Z_2(Z_3 + \omega_T L_s)}{Z_2 + Z_3 + \omega_T L_s}$$

$$Z_1 = sL_1 + \frac{1}{sC_1}, \quad Z_2 = sL_2 // \frac{1}{sC_2},$$

$$Z_3 = (sL_s // \frac{1}{sC_s}) + (\frac{1}{sC_{gs1}} // \frac{1}{sC_p}) + sL_g, \quad \omega_T = \frac{gm}{(C_{gs1} + C_p + C_s)}$$

(4.3)

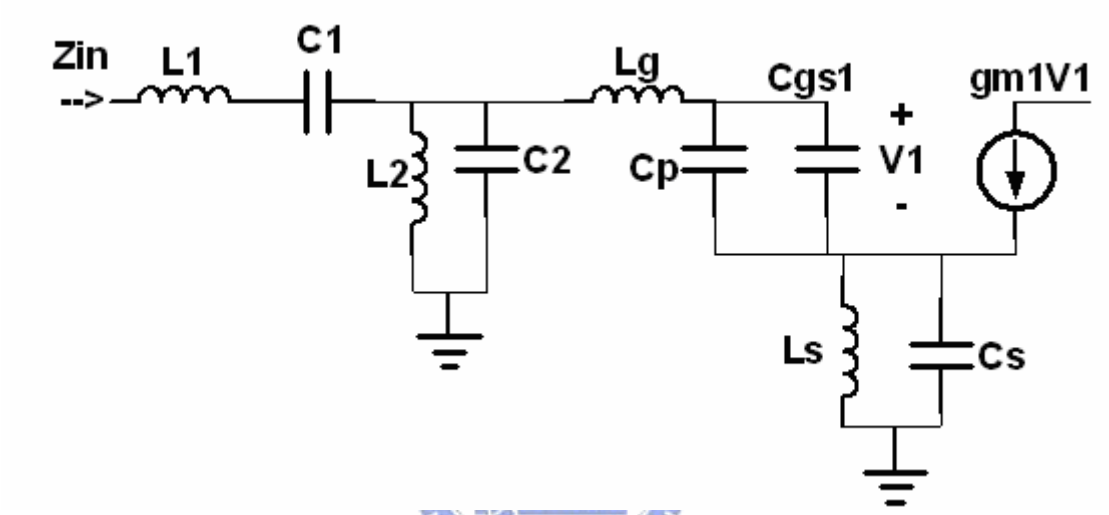


Figure 4-4 Input impedance of the UWB LNA.

Output impedance matching network is using source-follower voltage buffer. The advantage of using voltage buffer for output matching is that the impedance at output terminal (Z_{out}) is stable as equation (4.4). As frequency increasing, the impedance of voltage buffer raises slowly. The disadvantage is that the power consumption will increase without improving the circuit performance. Figure 4-5 is the output voltage buffer of the UWB LNA.

$$Z_{out} \cong \frac{1}{gm} \tag{4.4}$$

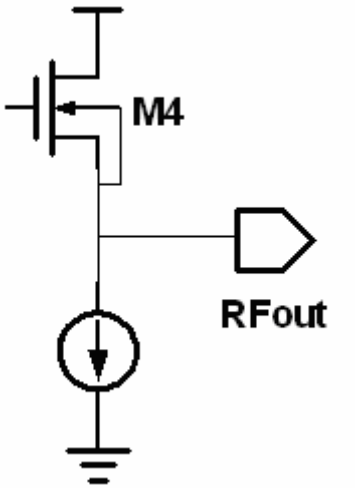


Figure 4-5 Output voltage buffer of the UWB LNA.

4.1.2 Gain stage and Inductive Peaking

The gain stage is cascode structure which improves the reverse isolation and provides the frequency response of the amplifier. The design flow is as follows. First, choose the dc-bias Vg which the bias point that provides minimum noise figure. Second, choose the transistor size based on the power constraint. The size of the transistor M_1 must be selected carefully. The gate capacitance C_{gs1} must follow the required component value in the Chebyshev filter design. The transistor size must yield to sufficient noise performance and power constraint [14]. Third, choose the additional capacitance C_p. The value of C_p should be chosen considering the compromise between the size of L_s and the available power gain. Too much L_s can lead to the increase in noise figure and area of die size, while large C_p leads to the gain reduction due to the degradation of the effective cutoff frequency of the

composite transistor (including C_p). We consider the relationship between the cutoff frequency and the total gate capacitance, and the addition of C_p leads to power-gain degradation [4-2]. At dc frequency, L_s provides the dc ground. As frequency increasing, the impedance of L_s degrades the frequency respond, and C_s which reduces the gain degradation caused by L_s provides ac ground at high frequency. $Av \cong gm_1 \cdot (R_d + sL_d)$ is the approximation of the gain equation. Figure 4-6 shows the gain stage and shunt peaking of the Ultra-Wideband LNA.

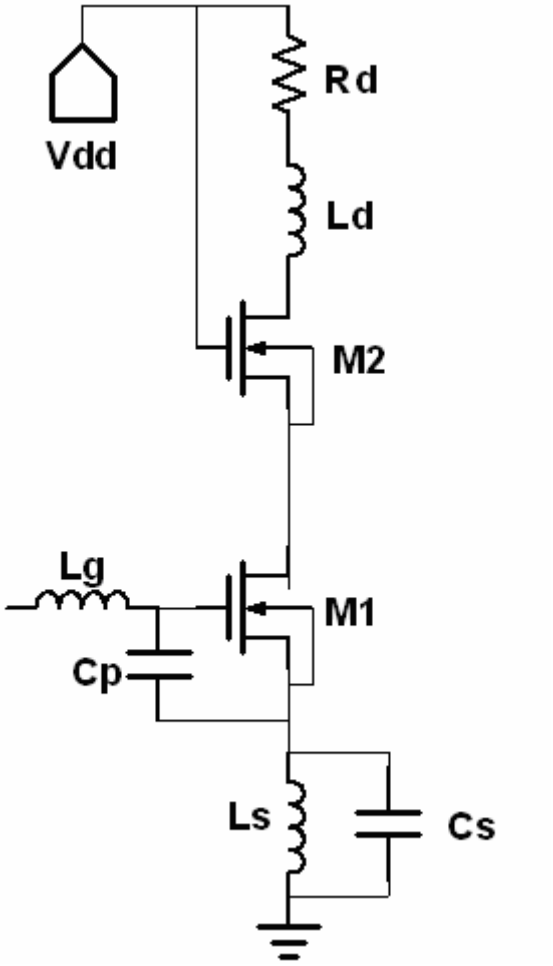


Figure 4-6 Gain stage and shunt peaking of the UWB LNA.

In the Figure 4-7, it shows the model of shunt peaking amplifier. Shunt peaking is one of the inductive peaking. The resistance *R* is the effective load resistance at that node and the inductor *L* provides the bandwidth enhancement. The capacitance *C* may be taken to represent all the loading on the output terminal, including that of a subsequent stage. It's clear from the model that the transfer function $\frac{v_{out}}{i_{in}}$ is just the impedance of the *RLC* network, so it should be straightforward to analyze. The addition of an inductance in series with the load resistor provides an impedance component that increases with frequency, which helps offset the decreasing impedance of the capacitance, leaving net impedance that remains roughly constant over a broader frequency range than that of the original *RC* network. The impedance of the *RLC* network may be written as

$$Z(s) = (sL + R) // \frac{1}{sC} \tag{4.5}$$

We introduce a factor *m*, defined as the ratio of the *RC* and *L/R* time constant:

$$m = \frac{RC}{L/R} \tag{4.6}$$

Then, the transfer function becomes

$$Z(s) = \frac{R[s(L/R)]+1}{s^2LC+sRC+1} = \frac{R(\tau s+1)}{s^2\tau^2 m+s\tau m+1} \tag{4.7}$$

where $\tau = L/R$.

The magnitude of the impedance, normalized to the DC value as a function of frequency, is then

$$\frac{|Z(j\omega)|}{R} = \sqrt{\frac{(\omega\tau)^2 + 1}{(1-\omega^2\tau^2 m)^2 + (\omega\tau m)^2}} \tag{4.8}$$

so that

$$\frac{\omega}{\omega_1} = \sqrt{\sqrt{(-\frac{m^2}{2}+m+1)^2 + m^2} + (-\frac{m^2}{2}+m+1)} \tag{4.9}$$

where ω_1 is the uncompensated -3dB frequency. Chose $m = 1+\sqrt{2} \approx 2.414$, then can lead to a bandwidth that is about 1.72 times as large as the un-peaked case. Hence, at least for the shunt-peaked amplifier, both a maximally flat response and a substantial bandwidth extension can be obtained simultaneously [15].

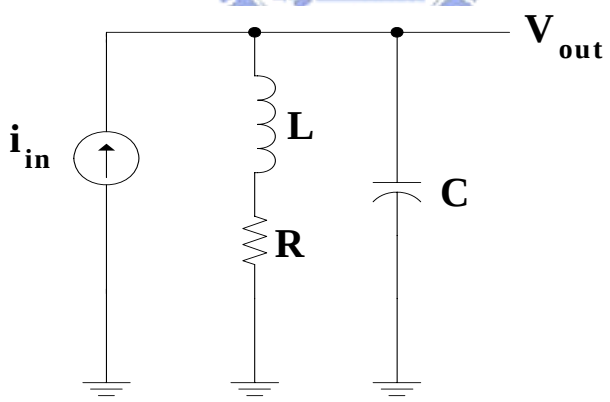


Figure 4-7 The model of the shunt peaking amplifier.

4.2 Chip Implementation and Measured Result

4.2.1 Circuit Implementations

According to the discussion in the section 4.1, the three-order band-pass Chebyshev filter can reach the broadband input impedance matching. Owing to the low power consideration, plus the additional gate capacitor C_p. The cacoded structure gain stage provides the gain of the amplifier. The capacitor C_s reduces the gain degradation caused by L_s at high frequency. The inductive shunt peaking maintain the gain flatness. Output buffer is used for output broadband matching. Figure 4-1 shows the whole proposed ultra-wideband CMOS LNA circuit schematic.

The device sizes are as follows. The transistor total width of M_1 is 150 μm, M_2 is 80 μm, M_3 is 60 μm, M_4 is 80 μm. L_1 is 1.2 nH. L_2 is 2 nH. L_g is 1 nH. L_s is 0.2 nH. L_d is 1.6 nH. R_d is 55 ohm. C_1 is 472 fF. C_2 is 278 fF. C_p is 57 fF. C_s is 112 fF. Vdd is 1.8 volt. Vg_1 is 0.7 volt. Vg_2 is 0.8 volt.

4.2.2 Experimental Results

The Ultra-Wideband LNA is fabricated using 0.18 μm RF CMOS technology. Figure 4-8 is the layout diagram of the UWB LNA. Figure 4-9 shows the full chip of the LNA circuit by microphotograph. The total die area is 0.985 mm by 1.008 mm.

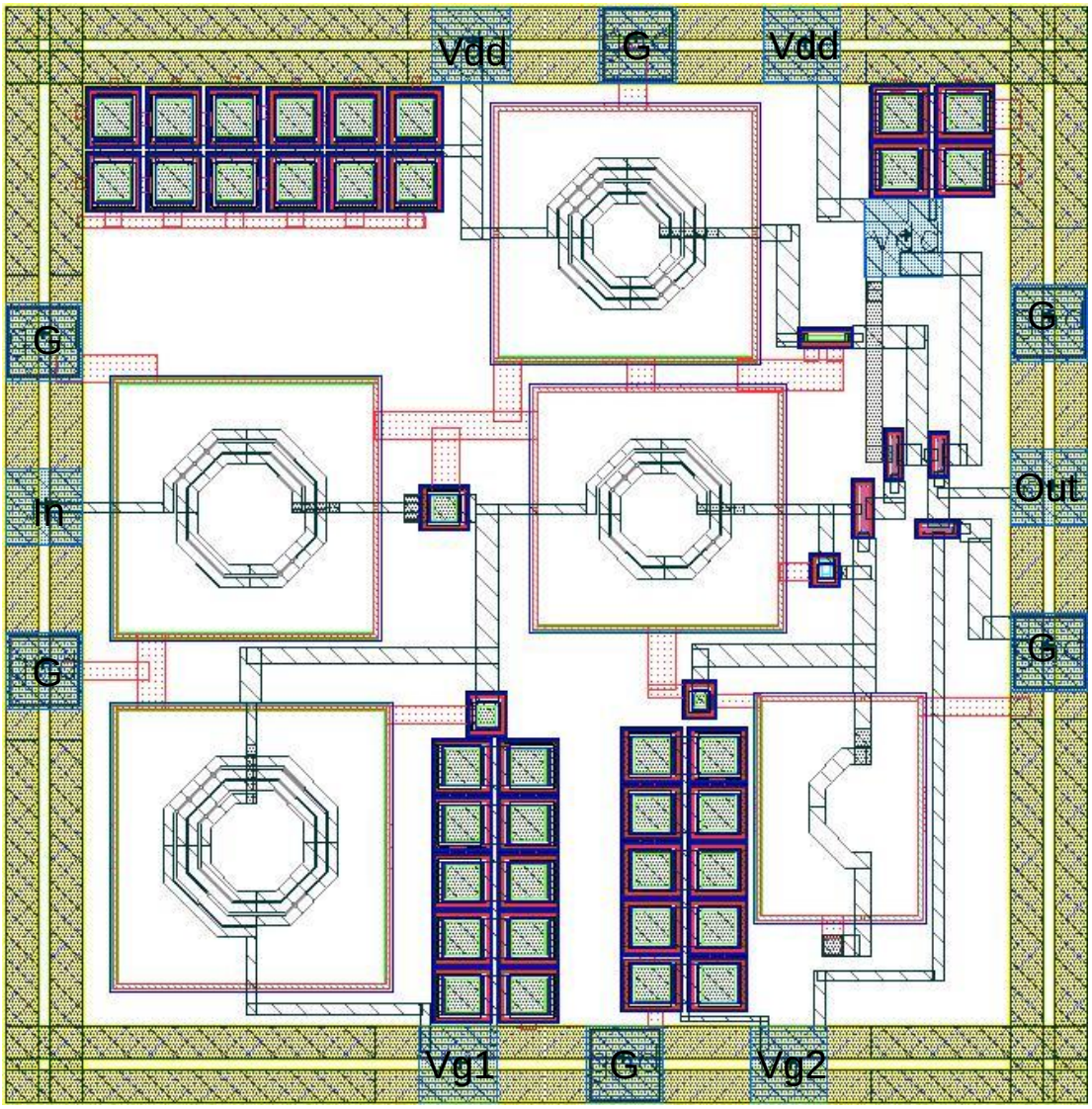


Figure 4-8 The layout diagram of the UWB LNA.

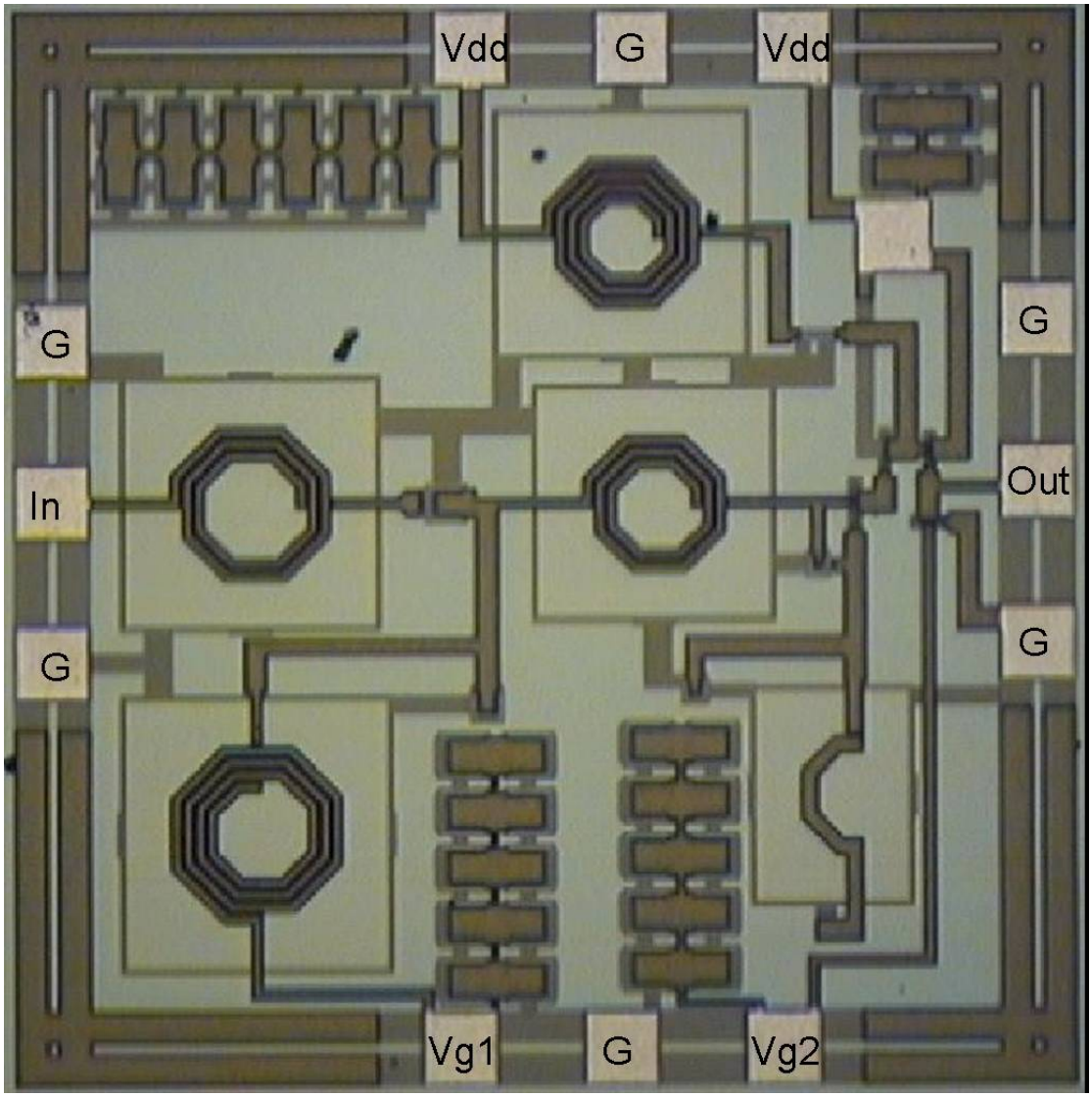


Figure 4-9 The microphotograph of the UWB LNA.

The way of measurement is on wafer test by RF probstation. The three pins GSG RF probes are used for transformation of input and output signal, and the one pin DC probes provide the bias voltages. The two bias tees are used for input and output dc block. Figure 4-10 and 4-11 show the simulated and measured results of input and output return loss S11 and S22. The average simulated result of S11 is smaller than -10dB from 3.1 to 10.6GHz, and the average measured data of S11 is smaller than

-7dB. The average simulated and measured result of S22 are both smaller than -10dB. Figure 4-12 is the simulated and measured results of the power gain S21. The simulated result of S21 is from 11 to 15.3dB, and the measured data of S21 is from 6 to 9.7dB. Figure 4-13 shows the simulated and measured results of reverse isolation S12. The simulated and measured results of noise figure (NF) is shown in Figure 4-14. The simulated minimum noise figure is 3dB, and the average noise figure is about 3.5dB. The measured minimum noise figure is 6.1dB, and the average noise figure is about 7dB. The two-tone test simulated and measured results for third-order intermodulation distortion are shown in Figure 4-15 and 4-16. The test is performed at 5.5GHz. The simulated result of IIP3 is 4.5dBm, and the measured result of IIP3 is 6dBm. The measured input referred 1-dB compression point P_{-1dB} (or ICP) is -2.5dBm. The power consumption of the proposed UWB LNA is 18mW for measurement. Complete measured results are summarized in Table 4.1 together with simulated results for comparison. In Table 4.2 listed is the comparison of circuit performance with previous work.

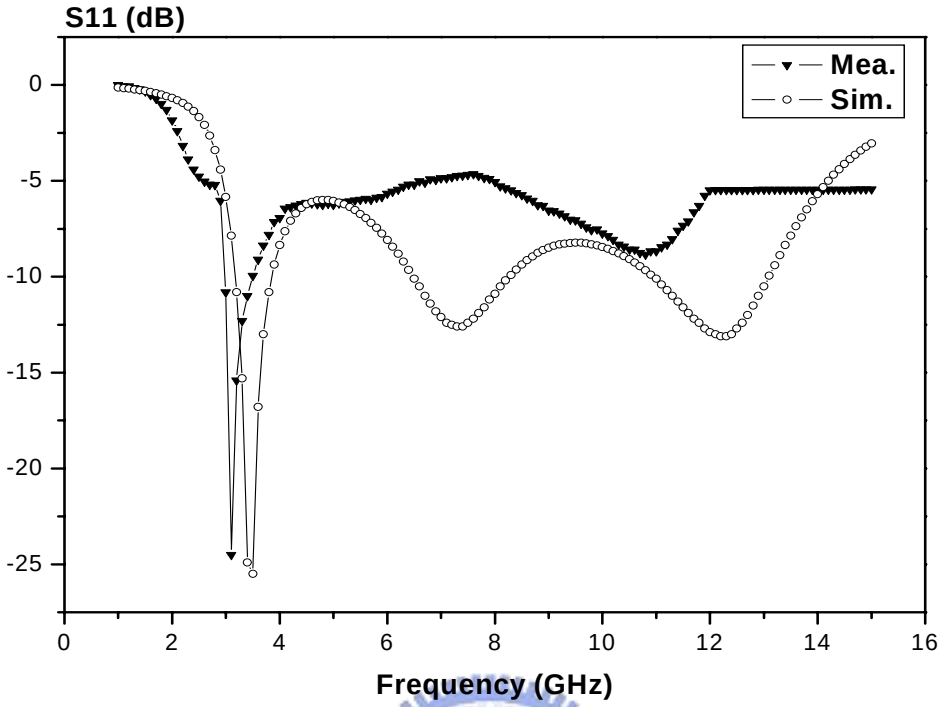


Figure 4-10 S11 simulated and measured result.

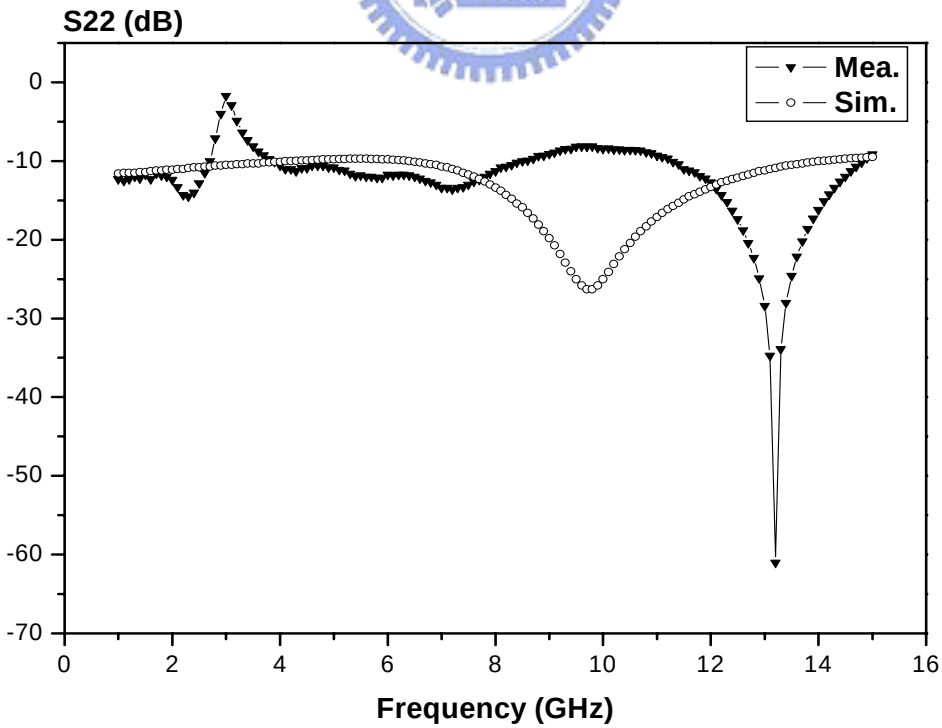


Figure 4-11 S22 simulated and measured result.

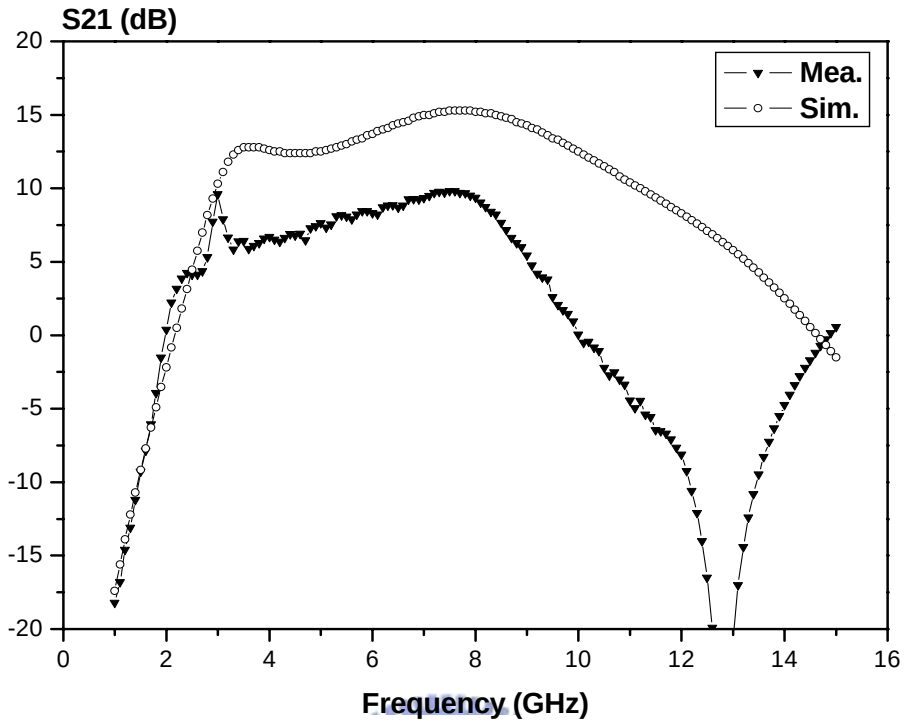


Figure 4-12 S21 simulated and measured result.

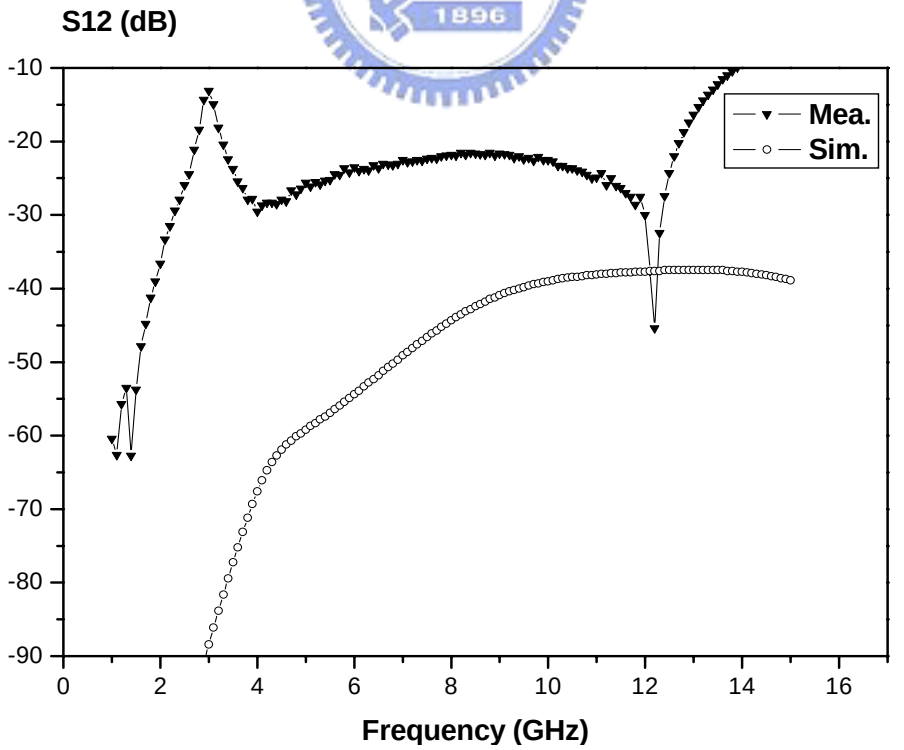


Figure 4-13 S12 simulated and measured result.

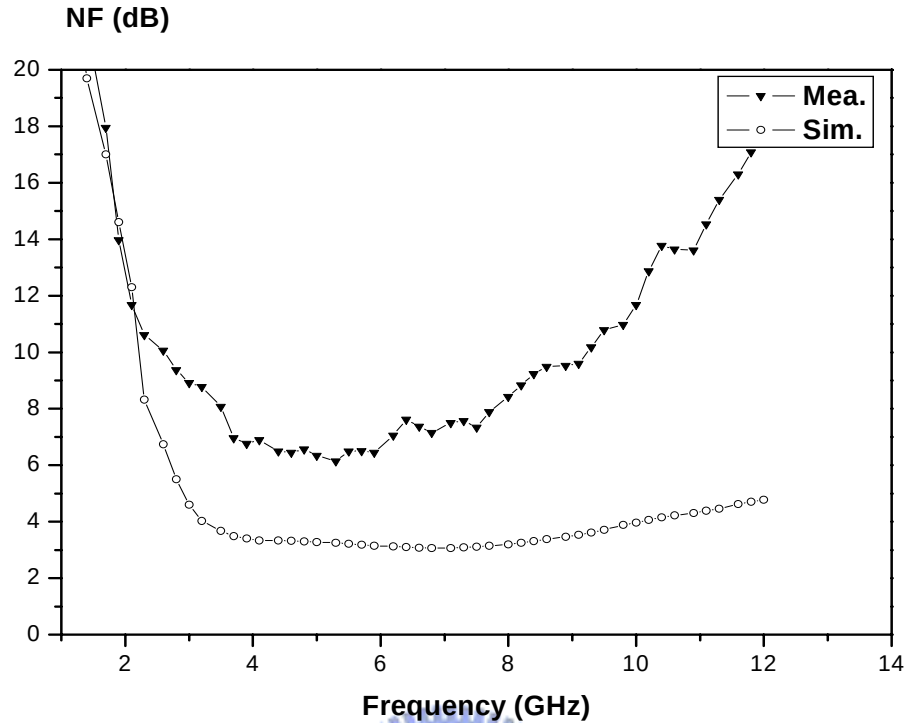


Figure 4-14 NF simulated and measured result.

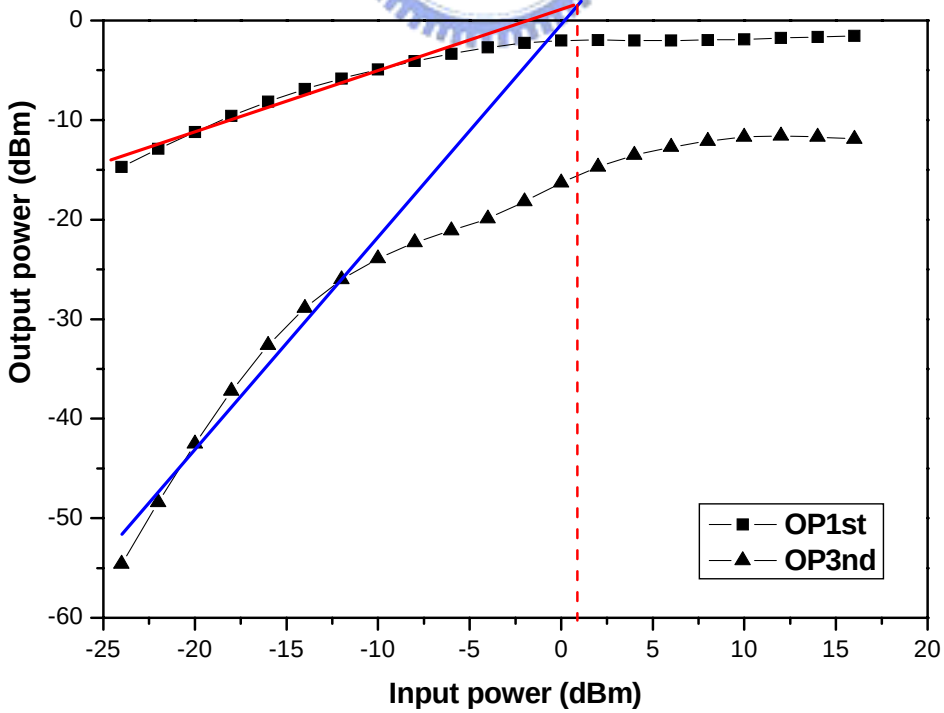


Figure 4-15 IIP3 simulated result.

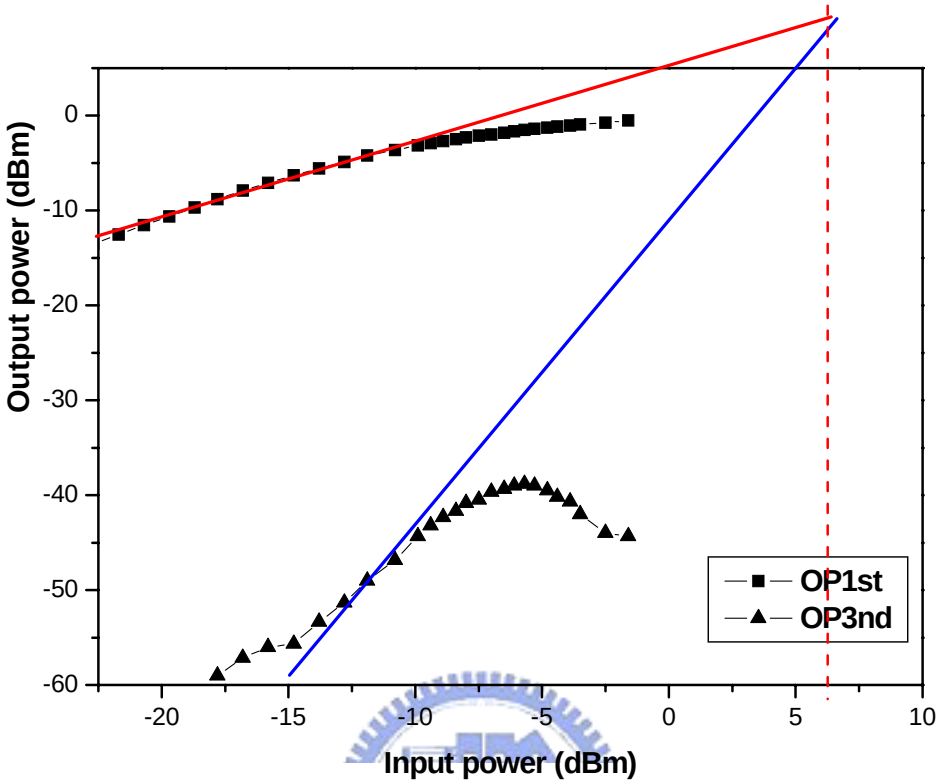


Figure 4-16 IIP3 measured result.

Table 4.1. Summary of simulated and measured results of UWB LNA.

Item (corner TT)	Simulation	Measurement
Supply voltage (V)	1.8	1.8
Gate1 bias (V)	0.7	0.7
Bandwidth (GHz)	3.1~10.6	3.1~10.6
Nosie Figure (dB)	Ave.:3.5 , min:3	Ave.:7 , min:6.1
Gain (dB)	11 ~15.3	6~9.7
S11 (dB)	Ave. < -10.	Ave. < -7.
S22 (dB)	Ave. < -10.	Ave. < -10.
S12 (dB)	< -40	< -20
IIP3@5.5GHz (dBm)	4.5	6
Pdc (mW)	22	18

4.2.3 Discussions

The measured data of S11 and S22 exhibit a little frequency shift. The difference between measured data and simulated result on the input and output return loss may be due to the variation of the pad capacitance, parasitic inductance of wire, and input matching components. The peak at 3GHz of the S22 may be caused by the extra LC resonance of metal line. The peak also has affection to S21 and S12. The gain degradation of the measured data showing in Figure 4-12 may be due to energy dissipation on the parasitic resistance of wire line and the underestimation of the load resistor parasitic. But the linearity improvement achieves more than 1.5 dBm without extra power consumption.

4.3 Comparison with no output buffer UWB LNA

The Ultra-Wideband LNA is fabricated using 0.18 μm RF CMOS technology. Figure 4-17 is the circuit schematic of the no output buffer UWB LNA. Figure 4-18 shows the simulated S21 comparison between with buffer and no buffer UWB LNA. We can see that the no buffer LNA has poor gain and gain flatness, because the output impedance changes with frequency. So, the output impedance matching of with buffer LNA is better than the no buffer one. Although the output matching of the buffer one is the advantage, it needs more power consumption and the transistor of buffer introduces extra noise source. In the Figure 4-19, it is the simulated NF comparison between with buffer and no buffer UWB LNA. We can see that the no buffer one has better NF performance. Figure 4-20 shows the layout diagram of the UWB LNA. The total die area is 0.813 mm by 1.08 mm.

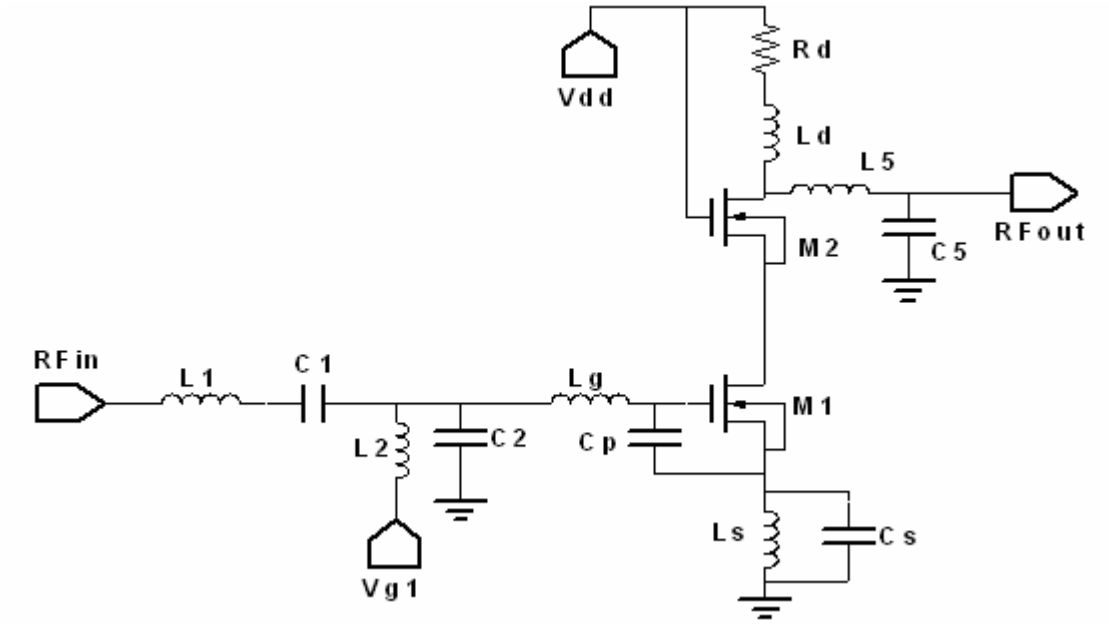


Figure 4-17 Circuit schematic of the no output buffer UWB LNA.

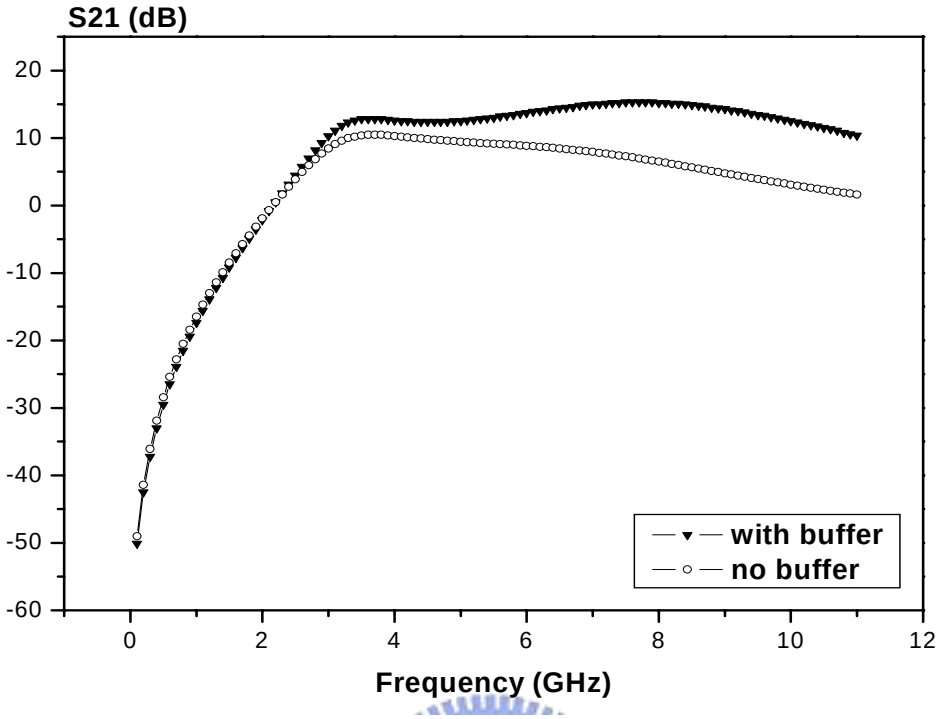


Figure 4-18 Simulated S21 comparison between with buffer and no buffer LNA.

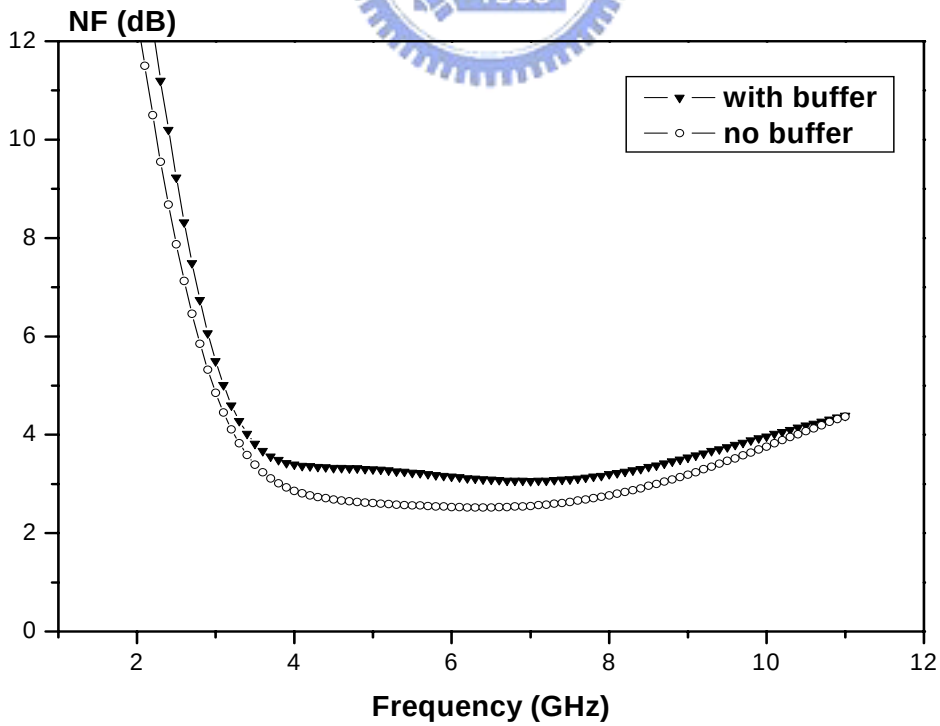


Figure 4-19 Simulated NF comparison between with buffer and no buffer LNA.

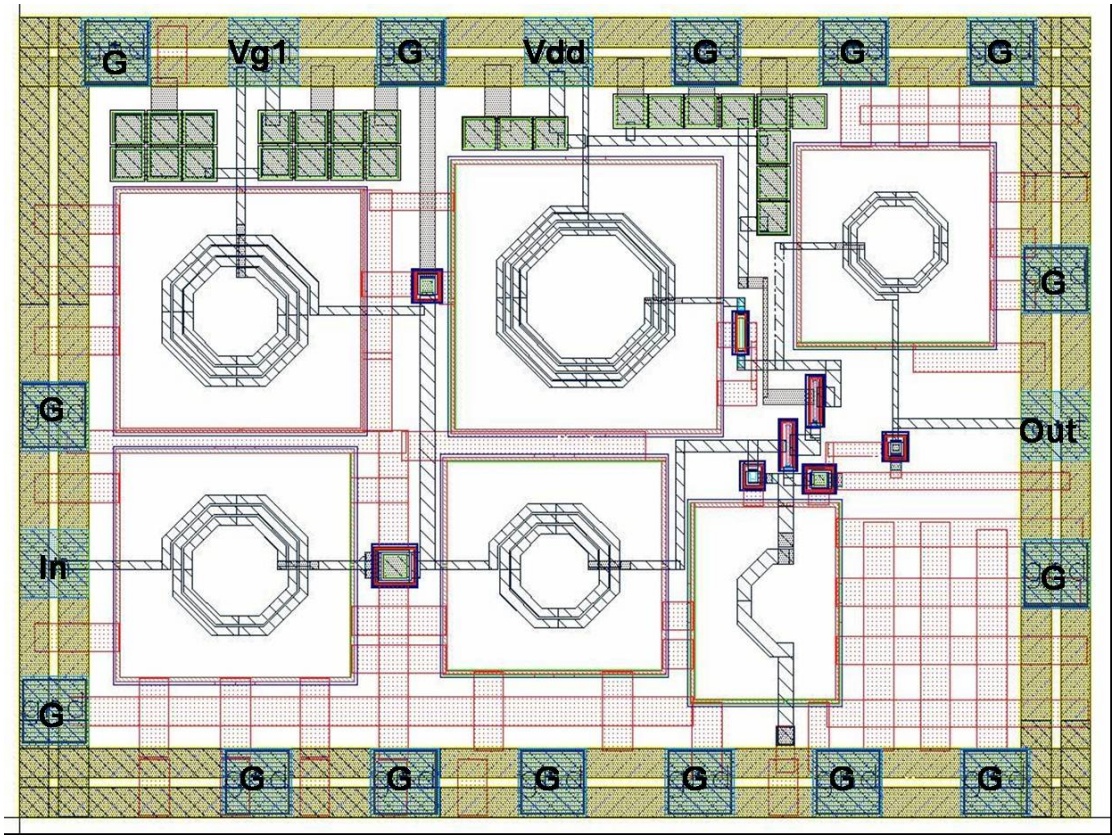


Figure 4-20 The layout diagram of the no buffer LNA.

CHAPTER 5

Summary

By the three-order band-pass Chebyshev filter, a broadband impedance matching, a low power consumption amplifier is developed for UWB system applications. Table 5.1 is the comparison of broadband LNA performance. We can find out that this work has the highest gain maximum and amazing linearity IIP3 in this table. This result can prove that this circuit topology is useful for UWB system application.

Table 5.1 Comparison of broadband LNA performance. * LNA core only

Ref.	**B.W. (GHz)**	**Gmax (dB)**	**NFmin (dB)**	**S11 (dB)**	**S22 (dB)**	**IIP3 (dBm)**	**Pdc (mW)**	**Tech. (um)**	**year**
[16]	2.4~9.5	9.3	4	< -9	< -20	-6.7	9*	0.18 CMOS	2004 ISSCC
[17]	0.6~22	8.1	4.3	< -8	< -9	NA	52	0.18 CMOS	2003 RFIC
This work	3~10	**9.7**	6.1	< -7	< -10	**6**	18	0.18 CMOS	2006

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（93 年 9 月入學）

論文題目：

1.8 伏金氧半低雜訊放大器之設計應用於超寬頻 UWB 3.1-10.6GH_Z 無線接收端

(Design of a 1.8 -V CMOS LNA applied for Ultra-Wideband 3.1 to 10.6GH_Z Wireless Receivers)