國 立 交 通 大 學

電 機 與 控 制 工 程 學 系 研 究 所

碩 士 論 文

適用於 Serial-ATA 之
展頻時脈產生器及其內建自我測試電路

A Spread Spectrum Clock Generator and Built-in-Self-Test Circuit for Serial-ATA

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中華民國 九十五年 九月


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摘要

隨著對高速傳輸速率需求的不斷提升，高速時脈信號所造成的電磁干擾(*Electro-Magnetic Interference*, EMI)成為不可忽視的問題。在常見的外部儲存規格 *Serial AT Attachment* (Serial-ATA)中，系統要求資料傳輸時的時脈頻率具有 5000 ppm 的展頻量與 30~33 kHz 之三角波調變率。展頻技術即是利用對時脈信號頻率做調變以有效降低電磁干擾。

在本論文中，我們提出一個符合 Serial-ATA 規格並適用於 6Gbps 資料發送器之展頻時脈產生器(*Spread Spectrum Clock Generator*, SSCG)及其內建自我測試(*Built-in-Self-Test*, BIST)電路。我們使用一個具備三階三角積分調變器的除小數頻率合成器來實現展頻時脈產生器，使用數位式三角積分調變技術可將量化雜訊調變到高頻以減少 spur 現象。為了減少展頻時脈產生器的相位跳動，我們採用相位調變的方式來達到展頻的效果。展頻時脈產生器的內建自我測試電路是用數位的方式偵測展頻時脈產生器的頻率變動，藉由此測試電路可以簡單的測試出展頻時脈產生器是否正常操作。

我們使用 TSMC CMOS 0.18 μm 製程實現了一個 1.2 GHz 10 個 phases，具有 5000 ppm、30 kHz 三角波調變的展頻時脈產生器及其內建自我測試電路。在非展頻情況所量測到的時脈抖動 peak-to-peak jitter 為 48 ps；RMS jitter 為 7.226 ps。在展頻模式下，頻譜上的時脈峰高能量降低了 21.633 dB。

索引詞彙—除小數頻率合成器、展頻時脈產生器、內建自我測試電路、鎖相迴路、三角積分調變器

A Spread Spectrum Clock Generator and Built-in-Self-Test Circuit for Serial-ATA

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ABSTRACT

As operating at high frequencies, currents and voltages present in the circuits and the signal traces lead to a great *Electro-Magnetic Interference* (EMI). In *Serial AT Attachment* (Serial-ATA), one of the popular external storage specifications, it requires a wide spreading of 5000 ppm at a 30~33 kHz triangular modulation rate. The *Spread Spectrum Clock Generator* (SSCG) is a special technique of frequency modulation to reduce EMI effectively.

In this thesis, we propose a SSCG for 6Gbps transceiver and its *Built-in-Self-Test* (BIST) circuit for Serial-ATA specification. We use a fractional-N frequency synthesizer with a digital third-order MASH 1-1-1 sigma-delta modulator to accomplish the spread spectrum function. The use of digital sigma-delta modulation technique in the fractional-N frequency synthesizer can eliminate spurs. Using phase modulation to spread the spectrum can reduce the phase jump of the SSCG. The BIST circuit for SSCG is a digital approach to detect the frequency variation of the SSCG, it can tests if the SSCG work or not effectively and precisely.

The SSCG which has 1.2 GHz 10 phases, a 5000 ppm down spread and a 30 kHz triangular modulation rate. The BIST circuit are implemented using TSMC CMOS 0.18 μm technology. The measurement results show that the non spreading clock has a peak-to-peak jitter of 48 ps, a RMS jitter of 7.226 ps, and a peak amplitude reduction of 21.633 dB in the spread spectrum mode.

Index Terms — fractional-N frequency synthesizer, spread spectrum clock generator, building-in-self-test, phase-locked loop, sigma-delta modulator

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周楙軒

08/30/2006

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Chapter 1

Introduction

1.1 Motivation

As the increasing demand for higher data transmitting rate, *Serial AT Attachment* (Serial-ATA) is one of the popular external storage specifications. High speed serial link technology is applied in optical communication, PCI Express and USB recently. Using serial link technology has many advantages including low cost, high speed and pin reduction. Serial-ATA is used with high transmission rate up to 3 Gbps and extends up to 6 Gbps in the next generation.

As operating at high frequencies, currents and voltages present in the circuits and the signal traces lead to a great *Electro-Magnetic Interference* (EMI). EMI is caused by the radiated emission of unwanted radio frequency signals that pollute

managed radio spectrum. In the United States, the *Federal Communications Commission* (FCC) regulates the amount of EMI an electronic device may emit to ensure that electronic devices do not interfere with each other.

Many EMI reduction techniques can be classified into two. One is to enclose the EMI from emitting and another is to reduce the EMI at the source. The reduction methods include *Printed Circuit Broad* (PCB) layout techniques, metal shielding, and passive components. Another popular technique, *Spread Spectrum Clocking* (SSC), belongs to the latter which can reduce the amplitude at each clock harmonic to meet EMI restriction [1]. Ideally, the EMI reduction is done on chip without using heavy shielding materials in order to be low cost and portable. Serial-ATA systems adopt the SSC technique to reduce EMI problem. The *Spread Spectrum Clock Generator* (SSCG) is a special technique of frequency modulation to reduce EMI effectively.

CMOS technology has been growing very fast in recent years. Design of *integrated circuits* (ICs) becomes so complex and gate counts become so large. Undoubtedly, faster and more complex test equipments are required to achieve test specifications and test functions. An innovative method to simplify the test equipment is to move test functions onto the chip itself, which is called *Built-in-Self-Test* (BIST).

In this thesis, we accomplish a SSCG for 6Gbps transceiver for Serial-ATA specification and its BIST circuit. The BIST circuit for SSCG is a digital approach to detect the frequency variation of SSCG, it can tests if the SSCG work or not effectively and precisely.

1.2 Basics of Serial Link

Figure 1.1 shows a general purpose serial link transceiver architecture. The low-speed parallel digital signals are to be transferred to far-end. The *phase-locked loop* (PLL), based on a low frequency reference clock, generates appropriate clock phases

and applies these clock phases to the *multiplexer* (MUX). The MUX transfers these parallel input data to a high speed serial output data. Since the driving capability of the MUX output is small, so it is enlarged stage by stage by the driver. When signal is transmitted through the channel, the frequency and phase may drift due to external noise and the amplitude will decay as well. The receiver front end enlarges the signal amplitude. Then the *Clock and Data Recovery* (CDR) finds the optimal sampling phase and retimes the signal. The De-MUX transfers the serial signals back to the parallel ones.

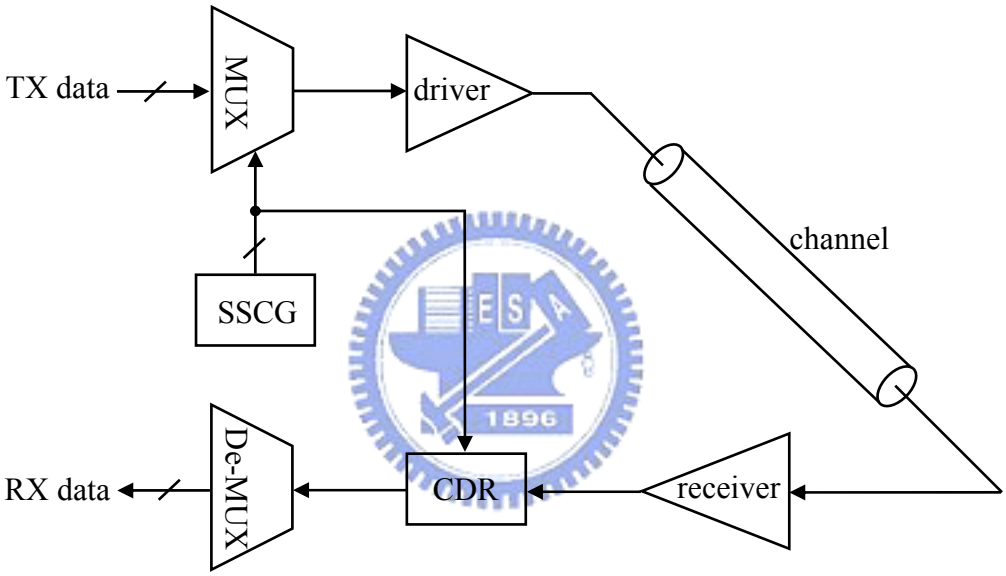


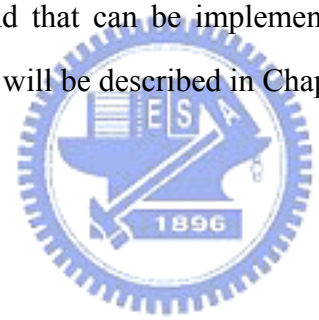
Figure 1.1: Serial link transceiver architecture

1.3 Thesis Organization

This thesis comprises seven chapters. Chapter 1 introduces the motivation of this thesis and thesis organization. In Chapter 2, we will introduce the spread spectrum theory, how it can reduce EMI problem, and the Serial-ATA requirements for SSCGs. In Chapter 3, we introduce the frequency synthesizer including PLL and the fractional-N concept. The most important part is to describe the digital sigma-delta modulator.

In Chapter 4, we will introduce the different types of SSCGs. We accomplish a SSCG using a conventional PLL consists of a phase frequency detector, a charge pump, a loop filter, a voltage controlled oscillator and a frequency divider. Then we will introduce address generator that generates the triangular waveform for frequency modulation, a third-order MASH 1-1-1 sigma-delta modulator, a multiplexer and a controller that control the VCO output phases to frequency divider for frequency modulation.

In Chapter 5, we will show the simulation and measurement results of the SSCG. The chip is implemented in TSMC 0.18 um 1P6M CMOS technology. In Chapter 6, a BIST circuit for SSCG is proposed. The BIST circuit for SSCG is a digital approach to detect the frequency variation of SSCG, it can tests if the SSCG work or not effectively and precisely. And that can be implemented with little area and power overhead. Finally, conclusion will be described in Chapter 7.



Chapter 2

Basics of Spread Spectrum Clocking

Faster operating speeds of electrical devices today result in more EMI at higher frequencies. Lots of methods have been proposed to reduce EMI. Commonly used EMI reduction solutions include: shielding, pulse shaping, slew-rate control [2], low voltage differential clocking [3], staggering the outputs [4], layout technique, and *spread spectrum clocking* (SSC). SSC is a popular technique to reduce EMI for *Serial-ATA* (Serial-ATA) requirement. In this chapter, we discuss the fundamental theory of SSC including the basic properties and the effects on the original timing.

2.1 The Fundamental Theory of SSC

SSC is a special technique of frequency modulation to reduce EMI effectively. As shown Figure 2.1 [5], by spreading the clock frequency slightly, the energy is spread out as well. This reduces the maximum peak energy under the same total amount of energy. Only a small amount of variation in frequency is needed to obtain several decibels of energy reduction. Otherwise, it would take a lot of expensive shielding to achieve the similar results. As a result, SSC is an effective and low cost technique to meet EMI restriction.

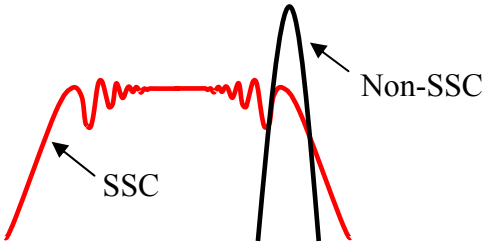


Figure 2.1: Spread fundamental frequency comparison

To obtain the details of spread spectrum, we analyze that how frequency modulation can lead to spread spectrum. Figure 2.2 shows the effect of frequency modulation on the frequency spectrum, where f_c is the carrier frequency, f_m is the modulating frequency, and Δf is the amplitude of frequency change. As can be seen frequency domain of the frequency-modulated sinusoidal waveform, sideband harmonics are generated, and the magnitude at center frequency is reduced compared to un-modulated signal. The frequency difference between each two adjacent sideband harmonics is f_m.

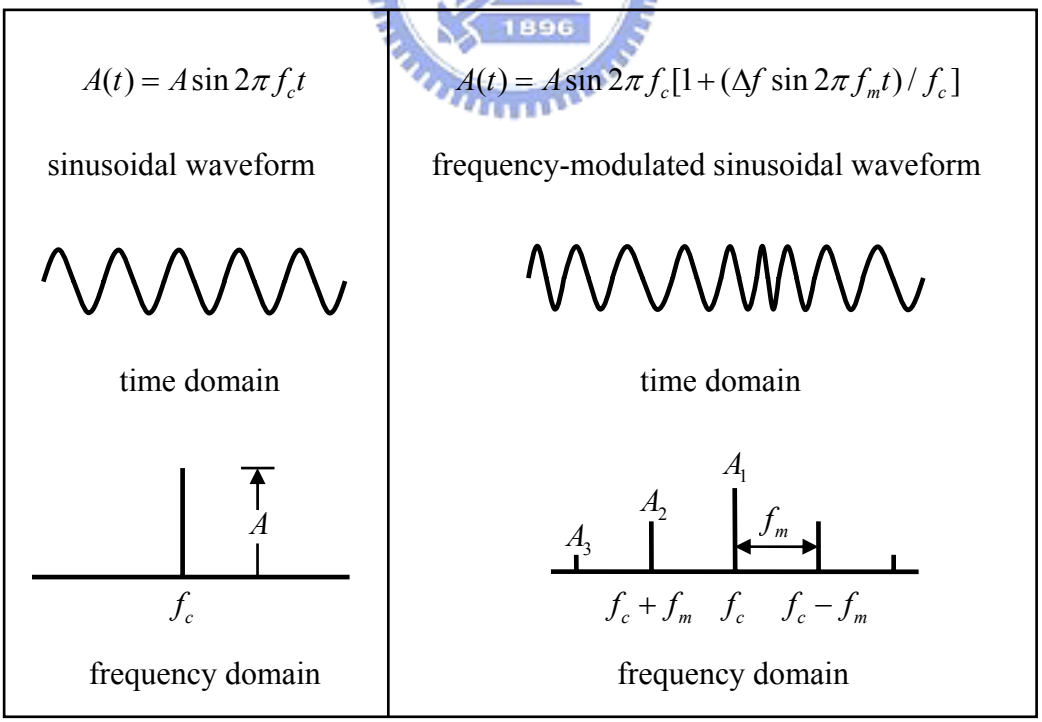


Figure 2.2: The effect of frequency modulation on the frequency spectrum

The extent of distribution and the magnitude of the resultant spectrum depend on the modulation index $\beta \equiv \Delta f / f_m$ [6]. Figure 2.3 shows the actual spectra for several β values. The larger the β values, the more evenly distributed are the spectrum.

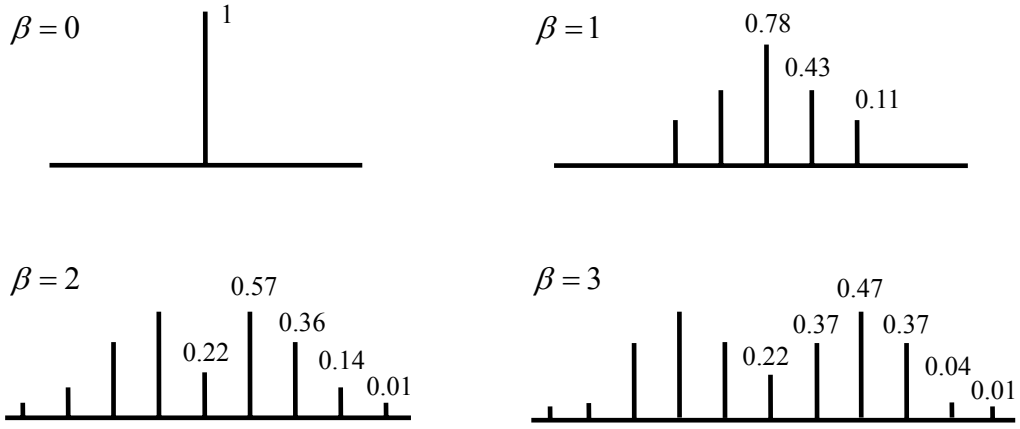


Figure 2.3: Spectra of frequency-modulated sine wave

There are two important characteristics of a frequency modulated signal according to Carson's Rule:

(1) Total power of a signal is unaffected by the frequency modulation. The total power of a signal is equal to the summation of the square of each harmonic amplitude. Referring to Figure 2.3, this means

$$A^2 = A_1^2 + 2(A_2^2 + A_3^2 + \ldots). \quad (2\text{-}1)$$

(2) 98% of the total power of a frequency modulated signal is contained inside the bandwidth β_T, where $B_T = 2(\beta + 1)f_m$. This means the side-band harmonic frequency ranges from $(f_c - B_T/2)$ to $(f_c + B_T/2)$. where $B_T = 2\Delta f(\beta + 1)/\beta$. If $\beta \gg 1$, the $B_T = 2\Delta f$.

As shown in Figure 2.4, if the un-modulated waveform is a pulse train, then it itself contains harmonics. Frequency modulation of the pulse train waveform distributes each of the switching harmonic components into sideband harmonic.

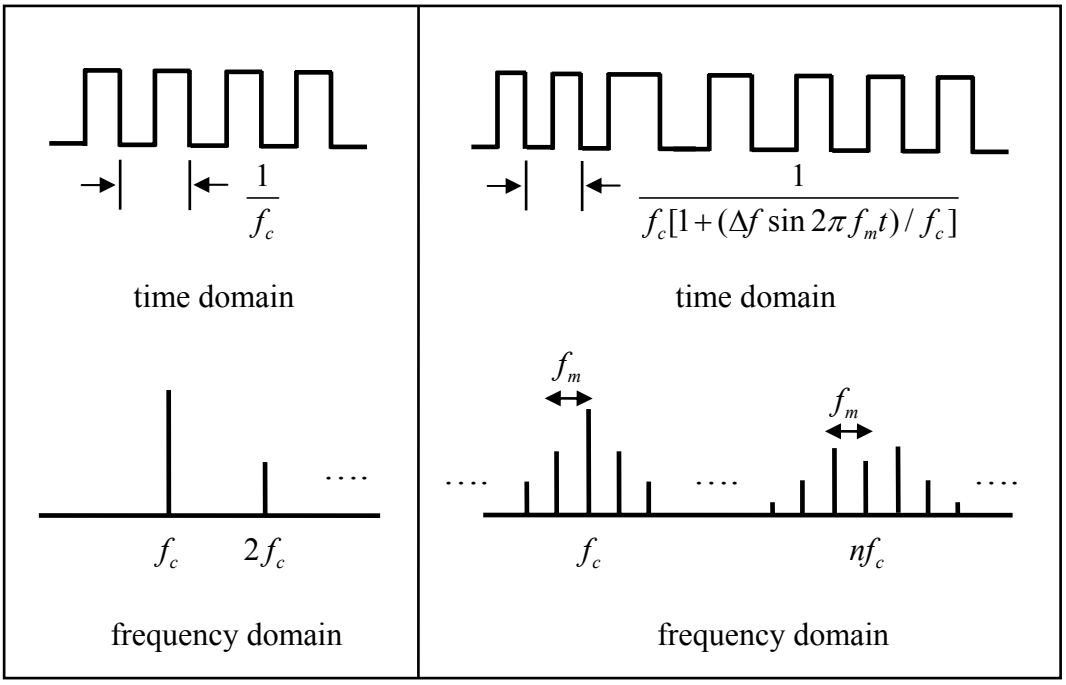


Figure 2.4: Spectra of pulse train waveform

Notice that, the frequency difference between each two adjacent side-band harmonics is still f_m, and an ideal square wave is composed of infinite sinusoidal components. For a frequency-modulated pulse train, the modulation index of each switching harmonics β_n is different, then $\beta_n = n\beta$. where n is the number of switching harmonics of the un-modulated pulse train. Carson's Rule applies to each harmonic, i.e.,

$$B_{nT} = 2(n\beta + 1) f_m . \tag{2-2}$$

If $\beta \gg 1$, then

$$B_{nT} = nB_T . \tag{2-3}$$

Thus, the higher harmonic number, the more is the spread-out power.

2.2 SSC Requirement in Serial-ATA

Figure 2.5 shows the Serial-ATA requirement for the 6Gbps transceiver system [7]. The frequency varies with time, a down spreading of 5000 ppm and a 30~33 kHz

triangular modulation rate. The frequency deviation is 6 MHz so the lowest frequency is 1.194 GHz. Down spreading frequency modulation ensures the highest frequency is below the original frequency, 1.2 GHz. Typical, the modulation frequencies should be above the 30 kHz audio band but low enough to avoid system timing problems. Serial-ATA specification define the 30~33 kHz triangular modulation rate.

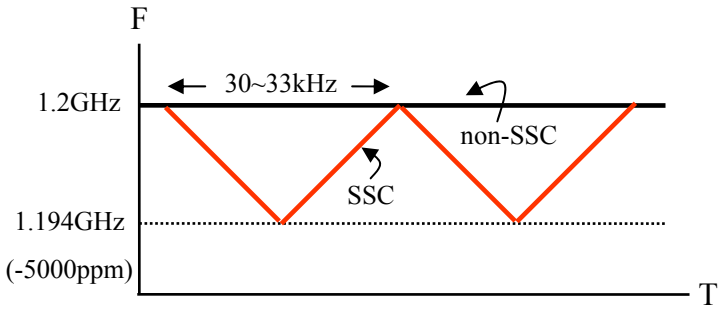
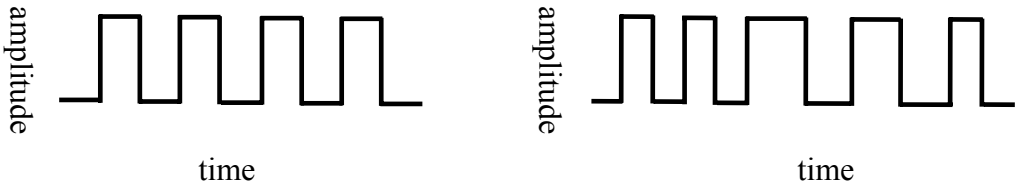


Figure 2.5: Spread spectrum requirement for Serial-ATA

2.3 Time Domain Impacts of SSC

SSC is a technique of frequency modulation. In frequency domain, the clock frequency is spreading; the energy is spread out as well. In time domain, the frequency varies periodically with time, so does the period of clock. As shown in Figure 2.6, the period of modulated signal varies with time and its change depends on the modulation profile. Due to the variation of modulated signal period, the impacts on timing are important [8].



(a) un-modulated signal (b) modulated signal

Figure 2.6: Time domain behavior of SSC

Despite of spreading of energies, the clock signal is still a square wave. Thus, we can define the cycle-to-cycle jitter and the long-term jitter of the SSC system.

A. Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is the change in a clock's output transition from its corresponding position in the previous cycle. Figure 2.7 shows a graphical representation of the cycle-to-cycle jitter [9].

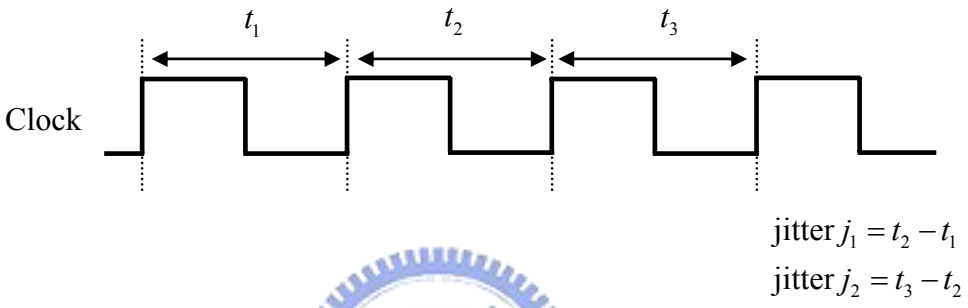


Figure 2.7: Graphical representation of cycle-to-cycle jitter

The period difference between the maximum and minimum frequencies in a SSC system is

$$\Delta T_{total} = \frac{1}{(1-\delta) f_{nom}} - \frac{1}{f_{nom}} \approx \frac{\delta}{f_{nom}}, \tag{2-4}$$

where f_{nom} is the non-spread frequency, δ specifies the total amount of spreading as a relative percentage of f_{nom}.

The number of clock cycles that exist in the time interval that the modulated clock migrates from f_{nom} to $(1-\delta) f_{nom}$ can be found as

$$N = f_{avg} \cdot \frac{1}{f_m} \cdot \frac{1}{2} = \frac{f_{avg}}{2 f_m}, \tag{2-5}$$

where f_{avg} is the average frequency of the spread spectrum clock, f_m is the modulation frequency.

Because the modulation profile is symmetric, we can only consider the f_{avg} in half of the modulation period.

$$f_{avg} = (1 - 0.5\delta) \cdot f_{nom} \quad . \tag{2-6}$$

We can rewrite Eq. 2-6 as

$$N = \frac{f_{avg}}{2f_m} = (1 - 0.5\delta)\frac{f_{nom}}{2f_m} . \tag{2-7}$$

Combining Eq. 2-6 and Eq. 2-7, the cycle-to-cycle period change, i.e., the increase in cycle-to-cycle jitter due to SSC, can be expressed as

$$\Delta T_{c\text{-}c} = \frac{\Delta T_{total}}{N} = \frac{2\delta}{1 - 0.5\delta} \cdot \frac{f_m}{{f_{nom}}^2} . \tag{2-8}$$

In our design, the spread spectrum clock generator with a down spreading of 5000 ppm and a 30 kHz modulation rate, the increase cycle-to-cycle jitter is

$$\Delta T_{c\text{-}c} = \frac{2 \cdot 0.5\%}{1 - 0.5 \cdot 0.5\%} \cdot \frac{30 \cdot 10^3}{(1.2 \cdot 10^9)^2} = 2.08855 \cdot 10^{-16} \ sec . \tag{2-9}$$

B. Long-Term Jitter

Long term jitter is defined that maximum change in a clock's output transition from its ideal position. Figure 2.8 shows the graphical representation of long-term jitter [9].

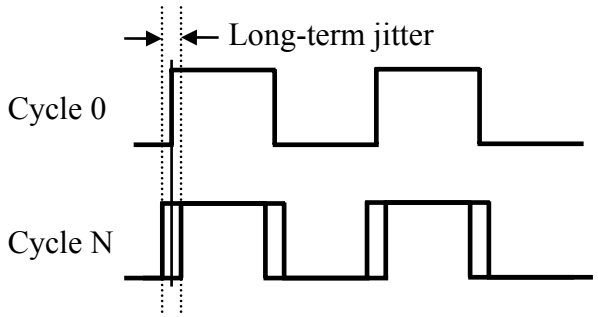


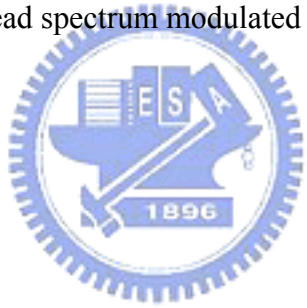
Figure 2.8: Graphical representation of long-term jitter

According to the definition above, Eq. 2-4 can be viewed as the long-term jitter of a down-spreading clock signal. The amount of long-term jitter is positively proportional to the modulation amount, negatively proportional to the nominal frequency, and is unconcerned with the other modulation factors.

In our design, the spread spectrum clock generator with a down spreading of 5000 ppm and a 30 kHz modulation rate, the increase long-term jitter is

$$\Delta T_{total} \approx \frac{\delta}{f_{nom}} = \frac{0.5\%}{1.2 \cdot 10^{9}} = 4.1667 \cdot 10^{-12} sec . \quad (2\text{-}10)$$

For the examples above, we can find that the cycle-to-cycle jitter of SSC system can be ignored. The Serial-ATA specification define a 5000 ppm down-spreading at 30~33 kHz modulation rate, there are many clock cycles pass by the reference period. The long-term jitter of the spread spectrum modulated signal is tremendous [10].



Chapter 3

Fractional-N Phase-Locked-Loop with ΣΔ modulator

The *Phase-Locked Loop* (PLL) has become an important technique to generate signals in radio and timing applications. Traditionally, fractional-N uses analog compensation mechanisms to suppress spurious signals. In recent years, there is an emerging activity for all-digital fractional-N implementation involving oversampling and noise shaping *sigma-delta modulators* (ΣΔ modulator). Several papers and products related to this technology have been published and put into market [11]. Since this method provides several advantages over the analog compensation method. It is the main architecture for today's fractional-N PLLs. In this chapter, we discuss the PLL fundamental theory and the fractional-N mechanism.

3.1 Phase-Locked Loop Fundamentals

A *Phase-Locked Loop* (PLL) is able to lock the output phase of frequency to an input reference by means of negative-feedback loop. A simple PLL consisting of a

Phase Detector (PD), a *Loop Filter* (LF) and a *Voltage Controlled Oscillator* (VCO) is shown in Figure 3.1. The PD served as an "error amplifier" in the feedback loop that is to minimize the phase difference $\Delta\phi$ between $\phi_{in}(t)$ and $\phi_{out}(t)$. The loop is considered "locked" if $\Delta\phi$ is constant with time, the result between the input and output frequency is equal [12].

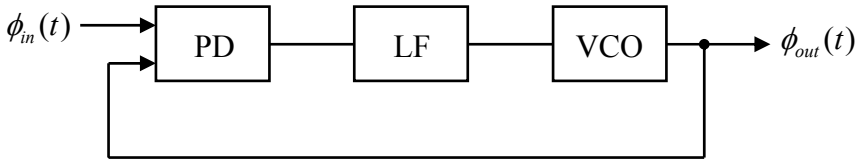


Figure 3.1: Simple phase-locked loop

In the locked condition, all the signals in the loop have reached a steady state and the PLL as follows. The PD produces an output whose pulse width is proportional to $\Delta\phi$. The LF suppresses high frequency components in the PD output and generates the DC value to control the VCO frequency. The VCO then oscillates at a frequency equal to the input frequency with a phase difference equal to $\Delta\phi$. The typical waveform of PLL is shown in Figure 3.2.

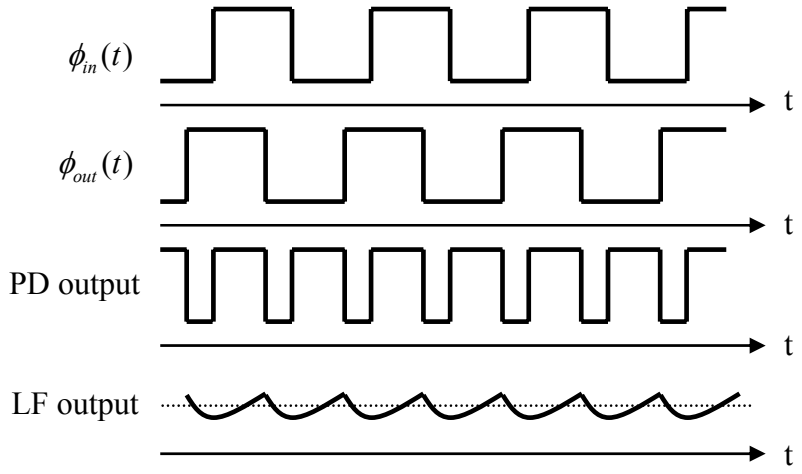


Figure 3.2: Waveform in a PLL

From a frequency perspective, if the input frequency w_{in} is momentarily greater than the output frequency w_{out}, $\phi_{in}(t)$ will accumulate phase faster than $\phi_{out}(t)$ and the PD generates increasingly wider pulses. These pulses make the higher DC voltage at the output of the LF, then the VCO frequency increasing.

The above analysis provides the tracking capabilities of a PLL. It is important to note that the loop locks only after two conditions have been satisfied:

(1) w_{out} is equal to w_{in}

(2) The phase difference $\Delta\phi$ has settled to proper value.

If the two frequencies become equal at a point in time but $\Delta\phi$ does not establish the required control voltage for the VCO, the loop must continue transient temporarily and makes the frequencies unequal again.

Figure 3.3 shows a block diagram of a typical PLL. The internal feedback signal "F_{div}" from the divider is compared to the external reference signal "F_{ref}" by *Phase Frequency Detector* (PFD). PFD generates lead or lag message to *Charge Pump* (CP). The CP will charge or discharge the loop filter to vary the VCO output frequency according to the phase difference detected by the PFD. Then the VCO oscillates at a frequency equal to the N times input frequency with a phase difference. Finally, the frequency of F_{div} can be adjusted according to synchronous the input signal and F_{out} will become $N \times F_{ref}$ in steady state.

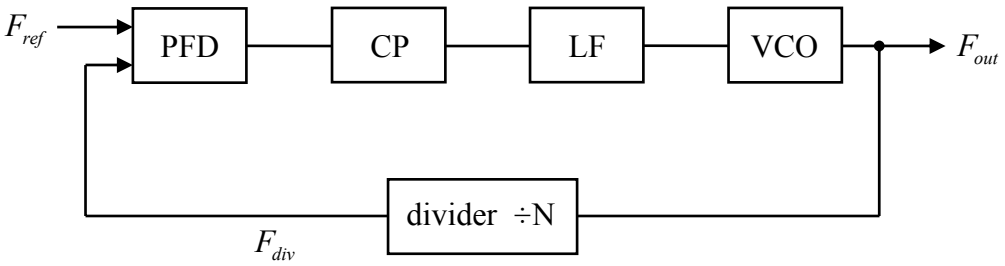


Figure 3.3: Block diagram of a typical PLL

3.2 Phase-Locked Loop Linear Model

We can use a linear approximation to gain intuition and understand the trade-off in the PLL design. Figure 3.4 shows a linear model of PLL [13]. The model is to provide the overall transfer function for the phase. The PFD with charge pump and has a gain K_{PFD} is represented simply. The LF can be represented with S domain transfer function $Z_{LF}(s)$. K_{VCO} is gain of the VCO with unit of $^{rad/s}/V$. Since integration is a linear operation on the VCO's output frequency, frequency divider is also divider the output phase by a factor of N.

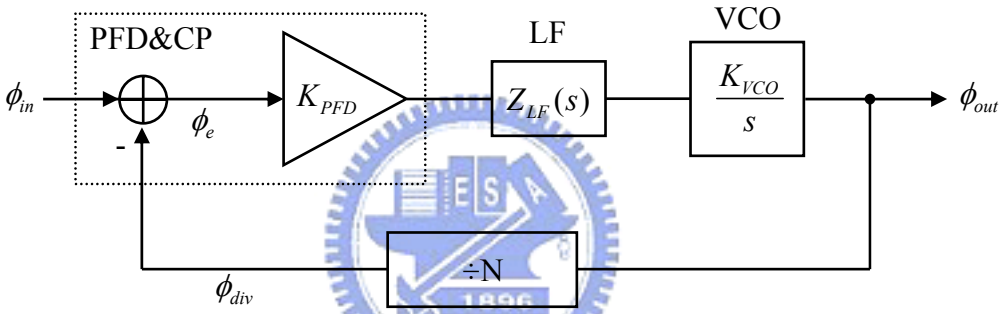


Figure 3.4: Linear model of PLL

The forward gain of the PLL is therefore derived as

$$G(s) = \frac{\phi_{out}}{\phi_e} = \frac{K_{PFD} Z_{LF}(s) K_{VCO}}{s}. \tag{3-1}$$

The reverse loop gain is

$$H(s) = \frac{\phi_{div}}{\phi_{out}} = \frac{1}{N}. \tag{3-2}$$

Then, the close loop transfer function can be expressed as

$$\frac{\phi_{out}}{\phi_{in}} = \frac{G(s)}{1 + G(s)H(s)} = \frac{\frac{K_{PFD} Z_{LF}(s) K_{VCO}}{s}}{1 + \frac{K_{PFD} Z_{LF}(s) K_{VCO}}{s \cdot N}}. \tag{3-3}$$

The order of PLL transfer function is determined by the loop filter. We consider a linear model charge-pump PLL and the loop filter transfer function as

$$Z_{LF}(s) = R + \frac{1}{sC}. \tag{3-4}$$

We can rewrite the close loop transfer function as

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{\frac{K_{PFD}K_{VCO}}{C}(sRC+1)}{s^2 + s\frac{K_{PFD}K_{VCO}}{NC}RC + \frac{K_{PFD}K_{VCO}}{NC}} = \frac{\frac{K_{PFD}K_{VCO}}{C}(sRC+1)}{s^2 + 2\delta\omega_n s + \omega_n{}^2}. \tag{3-5}$$

Now by using the control theory, the natural frequency ω_n and damping factor δ of the system can be derived as

$$\omega_n = \sqrt{\frac{K_{PFD}K_{VCO}}{N \cdot C}}, \quad \delta = \frac{RC}{2}\omega_n. \tag{3-6}$$

3.3 Types of Noise Sources in PLL

Using above linear model, several noise sources can be added to the linear model to further examine the behavior of PLL, and the model with noise is shown in Figure 3.5. $V_{n1}(s)$ is associated with the PFD and the CP and also known as the reference noise. $V_{n2}(s)$ is introduced by the loop filter's components and $V_{n3}(s)$ is the phase noise generated by the VCO.

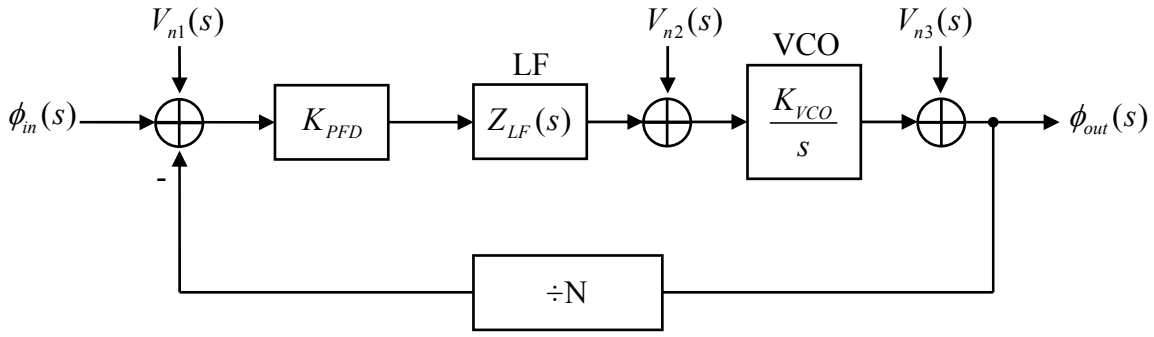


Figure 3.5: Noise sources in a PLL

The $H_1(s)$, $H_2(s)$, $H_3(s)$ represents transfer function of $V_{n1}(s)$, $V_{n2}(s)$, $V_{n3}(s)$ to the output phase $\phi_{out}(s)$, respectively. They can be expressed as follows

$$H_1(s)=\frac{\phi_{out}(s)}{V_{n1}(s)}=\frac{\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{s}}{1+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{s\cdot N}}=\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{S+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{N}}, \tag{3-7}$$

$$H_2(s)=\frac{\phi_{out}(s)}{V_{n2}(s)}=\frac{\frac{K_{VCO}}{s}}{1+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{s\cdot N}}=\frac{K_{VCO}}{S+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{N}}, \tag{3-8}$$

$$H_3(s)=\frac{\phi_{out}(s)}{V_{n3}(s)}=\frac{1}{1+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{s\cdot N}}=\frac{S}{S+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{N}}. \tag{3-9}$$

The noise transfer function of the reference noise and the filter's components are low pass while that of VCO phase noise is high pass. Figure 3.6 shows the frequency response of different noise sources. If the reference noise varies rapidly, then output phase does not fully track the variations. Physically, the "phase-lock" characteristics of PLL essentially suppress high frequency fluctuation in phase error and track the reference phase. On the other hand, VCO tends to accumulate its noise fluctuations and high pass them to the output. To achieve better noise suppression, a moderate loop bandwidth should be chosen with a trade-off between the VCO's noise and the reference noise [14].

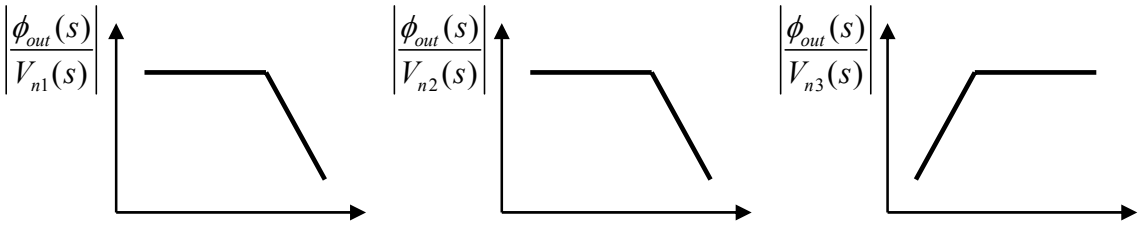


Figure 3.6: Transfer function of noise sources

3.4 Fractional-N Frequency Synthesis

When the finer frequency resolution is required, the lower reference frequency could result in narrow loop bandwidth and low switching speed [15]. A larger division ratio will also cause larger noise amplification from reference to the synthesizer output [12]. Using fractional-N frequency synthesis has the advantage of synthesize non-integer multiple output frequency with a fixed reference signal. Thus the reference frequency will not limit by the loop bandwidth as in integer frequency synthesizers. The idea comes form implementing a frequency divider that can divide the frequency from the VCO by an integer number plus a fractional part of it.

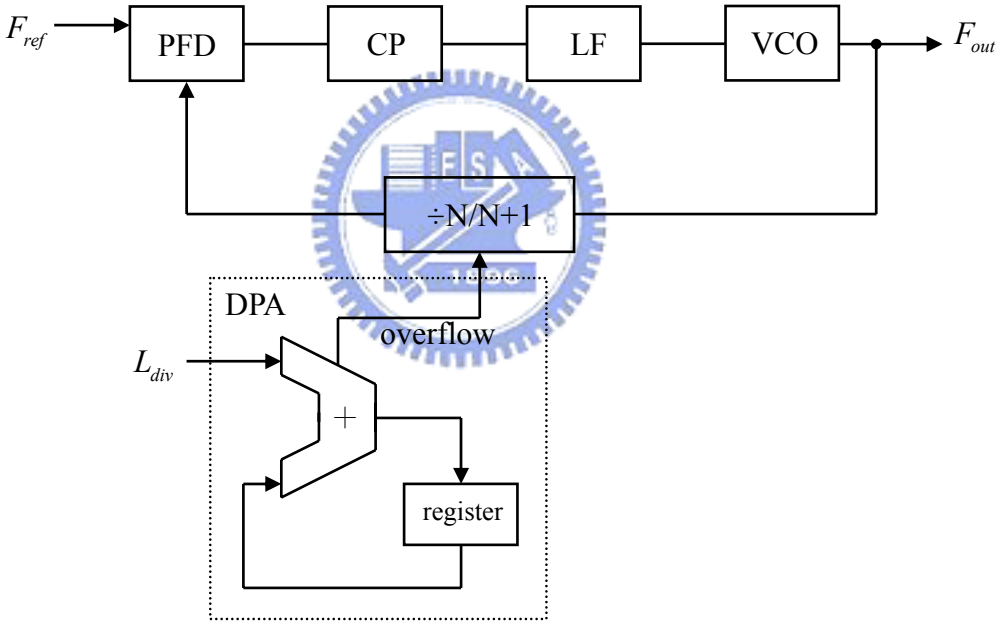


Figure 3.7: A fractional-N frequency synthesizer with divider controller

A fractional-N frequency synthesizer with a divide ratio controller is shown in Figure 3.7. This controller is simply realized by a *Digital Phase Accumulator* (DPA), and clocked by the reference frequency. The DPA accumulates its output with a divider ratio setting word L_{div} at each clock cycle. The dual-modulus divider splits its input by N as the DPA is not overflowed. As soon as overflow signal from the DPA appears, the dual-modulus divider divides its input by N+1. On average, by a

fractional value between N and N+1 can be revised as

$$N_{avg} = N + \frac{L_{div}}{L_{DPA}}, \tag{3-10}$$

where the L_{DPA} means the length of DPA. Hence, the dual-modulus divider can have a infinite frequency resolution theoretically when we increase the L_{DPA}.

However, this structure has a serious problem. It will result in sawtooth phase error in PFD. This periodic phase error will be the frequency modulated by the VCO and generates fractional spurs in the output spectrum. As shown in Figure 3.8, the periodical switch signal of the divider ratio will result in sawtooth phase error in PFD output.

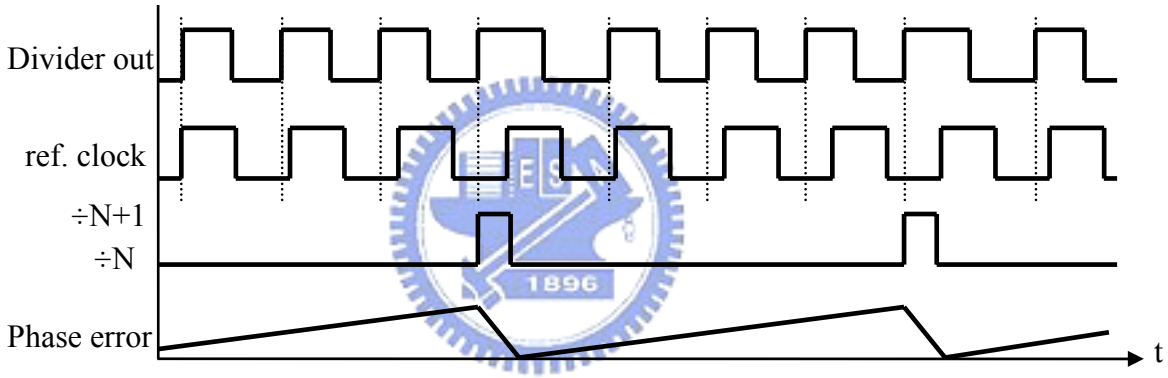


Figure 3.8: Sawtooth phase error

This periodic phase error will be frequency modulated by the VCO and generates fractional spurs in the output spectrum. As shown in Figure 3.9, the resulting fractional spurs is typically only 20 or 30 dB below center frequency and will serious degrade the purity of output spectrum [12].

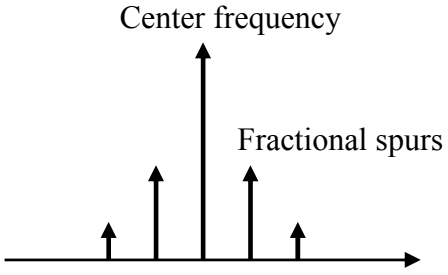


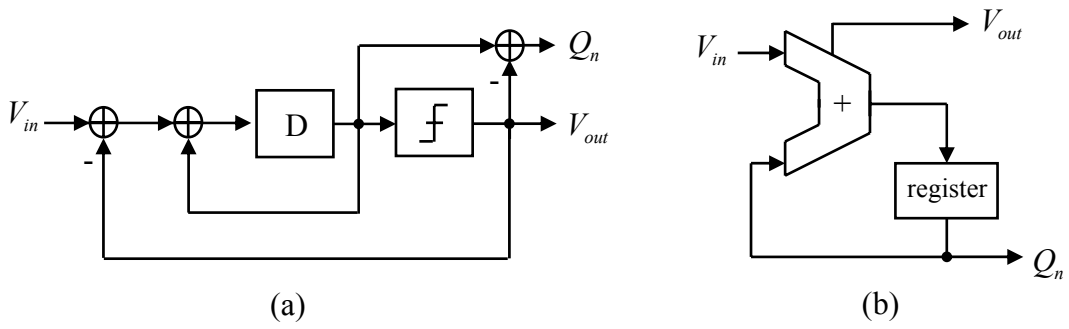
Figure 3.9: Spurious noise in VCO output spectrum

In fact, the DPA can be viewed as the first-order sigma-delta modulator. Theoretically, the higher order sigma-delta modulator suppresses more fractional spurs. Details for sigma-delta modulator techniques will be discussed later.

3.5 Sigma-Delta Modulator

Sigma-delta modulator (ΣΔ modulator) is widely used for *Analog-to-Digital converters* (ADC) and *Digital-to-Analog converters* (DAC) applications. The ΣΔ modulator leaves the average input unchanged and modulates the quantization noise to higher frequency [16]. In conventional sigma-delta DAC, the output of the modulator is followed by an analog low pass filter in order to remove quantization noise. Due to low pass characteristic of PLL, the out band quantization noise can be suppressed by higher order poles.

A first-order ΣΔ modulator is shown in Figure 3.10(a). The input signal feeds to the quantizer through an integrator, then the integrated output is quantized and fed back to subtract the input signal. The subtraction forms a negative feedback system and forces the quantized output to track the long term average of input signal. With the quantization set to two levels, an all digital ΣΔ modulator can be converted to the form given by Figure 3.10(b). Such a first-order ΣΔ modulator is also called DPA, which is described previous. DPA can totally replace the ΣΔ modulator in all digital applications such as DAC and fractional-N frequency synthesis [17].



(a) (b)

Figure 3.10: Block diagram of first-order (a) ΣΔ modulator, (b) DPA representation

To analyze the first-order ΣΔ modulator, several assumptions must be made so that the linear model can be applied [18], and the linear model of a first-order ΣΔ modulator is shown in Figure 3.11. The quantization noise can be thought of as white noise that is uncorrelated to the input signal under linear assumption. Thus, the quantizer is simply equivalent to an adder that adds the quantization noise source to the integrated signal.

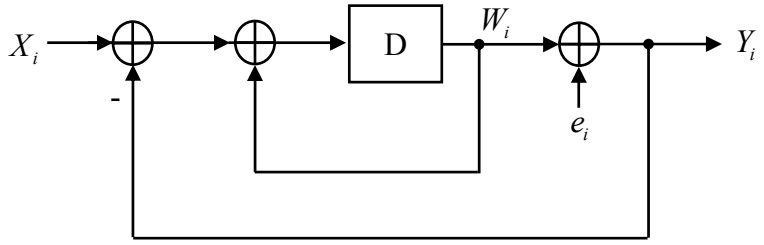


Figure 3.11: Linear model of first-order sigma-delta modulator

In z domain, the transfer function of first-order ΣΔ modulator can be written as

$$Y(z) = X(z) \cdot z^{-1} + E(z)(1 - z^{-1}), \tag{3-11}$$

where z^{-1} term is referred to as STF (Signal Transfer Function) and $1 - z^{-1}$ is NTF (Noise Transfer Function) in this modulator.

The absolute value of STF should be unity to track the input average value in the long term. It is known that an additional zero in the origin will make transfer function slope sharper by 20 dB/dec. Using more zeros at the origin can enhance the high-pass characteristics of ΣΔ modulator. The NTF of higher order ΣΔ modulator can be written as $(1 - z^{-1})^m$, where m is the order of modulator. After integration, the fluctuation in frequency is converted to phase domain and represented as phase noise. The detail mathematical calculation is refer to [19], and the power spectrum density of NTF can be written as

$$L(f) = \frac{(2\pi)^2}{12 f_s} \cdot \left[2\sin(\pi \frac{f}{f_s}) \right]^{2(m-1)}, \tag{3-12}$$

where f_s is oversampling rate and m is order of ΣΔ modulator.

The phase noise generated by quantization noise of ΣΔ modulator is plotted with second-order, third-order and fourth-order structures as shown in Figure 3.12. The improvement in *Signal-to-Noise Ratio* (SNR) is significant especially when higher order ΣΔ modulator is used.

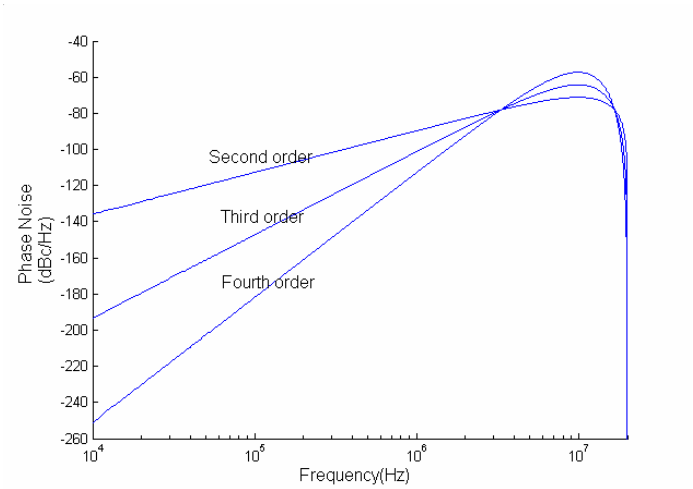


Figure 3.12: Quantization noise of second to fourth ΣΔ modulator

With oversampling and noise shaping characteristics, ΣΔ modulators are quite suitable for fractional-N synthesis applications. With higher order modulation, the quantization noise is pushed more out of band and a higher SNR can be gained at a given oversampling ratio.

3.6 MASH 1-1-1 Sigma-Delta Modulator

Higher order ΣΔ modulator can suppress more fractional spurs effectively, but they tend to become "unstable". The single-loop higher order ΣΔ modulator architecture offers a higher flexibility in terms of noise shaping; however, it has instability problem and is more complex. The *Multi-Stage-Noise-Shaping* (MASH) modulator is another structure that can achieve high order noise shaping by cascade several first-order modulators. It can solve instability problem and can be designed easily. Figure 3.13 shows a typical third-order MASH 1-1-1 ΣΔ modulator that is formed by cascading three first-order ΣΔ modulators [20].

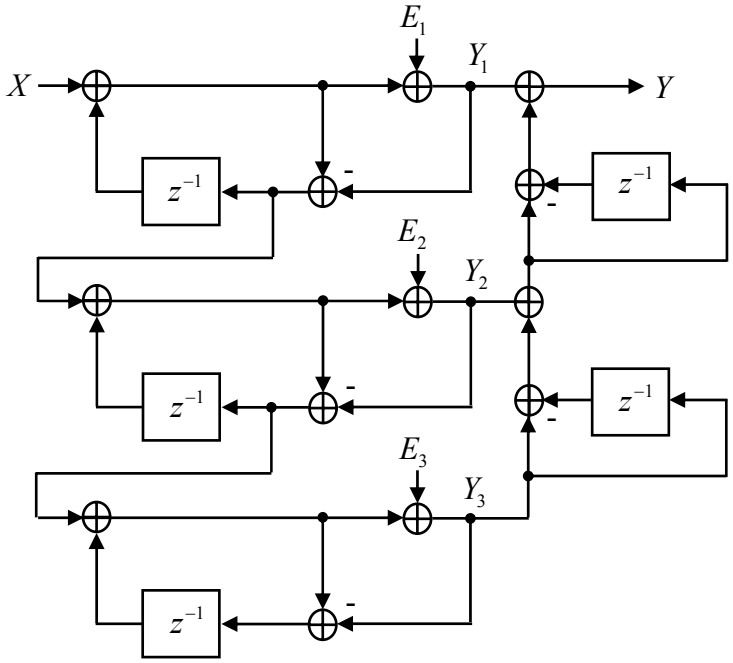


Figure 3.13: Third-order MASH 1-1-1 ΣΔ modulator

The quantization error of the first modulator is fed to the second modulator and the second modulator's quantization error is fed to the third. The equations of the individual modulators can be written as

$$\begin{aligned} Y_1(z) &= X(z) + E_1(z)\cdot(1 - z^{-1}) \\ Y_2(z) &= -E_1(z) + E_2(z)\cdot(1 - z^{-1}), \\ Y_3(z) &= -E_2(z) + E_3(z)\cdot(1 - z^{-1}) \end{aligned} \tag{3-13}$$

where $E_1(z)$, $E_2(z)$ and $E_3(z)$ each represents the quantization noise of the three modulators. Combination of above equations, the transfer function of MASH 1-1-1 ΣΔ modulator is

$$\begin{aligned} Y(z) &= Y_1(z) + Y_2(z)\cdot(1 - z^{-1}) + Y_3(z)\cdot(1 - z^{-1})^2 \\ &= X(z) + E_3(z)\cdot(1 - z^{-1})^3 \end{aligned} . \tag{3-14}$$

The quantization error of third-order modulator is noise shaped by placing three zeros at the origin.

Chapter 4

Spread Spectrum Clock Generator Implementation

4.1 Implementation of SSCG

There are many types of *Spread Spectrum Clock Generator* (SSCG) in the literature [21], [22], [23], [24]. Figure 4.1 shows the different approaches of SSCG. The first type modulates the VCO directly. Using another charge pump to generate the triangular wave in to the low pass filter and modulating the PLL output clock. Due to the process variation, this analog approach may need calibration to sure 5000 ppm spread amounts. The second type modulates the divider in a PLL to modulate the output frequency of PLL. The third type combines the multiphase circuits to achieve the spread-spectrum function. This approach needs multiphase and has large load, so the power consumption is very large. Finally, the forth type modulates the PLL output phases to the divider. The phase jump of it is less than type II, and the power consumption is lower than type III. In this thesis we accomplish the SSCG based on this architecture. Details for SSCG architecture of our design will be discussed latter.

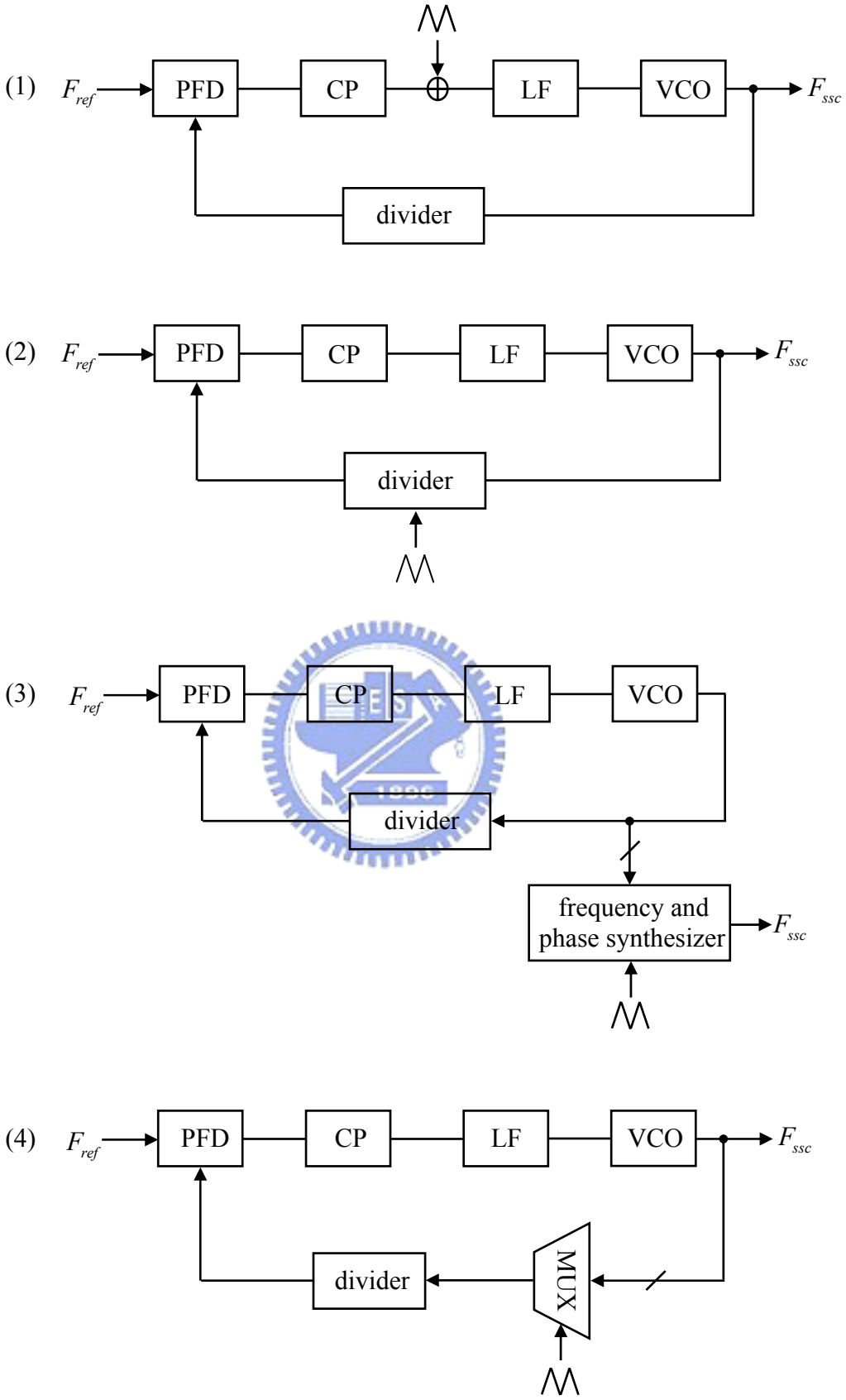


Figure 4.1: Types of SSCG architecture

4.2 Spread Spectrum Clock Generator Architecture

A building block of the accomplished SSCG is shown in Figure 4.2. The SSCG is based on a fractional-N PLL using sigma-delta modulation technique. The address generator is used to produce a 30 kHz triangular modulation rate and a 5000 ppm frequency deviation of the SSCG. It is the control signal of the ΣΔ modulator. The controller receives the signals from ΣΔ modulator to control the multiplexer for select the suitable phase to divider. When the VCO output phases deliver to the divider be changed that is equivalent to change the divider ratio. Hence, when we modulated the VCO output phases and make the equivalent divider ratio is triangular modulation it will generate a triangular modulation profile on the loop filter to achieve our goal.

Although the power consumption of this architecture is larger but the phase jump is lower [24], and the modulation profile will be more smoothly. The behavior simulation results of the modulation divider type SSCG and the modulation VCO phases type SSCG will show in chapter 5.

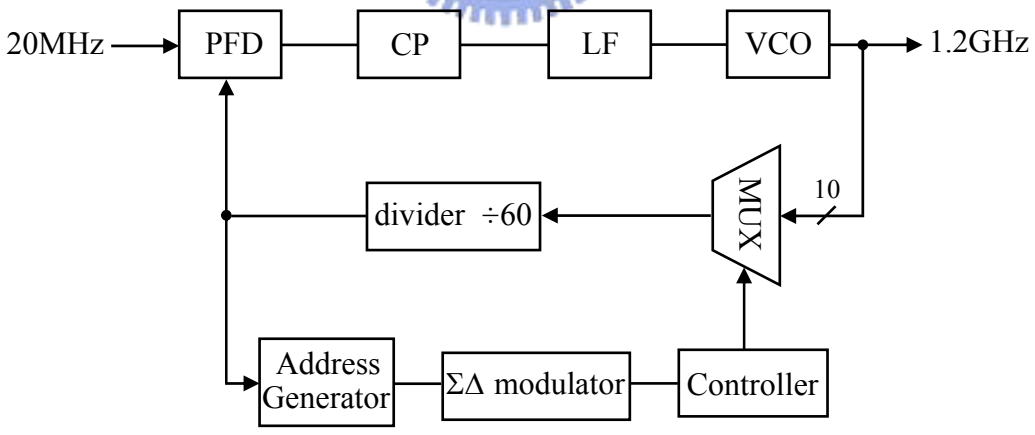


Figure 4.2: System architecture of spread spectrum clock generator

■ Phase Frequency Detector

The *Phase Frequency Detector* (PFD) is composed of two *D-flip flops* (DFF) and a NOR gate, as shown in Figure 4.3 (a) [25]. When the outputs of two DFFs are

both active, the two DFFs will be reset. The two transmission gates of PFD are used to balance the timing. The *True Single Phase Clock* (TSPC) type DFFs of the PFD are used at high speed operation as shown in Figure 4.3 (b).

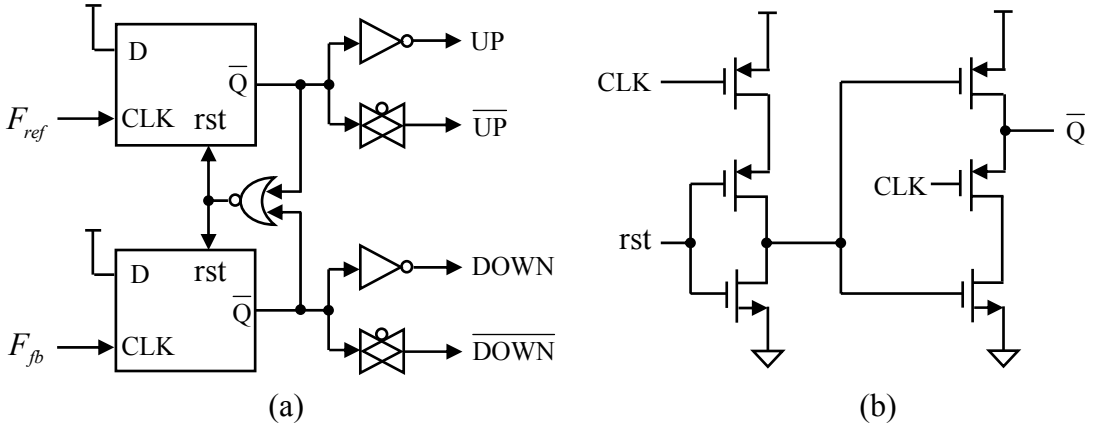


Figure 4.3: Circuit schematic of (a) PFD (b) TSPC D flip-flop of PFD

The conventional PFD generates phase jitter since it does not have sufficient turn on time to change the control voltage when phase difference is within the dead zone. The advantage of this PFD is that it has no deadzone. Figure 4.4 is the timing diagram of this PFD. For in-phase inputs of F_{ref} and F_{fb}, the charge pump will see both "UP" and "DOWN" pulses for the same short period of time. If there is a phase difference between F_{ref} and F_{fb}, the distinction between the widths of UP and DOWN pulses will be proportional to the phase differences of the inputs.

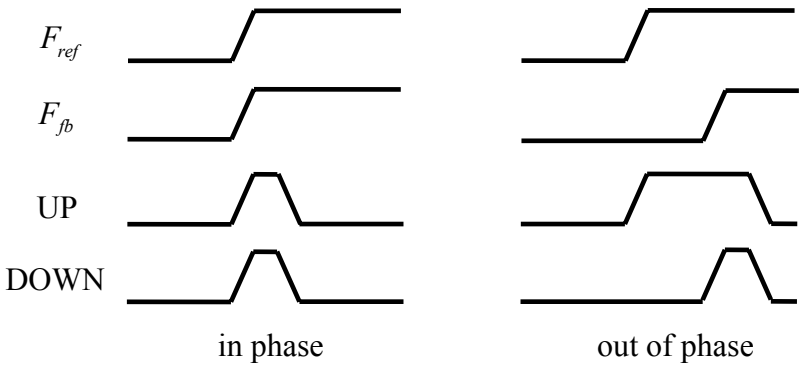


Figure 4.4: Timing diagram of PFD

■ Charge Pump

The *charge pump* (CP) is used to convert the logic states of the PFD into analog signals suitable for controlling the VCO. The architecture of CP is shown in Figure 4.5 [26], it consists of two current source, four current switches and an *operational amplifier* (OP-amp). The unity gain buffer will maintain the voltage of intermediate node to the same as the output node when the switch is off. Thus the charge in-jection will never occur when the switch is turned on. In this way, voltage glitches on the loop filter due to charge sharing can be eliminated.

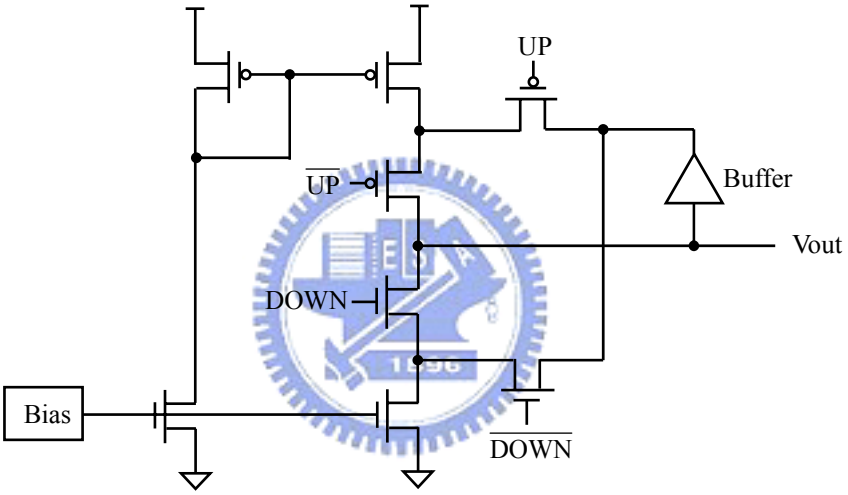


Figure 4.5: Circuit schematic of charge pump

Figure 4.6 is the waveform of the CP. The PFD generates lead or lag message to the CP. The CP will charge or discharge the loop filter to vary the VCO output frequency according to the phase difference detected by PFD.

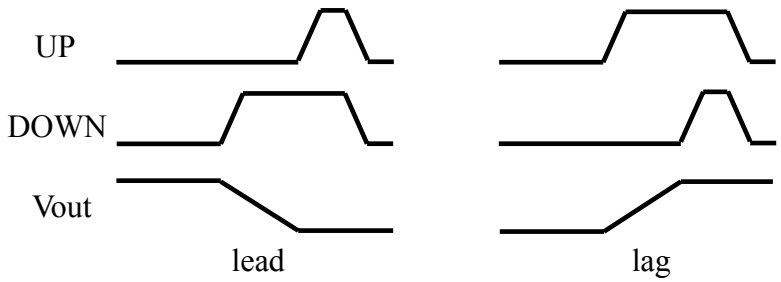


Figure 4.6: Waveform of charge pump

■ Loop Filter

The design of the loop filter determines most of the specifications of the PLL. Extra poles and zeros in the loop transfer function influence the noise and dynamic performance of the loop. The parameter of the loop filter should be carefully designed. As shown in Figure 4.7, we consider second-order loop filter to design type-II current mode charge pump PLL system.

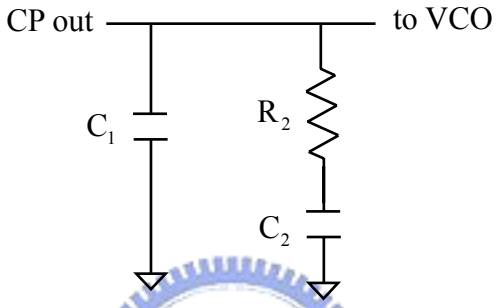


Figure 4.7: Schematic of second-order filter

The impedance of second-order filter in Figure 4.7 is

$$Z(s)=\left[\left(R_2+\frac{1}{sC_2}\right)//\frac{1}{sC_1}\right]=\frac{1}{s(C_1+C_2)}\cdot\frac{sR_2C_2+1}{sR_2(C_1//C_2)+1}. \quad (4\text{-}1)$$

Then, we can define the time constants which determine the pole and zero frequencies of the filter

$$T_1=R_2(C_1//C_2)\ ,\ T_2=R_2C_2\,. \quad (4\text{-}2)$$

Generally, we can design the loop filter using open loop gain bandwidth ω_p and phase margin ϕ_p to determine the passive component values [27]. High phase margins provide with stable system and can decrease peaking response of the loop filter at the expense of degrading the lock time of the PLL. In general, the phase margin is chosen between 45 and 60 degrees. Choosing the loop bandwidth too small will yield a design with improved reference spurs and RMS phase error, but will increase the locking time. In general, the suggested method of choosing the loop

bandwidth is to choose it so that it is sufficient to meet the lock time requirement with sufficient phase margin.

Locating the point of minimum phase shift at the unity gain frequency of the open loop response as shown in Figure 4.8 ensures loop stability.

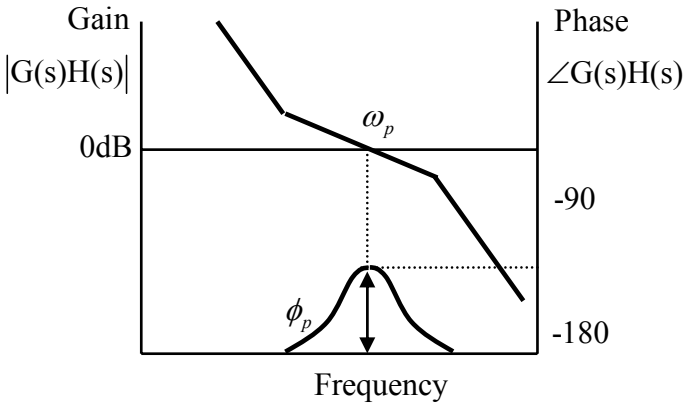


Figure 4.8: Open loop response bode plot

The formulas for T_1 and T_2 are shown in Eq. 4-3.

$$T_1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p}, \quad T_2 = \frac{1}{\omega_p{}^2 \cdot T_1}. \tag{4-3}$$

Then, we can achieve passive component values as

$$C_1 = \frac{T_1}{T_2}\frac{K_{PFD}K_{VCO}}{\omega_p{}^2 N}\sqrt{\frac{1+(\omega_p \cdot T_2)^2}{1+(\omega_p \cdot T_1)^2}}, \tag{4-4}$$

$$C_2 = C_2 \cdot (\frac{T_2}{T_1} - 1), \tag{4-5}$$

$$R_2 = \frac{T_2}{C_2}, \tag{4-6}$$

where K_{PFD}, K_{VCO}, N are gain of the PFD, gain of the VCO and the divider ratio.

The out-band quantization noise from ΣΔ modulator will be suppressed by the low-pass characteristic of the PLL. But ΣΔ modulator will introduce current switching

noise in the divider and CP at the reference rate. This may cause unwanted FM sidebands at RF output. As shown in Figure 4.9, an additional pole of third-order loop filter can be added to suppress the reference spur.

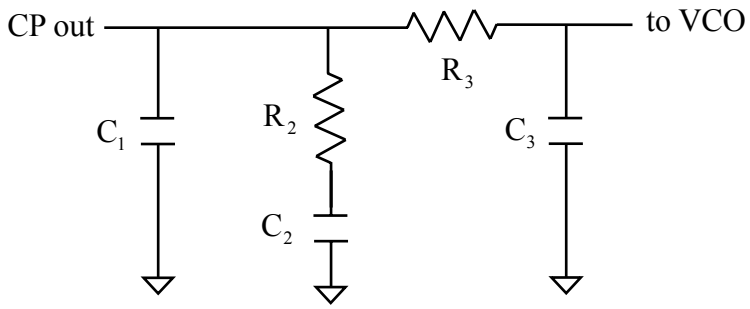


Figure 4.9: Schematic of third-order loop filter

The added attenuation from the low-pass filter is

$$ATTEN = 20 \log [(2 F_{ref} R_3 C_3)^2 + 1], \quad (4\text{-}7)$$

and we can define the additional filter time constant as

$$T_3 = R_3 C_3 . \quad (4\text{-}8)$$

Then, in terms of the attenuation of the reference spurs added by the low pass pole the formulas for T_3 can be expressed as

$$T_3 = \sqrt{\frac{10^{\frac{ATTEN}{10}} - 1}{(2\pi \cdot F_{ref})^2}} . \quad (4\text{-}9)$$

In general, we can choose $C_3 = \frac{C_1}{10}$, then $R_3 = \frac{T_3}{C_3}$.

The PLL becomes a higher order loop and stability is an important issue. So, one must be careful in determining the loop bandwidth of the system. A PLL needs a sufficiently large loop bandwidth to track the modulation rate of SSCG. But, we need to choose a small loop bandwidth to suppress the reference spur and the RMS phase error. In general, the loop bandwidth need to meet the RMS phase error to reduce jitter and it is sufficient to track the modulation rate. According to [28], the dynamic

range of the Lth-order ΣΔ modulator should meet the following condition

$$\frac{3}{2}\cdot\frac{2L+1}{\pi^{2L}}\cdot(OSR_{eff})^{2L+1}>\left(\frac{f_{PFD}}{\Delta f_n}\right)^2 \quad , \tag{4-10}$$

where OSR_{eff}, f_{PFD}, Δf_n are the oversampling ratio and the bandwidth of the PFD and the in-band noise respectively. So the approximate upper bound of the loop bandwidth is obtained as

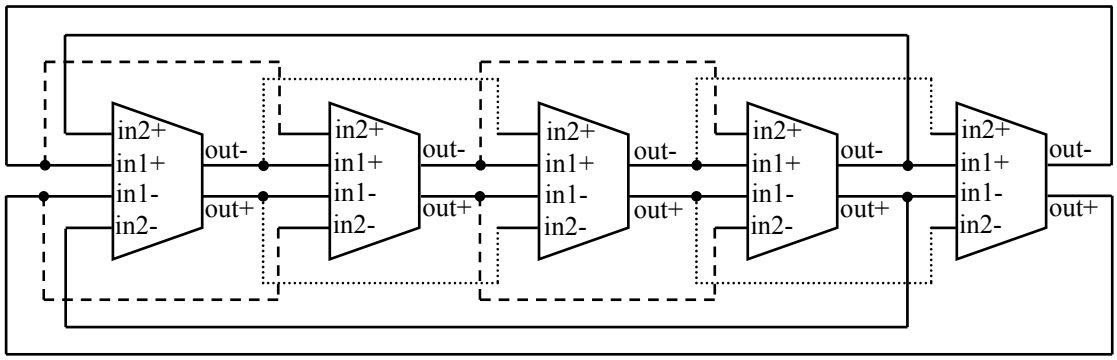
$$f_c<\left[\left(\frac{\theta_{rms}}{\sqrt{2}}\right)^2\cdot\frac{L+0.5}{(2\pi)^{2L}}\right]^{(1/2L-1)}\cdot f_{PFD}, \tag{4-11}$$

where θ_{rms} [rms rad] is the in-band phase error.

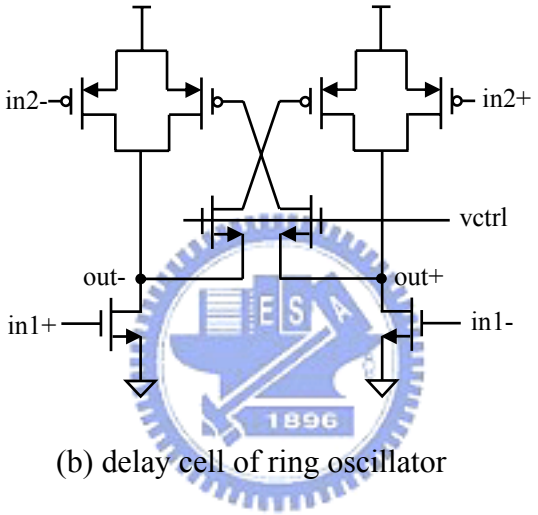
In our design, when the reference frequency of PFD is 20 MHz, the upper bound of the bandwidth with a third-order ΣΔ modulator to have less than 1^0 RMS phase error is about 448 kHz.

■ Voltage Controlled Oscillator

In a conventional ring oscillator, the oscillation frequency is determined as $1/N\tau$, where N is the number of stages and τ is the unit delay time of a delay cell. Hence the frequency of the oscillator is decided by the delay time of one delay element. The maximum frequency of the VCO is limited by the delay time of the basic inverter delay cell. Using a dual-delay scheme to implement the VCO, high operation frequency and wider tuning range are achieved simultaneously [29]. Figure 4.10 shows the circuit schematic of the VCO, which includes a 5-stage ring oscillator for frequency tuning. The dual-delay cell of ring oscillator has both the negative skewed delay paths and the normal delay paths. The negative skewed delay paths decrease the unit delay time of the ring oscillator below the single inverter delay time. As a result, higher operation frequency can be obtained.



(a) 5-stage ring oscillator



(b) delay cell of ring oscillator

Figure 4.10: Circuit schematic of VCO

■ Address Generator

The *Serial-ATA* (Serial-ATA) systems require the SSCG with a down spreading of 5000 ppm and a 30 kHz modulation rate. One can use address generator to determine the above required parameter. As shown in Figure 4.11, the address generator consists of an up/down counter and some logic gates [30]. The outputs of up/down counter are used to control the ΣΔ modulator and that produce a triangular waveform to make the frequency spreading. The more bit number of the up/down counter is used, the more accurate shape of triangular waveform will be. In this thesis, we use a 10 bit up/down counter to perform the address generator.

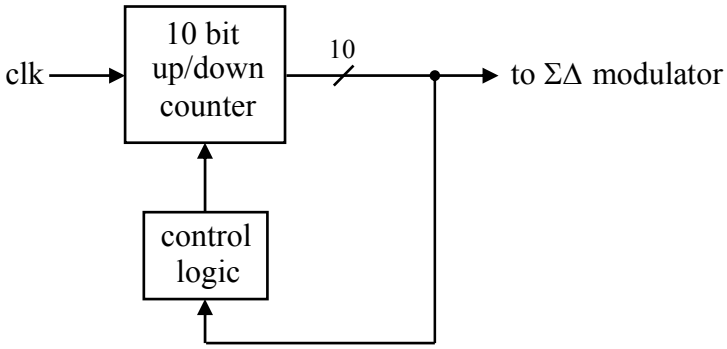


Figure 4.11: Architecture of address generator

■ Third-order MASH 1-1-1 Sigma-Delta Modulator

Higher order ΣΔ modulator can suppress more fractional spurs effectively, but they tend to become "unstable". The single-loop architecture offers a higher flexibility in terms of noise shaping; however, it has instability problem and is more complex. The *Multi-Stage-Noise-Shaping* (MASH) modulator can solve instability problem and can be implemented using all digital architectures. Thus, it can be easily integrated into single chip and is insensitive to process variation.

By performing linear analysis on this model in section 3.6, the input/output relationship of this modulator can be found as follow

$$Y(z) = X(z) + E_3(z) \cdot (1 - z^{-1})^3, \tag{4-12}$$

where $X(z)$, $Y(z)$, and $E_3(z)$ are the Z-transform of the input, output and quantization noise from three stages respectively.

The quantization error of the third-order ΣΔ modulator is noise shaped by placing three zeros at the origin. The quantization error is shaped and pushed to high frequency and then the closed loop behavior of PLL will filter it out. Using DPA to realize MASH 1-1-1 architecture is shown in Figure 4.12. With the advantage of all digital implementation in synthesizer applications, there is no analog mismatch problem for MASH type modulator.

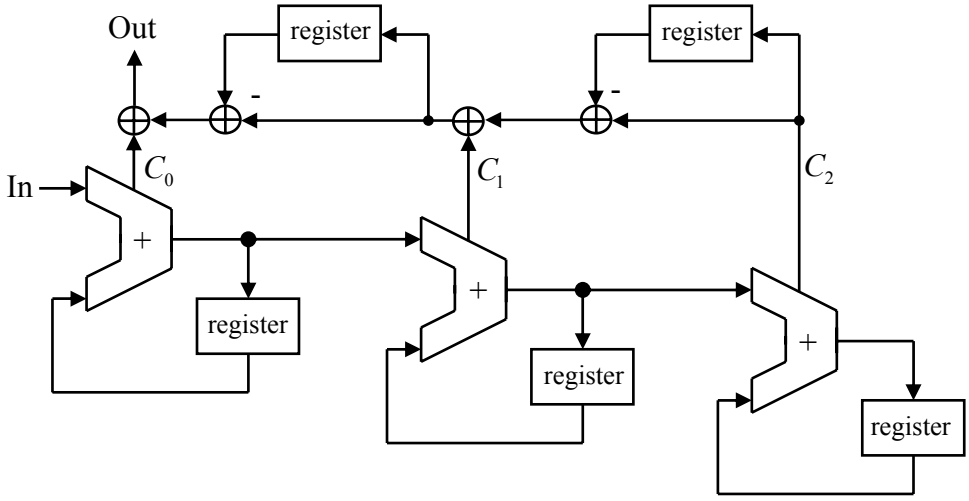


Figure 4.12: Digital realization of MASH 1-1-1 ΣΔ modulator

The input range and output spreading for a MASH 1-1-1 ΣΔ modulator is shown in Figure 4.13 [28]. For a third-order MASH 1-1-1 ΣΔ modulator, it output has 8 levels. The output average is always between N and N+1, and the output average track the long term average of the input signal.

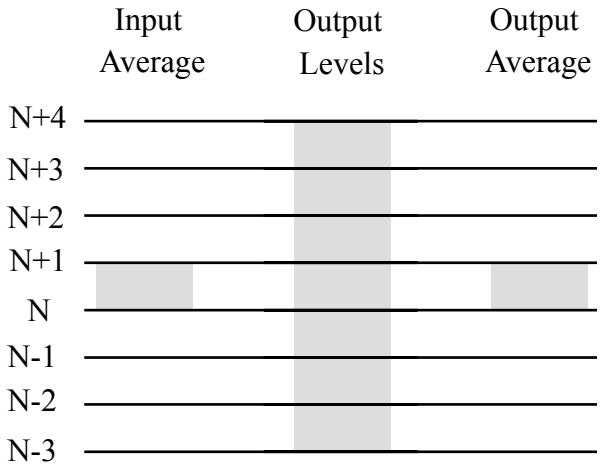


Figure 4.13: The input range and output spreading of MASH 1-1-1 ΣΔ modulator

■ Controller

The controller receives the control signal from ΣΔ modulator and control the multiplexer for the phase selection. The controller is composed of a *finite state machine* (FSM) and a barrel shifter. Due to that the MASH 1-1-1 ΣΔ modulator output has 8 levels, as shown in Figure 4.13, it makes the phase shifted greatly. It may let the divider lose the rising edge of VCO output when phase changed. Thus, the SSCG won't work successfully. The FSM makes the multiplexer shifted one phase at a time. The phase shifted one by one until complete the total phase shift. The FSM output signals control the data in the barrel shifter to rotate right, or left or hold the original value. When finishing the phase shift, the FSM will hold the data in the barrel shifter until it receives new control signal from the ΣΔ modulator for the phase shift.

The state table and state diagram of the FSM are show in Table 4.1 and Figure 4.14. The FSM receive the control signal from ΣΔ modulator and then change the state step by step to control the barrel shifter.

Table 4.1: State table of the FSM

DSM output (Decimal number)	present state	next state	Out (LRH)
4	A	B	1 0 0
3	B	C	1 0 0
2	C	D	1 0 0
1	D	E	1 0 0
0	E	E	0 0 1
-1	F	E	0 1 0
-2	G	F	0 1 0
-3	H	G	0 1 0

L: rotate left R: rotate right H: hold

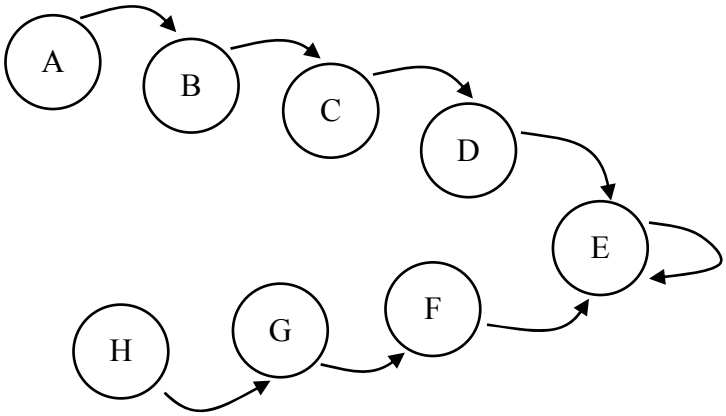


Figure 4.14: State diagram of the FSM

In fact, barrel shifter is a shifter register. In our design, we use a 3×10 barrel shifter in the controller which is shown in Figure 4.15. The 3-bit control signals from FSM are used to control the data in barrel shifter. The 10-bit data are used to control the multiplexer for phase selection and that are in one hot encoded. When FSM makes the data in barrel shifter rotated, the multiplexer changes the VCO output phases to the frequency divider.

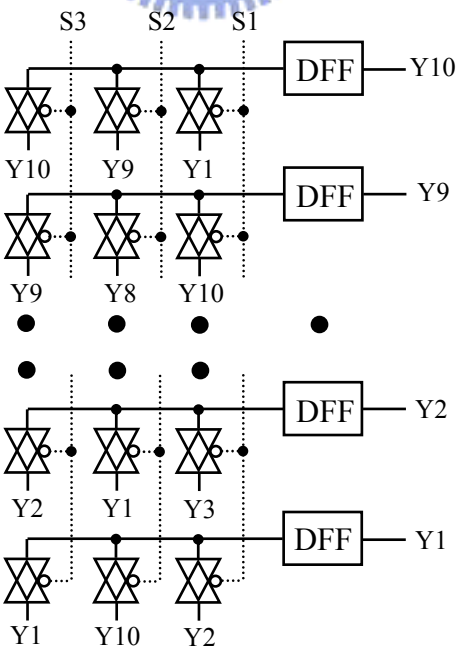
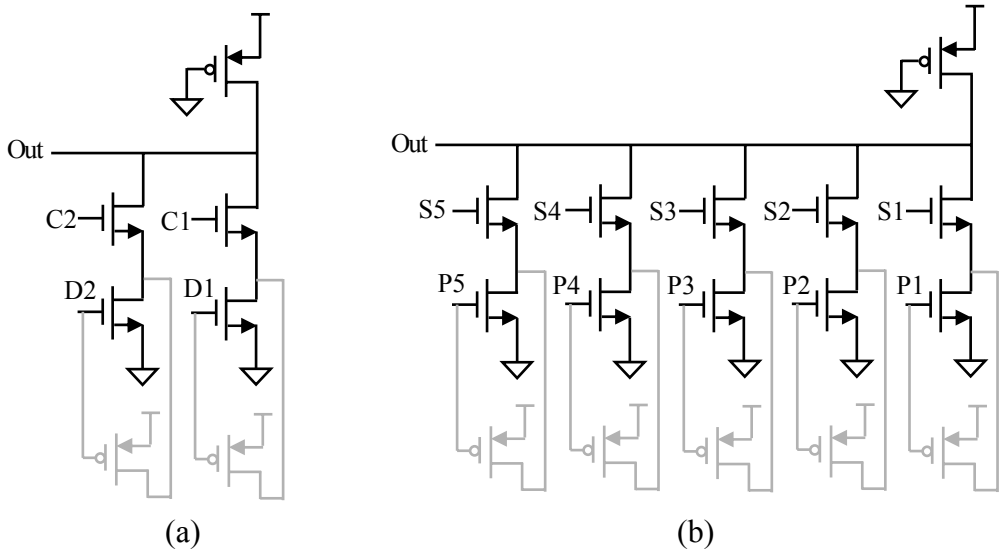


Figure 4.15: The 3×10 barrel shifter

One of the ten DFFs in barrel shifter is a reset-to-one type DFF, and others are reset-to-zero type DFFs. The reset mechanism is used to control the SSCG in the non-SSC mode or the SSC mode. When reset ten DFF s, the output phase of the MUX is fixed and the SSCG is in the non-SSC mode. Otherwise the barrel shifter changes the output phase of MUX by the FSM control signals, and the SSCG is in the SSC mode.

■ Multiplexer

The *multiplexer* (MUX) is used to select the suitable phase to the divider from VCO and the controller outputs are used to contorl it. For our design, a 10-to-1 MUX is needed and we use a 2-to-1 MUX and two 5-to-1 MUXs to perform the 10-to-1 MUX as shown in Figure 4.16 [25]. The dummy PMOS of the MUX are used to avoid the leakge current effect of the NMOS. Table 4.2 shows the relation between control signals and output of the MUX. Figure 4.17 shows the waveform when the control signals of the controller make the MUX output shift one phase. As shown in Figure 4.17, changing the VCO output phase to the divider is equivalent to changing the divider ratio. Hence, we can spread the output frequency of VCO by changing the VCO phase to the divider.



(a) (b)

Figure 4.16: Architecture of (a) 2-to-1 MUX (b) 5-to-1 MUX

Table 4.2: Relation between control signals and output of the MUX

Control Signal										Output Phase
S_{10}	S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1	
0	0	0	0	0	0	0	0	0	1	phase 1
0	0	0	0	0	0	0	0	1	0	phase 2
0	0	0	0	0	0	0	1	0	0	phase 3
0	0	0	0	0	0	1	0	0	0	phase 4
…….										…….

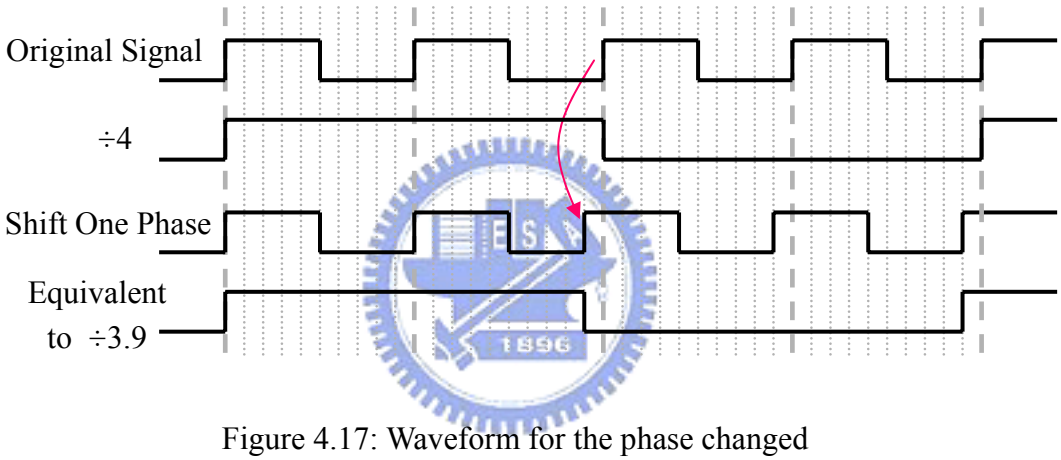


Figure 4.17: Waveform for the phase changed

■ Frequency Divider

In our design, a divide-by-60 divider is needed and we use a divide-by-3, a divide-by-4 and a divide-by-5 dividers to perform the division. The dividers are composed of DFFs and some simple logic gates. They are capable of dividing by these divisions. For operating at high speed, it is important to reduce the effective capacitance of internal and external nodes. It leads to the reduction of the propagation delay. The TSPC type DFFs have been widely used in many digital circuits because of it features of high operating speed and simple circuit requirement. Figure 4.18 shows the circuit schematic of the TSPC type DFF for the divider [26].

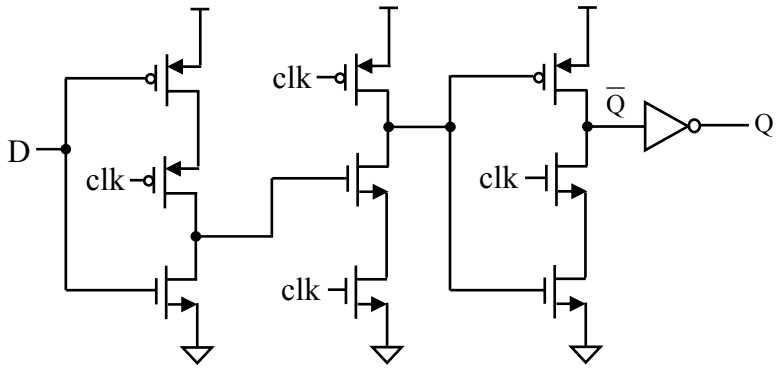


Figure 4.18: TSPC type D flip-flop

Chapter 5

Simulation and Measurement Results

The spread spectrum clock generator using fraction-N PLL with ΣΔ modulator has many system design issues. We need to consider the stability problem, the loop bandwidth, and spreading ratio, etc. Hence, the system behavior simulation of SSCG is very important. In this chapter, we verify the spread spectrum clocking function from behavior simulation to circuit level simulation. Finally, we show the measurement results of our spread spectrum clock generator chip.

5.1 SSCG Behavior Simulation

We use SIMULINK to analyze the loop stability and verify the SSC function. Figure 5.1 shows the model of SSCG system which is based on a charge-pump PLL with a third-order loop filter. Figure 5.2 shows the SSCG behavior simulation. We can see a down spreading of 5000 ppm and a 30 kHz triangular modulation rate clearly.

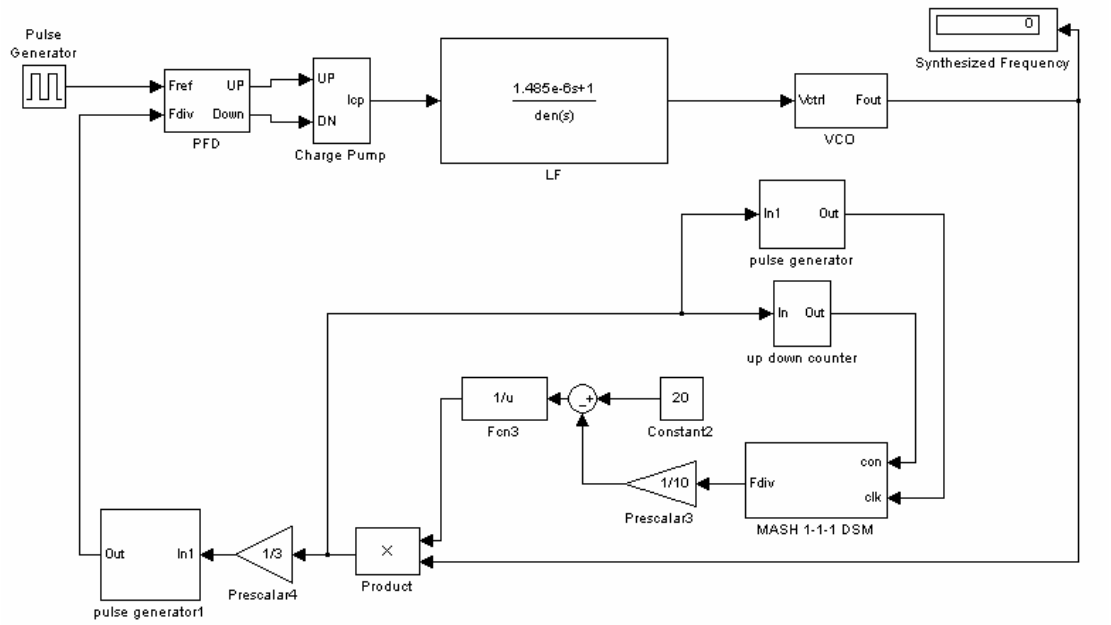


Figure 5.1: SIMULINK model of the SSCG system

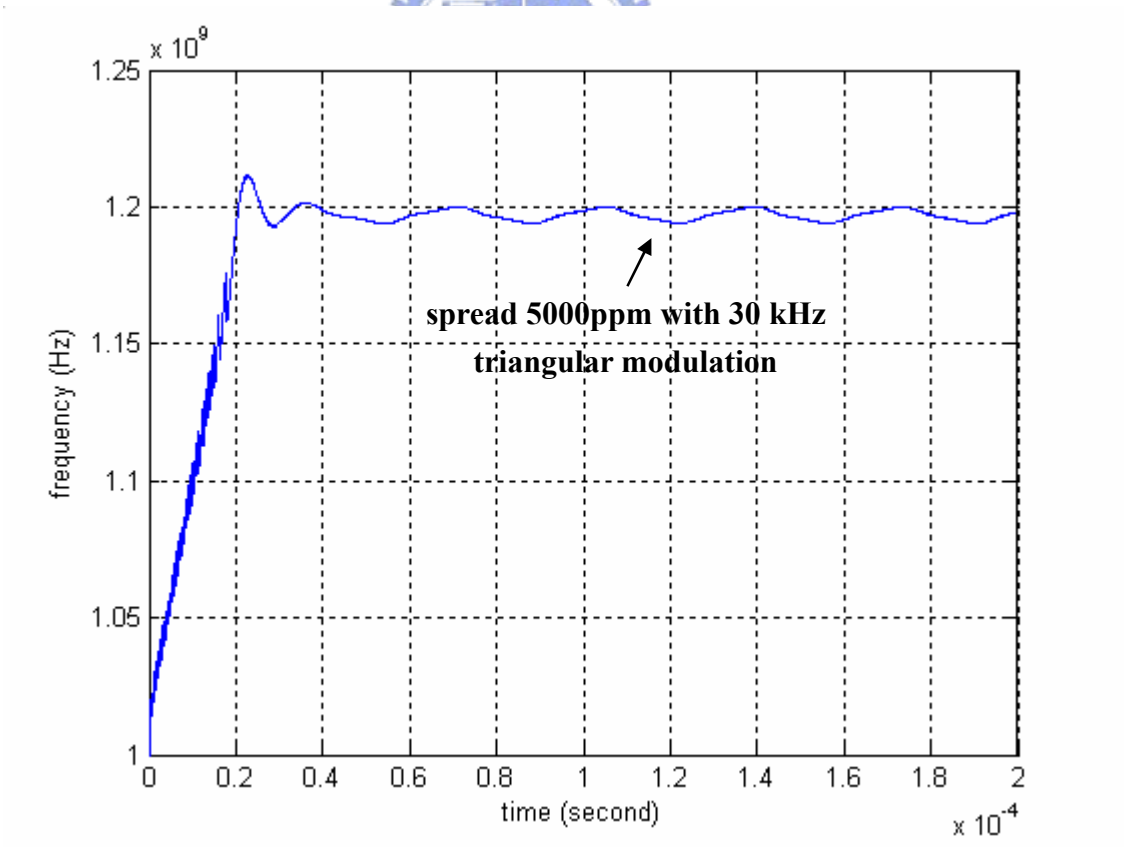


Figure 5.2: SSCG behavior simulation

According to Eq. 4-11, we choose 400 kHz for the loop bandwidth and the phase margin is 60 degree. The open-loop response bode plot of this system is shown in Figure 5.3.

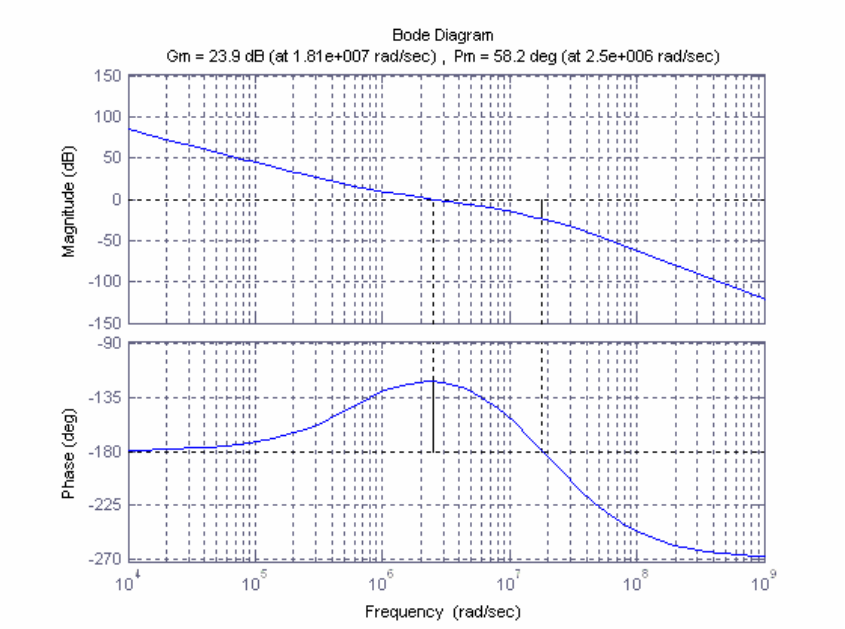


Figure 5.3: Bode plot of open-loop response

Figure 5.4 shows the FFT of SSCG at non-SSC mode and SSC mode. The peak amplitude reduction is about 20 dB. Figure 5.5 shows the comparison of two type of SSCGs. The triangular modulation waveform of modulation VCO phases type SSCG is smoother. The noise floor of this type is also lower as shown in Figure 5.6.

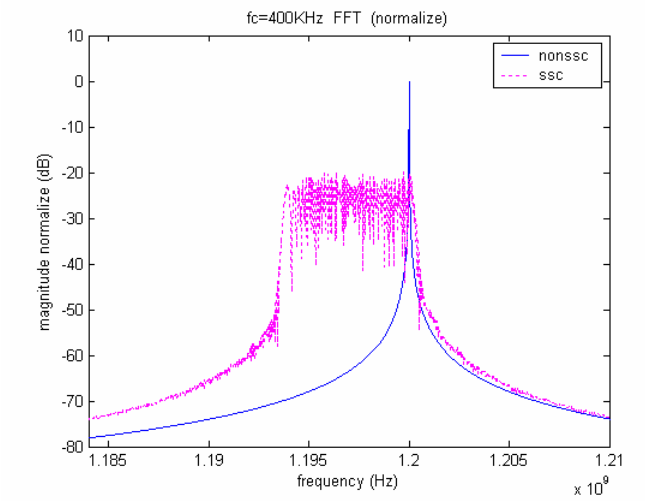
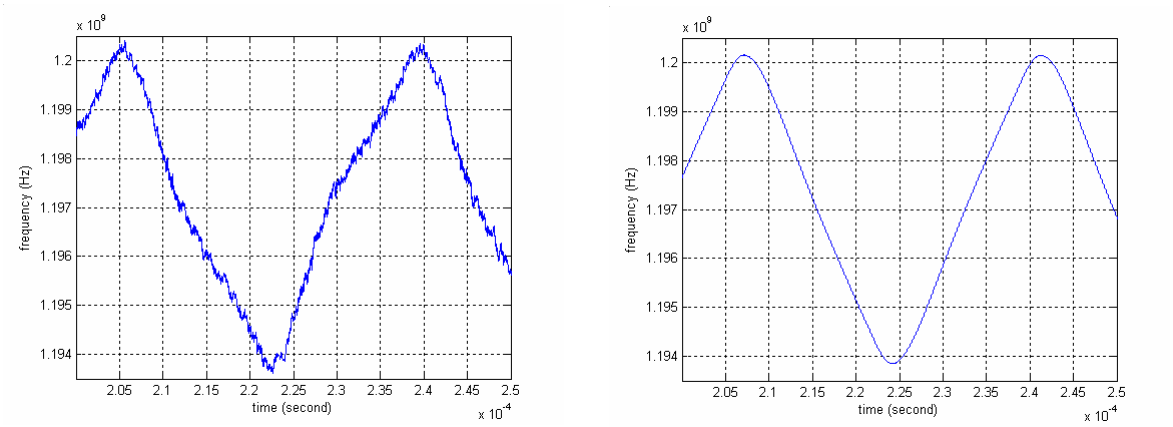


Figure 5.4: FFT of SSCG at non-SSC mode and SSC mode



(a) modulation divider (b) modulation VCO phases

Figure 5.5: Waveform of two type SSCGs

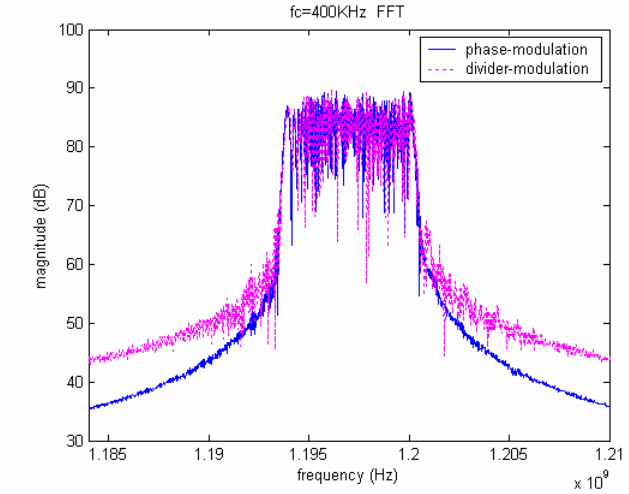


Figure 5.6: FFT comparison of two type SSCG

5.2 SSCG Circuit Level Simulation

The circuit level simulation of SSCG using HSPICE takes a significant amount of time but the results are more precise. Figure 5.7 shows the simulation of VCO tuning characteristics with corner model variation. The gain of VCO is about 400 MHz/V and the tuning range of the VCO is from 1.03 GHz to 1.37 GHz at TT corner. Figure 5.8 shows the eye diagram of VCO outputs at non-SSC mode and the

peak-to-peak jitter is 5.31 ps. Figure 5.9 shows the control voltage of VCO at SSC mode. We can see a frequency modulation by triangular waveform obviously. The voltage variation of VCO control voltage can be expressed as

$$\Delta V = \frac{\Delta f}{K_{VCO}} = \frac{6MHz}{400MHz/V} = 15mV\ . \qquad (5\text{-}1)$$

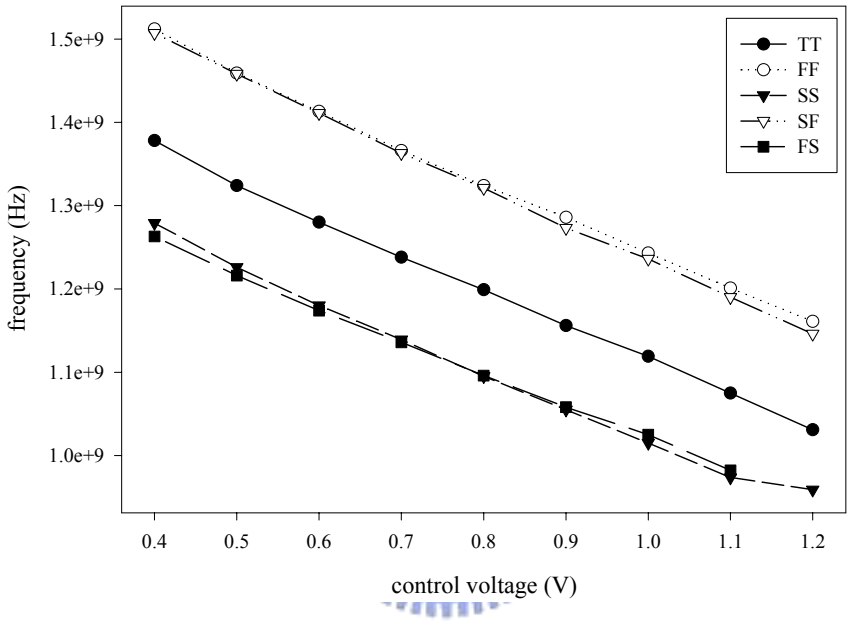


Figure 5.7: Tuning characteristic of VCO with corner model variation

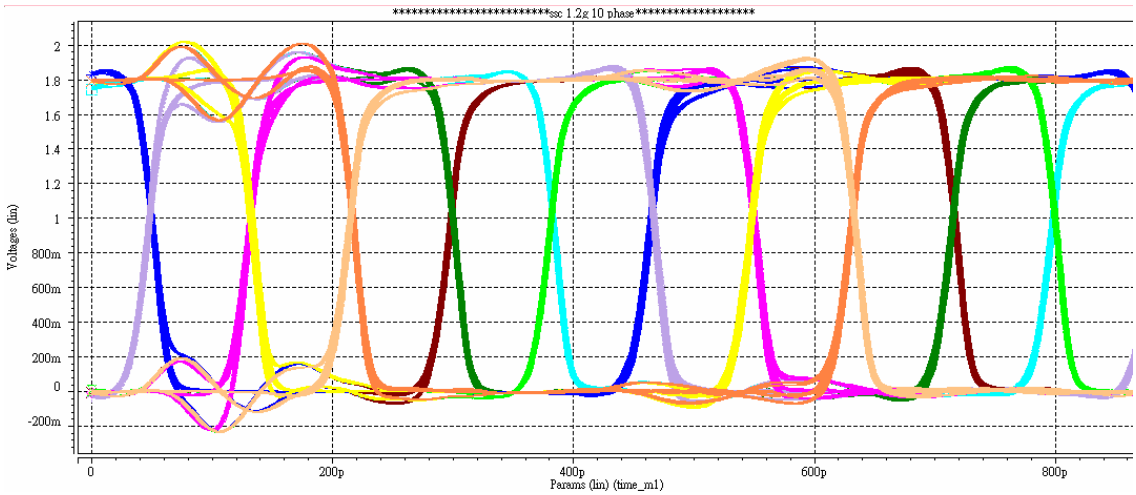


Figure 5.8: Eye diagram of VCO output at non-SSC mode

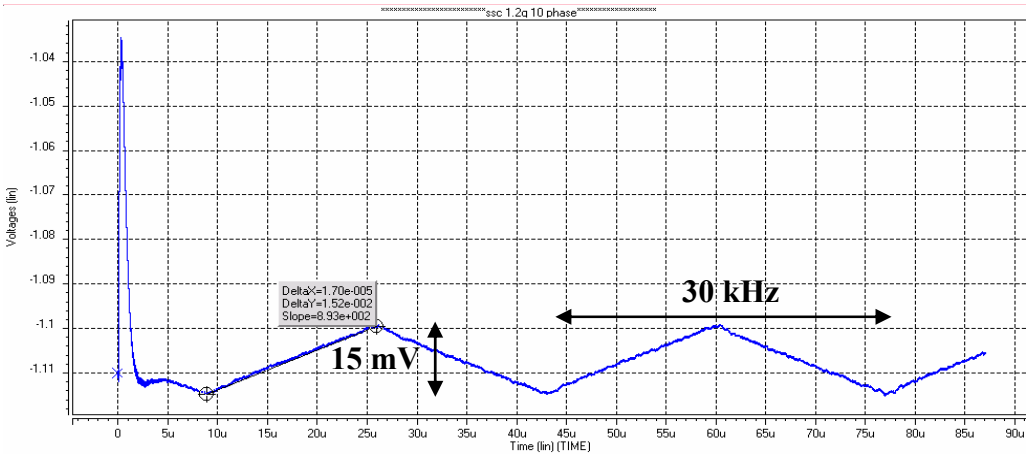


Figure 5.9: Control voltage of VCO at SSC mode

5.3 Testing Setup

Figure 5.10 shows the SSCG die photo. The chip area is 860um by 860um. The chip is implemented in TSMC 0.18 um CMOS 1P6M technology. Considering the speed and noise issues, the IC is un-packaged to reduce parasitic loading of the packages.

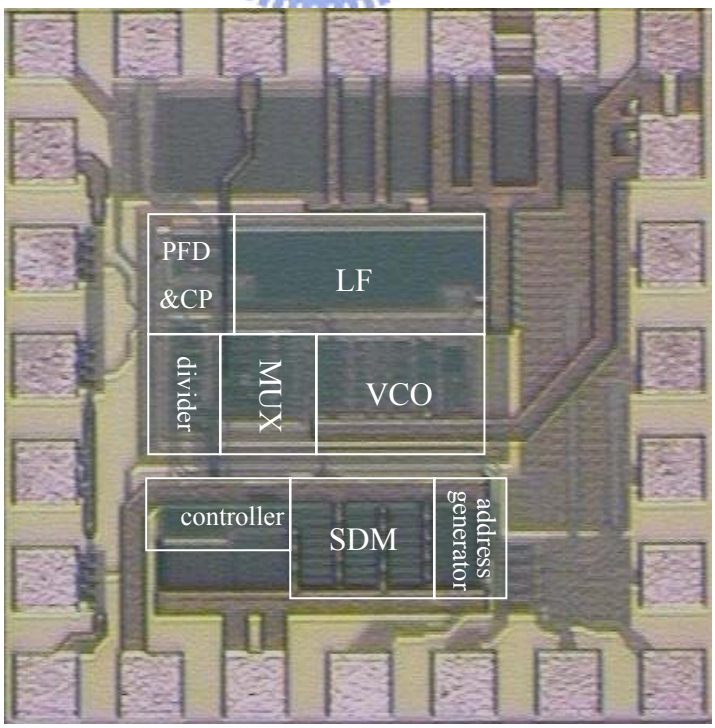


Figure 5.10: Micrograph of die

Figure 5.11 is the photograph of the testing board. External charge pump bias resistance is used to adjust the charge pump current thus the open loop gain to be more flexible. A switch is used to select the SSC mode or the non-SSC mode of the SSCG. It controls the D flip-flops of barrel shifter in the SSCG. The impedance matching is done on the PCB and one of the differential outputs is terminated by a 50 ohm terminal for the single-end signal measurement.

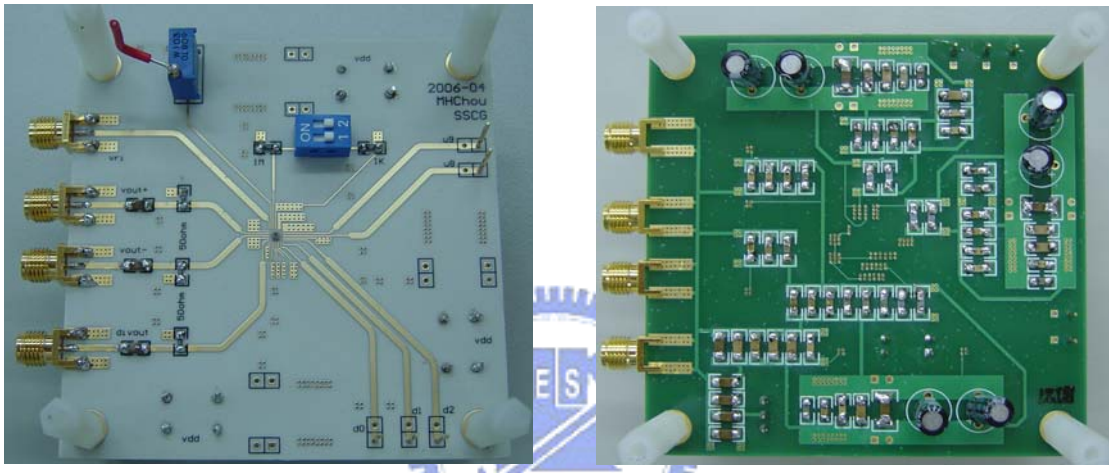


Figure 5.11: Photograph of testing board

Figure 5.12 shows the instruments that we use to measure the SSCG chip. Pulse data generator is used to send a 100 MHz reference clock to the SSCG. Wide-Bandwidth Oscillator is used to show the VCO output waveform of SSCG at non-SSC mode. Spectrum Analyzer is used to show the spectrum of SSCG output at SSC and non-SSC mode.

Figure 5.12: Instruments for testing the SSCG chip

5.4 Measurement Results

Figure 5.13 shows the eye diagram of VCO output at non-SSC mode. The peak-to-peak jitter is 48 ps and the RMS jitter is 7.226 ps.

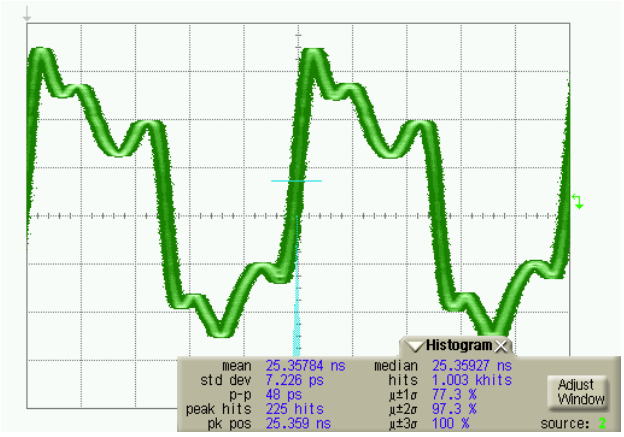


Figure 5.13: Measured jitter of SSCG output at non-SSC mode

Figure 5.14 shows the comparison of VCO outputs at SSC mode and non-SSC mode. Line A is the spectrum of VCO output at non-SSC mode; the center frequency is 1.2 GHz. Line B is the spectrum of VCO output at SSC mode. Each scale is 6 MHz, and we can see the frequency down spread 6 MHz. The peak amplitude reduction is 21.633 dB.

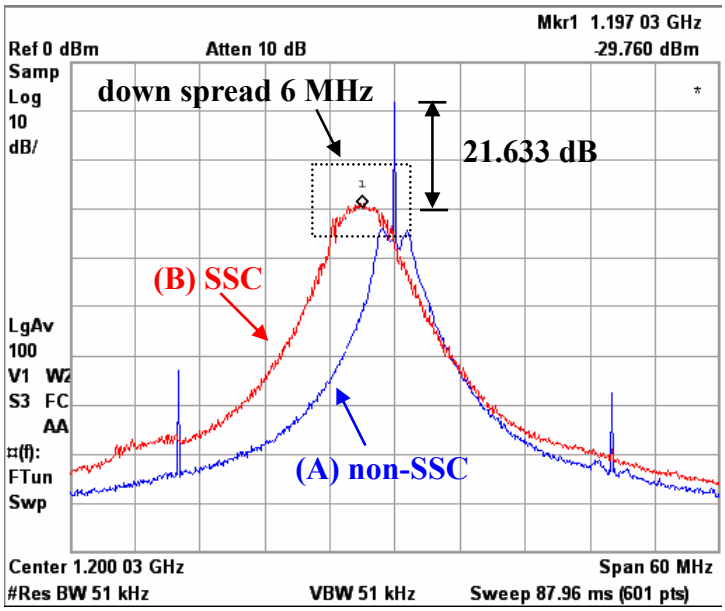
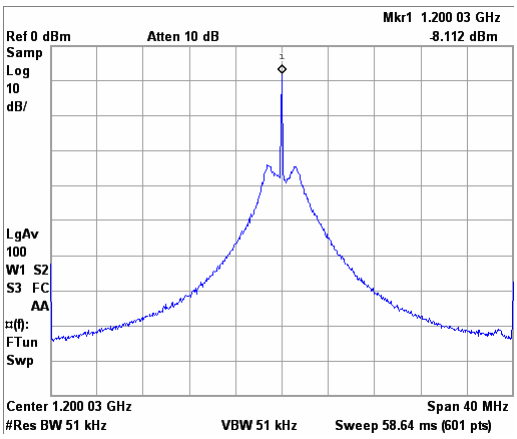
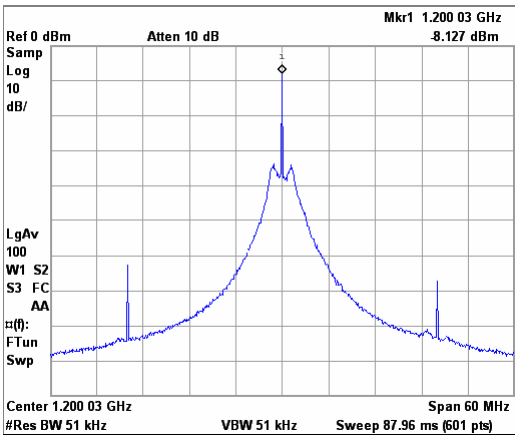


Figure 5.14: Spectrum of SSCG output

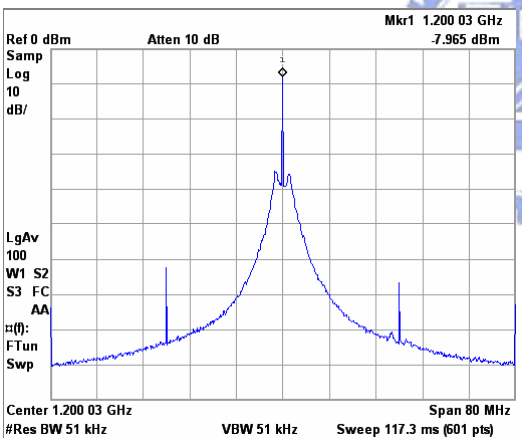
Figure 5.15 shows the measured spectrum of VCO output at non-SSC mode under the different scale of span.



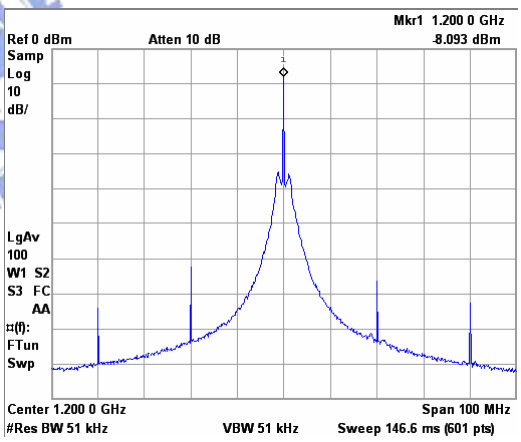
span 40 MHz



span 60 MHz



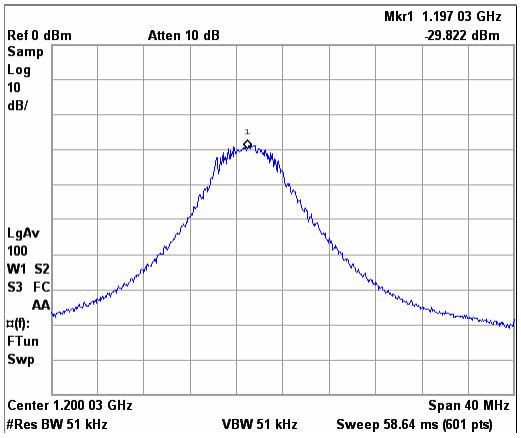
span 80 MHz



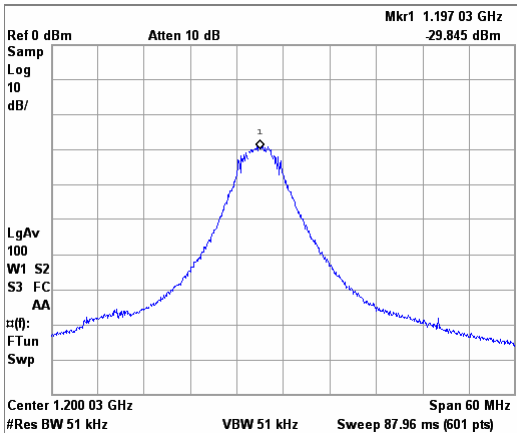
span 100 MHz

Figure 5.15: Spectrum of VCO output at non-SSC mode

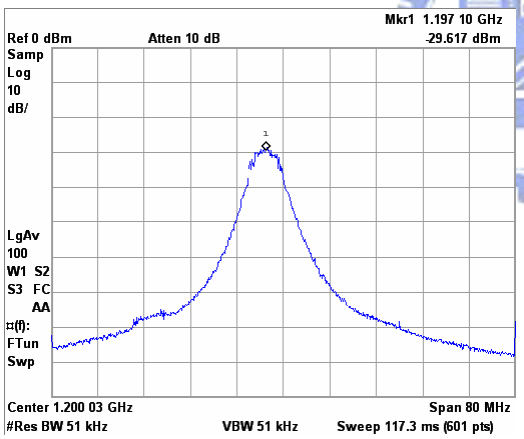
Figure 5.16 shows the measured spectrum of VCO output at SSC mode under the different scale of span. The peak energy is reduced and the spectrum is spreading.



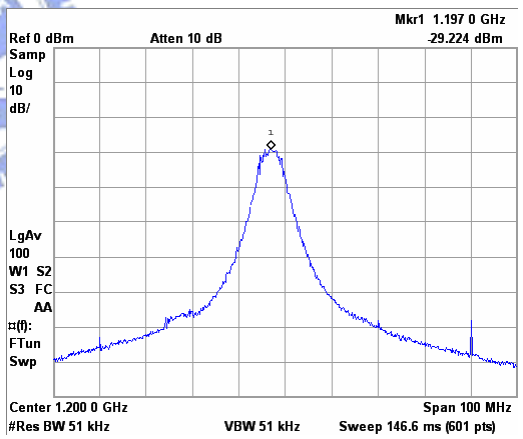
span 40 MHz



span 60 MHz



span 80 MHz



span 100 MHz

Figure 5.16: Spectrum of VCO output at SSC mode

5.2 Summary and Comparisons

Table 5.1 shows the performance summary of the SSCG chip. Table 5.2 shows the comparisons among different SSCGs. The accomplished SSCG has smaller area than [22], [30]. The EMI reduction is better than [24].

Table 5.1: Performance summary of the SSCG chip

SSCG center frequency	1.2 GHz
Technology	TSMC 0.18um CMOS
Modulation Method	Modulation on VCO phases
Modulation Profile	30 kHz Triangular
Frequency Deviation	5000 ppm
Loop Bandwidth	400 kHz
Supply Voltage	1.8V
Power Consumption	57mW
p-to-p jitter (non-SSC)	48ps
RMS jitter (non-SSC)	7.226ps
Peak Energy Reduction	21.633 dB
SSCG chip area	860um×860um

Table 5.2: Performance comparison of SSCGs

Type	this work	ISSCC 05 [22]	ISSCC 05 [24]	ISCAS 05 [30]
Technology	0.18um CMOS	0.15um CMOS	0.18um CMOS	0.18um CMOS
Supply Voltage	1.8V	1.5V	1.8V	1.8V
Power	57mW	54mW	-	55mW
Core Area	500×500um	880×480um	-	650×600um
p-to-p jitter	48ps	-	41.008ps	80ps
RMS jitter	7.226ps	8.1ps	3.067ps	-
EMI Reduction	21.633 dB	20.3dB	9.807dB	23.44dB

Chapter 6

Built-in-Self-Test Circuit for SSCG

CMOS technology has been growing very fast in recent years. Design of *integrated circuits* (ICs) becomes so complex and gate counts become so large. Undoubtedly, faster and more complex test equipments are required to achieve test specifications and test functions. An innovative method to simplify the test equipment is to move test functions onto the chip itself, which is called *Built-In-Self-Test* (BIST). The proposed BIST circuit for SSCG will be discussed in this chapter.

6.1 Introduction

The SSCG spreads the spectrum of conventional PLL and reduces the EMI effectively. The Serial-ATA specified the SSCG with 5000ppm frequency spreading and 30~33 kHz triangular modulation rate. In general, we can use frequency analyzer to measure the spectrum of SSCG as shown in section 5.4. It can measure the frequency range of SSCG output but can't measure the waveform of triangular modulation. The linearity of triangular modulation of SSCG can't be measured easily

as shown in Figure 6.1. If we measure the control voltage of VCO by external equipment it may cause extra noise to the PLL loop and increase jitter. The BIST circuit can detect the frequency variation of SSCG and show the waveform of triangular modulation of SSCG. The BIST methodology for the SSCG that we proposed is an all digital design to minimize the hardware overhead. Details for BIST circuit architecture will be discussed later.

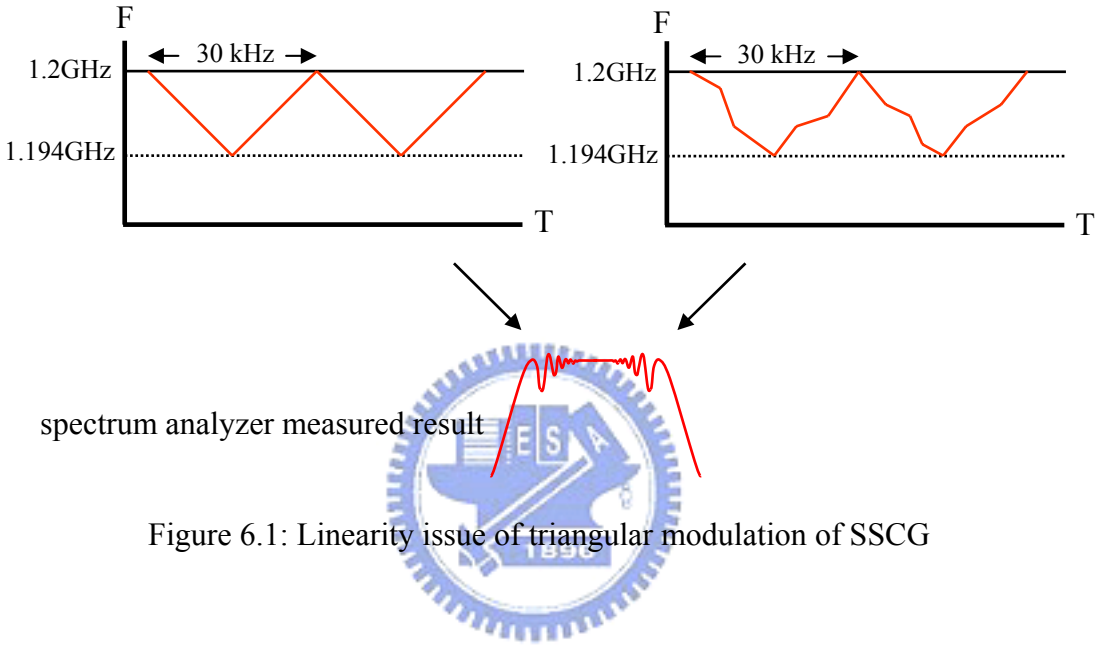


Figure 6.1: Linearity issue of triangular modulation of SSCG

6.2 Architecture of BIST Circuit for SSCG

The proposed BIST architecture of the SSCG is shown in Figure 6.2. The *multi-phase phase detector* (MPD) is used to detect the phase with a resolution of 0.1UI (*unit interval*). The *phase shift detector* (PSD) is a phase shift detection circuit. It detects the phase shift of the SSCG. The amount of the phase shift is accumulated in accumulator. Each block and its function are detailed as follows.

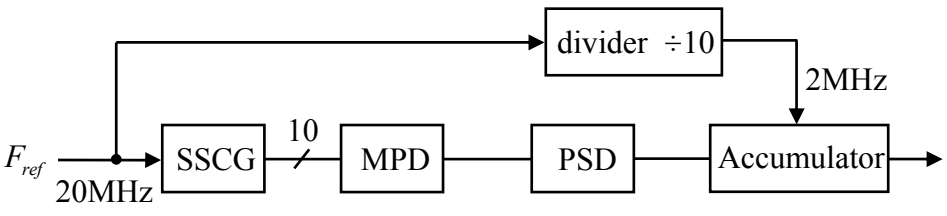


Figure 6.2: Architecture of BIST circuit

■ MPD

The MPD is used to increase the resolution of the phase detection. The circuit diagram is shown in Figure 6.3. It is composed of 10 D flip-flops. The reference clock is used to trigger and sample the 10 output phases of the SSCG. Figure 6.4 shows the waveform of MPD when it detects the phase of the SSCG output. In Figure 6.4 the MPD detects the phase 9 in phase at first rising edge of sampling frequency, and phase 7 in phase at second rising edge. In this case, the phase shifted of the SSCG is 0.2UI. Notice that the resolution and the uncertainty of MPD is 0.1UI.

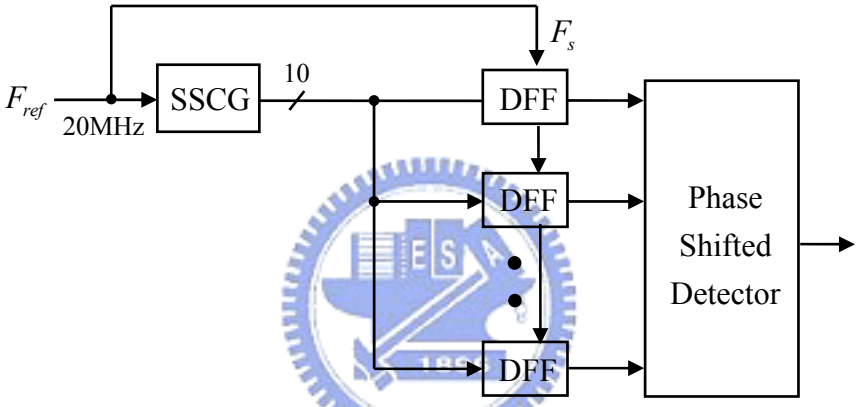


Figure 6.3: The architecture of MPD

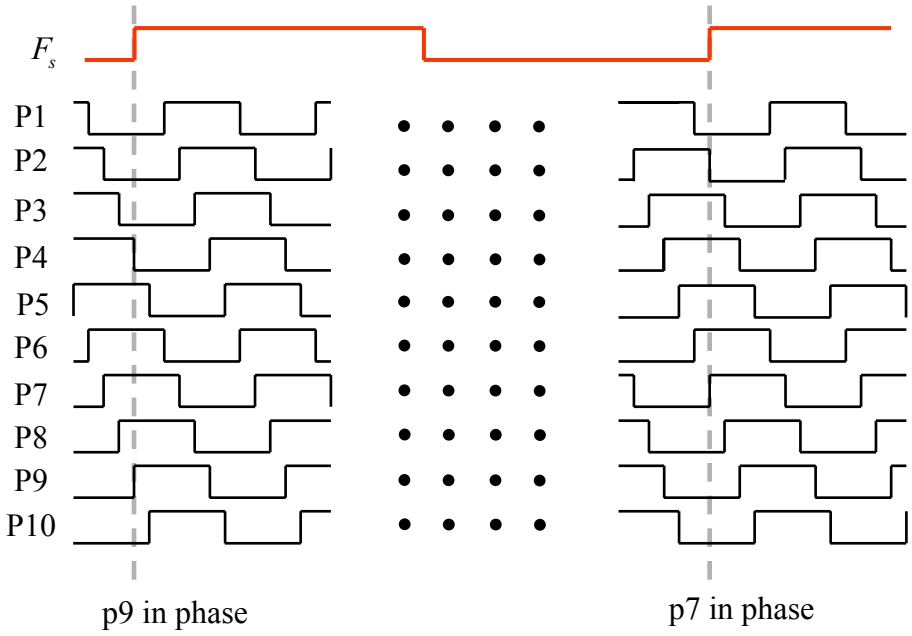


Figure 6.4: Waveform of MPD

■ PSD

The circuit strecture of the PSD is shown in Figure 6.5. It is encoded MPD outputs into binary first. The phase shift is calculated by taking the phase difference between two samples of MPD. Here, we need overflow correction circuit to correct the over-flow. The relation of phase shift $\Delta\phi$ and frequency spreading Δf of SSCG can be expressed as

$$\Delta\phi_i = \Delta f_i \times T_s \tag{6-1}$$

where T_s is the period of the sampling frequency of MPD.

For the SSCG in our design, the maximum Δf is 6 MHz. When the reference clock of MPD is 20 MHz (50ns), the maximum $\Delta\phi$ is 0.3UI.

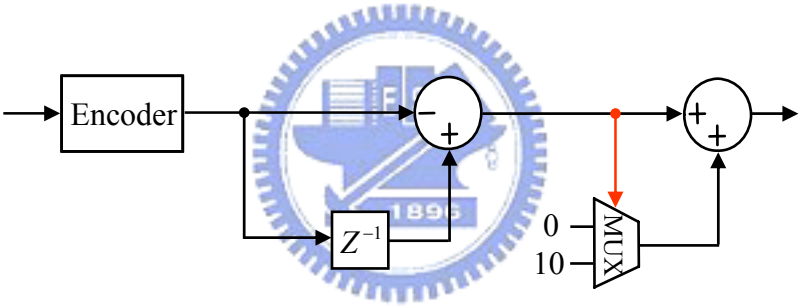


Figure 6.5: The architecture of PSD

■ Accumulator

If the frequency detection of MPD is made every T_1 , the number of samples being taken in a up (or down) spreading process for a modulation of 30 kHz is

$$Samples = \frac{16.6\mu s}{T_1} \tag{6-2}$$

For 6 MHz frequency spreading and MPD resolution of 0.1UI, the frequency detection resolution is

$$Resolution = \frac{6MHz \times T_1}{0.1UI} \tag{6-3}$$

For different T_1 , presented as sampling frequency , the number of samples and the resolution is shown in Figure 6.6. As one can see, the number of samples and the resolution are equal when the sampling frequency close to 2 MHz (T_1= 500ns). For T_1= 500ns, the number of samples taken in 16.6μs is 33 and the phase resolution is 30. If the sampling rate is higher (or lower), for example 4 MHz (1 MHz) or 25ns (100ns), we can take a total of 66 (16) samples. However, the phase shift at 6 MHz is 1.5 (6.0) UI with a resolution of 15 (60). Hence, T_1= 500ns is the optimal compromise that maximize the measurement resolution.

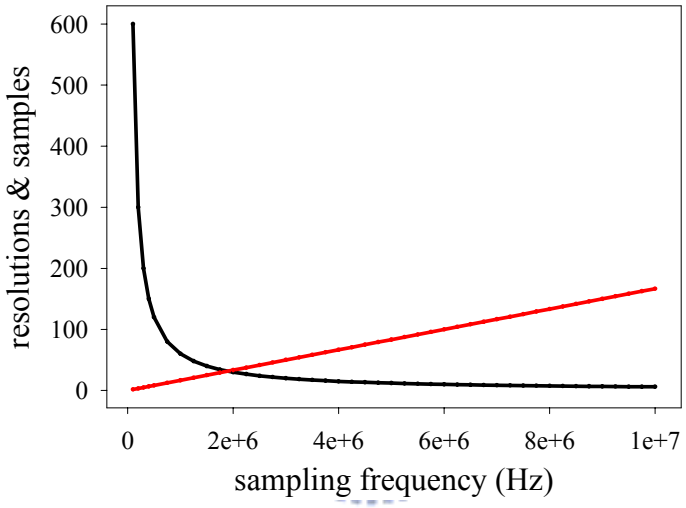


Figure 6.6: The resolution & samples vs. sampling frequency

For the MPD and PSD, they detect the phase shifted of SSCG. The serious problem of MPD and PSD is that when the phase shifted of SSCG is larger than 1UI the BIST results of them are incorrectly. Hence, we use higher sampling rate for MPD and PSD and an accumulator to accumulate the results of PSD to solve this problem. We use 20 MHz for the sampling rate of MPD and PSD, and the BIST circuit can detect the frequency variation of SSCG from 1206 MHz to 1188 MHz. It is wide enough to detect the frequency variation of the SSCG.

Figure 6.7 shows the circuit strecture of the accumulator. The accumulator accumulates the phase shifted results of PSD, and use 2 MHz to sample the results of accumulator which is the optimal sampling frequency.

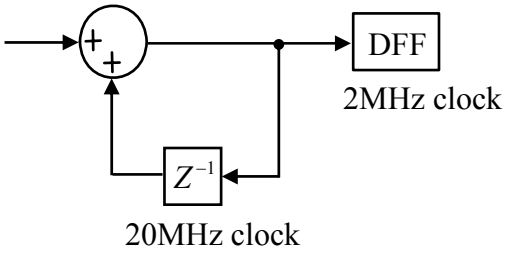


Figure 6.7: The architecture of accumulator

According to Eq. 6-1, for the accumulator results with 2 MHz sampling rate, the accumulator ourput is in between 0UI and 3UI. Therefore, if accumulator output is less than 0UI or greater than 3UI, one knows that the clock frequency is out of range. Due to the resolution and the uncertainty of MPD is 0.1UI, a tolerance of 0.1UI needs to be inserted as the guard band.

6.3 BIST Circuit Behavior Simulation

The behavior simulation of BIST circuit is simulated using SIMULINK. Figure 6.8 shows the model of the BIST system which includes MPD, PSD and accumulator.

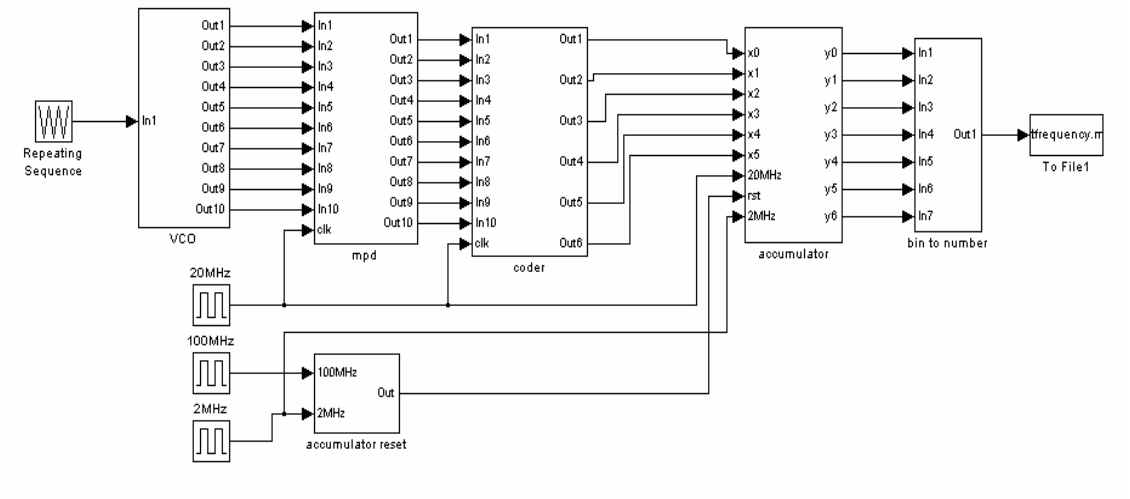


Figure 6.8: SIMULINK model of the BIST system

Figure 6.9 shows the comparison between the accumulator output and the VCO frequency. We can see the BIST circuit is able to track the clock frequency of the SSCG. Figure 6.10 shows the simulation results for the accumulator output for T_1 of 2000ns and 500ns or a rate of 500 kHz and 2 MHz. As analyzed in the previous section, the theoretical resolution is 120 and 30 respectively. Due to the limit of samples, the simulation results show that the resolutions are 8 and 30.

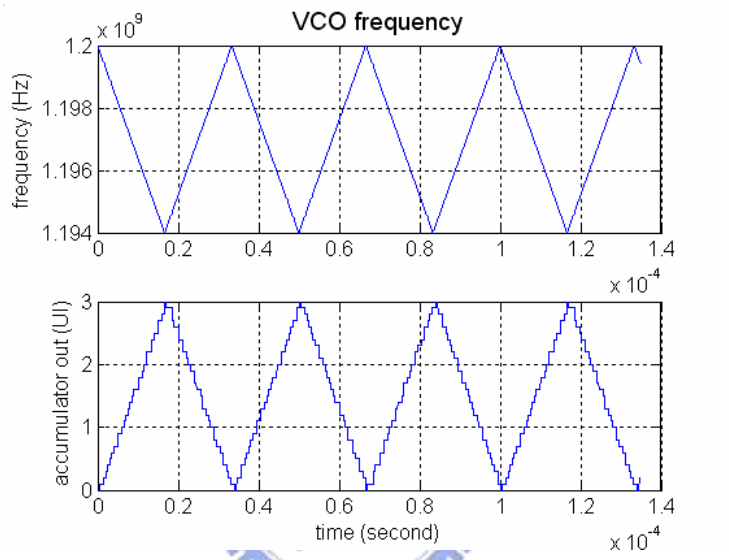
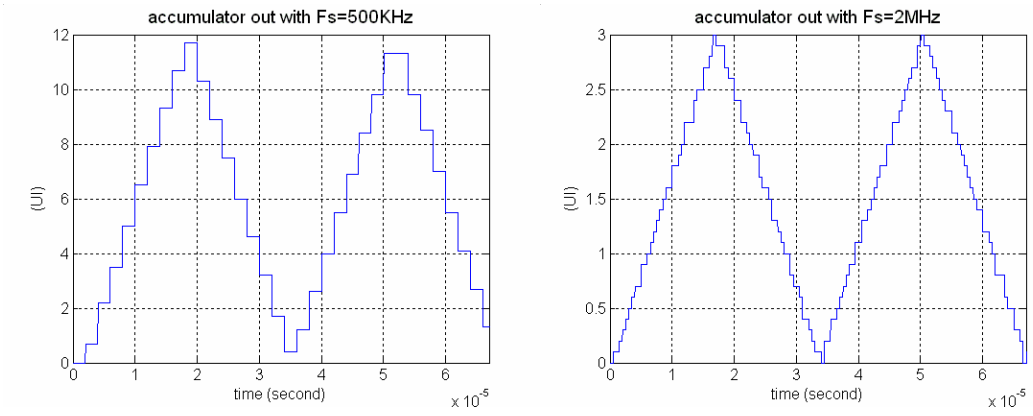


Figure 6.9: The VCO frequency vs. accumulator output



(a) (b)

Figure 6.10: The accumulator output for T_1 of (a) 2000ns (b) 500ns

6.4 Circuit Level Simulation and Layout

The circuit level simulation of BIST circuit also using HSPICE. The accumulator outputs are digital signal and we transfer the binary code into the decimal. Thus, the simulation results can be observed easily. Figure 6.11 shows the comparison of the accumulator output (in decimal) and the VCO control voltage. The BIST circuit is able to track the clock frequency of the SSCG. The accumulator outputs are between 0 and 30, presented as 0UI and 3UI.

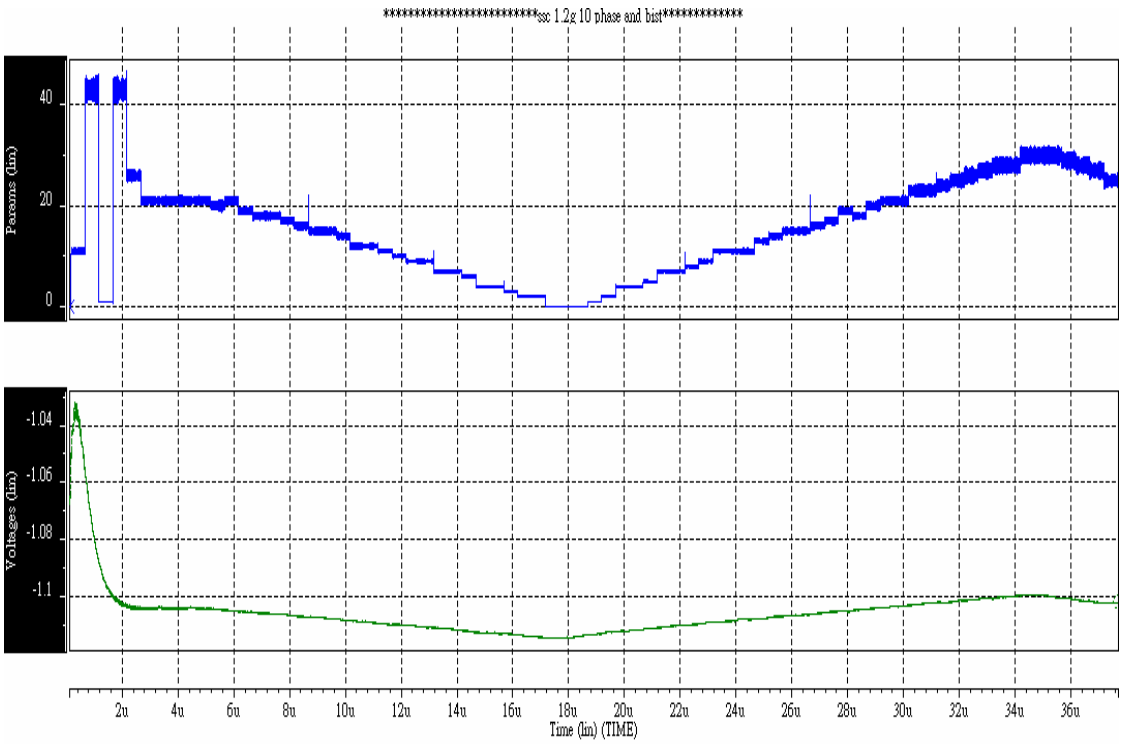


Figure 6.11: The VCO control voltage vs. accumulator output

Figure 6.12 shows the chip layout of the SSCG and the BIST circuit. The chip area is 990um by 990um. The chip is implemented in TSMC 0.18 um CMOS 1P6M technology. Different to the SSCG, we can use logic analyzer to measure the BIST results. The digital signal of the BIST results can be measured easily.

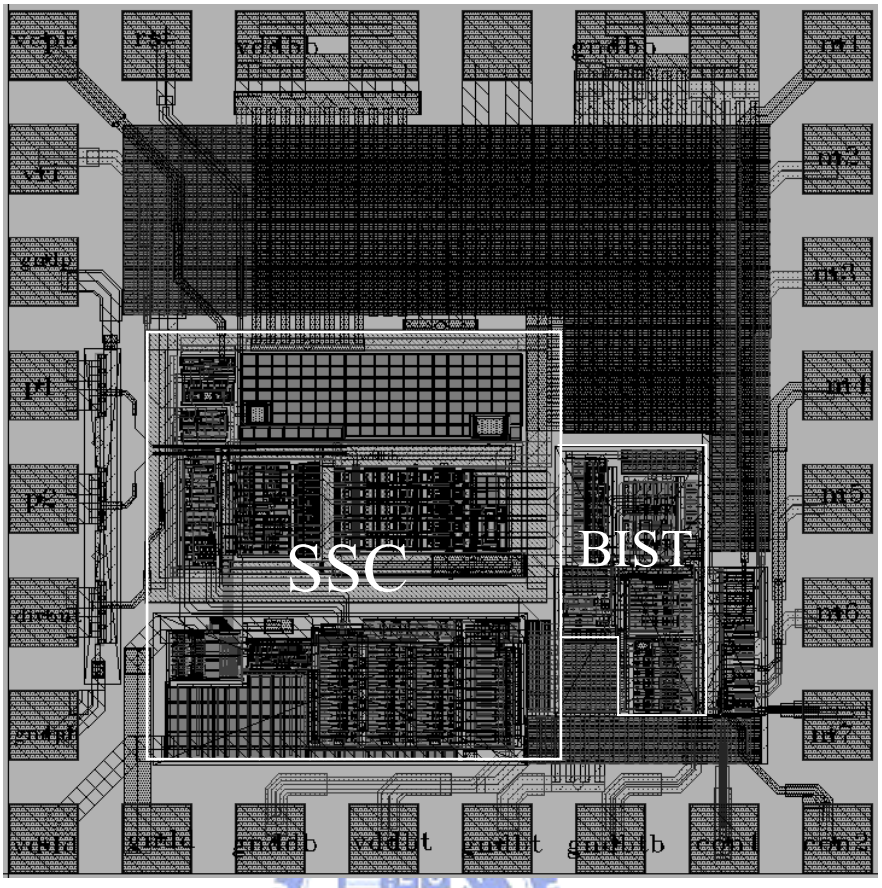


Figure 6.12: Layout of SSCG and BIST circuit

Table 6.1 shows the performance summary of the SSCG and the BIST circuit chip. The power consumption of the BIST circuit is 1.53mW and the core area of the BIST circuit is 150um by 250um.

Table 6.1: Performance summary of the SSCG and BIST chip

SSCG center frequency	1.2 GHz
Technology	TSMC 0.18um CMOS
Supply Voltage	1.8V
Power Consumption	SSCG 57mW
	BIST 1.53mW
Core area	SSCG 500um×500um
	BIST 150um×250um
SSCG + BIST chip area	990um×990um

Chapter 7

Conclusions

In this thesis, we have designed a spread spectrum clock generator and its Built-in-Self-Test circuit for the Serial-ATA system. The SSCG uses a fractional-N frequency synthesizer to achieve spread spectrum function with triangular waveform modulation. The SSCG consists of a conventional PLL, an address generator, a sigma-delta modulator, a controller and a multiplexer. Fractional-N PLL can achieve high resolution with high operation frequency. But, one major disadvantage is the generation of high tones at multiples of the channel spacing. The use of digital sigma-delta modulation technique in the fractional-N PLL can eliminate spurs. Using phase modulation to spread the spectrum can reduce the phase jump of the SSCG.

The SSCG circuit has been implemented in TSMC 0.18 um 1P6M CMOS technology. The measurement results show that the non spreading clock has a peak-to-peak jitter of 48 ps, a RMS jitter of 7.226ps, and a peak amplitude reduction of 21.633 dB in the spread spectrum mode.

In order to measure the frequency variation of SSCG, we have proposed a BIST circuit for the SSCG in this thesis. The BIST circuit consists of a multi-phase phase detector, a phase shifted detector and an accumulator. The BIST circuit can detect the frequency variation of the SSCG and show the waveform of triangular modulation of the SSCG. The BIST methodology for the SSCG that we proposed is an all digital design to minimize the hardware and power overhead.

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