國 立 交 通 大 學

電信工程學系

博 士 論 文

高效能 CMOS 展頻訊號產生器之設計與分析

Design and Analysis of High Performance CMOS Spread-Spectrum Clock Generators

研 究 生：謝義濱

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中 華 民 國　九十七　年 五 月

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國立交通大學

電信工程學系

博士論文

A Dissertation

Submitted to Institute of Communication Engineering
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy
in
Communication Engineering
Hsinchu, Taiwan

2008 年 5 月


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推　薦　函

中華民國九十七年四月十七日

一、 事由：本校電信研究所博士班研究生 謝義濱 提出論文以參加國立交通大學博士班論文口試。

二、 說明：本校電信研究所博士班研究生 謝義濱 已完成本校電信研究所規定之學科課程及論文研究之訓練。

有關學科部分，謝君已修滿十八學分之規定（請查閱學籍資料）並通過資格考試。

有關論文部分，謝君已完成其論文初稿，相關之論文亦分別發表或即將發表於國際期刊（請查閱附件）並滿足論文計點之要求。

總而言之，謝君已具備國立交通大學電信研究所應有之教育及訓練水準，因此特推薦

謝君參加國立交通大學電信工程學系博士班論文口試。

交通大學電信工程學系教授　高　曜　煌


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摘　要

在消費電子中隨著高速傳輸需求的日益增加，工作頻率已達到數仟兆赫。因為工作頻率增加時，這些裝置所產生及輻射的電磁干擾也快速遞增。所以一個低成本且有效降低電磁干擾的方法是目前所需要的。目前有很多方法可以來減少電磁干擾，在這些方法中，展頻訊號時脈正受到許多矚目因為其系統成本是最低的，其原理為在一定的速度及方法下調變時脈使其有效抑制電磁干擾。

本論文介紹四個不同展頻訊號產生器將，其中用了三種不同的調變方法。首先研究一個傳統的分數差異積分調變展頻訊號產生器，其原理為使用差異積分調變器來調變除法器。傳統的差異積分調變器的輸入範圍有限制，當展頻大小超過其輸入範範圍時，展頻訊號產生器會無法正常工作導致大幅降低電磁干擾抑制能力及時間抖動成效。因此本論文的第一個主題為克服這個限制並發展出一個新型分數差異積分調變展頻訊號產生器且具有廣輸入範圍的差異積分調變器。

接著研究一個使用電壓控制振盪器調變的展頻訊號產生器。傳統的電壓控制振盪器調變的展頻訊號產生器的其中一個問題為在產生三角波時有太多的限制，三角波為普遍使用的調變型式。另外一個困難為所需要的電容面積太大(大於數十個十億分之一法拉)使其很難整合在晶片中，其原因為其所需要的迴路頻寬太小了。本論文中所提出的電壓控制振盪器調變的展頻訊號產生器使用了一個雙迴路濾波器並同時使用了一個特定的充電泵來克服這兩個問題。

最後，本論文發展出兩個使用雙點調變機制的新型的展頻訊號產生器，其同時改變除法器及電壓控制振盪器。其中一個針對雙點調變機制中的時間抖動及電磁干擾做詳細的分析。為了研究雙點調變機制在高速傳輸的應用，進而發展出另一個適用於序列進階技術附加裝置的展頻訊號產生器並證明其可符會其規格。雙點調變中的全導通特性可以增加調變頻寬使得調變的準確度及由差異積分器所產生的時間抖動可以一起改善。此技術導致所提出的展頻訊號產生器具有面積小及功耗低的特點。

ABSTRACT

With the growing demands of high data rate transmission in consumer electronics, the operation frequency is toward several GHz. As the operation frequency increases, the electromagnetic interference (EMI) generated and radiated by those devices also increases rapidly. Therefore, an effective and low cost method to reduce EMI is becoming imperative. There are many techniques to reduce the EMI. Among these techniques, spread spectrum clocking (SSC), modulating the clock in a given rate and style such that the EMI is lower, is receiving many eyes because the cost to the system is minimal.

In this thesis, four different SSCGs with three kinds of modulation schemes are presented. First, a conventional fractional-N based SSCG, using a ΔΣ modulator to modulate the divider, is studied. The input range of the conventional ΔΣ modulator is limited. When the spread ratio is exceeded its input range, the SSCG will be breakdown, and the EMI reduction and jitter performance will be degraded very much. Thus the subject of this dissertation is to overcome the limitation and to develop a new fractional-N based SSCG with a wide input range of ΔΣ modulator.

Then, a voltage controlled oscillator (VCO) modulated SSCG is investigated. One major issue of the conventional VCO modulated SSCG is that it has much constraints on the generation of the triangular waveform, which is a popular modulation profile. Another difficulty is the required large capacitance (more than tens of nF) to make it hard totally integration because the loop bandwidth is very small. The proposed VCO modulated SSCG overwhelms these two issues by combing a dual-path loop filter with a particular charge pump.

Last of all, two new SSCGs with a two-point modulation scheme are built. Both the divider ratio and the voltage controlled oscillator are varied. One is focused on the jitter and EMI analysis of the two-point modulation scheme. In order to evaluate the high data rate application of two-point modulation, the other is developed for the application of serial advanced technology attachment (SATA) and is proven to meet the specifications of SATA. An all-pass characteristic of the two point modulation can enhance modulation bandwidth in order that the modulation profile accuracy and jitter performance caused by the ΔΣ modulator can be improved at the same time. This technique results in the proposed SSCG with small area and low power consumption.

Acknowledgments

First of all I would like to express my immense gratitude to my advisor, Prof. Dr. Yao-Huang Kao for the confidence in me and his enthusiasm during my research at National Chiao-Tung University. He planted the initial seed for this thesis and gave me enough freedom to pursue my own ideas. His energy and concept guide me to a successful result. I learn a lot from his supervision that includes both the technical and the personality. He truly opens a door to my future.

Then, I would like to give many thanks to my colleagues in the HF circuits and Optical Fiber Communication Lab for their friendship and all of their help over these years. Their friendly treatment helps me a lot.

Finally, special thanks to my wife and daughter for their endless love and inspiration. Without their kindly understanding and encouragement, this dissertation could not be finished so smoothly.

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CHAPTER 1

Introduction

With the progress of CMOS technology, the operated frequency of electrical devices has been increased to meet the demand of high performance. When the operation frequency of electrical equipments is increasing rapidly, it radiates or generates more electromagnetic interference (EMI). Excessive EMI has disastrous damage to communication system; therefore, EMI levels have been strictly defined for different devices and systems. There are kinds of EMI standards defined by Federal Communication Commission (FCC) in USA or CISPR which is a committee of the International Electrotechnical Commission (IEC). For example, in the PC-based equipments, the frequency of microprocessor is up to several GHz and its EMI emission may exceed the related standard. The same case happens in portable devices with high speed data throughput like serial advanced technology attachment (SATA). Therefore, an effective and low cost method to reduce EMI is necessary. Several techniques have been used to diminish EMI, such as shielding [1], slew-rate limitation [1], filtering [1], and spread-spectrum clocking (SSC) [2]. Among these techniques, SSC, a technique of reducing the clock power of fundamental frequency as well as its harmonics, has been proven to being the most suitable and cost effective way to alleviate EMI [2] for clock-based systems. It also offers a good way to be integrated in VLSI chips. The function of SSC is shown in Fig. 1.1(a) and (b). When a clock generator turns on the mechanism of spread-spectrum clocking, the output of the clock generator is not a constant frequency; instead, it is a variable frequency with a fixed and slow modulation profile as shown in Fig. 1.1(a). From the view point of communication, it acts like a frequency modulator with a dedicated modulation profile. The modulation profile illustrated here is a triangular wave with two important parameters: spread ratio and modulation frequency. Usually, a peak-to-peak spread ratio within 0.25% to 5% and a modulation frequency within 30 kHz to 50 kHz are usually used. The spectra of the output when SSC is off and on are shown in Fig. 1.1(b). The spectrum has a peak reduction with a specified spread amount when SSC is on; therefore, the spread-spectrum clocking can effectively reduce the EMI levels.

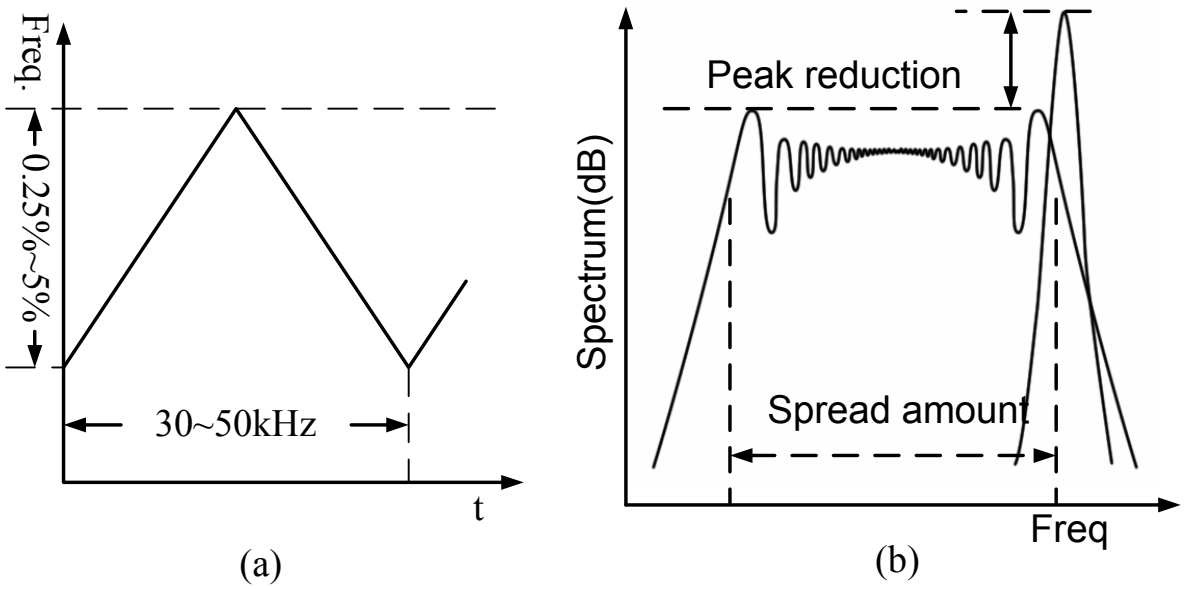


Fig. 1.1. Illustration of spread-spectrum clocking: (a) frequency output with time (b) spectra output when SSC off and on.

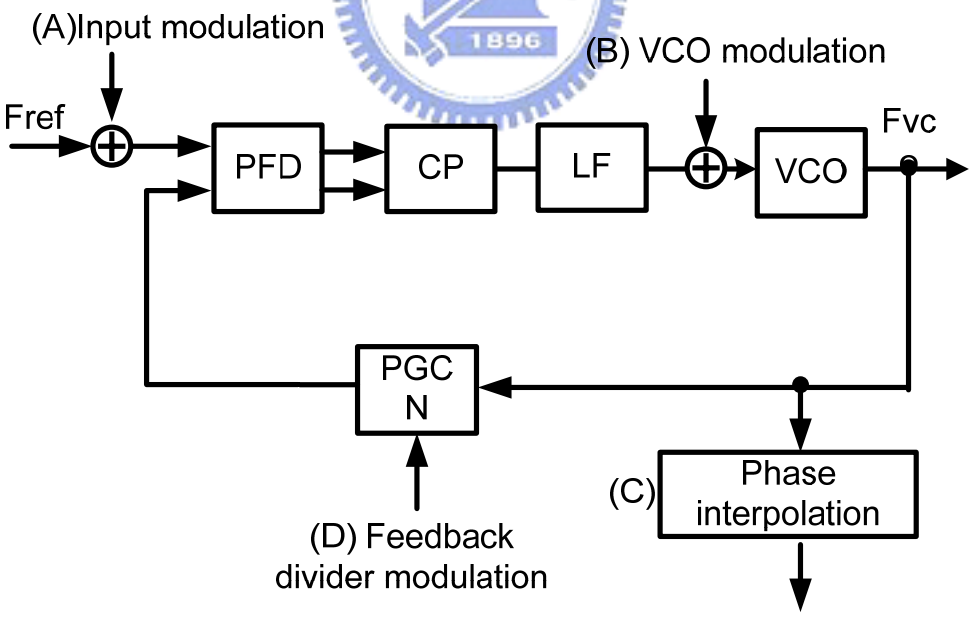


Fig. 1.2. SSC techniques employed in PLL.

1.1 Review of SSCG

Spread-spectrum clock generator (SSCG) is the clock generator utilizing the technique of SSC. Phase locked-loop (PLL) is a popular candidate for a clock generator in VLSI technology. Therefore, PLL becomes an important employee for SSCG. The block diagram of PLL with various modulations is shown in Fig. 1.2. The key components of the PLL are a phase frequency defector (PFD), a charge-pump (CP) current, a loop filter (LF), a voltage-controlled oscillator (VCO) and a programmable counter (PGC). There are three major SSC techniques employed in PLL. First, modulating the divider using a ΔΣ modulator [8] in a PLL like (A) or (D) in Fig. 1.2. It is called the Fractional-N based SSCG. The second type is to modulate the VCO directly like (B) in Fig. 1.2. Last, one may combine the multiphase outputs with special phase interpolation algorithms to achieve SSC function like (C) in Fig. 1.2. Here, three major techniques are reviewed.

1.1.1 Fractional-N based SSCG

The block diagram of a fractional-N based SSCG [8] is shown in Fig. 1.3. It is basically a fractional-N PLL using a ΔΣ modulator to modulate the divider. An up-down counter is used to generate a triangular modulation profile. The k-bits outputs of the counter are fed into the first-order ΔΣ modulator to control the dual modulus divider N-1/N+1. As a result, the output of the PLL can also track the triangular modulation profile and establish the function of spread-spectrum clocking. The first-order delta modulator is simply a (k+1) bits accumulator. The modulation frequency is determined by bit number and operation frequency of the up-down counter while the spread ratio is determined by bit number of the up-down counter and bit number of the accumulator. In this thesis, k=4 means that the bit number of the up-down counter is 4 and the bit number of the accumulator is 5. N=402. Therefore, the spread ratio is ±1/402=±0.124%. Besides, the reference frequency F_{ref}=27 MHz and M=81. The modulation frequency can be evaluated by 27 MHz/81/32=10.417 kHz. The advantage of this technique is that the spread ratio and modulation frequency can be easily adjusted by change the parameters of the up-down counter, composed of some simple digital circuits.

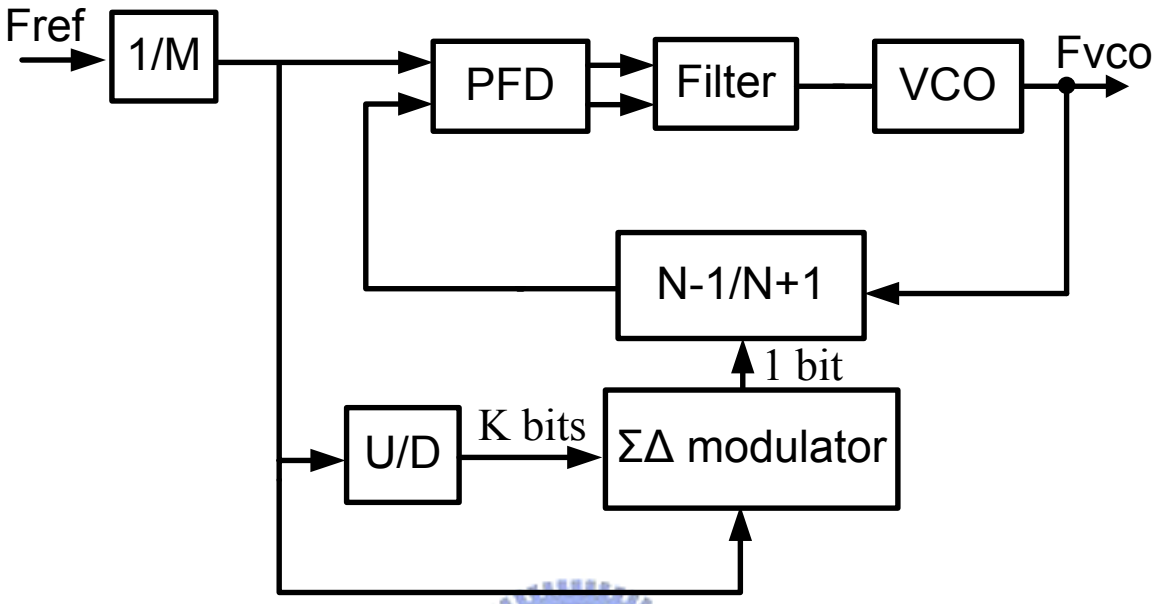


Fig. 1.3. Block diagram of Fractional-N based SSCG.

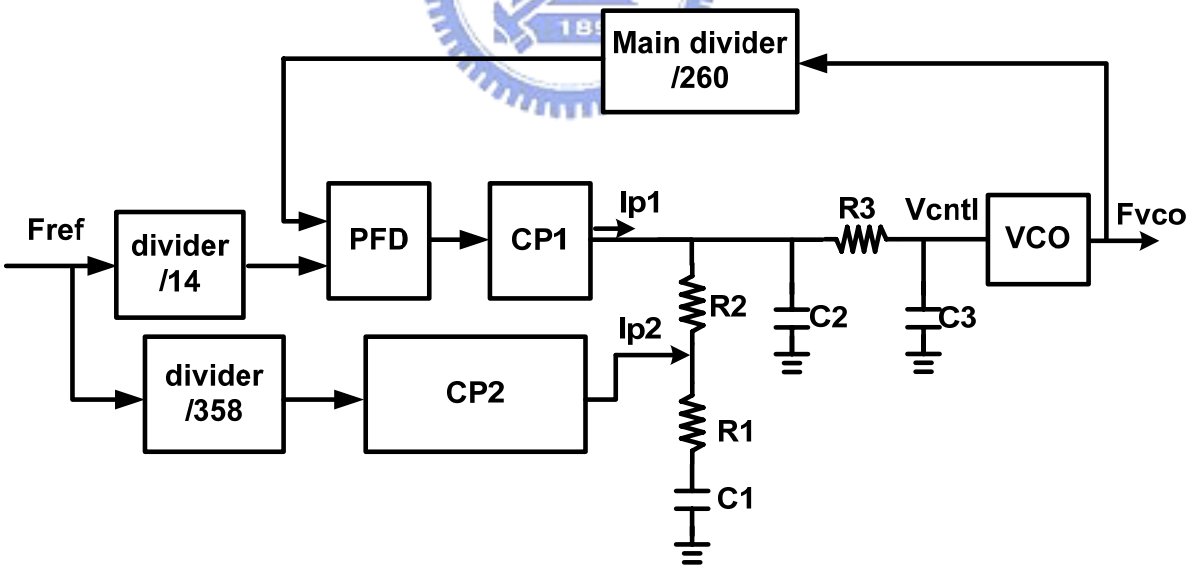


Fig. 1.4. Block diagram of SSCG using direct VCO modulation.

Therefore, it can be integrated in the VLSI chips with few costs. However, the quantization noise of the sigma-delta modulator will degrade the jitter performance and EMI performance and needs carefully design.

1.1.2 SSCG Using Direct VCO Modulation

The block diagram of the SSCG using direct VCO modulation [3] is shown in Fig. 1.4. It utilizes an extra charge-pump I_{p2} combined the special loop filter components R_1, R_2, C_1 and C_2 to generate the triangular waveform as the modulation profile. When $R_1C_1=R_2C_2$, the relationship between VCO controlled voltage V_{cntl} and I_{p2} can be found as

$$\frac{V_{cntl}}{I_{p2}} = \frac{1}{sC_1C_2}. \tag{1.1}$$

Therefore, the triangular waveform can be formed when I_{p2} is a rectangular waveform. In order to pass the modulation profile, the loop bandwidth of the PLL needs to be much smaller than the frequency of the triangular waveform. The advantage of this technique is that the architecture is very simple; however, the capacitors in the loop filter is so large (C_1=0.33 uF and C_2=0.22 uF) that makes it is hard to be integrated in the chips. Moreover, the spread ratio is related to the process parameters and the accuracy is also a concern.

1.1.3 SSCG Using a Multiphase VCO

The block diagram of the SSCG using a multiphase VCO with a spread spectrum generator is shown in Fig. 1.5 [7]. The VCO has 32 phase outputs. The spread spectrum generator picks up a sequence of suitable phases to periodically change the period of the VCO. The simplified block diagram of the spread spectrum generator is shown in the down side of Fig. 1.5. The spread spectrum generator uses a controller to adjust the up-down counter dependent on the current output phase. The up-down counter is fed into a 5-to-32 decoder to pick up one of 32 phases via 32-to-1 multiplexer and then feedback to the up-down counter with a frequency divided by 2. The advantage of this technique is that only some digital circuits are added to implement the function of SSCG and therefore, it is easy to be integrated in VLSI. But the maximal jitter is determined by the resolution of the multiphase generation. If one needs to minimize the jitter, the number of VCO phase needs to

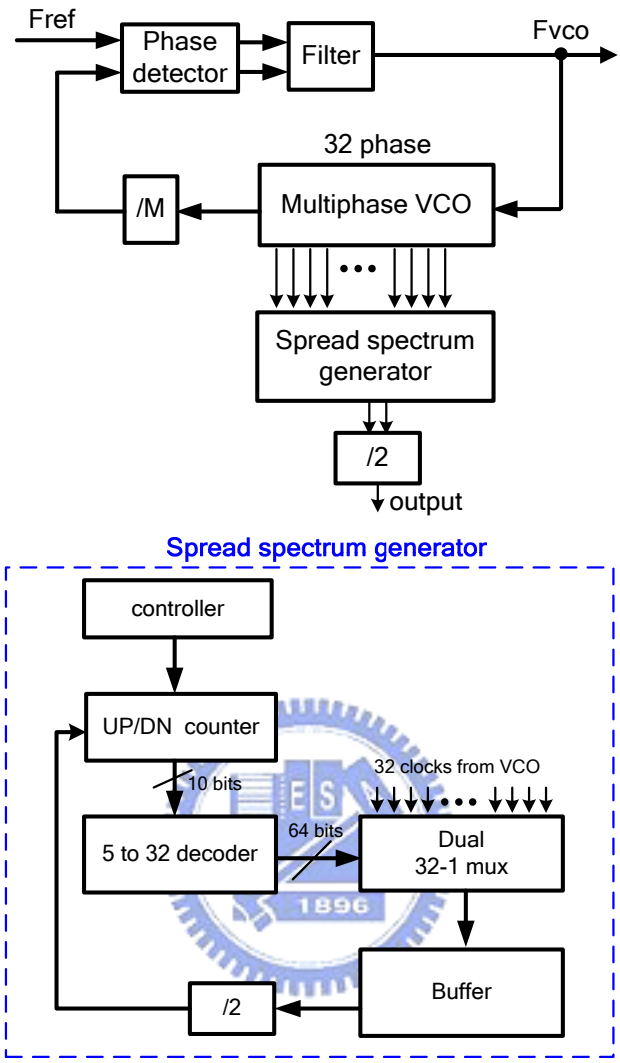


Fig. 1.5. Block diagram of SSCG using the multiphase VCO.

Table 1.1 SSCG Performance Comparisons for Different Architectures

Modulation method	**Sigma-delta**	**VCO**	**Multi-phase**
EMI performance	Good	Good	Bad
Jitter performance	Moderate	Good	Bad
Integration	Good	Bad	Good
Loop filter area	Small	Large	Small
Spread ratio accuracy	Good	Bad	Moderate
Operation frequency	High	High	Low

be increased and in the mean time, the power consumption and area will be increased as well. In other words, it is not suitable for high frequency application like SATA. In addition, the accuracy of each phase will affect the linearity of the modulation profile and the EMI performance.

1.1.4 Performance Comparison Between Different SSCG Architectures

The SSCG performance comparisons for different architectures are listed in Table 1.1. Three architectures discussed above (1.1.1~1.1.3) are taken into consideration. Key parameters like EMI performance, jitter performance, flexibility to integration, loop filter area, spread ratio accuracy and operation frequency are compared. The Fractional-N based SSCG using a sigma-delta modulator has the most advantages among these architectures; therefore, there are more and more literatures [9], [10], [13], [15], [22], [23], [24], [36], [37] using this architectures. The SSCG using direct VCO modulation has advantages of good EMI and jitter performance and high operation frequency except some drawbacks like large loop filter areas, obstacles to triangular waveform generation and bad spread ratio accuracy.

1.2 Motivation

SSCG is known to a key component in many consumer and portable products such as personal computer, notebook computer, printer, projector, scanner and LCD TV. The request of a low cost and high performance SSCG is expanding especially for integration on system on chips (SOC). In this thesis, we proposed four different SSCGs with three kinds of modulation schemes. First, the fractional-N PLL with a ΔΣ modulator [8]-[9] has advantages of being fully digital controlled and of being indirect modulated the sensitive VCO according to the analysis in section 1.1. But, the input range of the conventional ΔΣ modulator is limited. The required input range is determined by the spread ratio and target frequency. An overflow problem which may be encountered as the spread ratio is exceeded its input range. This problem will result in the stability problem and frequency error; therefore, the EMI reduction and jitter performance will be degraded very much. In Chapter 2, the input range of the proposed ΔΣ modulator is enhanced to accommodate a wide variety of divider ratio. In Ref.

[9], a method with a level shifter is used to shift the modulation profile to keep within the input range of the ΔΣ modulator. However, some more circuits and complicated algorithm are needed. Here, a simpler method with an extra bit added to the output of the first stage modulator is presented to extend the input range of ΔΣ modulator, solve saturation problem and thus, reduce the jitter introduced by the non-correct modulation.

Then, a voltage controlled oscillator (VCO) modulated SSCG has the advantages of a simple circuit structure and the absence of sigma-delta modulator noise, but has two major issues according to the analysis in section 1.1. One major issue is that the generation of the triangular waveform depends on special relationship between loop filter. This dependency makes it less flexible. The other issue is the required large capacitance (more than tens of nF) to make it hard totally integration the loop bandwidth of a PLL has to be much less than the modulation frequency to allow the frequency variation of the VCO. Recently, the technique of capacitance multiplication is proposed to eradiate this problem [16], [18]-[20]. However, in order to accommodate another charge pump to generate the triangular modulation, a floating capacitor is connected [16]. The floating capacitor needs extra masks and process steps. In Chapter 3, a modified architecture with a grounded capacitor in mixed configuration containing both a dual-path loop filter (DPLF) [18] and an extra charge-pump circuit is proposed to attain a smaller size and triangular modulation. This method also reduces both hardware complexity and chip area.

Finally, re-considering the fractional-N based SSCG with a ΔΣ modulator, the allocation of three frequencies of modulation, loop bandwidth, and phase comparison are very decisive for the performance of low jitter and good EMI. The loop bandwidth needs to be large enough to react sufficiently to the triangular waveform. Otherwise, the modulation profile is distorted and EMI suppression is compromised [24]-[26]. In contrast, much less than the comparison frequency is normally required to filter the quantization noise of ΔΣ modulator and to obtain low jitter. To obtain sufficient suppression in the case of a large bandwidth, a third-order ΔΣ modulator is normally employed. However, the power consumption and area associated with this type of modulator are a disadvantage. Therefore, in Chapter 4 and 5, an alternative method with two-point modulation is proposed. Both the divider ratio and the voltage controlled oscillator are varied. An all-pass characteristic of the two point modulation

can enhance modulation bandwidth in order that the modulation profile accuracy and jitter performance caused by the ΔΣ modulator can be improved at the same time. Furthermore, only a second order ΔΣ modulator is required, which reduces both the required power and chip area. The simulation time is also a concern when implementing SSCGs due to low modulation frequency and high output frequency. In order to obtain the correct EMI levels, the output spectrum obtained through Fourier transform needs large data and therefore requires the long simulation time. Here, an efficient model built in Matlab [33] is developed to reduce the simulation time dramatically.

1.3 Organization

In the rest of this dissertation, we focus on the design and implementation of the SSCG based on PLL. Three proposed SSCG are discussed.

In chapter 2, an extended input range ΔΣ modulator is developed and a fractional-N based SSCG utilizing the new ΔΣ modulator is designed and analyzed. Theoretical analysis for the input range of the new ΔΣ modulator is derived. Few simulations are made to compare the proposed SSCG and the conventional SSCG. Experimental results are coincided with the simulation results.

Chapter 3 focuses on the improvement of the SSCG using direct VCO modulation. A compact SSCG using a dual-path loop-filter combined another charge-pump can make the SSCG fully integration. The non-ideality of the dual-path loop-filter is analyzed. The phase noise of the SSCG is intensively studied. The modulation limitation and spurious modulation is also analyzed. Measurements show good agreement with the simulation results.

Chapter 4 presents a proposed SSCG with a two-point modulation. By mixing the analog modulation (VCO modulation) and the digital modulation (ΔΣ modulation), the proposed SSCG features good EMI performance and jitter performance by optimizing the loop bandwidth and the order of the ΔΣ modulator. The jitter and EMI from the quantization noise of the ΔΣ modulator and the VCO phase noise are deeply diagnosed. The simulation time is dramatically reduced by a well-built Matlab model. This model can analyze and predict the EMI performance and the jitter performance. The proposed DAC and other circuits are described. Measurements show good correspondence with the simulation results.

Chapter 5 develops another two-point SSCG for the application of SATA. The proposed DAC and the adopted dual-path loop filter are discussed. The linear model of the system including phase noise and jitter are presented. The major circuits are also discussed. Measurements can meet SATA specifications and agree with the simulation results.

Finally, the conclusion of this thesis is given in Chapter 6.

CHAPTER 2

A Wide Input-Range ΔΣ Modulator for Applications to Spread-Spectrum Clock Generator

A spread-spectrum clock generator (SSCG) using fractional-N phase-locked loop (PLL) with an extended range sigma-delta (ΔΣ) modulator is presented. The proposed ΔΣ modulator simply adds an extra output bit in the first stage modulator. It can enlarge the input range about three times as compared to the conventional modulator and solve the saturation problem when the input exceeds the boundary of the conventional modulator. A flexible digital modulation controller can generate center and down spread-spectrum modulation and each has spread ratios of 0.4%, 0.8%, 1.6% and 3.2%. The proposed SSCG has been fabricated in TSMC 0.35-um double-poly quadruple-metal CMOS process with output frequency of 300 MHz. The active area is 0.63×0.62 mm^2 and the power consumption is 17.5 mW.

2.1 Introduction

Spread-spectrum clock generators have been widely used in the PC-based equipments as an effective method to reduce the high frequency emissions. Through the frequency modulation, the energy in each clock harmonic is spread evenly over a dedicated bandwidth, and thus, the power level at each clock harmonic is reduced as much as 10-20 dB, depending on the modulation index and the speed. Several techniques for spectrum spreading have been developed [2]-[9]. The fractional-N PLL with a ΔΣ modulator [8]-[9] has recently received much attention due to its advantages of being fully digital controlled and of being indirect modulated the sensitive VCO. The wider input range of the ΔΣ modulator is requested under the spread spectrum mode because the divider ratio changes all the time. An overflow problem may be encountered as the divider is set near the input boundary. Especially, in PC applications, a wide variety of divider numbers are often applied for different CPU

frequencies. For an example with the reference frequency (F_{ref}) at 14.318 MHz and the output frequency at 300 MHz, the average value of the divider is 20.9526. Under a 3.2% deviation in center spread-spectrum mode, the variation of the fractional part is from 0.6173 to 1.2878, which crosses the unity boundary. However, the input range of the conventional ΔΣ modulator is limited under unity as its architecture is defined. Exceeding the input range will cause the stability problem and frequency error. In this study, the input range is enhanced to accommodate a wide variety of divider ratio. In Ref. [9], a method with a level shifter is used to shift the modulation profile to keep within the input range of the ΔΣ modulator. Therefore, some extra circuits are needed and make the modulator more complicated. Here, a simpler method with an extra bit added to the output of the first stage modulator is presented to extend the input range of ΔΣ modulator, solve saturation problem and thus, reduce the jitter introduced by the non-correct modulation.

2.2 Proposed Spread-Spectrum Clock Generator

The block diagram of the proposed spread-spectrum clock generator is shown in Fig. 2.1. It is composed of a phase frequency detector (PFD), a charge pump circuit (CP), an off-chip loop filter (LF), a VCO, an asynchronous programmable counter (ASPC) and a digital modulation controller (DMC). The ΔΣ modulator of MASH type is employed due to the advantages of unconditional stability and easy high-order implementation. [11], [12]

2.2.1 Digital Modulation Controller

DMC which consists of a spread-spectrum profile generator and a ΔΣ modulator is used to control the divider value of ASPC. The profile generator as shown in Fig. 2.2(a) consists of a triangle wave generator and a profile controller to control the frequency deviation and spreading direction. The output of the controller denoted as INSD[k], where k is an integer, is fed to the ΔΣ modulator. The waveform of INSD[k] is shown in Fig. 2.2(b). The amplitude of the triangle wave, V_{amp}, controlled by SSPER is used to decide the frequency deviation ratio. The mean value of the triangle wave, FN_{mean}, controlled by SSTYP, is used to decide the center frequency of the SSCG. The maximal number of INSD[k], $INSD[k]_{max}$, is given as

$$INSD[k]_{\max} = FN_{mean} + V_{amp}. \tag{2.1}$$

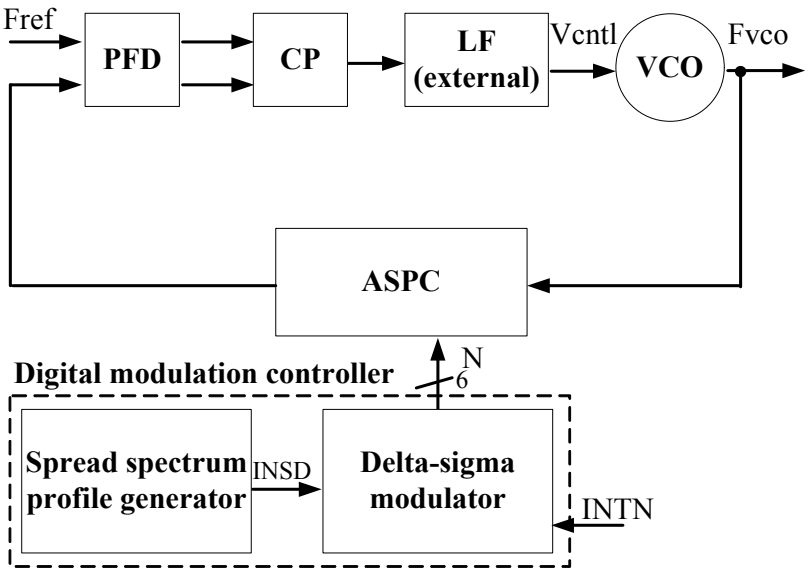


Fig. 2.1. Block diagram of the spread-spectrum clock generator.

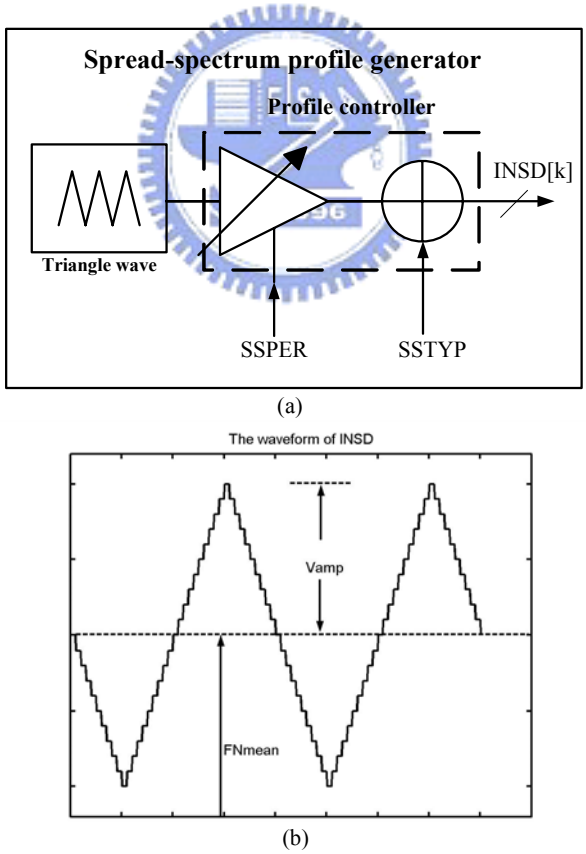


Fig. 2.2. (a) Proposed spread-spectrum profile generator, and (b) The output waveform at INSD.

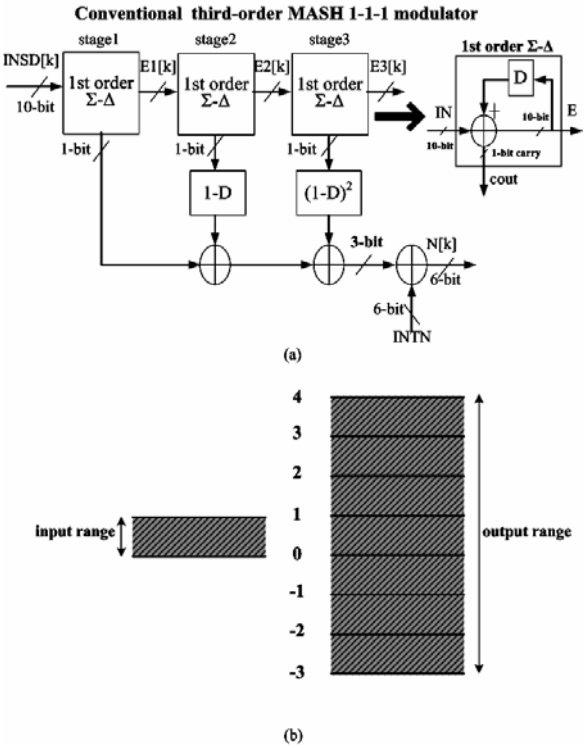


Fig. 2.3. Convectional third-order MASH 1-1-1 modulator (a) architecture and (b) input and output range.

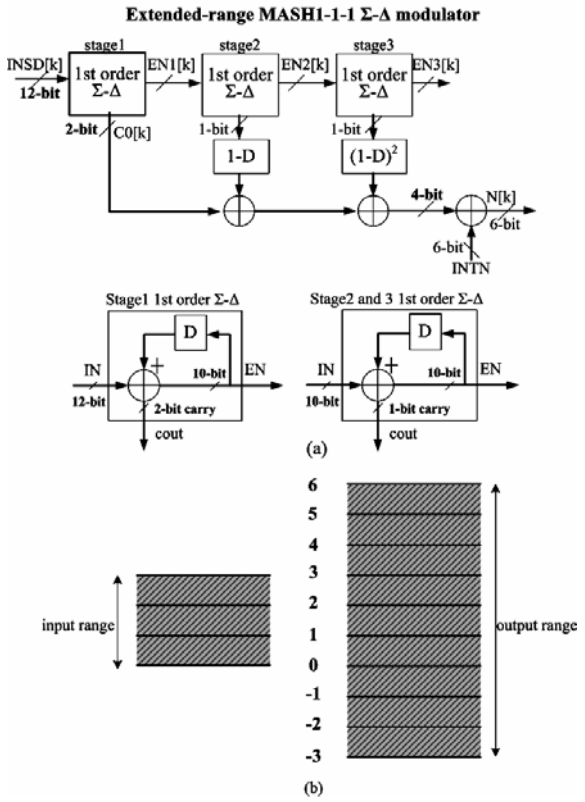


Fig. 2.4. Proposed extended range MASH-type modulator (a) architecture and (b) input and output range.

The peak-to-peak frequency deviation ratio, $F_{dev,pp}$, is given as

$$F_{dev,pp} = \frac{2 \times V_{amp}}{INTN \times 2^{BT} + FN_{mean}}, \quad (2.2)$$

where INTN is the integer part of the divider and BT is bit width of the modulator. In this design, there are two kinds of spread direction, i.e. center spread and down spread, and four peak-to-peak frequency deviation indexes: 0.4%, 0.8%, 1.6% and 3.2%. The frequency of the triangle wave is set at 40 kHz.

2.2.2 Modified ΔΣ Modulator

For clarity, the disadvantage of the conventional modulator as shown in Fig. 2.3(a) is indicated. Three first-order modulators are cascaded to implement a third-order MASH 1-1-1 modulator. The block diagram of each stage is shown in the right of Fig. 2.3(a), which is simply an accumulator with one-bit carry output. Both the input and output ranges are illustrated in Fig. 2.3(b). The exact input range is from $1/2^{BT}$ to $(2^{BT}-1)/2^{BT}$. It implies $INSD[k]_{max}$ is $(2^{BT}-1)$. Here BT=10. Each of the outputs of the three stages is 0 and 1. The output of the second stage passes through a differentiator and then its possible values become -1, 0 and 1. The output of the third stage passes through two differentiators and then its possible values become -2, -1, 0, 1 and 2. Summing the three branches together yields 8 possible outputs, i.e., -3, -2, -1, 0, 1, 2, 3 and 4. Therefore, the output range of the modulator is from -3 to +4 to accommodate all the possible inputs. So that 3bits at output are built. If INSD[k] is modulated beyond $(2^{BT}-1)$, then the modulator is saturated and can not function well. Therefore, such an arrangement can't meet our requirement.

The proposed one with extended input range is shown in Fig. 2.4(a). Two different kinds of first-order ΔΣ modulator are employed. The block diagrams are shown in the bottom of Fig. 2.4(a). In stage-1 modulator, a 2-bit carry output denoted as C0[k] is designed. Stage2 and stage3 are unchanged. The inputs to the stage-1, stage-2, and stage-3 are denoted as INSD[k], EN1[k], and EN2[k], respectively. With the 2-bit carry output in stage-1 modulator, the input value INSD[k] can be set equal to or larger than one without error occurrence. As the input value is bigger than one, the stage-1 modulator can response quickly the integer part of the input to the output and will not saturate the following stages. The difference equation for

stage-1 modulator is given as follows. Let

$$SUM[k] = INSD[k] + EN1[k-1]. \tag{2.3}$$

Then

$$\begin{aligned} &EN1[k] \\ &= SUM[k],\ for\ \ 0 < SUM[k] < 2^{BT} \\ &= SUM[k] - 2^{BT},\ for\ \ 2^{BT} \le SUM[k] < 2^{(BT+1)} \\ &= SUM[k] - 2^{(BT+1)},\ for\ \ 2^{(BT+1)} \le SUM[k] < 3\times 2^{BT} \\ &= SUM[k] - 3\times 2^{BT},\ for\ \ 3\times 2^{BT} \le SUM[k] < 2^{(BT+2)} \end{aligned}. \tag{2.4}$$

And

$$\begin{aligned} C0[k] &= 0,\ for\ \ 0 < SUM[k] < 2^{BT} \\ &= 1,\ for\ \ 2^{BT} \le SUM[k] < 2^{(BT+1)} \\ &= 2,\ for\ \ 2^{(BT+1)} \le SUM[k] < 3\times 2^{BT} \\ &= 3,\ for\ \ 3\times 2^{BT} \le SUM[k] < 2^{(BT+2)} \end{aligned}. \tag{2.5}$$

From (2.4), the maximal number of EN1[k], $EN1[k]_{max}$ can be found as 2^{BT}-1. From (2.5), the maximal number of C0[k] is equal to 3 and, thus, a two-bit carry output is needed. From (2.4) and (2.5), the maximal number of SUM[k], $SUM[k]_{max}$ can be found as $2^{(BT+2)}$-1. Substitute $EN1[k]_{max}$ and $SUM[k]_{max}$ into (2.3), $INSD[k]_{max}$ can be obtained as $3\times 2^{BT} - 1$. The maximal input number of the proposed modulator is about 3 times compared to conventional modulator and hence extra two input bits are added. The output range of the proposed modulator becomes from -3 to 6. One extra bit is added. The input range and output range of the proposed modulator are shown in Fig. 2.4(b). The minimal input number of the proposed modulator is 1, which is the same to the conventional one.

From (2.1), one can get the following equation.

$$INSD[k]_{max} = FN_{mean} + V_{amp} = 3\times 2^{BT} - 1 \tag{2.6}$$

From (2.6) the advantages of the proposed modulator can be seen. When FN_{mean} is equal to (2^{BT}-1), which is the largest input number for the conventional modulator, the maximal number of V_{amp} is 0. Here, the maximal number of V_{amp} for the proposed architecture can be found as (2^{BT}-2) by (2.6). When FN_{mean} is equal to 1, which is the smallest input number for the conventional modulator, the maximal number of Vamp is 0. However, in proposed architecture, we can reduce the integer part of the divider by 1, and change the FN_{mean} to

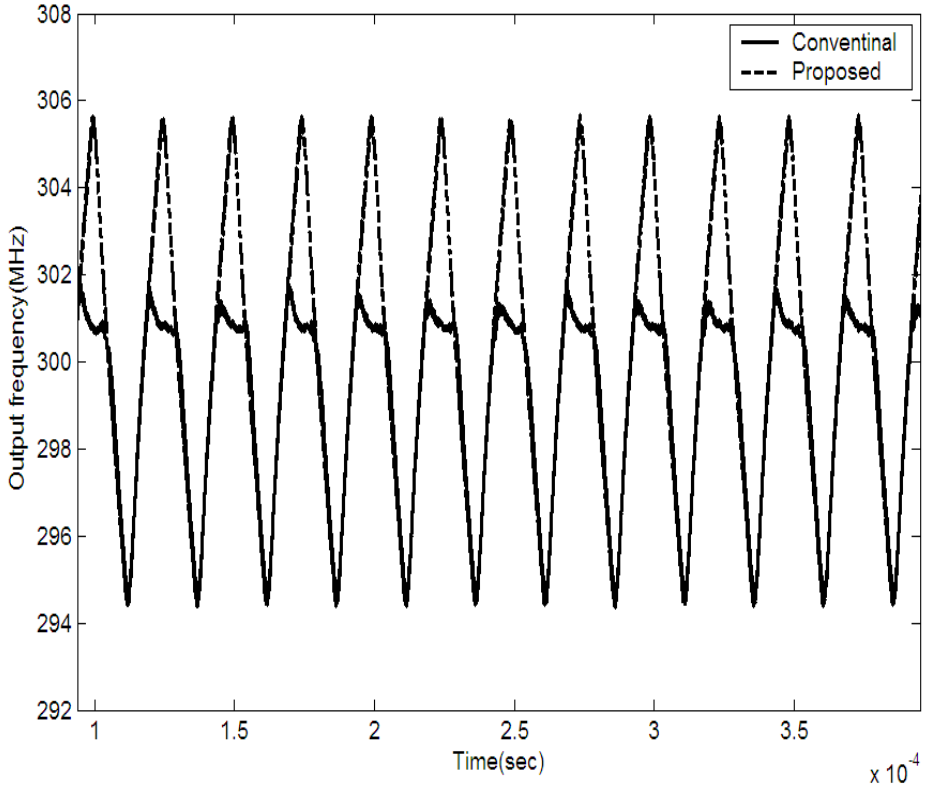
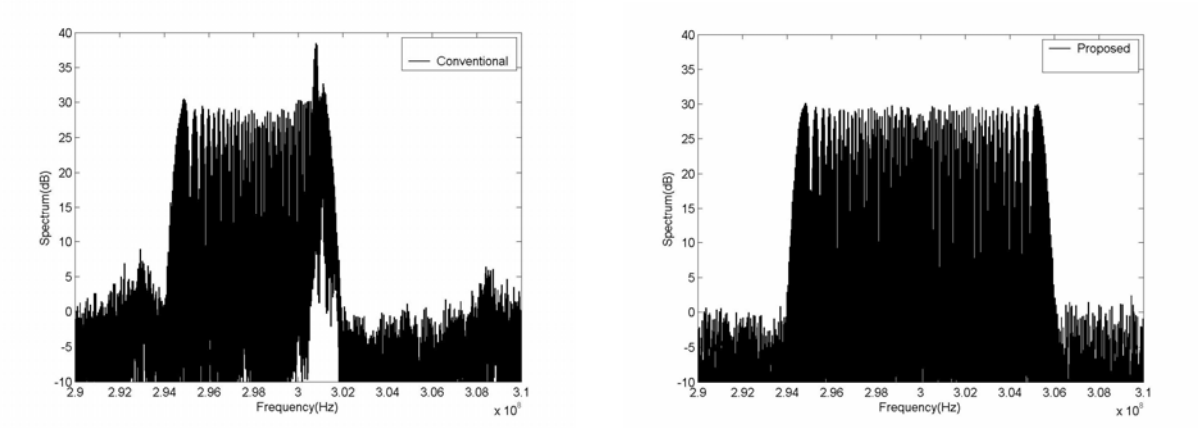


Fig. 2.5. The 300MHz output frequency simulation results for conventional (solid line) and proposed (broken line) architectures at the 3.2% center-spread spectrum mode.



(a) (b)

Fig. 2.6. The 300MHz output FFT simulation results of (a) conventional architecture and (b) proposed architecture at the 3.2% center-spread spectrum mode.

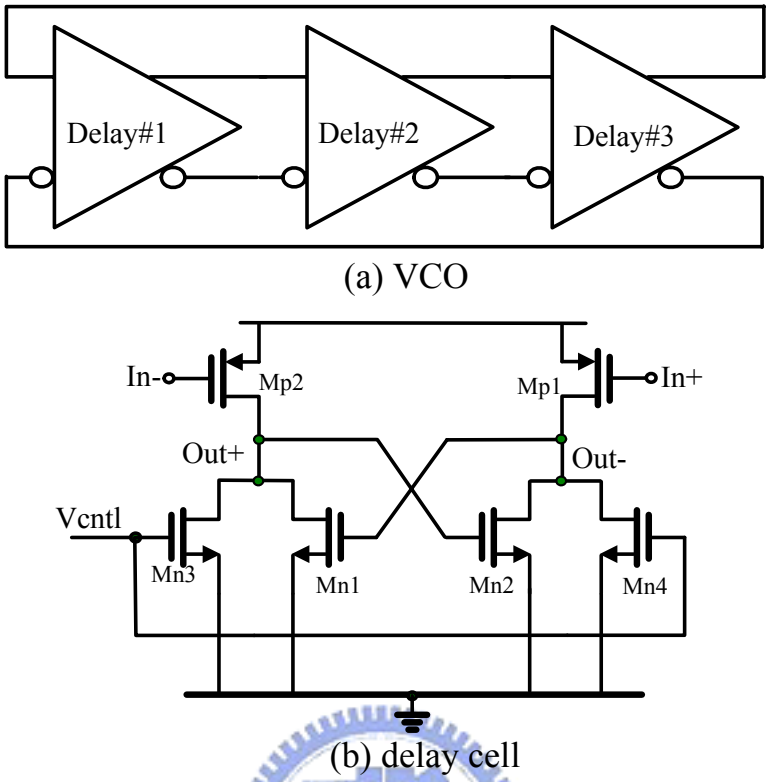


Fig. 2.7. (a) VCO with three-stage delay cells and (b) Schematic of each delay cell.

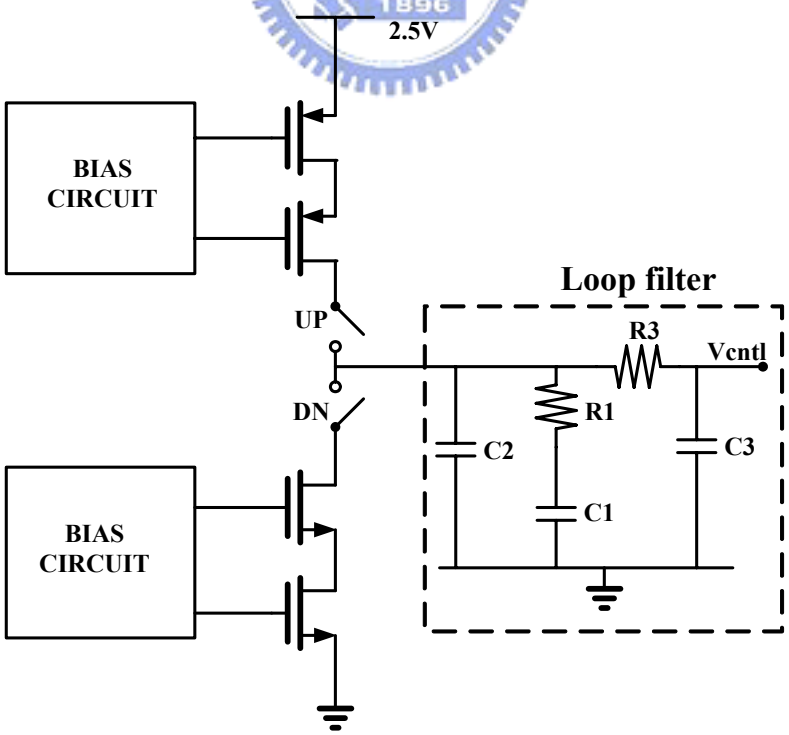


Fig. 2.8. Charge-pump and loop filter circuit.

(2^{BT}+1). Then the maximal number of Vamp is 2^{BT}. The maximal frequency deviation appears when $FN_{mean}=V_{amp}$, which is almost half of the input range. Therefore, one can efficiently use the the proposed modulator by simply shifting FN_{mean} to $FN_{mean}+2^{BT}$.

The numerical comparisons of the output frequency between two architectures are illustrated in Fig. 2.5 and Fig. 2.6. The results are obtained from time-domain model built by MATLAB. The simulation case is a 300 MHz output with a 3.2% center-spread spectrum with the input frequency of 14.318 MHz. The fractional part of the modulator is changed between 0.6173 and 1.2878 and the mean value is 0.9526 as we mentioned above. Given BT=10, $FN_{mean} = 2^{BT}\times0.9526 = 975$, and $V_{amp} =2^{BT}\times(1.2878-0.6173)/2 = 343$.

Fig. 2.5 shows the output frequency swing with respect to time for two architectures. It is shown that the solid line from the conventional modulator is clamped near 301 MHz, On the contrary, the curve by broken line can response well. Fig. 2.6(a) and 2.6(b) show the corresponding FFT results. The output spectrum in Fig. 2.6(a) for conventional modulator appears a peak near center frequency and a narrow peak-to-peak spreading ratio. However, the proposed one can correctly response the spreading profile.

The maximal frequency deviation can also be predicted. In above case, the maximal number of V_{amp} can be found as 974, which is equal to (FN_{mean}-1). The INTN in this case is 20. From (2.2), the maximal peak-to-peak frequency deviation ratio can be found as 9.07%. On the contrary, the conventional one only achieves 0.23% maximal peak-to-peak frequency deviation ratio. In summary, using this simple two carry-bits technique, the modulator can avoid the saturation region and enlarge the frequency deviation. Usually the spread spectrum ratio is less than 5% because of the jitter consideration. Therefore, the proposed SSCG can fulfill the requirement.

2.3 Circuit Description

The circuits in building blocks of Fig. 2.1 are briefly described. The wide band VCO which consists of the three stages of differential delay cells is shown in Fig. 2.7(a). The schematic of the cell is shown in Fig. 2.7(b). [10] The cross-coupled transistors, Mn1 and Mn2, give the VCO full swing and sharpen the edge of the output signal to reduce the jitter.

The transistors, Mn3 and Mn4, control the frequency of VCO. The voltage to current converter that will cause extra jitter is not needed because it is a voltage-controlled oscillator. The tail current source is also avoided for low voltage application and for lower flicker noise up-conversion. [10] A 6-bit ASPC is adopted here for low power consumption. The charge-pump circuit and loop filter circuit are shown in Fig. 2.8. The cascoded current source is employed for good immunity against the power supper noise. The wide-swing bias circuit, which is not shown in the Fig. 2.8, is designed for low voltage operation. The controlling signals for UP and DN switches are fed from the output of PFD. The current of the charge pump is 6 uA and an external 3rd-order low-pass filter is used in this work to filter out the quantization noise of the modulator. The loop bandwidth of the PLL is traded off between modulation speed and modulator quantization noise. Here, the loop bandwidth of 150 kHz is chosen. The values of the components are listed in Table 2.1.

2.4 Measurement Results

The proposed SSCG has been fabricated in TSMC 0.35-μm double-poly quadruple-metal CMOS process. Fig. 2.9 shows the microphotograph of the chip. The active area is 0.63×0.62 mm^2 and the total area including pads is 1.36×1.35 mm^2. The tuning sensitivity of VCO is shown in Fig. 2.10 with a gain of 270 MHz/V near 300 MHz output. The VCO reveals a good linear voltage to frequency transfer curve and has a maximal frequency more than 600 MHz. Fig. 2.11 indicates that the proposed SSCG operating at nonspread-spectrum mode achieves -104.31 dBc/Hz at 1 MHz offset from the carrier. It also reveals the closed-loop bandwidth of about 150 kHz. Fig. 2.12(a) shows the measured output spectrum at nonspread-spectrum mode. The amplitude is about 5.74 dBm. Fig. 2.12(b) shows the measured output spectrum under the 0.8% option in center spread-spectrum mode. The peak reduction is about 15.82 dB as compared to Fig. 2.12(a), which is very close to predicted results of 15.68 dB shown in Fig. 13. Fig. 2.12(c) shows the measured output spectrum under the 3.2% option in center spread-spectrum mode. The peak reduction is about 20.54 dB as compared to Fig. 2.12(a) that is slightly smaller than the predicted 21.36 dB in Fig. 2.14. This is because there exists small peaks at two ends of the measured spectrum. The phenomenon is due to the insufficient loop bandwidth. When the loop bandwidth is not

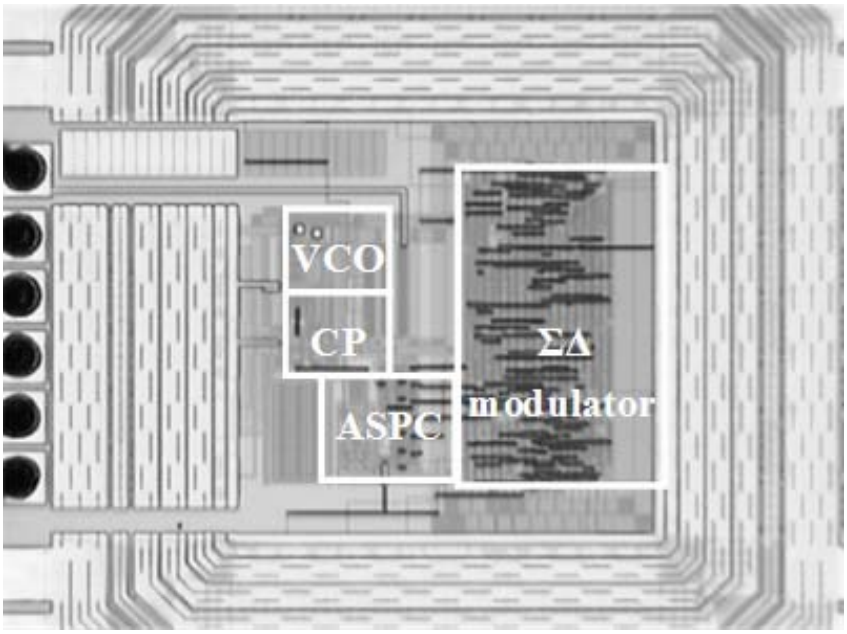


Fig. 2.9. Microphotograph of the proposed SSCG.

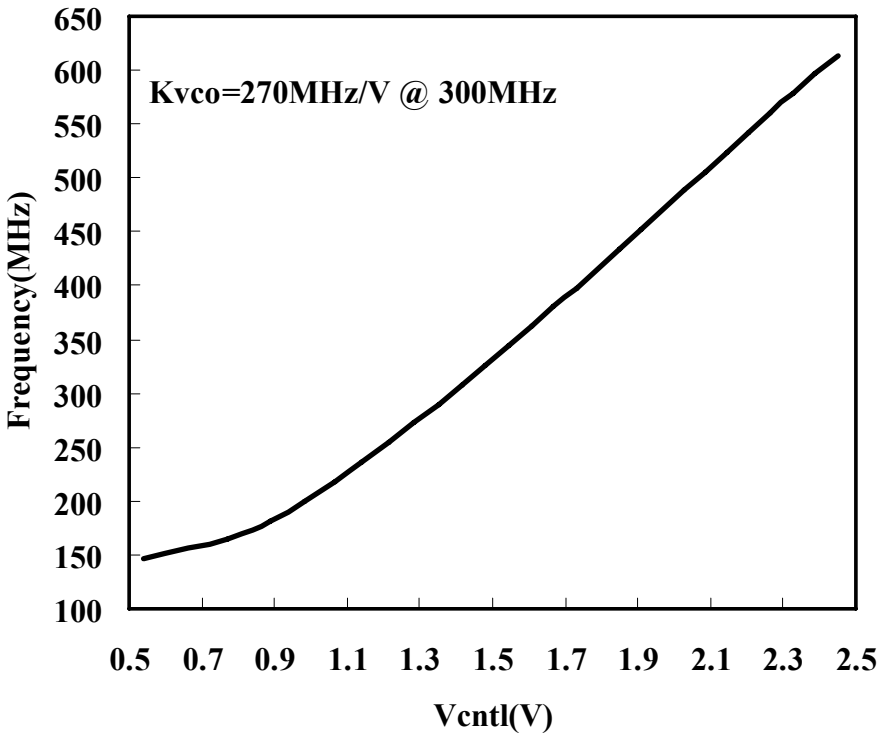


Fig. 2.10. Measured VCO frequency tuning curve.

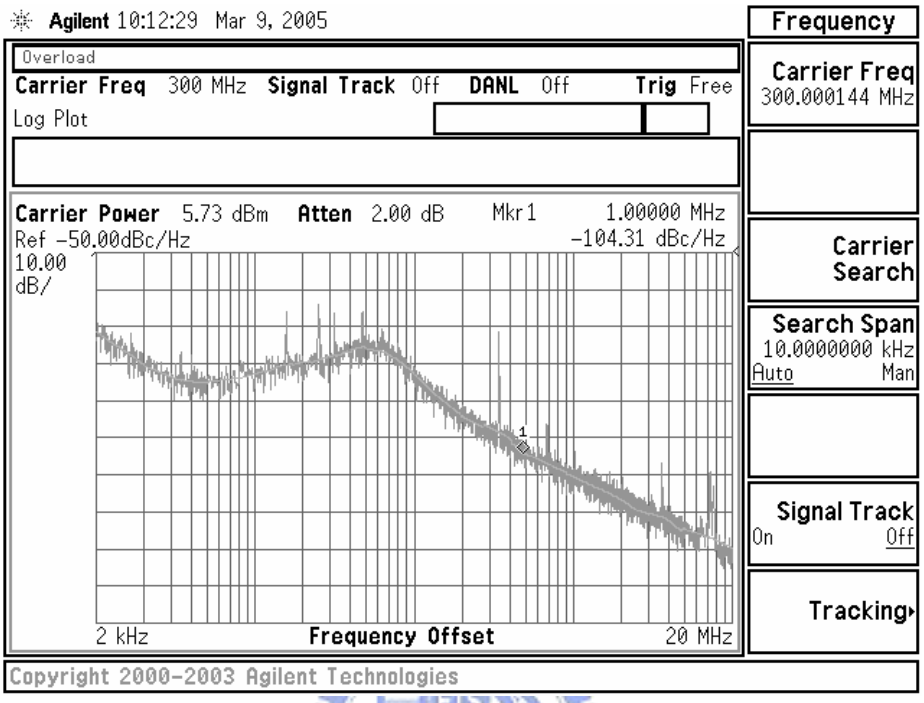
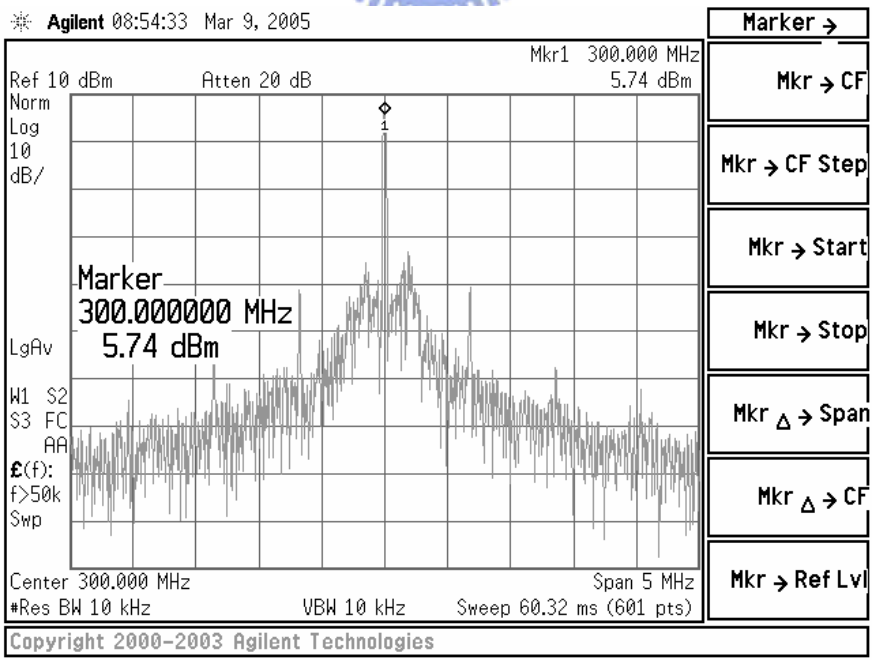
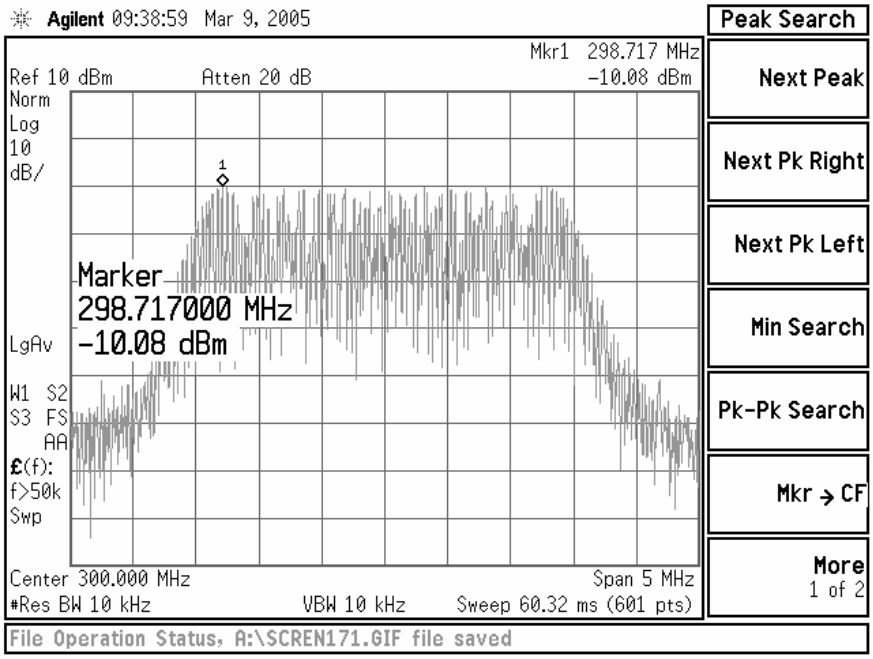


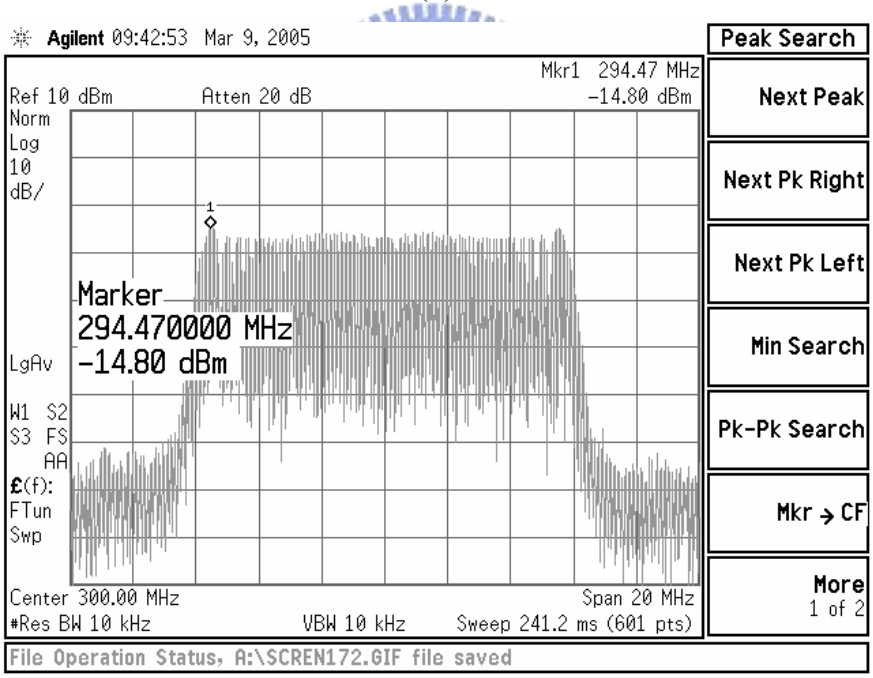
Fig. 2.11. Phase noise measurement at non-spread spectrum mode.



(a)



(b)



(c)

Fig. 2.12. Measured spectrum (a) at non-spread spectrum mode, (b) at spread-spectrum mode with 0.8% center spread ratio, and (c) with 3.2% center spread ratio.

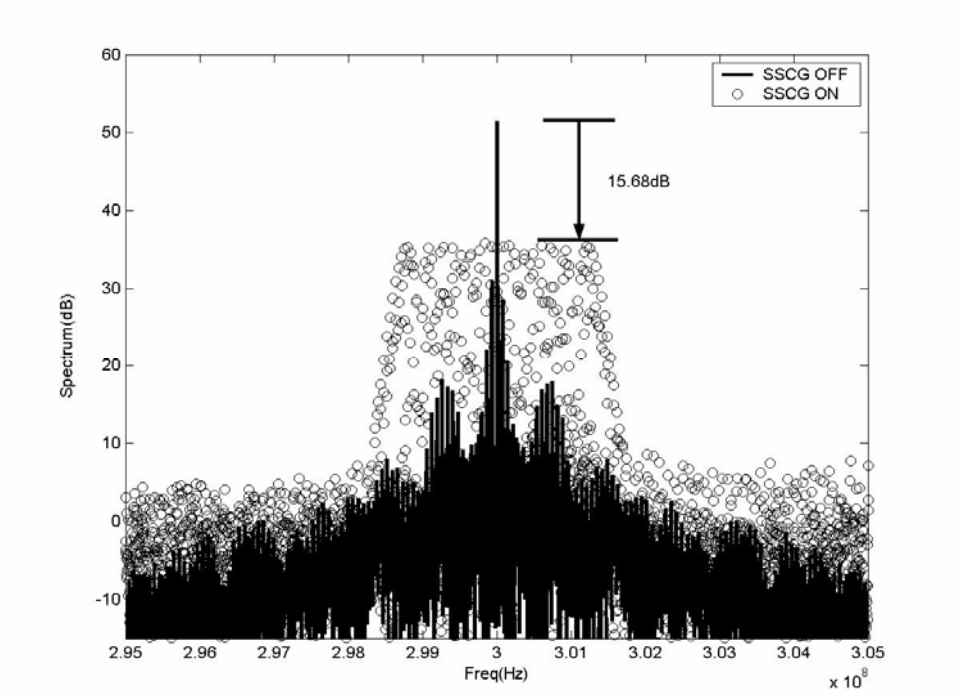


Fig. 2.13. Comparison for FFT simulation results for spread-spectrum mode on with 0.8% center spread (o) and off (black).

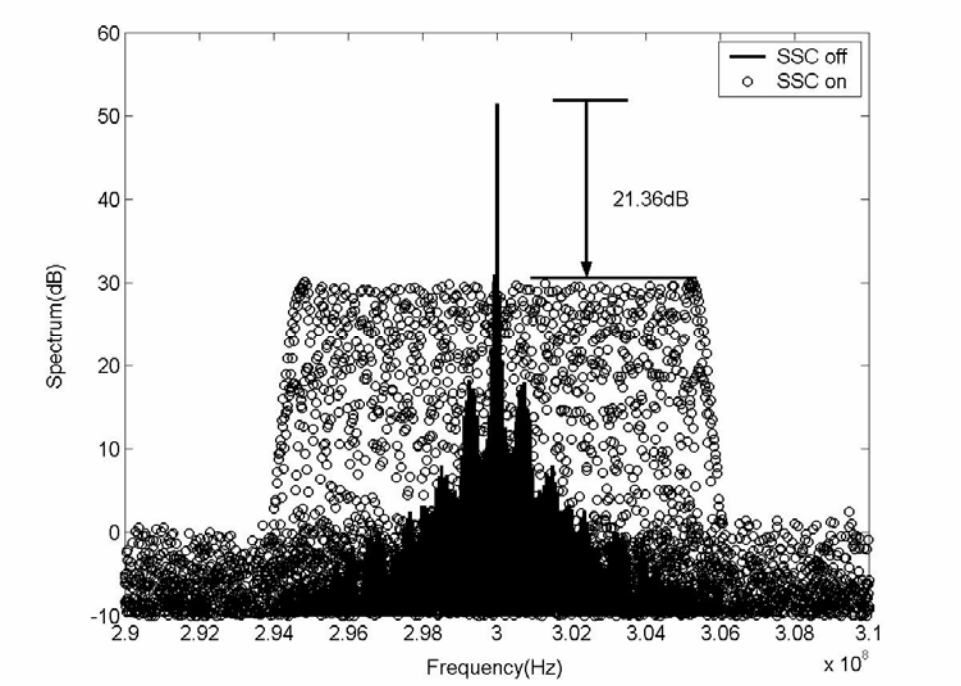
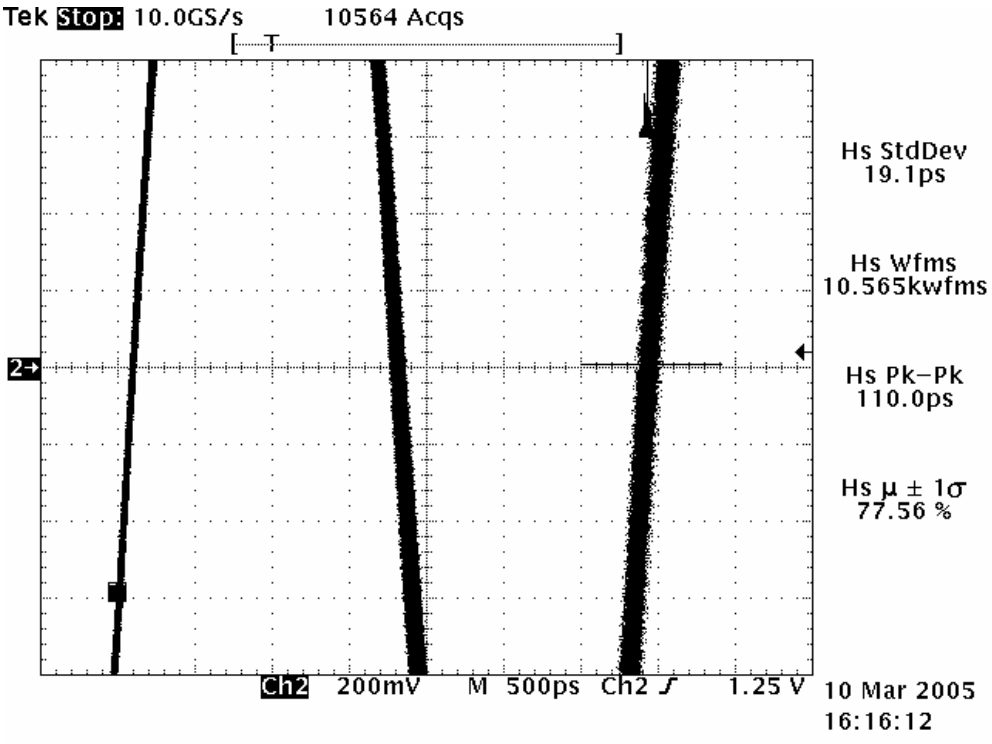
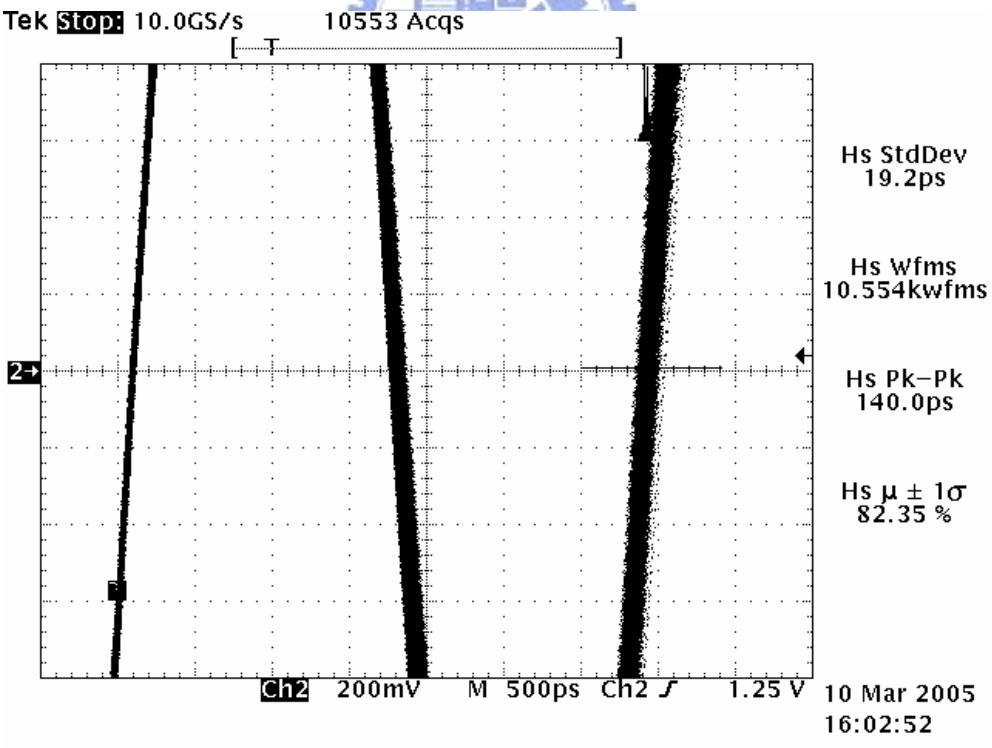


Fig. 2.14. FFT simulation results for spread-spectrum on with 3.2% center spread (o) and off (black).



(a)



(b)

Fig. 2.15. Measured period jitter (a) at non-spread spectrum mode, and (b) with the center spread ratio of 0.8%.

enough to pass through high frequency components of the triangle signal, the modulation profile will be destroyed especially at the two ends. It is also founded in our simulation result of Fig. 2.6(b). The jitter performances at non-spread spectrum mode and spread-spectrum mode are shown in Fig. 2.15(a) and 2.15(b), respectively. The peak-to-peak jitter is 110 ps in non-spread spectrum mode and 140 ps under the 0.8% option. Table 2.1 gives the performance summary of the SSCG. Table 2.2 gives the comparison of EMI reduction between simulation and measurement.

2.5 Summary

In this work, an extended range MASH-type ΔΣ modulator is presented to solve the input range problems when the fractional-N PLL is operated as the SSCG. At the expanse of two extra input bits and one extra carry bit the proposed modulator is proven to have about 3 times input range as compared to conventional modulator. In the meantime the modulator can handle up to 9% frequency deviation. The spreading ratio and direction can be easily obtained by adjusting the amplitude and DC value of the digital triangle wave. The SSCG is implemented in TSMC 0.35 μm double-poly quadruple- metal CMOS process. Measurement results at 300 MHz under 0.8% and 3.2% spread ratio are in good agreements with the predictions. These results can be further applied to a wide variety of clock sources with spreading spectrum.

Table 2.1 Performance Summary

Modulation Method	Modulation on divider
Modulation Type	Center-spread/Down-spread
Modulation Frequency	40 kHz
Spread Ratios(pp)	0.4%,0.8%,1.6%,3.2%
Output Frequency	300 MHz
Input Frequency	14.31818 MHz
VCO Gain(Kvco)	270 MHz/V
Loop bandwidth	~150 kHz
Loop filter	R1=12 kΩ C1=400 pF C2=40 pF R3=10 kΩ C3=10 pF
EMI reduction	15.82 dB @ 0.8% center spread ratio 20.54 dB @ 3.2% center spread ratio
Jitter(PP)	110 ps at non-spread spectrum mode
Jitter(PP)	140 ps at spread spectrum mode (0.8%)
Chip Area (active)	0.63×0.62 mm^2
Power Dissipation	17.5 mW including output buffer @ 2.5V

Table 2.2 EMI reduction Between Simulation and Measurement

Condition	Simulation results	Measurement results
Center-spread 0.8%	15.68 dB	15.82 dB
Center-spread 3.2%	21.36 dB	20.54 dB

CHAPTER 3

A Fully Integrated Spread Spectrum Clock Generator by Using Direct VCO Modulation

A compact architecture for a fully-integrated spread spectrum clock generator (SSCG) using VCO direct modulation is presented in this thesis. A dual-path loop filter in the phase-locked loop (PLL) is employed to reduce the size of the capacitance in the filter with the aid of an extra charge pump and a unity gain amplifier. At the same time, a third -charge pump which generates triangular waves is used to perform the function of a spread-spectrum. The proposed circuit has been fabricated using a 0.35 μm CMOS single-poly quadruple-metal process. The clock rate from 50 to 480 MHz with a center spread range of between 0.5% and 2% are verified and are close to the theoretical analyses. The size of the chip area is 0.82×0.8 mm^2 (including the loop filter) and the power consumption was 27.5 mW at 400 MHz.

3.1 Introduction

The electromagnetic interference (EMI) in electronic devices such as a PC, printer, PCI Express and SATA increases rapidly as the clock speed is raised. In many applications, clock generators are one of the major contributors of EMI. Spread-spectrum clock generators (SSCG) are proven to be an efficient way to reduce EMI levels [2]-[4], [7]-[9], [13]-[15]. A SSCG is basically a PLL with an appropriate frequency-modulated output. The frequency modulation is used to spread the output spectrum. There are three kinds of modulation schemes employed in PLLs. The first type involves a change to the divider made by a sigma-delta modulator [8]-[9]. The second type includes either digital manipulation of the output of a multiphase PLL or the use of a DLL/phase interpolator combo on the output of a standard PLL [5]-[7]. The last type involves direct modulation of the VCO in PLL [3]-[4], [16]-[17]. The latter has the advantages of a simple circuit structure and the absence of sigma-delta modulator noise. But the loop bandwidth of a PLL has to be much less than the modulation frequency to allow the frequency variation of the VCO. In general, the required loop bandwidth is about one of ten times that in the modulation. The modulation frequency is

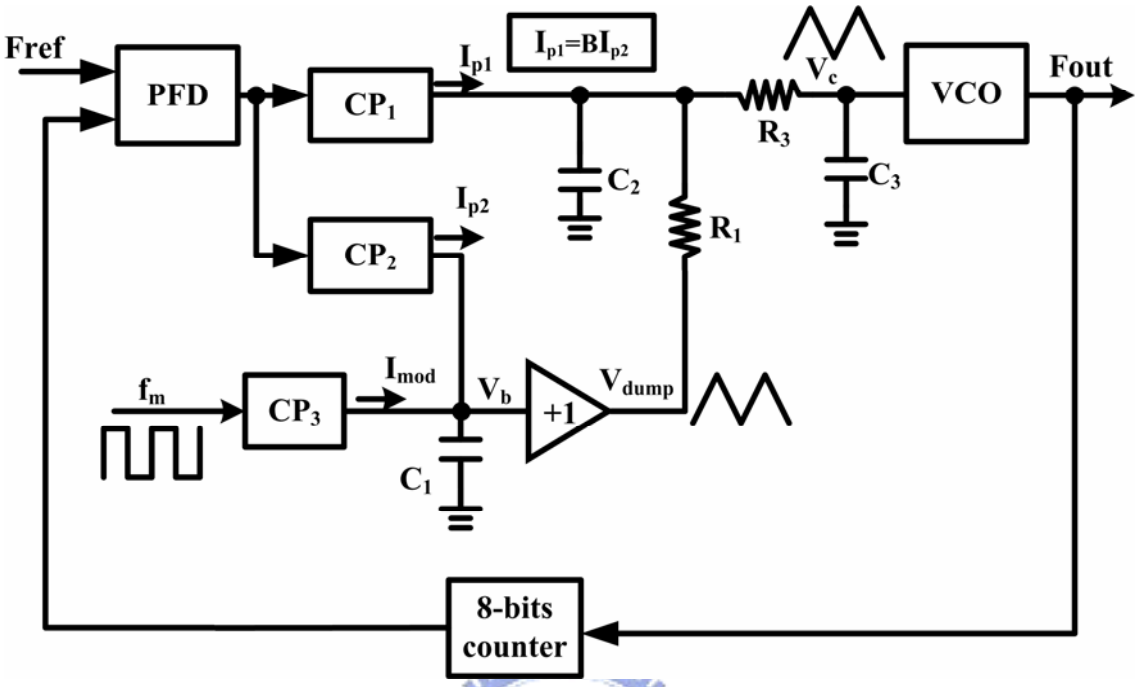


Fig. 3.1. Proposed SSCG.

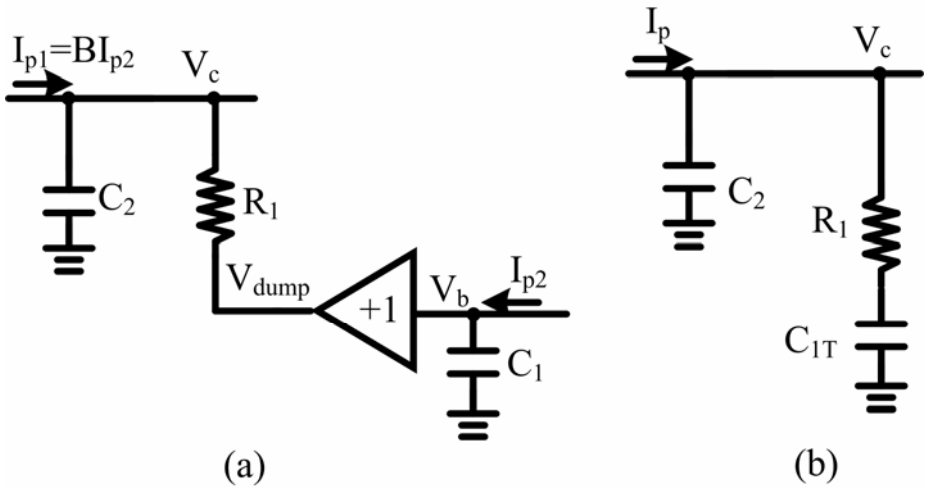


Fig. 3.2. (a) Dual-path loop filter (b) Traditional loop filter.

typically around 30 kHz to 50 kHz so that the loop bandwidth is around 3 kHz to 5 kHz. This leads to a large capacitor of more than 10nF in the loop filter, which becomes too large to be integrated in the chip [3].

Recently, the technique of capacitance multiplication is proposed to eradiate this problem [16], [18]-[20]. However, in order to accommodate another charge pump to generate the triangular modulation, a floating capacitor is connected [16]. The floating capacitor in a standard CMOS process can be PIP (poly to poly) or MIM (metal to metal) and needs extra masks and process steps. It also has the area and cost penalties comparable to those of a MOS capacitor. In this thesis, a modified architecture with a grounded capacitor in mixed configuration containing both a dual-path loop filter (DPLF) [18] and an extra charge-pump circuit is proposed to attain a smaller size and triangular modulation. This method also reduces both hardware complexity and chip area. Although, a non-linear modulation profile known as the 'Hershey-Kiss' profile [2] shows a better EMI performance, its nonlinear equations make it more expensive due to a larger area and power consumption. Therefore, the linear triangular profile is adopted in this thesis.

3.2 Proposed SSCG and its Theoretical Analysis

3.2.1 Proposed SSCG

The proposed SSCG is shown in Fig. 3.1. It consists of a phase-frequency detector (PFD), a dual-path loop filter [18] which is composed of two charge pumps CP_1 and CP_2, a unity-gain buffer, two capacitors C_1 and C_2 and a resistor R_1, a charge pump CP_3, a VCO, and a 8-bits programmable counter. The CP_1 and CP_2 provide the dual-path charging currents I_{p1} and I_{p2}, respectively, to the loop capacitors. The CP_3 provides the charging current I_{mod} to the grounded capacitor C_1 in order to form the triangular waveform of the control voltage V_c. The first path composed of the R_1 and C_2 is a low-pass filter. The second path composed of the C_1 and unity gain buffer acts as an integrator. The voltages from these two paths are combined together so that a zero is created in transfer function. In order to obtain the multiplication effect of the capacitance C_1, the pumping current I_{p1} is set at $I_{p1}=BI_{p2}$ with a factor $B>>1$. To simplify the analysis, the higher order filtering effect of R_3 and C_3 is ignored in the following analysis. The relationship between the controlling voltage V_c and pumping current I_{p1} can be

easily obtained via the dual-path loop filter redrawn in Fig. 3.2(a). The transfer function is given as

$$F(s)=\frac{V_c}{I_{p1}}=\frac{R_1\left(s+\frac{1}{R_1BC_1}\right)}{s\left(1+sR_1C_2\right)}. \tag{3.1}$$

For a comparison, the conventional 2nd-order loop filter with only one charge pump I_p is presented in Fig. 3.2(b), in which both the capacitor C_1 and the unity gain buffer are replaced

by an equivalent capacitor C_{1T}. The corresponding transfer function is given by

$$F(s)=\frac{V_c}{I_p}=\frac{R_1\left(s+\frac{1}{R_1C_{1T}}\right)}{s\frac{C_{1T}+C_2}{C_{1T}}\left(1+sR_1\frac{C_{1T}C_2}{C_{1T}+C_2}\right)}. \tag{3.2}$$

When compared with (3.1), it was found that two circuits have the same zero response under the condition of $BC_1=C_{1T}$. It implies that capacitance C_1 in the former case is B times smaller than C_{1T}. The area of capacitor C_1 can be reduced dramatically by using this technique. In this work, B=50. Moreover, one of terminals in C_1 is grounded. Therefore, capacitor C_1 can be realized by using the MOS capacitor. The pole in (2) is caused from R_1 and a capacitor with C_{1T} and C_2 in series. If $C_{1T}>>C_2$. it is almost equal to that of R_1C_2 in (3.1), It is generally the case that the pole is about ten to hundred times the zero, depending on the damping ratio of the system.

3.2.2 Analysis of the Non-ideality of the Dual-Path Loop Filter

The non-ideality of the dual-path loop filter can be viewed in two ways: filter transfer function and phase noise. The unity gain buffer is built by an OP-AMP, which can be modeled by the DC gain A_v and the gain-bandwidth product ω_t. The transfer function of unity gain buffer can be expressed as

$$A(s)=\frac{A_v/(A_v+1)}{1+\frac{s}{\omega_t}}=\frac{A_{err}}{1+\frac{s}{\omega_t}}, \tag{3.3}$$

where A_{err} denotes the gain error and is less than 1.

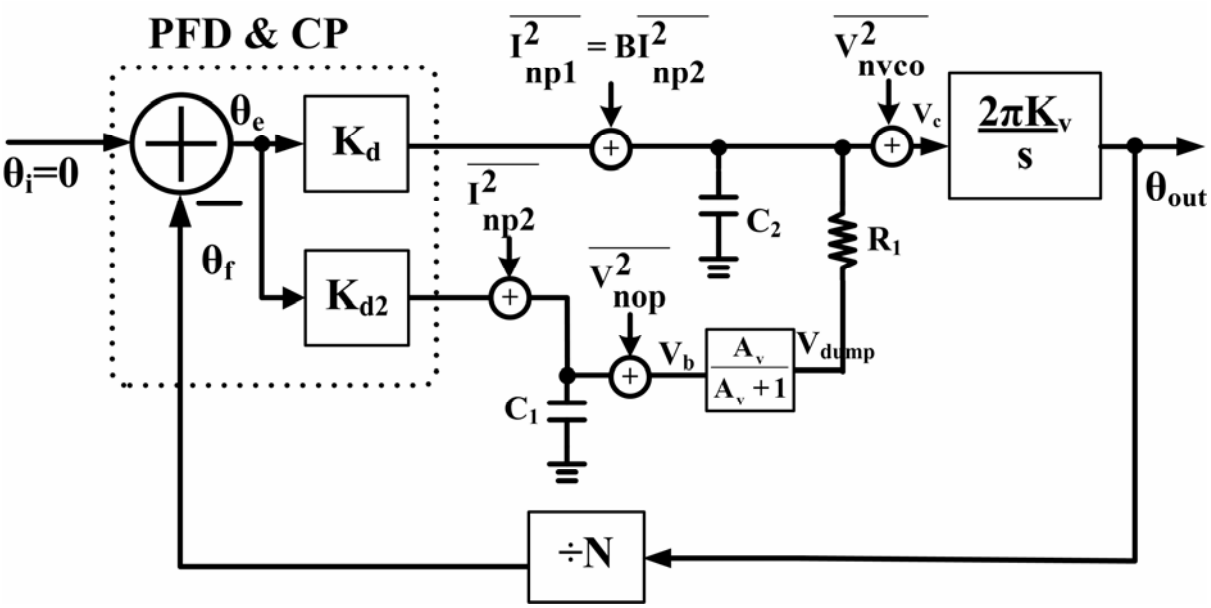


Fig. 3.3. Block diagram with relevant noise sources.

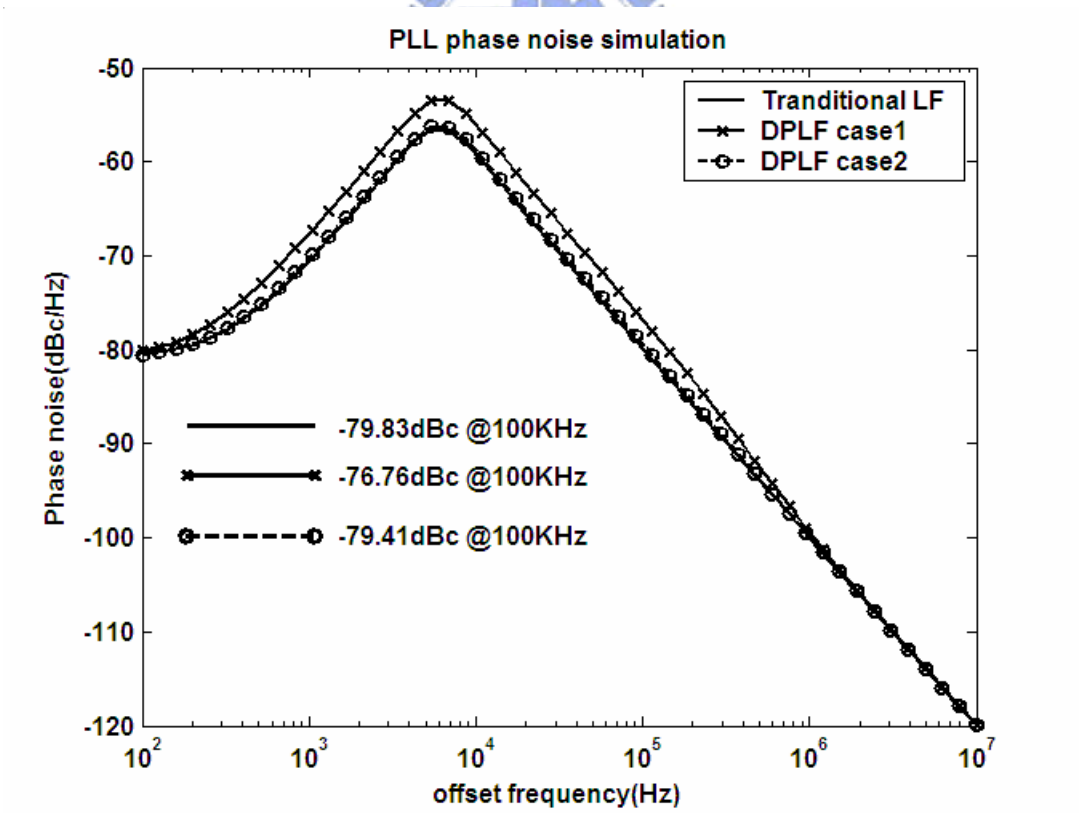


Fig. 3.4. Phase noise simulation results.

By using (3.3) and re-calculating F(s), one can get

$$F(s)=\frac{R_1}{(1+sR_1C_2)}+\frac{1}{sBC_1(1+sR_1C_2)}\frac{A_{err}}{1+\frac{s}{\omega_t}}. \tag{3.4}$$

Equation (3.4) can be reduced to

$$F(s)\approx\frac{R_1\left(s+\frac{A_{err}}{R_1BC_1}\right)}{s(1+sR_1C_2)} \tag{3.5}$$

when $\omega_t >> 1/(R_1C_2)$. When (3.5) is compared to (3.1), it can be expected that the gain error will cause the ratio of capacitance multiplication to be higher than the expected.

With reference to phase noise analysis, the block diagram with relevant noise sources is shown in Fig. 3.3. Here, noise from CP_1, CP_2, the unity-gain buffer and VCO are considered and denoted as $\overline{I_{np1}^2}$, $\overline{I_{np2}^2}$, $\overline{V_{nop}^2}$, and $\overline{V_{nvco}^2}$, respectively. The unity buffer is only modeled by its gain error for the worst case scenario and the second order loop filter is adopted for the purpose of simplification. It should be noted that all noise sources are assumed to be white although this is only an approximate for VCO.

The noise spectral density at the PLL output $S_{\Phi n}(f)$ is represented as

$$S_{\Phi n}(f)=S_{\Phi nvco}(f)+S_{\Phi np}(f)+S_{\Phi nop}(f)=|H_{vco}|^2\overline{V_{nvco}^2}+|H_{cp}|^2\overline{I_{np1}^2}+|H_{op}|^2\overline{V_{nop}^2} \tag{3.6}$$

where $S_{\Phi nvco}(f)$, $S_{\Phi np}(f)$, and $S_{\Phi nop}(f)$ are the noise spectral densities of VCO, both charge-pump currents, and the unity gain buffer, respectively. The definition of $\overline{V_{nvco}^2}$ can be found in [11]. From the PLL linear model shown in Fig. 3.3, the transfer functions are calculated as follows:

$$H_{cp}=\frac{2\pi NK_vF_1(s)}{sN+2\pi K_dF_1(s)K_v}, \tag{3.7}$$

$$H_{op}=\frac{2\pi NK_v}{sN+2\pi K_dF(s)K_v}\frac{A_{err}}{1+sR_1C_2}, \tag{3.8}$$

and $H_{vco} = \dfrac{2\pi N K_v}{sN + 2\pi K_d F(s) K_v}$. (3.9)

Where K_v is the gain of the VCO in Hertz/Volts, $K_d=I_{p1}/2\pi$ is the gain of the PFD and CP, F(s) is the transfer function of loop filter of (3.5), and N is value of the divider. $F_1(s)$ is the noise transfer function from CP_1 and CP_2 and can be found using

$$F_1(s) = \frac{R_1\left(s + \dfrac{A_{err}}{R_1\sqrt{B}C_1}\right)}{s(1 + sR_1C_2)}. \quad (3.10)$$

From (3.10) it can be seen that the noise transfer function is slightly different to the signal transfer function (3.5). The capacitor multiplication factor in noise analysis is $\sqrt{B}$ not B. In addition, by comparing (3.8) and (3.9), the noise from the unity gain buffer and from the VCO have the same contribution when frequency is below $1/R_1C_2$. The PLL phase noise simulation results are shown in Fig. 3.4, where the solid line uses the traditional loop filter presented in Fig. 3.2(b). The solid line with a cross mark denoted by DPLF case1 uses the dual-path loop filter seen in Fig. 3.2(a) with $\overline{V_{nop}^2} = \overline{V_{nvco}^2}$. Finally, the dashed line with a circle mark denote by DPLF case 2 uses the dual-path loop filter shown in Fig. 3.2(a) with $\overline{V_{nop}^2} = 0.1 \times \overline{V_{nvco}^2}$. Here, the VCO phase noise is assumed to be -100dBc at 1MHz offset frequency. From Fig. 3.4, it can be seen that the phase noise of solid line, solid line with a cross mark and dashed line with a circle mark at the offset frequency of 100 kHz are -79.83 dBc, -76.76 dBc, and -79.41 dBc, respectively. The phase noise is degraded by 3.07 dB at the 100 kHz offset frequency if unity gain buffer noise is the same as the VCO noise, while the phase noise is only degraded by 0.42 dB if the unity gain buffer noise is one-order less than the VCO noise. Therefore, it is necessary to design a unity gain buffer with a low phase noise.

In addition to the filter transfer function and the phase noise, the offset of OP-AMP is also considered. If some offsets appear, they are the result of a voltage difference between V_c and V_b. But CP_2 will automatically adjust V_b to compensate for the voltage difference between V_b and V_c.

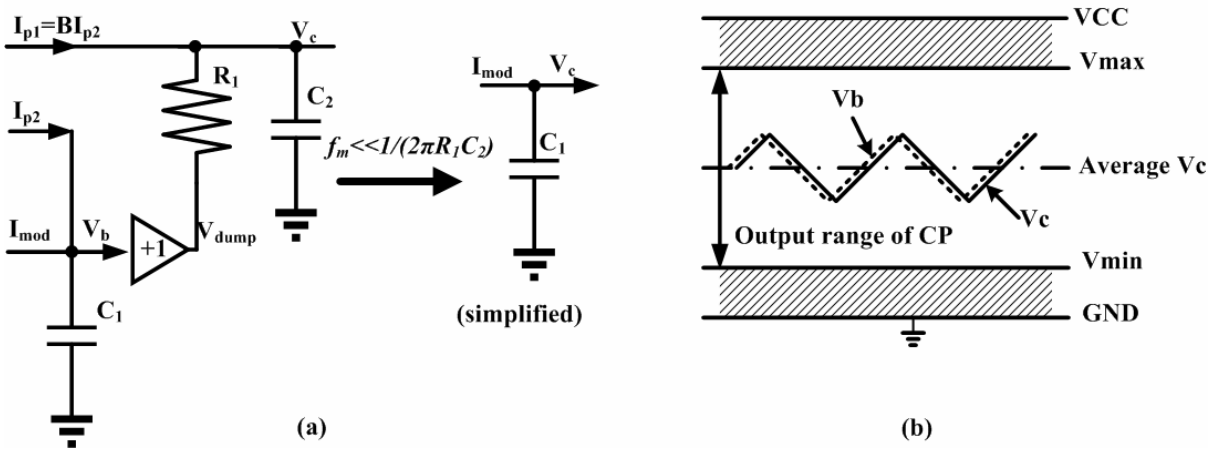


Fig. 3.5. (a) Proposed technique of triangular modulation (b) Waveform of Vc and Vb.

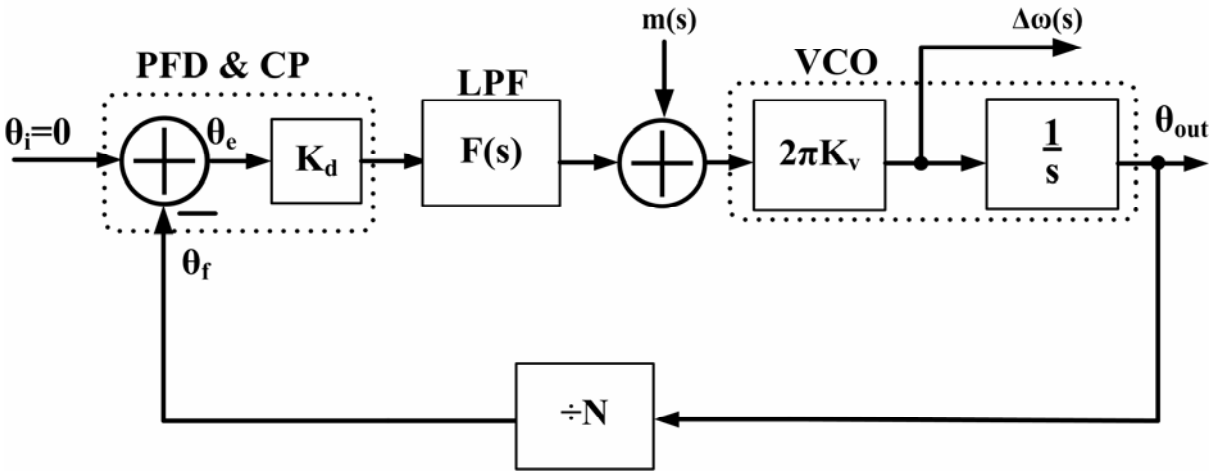


Fig. 3.6. Linear model of PLL with frequency modulation.

3.2.3 Analysis of Modulation

The realization of a triangular waveform for controlling voltage is illustrated in Fig. 3.5(a). The current I_{mod} from CP_3, which is controlled by an external pulse, is also applied to C_1. By superposition, the transfer function between I_{mod} and V_c can be expressed as

$$\frac{V_c}{I_{\mathrm{mod}}} = \frac{1}{sC_1\left(1+sR_1C_2\right)}. \tag{3.11}$$

By assuming that the modulation frequency is much smaller than the pole, $f_m << 1/(2\pi R_1C_2)$, (3.11) can be further simplified as

$$\frac{V_c}{I_{\mathrm{mod}}} \approx \frac{1}{sC_1}. \tag{3.12}$$

Then the controlled voltage is integrated from the modulation current. The requested triangular signal at the input node of the VCO is created as a square wave, I_{mod}. According to (3.12), the triangular voltage of modulation is easily obtained by just adding an extra charge-pump circuit without an additional passive component. The particular third charge pump circuit combined with the dual-path loop filter can easily generate the triangular modulation and considerably reduces the chip area. Here C_1 plays an important role that it not only acts as the loop filter in PLL as indicated in [18] but also serves the integration function in triangular wave generation. Unlike [3], the proposed model does not require the parameters C_1, C_2, R_1 and R_2 to meet the special theory requirement $R_1C_1=R_2C_2$, nor does it require a large capacitor. Therefore, the clear advantage of the proposed technique is its flexibility and fully integrated nature.

The waveforms of V_c and V_b are shown in Fig. 3.5(b), where V_b is the voltage at the input of the buffer and V_b is almost the equivalent of V_c with only a slightly phase leading. The output range of the charge pump is from V_{min} to V_{max} which are the ground voltage plus a saturation voltage and the supply voltage minus a saturation voltage, respectively as shown in Fig. 3.5(b). This suggests that CP_3 has enough headroom to generate the triangular wave. Therefore, the output swing deduced from the three charge pumps can be safely operated without distortion. In [16] with floating capacitance, the output voltage of CP_2 seems to be equal to zero in steady state. Thus, extra bias circuit might be needed.

The choice of loop bandwidth is essential to achieve a uniform spread. The modulated behaviors in the closed loop are analyzed through the linear model as shown in Fig. 3.6. The modulated voltage denoted as m(t) is applied to the input of the VCO. The instantaneous output frequency is $\omega_{out}=\omega_o+\Delta\omega(t)$, where ω_o is the un-modulated carrier frequency and $\Delta\omega$ is the frequency deviation. The transfer function from m(s) to $\Delta\omega(s)$ is obtained as

$$\frac{\Delta\omega(s)}{m(s)}=\frac{2\pi K_v s}{s+\frac{2\pi K_d F(s) K_v}{N}}. \tag{3.13}$$

From (3.1), F(s) can be rewritten as

$$F(s)=\frac{R_1\left(s+\frac{1}{R_1 B C_1}\right)}{s} \tag{3.14}$$

when $f_m << 1/(2\pi R_1 C_2)$. By substituting (3.14) into (3.13), the following results:

$$\frac{\Delta\omega(s)}{m(s)}=\frac{2\pi K_v s^2}{s^2+\frac{2\pi K_d K_v R_1}{N}s+\frac{2\pi K_d K_v}{N C_1 B}}. \tag{3.15}$$

Actually, its behavior is a high-pass characteristic. As indicated earlier, the loop bandwidth is roughly equal to $K=K_d K_v R_1/N$ around a unity damping constant. (3.15) can be further simplified to

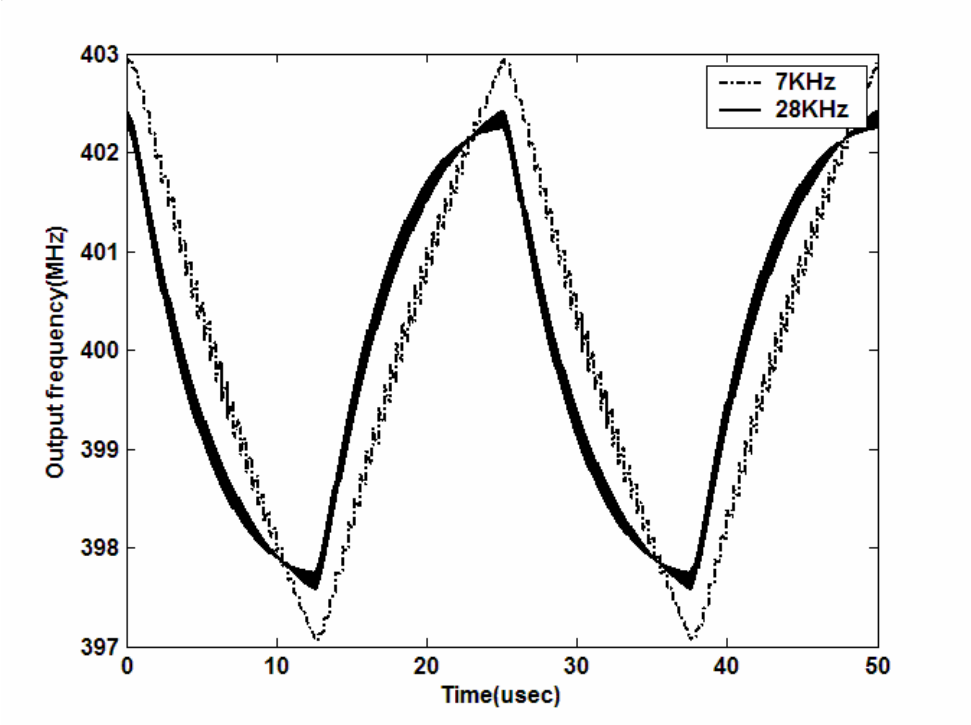
$$\frac{\Delta\omega(s)}{m(s)}\approx 2\pi K_v \tag{3.16}$$

if the modulation frequency is much larger than the loop bandwidth. This means that the frequency deviation is proportional to the input amplitude with a coefficient of $2\pi Kv$. By definition, the feedback phase signal is θ_f:

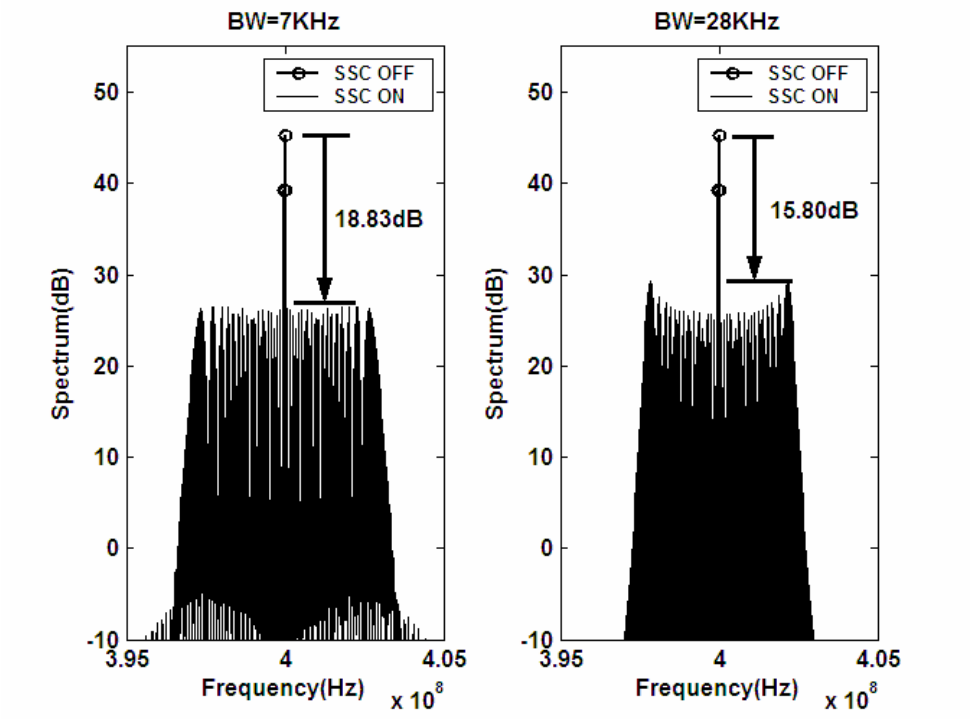
$$\theta_f(t)\equiv\int\frac{\Delta\omega(t)}{N}dt. \tag{3.17}$$

In a steady state, the phase error of the PFD output is $\theta_e=-\theta_f$ with the assumption that the input phase signal is $\theta_i=0$. To satisfy the linear operation, the phase error is limited by the following relationship,

$$|\theta_e(t)|=\left|\int\frac{\Delta\omega(t)}{N}dt\right|\le\theta_{e,\max}, \tag{3.18}$$



(a)



(b)

Fig. 3.7. Simulation results of (a) frequency profile (b) spectra under different loop bandwidth with fm=40 kHz.

where $\theta_{e,max}$ is the limit of the linear range of the PFD. Here $\theta_{e,max}$ equals 2π as a typical phase-frequency detector. The triangle waveform m(t) with a mean of zero can be written as

$$\begin{aligned} m(t) &= 2V_m(2f_m t - 0.5) \quad for \quad 0 \le t < \frac{1}{2f_m} \\ &= 2V_m(1.5 - 2f_m t) \quad for \quad \frac{1}{2f_m} \le t < \frac{1}{f_m} \end{aligned}, \tag{3.19}$$

where V_m is the amplitude and f_m is the frequency. By substituting (3.19) and (3.16) into (3.17), the following is obtained:

$$V_m \le 8\frac{N}{K_v} f_m \tag{3.20}$$

under the constraint of (3.19) with its lower limit of 0 and its upper limit of $1/(4f_m)$. It can be seen that the maximum amplitude of the triangle wave is proportional to the divider value and modulation frequency, and is inversely proportional to the VCO gain. Accordingly, the upper bond of a peak to peak spread ratio δ is found as

$$\delta = \frac{2V_m K_v}{f_o} \le \frac{16Nf_m}{f_o}, \tag{3.21}$$

where f_o is the center frequency of the VCO output. The distortion occurs if the spread ratio exceeds this limit. The upper bond is limited by the divider value and the modulation frequency, and is independent of VCO gain.

The spread ratio can be controlled by adjusting the value of I_{mod}. According to (3.12) and (3.21), the I_{mod} can be determined by using

$$I_{\text{mod}} = \delta \frac{2C_1 f_{\text{m}}}{K_v} f_o . \tag{3.22}$$

(3.22) indicates that the variation in the spread ratio comes from the process variations of K_v, C_1 and I_{mod}. In this work, I_{mod} is about 1.05 uA for a 1.5% spread ratio with K_v=275 MHz/V, f_m=40 kHz, C_1=600 pF, and f_o=400 MHz.

Based on condition (3.12), the loop bandwidth is required to be much less than the modulation in order to achieve linear integration. The effect of the loop bandwidth on the modulation profile is examined as follows. The simulated frequency deviation and suppressed spectra of a 400 MHz output signal by Matlab under different bandwidths are shown in Fig. 3.7(a) and 3.7(b), respectively. In Fig. 3.7(a), the frequency variation becomes nonlinear

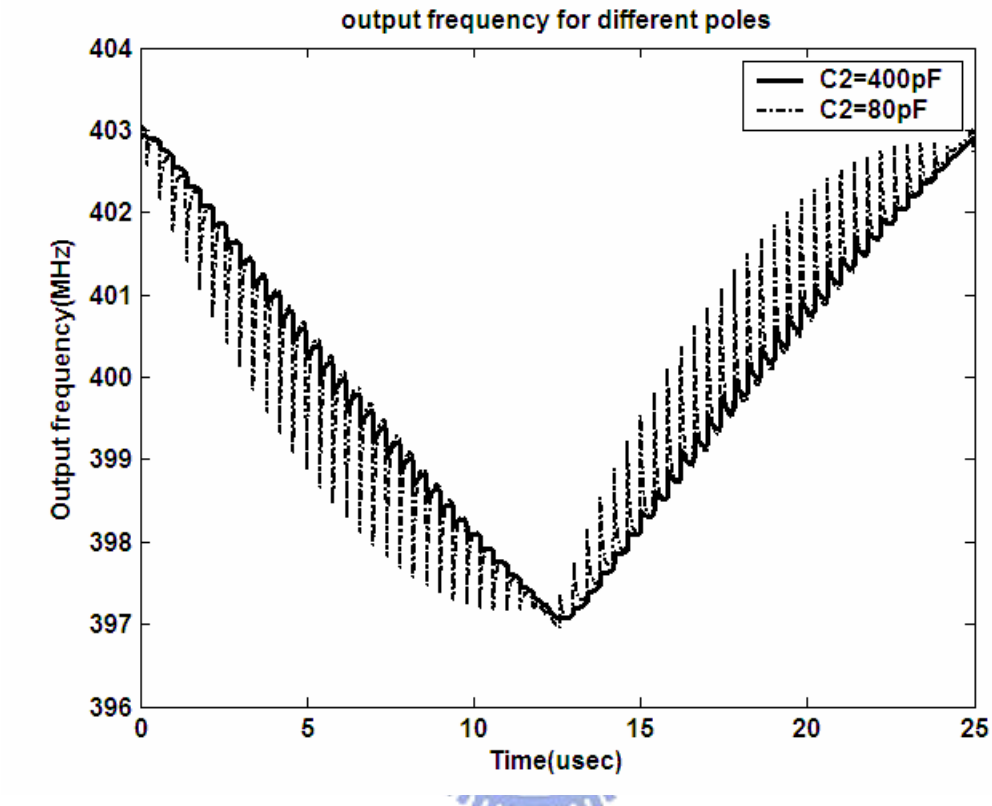


Fig. 3.8. Simulation results of output frequency for different poles.

Table 3.1 The Critical Parameters of the PLL

Reference Frequency	2.5 MHz
Zero Frequency	5.3 kHz
Loop Bandwidth	7 kHz
Pole frequency	398 kHz

(solid line) and smaller as the loop bandwidth is raised toward the modulation frequency. The simulated spread ratio is 1.47% for a 7 kHz loop bandwidth, while it is reduced to 1.21% for a 28 kHz loop bandwidth with f_m=40 kHz. The reason for this can be found in the fact that the PLL acts as a high-passed filter with a corner frequency at the loop bandwidth and the modulated signal is attenuated as the modulation frequency approaches the loop bandwidth. The EMI reductions for 7 kHz and 28 kHz loop bandwidths are 18.83 dB and 15.80 dB, respectively. The spectra level for the latter is 3.03 dB worse than that for the former bandwidth. It is suggested that the loop bandwidth should be at least five times less than modulation frequency.

3.2.4 Spurious Modulation

In addition to the requirement of a loop bandwidth, the spurious effect is also taken into account. The spurious effect is mainly caused by the mismatch of the pumping currents and the switches in the charge pump circuits. As modulated in a SSCG, the phase error of the PFD output is periodically perturbed by the triangular profile. As a result of the loop bandwidth being small, the modulation signal is not cancelled. The high frequency components of the phase error may pass through the loop filter and deteriorate the jitter This spurious modulation can be suppressed by appropriately adding a pole, i.e., $1/(R_1C_2)$. The variations in output frequency under the influence of different poles are illustrated in Fig. 3.8. The solid and doted lines are with 0.4 MHz and 2 MHz poles, respectively. The corresponding values of C_2 are 400 pF and 80 pF which both have R_1=1 kΩ. It is clearly seen that except for the sweep, there exist instantaneous frequency spikes. The higher the frequency of the pole has, the greater the variation of the spike has. These undesired frequency spikes result in a poor triangular modulation profile and generate extra jitter. Accordingly, the pole is traded off between the linear modulation and spurious rejection. In this work, the pole is chosen as 0.4 MHz. Extra poles composed of R_3 and C_3 are employed to further lower spurious modulation. Here, R_3=10 kΩ and C_3=10 pF are adopted and the pole is 1.59 MHz.

It is noted that there are many trade-offs in frequency setting involving direct VCO modulation. First of all, the reference clock of the PFD is chosen as the guidepost, which is the highest one in the loop and is far from the loop bandwidth. Then, the zero BR_1C_1 is traded

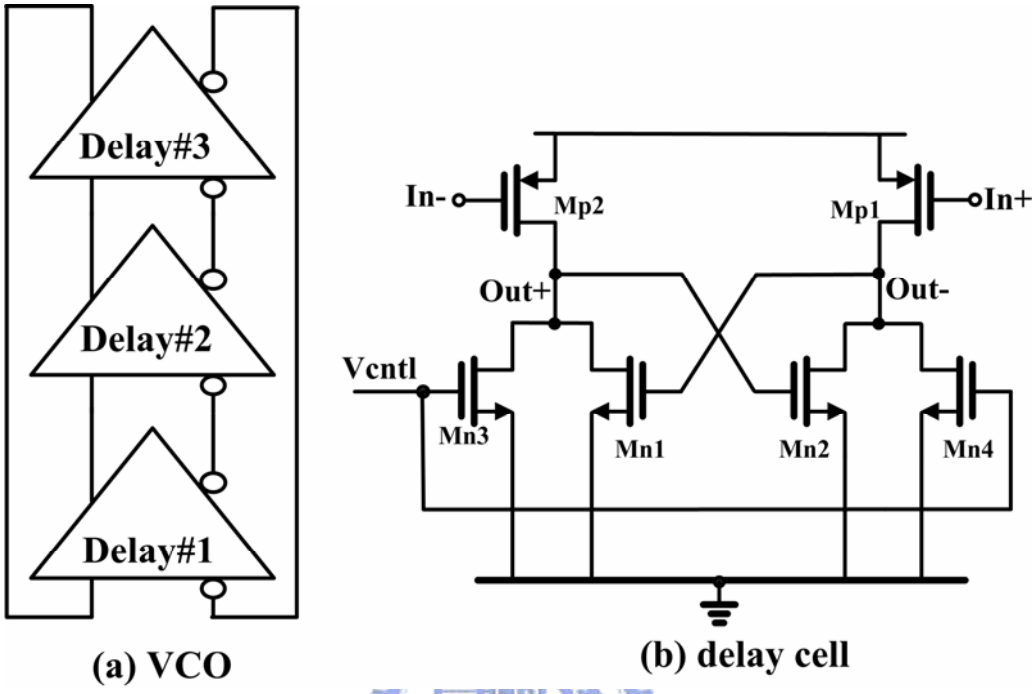
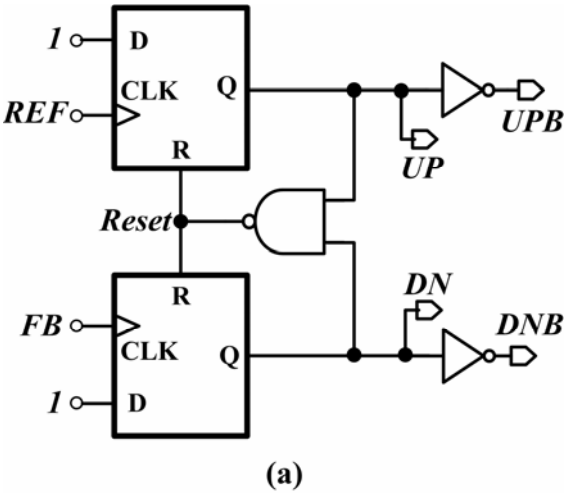


Fig. 3.9. (a) VCO and (b) Delay cell in VCO.



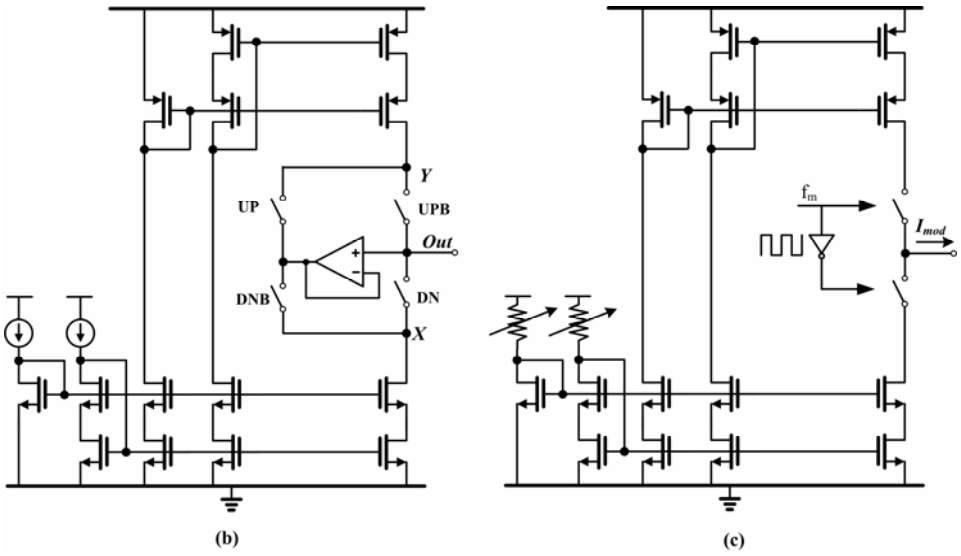


Fig. 3.10. (a) PFD circuit , (b) CP1 and CP2 circuits, and (c) CP3 circuit.

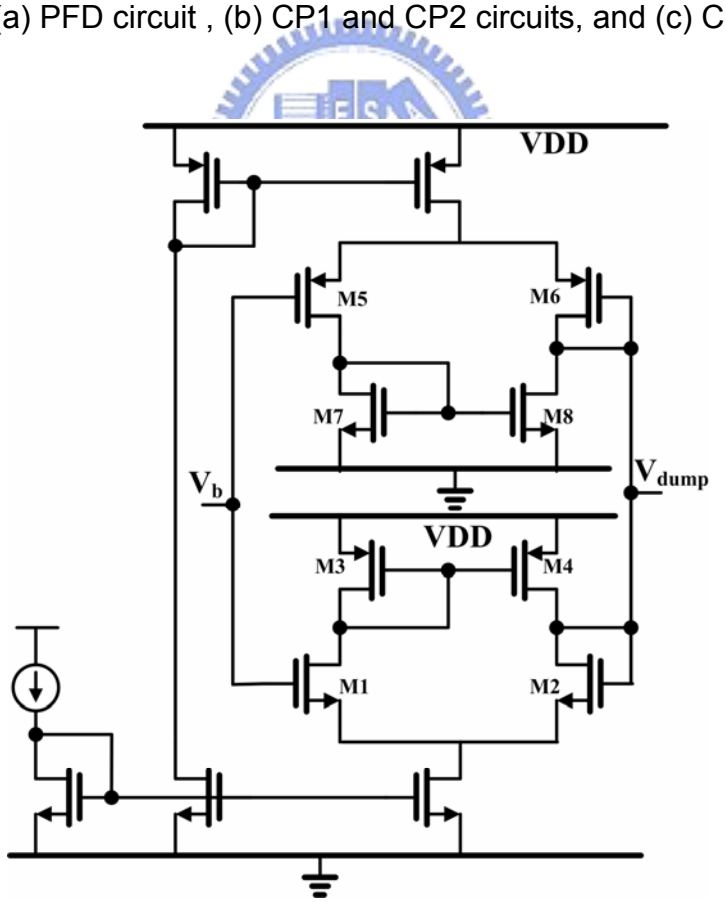


Fig. 3.11. Unity gain buffer circuit used in dual-path loop filter.

off between capacitance area and damping constant. The loop bandwidth is traded off between stability and modulation. Modulation is set higher than the loop bandwidth. The pole is then traded off between linear integration and modulation spurious rejection. The critical parameters of the PLL are listed in Table 3.1.

3.3 Circuit Descriptions

The circuits used in this work are briefly described next. The wide band VCO [10], which consists of the three stages of differential delay cells, is shown in Fig. 3.9(a). The schematic of each delay cell is shown in Fig. 3.9(b). A cross-coupled connection is employed to obtain full swing and sharp output waveform to reduce the jitter. A conventional voltage to current converter and tail current source are omitted for low voltage applications and for lower flicker noise up-conversion [10]. The PFD and charge-pumps $CP_{1(2)}$ and CP_3 are shown in Fig. 3.10(a), 3.10(b) and 3.10(c), respectively. The cascoded current sources with a wide-swing bias circuit in Fig. 3.10(b) are employed to achieve good immunity against the power supply noise. The controlling signals of UP, UPB, DN and DNB switches are directly fed from the outputs of PFD represented in Fig. 3.10(a). A unity-gain buffer is used to clamp the terminal voltages of the current sources during the zero-current pumping period. In this way, voltage glitches on the loop filter resulting from charge sharing can be eliminated [21]. The currents I_{p1} and I_{p2} of CP_1 and CP_2 are 25 uA and 0.5 uA, respectively. The current I_{p3} is adjusted by using an external resistor to match the various spread ratios.

The unity gain buffer with rail-to-rail input and output used in the dual-path loop filter is shown in Fig. 3.11. The driving current is designed to be twice that of I_{p1} to provide enough driving capacity. The simple one-stage design is adopted for the low phase noise requirement discussed in part B of section II. In the mean time, the long channel devices are used for M1 through M8. The GBW is designed much larger than the poles of $1/R_3C_3$ and $1/R_1C_2$ to maintain linear modulation. The load of the buffer comprises a resistor series with a capacitor; therefore, no driving stage is needed.

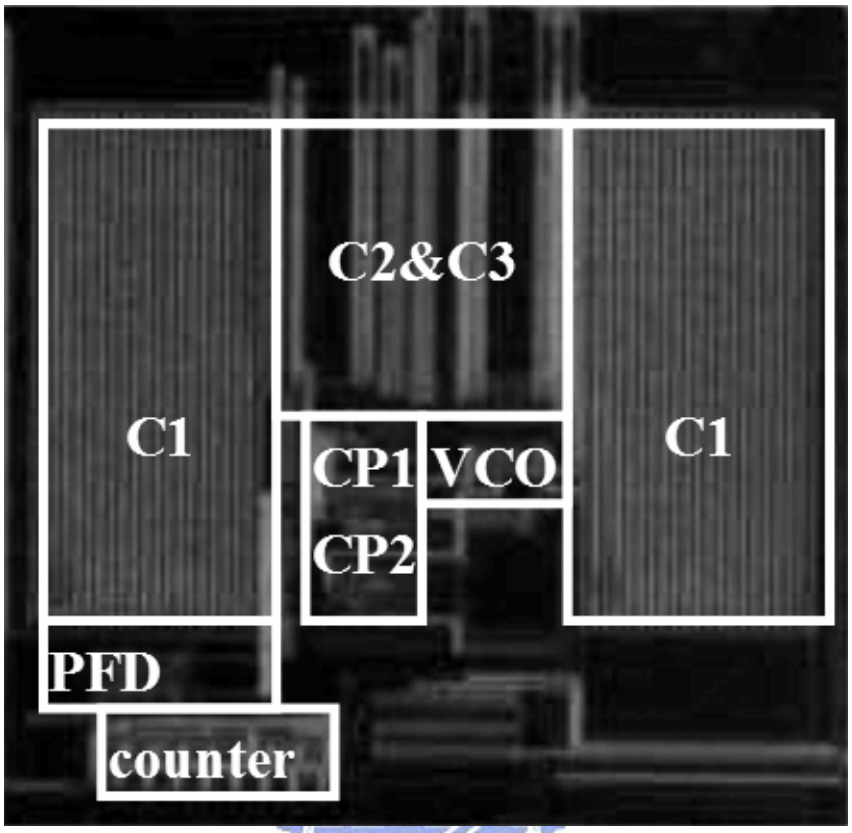


Fig. 3.12. Die photograph of the proposed SSCG.

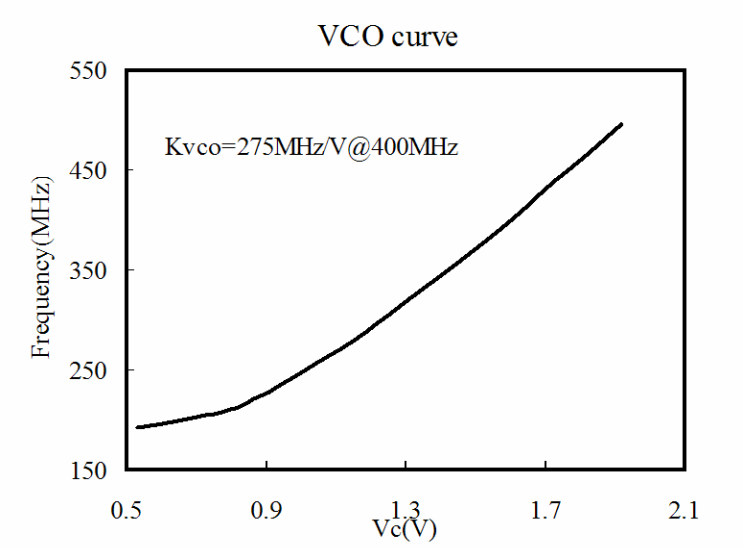
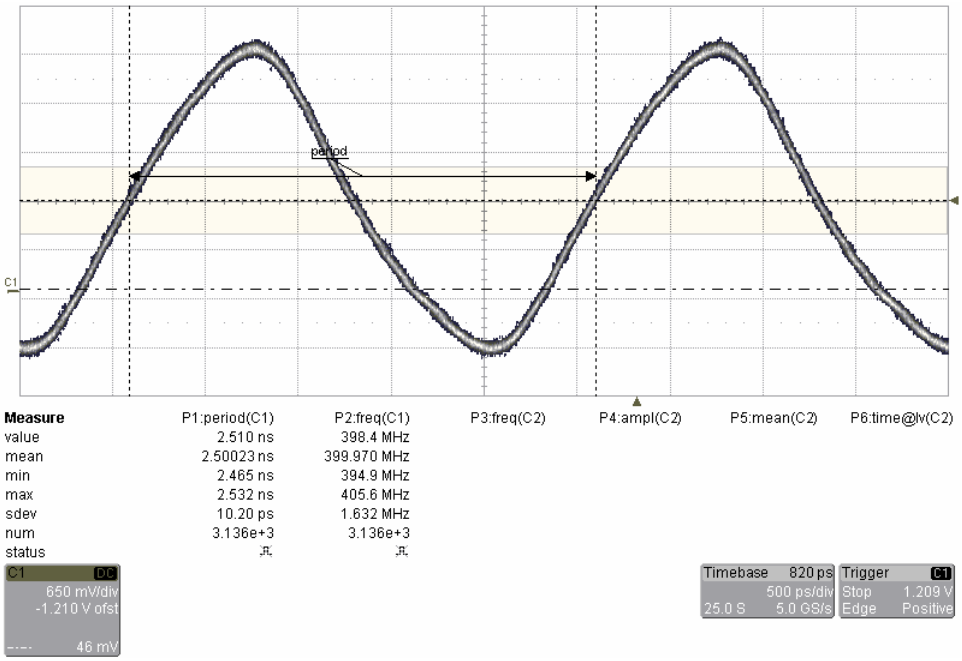
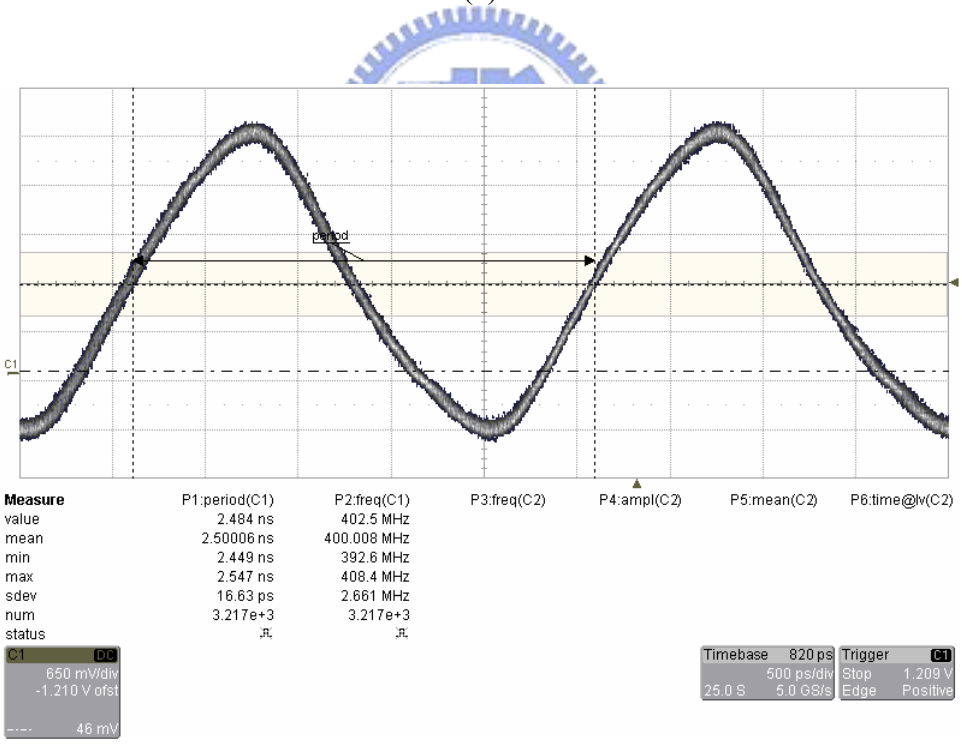


Fig. 3.13. Measured VCO frequency tuning curve.

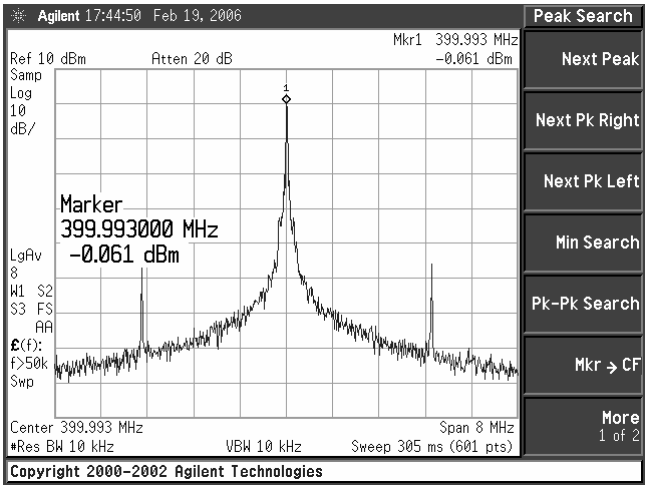


(a)

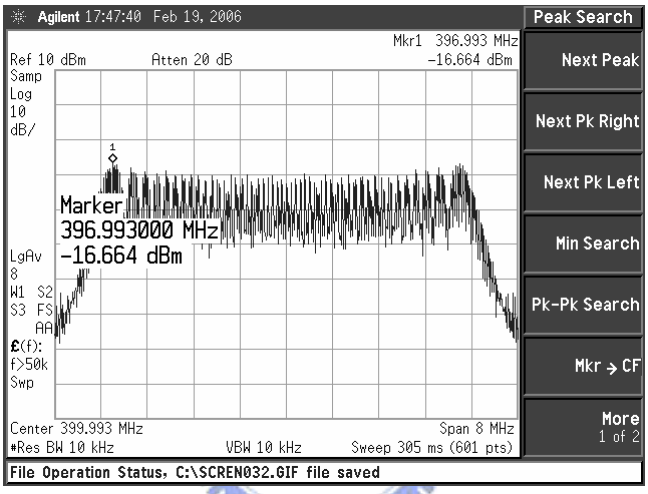


(b)

Fig. 3.14. Measured jitter of SSCG output at 400MHz when (a) SSC off (b) SSC on of 1.5% spread ratio.



(a)



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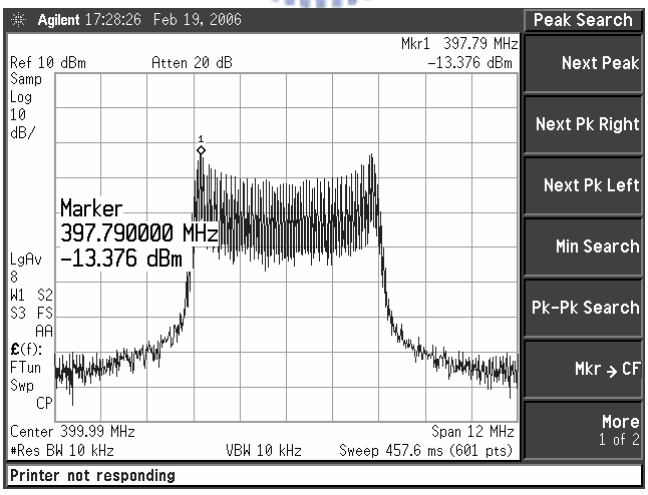


(c)

Fig. 3.15. Measured spectra of the 400 MHz output signal (a) without modulation, (b) with 1.5% center-spread and 7 kHz bandwidth, and (c) with center-spread 1.5% and 28 kHz bandwidth.

Table 3.2 Performance Summaries and Comparison With Previous Works

	[8]	[7]	[14]	[3]	[16]	[4]	This work	Unit
Modulation method	ΔΣ	PI	PI	VCO	VCO	VCO	VCO	N/A
Modulation profile	Triangle	Triangle	Non-linear	Triangle	Triangle	Triangle	Triangle	N/A
EMI reduction	13.9	10.6	8.02	N/A	16	11.2	16.6	dB
Jitter (SSC OFF)	70	N/A	N/A	N/A	62	55.6	67	ps-pp
Jitter (SSC ON)	197	N/A	N/A	N/A	N/A	N/A	98	ps-pp
Modulation bandwidth	+0.12/ -0.12	+1.17/ -1.17	+0/ -0.50	+1.25/ -1.25	+0.75/ -0.75	+5/ -5	+0.75/ -0.75	%
Frequency	134	14.3	25	266	320	65	400	MHz
Technology	0.2	0.6	0.15	0.35	0.35	0.3	0.35	μm
Total capacitor	N/A	N/A	N/A	352.47	78.959	N/A	1.01	nF
Capacitor multiplication ratio	N/A	N/A	N/A	N/A	4	N/A	50	N/A
Power	N/A	99	N/A	300	150	N/A	27.5	mW

3.4 Measurement Results

The proposed SSCG has been fabricated using TSMC 0.35 μm single-poly quadruple-metal CMOS process. The die photograph with its area of 0.82×0.80 mm^2 is shown in Fig. 3.12. The tuning sensitivity of the VCO is shown in Fig. 3.13 with a gain of 275 MHz/V at 400 MHz output. The VCO reveals a good linear voltage to frequency transfer curve and has a maximum frequency of more than 500 MHz. The measured jitter with the SSC off and on is shown in Fig. 3.14(a) and 3.14(b), respectively. The peak-to-peak period jitter is 67 ps with the SSC off and 98 ps with it on, and with a 1.5% spread ratio. The measured spectra of the 400 MHz output signals without and with a center-spread of 1.5% are shown in Fig. 3.15(a) and 3.15(b), respectively. The peak amplitude reduction is 16.603 dB, which is only 2.227 dB lower than the simulation results, as shown in Fig. 3.7(b). For comparison, the measured result with the larger loop bandwidth of 28 kHz is shown in Fig. 3.15(c). The reduced peak amplitude is 13.315 dB, which is 3.288 dB deterioration compared with Fig. 3.15(b). Thus, the effect of a higher loop bandwidth is clearly verified.

Table 3.2 summarizes the performances of the proposed SSCG and compares them with the others. The power consumption is only 27.5 mW and this is much lower than for the previous models in [3] and [16] with a similar frequency due to the benefits of full integration. The total capacitor used here (C_1+C_2+C_3) is only 1.01 nF while it is 352.47 nF for the one in [3] and 78.959 nF for the one in [16]. Hence, the advantage of capacitor multiplication is clearly evident. The added jitter is in the proposed SSCG is only 31 ps while it is 127 ps in [8] due to the larger sigma-delta noise.

3.5 Summary

In this chapter, a new 400 MHz SSCG which adopts a direct VCO modulation is presented. By using a dual-path loop filter, the capacitance of the low frequency loop filter is so significantly reduced such that full integration becomes possible. At the same time, a triangular modulation of spectral spread is easily obtained by the appropriate inclusion of

both an extra charge-pump circuit and an isolated buffer in the loop filter. The determination of zero, loop bandwidth, modulation frequency, pole, and comparison clock are carefully studied. The chip is fabricated using a 0.35 μm standard CMOS process. The measurement results are mostly as predicted.

CHAPTER 4

A High Performance Spread Spectrum Clock Generator Using Two-Point Modulation Scheme

A low jitter spread spectrum clock generator (SSCG) using two-point ΔΣ modulation is presented in this thesis. Both the divider ratio and the voltage controlled oscillator are varied. This technique can enhance modulation bandwidth in order to reduce electromagnetic interference (EMI). A second order ΔΣ modulator is utilized simultaneously to reduce the required area and power consumption. Both VCO phase noise and quantization noise of the modulator are carefully examined through developed Matlab models before the loop bandwidth is selected. The simulation time can be dramatically reduced. The effects of any gain mismatch are also analyzed. In addition, the proposed two-path loop filter and DA converter for VCO modulation are accommodated within an attractive structure. The result is total integration and low reference spurious. The proposed SSCG has been fabricated using 0.35 μm CMOS process. A 400 MHz clock with center spread ratios of 1.25% and 2.5% are verified. The latter ratio achieved the peak EMI reduction of 19.73 dB .The chip area is 0.90×0.89 mm^2.

4.1 Introduction

Spread-spectrum clocking techniques have been widely employed in high-speed clocks to reduce EMI levels [2]-[5], [7]-[9], [13]-[17], [22]-[28], [38]. Among those techniques, the fractional-N phase-locked loop (PLL) with a ΔΣ modulator is generally adopted [9], [13], [22]-[24]. A special triangle waveform is applied to the modulator to vary the fractional part of the divider to spread slightly the spectrum via frequency modulation. As regards to modulation in a PLL, the allocation of three frequencies of modulation, loop bandwidth, and phase comparison are very crucial to achieving low jitter and good EMI operation. The loop bandwidth needs to be large enough to react sufficiently to the triangular profile. Otherwise,

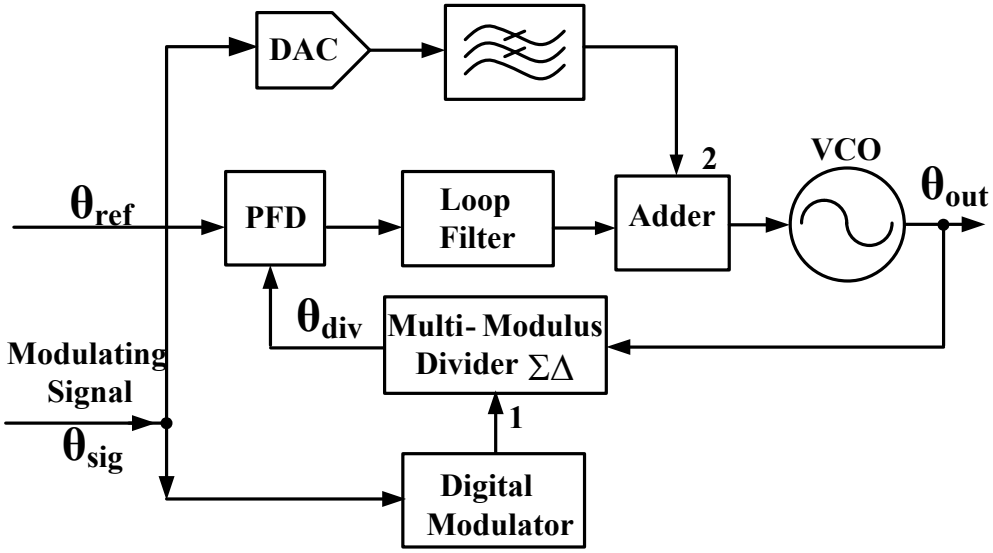


Fig. 4.1. Block Diagram of two-point modulation PLL.

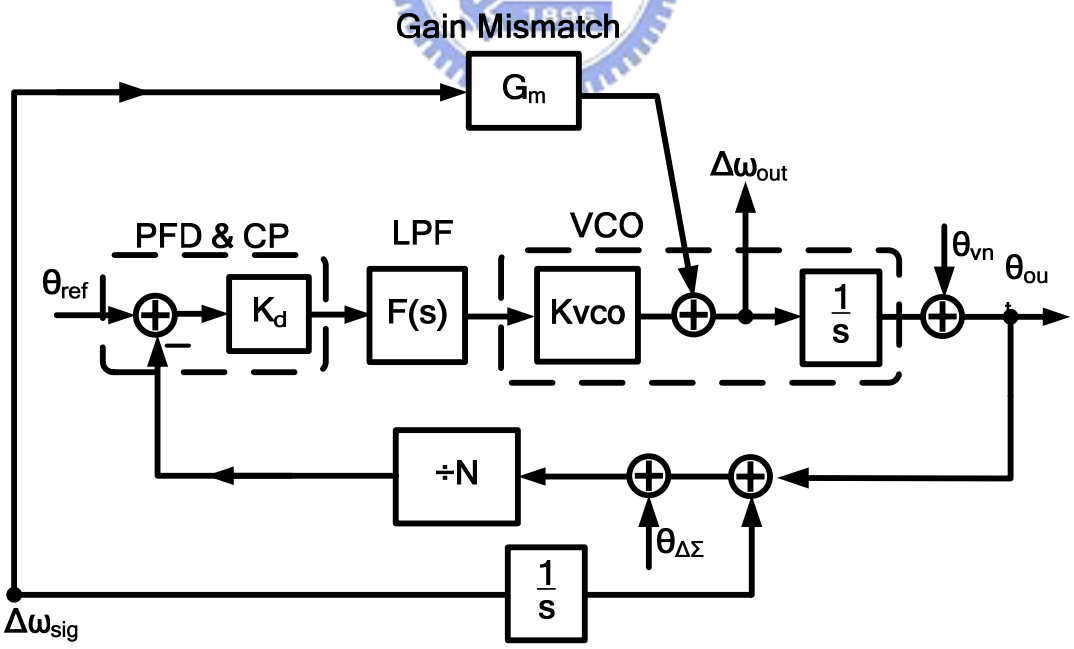


Fig. 4.2. Linear model of TP-SSCG.

the modulation profile is distorted and EMI suppression is compromised [24]-[26]. In contrast, much less than the comparison frequency is normally required to obtain low jitter by virtue of the low-pass nature of PLL. In-band fractional spur is suppressed by ΔΣ spreading. To obtain sufficient suppression in the case of a large bandwidth, a third-order ΔΣ modulator is normally employed. However, the power consumption and area associated with this type of modulator are a disadvantage. Therefore, an alternative method with two-point modulation [25]-[26] is proposed. Both the ΔΣ modulator and the VCO are modulated, so that the loop bandwidth can be reduced significantly with respect to the comparison frequency. This results in two advantages. First, a linear saw-tooth waveform is retained and good EMI suppression is obtained with the effective all-pass nature of modulation bandwidth. Furthermore, only a second order ΔΣ modulator is required, which reduces both the required power and chip area.

The simulation time is also a concern when implementing SSCGs due to low modulation frequency and high output frequency. In order to obtain the correct EMI levels, the output spectrum obtained through Fourier transform needs large data and therefore requires the long simulation time. Here, an efficient model built in Matlab [33] is developed to speed up the simulation time tremendously.

The block diagram of a two-point modulation with an input of -1 at the multi-modulus divider and an input of -2 at the VCO is shown in Fig. 4.1. It has possible applications in DC-FM frequency generators [25]-[26]. Its transfer function displays all-pass behavior if the two modulation paths are matched [29]. Usually, a high resolution digital-to-analog converter (DAC) is needed to overcome the highly sensitive VCO gain. An adder is also required to combine the two path signals which can lead to the disadvantages of high power consumption and large area. In this study, a simple architecture is utilized to achieve a fine VCO modulation and a dual-path loop filter is involved for total integration. The interrelation between modulator order and loop bandwidth are studied, and the phase noise which originated from the ΔΣ modulator and VCO are closely examined.

4.2 Jitter Analysis

4.2.1 System Modeling

The dynamics of the proposed architecture are analyzed using the linear model shown in Fig. 4.2. Where K_d is gain of the phase-frequency detector (PFD) and charge pump, F(s) is the transfer function of the loop filter, K_{vco} is the VCO conversion gain, N is the divider value, and G_m is the gain factor which accounts for the mismatch between the two modulation points. The delay mismatch is disregarded here due to the proposed DAC and will be discussed in Section III. Two noise sources are taken into account. One is the modulator quantization noise $\theta_{\Delta\Sigma}$ and the other is VCO phase noise θ_{vn}. Reference noise is neglected due to the simplicity.

The frequency relationship is derived instead of the phase response chosen in [29] due to the nature of frequency modulation of SSCGs. $\Delta\omega_{out}$ is the frequency deviation of VCO output signal f_{out}. $\Delta\omega_{sig}$ is the frequency deviation of the input modulation signal f_{sig}. The closed-loop transfer function can be derived as

$$\frac{\Delta\omega_{out}}{\Delta\omega_{sig}} = T(s) + \left(1 - T(s)\right) \times G_m \tag{4.1}$$

$$\text{with} \quad T(s) = \frac{K_{vco}K_d F(s)}{Ns + K_{vco}K_d F(s)}. \tag{4.2}$$

The first term in the right-hand side of (4.1) appears as a low pass and the second term appears as a high pass F(s) in (4.3) which, as usual, is a second-order loop filter:

$$F(s) = \frac{R_1\left(s + \omega_{zero}\right)}{s\left(1 + \dfrac{s}{\omega_{pole}}\right)}, \tag{4.3}$$

where R_1 is a resistor in the loop filter, ω_{zero} and ω_{pole} are the zero and pole of the loop filter, respectively..

From (4.1), $\Delta\omega_{out}$ is equal to $\Delta\omega_{sig}$ if G_m=1. In other words, if there are no mismatches between the two modulation points, the bandwidth is very wide and gives rise to low distortion in the output signal.

Table 4.1 Simulation Parameters

	One point	Two point
Input Frequency f_{bk}	14.31818 MHz	14.31818 MHz
Output Frequency	400 MHz	400 MHz
Spread Ratio	2.5%	2.5%
Modulation Freq.	40 kHz	40 kHz
Modulator	third-order MASH	second-order MASH
Loop Bandwidth	120/400 kHz	120/400 kHz
VCO Gain	200 MHz/V	200 MHz/V
Loop filter	third-order	second-order
K_d	9 μ/2π / 35 μ/2π	9 μ/2π / 30 μ/2π
ω_{zero}	8.3 kHz	8.3 kHz
ω_{pole}	332 kHz	332 kHz
Third pole frequency	4.55 MHz	N/A

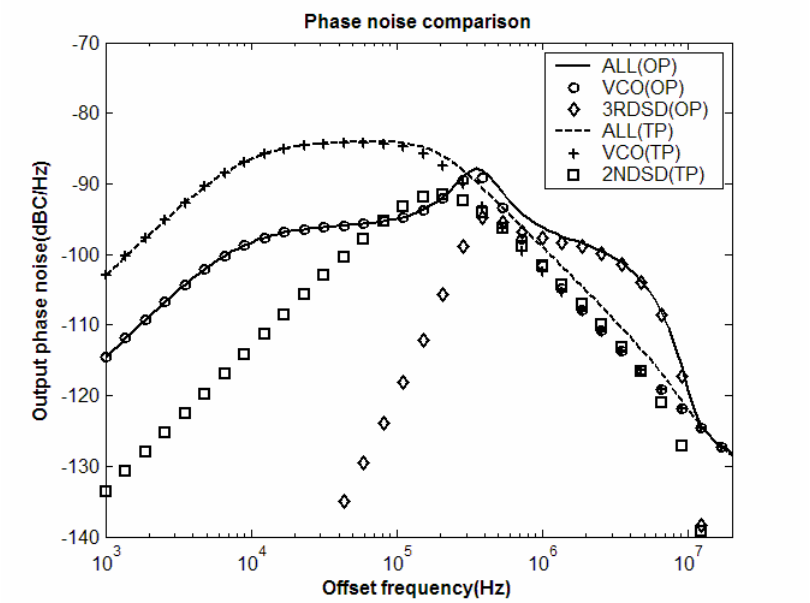


Fig. 4.3. Phase noise simulation for different PLL loop bandwidths.

4.2.2 Consideration of Phase Noise

Two important issues need to be taken into account regarding modulator design. One is the order of the modulator and the other is the loop bandwidth of the PLL. To understand the interrelation, the output phase noise from the noise sources of the modulator and the VCO as illustrated in Fig. 4.2 are investigated. The power spectral density (PSD) of phase noise $S_{\theta out}(f)$ is expressed as

$$S_{\theta out}(f) = S_{\theta vco}(f) + S_{\theta \Delta\Sigma}(f), \tag{4.4}$$

where $S_{\theta vco}(f)$ and $S_{\theta \Delta\Sigma}(f)$ are the PSDs of theVCO and the ΔΣ modulator, respectively. $S_{\theta \Delta\Sigma}(f)$ [32] can be determined as follows

$$S_{\theta \Delta\Sigma}(f) = \frac{(2\pi)^2}{12 f_{div}} \left[2\sin\left(\frac{\pi f}{f_{div}} \right) \right]^{2(m-1)} \left| T(s)_{s=j2\pi f} \right|^2, \tag{4.5}$$

where m is the order of the modulator and f_{div} is the clock frequency of the modulator which is equal to the phase comparison frequency. $S_{\theta vco}(f)$ can be easily derived as

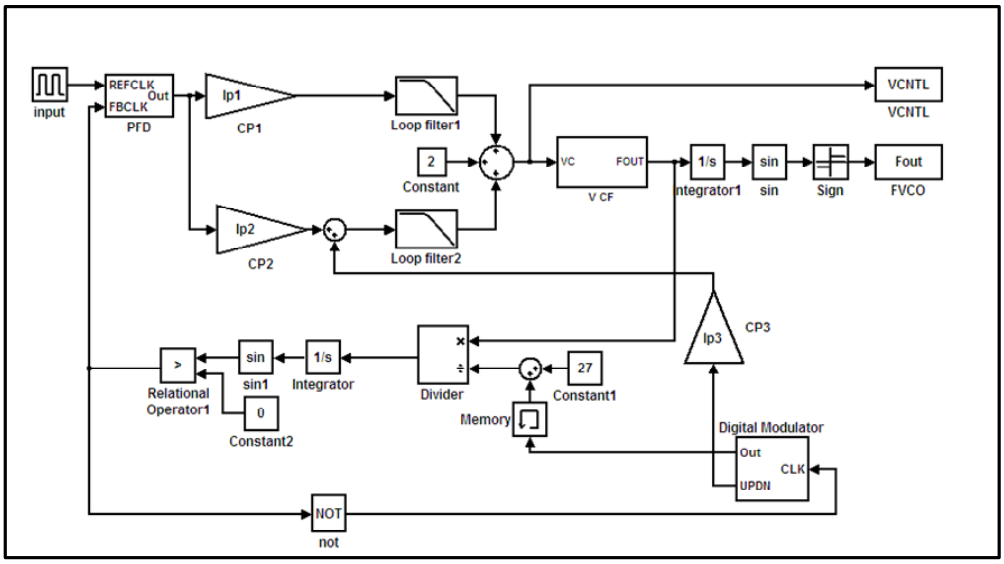
$$S_{\theta vco}(f) = S_{\theta vn} \cdot \left| 1 - T(s)_{s=j2\pi f} \right|^2, \tag{4.6}$$

where $S_{\theta vn}$ is the stand alone VCO phase noise.

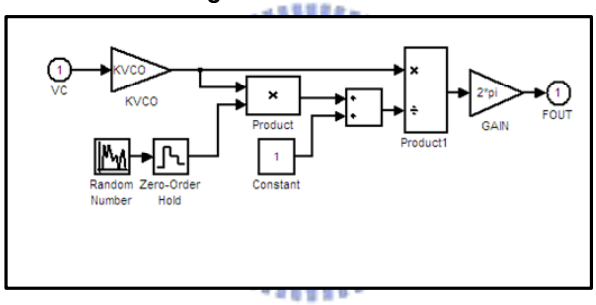
From (4.5), it can be seen that the output phase noise caused by the ΔΣ modulator increased inside the PLL bandwidth with the shape of $f^{2(m-1)}$ if $f/f_{div} << 1$ and decreased outside that bandwidth. In general, the loop bandwidth is selected to be much less than f_{div} to avoid any spurious reference due to the mismatch in the charge pump [31]. Same noise level

is achieved by using a second-order modulator m=2 instead of a third-order m=3 if the bandwidth is reduced by10 times. However, a narrow bandwidth causes a distorted profile and a degraded EMI. Due to the all-pass nature of a two-point modulation, the modulation profile was retained without distortion. Hence, in this design, a second-order ΔΣ modulator was chosen so that both area and power could be reduced.

The PSDs for a conventional one-point (OP) and two-point modulation (TP) in a non-spread spectrum mode are illustrated in Fig. 4.3. Only the VCO and modulator quantization noise have been taken into account. The VCO phase noise measured approximately -100 dBc/Hz at an offset frequency of 1 MHz with a f^{-2} shape. Other simulation parameters are listed in Table 4.1. Two different cases with loop bandwidths of 120 and 400 kHz were studied. $\omega_{pole}=2\pi\times332$ kHz and $\omega_{zero}=2\pi\times8.3$ kHz are the same for both architectures. A third pole of 4.55 MHz was needed for the one-point SSCG to further filter the quantization noise of the third-order modulator. The pole and zero frequencies were chosen to achieve a good phase margin. K_d was adjusted to achieve the desired loop bandwidth. The center was set at 400 MHz, the spread ratio was 2.5%, and the modulation frequency was set at 40 kHz. The solid and dashed lines represent the total phase noise for a one-point with a 400 kHz loop bandwidth and a two-point with a 120 kHz loop bandwidth, respectively. The contributions from the VCO are denoted by a circle and a cross in different cases. The phase noise from the ΔΣ modulator is denoted by a diamond and square. The rms phase jitter can be obtained by integration of (4.4) for a dedicated bandwidth. The rms phase jitter integrated from 1 kHz to 400 MHz is 13.4 ps and 14.3 ps for OP-SSCG and TP-SSCG, respectively. The proposed TP-SSCG with a second order ΔΣ modulator has a jitter performance slightly greater than those in the OP-SSCG with a third order ΔΣ modulator. The advantages of the proposed option can be summarized as follows. First, a lower order ΔΣ modulator can be used to reduce power consumption. Second, a lower order loop filter was used to save chip area. Third, the linear modulation profile and jitter can be optimized simultaneously. Because the two-point case is VCO dominated, the jitter can be further reduced by minimizing the VCO phase noise.



Modeling of VCO with Jitter



Digital modulator

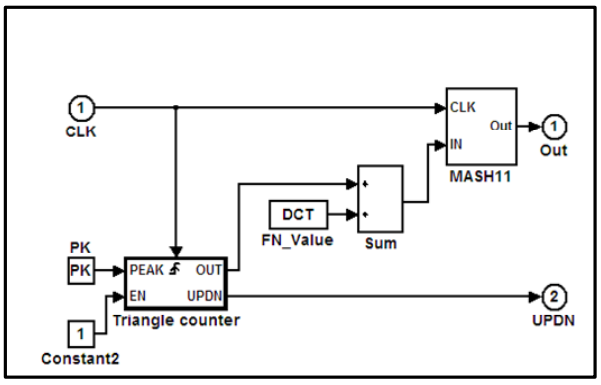


Fig. 4.4. SSCG behavior model in MATLAB.

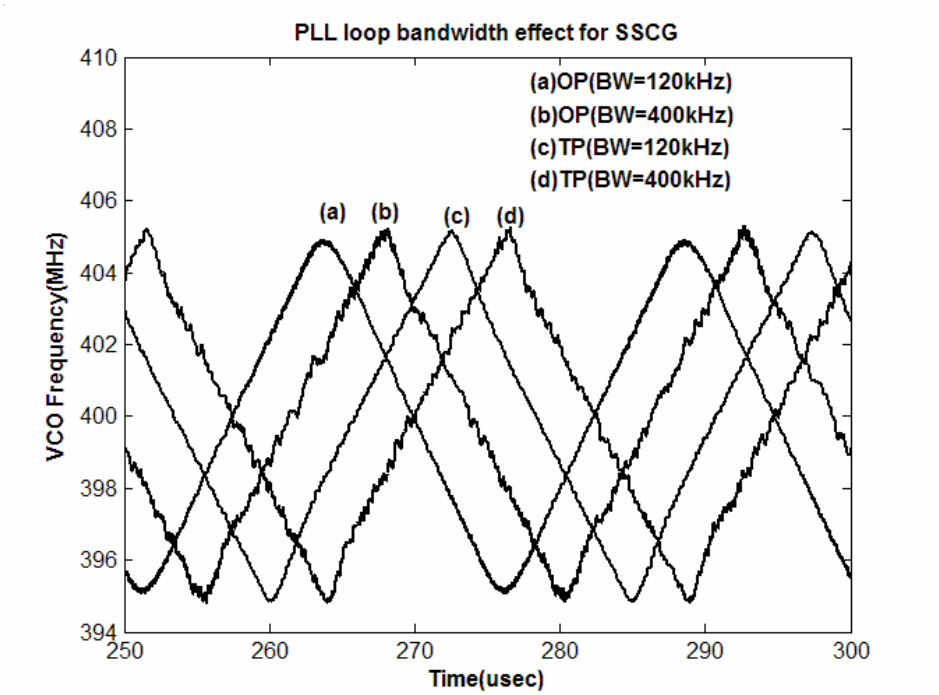


Fig. 4.5. Frequency swings for OP-SSCG and TP-SSCG under different loop bandwidths with the ΔΣ modulator noise.

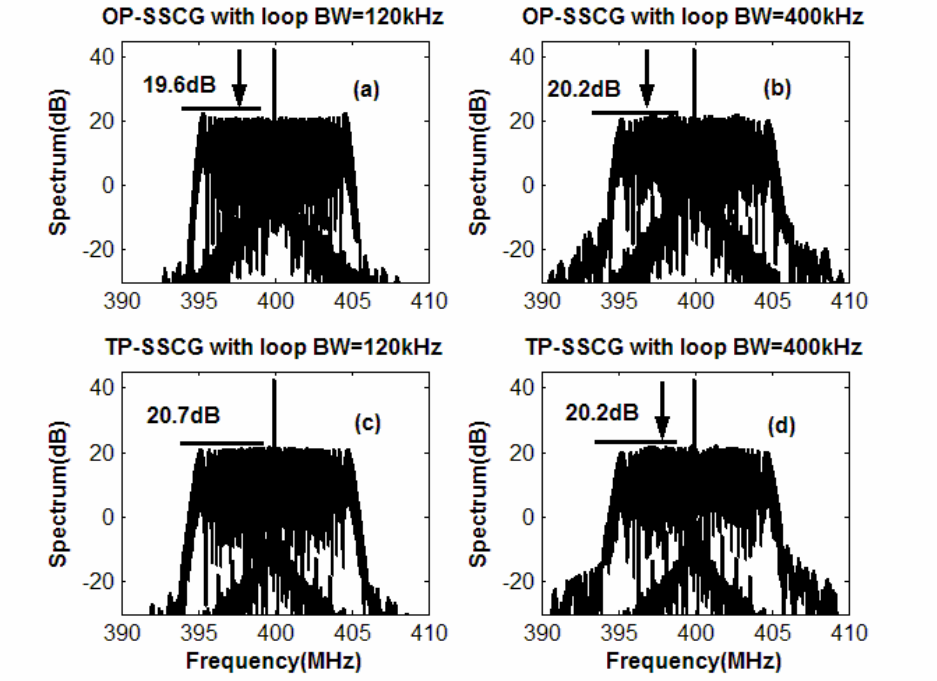


Fig. 4.6. Spectra simulation results for OP-SSCG and TP-SSCG under different loop bandwidths with the ΔΣ modulator noise.

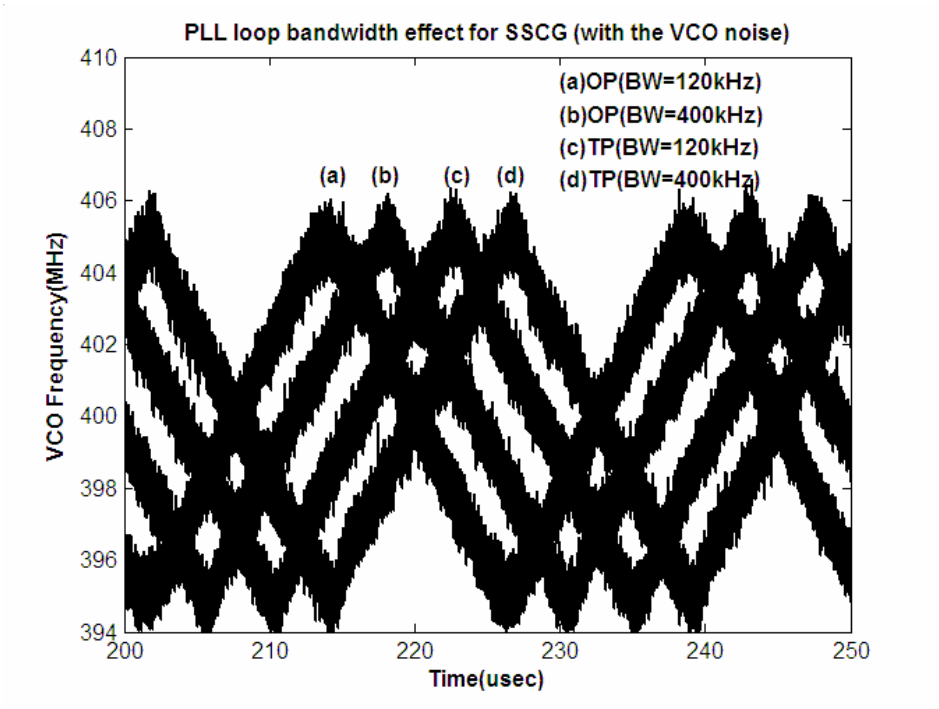
4.2.3 Closed Loop Simulation

The frequency variations involving different loop bandwidths and modulator orders can be examined effectively using MATLAB software [33]. The behavior model using SIMULINK in MATLAB has been constructed in Fig. 4.4. It contains the corresponding blocks, as shown in Fig. 4.1. The digital modulator is detailed in the inset at the lower right side. It is composed of a triangular wave counter to generate the triangle profile, which combines with the fractional part and was sent to the MASH 1-1 ΔΣ modulator. Its output denoted as "Out", was applied to a programmable divider. A memory cell was used to avoid delays during simulation. Another output denoted UPDN was fed to charge pump CP_3 to perform the digital to analog conversion. The VCO is modeled by a voltage controlled frequency (VCF) followed by a frequency-to-clock transformation. The accumulation jitter is modeled by the frequency error as shown in the upper section of Fig. 4.4 [34]. The frequency output of the VCO combined with the accumulation jitter can be evaluated as

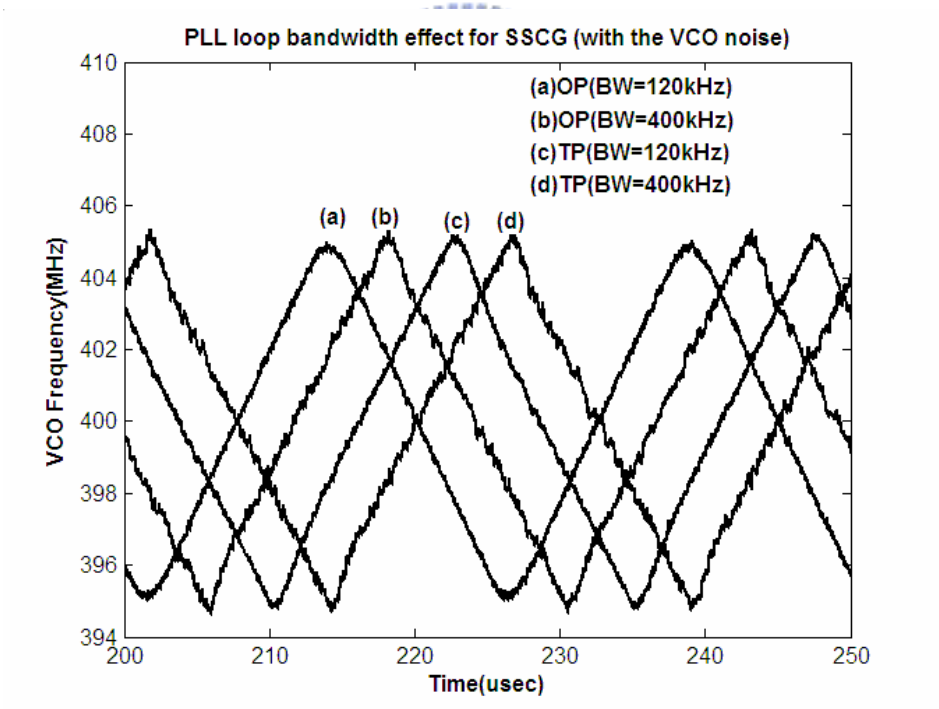
$$\omega_{out} = 2\pi \frac{V_c K_{vco}}{1 + J V_c K_{vco}} \tag{4.7}$$

where J is the factor of the accumulation jitter represented by a zero-mean Gaussian random process and can be evaluated from the VCO phase noise [34]. The standard deviation of J is 1.25 ps in our case according to -100 dBc/H at 1 MHz offset. Only the VCO output frequency was manipulated, rather than the real waveform. The divided frequency was integrated into a phase output and digitized into a clock. Except for the PFD, the main PLL loops use a S-domain transfer function only; therefore, the simulation speed was very fast. For instance, approximately 5 minutes are required for 200 us simulation time using Matlab; while nearly 24 hours are needed when using a real circuit simulator such as Hspice.

The influence of the VCO phase noise and modulator quantization noise are examined step by step. First, only the latter needs to be considered. In other words, J is equal to 0 in this context. The frequency swings from f_{out} are illustrated in Fig. 4.5. The center is at 400 MHz with a spread ratio of 2.5%. The modulation frequency is at 40 kHz. Curve (a) is with a one-point modulation and a narrow loop bandwidth of 120 kHz. It appears smooth and clean, but with a reduced spread. This implies that any spurious affect is suppressed, but the loop



(a)



(b)

Fig. 4.7. Frequency swings for OP-SSCG and TP-SSCG under different loop bandwidths with the ΔΣ modulator noise and the VCO noise (a) original (b) filtering out the VCO noise.

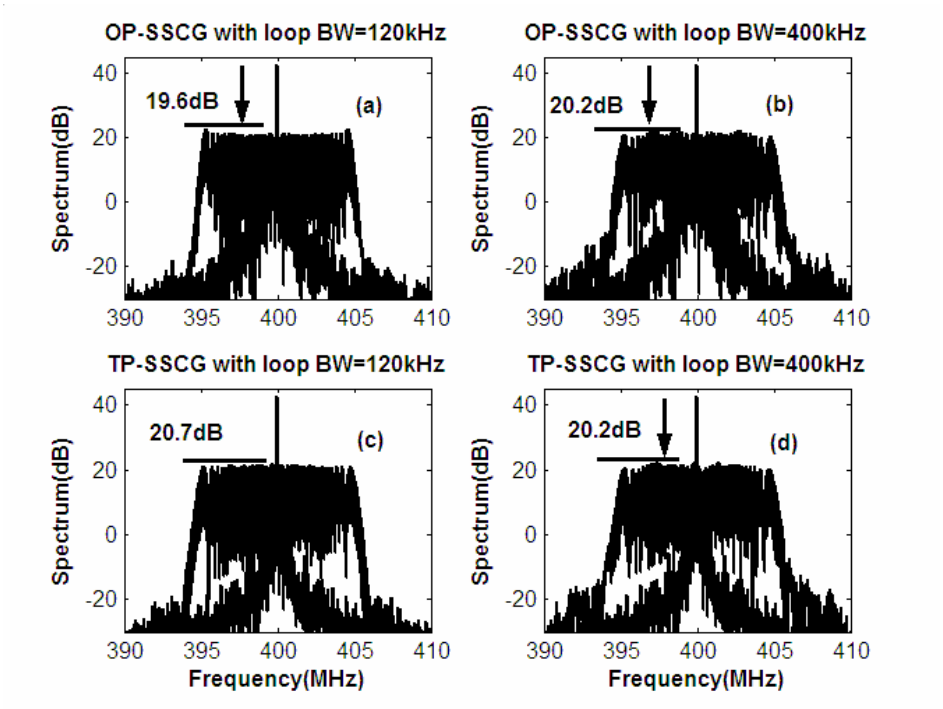


Fig. 4.8. Spectra simulation results for OP-SSCG and TP-SSCG under different loop bandwidths with the ΔΣ modulator noise and the VCO noise.

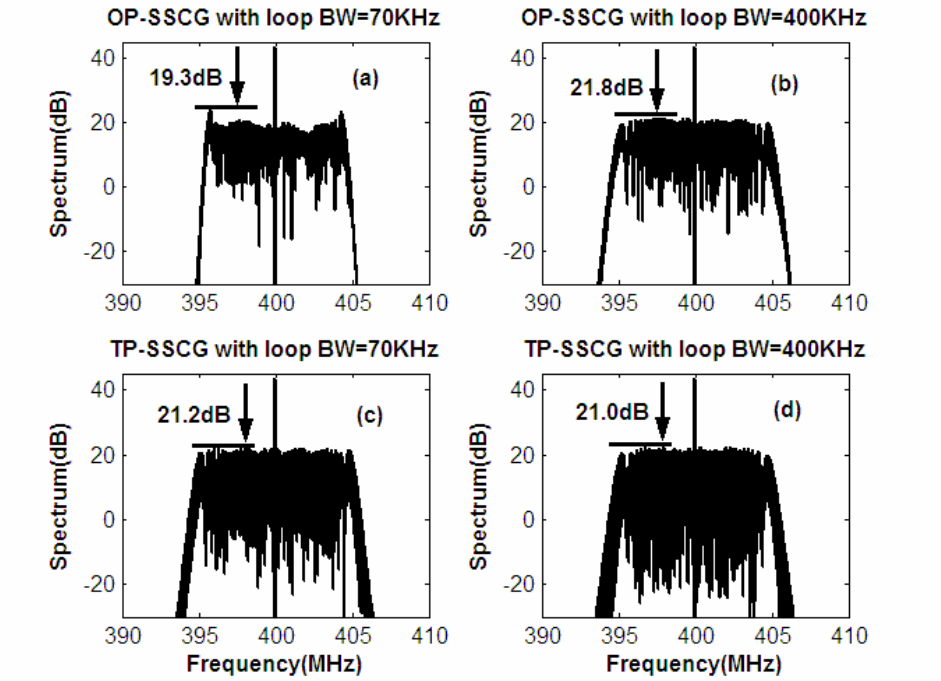


Fig. 4.9. Spectra simulation results for OP-SSCG and TP-SSCG under different loop bandwidths without any noise.

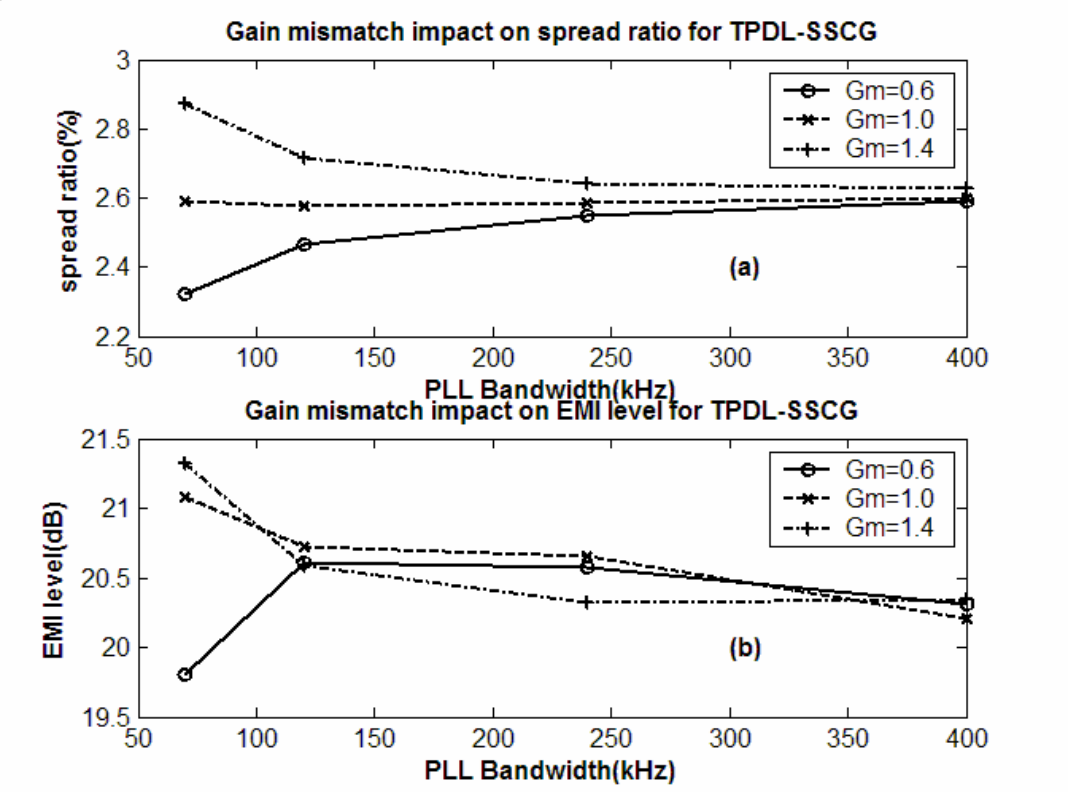


Fig. 4.10. Simulation results for gain mismatch effects under different loop bandwidths.

Table 4.2 SSCG Simulation Summary

	With ΔΣ noise		With ΔΣ noise and VCO phase noise	Without any noise
	Spread ratio	EMI	EMI	EMI
OP-SSCG (120KHz)	2.440	19.6	19.6	20.5
OP-SSCG (400KHz)	2.620	20.2	20.2	21.8
TP-SSCG (120KHz)	2.578	20.7	20.7	21.1
TP-SSCG (400KHz)	2.598	20.2	20.2	21.0
UNIT	%-pp	dB	dB	dB

bandwidth is not wide enough. Curve (b) is a one-point modulation with a wide bandwidth of 400 kHz. It appears noisy but greater in span. Curve (c) is with a two-point modulation and a narrow bandwidth of 120 kHz. It exhibits clean lines and has a sufficient span. Curve (d) is with a two-point modulation and a wide bandwidth of 400 kHz. It also has sufficient span but is noisy. The spreading ratios of 2.440%, 2.620%, 2.578%, and 2.598% were attained in curves (a), (b), (c), and (d), respectively. It is clear that curve (c) has not only a more accurate spread ratio, but also lower noise. Compared to curves (a) and (b) there is a 0.2% difference in spread ratios; while there is only a 0.02% difference when compared to curves (c) and (d). The slight difference between curves (c) and (d) is due to the influence of quantization noise. This suggests that the effect of bandwidth is insignificant in the proposed modulation.

After Fourier transformation at f_{out} with Hanning window, the EMI suppression levels attained are shown in Fig. 4.6: 19.6 dB, 20.2 dB, 20.7 dB and 20.2 dB for curves (a), (b), (c), and (d), respectively. It is clear that curve (c) has a better suppression performance than curve (b). Curve (a) has the worst EMI suppression levels because the PLL loop bandwidth is not wide enough and resulted in two peaks appearing in the two ends of the spectrum. Moreover, the quantization noise impact on the EMI suppression levels are clearly evident from curves (c) and (d). As the bandwidth is creased from 120 kHz to 400 kHz, the suppression level is degraded with a value of 0.5 dB.

Next, the VCO phase noise was added. The frequency swings and spectra from f_{out} are depicted in Fig. 4.7 and 4.8, respectively. The results are summarized in Table 4.2. Fig. 4.7(a), indicates almost the same clearance for both SSCGs. It is difficult to discern any difference between both SSCGs from Fig. 4.7(a). A test was done with the VCO phase noise filtered as shown in Fig. 4.7(b). It implies that the VCO phase noise only contributes the jitter not the EMI levels as confirmed in Fig. 4.8. Therefore, it can be concluded that quantization noise is more important in terms of EMI performance than VCO phase noise.

Third, in order to investigate thoroughly the effect of quantization noise on EMI suppression, the spectra simulation without the ΔΣ modulator noise for OP-SSCG and TP-SSCG under the same conditions as in Fig. 4.5 and 4.6 was applied (Fig. 4.9). The simulation results are also summarized in Table 4.2. The impact of quantization noise on EMI suppression levels for

curve (b) is 1.6 dB (=21.8-20.2); while it is 0.8 dB (=21.0-20.2) for curve (d). It can be clearly seen that the impact on the EMI performance of curve (c) is only 0.4 dB (=21.1-20.7). In short, the noise introduced by the modulator has a detrimental effect on EMI suppression levels. It can be said, therefore, that the advantages of a lower loop bandwidth in a two-point case have been proven.

Finally, the impact of gain mismatch on both spread ratios and EMI performance has also been verified. The cases for G_m=0.6, G_m=1.0 and G_m=1.4 are simulated using varied PLL loop bandwidths. The impact on spread ratios are shown in Fig. 4.10(a). From the results, it can be concluded that the smaller the PLL loop bandwidth, the greater the sensitivity of the spread ratio. When the PLL loop bandwidth is less than 120 kHz, the spread ratio is very sensitive to the gain mismatch between the two points. The variation in spread ratio is about 0.25% for the 120 kHz case. The impact on the EMI performance is shown in Fig. 4.10(b). The EMI performance is less related to the PLL loop bandwidth compared to the spread ratio when the PLL loop bandwidth is greater or equal to 120 kHz. However, the EMI performance is sensitive to the gain mismatch when the PLL loop bandwidth is less than 120 kHz. The variation in EMI performance is about 0.02 dB when120 kHz are involved. The reason for gain mismatch effects on the proposed SSCG is described below and can be restated (4.1) as follows:

$$\Delta\omega_{out} = T(s)\Delta\omega_{sig} + \left(1 - T(s)\right) \times G_m \Delta\omega_{sig} \tag{4.8}$$

The first term in (4.8) is the contribution of the divider modulation and the second term is the contribution of VCO modulation. When the loop bandwidth is quite small, the output is dominated by the second term in (4.8); that is the spread ratio is sensitive to gain mismatch. In other words, when the loop bandwidth is quite large, the output is dominated by the first term in (4.8); that is, the spread ratio is less sensitive to gain mismatch. However, it can be noted from the previous analysis that EMI performance is degraded when the loop width is large due to modulator quantization noise. Therefore, based on the analysis in Section II-C., if the gain mismatch is insignificant, the bandwidth can be lowered in order to achieve the desired performance. If the gain mismatch is equal to or greater than 0.4, a trade-off is required involving loop bandwidth and performance. Thus, in order to reduce the effect of gain mismatch, an appropriate loop bandwidth needs to be selected to allow the passage of

the first and the third Fourier frequencies of the triangular waveform through the divider path and to allow the fifth and higher Fourier frequencies through the VCO path. This approach allows the output waveform to be affected by both the divider and VCO modulation paths. As a rule of thumb, the desired loop bandwidth should be three times the modulation frequency. Therefore, the 120 kHz loop bandwidth is chosen in this study with a 40 kHz modulation frequency.

4.3 Circuit Description

In order to eradicate the problem of sensitive tuning associated with VCO and to accomplish total integration, an attractive arrangement for the loop filter has been proposed. The complete block diagram of the proposed SSCG with a PFD, a dual-path loop filter with charge pumps CP_1, CP_2, a VCO, a 8-bit programmable counter (PGC), a digital ΔΣ modulator, a modulation profile generator, and a digital to analog converter (DAC) is shown in Fig. 4.11. The dual-path loop filter [18] consists of charge pumps CP_1, CP_2, capacitors C_1, C_2, resistor R_1, and a unity-gain amplifier. The triangular wave generated from the profile generator is fed simultaneously to the digital ΔΣ modulator and the DAC. The modulation points are denoted by V_1 and V_2.

The proposed DAC is redrawn in Fig. 4.12(a). It consists of a digital slicer, charge pump CP_3, and capacitance C_1. An analog triangular waveform across C_1 is obtained from digital triangular waveform, f_{sig}. The digital triangular waveform is first sliced into a square waveform, f_{sig1}, and then the capacitor C_1 is charged to a achieve digital-to-analog conversion. The digital transition is smoothed out to reduce VCO interference. Unlike a traditional DAC [29], neither a high resolution DAC nor a reconstruction filter is needed. Therefore, both power consumption and chip area can be reduced.

The delay mismatch might degrade performance of the two point architecture [29]. The following approach is utilized to eliminate this degradation. With reference to the timing diagram in Fig. 4.12(b), f_{sig1} and V_y are two clocks with delayed f_{sig} in order to be synchronized with the output of the ΔΣ modulator, V_x. Due to the fact that the digital slicer, the profile generator, and the ΔΣ modulator all use the same clock, f_{div}, a mismatched delay can be avoided.

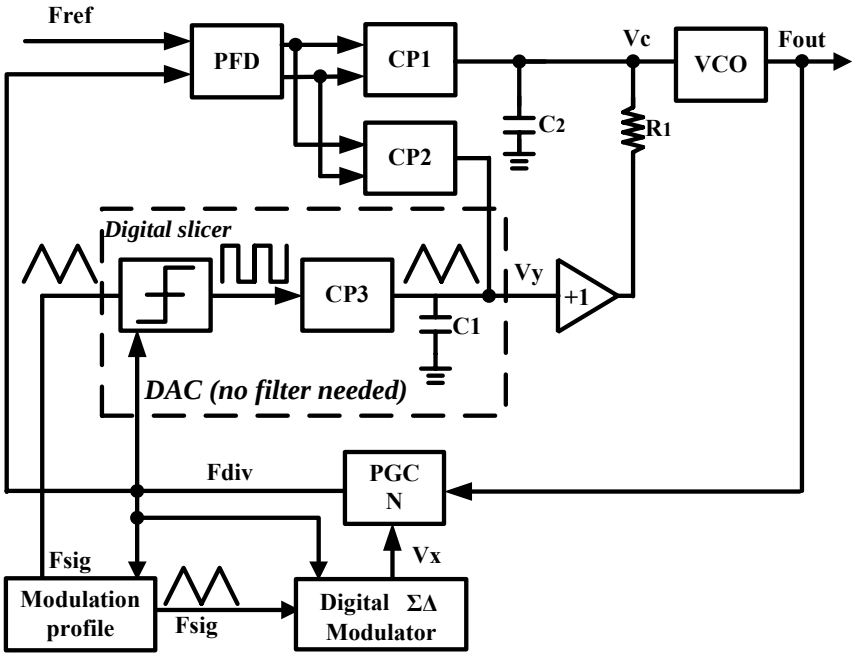
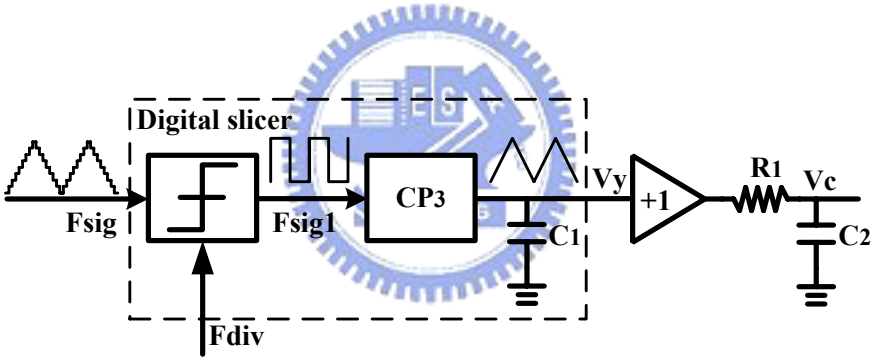
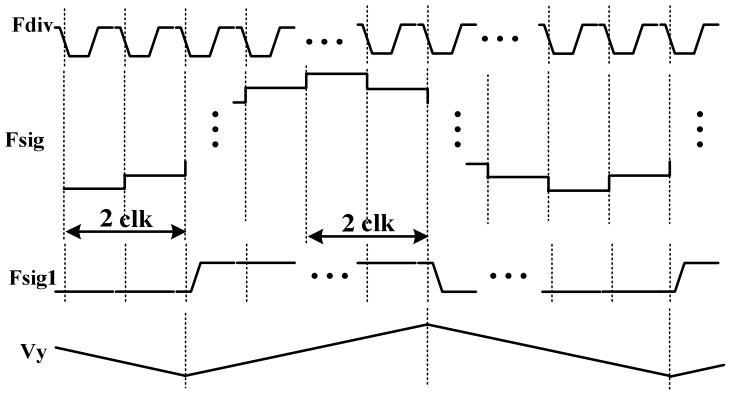


Fig. 4.11. The block diagram of proposed TP-SSCG.



(a)



(b)

Fig. 4.12. (a) Proposed DAC (b) Timing diagram for the proposed DAC.

After digital transition is smoothed out, fine tuning can be achieved by controlling the charge current. Disregarding the loading effects in CP_1 and CP_2, the relation between controlled voltage V_c and the current I_{p3} of CP_3 can be expressed as

$$\frac{V_c}{I_{p3}} \approx \frac{1}{sC_1} \tag{4.9}$$

when $f_{sig} << 1/(2\pi R_1 C_2)$. The analog triangular wave is generated as a result of I_{p3} being a square wave. The digital transitions which reside in the triangular wave can be effectively smoothed out. The relationship between the spreading ratio δ and I_{p3} which is defined as $\Delta f_{out} / f_{out}$, is derived as

$$\delta = \frac{I_{p3} K_{vco}}{2C_1 f_{sig} f_{out}}. \tag{4.10}$$

The gain mismatch factor may be the result of I_{p3}, C_1, and K_{VCO}. Since C_1 varies by approximately 5% in the typical CMOS process, the gain mismatch is mainly the contribution of K_{vco}. Therefore, a VCO with low sensitivity to VCO gain is needed. In this work, K_{vco} is varied by about +/-25% with respect to process, voltage and temperature variations. This results in an alteration in G_m from 0.75 to 1.25. From the simulation results in Section II-D, the impact of gain mismatch on the spread ratio will vary by approximately 0.15% and the gain mismatch impact on EMI performance is about 0.01 dB. The variation both in spread ratio and EMI performance is acceptable in the proposed model. Once the variation in spread ratio is greater than the specification, VCO calibration technique can be applied, as in [24], to further improve performance.

Capacitor C_1 plays an important role. It converts not only the digital modulation signal into analog, but it also acts as a part of the loop filter. In the proposed model C_1 with one grounded terminal is implemented by the accumulation of an MOS capacitor to save area and to reduce distortion when the gate-source bias voltage is equal to or greater than 1 V [30]. The driving-point impedance function V_c/I_{p1} is easily obtained as follows:

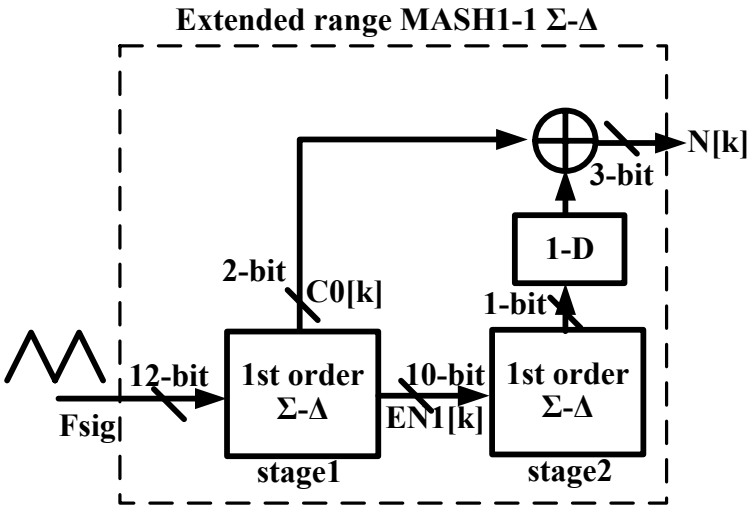


Fig. 4.13. Extended range MASH 1-1 ΔΣ modulator.

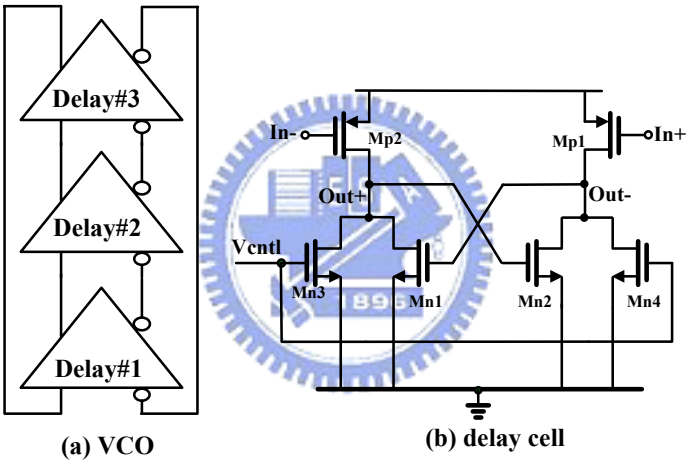


Fig. 4.14. (a) VCO circuit and (b) delay cell used in VCO.

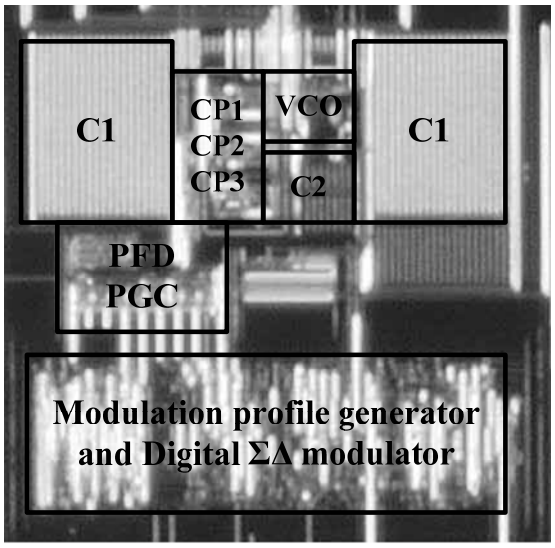


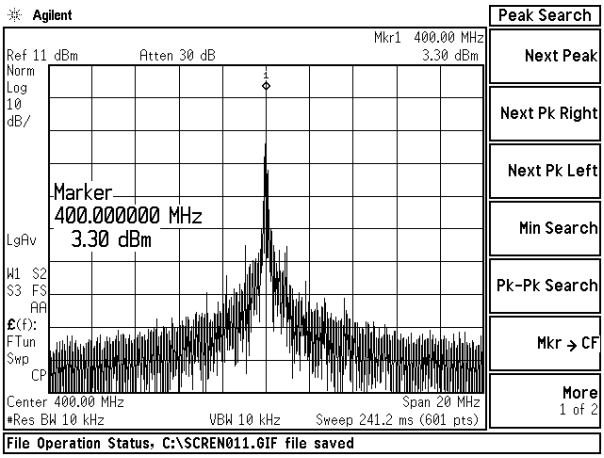
Fig. 4.15. TP-SSCG die photograph.

$$F(s)=\frac{V_c}{I_{p1}}=\frac{R_1\left(s+\frac{1}{R_1BC_1}\right)}{s\left(1+sR_1C_2\right)}. \tag{4.11}$$

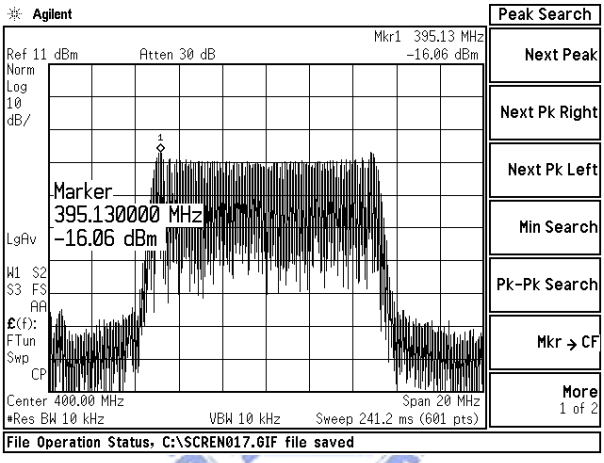
The pole is determined by $1/R_1C_2$, zero is determined by $1/BC_1R_1$, where B is the multiplier factor of charge pump currents I_{p1} and I_{p2},, and $I_{p1}=BI_{p2}$. The area of C_1 is reduced with the aid of CP_2.

The circuits employed in the work are described briefly next. It is worthwhile to briefly mention in this context the 2nd order MASH 1-1 ΔΣ modulator. Its input range must be extended to overcome the overflow problem due to the equivalent fractional part being greater than 1 [23], as shown in Fig. 4.13. The input range of a conventional modulation is between $1/2^{BT}$ to $1-1/2^{BT}$ with a bit width of BT=10. As input exceeds 1, the saturated modulator collapses.. In order to overcome this drawback, Stage-1 is modified to have a two-bit carry while Stage-2 remains unchanged. The two-bit carry output can manifest an input larger than or equal to 1 in such a way that it quickly transfers the integer part of the input to the output without saturating the subsequent stages. The input range can be extended to $3-1/2^{BT}$. The chip areas for second-order and third order MASH ΔΣ modulators measure 3920 and 4887 in units of gate-counts, respectively. The area of the proposed modulator is about 40% of the total area; therefore, the area is approximately 9% smaller than that needed when using a second-order ΔΣ modulator. The power consumption is also reduced.

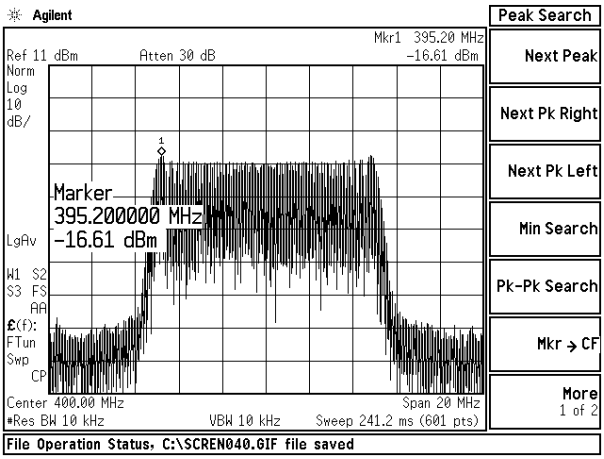
A wide band VCO consists of three stages of differential delay cells, as shown in Fig. 4.14(a) [10]. A schematic representation of the delay cell is shown in Fig. 4.14(b). The cross-coupled connection M_{n1} and M_{n2} is utilized to achieve a full swing and sharp waveform in order to reduce jitter. The VCO gain was found to vary by approximately +/-25% dependent on process, voltage and temperature corners making this VCO suitable for two point modulation.



(a)

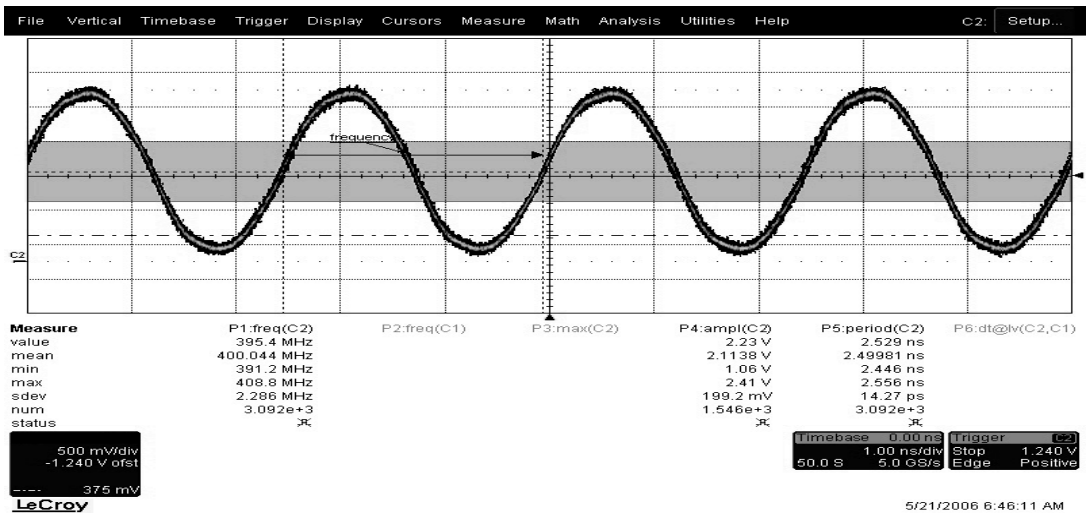


(b)

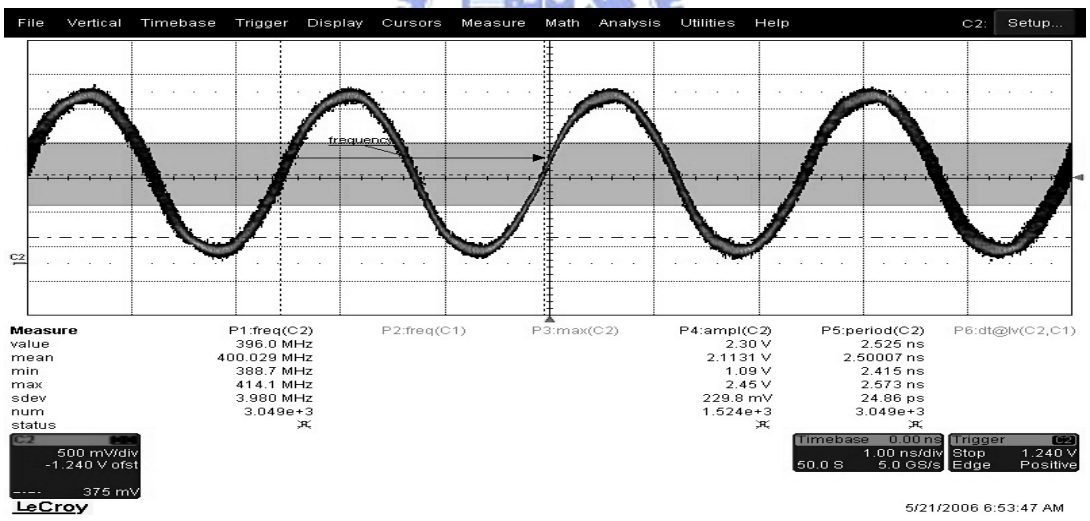


(c)

Fig. 4.16. Measured spectra of 400 MHz output frequency (a) at non-spread spectrum mode, (b) of conventional SSCG with 2.5% spread ratio, and (c) of TP-SSCG with 2.5% spread ratio.



(a)



(b)

Fig. 4.17. Measured jitter of 400MHz output frequency (a) at non-spread spectrum mode, and (b) of TP-SSCG with 2.5% spread ratio.

4.4 Measurement

The chip is designed and fabricated using TSMC 0.35 μm single-poly quadruple-metal CMOS process. The die photograph is shown in Fig. 4.15 and has an area equal to 0.90×0.89 mm^2. The output spectrum at 400 MHz without spreading is shown in Fig. 4.16(a). The magnitude of the peak is 3.30 dBm. The spectra for one and two-point modulations under a

2.5% spread ratio are shown in Fig. 4.16(b) and (c) with magnitudes of -16.06 dBm and -16.61 dBm, respectively. The loop bandwidth is 120 kHz for both modulations. Fig. 4.16(b) is obtained by switching off the VCO modulation. The reductions in peaks are approximately 19.36 dB and 19.91 dB for Fig. 4.16(b) and (c), respectively. Two small peaks which are due to an insufficient loop bandwidth are still visible at the edges in Fig. 4.16(b).With reference to Fig. 4.16(c), the EMI improved to 0.55 dB under the same loop bandwidth. The measured rms jitter is 14.27 ps under the non-spread spectrum mode as in Fig. 4.17(a) and reaches 24.86 ps under the 2.5% spread ratio as in Fig. 4.17(b).The rms jitter is increased to 10.59 ps, which is very close to the theoretical estimation of 10.42 ps (=2.5%×2500 ps/6). It has also been assumed that the total jitter is six times that of the rms jitter. Table 4.3 provides a summary of performance. The total power consumption is 33 mW and includes an output buffer.

4.5 Summary

In this study, a low jitter SSCG with a two-point modulation scheme has been presented. This technique permits an all-pass feature, even when a finite loop bandwidth is involved. This technique offers two advantages; first, an almost distortion-free response involving triangular modulation, which provides a 0.55 dB improvement in EMI suppression when compared with a conventional scheme. Second, a small loop bandwidth also offers the possibility of choosing a second order sigma-delta modulator without the disadvantage of quantization noise. Furthermore, both chip area and power consumption have been reduced. An attractive DAC structure has been proposed to accommodate the two-path loop filter and sensitive VCO modulation. The proposed technique provides total integration and suppresses the digital spur associated with highly sensitive VCO input. The effects of the VCO phase noise and the

quantization noise of the modulator are clearly verified. The VCO phase noise shows minor impact on the EMI performance; while the quantization noise has big degradation on the EMI performance.

Table 4.3 Performance Summary

Modulation Method	Two point
Modulation Type	Center-spread
Modulation Frequency	40 kHz
Spread Ratios(pp)	1.25%, 2.5%
Output Frequency	400 MHz
VCO Gain	200 MHz/V
Input Frequency	14.31818 MHz
Loop bandwidth	~120 kHz
Loop filter	R_1=12 kΩ C_1=400 pF C_2=40 pF
Charge Pump Current	Ip_1=9 uA
EMI reduction	19.91 dB @ 2.5% center spread ratio
Jitter	14.27 ps rms at SSC-off 24.86 ps rms at SSC-on
Chip Area (active)	0.90×0.89 mm^2
Power Dissipation	33 mW including output buffer @ 3.0V

CHAPTER 5

A Low Power and High Precision Spread Spectrum Clock Generator for SATA Applications Using Two Point Modulation

A new technique utilizing two-point modulation (TP) for a spread-spectrum clock generator (SSCG) for serial advanced technology attachment is presented in which the divider ratio is varied by a ΔΣ modulator, and the voltage-controlled oscillator is modulated. With this technique, the modulation bandwidth is enhanced in order that the modulation profile accuracy and jitter performance caused by the ΔΣ modulator can be improved at the same time. The order of the ΔΣ modulator and the loop filter can be reduced to save power and area, while the electromagnetic interference (EMI) suppression still satisfies specifications. The dual-path loop-filter (DL) reduces the size of the loop capacitor and enables full integration. The proposed TPDL-SSCG has been fabricated in a 0.18 μm complementary metal oxide semiconductor process. The size of chip area is 0.44×0.48 mm^2. The circuit produces a clock of 1.5 GHz with a down spread ratio of 0.5%, 10.14 dB EMI of reduction, 5.485 ps rms jitter and 35 ps peak-to-peak jitter. The power consumption, excluding an output buffer, is only 15.3 mW.

5.1 Introduction

Serial interfaces are widely used for high data rate transmission. For example, serial advanced technology attachment (SATA), which is the standard for high-speed storage devices such as hard disc drives and compact disc (CD)/digital versatile disc (DVD), can transmit data at rates up to 1.5 Gbps or 3 Gbps for generation I and II, respectively [35]. High-speed clocks often cause electromagnetic interference (EMI). Therefore, the spread-spectrum clock generators (SSCG) are employed in SATA to reduce EMI levels.

Typical specifications in SATA are the 5000 ppm down-spread ratio, modulation frequency within 30-33 kHz, and EMI suppression of at least 7 dB. In order to realize such a fine spread ratio, fractional-N phase-locked loops (PLLs) with a ΔΣ modulator are usually used [9], [13], [22]-[24]. This technique has the advantages of fully digital control and fine resolution. The modulator is normally driven by a triangular waveform. A non-linear profile, known as the 'Hershey-Kiss' profile, has been suggested for better EMI performance [2]. The nonlinear function of the 'Hershey-Kiss' profile makes it more expensive due to large area and power consumption. Therefore, triangular waveforms are still used due to their simple implementation [9], [15], [36]. Another important issue is the choice of loop bandwidth of PLL. The loop bandwidth has trade-offs between the modulation profile and the jitter caused by ΔΣ modulator. The profile is distorted and the effect of EMI suppression is degraded if the loop bandwidth is not wide enough. Therefore, the wide bandwidth leads to a request for a third order ΔΣ modulator in order to suppress the in-band fractional spurious. A design of a third order ΔΣ modulator with a third order loop filter and a 300 kHz loop bandwidth to improve the jitter and the modulation profile was presented in [36]. However, the third order ΔΣ modulator has high power consumption and occupies a large area. Recently, the method of two-point (TP) modulation, which has the divider and the voltage-controlled oscillator (VCO) modulated at the same time, was presented to enhance the bandwidth and improve EMI performance [25]-[26]. Here, a new version of SSCG with two-point modulation is presented for the SATA application [38]. The jitter caused by the ΔΣ modulator can be reduced by a small loop bandwidth, while the modulation profile can still be maintained. Only a second order ΔΣ modulator, as well as a second order loop filter, is adopted. The chip area and power consumption are improved. In addition, aided with a dual-path loop filter (DL), the proposed TPDL-SSCG can be fully integrated.

5.2 Proposed TPDL-SSCG

It is well known that the transfer function of the phase response from the feedback divider to VCO output is a low pass function. On the contrary, the function from VCO input

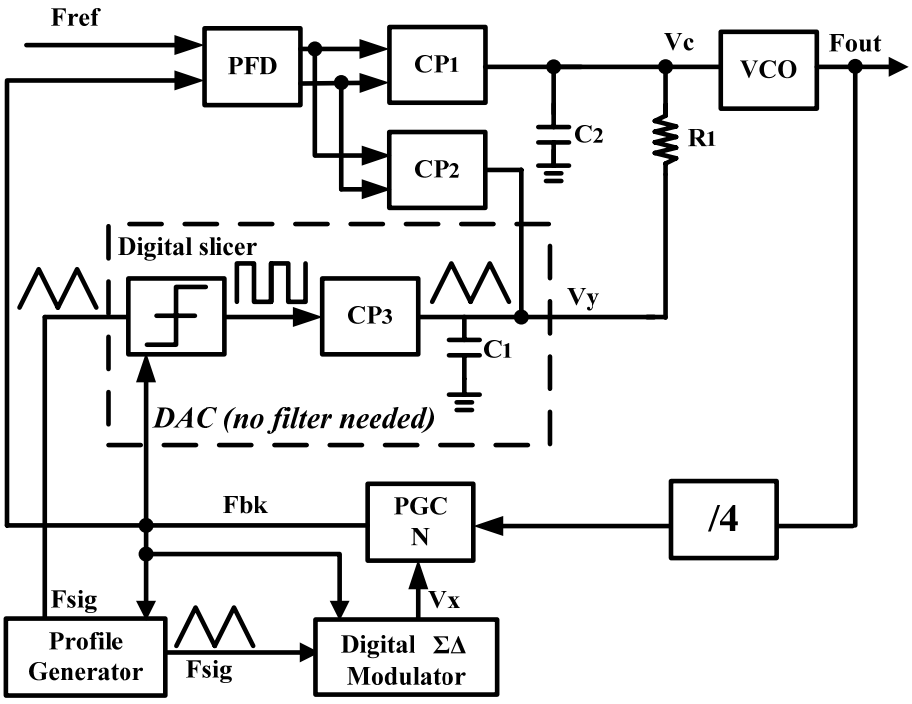
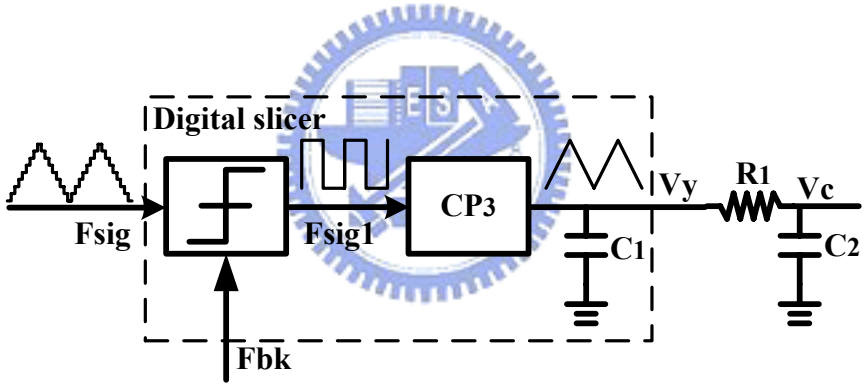
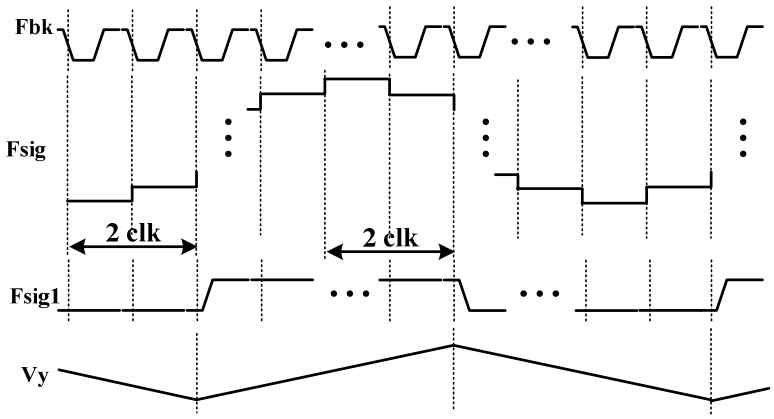


Fig. 5.1. The block diagram of the proposed TPDL-SSCG



(a)



(b)

Fig. 5.2. (a) Proposed DAC. (b)Timing diagram for the proposed DAC.

to VCO output is a high pass function. A wideband response can be achieved if the loop is excited through these two points. The block diagram of the proposed SSCG is shown in Fig. 5.1 with a phase frequency detector (PFD), a dual path loop filter containing CP_1, CP_2, R_1, C_1, and C_2, a VCO, a prescaler, a 5-bit programmable counter (PGC), a digital ΔΣ modulator, a modulation profile generator, and a DAC. Compared to the conventional one, this circuit incorporates two extra circuits of charge pump CP_2 and DAC. The staircase triangular waveform is digitally generated by the profile generator. The frequency modulation is obtained from two inputs V_x and V_y. V_x is the input of the multi-modulus divider and V_y is the input of the VCO. The all pass behavior is obtained as long as the modulation coefficients along the two paths are matched.

5.2.1 The Proposed DAC

The function of the DAC is redrawn in Fig. 5.2(a). It consists of a digital slicer, charge pump CP_3, and capacitance C_1. An analog triangular waveform across C_1 is obtained from a digital triangular waveform, f_{sig}. The digital triangular waveform is first sliced into a square waveform, f_{sig1}, and then charges the capacitor C_1 to achieve digital-to-analog conversion. The digital transition is smoothed out to reduce VCO interference. As compared to a traditional one, no high resolution DAC or reconstruction filter is needed [29]. Therefore, the power consumption and the chip area can be reduced.

The delay mismatch is known to degrade the performance [29]. The following approach is utilized to eliminate this non-ideality. Referring to the timing diagram in Fig. 5.2(b), f_{sig1} and V_y are two clocks delayed with respect to f_{sig} in order to synchronize the delay from f_{sig} to the output of the ΔΣ modulator, V_x. Because the digital slicer, the profile generator, and the ΔΣ modulator use the same clock, f_{bk}, which is the output frequency of the PGC, the delay mismatch can be avoided.

The relation between controlled voltage V_c and the current I_{p3} of CP_3 can be written as

$$\frac{V_c}{I_{p3}} \approx \frac{1}{s(C_1 + C_2)}, \tag{5.1}$$

under the condition $f_{sig} << 1/(2\pi R_1 C_2)$. The loading effects of CP_1 and CP_2 are neglected due to high output impedances. Accordingly, the smooth triangular waveform is obtained, as Ip3 is a square waveform. Here, both C_1 and C_2 with one terminal grounded are implemented by

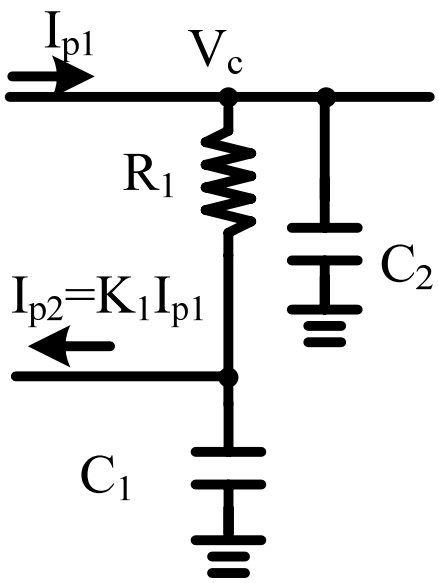


Fig. 5.3. Simplified block diagram of the dual path loop filter.

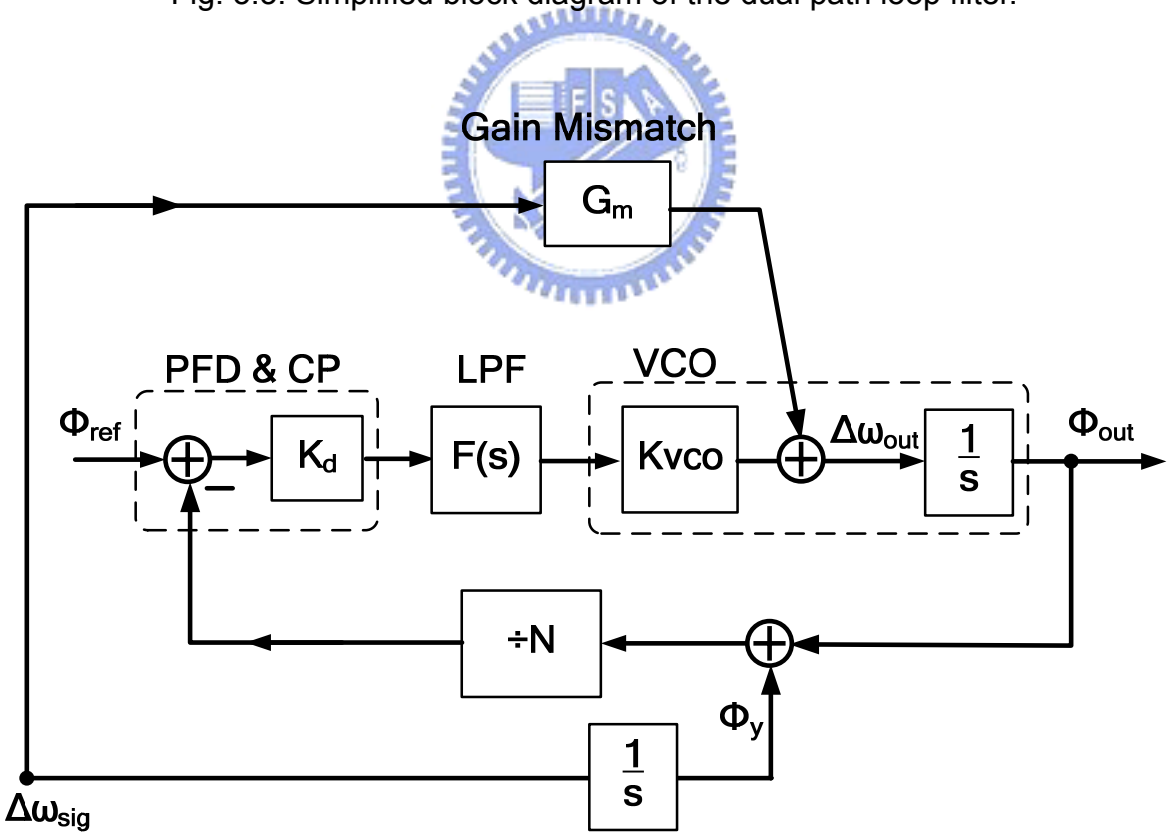


Fig. 5.4. Linear model of the proposed TPDL-SSCG.

the accumulation MOS capacitor to save area. Both have good distortion performance when the gate-source bias voltage is equal to, or large than, 1 V [30]. The spread ratio $\delta \equiv \Delta f_{out} / f_{out}$ as a function of I_{p3} is predicted as

$$\delta = \frac{I_{p3} K_{vco}}{2(C_1 + C_2) f_{sig} f_{out}}, \tag{5.2}$$

where f_{out} is the nominal VCO output frequency, f_{sig} is the modulation frequency of the triangle wave, and K_{vco} is the conversion gain of VCO.

5.2.2 Dual-Path Loop Filter

To save the capacitor area in the loop filter, a modified dual-path loop filter is utilized [37]. The paths of pumping currents are shown in Fig. 5.3, in which I_{p1} is the current of CP_1, and I_{p2} is the current of CP_2. $I_{p2}=K_1 I_{p1}$. The loading effect of CP_3 is neglected. The loop filter transfer function can be derived as

$$F(s) = \frac{V_c}{I_{p1}} = \frac{\frac{R_1 C_1}{C_1 + C_2}\left(s + \frac{1}{R_1 K_2 C_1}\right)}{s\left(1 + sR_1\left(C_1 // C_2\right)\right)}, \tag{5.3}$$

where $K_2=1/(1-K_1)$. The zero is at $1/(K_2 C_1)R_1$. From (5.3), the effect of capacitance multiplication is high when K_1 is close to 1. It means that the I_{p1} and I_{p2} are close to each other. However, the mismatch between I_{p1} and I_{p2} depends on the area. Therefore, a trade-off should be made. Here $K_1=0.75$ and $K_2=4$ such that the size of capacitance C_1 can be reduced by four times. Compared to the dual path filter in [18], the dual path filter adopted here doesn't need a unity-gain amplifier; therefore the phase noise is smaller.

5.2.3 Linear Model Analysis

Rather than finding out the phase relationship, here the frequency relationship in s-domain is adopted to study the frequency modulation in SSCG. The linear model is shown in Fig. 5.4, where $\Delta\omega_{out}$ is the output frequency deviation, $\Delta\omega_{sig}$ is the input modulation frequency deviation, and G_m is the gain mismatch factor stand for compensation between two paths. Two noise sources are taken into consideration: modulator quantization noise $\Phi_{\Delta\Sigma}$ and VCO phase noise Φ_{vn}. According to (5.2), the gain mismatch may come from the process

variation of K_{vco}, I_{p3}, and C_1 and C_2. Here the delay mismatch is assumed to be negligible due to the proposed DAC.

To see the advantage of two-point modulation, we first examine the results with only one point modulation Vx. For simplicity, the noise sources are ignored. The transfer function from $\Delta\omega$sig to $\Delta\omega$out can be described as

$$\frac{\Delta\omega_{out}}{\Delta\omega_{sig}} = \frac{K_{vco}K_dF(s)}{Ns + K_{vco}K_dF(s)}. \tag{5.4}$$

Here K_d is gain of the PFD and the charge pump and N is the nominal divider value. It is actually a low pass behavior when F(s) in (5.3) is taken into account. $\Delta\omega_{out}$ can be given as

$$\Delta\omega_{out} = \frac{K_{vco}K_dF(s)}{Ns + K_{vco}K_dF(s)}\frac{M_{ramp}}{s} \tag{5.5}$$

as a frequency ramp with a slope of M_{ramp} is applied, i.e., $s\Delta\omega_{sig}=M_{ramp}$. Equation (5.5) can be re-written as

$$\Delta\omega_{out} = \frac{Ks + K\omega_2}{s^2 + Ks + K\omega_2}\frac{M_{ramp}}{s}, \tag{5.6}$$

with $K=K_d\times K_{vco}\times R_1/N$. K is approximately equal to the loop bandwidth of PLL and $\omega_2=1/R_1C_1K_2$ is the zero of the loop filter. Here, the C_2 effect is neglected. The frequency error defined by $\Delta\omega_{err}=\Delta\omega_{sig}-\Delta\omega_{out}$ can be found by

$$\Delta\omega_{err} = \frac{sM_{ramp}}{s^2 + Ks + K\omega_2}. \tag{5.7}$$

Usually $\omega_2 << K$, (5.7) can be approximated by

$$\Delta\omega_{err} = \frac{sM_{ramp}}{(s+K)(s+\omega_2)}. \tag{5.8}$$

Using inverse Laplace transforms, the transient response is obtained

$$\begin{aligned}\Delta\omega_{err}(t) &\approx \frac{M_{ramp}}{K-\omega_2}\left(-\omega_2 e^{-\omega_2 t} + Ke^{-Kt}\right)\\ &\approx \frac{M_{ramp}}{K}\left(-\omega_2 e^{-\omega_2 t} + Ke^{-Kt}\right)\end{aligned}. \tag{5.9}$$

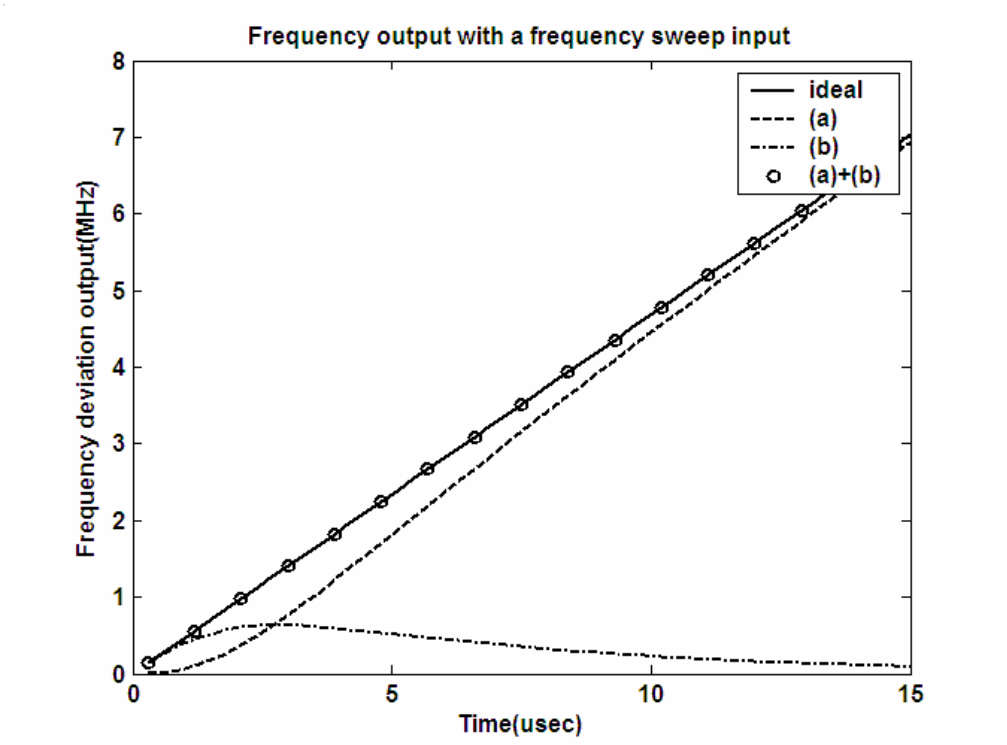


Fig. 5.5 Simulation results of frequency error with a frequency sweep input

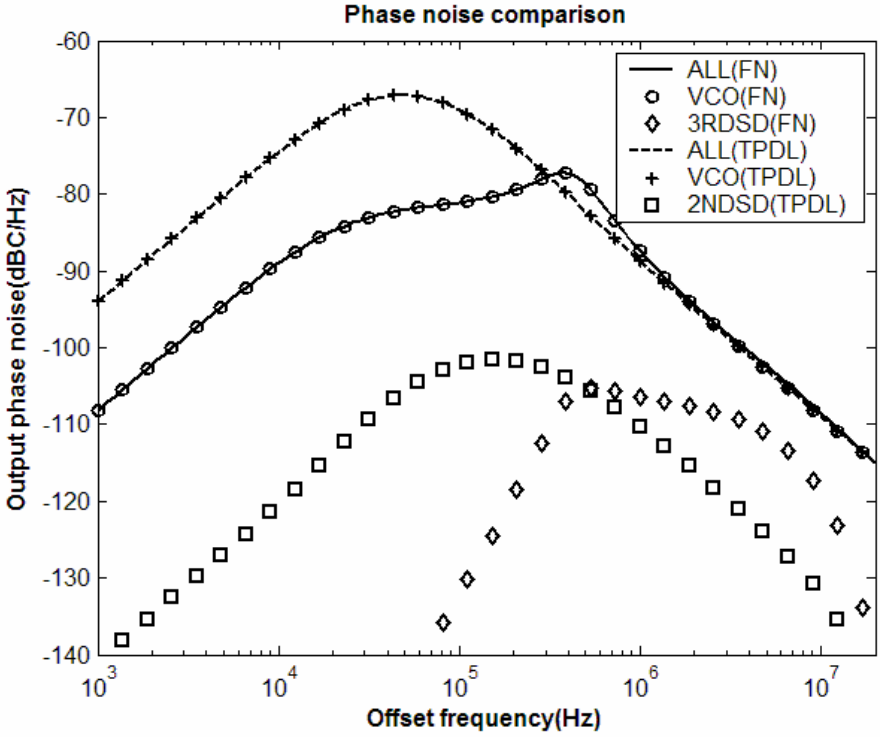


Fig. 5.6 Phase noise simulation for FN-SSCG and TPDL-SSCG

The maximum frequency error, $\Delta\omega_{err}$, can be found by (5.9)

$$\max(\Delta\omega_{err}) \propto \frac{M_{ramp}}{K}. \tag{5.10}$$

Equation (5.9) and (5.10) indicate how the low pass behavior causes frequency errors and distorts the output. It is clear that $\Delta\omega_{err}=0$ only if $K=\infty$, i.e., the loop bandwidth is infinitely large.

With two point modulation activated, by the superposition principle, the closed loop transfer function of Fig. 5.4 can be derived as:

$$\frac{\Delta\omega_{out}}{\Delta\omega_{sig}} = T(s) + (1 - T(s)) \times G_m, \tag{5.11}$$

$$\text{with} \quad T(s) = \frac{K_{vco}K_dF(s)}{Ns + K_{vco}K_dF(s)}. \tag{5.12}$$

The first term in the right hand side is the same as (5.4). The second term appears as a high pass and can be treated as a complementary part if $G_m=1$. Therefore, from (5.11), $\Delta\omega_{out}$ is equal to $\Delta\omega_{sig}$ if $G_m=1$. This means that the output is all pass without distortion and bandwidth limitation. The frequency errors for both one-point modulation and the proposed scheme, with a frequency ramp input, are shown in Fig. 5.5. Here, $G_m=1$. The other parameters are listed in Table 5.1. The solid line is the ideal all pass, the dashed line is from (5.4), the dashed-doted line is from the second term in (5.11), and the line with a circle mark are the output from (5.11). The dashed line cannot track the input frequency change well due to insufficient loop bandwidth. On the contrary, the line with circle mark can always track the input so that the output error is eliminated. Thus, the proposed scheme can track the modulation waveform very well and is independent of the PLL loop bandwidth as long as the paths are matched.

5.2.4 Analysis of Noise Power Spectral Density from the ΔΣ Modulator

The power spectral density is closely related to the order of the ΔΣ modulator and the loop bandwidth. It is already known that a high order ΔΣ modulator is used to reduce the fractional spur within the loop bandwidth. In this design, only a second order ΔΣ modulator is chosen to save area and power, while maintaining jitter and EMI performance. To see the

interrelation between the order of the ΔΣ modulator and the PLL loop bandwidth, the output phase noise originated from the ΔΣ modulator and the VCO are investigated. The noise power spectral densities (PSD) of the phase $S_{\Phi(f)}$ can be expressed as

$$S_{\Phi}(f) = S_{\Phi VCO}(f) + S_{\Phi\Delta\Sigma}(f), \tag{5.13}$$

where $S_{\Phi vco(f)}$ and $S_{\Phi\Delta\Sigma(f)}$ are the noise of the VCO and the ΔΣ modulator, respectively. $S_{\Phi\Delta\Sigma(f)}$ [11] can be found as

$$S_{\Phi\Delta\Sigma}(f) = \frac{(2\pi)^2}{12 f_{bk}}\left[2\sin(\frac{\pi f}{f_{bk}})\right]^{2(m-1)}\left|T(s)_{s=j2\pi f}\right|^2, \tag{5.14}$$

where m is the order of the modulator, and f_{bk} is the operational frequency of the modulator. $S_{\Phi vco(f)}$ can be easily derived as

$$S_{\Phi VCO}(f) = S_{\Phi vn}\cdot\left|1 - T(s)_{s=j2\pi f}\right|^2, \tag{5.15}\backslash$$

where $S_{\Phi vn}$ is the stand alone VCO phase noise.

In general, the loop bandwidth is much less than the phase comparison frequency f_{bk} at the phase detector to avoid the spur. From (5.14), it is realized that the shape of output PSD, caused by the ΔΣ modulator, is increasing inside of the PLL loop bandwidth with $f^{2(m-1)}$ and decreasing outside of the PLL loop bandwidth. In other words, the smaller the PLL loop bandwidth, the lower the jitter caused by the ΔΣ modulator. However, a large PLL loop bandwidth is needed to pass faithfully the modulation profile. Otherwise, the spectrum appeared at the output of PLL will be distorted, the spread ratio will be incorrect and EMI performance will be degraded. Thus, the PLL loop bandwidth is a trade-off between the modulation profile and the jitter performance. In the conventional situation [36], the bandwidth is approximately ten times the modulation frequency to obtain modulation performance. The in-band fractional spur are suppressed by a third-order ΔΣ modulator to minimize the phase noise and jitter. In addition, a third-order loop filter is needed to reduce the out-of-band phase noise and jitter caused by the comparison clock. In other words, it requires higher power consumption and more area. However, thanks to the all pass nature in

the proposed method, the PLL loop bandwidth can be shrunk for jitter without the modulation profile distortion.

The PSDs for the conventional fractional-N SSCG (FN-SSCG) and the two-point SSCG (TPDL-SSCG) in non-spread spectrum mode are illustrated in Fig. 5.6. Only the VCO and the modulator quantization noise are taken into account. The VCO phase noise is assumed as -89 dBc/Hz at the offset frequency of 1 MHz with the shape of f^2. Other simulation parameters are listed in Table 5.1. Two different cases with loop bandwidths of 100 kHz and 300 kHz are studied. A third pole of 4.5 MHz is needed for the FN-SSCG to further filter the quantization noise of the third-order modulator. The center frequency is set at 1500 MHz, the spread ratio is -0.5%, and the modulation frequency is set at 31.25 kHz. The solid and dashed lines represent the total phase noise for the FN-SSCG with a 300 kHz loop bandwidth and TPDL-SSCG with a 100 kHz loop bandwidth, respectively. The contributions from the VCO are denoted by circle and plus marks in different cases. The phase noise from the ΔΣ modulator is denoted by diamond and square marks. Although the in-band phase noise in the proposed TPDL-SSCG with a second order ΔΣ modulator is larger than the case in the FN-SSCG with a third order ΔΣ modulator, the TPDL-SSCG still has enough performance in terms of EMI suppression, modulation profile linearity, and jitter through the following analysis and measurements.

The chip areas for the second-order, and third-order, MASH ΔΣ modulator are evaluated as 3920 and 4887, in units of gate-counts, respectively. The power consumption using the TSMC 0.18 μm process is 1.40 mW and 2.00 mW, respectively. The area is approximately 20% off in digital area and approximately 5% off in whole area, and the power is approximately 4% off in whole power consumption when using the second-order ΔΣ modulator. The 4 to 5% difference is still important because the power and area of the proposed SSCG is only 15.3 mW and 0.21 mm^2, respectively. Hence, in this work, a second-order ΔΣ modulator and a 100 kHz loop bandwidth, with a second-order loop filter, are designed for saving power and area.

Table 5.1 SSCG Simulation Parameters

	FN-SSCG	TPDL-SSCG
Input Frequency	25 MHz	25 MHz
Output Frequency	1500 MHz	1500 MHz
Spread Ratio	-0.5%-0	-0.5%-0
VCO Gain	480 MHz/V	480 MHz/V
Loop Bandwidth	100/300 kHz	100/300 kHz
Modulator	third-order MASH	second-order MASH
Loop filter	third-order	second-order
Third pole frequency	4MHz	N/A

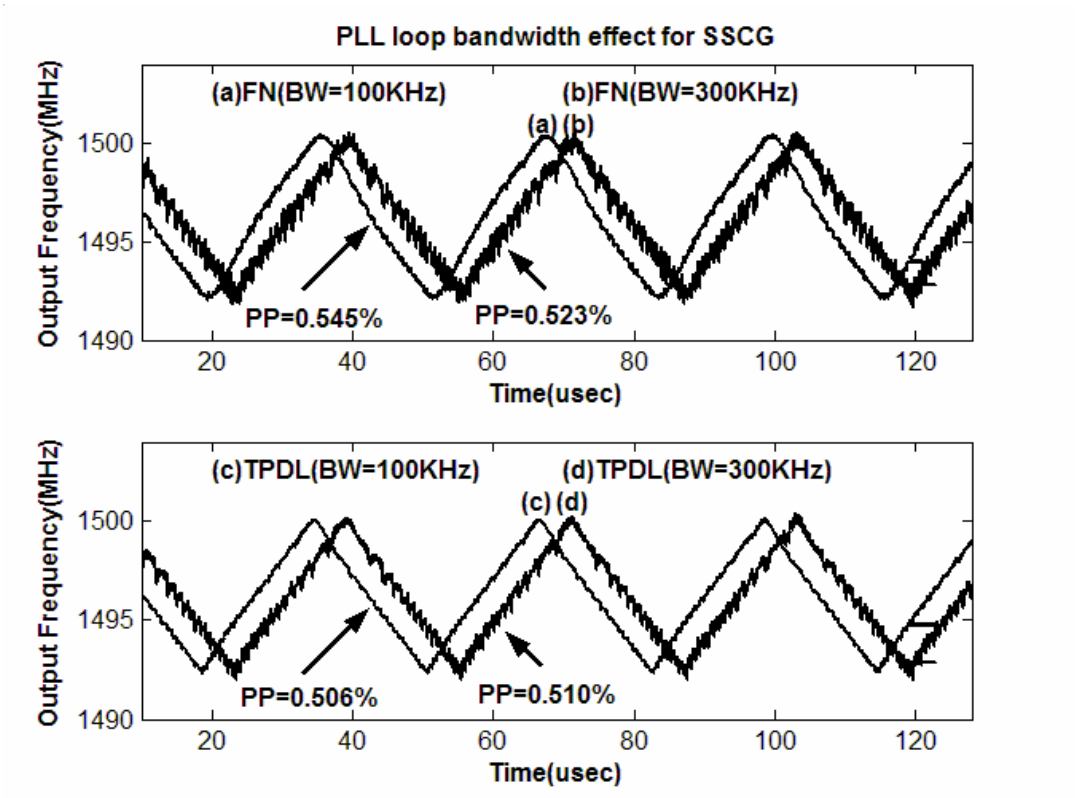


Fig. 5.7. Simulation results for the FN-SSCG and the TPDL-SSCG under different loop bandwidths.

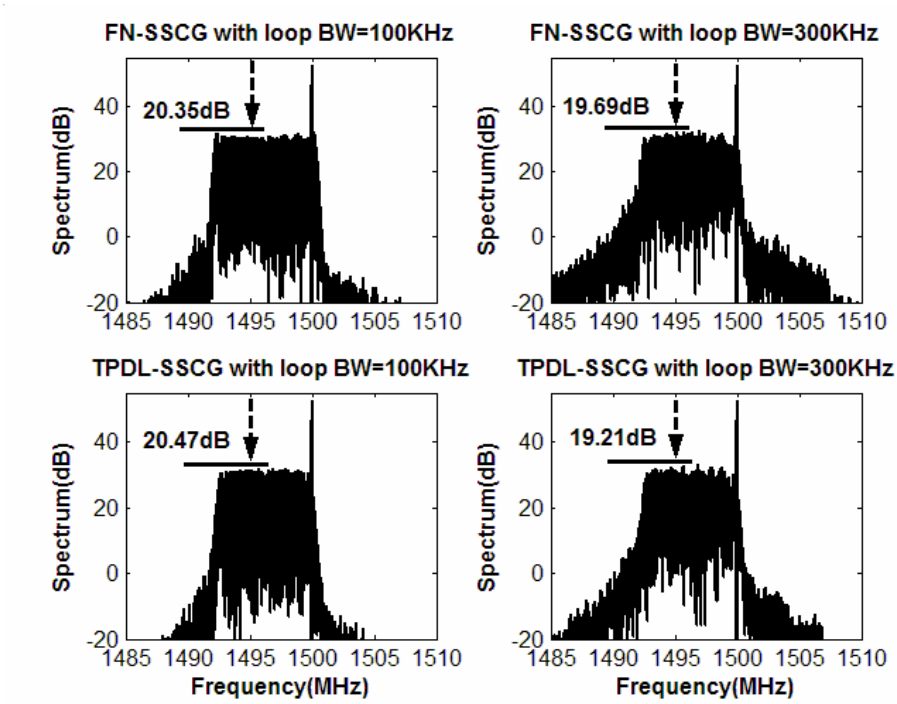


Fig. 5.8 .Spectrum simulation results with the ΔΣ modulator noise for the FN-SSCG and the PDL-SSCG under different loop bandwidths.

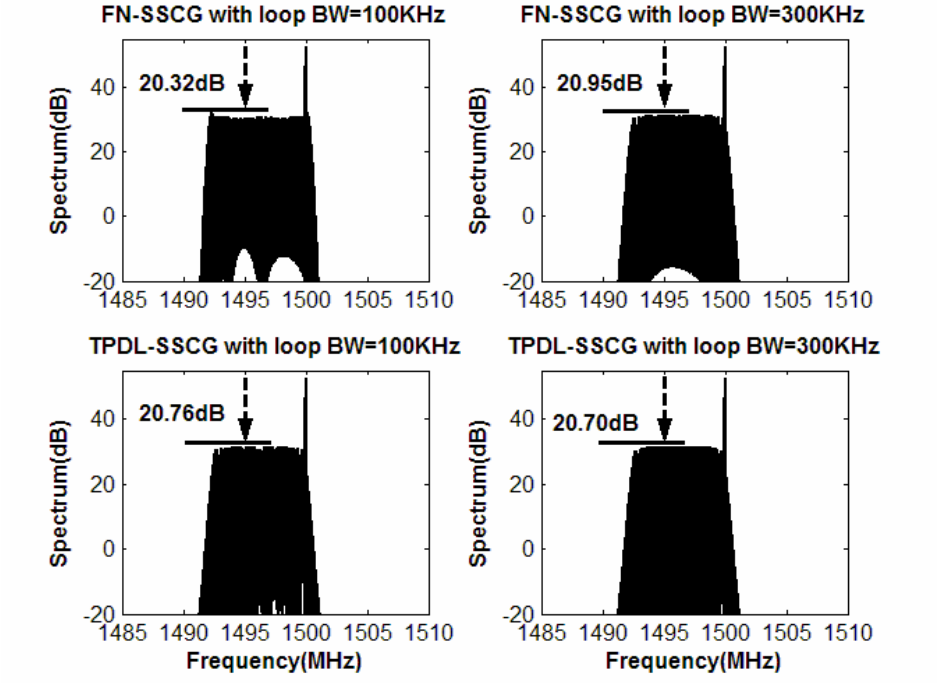


Fig. 5.9. Spectrum simulation results without the ΔΣ modulator noise for the FN-SSCG and the TPDL-SSCG under different loop bandwidths.

5.2.5 Simulation Results

To compare the performance between the FN-SSCG and the TPDL-SSCG, the following simulations are made. The same parameters listed in Table 5.1 are used. The output frequency swings are shown in Fig. 5.7. Four different spread ratios of 0.543%, 0.523%, 0.506%, and 0.510% for the FN-SSCG with a 100 kHz BW denoted curve-a, the FN-SSCG with a 300 kHz denoted curve-b, the TPDL-SSCG with a 100 kHz BW denoted curve-c, and the TPDL-SSCG with a 300 kHz BW denoted curve-d are obtained, respectively. The corresponding spectra results with the ΔΣ modulator noise are shown in Fig. 5.8. The simulated spectra with ΔΣ modulator noise are 20.35 dB, 19.69 dB, 20.47 dB, and 19.21 dB for curve-a, curve-b, curve-c, and curve-d shown in Fig. 5.7, respectively. The simulation results are summarized in Table 5.2. It is known that the larger the spread ratio, the better the EMI performance. To see the efficiency of EMI performance, the EMI reduction and its spread ratio need to be considered simultaneously. Therefore, the ratio of EMI in dB to spread ratios in percentage denoted by EMI_{norm} is also evaluated. The case of the FN-SSCG with a 100 kHz BW has the largest peak-to-peak spread ratio (0.545%) deviation from the ideal value 0.5%, and the smallest EMI efficiency with the value of 37.34 dB/% because the PLL loop bandwidth is not enough that the output could not track the modulation profile and is distorted. Small peaks existed at two ends of the spectrum for the case of the FN-SSCG with a 100 kHz BW, meaning that it is not a good triangular waveform. The case of the FN-SSCG with a 300 kHz BW has better performance in terms of the spread ratio (0.523%) and EMI efficiency (37.65 dB/%) compared to one with a 100 kHz BW. However, it is clearly indicated that the case of the TPDL-SSCG with a 100 kHz BW has not only a more accurate spread ratio (0.506%), but also better EMI efficiency (40.45 dB/%) with respect to the two cases of the FN-SSCG because the case of the TPDL-SSCG with a 100 kHz BW has smaller ΔΣ modulator noise than the case of the FN-SSCG with a 300 kHz BW and utilizes the technique of the two point modulation to faithfully pass the modulation profile. This is also indicated from the spectrum shape that no obvious peaks appeared at the two ends of the spectrum. In addition, there is a 0.023% difference in spread ratios for PLL loop bandwidths changed from 100 kHz to 300 kHz for the FN-SSCG, while there is only 0.003% difference in spread ratios for the TPDL-SSCG. The slight difference between curve (c) and (d) in Fig. 5.7

Table 5.2 SSCG Simulation Summary

	With ΔΣ noise			Without ΔΣ noise
	Spread ratio	EMI	EMI_{norm}	EMI
FN-SSCG (100KHz)	0.545	20.35	37.34	20.32
FN-SSCG (300KHz)	0.523	19.69	37.65	20.95
TPDL-SSCG (100KHz)	0.506	20.47	40.45	20.76
TPDL-SSCG (300KHz)	0.510	19.21	37.67	20.70
UNIT	%-pp	dB	dB/%	dB

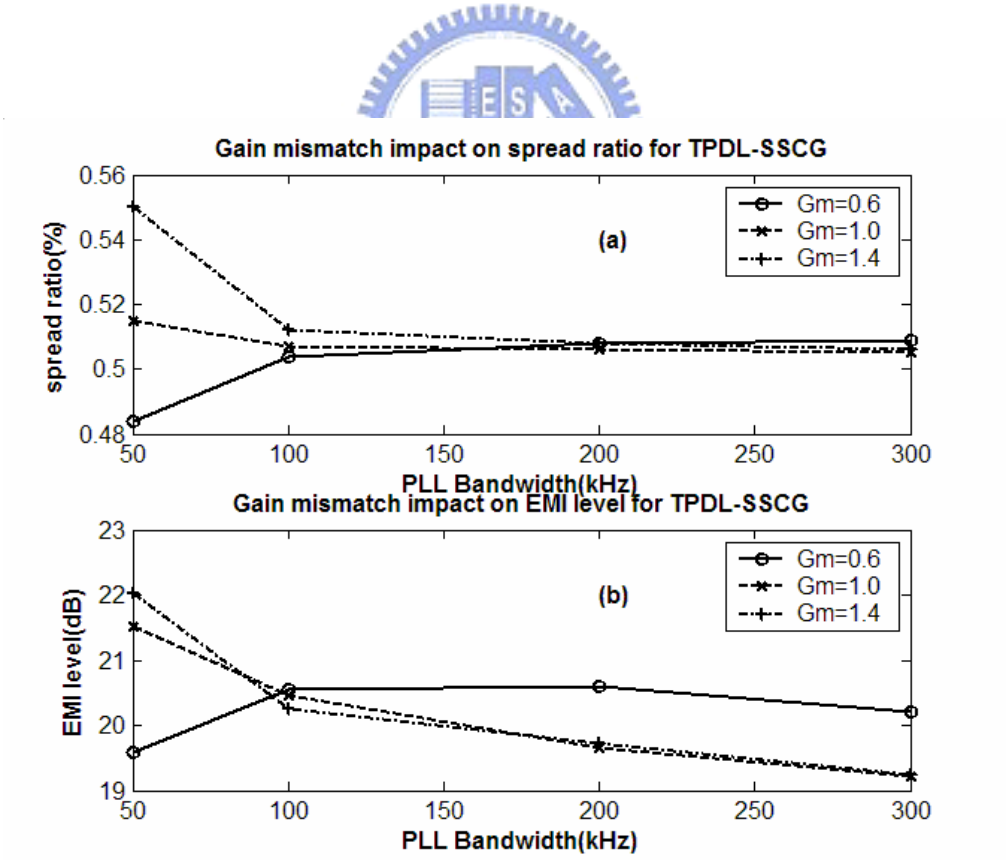


Fig. 5.10. Simulation results for gain mismatch impact on spread ratio for the TPDL-SSCG.

is due to the quantization noise influence. It implies that the effect of bandwidth is of little importance in the proposed modulation.

More effects are illustrated in Fig. 5.7 and 5.8, which show that the bigger loop bandwidth and worse jitter both appeared at the output. The cases with a 300 kHz BW show the bigger instantaneous frequency fluctuations from Fig. 5.7, and the higher noise level from Fig. 5.8, with respect to the cases with a 100 kHz BW in both architectures. This confirms the results in (5.14). The proposed TPDL-SSCG has the advantage of low distortion, so that the modulation profile is more like a triangular wave, and can improve the linearity of the modulation profile and the EMI performance at the same time.

In order to deeply investigate the jitter effect on the EMI suppression level, the spectra simulation without the ΔΣ modulator noise for FN-SSCG and TPDL-SSCG under the same case as in Fig. 5.7 and Fig. 5.8 are drawn in Fig. 5.9. The simulation results are also summarized in Table 5.2. The simulated spectra without the ΔΣ modulator noise are 20.32 dB, 20.95 dB, 20.76 dB, and 20.70 dB for the FN-SSCG with a 100 kHz BW, the FN-SSCG with a 300 kHz BW, the TPDL-SSCG with a 100 kHz BW, and the TPDL-SSCG with a 300 kHz BW, respectively. It shows a 1.26 dB (=20.95-19.69) EMI degradation for the case of FN-SSCG with a 300 kHz BW when the ΔΣ modulator noise is taken into consideration; while it is 1.49 dB (=20.70-19.21) for the case of TPDL-SSCG with a 300 kHz BW. It is clearly to seen that there is only 0.29 dB (=20.76-20.47) impact on EMI performance for the case of TPDL-SSCG with a 100 kHz BW. Therefore, the random jitter introduced by the modulator has a deteriorating effect on EMI suppression levels.

The impacts of the gain mismatch on spread ratios and the EMI performance are verified. The cases for G_m=0.6, G_m=1.0 and G_m=1.4 are simulated under different PLL loop bandwidths. The impacts on spread ratios are shown in Fig. 5.10(a). When the PLL loop bandwidth is smaller than 100 kHz, the spread ratio is very sensitive to the gain mismatch between the two points. When the PLL loop bandwidth is larger than 100 kHz, the spread ratio variation is small. The impacts on the EMI performance are shown in Fig. 5.10(b). When G_m =1.0 or G_m=1.4, the higher the PLL loop bandwidth has, the worse the EMI performance is. When G_m=0.6, the EMI performance is less related to the PLL loop bandwidth. In addition, the EMI variation is sensitive to the gain mismatch when the PLL

loop bandwidth is smaller than 100 kHz. The reason for gain mismatch effects on the proposed SSCG is described below. One can rewrite (5.11) as

$$\Delta\omega_{out} = T(s)\Delta\omega_{sig} + \left(1 - T(s)\right) \times G_m \Delta\omega_{sig} \tag{5.16}$$

The first term in (5.16) is contributed by the modulation of divider and the second term is contributed by the modulation of the VCO. When the loop bandwidth is quite low, the output is dominated by the second term in (5.16), meaning that the spread ratio is sensitive to gain mismatch. In other words, when the loop bandwidth is quite high, the output is dominated by the first term in (5.16), meaning that the spread ratio is less sensitive to gain mismatch. But, it is noted from the above analysis that the EMI performance will be degraded once the loop width is large due to the quantization noise of the modulator. Therefore, if the gain mismatch is small, one can lower the bandwidth to achieve the desired performance according to the above analysis. If the gain mismatch is high as, or more than 0.4, one needs to tradeoff the loop bandwidth with the performance. Thus, in order to reduce the effect of gain mismatch, one can choose an appropriate loop bandwidth to let the first and the third Fourier frequencies of the triangular waveform to be passed through the divider path and to let the fifth and higher Fourier frequencies to be passed through the VCO path. This approach makes the output waveform dominated by the divider modulation path and aided by the VCO modulation path. A rule of thumb of 3 times of the modulation frequency can be the target loop bandwidth. Thus, the 100 kHz loop bandwidth is adopted in this work.

From (5.2), since C_1 is varied within 5% and I_{p3} is varied within 15% in the typical CMOS process, the gain mismatch is mainly contributed by K_{vco}. Therefore, the VCO with low sensitivity to VCO gain is needed. In this work, K_{vco} is varied about +/-30% over process, voltage, and temperature variation. It means G_m is changed about from 0.7 to 1.3. From the above simulation results, the gain mismatch impact on spread ratio with will be varied about 0.008% and the gain mismatch impact on EMI performance is about 0.23 dB. Moreover, the VCO calibration technique in [24] can be used to further improve the performance.

In short, the advantages of the proposed TPDL-SSCG are remarkable. First, a lower order ΔΣ modulator can be used for lower power consumption. Second, the lower order loop filter can be used for a smaller chip area. Third, the linear modulation profile, and small ΔΣ modulator noise can be optimized simultaneously.

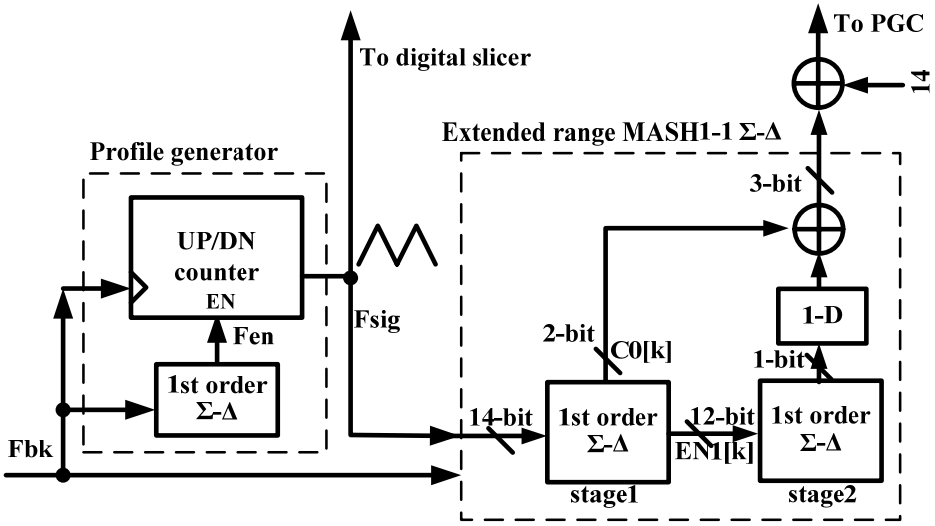


Fig. 5.11. Block diagram of the proposed profile generator and ΔΣ modulator.

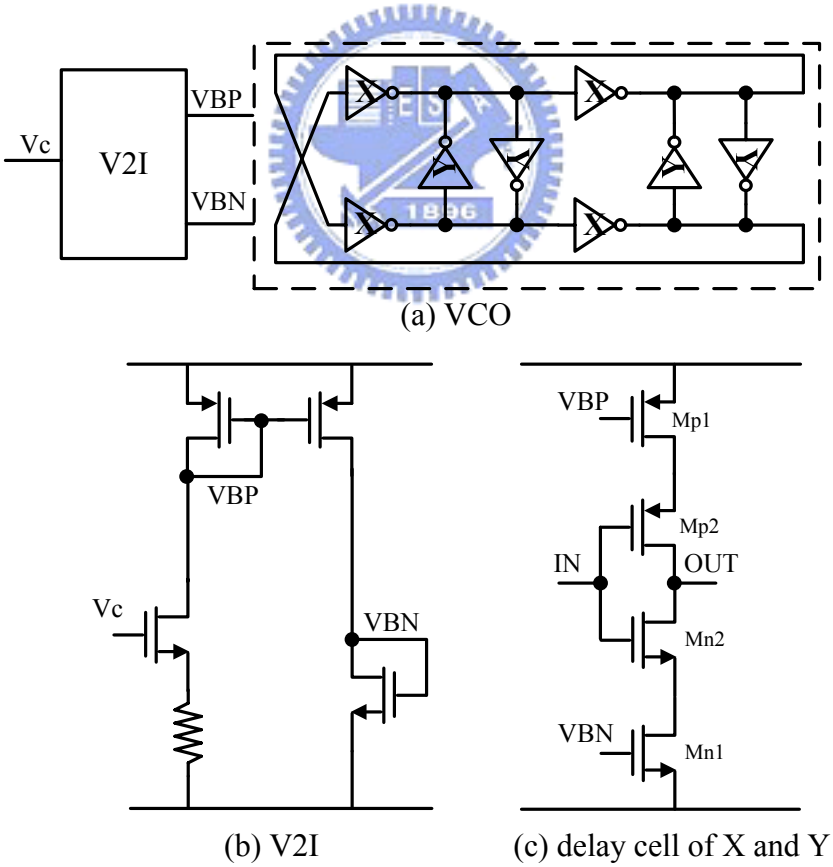


Fig. 5.12. VCO circuits.

5.3 Circuit Descriptions

The block diagram of the proposed profile generator and ΔΣ modulator is shown in Fig. 5.11. The input range of the ΔΣ modulator must fulfill the requirement of 0 to -5000 ppm spread ratio. Accordingly, the fractional number is varied between 0.925 and 1. A MASH type ΔΣ modulator has an input range of less than 1 and cannot be used in this application. To eradicate this issue, a new version of the MASH-1-1 ΔΣ modulator, with extended input range, is used to overcome the overflow problem in the modulator [23]. Stage 1 has two carry bits while stage 2 only has one carry bit. The two-bit carry outputs cause inputs larger than, or equal to, 1 to quickly pass the integer part of the input to the output, and will not saturate the following stages. The advantages of this design are unconditional stability, and small area similar to the conventional MASH-1-1 ΔΣ modulator. In addition, this circuit has approximately 3 times the input range of the conventional MASH-1-1 ΔΣ modulator.

The profile generator consists of an up/down counter and a first-order ΔΣ modulator [39]. Although the clock input shown is f_{bk}, the actual operating frequency of the up/down counter is f_{cnt}, which is determined from the spread ratio of δ, the modulation frequency of f_{sig}, and the bit number of the MASH-1-1 ΔΣ modulator (B) as described by

$$f_{cnt} = \frac{f_{out}}{4 f_{bk}} \times 2 \times \delta \times 2^{B} \times f_{sig} . \tag{5.17}$$

Therefore, an extra first-order ΔΣ modulator is added to generate the additional enable signal, fen to lower the operation frequency of the up/down counter, as shown in Fig. 5.11. The relationship between f_{cnt} and f_{en} is $f_{cnt}=f_{en}$ AND f_{bk}. In this study, f_{out} is 1.5 GHz, f_{sig} is 31.25 kHz, and δ is 0.5% to meet SATA specifications. In addition, B=12 and f_{bk}=25 MHz. One can calculate that f_{cnt}=19.2 MHz.

Fig. 5.12 shows the schematic of VCO used in this work [41]-[42]. It is composed of four current starved inverters (denoted by X) as delay cells, two pairs of cross-coupled current starved inverters (denoted by Y), and a voltage to current converter (V2I). The detailed circuit of the V2I is shown in Fig. 5.12(b), and the inverters of X and Y are shown in Fig. 5.12(c). This simple architecture is selected for its large signal swing, which allows better phase noise performance and large tuning range. The cross-coupled inverters have two

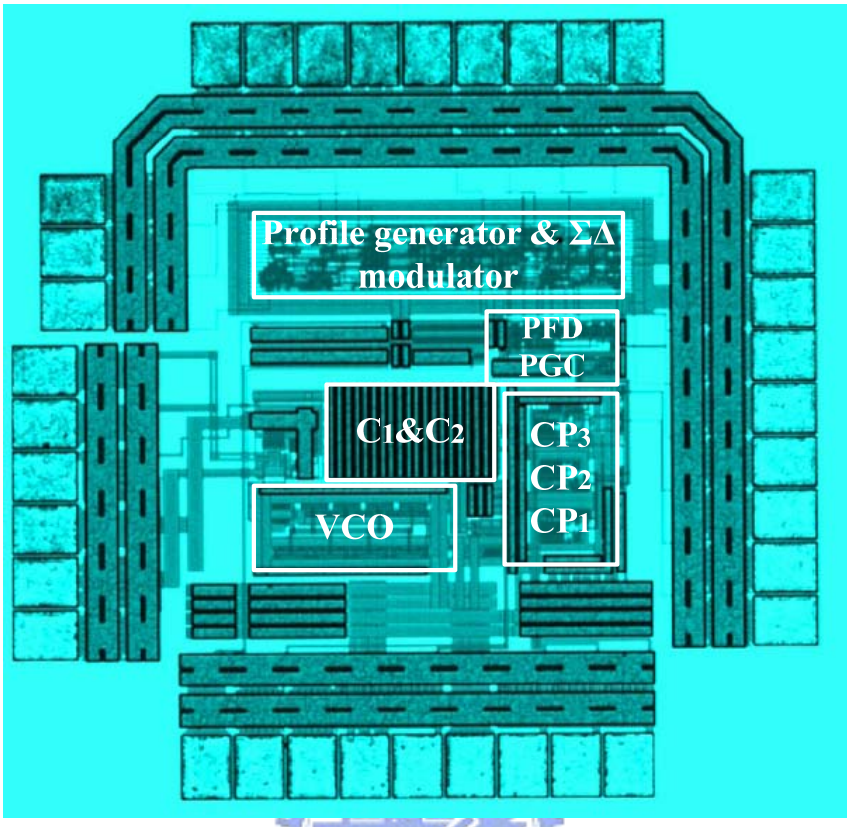
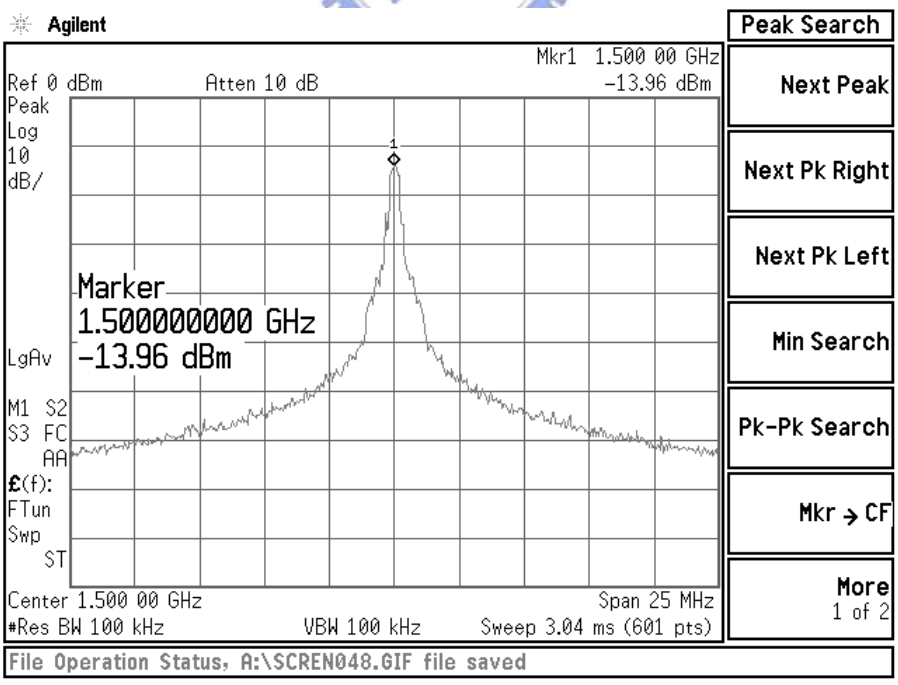
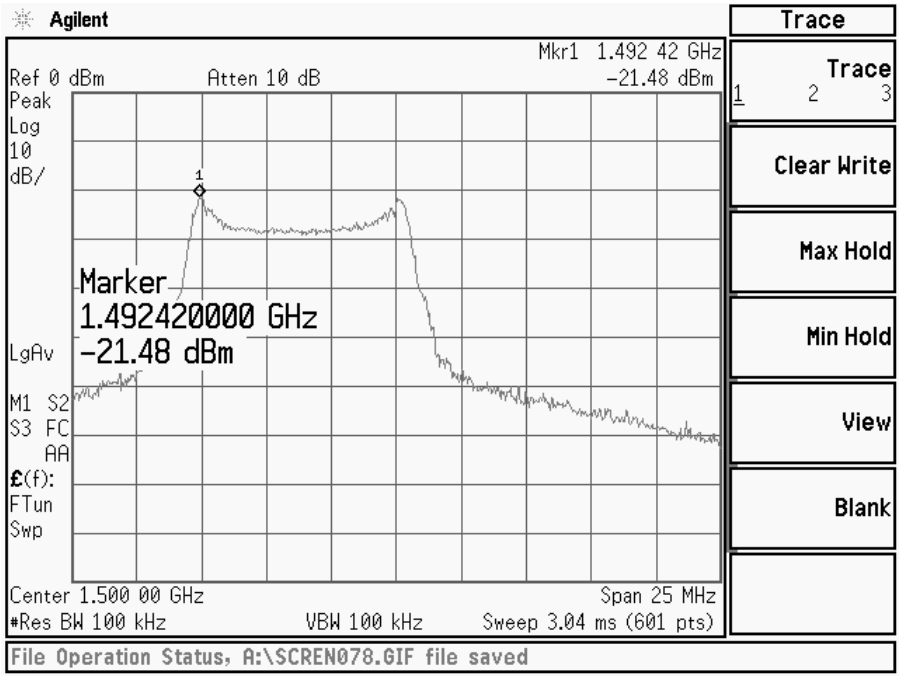


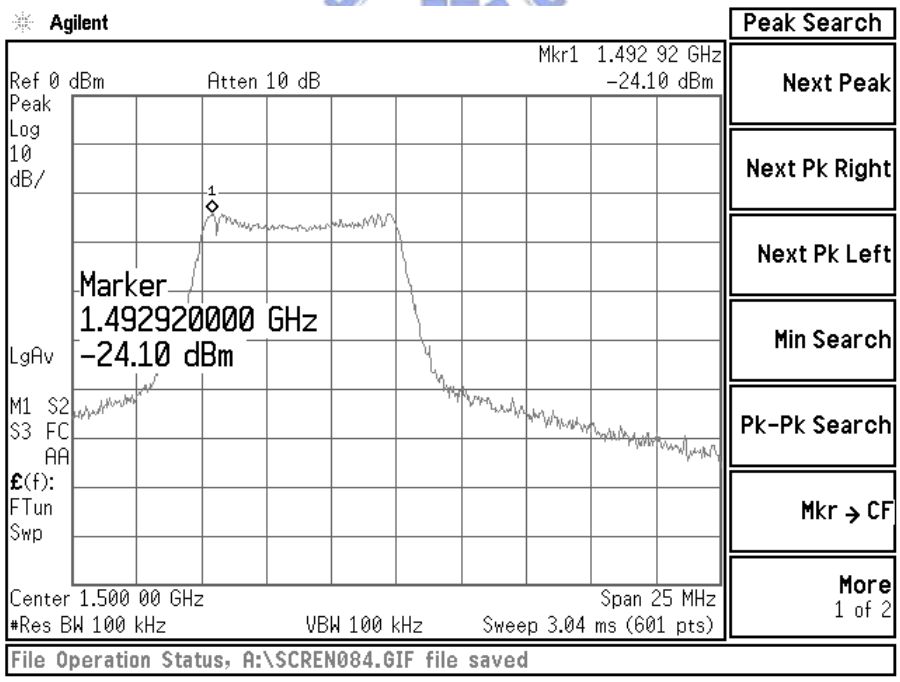
Fig. 5.13. Die photograph of the proposed TPDL-SSCG.



(a)

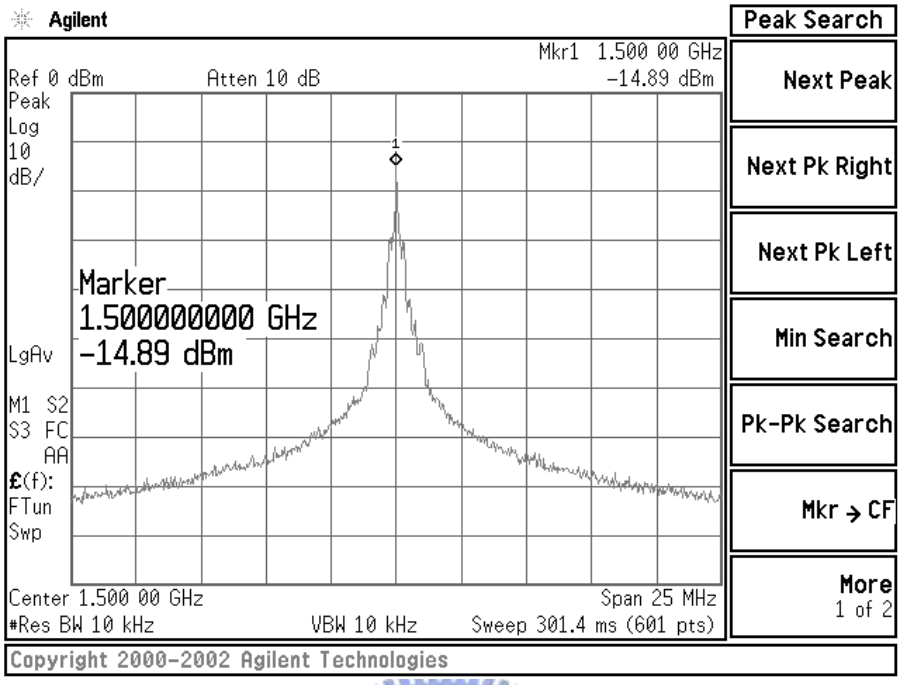


(b)

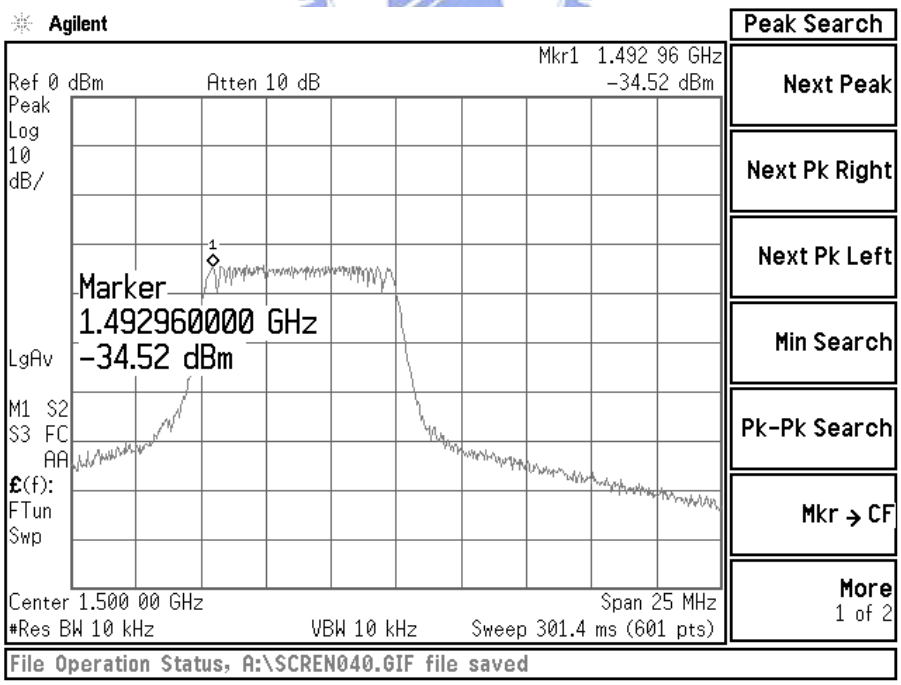


(c)

Fig. 5.14. Measured spectra (a) at non-spread spectrum mode, (b) of the conventional FN-SSCG, and (c) of the proposed TPDL-SSCG.
Measurement condition: RBW= 100 kHz, VBW= 100 kHz and Peak-Hold mode.



(a)



(b)

Fig. 5.15. Measured spectra for the TPDL-SSCG (a) with SSC-off (b) with SSC-on Measurement condition: RBW=10 kHz, VBW= 10 kHz and Peak-Hold mode.

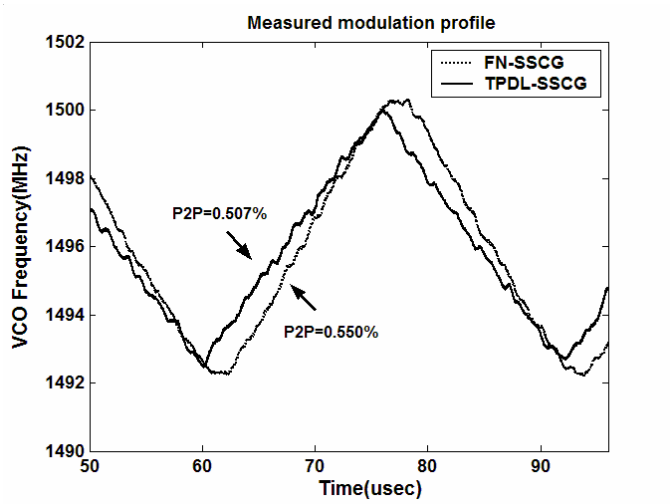
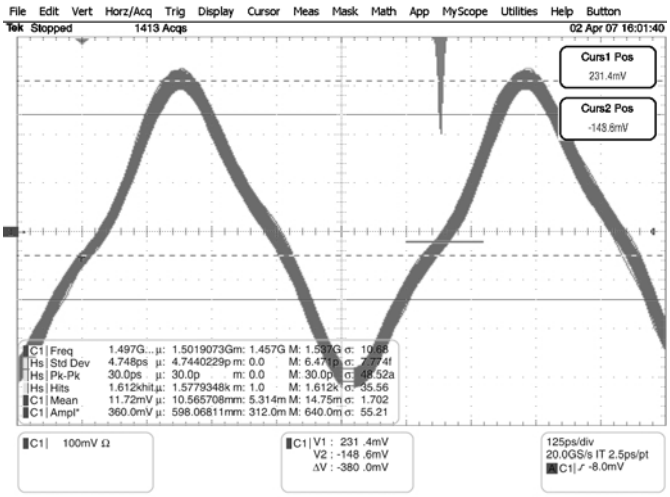
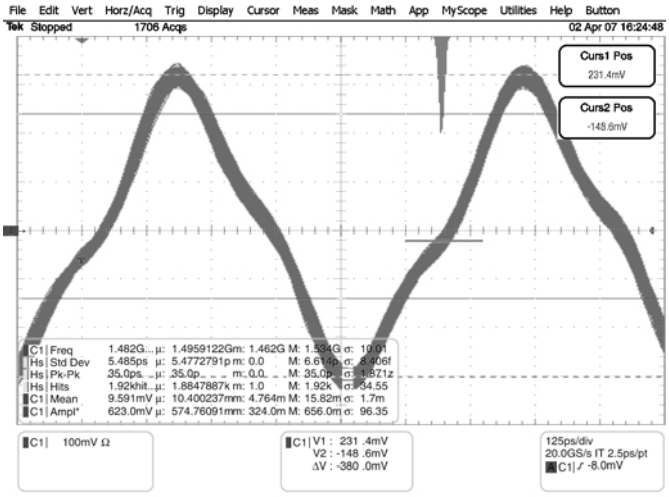


Fig. 5.16. Measured modulation profile in time domain.



(a)



(b)

Fig. 5.17. Measured jitter for the TPDL-SSCG (a) with SSC-off, (b) with SSC-on.

functions: One is to provide negative impedance to mandate the phase delay in each inverter at 90 degrees, and the other is to allow the VCO to operate pseudo-differentially to obtain better PSRR. In other words, the VCO is a two-stage differential type. The size of inverter Y is suggested to be more than 0.5 times of size of inverter X to maintain oscillation [41]. Here, the factor is 0.7 times to allow a higher oscillation frequency than that of the 3-stage single-ended ring oscillator [41] because it has an additional coupling path from the cross coupled inverters with reduced delay time. Therefore, the power consumption can be relaxed for a given frequency. Moreover, unlike a singled-ended ring oscillator, which produces a distorted triangular waveform output, this topology produces a sinusoidal output, and a more symmetrical waveform, to get better phase noise performance [43]. To further minimize the phase noise, a low VCO gain of 480 MHz/V is chosen to lower the phase noise due to the noise coupling to the VCO input node. The noise of the V2I is also a main contributor to the phase noise. Therefore, the size of the V2I is the same as that in inverter X to lower the up-conversion noise from the bias circuit. The measured phase noise at 1 MHz offset frequency is -89 dBc with a power consumption of 3 mA.

5.4 Measurement Results

The proposed SSCG is designed and fabricated by TSMC 0.18 μm CMOS process. The die photograph is shown in Fig. 5.13. The active area is 0.42×0.48 mm^2. The output spectra without spreading, with spreading, using the conventional FN-SSCG, and with spreading using the TPDL-SSCG are shown in Fig. 5.14(a), (b), and (c), respectively. The resolution bandwidth (RBW) is set to 100 kHz to meet SATA specifications [35]. A second-order loop filter and a PLL bandwidth close to 100 kHz are chosen for both Fig. 5.14(b) and (c). The second-order extended range MASH ΔΣ modulator is adopted for both Fig. 5.14(b) and (c). In other words, the conventional FN-SSCG is obtained just by switching off the path of the VCO modulation. The EMI reduction is approximately 7.52 dB for the conventional FN-SSCG and is approximately 10.14 dB for the TPDL-SSCG. The proposed SSCG has 2.62

dB improvements in EMI reduction. In order to compare with the simulation results, the RBW needs to be smaller than the modulation frequency [40]. Therefore, the spectra for the TPDL-SSCG, with SSC off and on using 10 kHz RBW, are measured and shown in Fig. 5.15(a) and (b), respectively. The measured EMI reduction is 19.63 dB and is close to the simulation results of 20.47 dB. No peak is appeared in Fig. 5.15(b), which indicates the modulation profile is nearly a triangular waveform.

It is difficult to determine the real peak-peak spread ratio and the shape of the triangular modulation in the frequency domain. Therefore, the time domain modulation profile is verified in Fig. 5.16. The solid line and dashed line represent the profile of the proposed TPDL-SSCG and the profile of conventional FN-SSCG, respectively. The measured spread ratios are 0.55% and 0.507% for the conventional FN-SSCG and the TPDL-SSCG, respectively. The measured spread ratio of the TPDL-SSCG is very close to the simulation results listed in Table 5.2. The measured modulation profile for the conventional FN-SSCG looks like a distorted triangular waveform due to the insufficient PLL loop bandwidth; therefore, the EMI performance is bad. The measured jitter, using a self-triggered method under different condition, is shown in Fig. 5.17. The measured rms jitter is 4.748 ps and 5.485 ps at SSC-off and SSC-on, respectively. The measured peak-to-peak jitter is 30 ps and 35 ps at SSC-off and SSC-on, respectively. Only a 0.737 ps rms jitter is increased when the TPDL-SSCG is active, which is very close to the theoretical estimation of 0.556 ps (=0.5%/1500MHz/6). Therefore, the rms jitter caused by non ideality of the circuits (mostly from the ΔΣ modulator) is only 0.181 ps. The power consumption with and without an output buffer is 15.3 mW and 27 mW, respectively. The lower power consumption is achieved due to the low power VCO and the low order ΔΣ modulator. Table 5.3 summaries the performance of the proposed TPDL-SSCG and compares with previous works. In Table III, the EMI reduction amounts are compared for the 100 kHz RBW. Note that the proposed TPDL-SSCG results in smaller area, lower power consumption and better peak-to-peak jitter performance. The EMI performance is comparable to other works.

Table 5.3 Performance Summary

	This work	[9]	[13]	[15]	Spec.	Unit
Modulation method	Two-point	ΔΣ	ΔΣ	Phase interpolation	N/A	N/A
EMI reduction	10.14	10	9.8	5.43	>7	dB
Modulation frequency	31.25	31.1	30	31.6	30-33	kHz
PLL loop BW	100	300	N/A	N/A	N/A	kHz
RMS jitter (SSC-on)	5.485	8.1	3.24	N/A	N/A	ps
Peak-Peak jitter (SSC-on)	35.0	N/A	58.3	N/A	N/A	ps
Spread ratios	0.507	0.535	0.5	0.37	0.535	%
Technology	0.18	0.15	0.18	0.15	N/A	μm
Chip Area (active)	0.21	0.42	0.31	N/A	N/A	mm^2
Power consumption	15.3/27*	54	77	N/A	N/A	mW

*15.3 mW measured without an output buffer and 27 mW measured with an output buffer

5.5 Summary

In this work, a new SSCG architecture with two point modulation is presented. The PLL bandwidth is effectively expanded to improve the modulation waveform. The spread ratio can be finely controlled by a simple DAC. The most important success is the usage of the second order ΔΣ modulator and the second order dual-path loop filter, which remarkably reduce power consumption and chip area without the jitter penalty. In addition, the total integration is realized without using an external loop filter or a high resolution DAC. The clock rate of 1.5 GHz with a down spread ratio of 0.5% is achieved. The jitter at SSC-on is 5.485 ps-rms and 35 ps-pp with only a 0.737 ps-rms jitter attributed from spread spectrum clocking. The improvement in EMI reduction is better than 2.62 dB with respect to a conventional one-point implementation.

CHAPTER 6

Conclusions

There are four new developed SSCGs presented in this thesis. We use three different topologies for these SSCGs. First of all, the fractional-N based SSCG with an extended input range MASH ΔΣ modulator is proven to have 3 times input range more than the conventional MASH ΔΣ modulator. The proposed modulator solves the issue that the conventional MASH ΔΣ modulator will be malfunctioned when the fractional part of divider exceeds its input range. From the analysis, the proposed modulator can achieve 9% spread ratio; while it is only 0.23% spread ratio for the conventional one. The cost of the proposed modulator is only two extra input bits and one extra carry bit in the first stage modulator. The proposed SSCG has been implemented in TSMC 0.35 μm double-poly quadruple-metal CMOS process. Measurement results are in good agreements with the predictions. These results can be further applied to variable system with spread spectrum clocking.

Next, the VCO modulated based SSCG with a compact dual-path loop filter has been fabricated in TSMC 0.35 μm double-poly quadruple-metal CMOS process. The triangular waveform is realized with a particular charge pump combined in the dual-path loop filter. The advantage of the proposed SSCG is to save enormous chip area and make the generation of the triangular waveform more flexible than the conventional VCO modulated based SSCG. The whole capacitor is about 1.01 nF, which is an order less than the conventional SSCG, to make this SSCG totally integrated. The phase noise of the proposed SSCG is intensively analyzed including the non-ideality of the dual-path loop filter. The modulation effects of the SSCG are carefully studied through the determination of zero, loop bandwidth, modulation frequency, pole, and comparison clock. The measurement results are mostly as predicted.

Third, the new two-point modulation based SSCG has been realized in TSMC 0.35 μm double-poly quadruple-metal CMOS process. The all-pass feature of the two-point modulation scheme de-couples the interrelation between the quantization noise influences of the ΔΣ modulator and the modulation profile linearity. The loop bandwidth can be shrunk to reduce the impact of the ΔΣ modulator and the modulation waveform is still appeared at the

output with good linearity and EMI performance. A robust and simple DAC structure combined with the two-path loop filter has been proposed to eliminate the delay mismatch between two modulation paths to make this technique more attractive to applications of SSCG. The area and power consumption are reduced because a second-order ΔΣ modulator is adopted instead of a third-order ΔΣ modulator in a conventional scheme. A 0.55 dB improvement in EMI suppression has been achieved when compared with a conventional scheme. The simulation time is greatly reduced with the proposed almost S-domain Matlab model, in which the effects of the quantization noise of the ΔΣ modulator and the impact of the VCO phase noise are taken into consideration. The VCO phase noise shows minor impact on the EMI performance; while the quantization noise has big degradation on the EMI performance.

Fourth, a low power and high precision SSCG for SATA applications using two point modulation schemes is developed in TSMC 0.18 μm CMOS process. Accompanying the feature of the two-point modulation, a low jitter SSCG with a high precision spread amount is accomplished. The area is only 0.21 mm^2 and the power consumption is only 15.3 mW resulting from the adoption of a modified dual-path loop filter and a second-order ΔΣ modulator. The EMI reduction is 10.14 dB on 100 kHz RBW, fulfilling the 7 dB requirement in SATA specification and it reveals 2.62 dB improvements with respect to a conventional implementation.

Finally, Table 6.1 summaries the features and the suitable applications of the proposed SSCGs.

Table 6.1 Features and Suitable Applications of Proposed SSCGs

	Chapter 2	**Chapter 3**
Modulation method	ΔΣ	VCO
Problems Solved	Modulator input range	Large Area
Features	Wide spread ratio Wide input range modulator Wide frequency range	Fully integrated Small capacitor area
Suitable Applications	PC, Notebook, FAX, Printer and LCD TV, other SSCGs	PC, Notebook, FAX, Printer and other SSCGs
	Chapter 4	**Chapter 5**
Modulation method	Two-point	Two-point
Problems Solved	High ΔΣ order	High ΔΣ order
Features	High accurate spread ratio Low jitter Low EMI	High accurate spread ratio Low jitter Low EMI High speed
Suitable Applications	PC, Notebook, FAX, Printer, LCD TV, other SSCGs	HDMI, and other high speed SSCGs

Bibliography

[1] C. R. Paul, “Introduction to Electromagnetic Compatibility”, John Wiley Interscience, New York, 1998, Ch 2.

[2] K. B. Hardin, J. T. Fessler, and D. R. Bush, “Spread-spectrum clock generation for the reduction of radiated emissions,” in *Proc. IEEE Int. Symp. Electromagnetic Compatibility*, 1994, pp. 227–231.

[3] H. H. Chang, I. H. Hua, and S. I. Liu, “A Spread-spectrum clock generator with triangular modulation,” *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp.673-676, April 2003.

[4] H. S. Li, Y. C. Cheng, and D. Puar, “Dual-loop spread-spectrum clock generator,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1999, pp. 184–185.

[5] Y. Moon, D. K. Jeong, and G. Kim, “Clock dithering for electromagnetic compliance using spread-spectrum phase modulation,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1999, pp. 186–187.

[6] H. Mair and L. Xiu, “An architecture of high-performance frequency and phase synthesis,” *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 835–846, June 2000.

[7] H. W. Chen and J. C. Wu, “A spread-spectrum clock generator for EMI reduction,” *IEICE Trans. Electron.*, vol. E84-C, no. 12, pp. 1959–1966, Dec. 2001.

[8] J. Y. Michel and C. Neron, “A frequency modulated PLL for EMI reduction in embedded application,” in *Proc. IEEE Int. ASIC/SOC Conf.*,1999, pp. 362–365.

[9] M. Kokubo, T. Kawamoto, T. Oshima, T. Noto, M. Suzuki, S. Suzuk,T. Hayasaka, T. Takahashi, and J. Kasai, “Spread-spectrum clock generator for serial ATA using fractional PLL controlled by ΔΣ modulator with level shifter,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 160–161, Feb., 2005.

[10] J. Lee, and B. Kim, “A low-noise fast-lock phase-locked loop with adaptive bandwidth control”, *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp.1137-1145, August 2000.

[11] M. H. Perrott, T. L. Tewksbury III, and C. G. Sodini, "A 27-mW CMOS fractional-N

synthesizer using digital compensation for 2.5-Mb/s GFSK modulation," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 2048 - 2060, December 1997.

[12] W. Rhee, B. S. Song, and A. Ali, "A 1.1-GHz CMOS fractional-N frequency synthesizer with a 3-b third-order ΔΣ modulator," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 10, pp. 1453 - 1460, October 2000.

[13] H. R. Lee, Ook Kim, Gijung Ahn, and D. K. Jeong, "A low-Jitter 5000 ppm spread spectrum clock generator for multi-channel SATA transceiver in 0.18 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp.162–163, Feb. 2005.

[14] T. Yoshikawa, T. Educhi, Y. Arima, and T. Iwata, "A spread spectrum clock generator using digital tracking scheme," *IEICE Trans. Electron.*, vol. E88-C, no. 6, pp. 1288-1289, June 2005.

[15] M. Aoyama et al., "3 Gb/s, 5000 ppm spread spectrum SerDes PHY with frequency tracking phase interpolator for Serial ATA," *Symp. VLSI Circuits*, pp. 107-110, June, 2003.

[16] C. C. Chen, S. C. Lee, and S. I. Liu, "A spread-spectrum clock generator using a capacitor multiplication technique," in *Emerging Information Technology Conference*, pp. 43-46, Aug. 2005,

[17] H. Y. Huang, S. F. Ho and L. W. Huang, "A 64-MHz~1920-MHz programmable spread-spectrum clock generator," *IEEE International Symposium on Circuit and Systems*, pp.3363-3366, 2005.

[18] Y. Koo, H. Huh, Y. Cho, J. Lee, J. Park, K. Lee, D.K. Jeong, and W. Kim, "A fully integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and cellular-CDMA wireless systems", *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp.536-542, May 2002.

[19] Chi-Wa Lo; Luong, H.C, "A 1.5-V 900-MHz monolithic CMOS fast-switching frequency synthesizer for wireless applications", *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp.459-470, April 2002.

[20] De Muer, B.; Steyaert, M.S.J.; "A CMOS monolithic ΔΣ-controlled fractional-N frequency synthesizer for DCS-1800", *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp.835-844, July 2002.

[21] A. Young, J. K. Greason, and K. L. Wong, "A PLL clock generator with 5 to 110 MHz of lock range for microprocessors," *IEEE J. Solid-State Circuits*, vol. 27, no. 11, pp. 1599-1607, Nov. 1992.

[22] W. T. Chen, J. C. Hsu, H. W. L, and C. C. Su, "A spread spectrum clock generator for SATA-II," *IEEE Int. Symp. on Circuits and Systems*, May. 2005, pp. 2643–2646.

[23] Y. B. Hsieh and Y. H. Kao, "A spread-spectrum clock generator using fractional-N PLL with an extended range ΔΣ modulator," *ICICE Trans. Electron*., vol. E-89C, no 6, pp. 851-857, June 2006.

[24] T. Kawamoto, et al., "Low-jitter and large-EMI-reduction spread-spectrum clock generator with auto-calibration for serial-ATA applications," in *Proc. IEEE CICC*, Sep. 2007, pp. 345-348.

[25] Y. B. Hsieh and Y. H. Kao, "A fully integrated spread spectrum clock generator using two-point ΔΣ Modulation," I*EEE Int. Symp. on Circuits and Systems*, May. 2007, pp. 2156-2159.

[26] Y. H. Kao and Y. B. Hsieh, "A high performance spread spectrum clock generator using two-point modulation scheme," *IEICE Trans. Electron.*, to be published.

[27] Y. H. Kao and Y. B. Hsieh, "A fully integrated spread spectrum clock generator using a dual-path loop filter," in *49th IEEE MWSCAS*, Aug. 2006, pp. 7-10.

[28] Y. B. Hsieh and Y. H. Kao, "A fully integrated spread spectrum clock generator by using direct VCO modulation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, to be published.

[29] K. C. Peng, C. H. Huang, C. J. Li, and T. S. Horng, "High-performance frequency-hopping transmitters using two-point delta–sigma modulation," *IEEE Trans. Microwave Theory and Tech.*, vol. 52, no. 11, pp. 2529–2535, Nov. 2004.

[30] S. Pavan, Y. Tsividis, and K. Nagaraj, "Modeling of accumulation MOS capacitors for analog design in digital VLSI processes," *Proc. IEEE Int. Symp. Circuits and Systems*, pp. 202–205, June 1999.

[31] B. Leung, "VLSI for Wireless Communication, Prentice Hall," Chap. 7, p.271, Prentice Hall, New Jersey, 2002.

[32] B. D. Muer, and M. S. J. Steyaert, IEEE "On the analysis of fractional-N frequency synthesizers for high-spectral purity," *IEEE J. Solid-State Circuits*, vol. 50, no. 11,

pp.784-793, November 2003.

[33] Using Simulink Version 5. Natick, MA: The Mathworks Inc., Jul. 2002.

[34] K. Kunderl, “Modeling and simulation of jitter in PLL frequency synthesizers,” Available from www.designers-guide.com, Sep. 2005.

[35] Serial ATA International Organization, ”Serial ATA Revision Specification 2.5,” August, 2005.

[36] M. Kokubo, et al., “Spread-spectrum clock generator for serial ATA with multi-bit ΔΣ modulator-controlled fractional PLL,” *ICICE Trans. Electron.*, vol. E-89C, pp. 1682-1688, Nov. 2006.

[37] Y. Moon, G. Ahn, H.Choi, N. Kim, and D. Shim, “A quad 6 Gb/s multi-rate CMOS transceiver with TX rise/fall-time control,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2006.

[38] Y. B. Hsieh and Y. H. Kao, “A new spread spectrum clock generator for SATA using double modulation schemes,” in *Proc. IEEE CICC*, Sep. 2007, pp. 297-300.

[39] D. S. Kim and D. K. Jeong, “A spread spectrum clock generation PLL with dual-tone modulation profile,” *in Symp. VLSI Circuits Dig. Tech. Papers*, 2005, pp. 96–99.

[40] J. Kim, D. G. Kam, P. J. Jun, and J. Kim, “Spread spectrum clock generator with delay cell array to reduce electromagnetic interference,” *IEEE Trans. Electromagnetic Compatibility*, vol. 47, no. 4, pp. 908–920, Nov. 2005.

[41] K. H. Kim et al., “A 20-Gb/s 256-Mb DRAM with an inductorless quadrature PLL and a cascaded pre-emphasis transmitter,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, pp. 127 - 134, January 2006.

[42] D. A. Badillo, and S. Kiaei, “A low phase noise 2.0 V 900 MHz CMOS voltage controlled ring oscillator,” *Proc. IEEE Int. Symp. on Circuits and Systems,* vol. 4, pp. IV-533-536, May 2004.

[43] A. Hajimiri, S. Limotyrakis, and T.H. Lee, “Jitter and phase noise in ring oscillators,” *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 790 - 804, January 1999.

[44] Y. H. Kao and Y. B. Hsieh, “A wide input-range ΔΣ modulator for applications to spread-spectrum clock generator,” in *Proc. IEEE APCCAS*, Dec. 2006, pp. 530-533.

[45] L. Y. Chang, “A spread spectrum clock generator based on a sigma-delta modulated

phase-locked loop," M.S. thesis, Graduate Institute of Electronics Engineering, National Taiwan University, June 2003.

[46] S. Damphousse, K. Ouici, A. Rizki, and M. Mallinson, "All digital spread spectrum clock generator for EMI Reduction," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 1, pp. 145 - 150, January 2007.

[47] M. Kokubo, et al., "Spread-spectrum clock generator for serial ATA with multi-bit ΣΔ modulator-controlled fractional PLL," *ICICE Trans. Electron.*, vol. E-89C, no. 11, pp. 1682-1688, Nov. 2006.

[48] A. Demir, A. Mehrotra, and J. Roychowdhury. "Phase noise in oscillators: a unifying theory and numerical methods for characterization," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 47, no. 5, pp. 655-674, May 2000.

Appendix A: Behavioral Modeling of VCO with Jitter

A.1 Oscillator Phase Noise and Accumulation Jitter

Noise within an oscillator causes phase noise at its output. The white noise and flicker noise are two major noise sources to attribute phase noise. The phase noise can be represented by its power spectral density $S_\Phi(\Delta f)$ [34]

$$S_\Phi(\Delta f) = n\left(\frac{1}{\Delta f^2} + \frac{f_c}{\Delta f^3}\right) \tag{A.1}$$

where Δf is the offset frequency from career, n is the parameter attributable to the white noise sources alone at Δf = 1 Hz and f_c is the flicker noise corner frequency. The phase noise exhibits a -30 dBc/Hz slope at the offset frequency less than the f_c, while the phase noise shows a -20 dBc/Hz slope at the offset frequency larger than the f_c. $S_\Phi(\Delta f)$ is difficult to find and instead, the single side-band (SSB) phase noise $L(\Delta f)$ is often used. In [48], the SSB phase noise of a free running oscillator with frequency f_0 disturbed by the white noise can be shown with a Lorentzian process

$$L(\Delta f) = \frac{cf_o^2}{c^2 f_o^4 \pi^2 + \Delta f^2} \tag{A.2}$$

where the corner frequency is $f_\Delta = cf_o^2\pi$.

When the frequency is well above f_Δ and well below f_0,

$$L(\Delta f) \simeq \frac{cf_o^2}{\Delta f^2} \tag{A.3}$$

The jitter of an oscillator, an undesired variation in time since the previous output transition, is strongly related to its phase noise. Period jitter, J, attributed from the white noise sources, defined as the standard deviation of the variation in one period, can be found as [48]

$$J = \sqrt{\frac{c}{f_0}}. \tag{A.4}$$

Modeling of VCO with Jitter

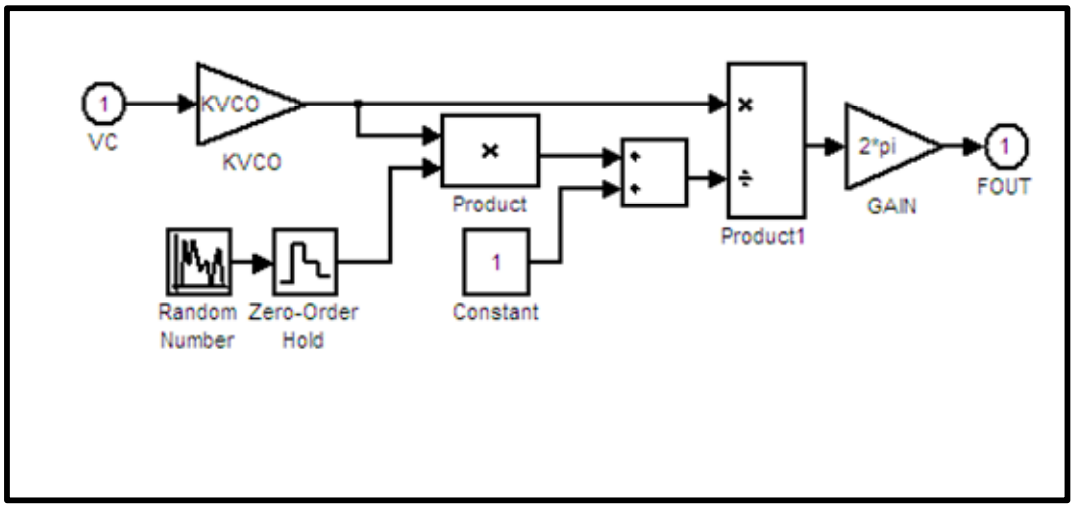


Fig. A.1. VCO model with jitter built in Matlab.

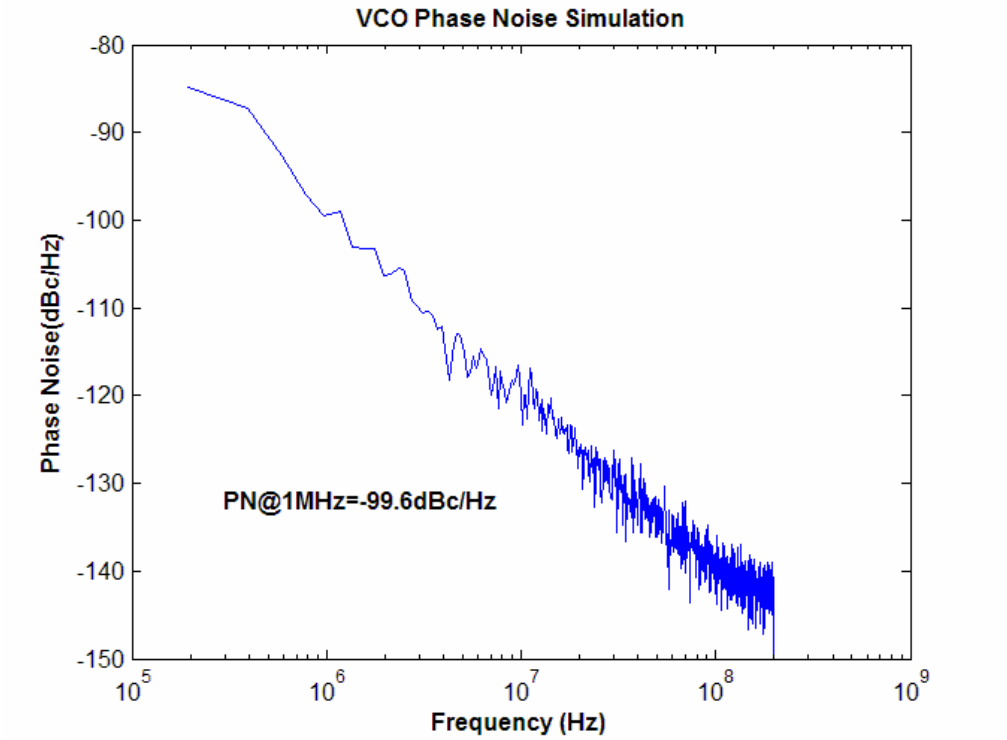


Fig. A.2. VCO phase noise simulation results.

where c can be evaluated from (A.3)

$$c = \frac{\Delta f^2 L(\Delta f)}{f_o^2} \tag{A.5}$$

Thus the phase noise and jitter can be linked from (A.4) and (A.5).

A.2 VCO Model with Jitter

The jitter of a VCO is modeled as a random variation in the frequency of the VCO. The duration of any interval τ_i with the period jitter, J,

$$\tau_i = \tau + J \tag{A.5}$$

where J is the standard deviation of a random process and can be evaluated from (A.3). $\tau = 1/f_0$. The output frequency f_{out} is

$$f_{out} = \frac{1}{\tau + J} = \frac{\frac{1}{\tau}}{1 + \frac{J}{\tau}} = \frac{f_0}{1 + f_0 J} \tag{A.6}$$

The output frequency in radian ω_{out} is

$$\omega_{out} = 2\pi f_{out} = 2\pi \frac{f_o}{1 + f_o J} \tag{A.7}$$

For a VCO, the career can be shown as

$$f_0 = f_{off} + V_c K_{vco} \tag{A.8}$$

where V_c is the input control voltage, f_{off} is the free running frequency when V_c=0, and K_{vco} is the sensitivity of the VCO in unit of MHz/V.

Thus, the VCO model with jitter built in Matlab is shown in Fig. A.1. The dither output frequency can be modeled by (A.7) and (A.8) where the period jitter is modeled by a random process. For an example, L= -100 dBc at offset frequency 1 MHz and the output frequency is 400 MHz. Applying (A.4) and (A.5) to evaluate J gives J=1.25 ps. The corresponding VCO phase noise is shown in Fig. A.2 and L=-99.6 dBc at offset frequency 1 MHz.

Vita

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Publication List

Journal Paper (Published or accepted)

1. Y. B. Hsieh and Y. H. Kao, "A Spread-Spectrum Clock Generator Using Fractional-N PLL with an Extended Range ΔΣ Modulator," *ICICE Trans. Electron.*, vol. E-89C, no. 6, pp. 851-857, June 2006.
2. Y. B. Hsieh and Y. H. Kao, "A Fully Integrated Spread Spectrum Clock Generator by Using Direct VCO Modulation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, accepted
3. Y. H. Kao and Y. B. Hsieh, "A High Performance Spread Spectrum Clock Generator Using Two-Point Modulation Scheme," *ICICE Trans. Electron.*, accepted.

Journal Paper (submitted)

1. Y. H. Kao and Y. B. Hsieh, "Effects of Loop Bandwidth on the Jitter Performance in Spread Spectrum Clock Generator," submitted to *IEEE Trans. Circuits Syst. I*
2. Y. H. Kao and Y. B. Hsieh, "A Low Power and High Precision Spread Spectrum Clock Generator for SATA Applications Using Two Point Modulation," submitted to *IEEE Trans. Electromagn. Compat.*.

Conference Paper (Published)

1. Y. H. Kao and Y. B. Hsieh, "A Wide Input-Range ΔΣ Modulator for Applications to Spread-Spectrum Clock Generator," in Proc. IEEE APCCAS, Dec. 2006, pp. 530-533.
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3. Y. B. Hsieh and Y. H. Kao, "A Fully Integrated Spread Spectrum Clock Generator Using Two-Point ΔΣ Modulation," in Proc. IEEE ISCAS, May 2007, pp. 2156-2159.
4. Y. B. Hsieh and Y. H. Kao, "A New Spread Spectrum Clock Generator for SATA Using Double Modulation Schemes," in Proc. IEEE CICC, Sep. 2007, pp. 297-300.