國立交通大學

材料科學與工程研究所

博士論文

銅金屬化製程及閘極介電層於低成本、低功率損耗 AlGaAs/InGaAs 假晶高電子遷移率電晶體單刀雙擲開關之應用

研 究 生：吳雲驥

指導教授：張　翼 博士

中華民國九十八年十二月

銅金屬化製程及閘極介電層於低成本、低功率損耗 AlGaAs/InGaAs 假晶高電子遷移率電晶體單刀雙擲開關之應用

Low Cost, Low Power Consumption SPDT GaAs Switches with Copper Metallization and Gate Dielectric

研 究 生：吳雲驥　　Student: Yun-Chi Wu

指導教授：張　翼 博士　　Advisor: Dr. Edward Yi Chang

國立交通大學

材料科學與工程研究所

博士論文

A Dissertation

Submitted to Department of Materials Science and Engineering

College of Engineering

National Chiao Tung University

In Partial Fulfill of the Requirements

For the Degree of

Doctor of Philosophy in Engineering

2009

Hsinchu, Taiwan, Republic of China

中華民國九十八年十二月

銅金屬化製程及閘極介電層於低成本、低功率損耗 AlGaAs/InGaAs 假晶高電子遷移率電晶體單刀雙擲開關之應用

研究生：吳雲驥　　指導教授：張 翼 博士

國立交通大學材料科學與工程研究所

摘要

這篇論文為研究低製作成本，低功率損耗之鋁砷化鎵/銦砷化鎵 (AlGaAs/InGaAs) 假晶高電子遷移率電晶體 (pseudomorphic high-electron-mobility transistor, PHEMT) 單刀雙擲 (single-pole-double-throw, SPDT) 開關之技術。內容包含了使用銅金屬化製程應用在 AlGaAs/InGaAs PHEMT 單刀雙擲開關的金屬內導線上，和評估不同溫度下銅金屬化製程單刀雙擲砷化鎵開關的電性特徵；及使用高介電係數之氧化鋁技術於 AlGaAs/InGaAs 金屬氧化物半導體假晶高電子遷移率電晶體單刀雙擲開關，以降低開關控制電流，減少損耗功率。

在銅內連接導線方面，本篇研究使用鉑做為擴散阻障層材料做為銅金屬化擴散阻障層以應用在 AlGaAs/InGaAs PHEMT 單刀雙擲開關上。比較使用金內連接導線之砷化鎵開關，銅製程單刀雙擲開關展現出相似的電特性，在 2.5 GHz 頻率下介入損耗小於 0.5 dB，隔離度大於 35 dB 和 input P_{1dB} 為 27 dBm 特性。從熱穩定測試，這些銅製程開關在 250 ℃溫度退火 20 個小時後，直流特徵沒有降低。此外經過高溫 150 ℃儲存壽命 (HTSL) 環境測試，這些銅製程開關仍舊保持優秀之功率處理特性。在操作可靠度測試方面，將銅製程開關在室溫施以 24 小時，控制電壓交換 +3/0 V 之 on/off 加速測試，元件經過 on/off 加速測試後依舊保持

優秀之微波特性。

之後我們更進一步研究鉑做為擴散阻障層製作出銅製程 AlGaAs/InGaAs PHEMT 單刀雙擲開關，在不同溫度下的電性特徵，首先比較金內連接導線之砷化鎵開關，銅製程單刀雙擲開關展現出在 2.5 GHz 頻率下可比較的介入損耗小於 0.5 dB，反射損耗大於 20 dB，隔離度大於 35 dB 和 input P_{1dB} 為 28.3 dBm 特性。為了研究高溫應用上，溫度效應對於銅製程單刀雙擲開關的直流和微波特性的影響，在不同溫度下測試單刀雙擲開關，元件在 300 °K 到 500 °K 的溫度區間展現出低的熱啟始電壓係數 ($\delta V_{th}/\delta T$)，其值為 -0.25 mV/°K，在 2.5 GHz 頻率及 380 °K 溫度操作下，其介入損耗小於 0.5 dB，隔離度大於 40 dB 和 input P_{1dB} 為 28.45 dBm 等好的微波特性。

另外我們使用原子層沈積技術氧化鋁為閘極氧化層製作 AlGaAs/InGaAs 金屬氧化物半導體假晶高電子遷移率電晶體單刀雙擲開關。相較於傳統的 PHEMT，MOS-PHEMT 有相若的直流表現和較低的閘極漏電流，微波測試顯示 MOS-PHEMT 開關在 2.5 GHz 頻率下其介入損耗小於 0.5 dB，反射損耗大於 15 dB，隔離度大於 30 dB 和 input P_{1dB} 為 31.4 dBm 等微波特性。由以上的結果顯示，我們成功的製作出銅製程 AlGaAs/InGaAs 假晶高電子遷移率電晶體單刀雙擲開關和完成原子層沈積技術氧化鋁為閘極氧化層製作 AlGaAs/InGaAs 金屬氧化物半導體假晶高電子遷移率電晶體單刀雙擲開關。這是文獻上第一次發表 AlGaAs/InGaAs 假晶高電子遷移率電晶體單刀雙擲開關之銅金屬化製程及使用金屬氧化物半導體，這些成果，有助於製造低成本、低功率損耗之 SPDT switch 以供無線通訊應用。

Low Cost, Low Power Consumption SPDT GaAs Switches with Copper Metallization and Gate Dielectric

Student: Yun-Chi Wu Advisor: Dr. Edward Yi Chang

Department of Materials Science and Engineering

National Chiao Tung University

Abstract

In this dissertation, the performances of the copper (Cu)-metallized AlGaAs/InGaAs pseudomorphic high-electron-mobility transistor (PHEMT) single-pole-double-throw (SPDT) switches and the AlGaAs/InGaAs metal-oxide-semiconductor PHEMT (MOS-PHEMT) SPDT switches with Al_2O_3 were studied.

Cu-metallized AlGaAs/InGaAs PHEMT SPDT switches utilizing platinum (Pt, 70 nm) as the diffusion barrier is reported. In comparison with the gold (Au)-metallized switches, the Cu-metallized SPDT switches exhibited comparable performance with insertion loss of less than 0.5 dB, isolation larger than 35 dB and the input power for one dB compression (input P_{1dB}) of 27 dBm at 2.5 GHz. To test the thermal stability of the Pt diffusion barrier, these switches were annealed at 250 ℃ for 20 h. After the annealing, the switches showed no degradation of the DC characteristics. In addition, after 144 h of high temperature storage life (HTSL) environment test at 150 ℃, these Cu-metallized switches still remained excellent and reliable radio frequency (RF) characteristics and power handling capability. To test the operation reliability of the Cu-metallized switches, the Cu-metallized switches were subjected to on/off (control voltage = +3/0 V exchange) stress test for 24 h at

room temperature. The devices maintained excellent RF characteristics after the stress test.

The electrical characteristics of these Cu-metallized AlGaAs/InGaAs PHEMT SPDT switches were also evaluated at elevated temperatures. Compared to the Au-metallized switches, the Cu-metallized SPDT switches exhibited comparable performance with insertion loss less than 0.5 dB, return loss larger than 20 dB, isolation larger than 35 dB, and the input P_{1dB} of 28.3 dBm at 2.5 GHz. In order to evaluate the temperature impact on DC and RF characteristics of the Cu-metallized switches for high-temperature applications, the switches were tested at different temperatures. The device exhibits low thermal threshold coefficients ($\delta V_{th}/\delta T$) of −0.25 mV/°K from 300 °K to 500 °K, good microwave performance at 380 °K with insertion loss less than 0.5 dB, isolation higher than 40 dB, and the input P_{1dB} of 28.45 dBm at 2.5 GHz.

An AlGaAs/InGaAs MOS-PHEMT SPDT switch using Al_2O_3 high-κ gate dielectric by atomic layer deposition (ALD) is fabricated for RF switch application. The MOS-PHEMT exhibited the comparable DC performance and much lower gate current as compared to the conventional PHEMT. RF test shows the MOS-PHEMT switch has an insertion loss of less than 0.5 dB, an isolation larger than 30 dB, a return loss larger than 15 dB, and an input P_{1dB} of 31.4 dBm at 2.5 GHz.

Overall, we have successful developed the Cu metallization process for the AlGaAs/InGaAs SPDT switch and the Al_2O_3 high-κ gate dielectric process for the MOS-PHEMT SPDT switch, and have reported the fabrication process and electrical performances of the Cu-metallized switches and the MOS-PHEMT switches with Al_2O_3 dielectric for low cost and low power consumption SPDT switches for wireless communication applications.

誌　　謝

能夠順利完成這份博士論文，首先必須對指導教授張翼博士表達深深的感謝之意，感謝教授在我就讀研究所的五年多期間，無論在生活上、課業上或實驗上所給予的許多指導與幫助，使我能夠順利的完成學業。

另外要感謝林岳欽學長在製程以及電性量測方面給予許多的意見以及協助排除製程問題方面給予的意見與指導；同時也感謝吳偉誠、黃瑞乾、陳克弦、楊宗禧、張家源等學長們，和陳俊淇同學，及黃延儀、張家達、許立翰、唐士軒、Trinh Hai、蘇詠萱，及電子所張哲榮等學弟妹們在實驗和儀器上的幫忙與協助；感謝元智通訊工程學系許恆通教授在電性分析的指導，並感謝國家實驗研究院儀器科技研究中心柯志忠博士在技術和儀器上的指導，在此對於大家的幫助與支持十分感謝。

在實驗設備上需感謝學校及國家實驗研究院儀器科技研究中心提供了良好的實驗環境與儀器設備，使整個實驗得以順利的進行，進而得到良好的實驗數據與結果，感謝NDL和奈米中心所提供的服務與協助。

最後我要感謝我的家人，尤其感謝父母親及女友在我求學期間，始終無怨無悔的提供經濟上以及精神上的全力支持與鼓勵，使我得以在無後顧之憂下順利完成學業，真的非常感謝大家。

Contents

Table Captions

Chapter 1

Figure Captions

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

Chapter 1

Introduction

1.1 General Background and Motivations

Copper (Cu) metallization and high-k dielectrics have been used in Si technology to resolve the RC delay issue and for lower power consumption at higher operating frequencies. The Cu metallization process has been widely used in Si integrated circuit technology since IBM announced its success with Cu metallization instead of aluminum (Al) in the Si 0.18-μm very large scale integration technology [1, 2, 3]. The advantages of using Cu metallization for Si technology include low resistivity and high electromigration resistance, high stress voiding resistance, and feasible for Damascene process for smaller line dimensions VLSI. However, Cu diffuses very fast into Si in absence of any diffusion barrier [4, 5, 6]. Cu also diffuses very fast into GaAs when Cu is in direct contact with the GaAs substrate without any diffusion barrier [7]. Even though the use of Cu as metallization metal has become very popular in Si devices, there are only a few reports on the Cu metallization of GaAs devices. Traditionally, titanium (Ti)/Au interconnect metal is widely used for the fabrication of GaAs-based field effect transistors and monolithic microwave integrated circuits (MMICs) and the reliability of the metal system has been well proven. In this study, Cu metal instead of gold (Au) metal is used as the interconnect metal for the AlGaAs/InGaAs pseudomorphic high-electron-mobility transistor (PHEMT) single-pole-double-throw (SPDT) switches. The employment of Cu as the metallization metal has several major advantages over Au, such as lower resistivity (1.67 μΩ-cm for Cu; 2.2 μΩ-cm for Au), higher thermal conductivity (3.98 W/cm°K for Cu; 3.15 W/cm°K for Au), and lower cost, as compared with Au.

Table 1.1 lists a comparison of the characteristics of interconnect metals [8]. The

price of Cu is 5400 times cheaper than that of Au, and thus the production cost will be reduced. However, Cu diffuses very fast into III-V semiconductors as well as Si. The diffusion barrier between the Cu interconnections and the semiconductor for GaAs devices has to possess the following properties:

(1) High resistance to diffusion of foreign atoms;

(2) High conductivity, thermal stability and crystallization temperature;

(3) Inert with Cu and underlying metal or substrate;

(4) Good adhesion between Cu and underlying materials;

(5) Smooth surface and low stress;

(6) Lack of grain boundaries and with an amorphous texture;

(7) The loss rate of barrier layer into overlying metal and underlying substrate should be small.

As mentioned above, Cu diffuses very fast into GaAs if without any diffusion barrier and forms a deep acceptor to capture carriers in GaAs. It will lead to the failure of GaAs devices. In our previous researches, we have demonstrated backside Cu metallization on GaAs semiconductor field-effect transistors (MESFET) using TaN as the diffusion barrier [9, 10], Cu airbridge on low noise GaAs high-electron-mobility transistors (HEMTs) using WN_x as the diffusion barrier [11], fully Cu metallized InGaP/GaAs heterojunction bipolar transistor (HBT) using platinum (Pt) as the diffusion barrier [12, 13] and a Au-free fully Cu-metallized InP HBT was also realized using Ti/Pt/Cu nonalloyed ohmic contacts with Pt as the diffusion barrier [14]. It has also been demonstrated that the Ti/Pt/Cu system structure was very stable even after being annealed up to 350 ℃ and that Cu started to diffuse through the Pt diffusion barrier and formed the Cu_4Ti phase after annealed at 400 ℃, as investigated by X-ray diffraction method, Auger electron spectroscopy depth profiles, and the sheet resistance measurement [12]. In this study, the electrical

performance of the PHEMT SPDT switches using Cu metallization technology are evaluated in Chapter 4. We characterized the electrical performance of the Cu-metallized PHEMT SPDT switches and compare the performance with the Au-metallized PHEMT SPDT switches. Pt was used as the diffusion barrier layer for Cu-metallized switches and we choose Pt as the diffusion barrier metal since Pt is commonly used as the plate metal for the metal-insulator-metal (MIM) capacitor of the switch. Moreover, the thermal stability of the Pt diffusion barrier and the electrical reliability are also investigated. In Chapter 5, the temperature-dependent characteristics of the Cu-metallized switches are studied.

For the low power consumption demands, the GaAs PHEMT based switches, which demonstrate low gate current, have an obvious advantage over Si p-i-n (PIN) diode based switches due to lower DC power consumption [15]. Overall, GaAs switches have lower control voltage, higher power handling capability, and higher electron mobility compared to other solid-state switches, which makes them suitable for cellular handset, wireless local area network (WLAN), and bluetooth applications. However, III-V HEMT using Schottky gate for current modulation usually results in higher gate leakage current as compared to MOSFET using high-κ dielectric for device modulation. The use of high-κ gate dielectric for III-V HEMT can significantly suppress direct-tunneling gate current and results in considerable reduction in power consumption. In Chapter 6, atomic layer deposition (ALD) Al_2O_3 with a high dielectric constant (8.6-10) and a high breakdown field (5~10 MV/cm) was used as high-κ material for AlGaAs/InGaAs MOS-PHEMT switches [16]. The major requirements for good RF switch are low insertion loss, high isolation, high power handling capability and low control current [17]. To achieve low control current, the methods include reducing the gate current and the size of devices. The MOS-PHEMT switches with extra high resistance between control electrode and signal path provide

good isolation and results in much lower control current as compared to conventional PHEMT switches.

1.2 Outline of the Dissertation

This dissertation covers the related studies of the novel SPDT switch technologies including the Cu-metallized AlGaAs/InGaAs PHEMT switches and the MOS-PHEMT switches. The contents are divided into 7 chapters. In Chapter 2, the introduction to the GaAs switch characteristics and the device equivalent circuit schematic are briefed. Then, the detailed fabrication process of the Cu-metallized switch and the MOS-PHEMT switch is described in Chapter 3.

In Chapter 4, the Cu-metallized AlGaAs/InGaAs PHEMT SPDT switches utilizing Pt (70 nm) as the diffusion barrier is reported. In comparison with the Au-metallized switches, the RF performance and the power handling capability of the Cu-metallized switches at 2.5 GHz were evaluated. To test the thermal stability of the Pt diffusion barrier, these switches were annealed at 250 ℃ for 20 h. In addition, after the high temperature storage life (HTSL) environment test at 150 ℃ for 144 h was carried out for these Cu-metallized switches, the RF characteristics and the power handling capability were observed. To test the operation reliability of the Cu-metallized switches, the Cu-metallized switches were subjected to on/off (control voltage = +3/0 V exchange) stress test for 24 h at room temperature.

In Chapter 5, in order to evaluate the temperature-dependent impact on DC and RF characteristics of the Cu-metallized switches for high-temperature applications, the switches were tested at different temperatures. The low thermal threshold coefficients ($\delta V_{th}/\delta T$) of the device were evaluated from 300 °K to 500 °K, the microwave performance at 380 °K at 2.5 GHz was evaluated.

In Chapter 6, an AlGaAs/InGaAs MOS-PHEMT SPDT switch is fabricated using

Al_2O_3 high-κ gate dielectric by ALD for RF switch application. The MOS-PHEMT exhibited the comparable DC performance and much lower gate current as compared to the conventional PHEMT. The RF test and an input power for one dB compression (input P_{1dB}) of the MOS-PHEMT switch at 2.5 GHz were measured. The MOS-PHEMT MMIC switch was realized using ALD Al_2O_3 gate dielectric in this study.

Chapter 7 is the conclusions of the dissertation.

TABLE

Table 1.1 Properties comparisons of the possible interlayer metals [8].

Property\Metal	Cu	Ag	Au	Al
Resistivity (μΩ • cm)	1.67	1.59	2.35	2.66
Young's modulus · (10^{-11} dyn/cm^2)	12.98	8.27	7.85	7.06
Thermal Conductivity (W/cm°K)	3.98	4.25	3.15	2.38
CTE · (10^6)	17	19.1	14.2	23.5
Melting Point (℃)	1085	962	1064	660
Specific heat Capacity (J/Kg•K)	386	234	132	917
Corrosion in air	Poor	Poor	Excellent	Good
Deposition				
Sputtering	Yes	Yes	Yes	Yes
CVD	Yes	No	No	No
Evaporation	Yes	Yes	Yes	Yes
Etching				
Dry	No	No	No	Yes
Wet	Yes	Yes	Yes	Yes
Resistance to Electromigration	High	Very Low	Very High	Low
Delay Time (ps/mm)	2.3	2.2	3.2	3.7

Chapter 2

Theory of Filed-effect-transistor Based Switch

2.1 Comparisons between FET Swicth and PIN Switch

The transmitter/receiver (T_x/R_x) switches are important components as common as amplifiers and mixers in microwave systems as shown in Fig. 2.1. Because of the booming demands for RF switches in cellular handset, base station, bluetooth, and WLAN systems, high performance GaAs RF switches become very important. T_x/R_x switch is for changing the RF signal path to transmitter or receiver. Therefore, a low insertion loss, high isolation and high power handling capability characteristics are needed for switches to improve the overall system performance for wideband frequency. Traditionally the PIN diode has been widely used for switching RF signals. However, PIN diodes have high insertion loss with high bias current. Thus, the GaAs switches predominate over the commercial RF switches because of its low on resistances, low off capacitances and high linearity for the switch market. GaAs PHEMT has been commercially applied in RF switches and power amplifier for wireless communication applications. Owing to its higher charge density and higher saturated electron velocity in InGaAs channel compared to the GaAs MESFET, PHEMT performs lower insertion loss for switch, and higher power gain and power added efficiency for power amplifier [18]. For realizing practical RF switch based on AlGaAs/InGaAs PHEMTs, two major factors must be emphasized: First, reduction of the on-state-resistance (R_{on}) at V_{gs} = 0 V for insertion loss. Second, reduction of the off-state-capacitance (C_{off}) when the V_{gs} is below V_{th} for isolation [19]. Besides, the depletion mode PHEMT is used for most commercial RF switches. Although switches can also use the enhancement mode PHEMT device, the performance of the power handling capability is poor. Therefore, it is straightforward to design the depletion

mode PHEMT switches [15]. Therefore, PHEMT switches have become prevalent because the field effect transistor (FET) switches have advantages over diode switches for low power consumption, good RF performance, and easy monolithic circuit integration [20].

2.2 Antenna Switch Design

The typical circuit schematic of the antenna SPDT switch is shown in Figs. 2.2(a) and 2.2(b) for the transceiver construction and the SPDT switch is designed for two control voltages to inversely feed to the transistor pairs. One control voltage is high and the other control voltage is low. In transmit mode, the shunt FET in the transmit path is off, whereas the series FET is on. The transmit signal is flowing to the antenna. Meanwhile, the shunt FET in the receiver stem is on, while the series FET is off preventing the transmit signal in the receiver. Oppositely, in the receive mode the control voltages are reversed. Therefore, switch isolation can easily be improved by joining shunt mounted FET without excessive increase of insertion loss [15]. As mentioned above, the gate widths of the series and shunt devices have to be detailed designed to optimize tradeoff between insertion loss in on-state and isolation in off-state [21].

2.3 Equivalent Circuit of a Switch Used FET

The drain-to-source resistance of the FET in the channel behaves as a voltage variable resistor for a switch, and the gate-to-source voltage (V_{gs}) controls the resistance. Therefore, the FET switch is a three-terminal device in which the V_{gs} determines the on/off states. A FET for a switch is biased with the drain and source at zero voltage DC. The RF signal path is flowing from drain to source and the gate is the control terminal. Fig. 2.3 shows the typical current-voltage characteristics of a

depletion mode FET about V_{ds} = 0 V at different V_{gs}. The V_{ds}/I_{ds} characteristic approaches a resistance (I_{ds}/V_{ds}) in the region of V_{ds}= 0V. This is a low resistance at V_{gs} = 0 V. Oppositely, the FET is off as V_{gs} below pinch-off voltage with a high resistance. This simple equivalent circuit is shown in Fig. 2.4. The gate resistor (R_g) with the value of several kΩ is designed to provide extra isolation between the signal and control terminal. Very little gate current below 0.5 mA/mm for FETs can be obtained. Therefore, the FET switches have very low DC power consumption as compared to PIN diode switch [15].

Fig. 2.5(a) depicts an equivalent circuit schematic for a GaAs FET used in switching applications. The FET serves as a passive two-terminal device, which the gate terminal acts as the control signal port in passive mode. The RF signal flows between the drain and source. The gate terminal determines the RF impedance between the drain and source. The drain-to-source impedance varies from a low value under open channel when the gate is biased at zero voltage, to a high value when the gate is biased at pinch-off voltage to prevent current from flowing through the transistor.

When the low-impedance state of the FET switch is dominated by the fully open channel in passive mode, the device channel resistance is low. Owing to the low channel resistance, the insertion loss is independent of frequency [22]. The practical equivalent circuit is the "on" resistance for the transistor, and the reduction of on-state resistance and insertion loss can be improved by the large device width. In the high-impedance state, the PHEMT is dominated by the pinched-off channel or large "off" resistance as shown the switch equivalent circuit in Fig. 2.5(b). While r_g is much smaller than the reactance of C_g $\left[r_g \le 1/(\omega C_g)\right]$, the equivalent circuit of Fig. 2.5(a) can be substituted by a parallel combination of R_{off} and C_{off} as shown in Fig. 2.5(b),

where R_{off} and C_{off} are expressed as shown in equation (2.1) and (2.2):

$$C_{off} = C_{sd} + \frac{C_g}{2} \tag{2.1}$$

$$R_{off} = \frac{2r_d}{2 + r_d \omega^2 C_g{}^2 r_g} \tag{2.2}$$

where ω is the operating frequency in radians/second [23]. The "off" state resistance R_{off} is an inverse function of the operating frequency ω, and reduces as frequency increases according to the equation (2.2). The off-state performance of the switch will degrade at high frequency [24]. Furthermore, the degradation of the isolation in the off-state would be also resulted from increases of gate-to-source, gate-to-drain capacitance, and source-to-drain fringing capacitance by large device width [22]. Therefore, the device gate width must be optimized for better RF performance.

2.4 RF Characteristics of a Switch

2.4.1 Insertion Loss (IL)

Insertion loss (IL) in the on state is defined as the difference (dB) between the power received at the load before and after the insertion of the switch [25]. In view of this definition, insertion loss for the switch in the on state is expressed as shown in equation (2.3):

$$IL = -10\log_{10}(\frac{P_L}{P_0}) \tag{2.3}$$

where

P_0= power delivered to the load with an ideal switch in the on state.

P_L= power delivered to the load with the practical switch in the on state.

2.4.2 Isolation

Isolation in the off state is defined as the difference (dB) between the power

delivered to the load for an ideal switch in the on state and the actual power delivered to the load when the switch is in the off state [25]. In view of this definition, isolation is expressed as shown in equation (2.4):

$$Isolation = -10\log_{10}(\frac{P'_L}{P_0}) \tag{2.4}$$

where

P_0 = power delivered to the load with an ideal switch in the on state.

P'_L = power delivered to the load with the practical switch in the off state.

2.4.3 Power Handing Capability

The FET switch maximum handling power (P_{max}) is evaluated in the on-state and in the off-state. P_{max} is expressed in equation (2.5) and (2.6) [17]:

$$P_{\max} = \frac{I_{dss}{}^2 Z_0}{2} \quad \text{(on-state)} \tag{2.5}$$

and

$$P_{\max} = \frac{(n(V_p - V_{BR}))^2}{2Z_0} \quad \text{(off-state)} \tag{2.6}$$

where

I_{dss}: saturation drain current;

Z_0: system impedance;

n: number of stacked FETs;

V_{BR}: breakdown voltage.

From the practical consideration for the power limitation of the switch operation is explained in [26], and the maximum input power P_{max} is expressed by equation (2.7):

$$P_{\max} = \frac{(V_C - V_{th})^2}{2Z_0} \tag{2.7}$$

where Z_0 is the line impedance, V_c is the absolute of the control voltage, and V_{th} is the

threshold voltage.

2.4.4 Input third-order intermodulation intercept point and third-order intermodulation distortion

In wireless communication system, multi-channel transmission is practically used for signal transmission [27]. The transmission bandwidth of communication system was divided into multiple information bandwidths and used multiple frequencies for data transmission to increase the transmission capacity. Nevertheless, when the system operating frequencies are more than two and the neighboring frequencies are located closely to each other, the device used in system will generate intermodulation distortion.

For analyzing the intermodulation distortion, two-tone signal consists of two signals as the input with the same amplitude at two closely spaced signals 5-10 MHz apart as shown in Fig. 2.6. Among all the intermodulation distortions of the devices, third-order intermodulation distortion (IM3) and the third-order intercept point (IP3) will dominate the device linearity because of device gain compression. Therefore, IM3 and IP3 of the devices have become the important factors for wireless communication applications. Input third-order intermodulation intercept point (IIP3) is defined as shown in equation (2.8):

$$IIP_3(dBm) = P_{in}(dBm) + \frac{\Delta}{2}(dB) \tag{2.8}$$

where

IIP3: input third-order intermodulation intercept point;

P_{in}: input power;

Δ: intermodulation ratio (P(f2)-P(2f2-f1)).

FIGURES

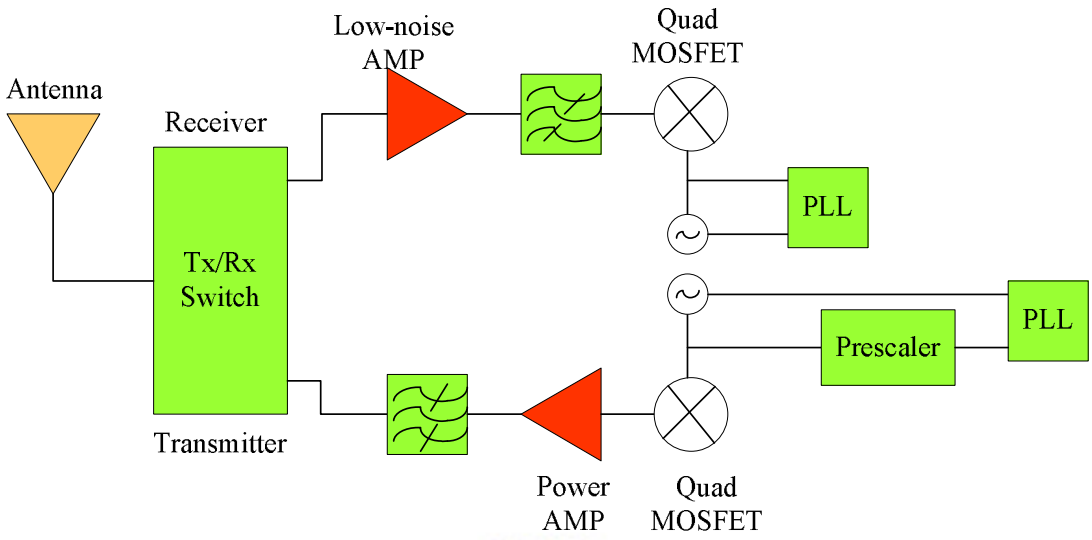
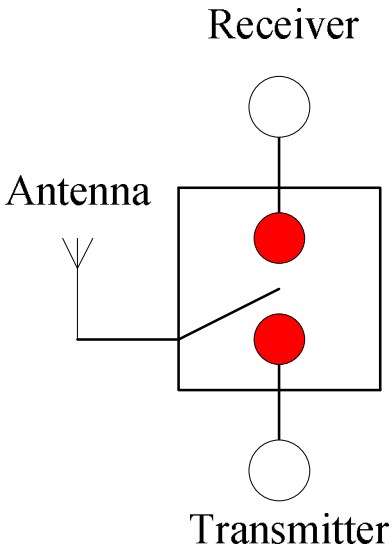
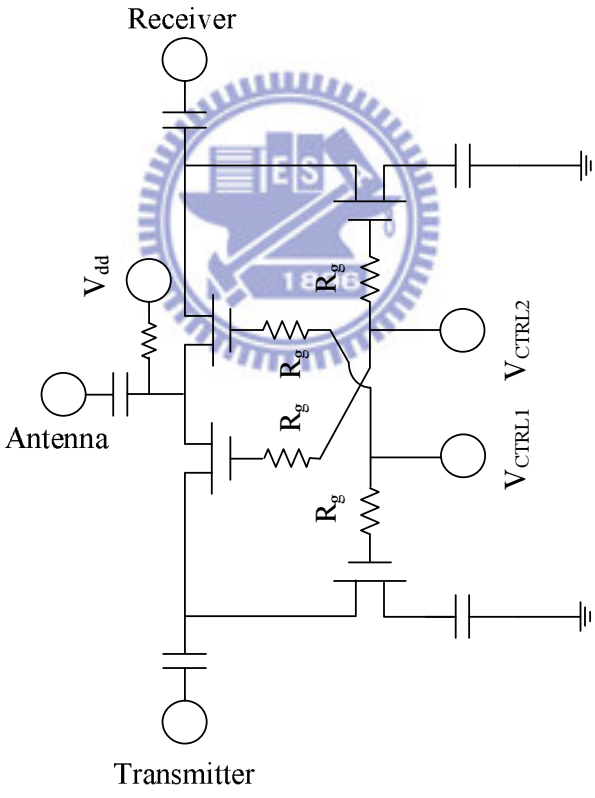


Figure 2.1 Radio frequency front-end system.



(a)



(b)

Figure 2.2 (a) Specific schematic of an antenna switch. (b) Circuit schematic of a single-pole-double-throw antenna switch [21].

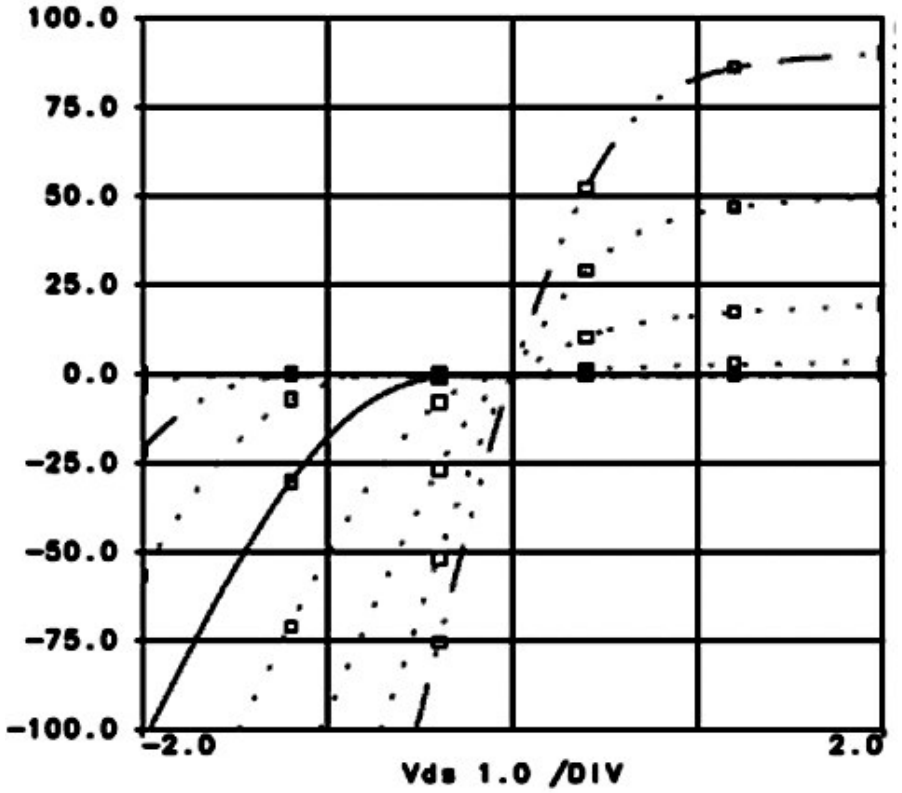


Figure 2.3 Typical I-V characteristics of a depletion mode field-effect transistor [15].

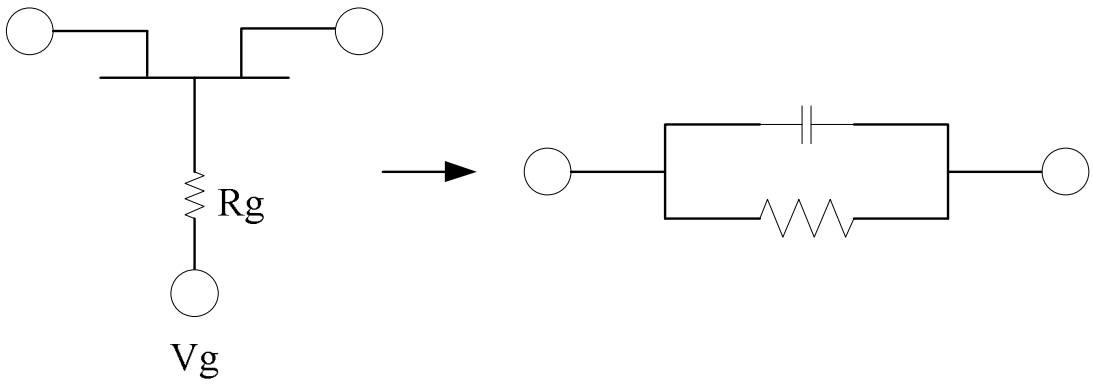
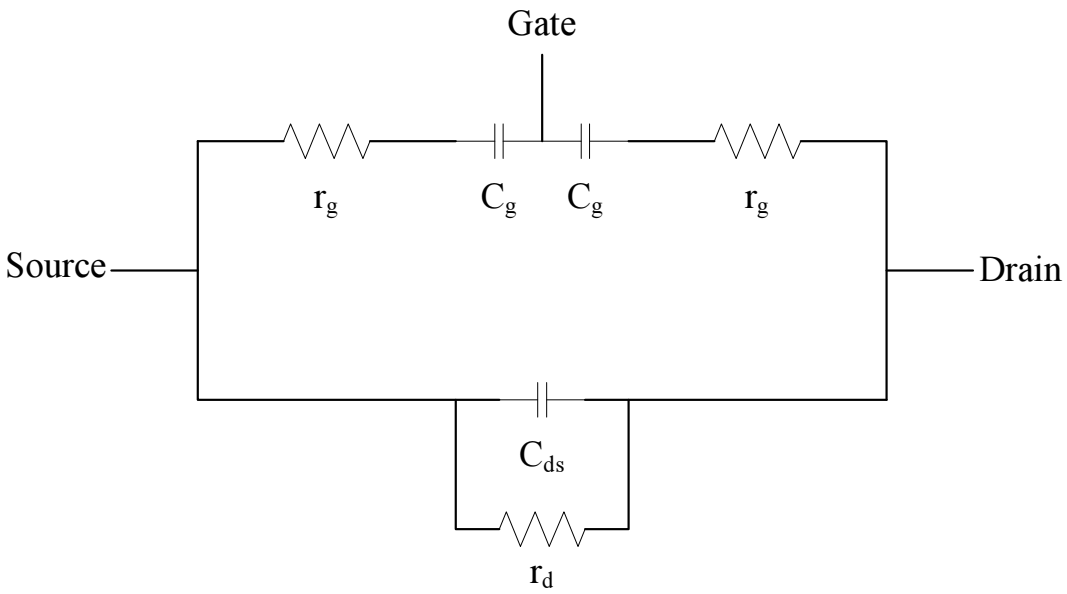
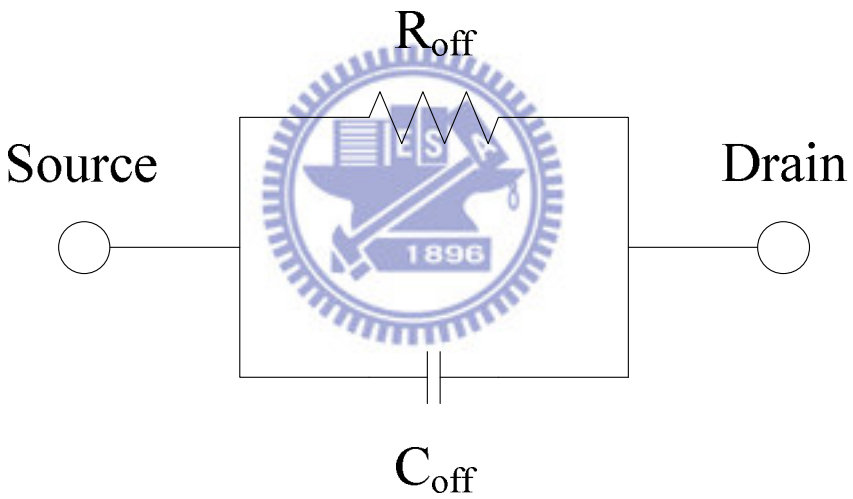


Figure 2.4 Equivalent circuit of a switching FET [15].



(a)



(b)

Figure 2.5 (a) Equivalent circuit schematic for a GaAs FET for switching applications. (b) Simplified off-state equivalent circuit for a FET switch in high-impedance state [23].

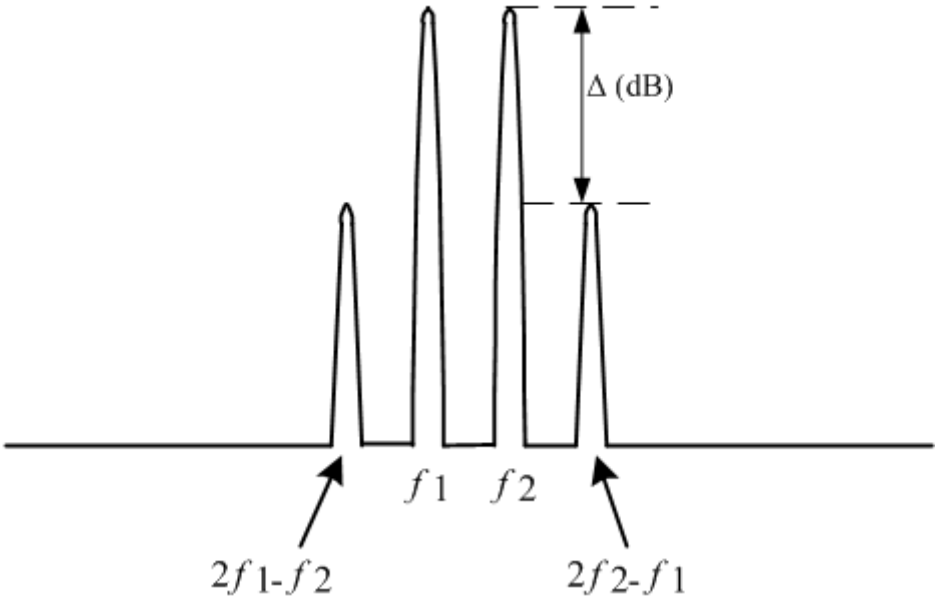


Figure 2.6 Output power spectrum of the two-tone input signal [27].

Chapter 3

Fabrication of Copper-Metallized GaAs Switch and MOS-PHEMT Switch

3.1 Introduction of PHEMT switch process

The five major steps of the series/shunt SPDT PHEMT switch process are device active region definition, ohmic metal deposition and annealing, gate formation by wet chemical recess and gate photolithography, device passivation, and interconnection formation [27]. The schematic cross section of the PHEMT switch is shown in Fig. 3.1. The detailed fabrication process of the Cu-metallized switch and the MOS-PHEMT switch will be described in the following section.

3.2 Cu-metallized switch process

3.2.1 Device active region definition

Device active region definition is to confine the electrically conductive part of the device to specific parts of its surface area so that electrical current is prevented from flowing to other active areas [28]. The electrically conductive region is called the “active region”. The GaAs PHEMT was etched to separate each device and to reduce the leakage current from the substrate for the isolation. The functions of the active region definition consist of the active region formation, device isolation, reduction of parasitic capacitance, parasitic resistance, leakage current, and back-gating effect.

The AlGaAs/InGaAs PHEMT SPDT switch wafer was grown by metal organic chemical vapor deposition (MOCVD) on a 4-in semi-insulating GaAs substrate. The structure, from bottom to top, is composed of a 600-nm GaAs/AlGaAs superlattice buffer, a 13-nm undoped InGaAs channel, a 3-nm undoped AlGaAs spacer, a delta-doped layer, a 37-nm undoped AlGaAs Schottky layer, and a 60-nm n^+-GaAs

capping layer, as shown in Fig. 3.2. The Hall electron mobility and sheet carrier concentrations at room temperature are 6500 $cm^2/V \cdot s$ and 3.0 x 10^{12} cm^{-2}, respectively.

The device fabrication was carried out by the use of traditional lithography and lift-off technique. In the PHEMT switch fabrication, the device active region and the epitaxial resistor formation are defined by photolithography. The wafer was etched to buffer layer to obtain a good isolation. Then the mesa isolation and epitaxial resistors were formed utilizing $H_3PO_4/H_2O_2/H_2O$ mixing solution. After mesa etching, we measured the etching depth by α-stepper to achieve the etch depth of about 400 nm, and checked the etched profile by scanning electron microscope (SEM).

3.2.2 Ohmic contact formation

The ohmic contact is formed by ohmic metal deposition and annealing. An ohmic contact is a low resistance junction between metal and semiconductor interface. Lower contact resistance will reduce device on-resistance and device power consumption. Therefore, in order to obtain good ohmic contact with low parasitic resistance, the semiconductor is doped heavily to form good contacts. After the ohmic metals deposition, a high temperature alloying process using rapid thermal anneal (RTA) was conducted to form the ohmic contacts.

For the ohmic metal layer formation, the germanium (Ge) is used for doping the GaAs and the nickel (Ni) is acted as a wetting agent and prevents the AuGe metal from “balling up” during alloy. In the PHEMT switch fabrication, Au/Ge/Ni/Au was used as the ohmic metal with total thickness of 410 nm. The Au/Ge alloy at 410 ℃ is commonly used to form low ohmic contact resistance and has good reliability.

For the ohmic contact formation, the ohmic contact was defined by conventional photolithography with undercut profile. Then O_2 plasma descum was applied to

remove the residual photoresist on the pattern. The wafer was dipped in 10 % HCl solution for 1 min to remove native oxide from the surface before the ohmic metal deposition. Finally, Au/Ge/Ni/Au ohmic metal was deposited by e-gun evaporation. The ACE was used to lift-off for devices, and then the wafer was alloyed by RTA at 410 ℃ for 30 seconds to form ohmic contacts. The typical ohmic contact resistance was 0.12 Ω · mm.

3.2.3 Recess and gate formation

The gate process includes wet chemical recess and gate photolithography. The gate recess process has two advantages. One is the gate is placed below the surface depletion layer of the surrounding material, preventing surface depletion from preventing current under forward gate bias, and the other one is gate recess will reduce channel thickness and drain-to-source saturation current. Consequently, gate recess process can increase device breakdown voltage, and decrease source-to-gate and gate-to-drain parasitic resistances. In the PHEMT switch fabrication, the wet chemical etching process was used for gate recess. The recess slot was defined by conventional photolithography. Then, a citric acid/H_2O_2/H_2O solution was used to etch the cap layer and AlAs as the etch stop layer until it reaches the target current for the gate-recess process. The target current will influence the PHEMT RF performance. The drain-to-source current is measured during the recess process to control the target current by curve tracer. After removing the recess photoresist, the gate openings were also defined by conventional lithography to form the gate lift-off photoresist profile. Before the gate metal deposition, the wafer was dipped in 10 % HCl solution for 1 min to remove the native oxide from the surface. Then that gate metal was deposited by e-gun evaporation. The gate metal is Ti/Pt/Au= 100/100/300 nm and the gate length of the devices was 0.5 μm. Ti has good adhesion to GaAs, Pt has a barrier to

prevent Au diffusing into GaAs, and Au has high electrical conductivity. Finally the wafer was immersed into ACE to lift-off the undesired metal.

3.2.4 Device passivation

Plasma enhanced chemical vapor deposition (PECVD) silicon nitride (Si_3N_4) was used on the device for surface encapsulation because Si_3N_4 is less permeable to ions than silicon dioxide (SiO_2). The major purpose of the Si_3N_4 protective encapsulation is simply for the surface passivation. This passivation protects the critical area of the originally exposed wafer surface from humidity, chemicals, gases, and particles. The Si_3N_4 film was grown at 300 ℃. The precursors were SiH_4/Ar, NH_3, and N_2. The film refractive index was about 2.0, which were measured by ellipsometer. In the PHEMT switch fabrication, the Si_3N_4 films were used for passivation and as the dielectric for capacitors and were deposited by PECVD. The capacitance per unit area of the MIM capacitor was 0.25 fF/μm^2 and the thickness of the dielectric was 200 nm.

After the passivation process, the contact via was defined for interconnections. Then the Si_3N_4 film was etched by reactive ion etching (RIE) system. The reactive plasmas are CF_4 and O_2. The RF power is 80 W, and the pressure is 60 mtorr.

3.2.5 Interconnect metal line

The first metal consists of the adhesion layer Ti (30 nm) and the diffusion barrier Pt (70 nm), which was also used as the top plate of a MIM capacitor and the bottom layer of the interconnects. [12, 13]. A 2-μm-thick electroplated Cu was formed on the first metal (Ti/Pt) layers with an electroplated Cu seeding layer for interconnects. Then, the electroplated Cu was annealed at 200 ℃ for 2 h for eliminating the hydrogen embrittlement effect [29] and obtaining the film with the lowest resistivity

and the smoothest surface [30, 31]. Finally, a 100-nm-thick Si_3N_4 was deposited for final passivation.

The AlGaAs/InGaAs PHEMTs used in the switches had a 0.5-μm gate length with dual fingers, and the drain-to-source spacing was 9 μm. The ohmic contact resistance for the PHEMTs was 0.12 Ω·mm, and the MIM capacitors used in the switches with 200-nm Si_3N_4 had a capacitance of 0.25-fF/μm^2. A 3 kΩ of gate resistor (R_g) between the signal and control terminal was designed to provide isolation between the signal and control paths. The circuit schematic of the series/shunt SPDT switch is shown in Fig. 3.3. The control current of the GaAs SPDT switch is typically < 0.5 mA/mm.

The DC and RF electrical characteristics of the Cu switches were characterized to demonstrate the practicability of using the Cu interconnection on the SPDT switches. Thermal stability of the Pt diffusion barrier is a major concern in this study. To demonstrate the reliability of the Cu switches with the Pt diffusion barrier, the devices with the Cu interconnects were furnace annealed at 250 ℃ for 20 h in the nitrogen atmosphere. The DC characteristics before and after thermal annealing were compared to verify the thermal stability of the Cu-metallized switches. Besides, the long-term thermal stress of Cu switches was evaluated by using HTSL method, which was carried out by annealing at 150 ℃ for 144 h with no bias [18, 19, 20, 32]. To test the operation reliability of the Cu-metallized switches, the Cu-metallized switches were subjected to an on/off stress test (control voltage = +3/0 V exchange) for 24 h at room temperature. Furthermore, the temperature-dependent characteristics of the Cu-metallized switches are also studied.

3.3 MOS-PHEMT switch process

The MOS-PHEMT switches were grown on semi-insulating GaAs substrates by

MOCVD. The sketch of the MOS-PHEMT cross section is shown in Fig. 3.4. The structure, from bottom to top, is comprised of a 600 nm GaAs/AlGaAs superlattice buffer layer, a 13 nm undoped $In_{0.2}Ga_{0.8}As$ channel, a 3 nm undoped $Al_{0.25}Ga_{0.75}As$ spacer, a delta-doped layer, a 37 nm undoped $Al_{0.25}Ga_{0.75}As$ barrier layer, a 1.5 nm AlAs etch-stop layer and a 60 nm n^+-GaAs cap layer.

The switches use dual-fingers 0.5 μm gate length MOS-PHEMT. Its processing includes the following steps: mesa isolation, wet chemical recess, oxide deposition, ohmic formation, gate formation, interconnect metallization, and passivation. The mesa isolation was achieved by $H_3PO_4/H_2O_2/H_2O$ solution. The n^+-GaAs cap layer was selectively etched by citric acid/H_2O_2/H_2O solution with AlAs layer as etch stop layer. The AlAs layer was removed by HCl (10 %) solution. Then, the AlGaAs was treated with $(NH_4)_2S_x$ at 60 ℃ for 30 mins before Al_2O_3 deposition [33]. $(NH_4)_2S_x$ treatment before ALD Al_2O_3 deposition can reduce the interface trap density between oxide and semiconductor and form a thin layer 5 ± 1 Å of sulfide on the surface [34], which results in further reduction of device leakage current. After $(NH_4)_2S_x$ treatment, 16 nm Al_2O_3 was deposited at 300 ℃ as gate dielectric by ALD and was annealed at 500 ℃ for 60 s in forming gas. Ohmic contacts were Au/Ge/Ni/Au and were annealed at 410 ℃ for 30 s. Ti/Pt/Au gate metal was formed on Al_2O_3 layer. PECVD Si_3N_4 was used as the dielectric layer for the capacitors and for final passivation. The interconnect metals are comprised of a Ti/Pt adhesion layer with 2 μm plated Au.

FIGURES

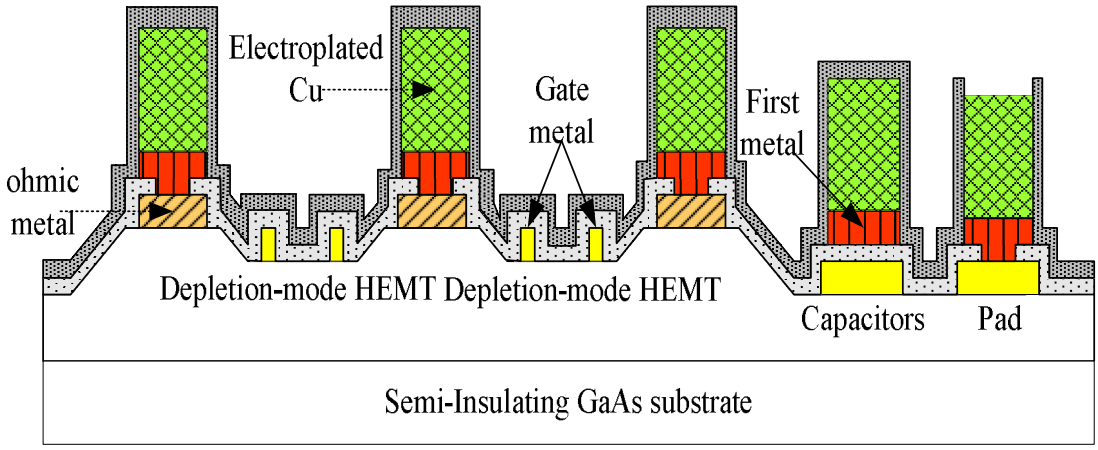


Figure 3.1 Schematic cross section of the PHEMT switch.

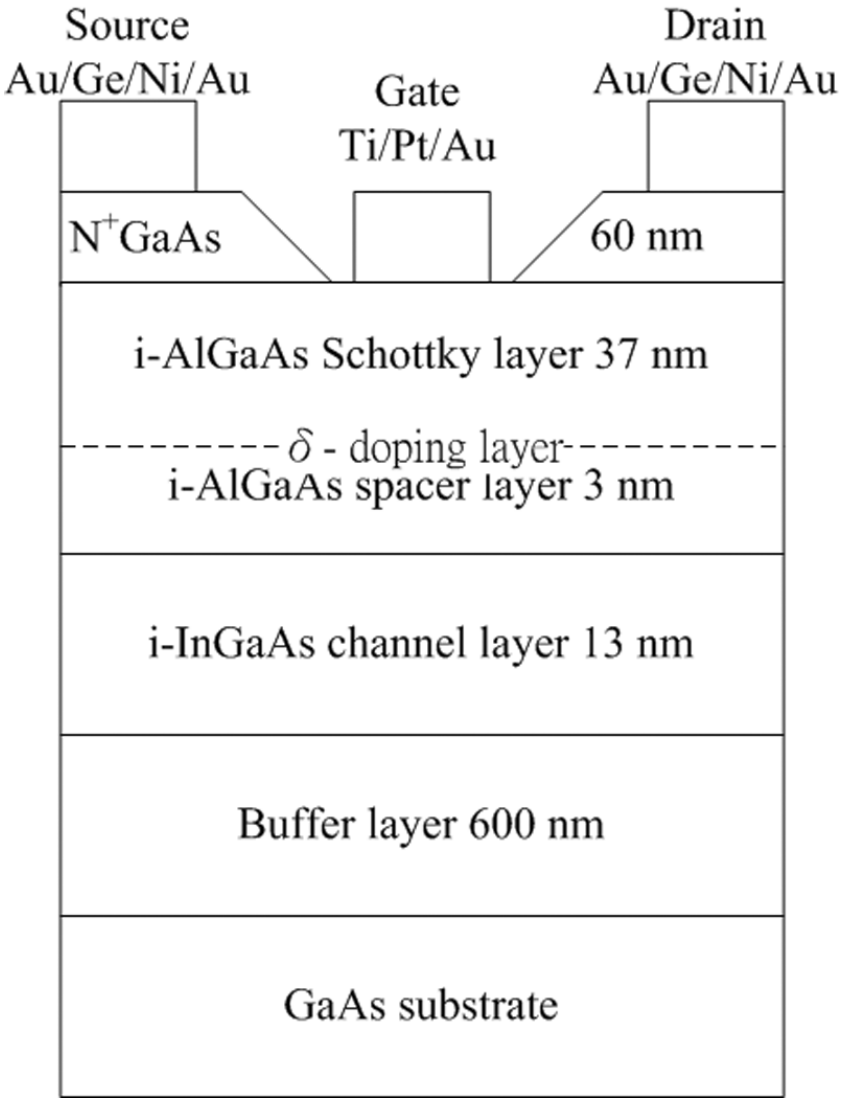


Figure 3.2 Epitaxy structure of the PHEMT used in the Cu-metallized AlGaAs/InGaAs SPDT switches.

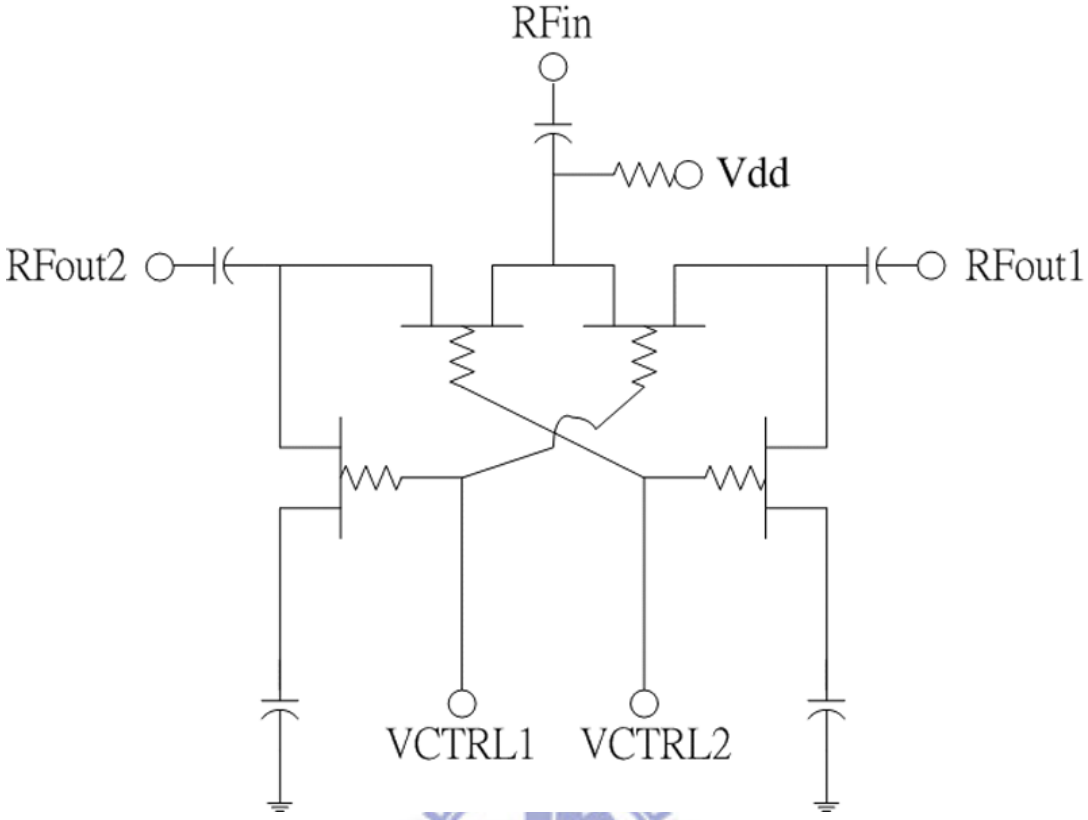


Figure 3.3 Circuit schematic of the series/shunt SPDT switch.

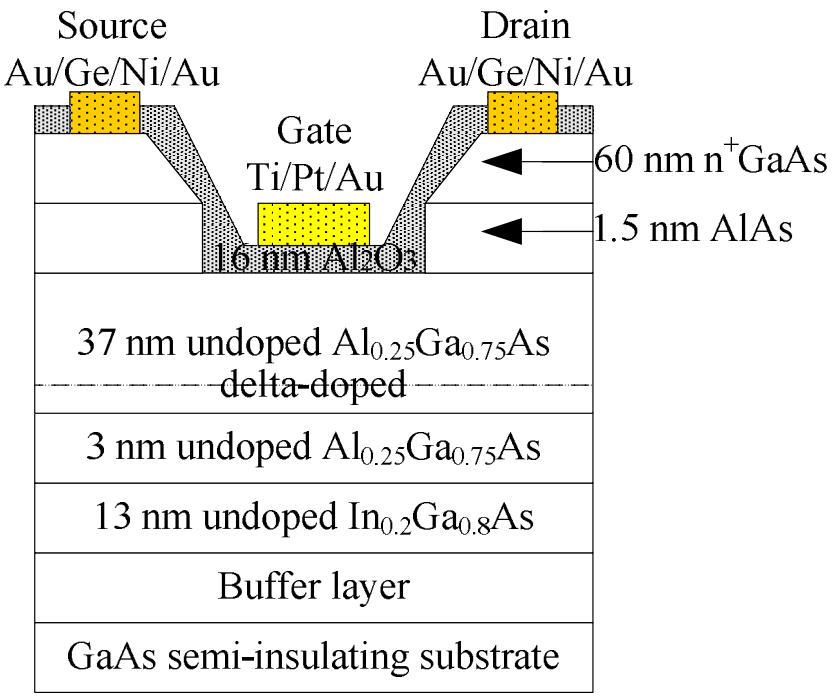


Figure 3.4 Sketch of the MOS-PHEMT cross section.

Chapter 4

SPDT GaAs Switches with Copper-Metallized Interconnects

4.1 Introduction

The Cu metallization process has been widely used in Si integrated circuit technology since IBM announced its success with Cu metallization in the Si very large scale integration process [1, 2, 3]. Traditionally, Ti/Au interconnect metal is widely used for the fabrication of GaAs based field effect transistors and MMICs and the reliability of the metal system has been well proven. In this study, we use Cu metal instead of Au metal as the interconnect metal for the AlGaAs/InGaAs PHEMT SPDT switches. The employment of Cu as the metallization metal has several major advantages over Au, such as lower resistivity, higher thermal conductivity, and lower cost.

Nevertheless, Cu diffuses very fast into GaAs if without any diffusion barrier and forms a deep acceptor to capture carrier in GaAs. It will lead to the failure of the electrical properties of the GaAs devices. In our previous research, we have demonstrated backside Cu metallization on GaAs MESFET using TaN as the diffusion barrier [9], Cu airbridge on low noise GaAs HEMTs using WN_x as the diffusion barrier [11], and fully Cu metallized InGaP/GaAs HBT using Pt as the diffusion barrier [12]. In this study, we choose Pt as the diffusion barrier metal since Pt is commonly used as the plate metal for the MIM capacitor of the switch. The Pt diffusion barrier was very effective in preventing Cu from diffusing into the conventional Schottky and ohmic metal in this study. The fabrication and the electrical performance of the SPDT MMIC switches using Cu metallization technology are reported for the first time.

4.2 Results and discussion

The switch developed in this study can be used in the WLAN system for switching between the transmitting and receiving modes. In this study, the series/shunt SPDT switch uses 0.5-μm gate length, dual-fingers AlGaAs/InGaAs PHEMTs. The gate resistor between the signal and control terminal has a value of 3 kΩ. Fig. 3.3 presents the circuit schematic of the series/shunt SPDT switch in Chapter 3. When the control voltage 1 (V_{CTRL1}) is biased at 3 V and the control voltage 2 (V_{CTRL2}) at 0 V, the RF signal is flowing from RF_{in} to RF_{out1}. Oppositely, the RF signal path is from RF_{in} to RF_{out2} as V_{CTRL1} is biased at 0 V and V_{CTRL2} at 3 V.

Compared with the HEMTs in the switch fabricated with conventional Au interconnects, the HEMTs in the switch fabricated using Cu metallization in this study showed similar DC characteristics. The HEMTs used in the Cu-metallized SPDT switches exhibited a drain saturation current density of 160 mA/mm and a transconductance of 140 mS/mm at V_{DS} = 3 V. The devices had threshold voltage of -1.5 V. The performances of insertion loss and isolation of the SPDT switches with Cu metallization and with Au metallization were measured at 2.5 GHz, respectively, and the results are as shown in Fig. 4.1. The Cu-metallized switch had an insertion loss of 0.33 dB and an isolation of 36.7 dB (control voltage = +3/0 V, input power = 0 dBm) at 2.5 GHz. The results in the RF characteristics showed very little deviation for the switches with Cu interconnects and the switches with Au interconnects. The deviation of these two switches is primarily due to the nonuniformity of the wet chemical etch in the gate recess process, which may influence the on-state resistance and off-state capacitance of the transistor dominating insertion loss and isolation. These RF results were consistent with the DC characteristics, which indicates that the use of Cu metallization would not increase the on-state resistance and the off-state capacitance of the active channel of the transistors and implies that the Cu

metallization could be applied to the interconnects of the SPDT switches without effecting the switch performance.

4.3 Reliability test

To test the thermal stability of the Pt diffusion barrier for long-term period, the Cu-metallized switches were annealed at 250 ℃ for 20 h, the DC characteristics of the HEMT device in the circuits after annealing are shown in Figs. 4.2 and 4.3. Although small degradation of the ohmic contact resistance was observed in Fig. 4.3, the drain saturation current density and the extrinsic transconductance of the device were not obviously influenced with very little change after annealing at 250 ℃ for 20 h, as shown in Figs. 4.2 and 4.3 (less than 1 % difference in drain saturation current density and less than 3 % difference in extrinsic transconductance). These results indicate that Cu–Pt interconnect layers are quite stable and that Pt is an effective diffusion barrier against Cu diffusion after thermal annealing. Thus, the Cu-metallized SPDT switches have maintained the electrical performance without any significant change during the high-temperature ambient test. Overall, the Cu-metallized SPDT switches have sustained the high temperature environment test without obvious DC performance degradation.

The RF performance of the Cu-metallized switches was also evaluated at high temperature. As shown in Fig. 4.4, the switch has an insertion loss of 0.33 dB and an isolation of 36.7 dB at 2.5 GHz before thermal test. After 144 h of high temperature storage life (HTSL) evaluation at 150 ℃ under nitrogen atmosphere, the Cu-metallized switches still possessed very good reliability with similar RF performance. The P_{out}–P_{in} relationships of the Cu-metallized switches at 2.5 GHz after annealing at 150 ℃ under nitrogen atmosphere for different annealing time are as shown in Fig. 4.5. Input P_{1dB} was kept at about 27 dBm without significant change

and maintained the same level without any obvious degradation after the long term test. Fig. 4.6 reveals that input third-order intermodulation intercept point (input IP3) of 50 dBm can be achieved at the input power of 15 dBm, and the trend of control current still remained stable. It suggests that no Cu diffusion into the active device region, and no degradation of on-state resistance and power handing capability for the transistors after thermal annealing occurred for the Cu-metallized SPDT switches using Pt as the diffusion barrier. Hence, the Cu-metallized switches demonstrated very good reliability and showed similar switch power handling capability after 144 h of HTSL environment test.

To test the operation reliability of the Cu-metallized switches, the Cu-metallized switches were subjected to an on/off stress test (control voltage = +3/0 V exchange) for 24 h at room temperature. As shown in Fig. 4.7, the Cu-metallized switches showed very little change after the stress test. The insertion loss and isolation still remained stable. Almost no obvious change in the insertion loss and isolation occurred, which indicated that no significant degradation of on-state resistance and off-state capacitance took place. It implies no Cu diffusion into the active device region for the transistors after control voltage exchange stress for the Cu-metallized SPDT switches using Pt as the diffusion barrier.

4.4 Conclusions

An SPDT GaAs switch fabricated with Cu-metallized interconnects using Pt as the diffusion barrier has been reported for the first time. The RF characteristics of the Cu-metallized SPDT switch exhibited an insertion loss of 0.33 dB and an isolation of 36.7 dB at 2.5 GHz, the performance is comparable to the SPDT switches fabricated using conventional Au interconnects. High power handling capability was achieved with input P_{1dB} of 27 dBm and IIP3 of 50 dBm. Based on the high temperature

reliability tests including thermal stress test (annealing at 250 ℃ for 20 h) and HTSL environment test, no significant changes in the DC and RF characteristics were observed for the SPDT switches after these tests. To test the operation reliability of the Cu-metallized switches, the Cu-metallized switches were subjected to an on/off stress test for 24 h at room temperature and showed very little change of the insertion loss and isolation. It is evident from these data that the Cu metallization process developed is very reliable and can be used for the GaAs MMICs fabrication.

FIGURES

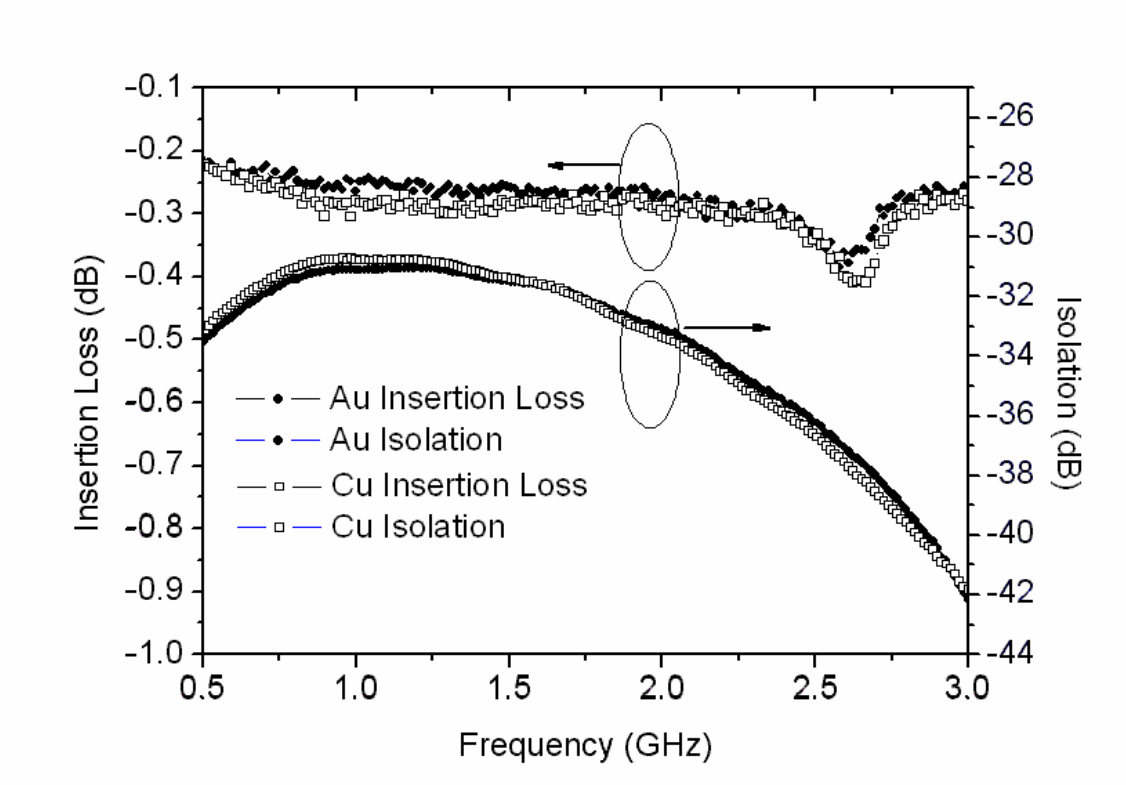


Figure 4.1 Insertion loss and isolation vs frequency of the SPDT switches with Cu and Au metallizations.

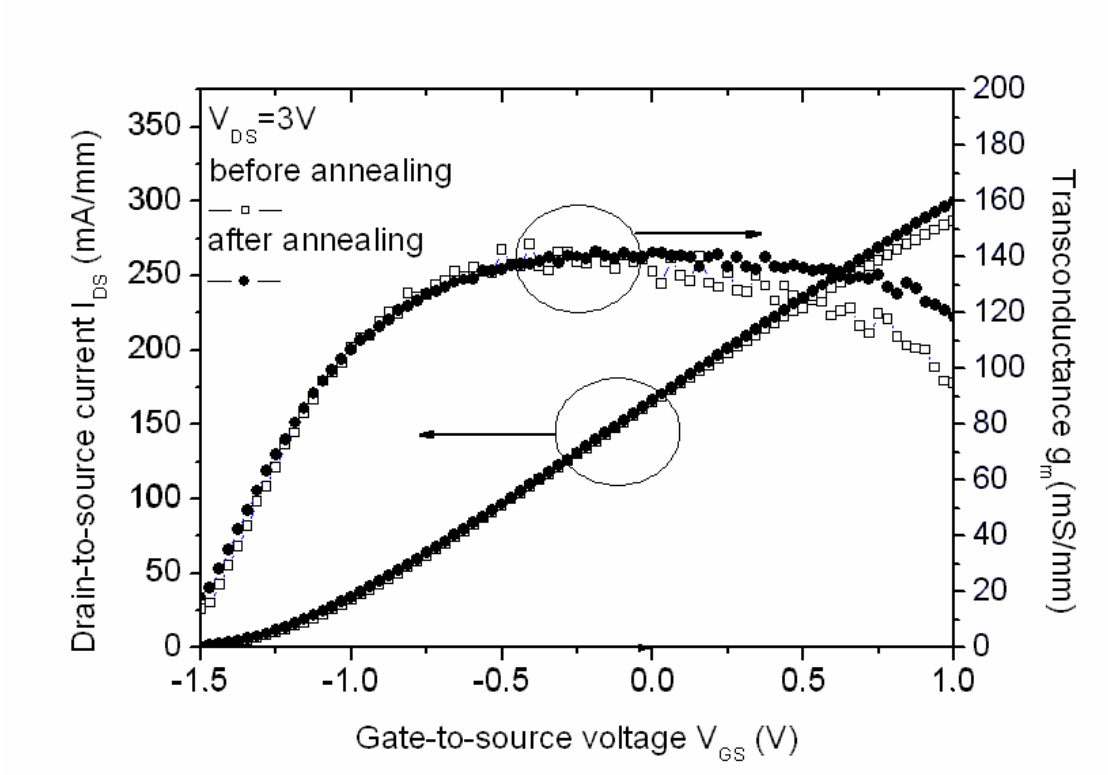


Figure 4.2 Transconductance and drain-to-source current versus V_{GS} bias characteristics of the Cu-metallized AlGaAs/InGaAs PHEMT SPDT switches for 0.5-μm gate length before and after annealing at 250 ℃ for 20 h.

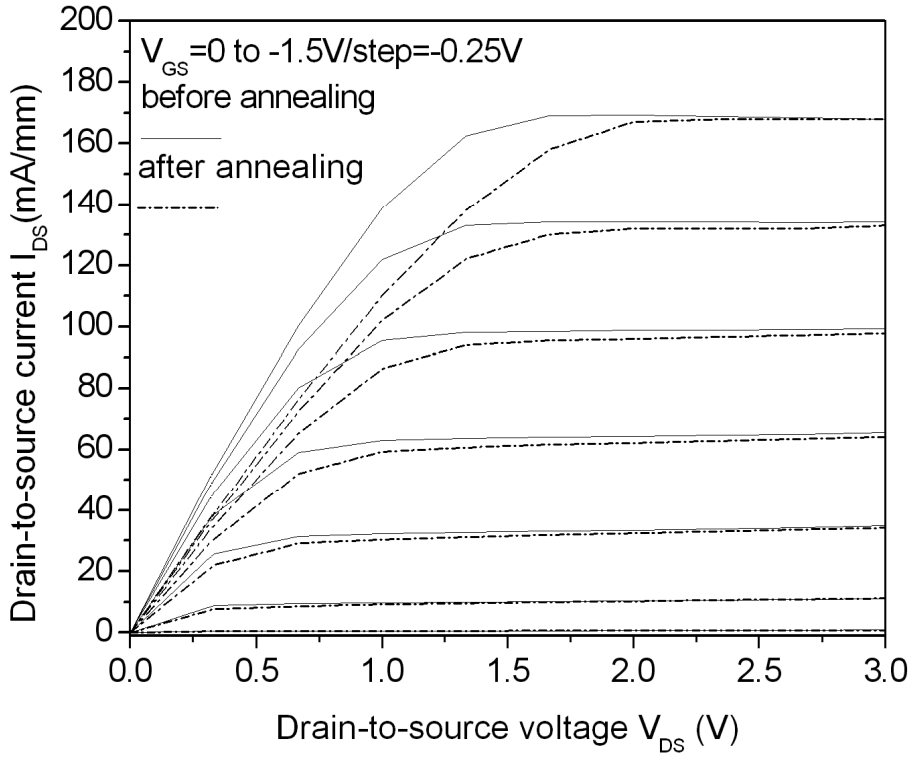


Figure 4.3 I–V characteristics of the Cu-metallized AlGaAs/InGaAs PHEMT SPDT switches for 0.5-μm gate length before and after annealing at 250 ℃ for 20 h.

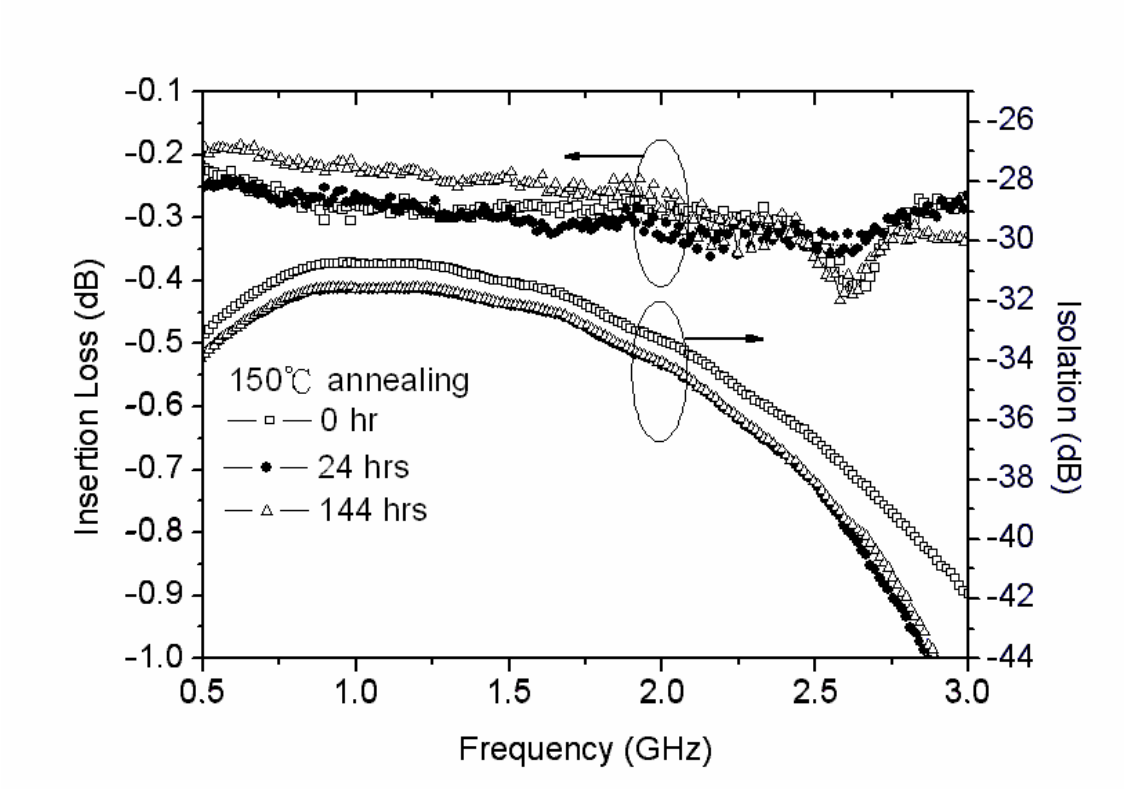


Figure 4.4 Insertion loss and isolation of the Cu-metallized SPDT switches at 2.5 GHz after annealing at 150 ℃ for different hours.

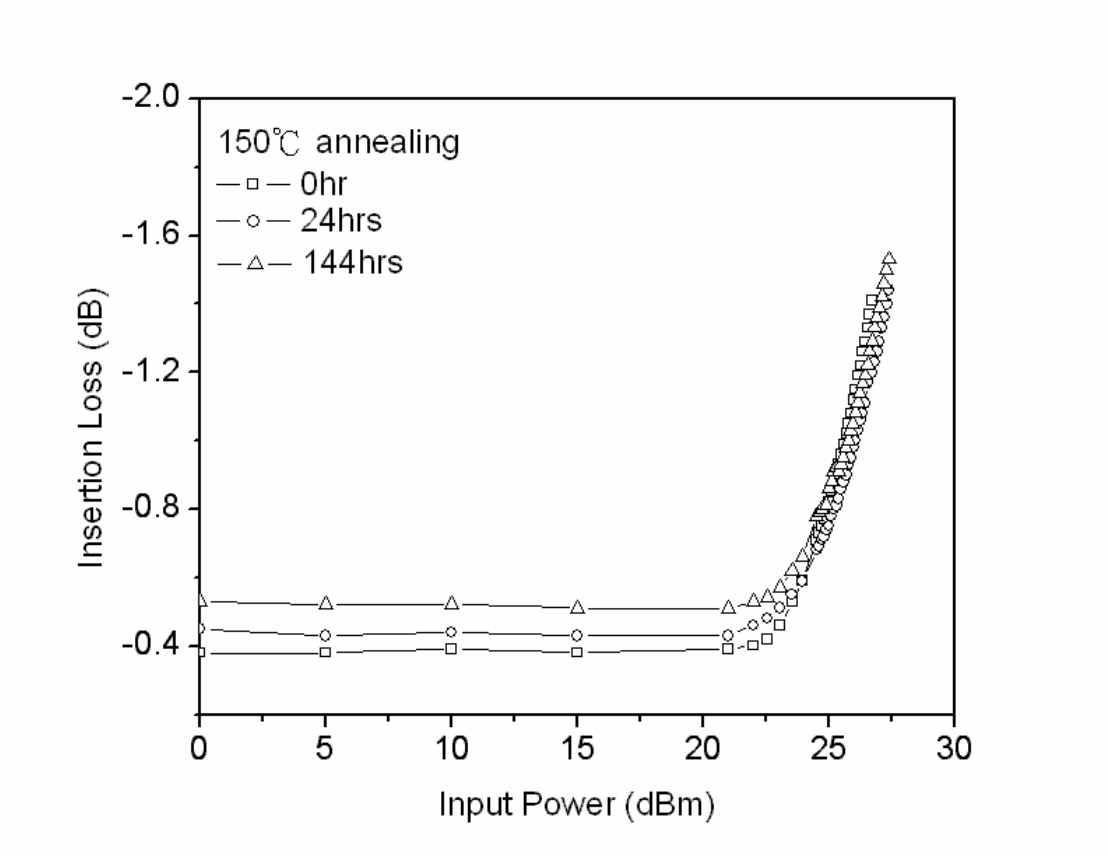


Figure 4.5 Insertion loss of the Cu-metallized SPDT switches with different input power levels at 2.5 GHz after annealing at 150 ℃ for different annealing periods.

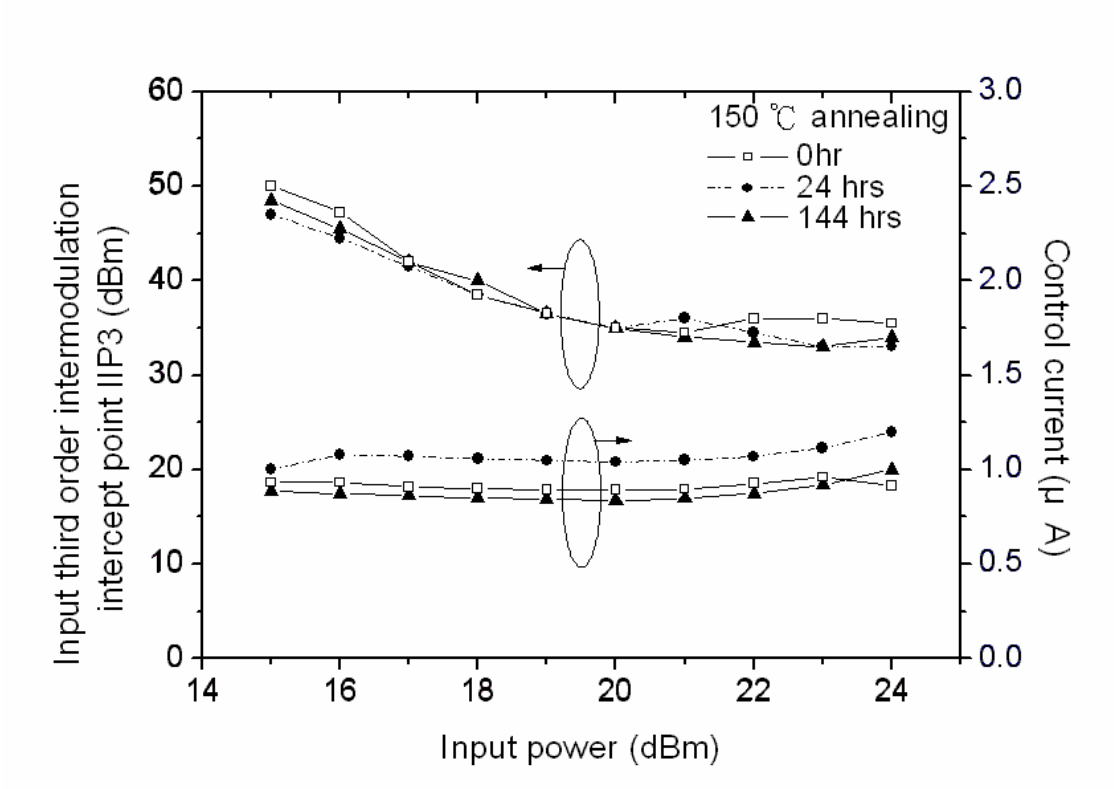


Figure 4.6 Input IP3 and control current of the Cu-metallized SPDT switches with different input power levels at 2.5 GHz after annealing at 150 ℃ for different annealing periods.

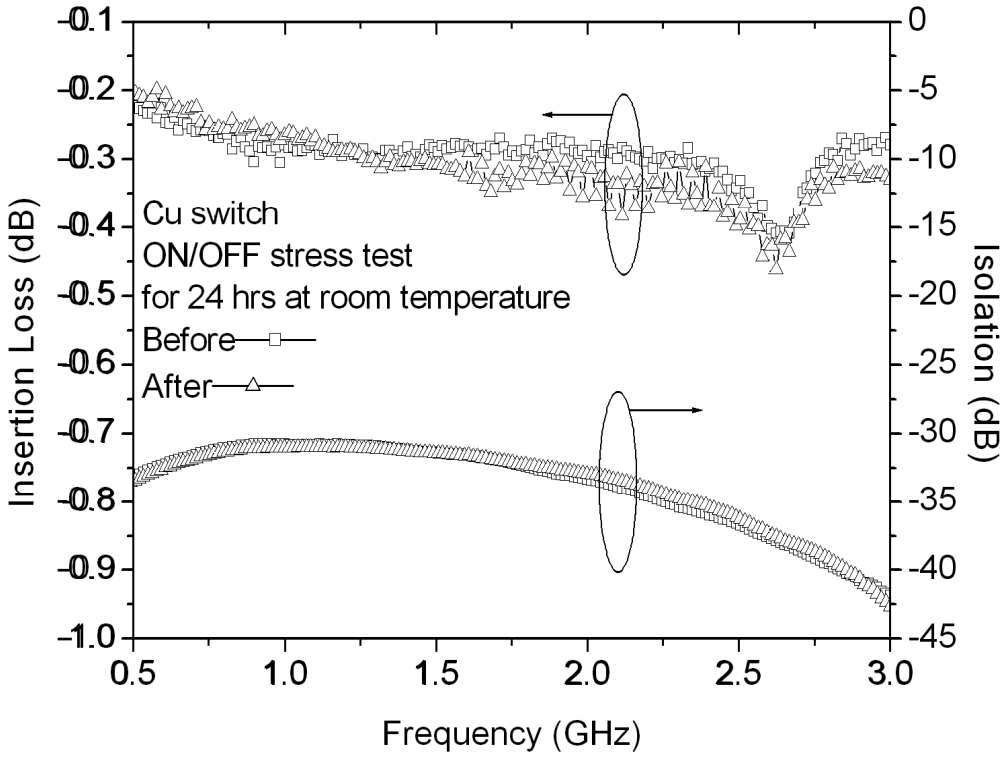


Figure 4.7 Insertion loss and isolation versus frequency of the Cu-metallized AlGaAs/InGaAs 0.5-μm PHEMT SPDT switches before and after on/off stress test for 24 h at room temperature.

Chapter 5

Evaluation of Electrical Characteristics of the Copper-Metallized SPDT GaAs Switches at Elevated Temperatures

5.1 Introduction

Cu has been used instead of Al as the interconnect metal for Si integrated circuit technology since IBM adapted Cu metallization in the Si 0.18-μm technology [1, 2, 3]. The advantages of using Cu metallization for Si technology include low resistivity and high electromigration resistance; however, there are only a few reports on the Cu metallization of GaAs devices. Ti/Au interconnect metal has been extensively used for the manufacture of GaAs-based field-effect transistors and MMICs, and the reliability of the metal system has been well proven. The application of Cu as the metallization metal for GaAs devices has several superior advantages over Au, such as lower resistivity, higher thermal conductivity, and lower cost, as compared with Au. In this paper, we characterized the electrical performance of the Cu-metallized AlGaAs/InGaAs PHEMT SPDT switches and compare the performance with the Au-metallized GaAs SPDT switches.

Cu diffuses very fast into GaAs if without any diffusion barrier and forms a deep acceptor in GaAs, which leads to the failure of the electrical properties of the GaAs devices. It was previously demonstrated that TaN can be used as the diffusion barrier for the backside Cu metallization on GaAs MESFETs [9, 10] and that WN_x can be used as the diffusion barrier for Cu airbridges on low-noise GaAs HEMTs [11]. Furthermore, Pt was used as the diffusion barrier layer for Cu-metallized switches [13], and an Au-free fully Cu-metallized InP HBT was also realized using Ti/Pt/Cu nonalloyed ohmic contacts with Pt as the diffusion barrier [14]. It has also been demonstrated that the Ti/Pt/Cu system structure was very stable even after being

annealed up to 350 ℃ and that Cu started to diffuse through the Pt diffusion barrier and formed a Cu_4Ti phase after being annealed at 400 ℃, as investigated by X-ray diffraction data, Auger electron spectroscopy depth profiles, and the sheet resistance measurement [12]. In this paper, the temperature-dependent characteristics of the Cu-metallized switches are studied. The thermal stability of the Pt diffusion barrier and the electrical reliability are also investigated.

5.2 Results and discussion

The HEMTs in the switch fabricated using Cu metallization showed similar DC characteristics in comparison with those in the switch fabricated with traditional Au metallization. As shown in Figs. 5.1 and 5.2, a drain saturation current density of 160 mA/mm and an extrinsic transconductance of 140 mS/mm at V_{DS} = 3 V were measured both for the Cu- and the Au-metallized switches. The devices had a threshold voltage (V_{th}) of −1.5 V. The insertion loss, return loss, and isolation characteristics of the SPDT switches with Cu metallization and with Au metallization measured at 2.5 GHz are shown in Figs. 5.3 and 5.4, respectively. The Cu-metallized switch had an insertion loss of 0.33 dB, a return loss of 23.3 dB, and an isolation of 36.7 dB (control voltage = +3/0 V; input power = 0 dBm) at 2.5 GHz. There is very little difference in the RF characteristics for the switches with Cu interconnects and with Au interconnects. The small differences of these two switches were due to the nonuniformity of the wet chemical etch in the gate recess process. The nonuniformity of the wet chemical etch could cause the fluctuation of the on-state resistance and off-state capacitance of the transistors which dominate insertion loss and isolation [13]. It appears from these data that Cu metallization does not affect the SPDT HEMT switch performance.

In order to evaluate the temperature-dependent effect on the DC and RF

characteristics of the Cu-metallized switches, the switches were evaluated at different temperatures. The DC characteristics of the device were measured at different temperatures from 300 °K to 500 °K. Fig. 5.5 shows the current–voltage (I–V) characteristics at different high-temperature ambients. The extrinsic transconductance and the drain-to-source current versus the temperature for the Cu-metallized SPDT switches were shown in Fig. 5.6. A drain saturation current density of 188 mA/mm and an extrinsic transconductance of 159 mS/mm at V_{DS} = 3 V at 300 °K were measured for the devices. While the background carrier concentration from the substrate rises exponentially with temperature, causing the 2-DEG concentration (n_{2DEG}) to increase in the active layer, the carrier velocity (v) degraded seriously by the lattice scattering and carrier–carrier scattering mechanisms [35]. Therefore, I_{DSS0} drops at high temperatures due to the enhanced scattering mechanisms even though the carrier concentration increases at high temperatures.

Furthermore, the gate leakage current (I_G) as a function of the gate-to-drain voltage (V_{GD}) is shown in Fig. 5.7. When the gate-to-drain voltage was biased at −22 V, the gate leakage currents were 430, 450, and 490 μA/mm at the temperatures of 300 °K, 380 °K, and 500 °K, respectively. The gate leakage current increases with increasing temperature mainly due to the tunneling mechanism with thermionic emission and partly caused by the reduction of barrier height [36].

Fig. 5.8 shows that the V_{th} decreases with increasing temperature. The V_{th} of a δ-doped HEMT can be obtained by solving the 1-D Poisson's equation (5.1) as follows [35, 37]:

$$V_{th} = \frac{\Phi_B}{q} - \frac{\Delta E_c}{q} - \frac{n_{2DEG}(d_d + \Delta d)}{\varepsilon} \tag{5.1}$$

Among the aforementioned parameters, Φ_B is the Schottky gate barrier height, ΔE_c is the conduction-band discontinuity between the Schottky layer and the InGaAs

channel, d_d is the distance between the gate and the n_{2DEG} location, ($d_d + \Delta d$) is the effective distance between the gate and the n_{2DEG} location, and ε is the permittivity of the Schottky layer. Based on Eq. (5.1), when the temperature is increased, the threshold voltage decreases owing to the increase of the intrinsic channel carrier concentration n_{2DEG} [35] and the lowering of the Schottky barrier height [38, 39]. Moreover, the decrease of V_{th} is partly caused by the leakage current from a semi-insulating substrate with increasing temperature [36]. Based on the relationship of $V_{th} = V_{th0} - K(T - T_0)$, V_{th} is relatively temperature insensitive. The V_{th} shift from 300 °K to 500 °K was only −0.05 V, and $\delta V_{th}/\delta T = -0.25$ mV/°K as a result.

As shown in Fig. 5.8, the maximum extrinsic transconductance ($g_{m,max}$) decreases with increasing temperature, which is attributed to the decrease of the intrinsic transconductance [35] and the increase of the ohmic contact resistance [40], respectively. Therefore, it can be seen that when the temperature is increased, the degradations of the device performance include the increase of the leakage current and the decrease of the breakdown voltage, threshold voltage, extrinsic transconductance, and drain saturation current density.

Furthermore, RF performances of the device were measured at high temperatures. Fig. 5.9 shows the insertion loss and isolation versus frequency of the SPDT switches with Cu metallization from 300 °K to 380 °K. The isolation characteristics of the Cu-metallized switches degrades slightly because of the increase of the leakage current from the semi-insulating substrate with increasing temperature. For this reason, the isolation is closely related to the off-state threshold characteristics which were affected by the leakage current. Although isolation of the Cu-metallized switch was influenced by the thermal effect, it still maintained excellent isolation value higher than 35 dB.

In addition, the transistor had a small on-state resistance which resulted in low

insertion loss. However, the on-state resistances of the Cu-metallized switches measured at V_{GS} = 0 V and V_{DS} = 0.5 V increased gradually from 300 °K to 500 °K, as shown in Fig. 5.10. The series resistance increased as the source, drain, and gate resistances increased with increasing temperature because of the carrier scattering [41] which would result in the reduction of the carrier transport velocity (υ) and the electron mobility (μ_e) in the channel due to the lattice scattering and carrier–carrier scattering at elevated temperatures [35]. The degradation of on-state resistance was also caused by the increase of the electrode contact resistance with temperature as verified in the previous reports [42]. This phenomenon led to the slight degradation of the insertion loss, but the increase in the insertion loss from 300 °K to 380 °K was only 0.08 dB, as shown in Fig. 5.9. Overall, for high-temperature operation, the Cu-metallized switch had an insertion loss of 0.46 dB and an isolation of 42.79 dB (control voltage = +3/0 V; input power = 0 dBm) when tested at 2.5 GHz at 380 °K. It demonstrates that the Cu metallization can be applied to the interconnects of the SPDT switches at high temperatures without affecting the switch performance.

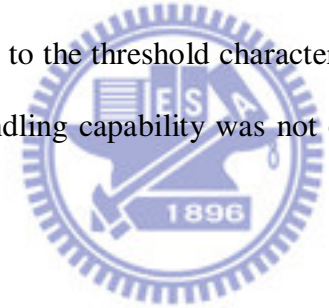
Fig. 5.11 shows the thermal effect on the switching time for the Cu-metallized switches. The switching time increases with increasing temperature primarily due to the degradation of the on-state resistance.

The power limitation of the switch operation is as explained in [17, 19, 26, 32], and the maximum input power P_{max} is expressed as in Chapter 2:

$$P_{\max} = \frac{(V_C - V_{th})^2}{2Z_0} \tag{2.7}$$

where Z_0 is the line impedance and V_c is the absolute of the control voltage. It indicates that small threshold voltage and higher control voltage can improve the power handling capability of the FET switch. The input P_{1dB}, the second and third harmonic characteristics of the Cu-metallized switches as a function of temperature

measured at 2.5 GHz are shown in Fig. 5.12. The value of the input P_{1dB} with different temperatures remained considerably steady because the threshold voltage shift was small and did not influence the power handling capability. The characteristics of the second and third harmonics from 300 °K to 380 °K under the input power of 20 dBm are shown in Fig. 5.12. The second and third harmonics of the device remained quite stable during this temperature range. The harmonic performance is highly associated with power handling capability [20], and the input P_{1dB} was kept at about 28.4 dBm in the current case. Fig. 5.13 shows the IIP3 versus different temperatures under several input power conditions. The IIP3 value of the device was kept at different temperatures. IIP3 of 40.5 dBm was achieved at 380 °K when the input power was 20 dBm. Based on the aforementioned results, it can be seen that the power handling capability was closely related to the threshold characteristics and that the temperature dependence of the power handling capability was not obviously from 300 °K to 380 °K.



5.3 Conclusions

An SPDT GaAs switch fabricated with Cu-metallized interconnects using Pt as the diffusion barrier has been fabricated and investigated. The Cu-metallized SPDT switch exhibited an insertion loss of 0.33 dB, a return loss of 23.3 dB, and an isolation of 36.7 dB at 2.5 GHz; the performance is comparable with the performance of the traditional Au-metallized SPDT switches. The input P_{1dB} of 28.3 dBm at 2.5 GHz was obtained for these switches. Moreover, the temperature-dependent effects on the insertion loss, isolation, switching characteristics, and power handling capability of the Cu-metallized switches using Pt as the diffusion barrier have also been investigated. The RF characteristics of the Cu-metallized SPDT switch still remained quite stable and exhibited a low insertion loss of 0.46 dB, an excellent isolation of

42.79 dB, a high input P_{1dB} of 28.45 dBm, and a high IIP3 of 40.5 dBm at 2.5 GHz when tested at 380 °K. These results show that the Cu metallization process using Pt as the diffusion barrier is a very reliable process and can be applied to the GaAs MMIC switch fabrication.

FIGURES

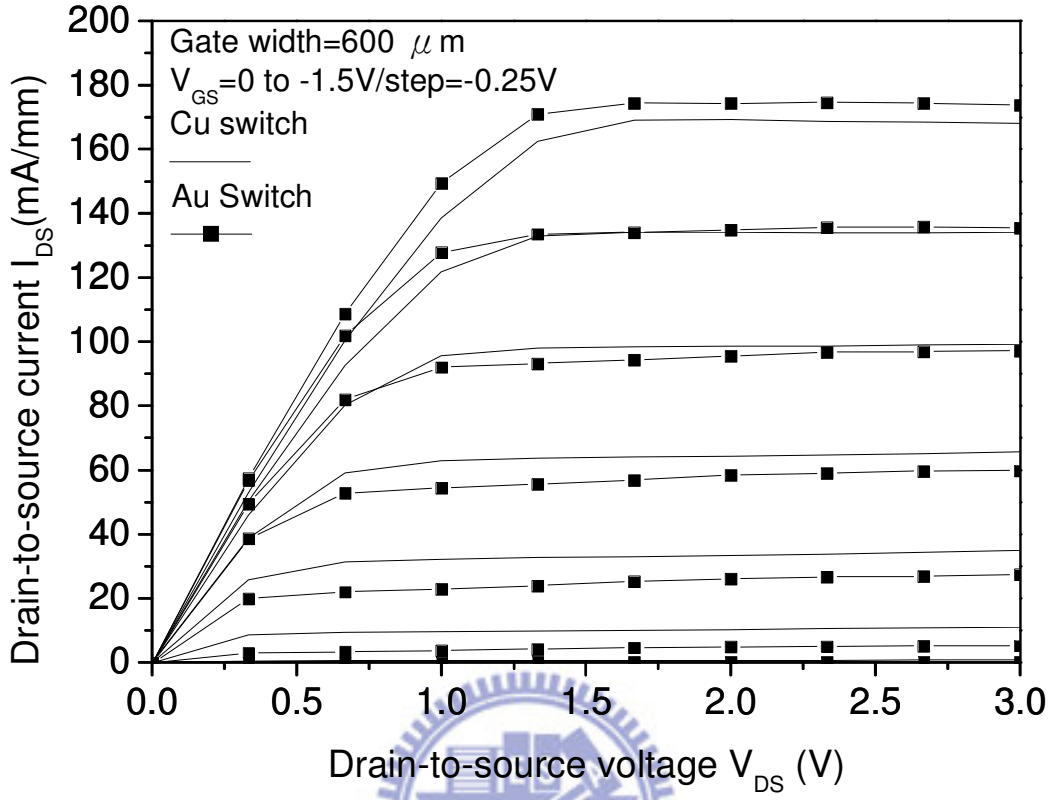


Figure 5.1 I–V characteristics of AlGaAs/InGaAs PHEMT SPDT switches for 0.5-μm gate length with Cu and Au metallizations.

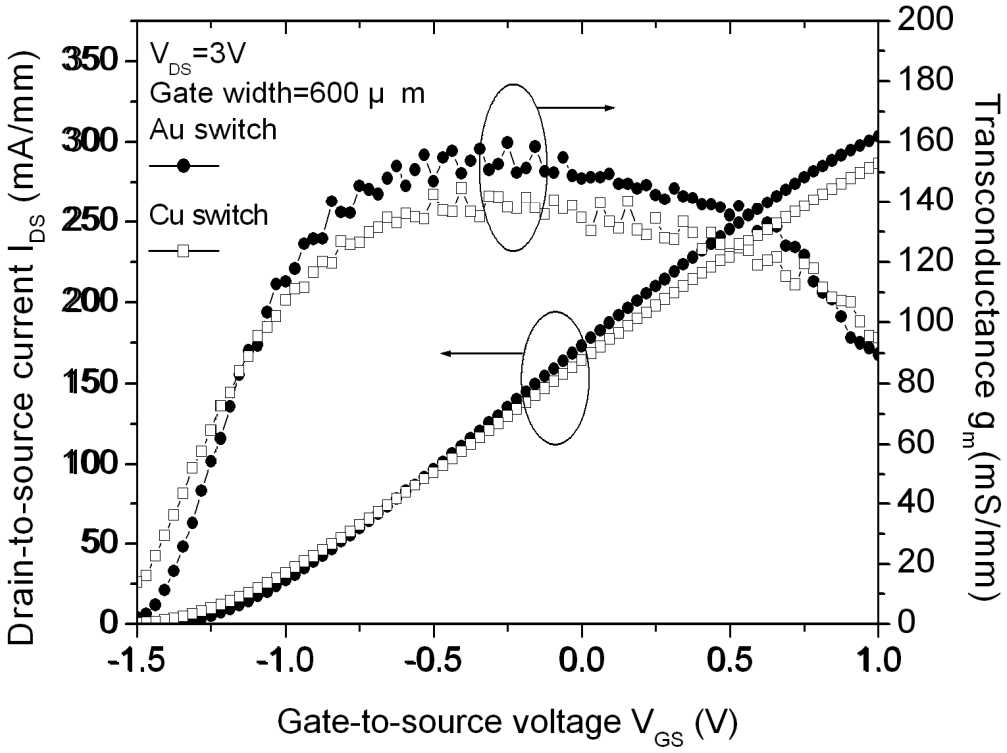


Figure 5.2 Extrinsic transconductance and drain-to-source current versus V_{GS} bias characteristics of the AlGaAs/InGaAs PHEMT SPDT switches for 0.5-μm gate length with Cu and Au metallizations.

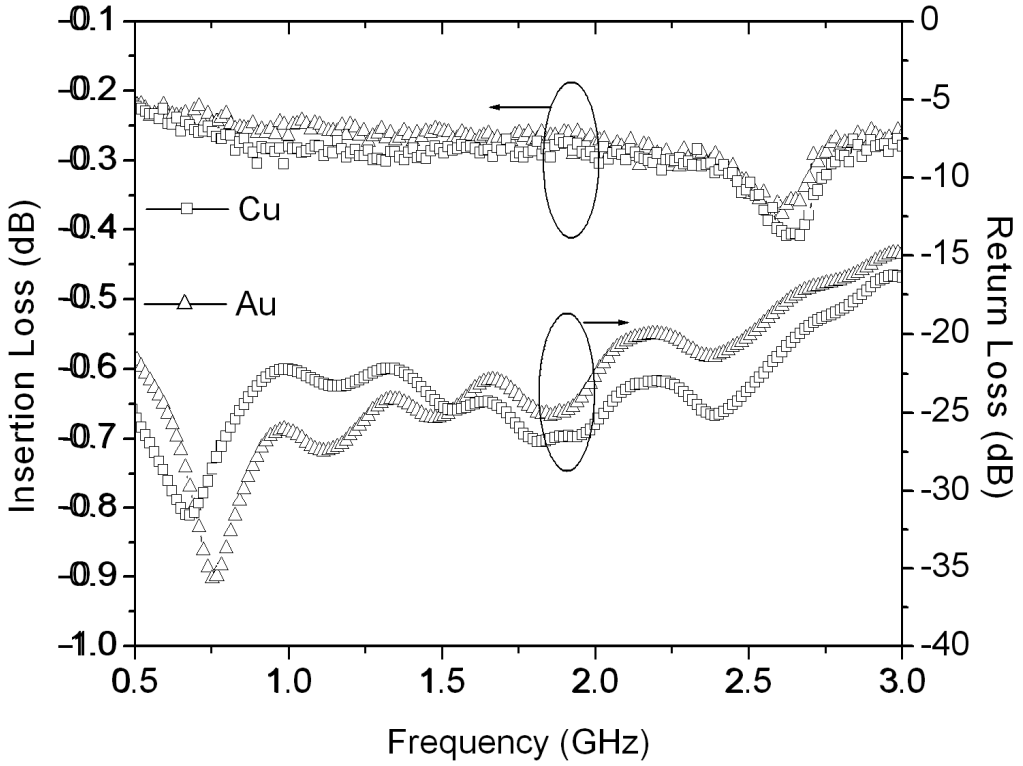


Figure 5.3 Insertion loss and return loss versus frequency of the SPDT switches with Cu and Au metallizations.

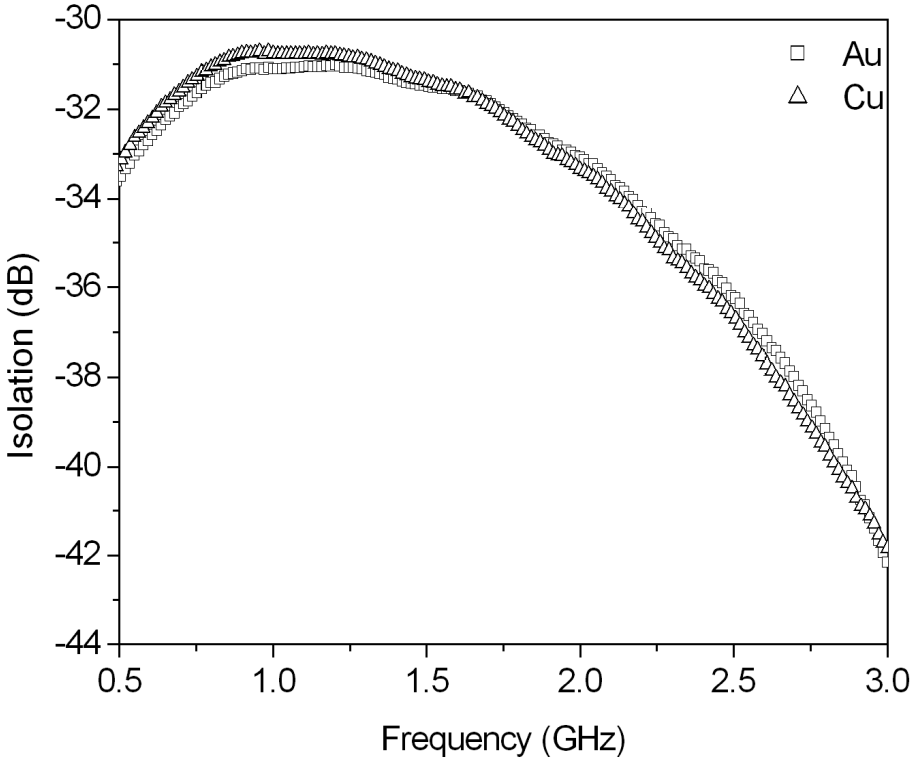


Figure 5.4 Isolation versus frequency of the SPDT switches with Cu and Au metallizations.

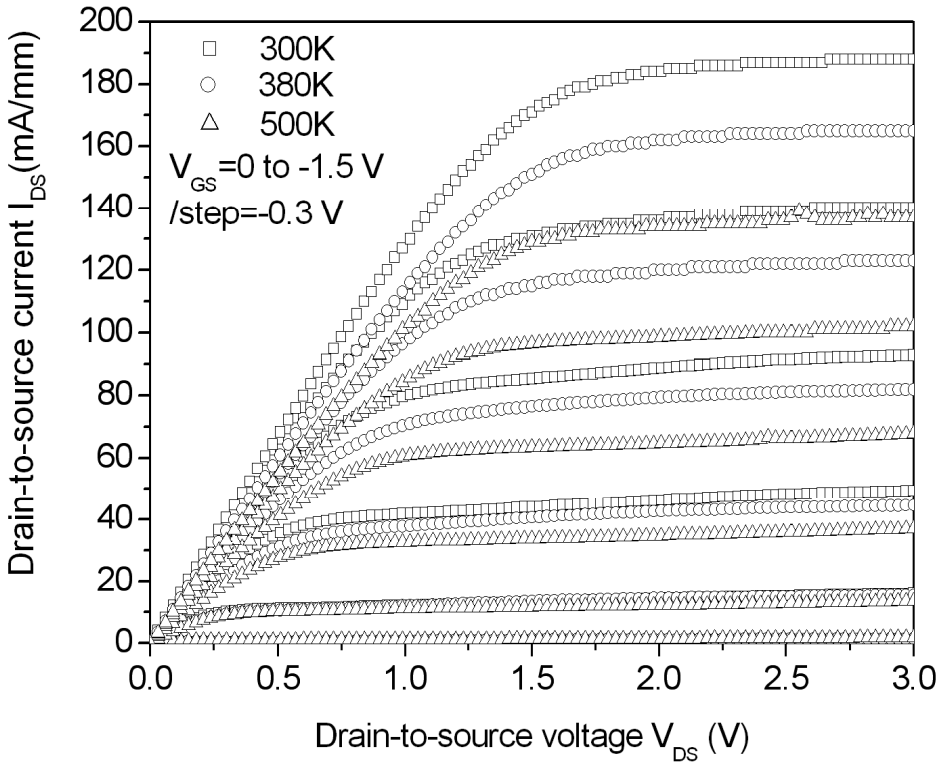


Figure 5.5 I–V characteristics of the 0.5-μm gate length PHEMT used in the Cu-metallized switches tested at 300 °K, 380 °K, and 500 °K, respectively.

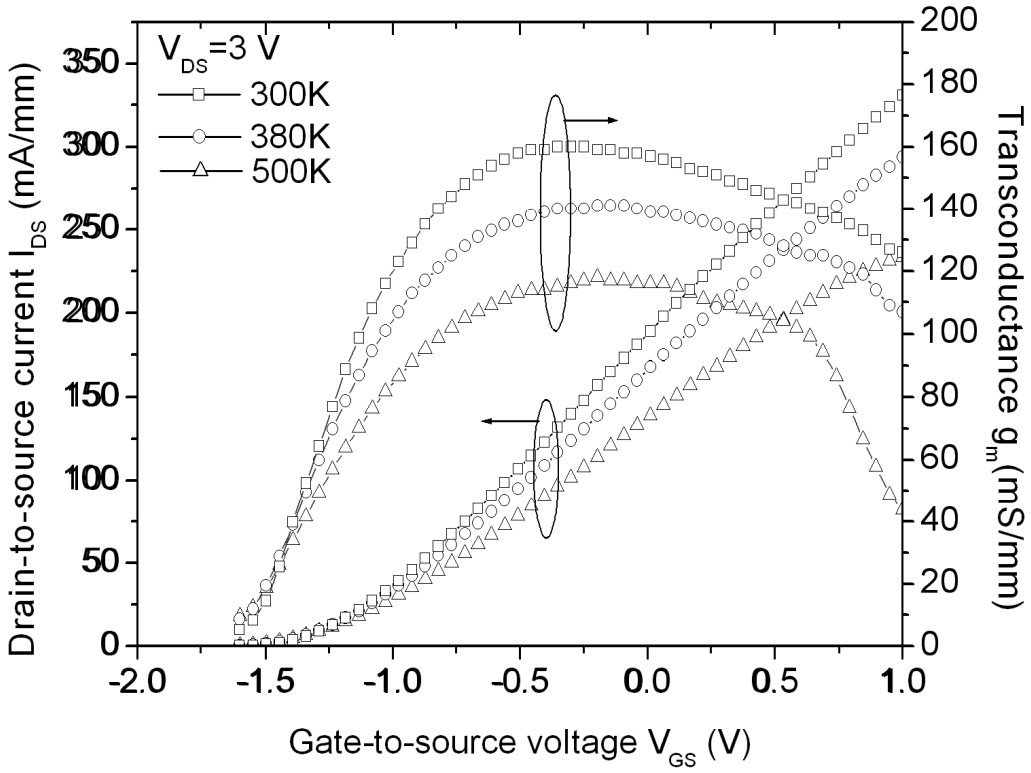


Figure 5.6 Extrinsic transconductance and drain-to-source current versus V_{GS} bias characteristics of the 0.5-μm gate length PHEMT used in the SPDT switches when measured at 300 °K, 380 °K, and 500 °K, respectively.

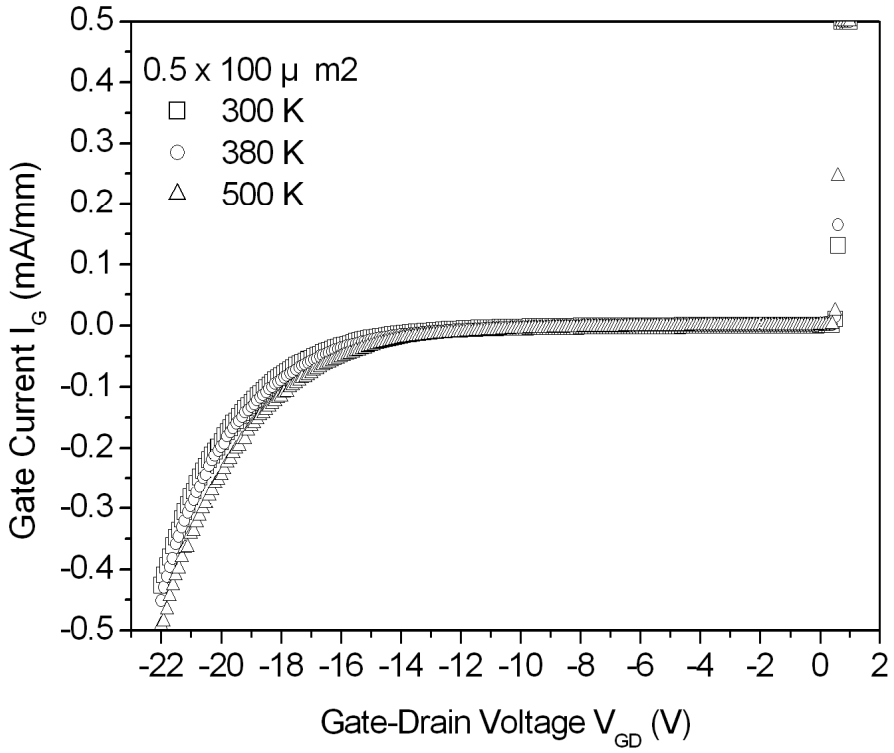


Figure 5.7 Gate leakage current (I_G) as a function of the gate-to-drain voltage (V_{GD}) for the PHEMTs used in the switches when tested at 300 °K, 380 °K, and 500 °K.

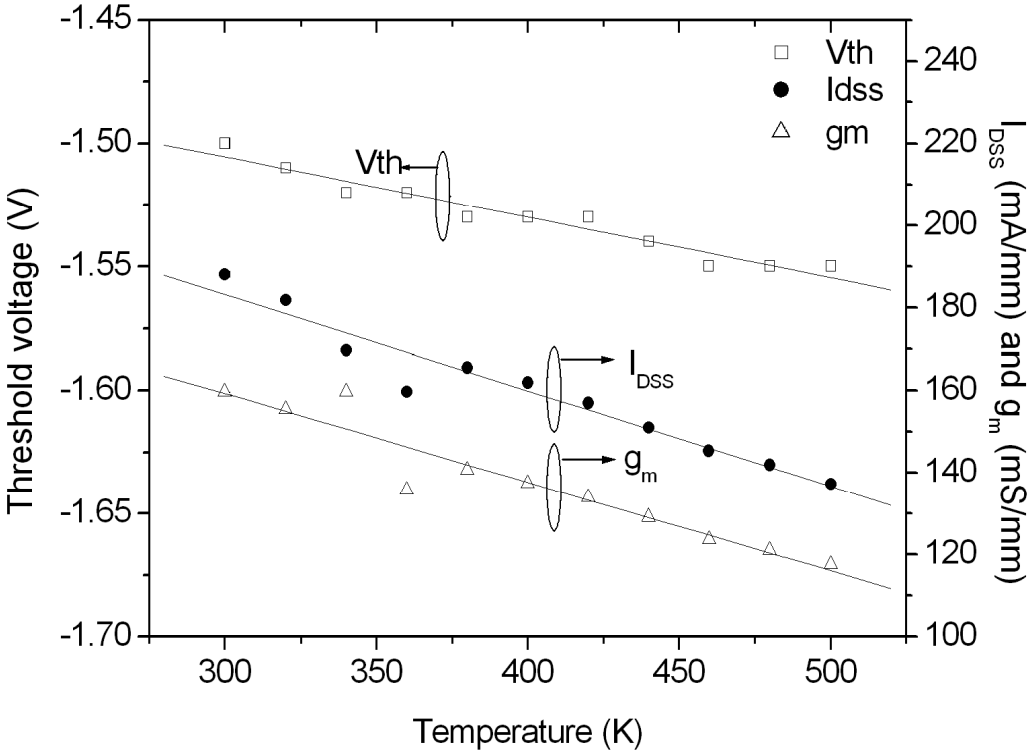


Figure 5.8 Threshold voltage (V_{th}), drain saturation current density (I_{dss}), and extrinsic transconductance (g_m) characteristics as a function of temperature for the Cu-metallized AlGaAs/InGaAs PHEMT used in the SPDT switches.

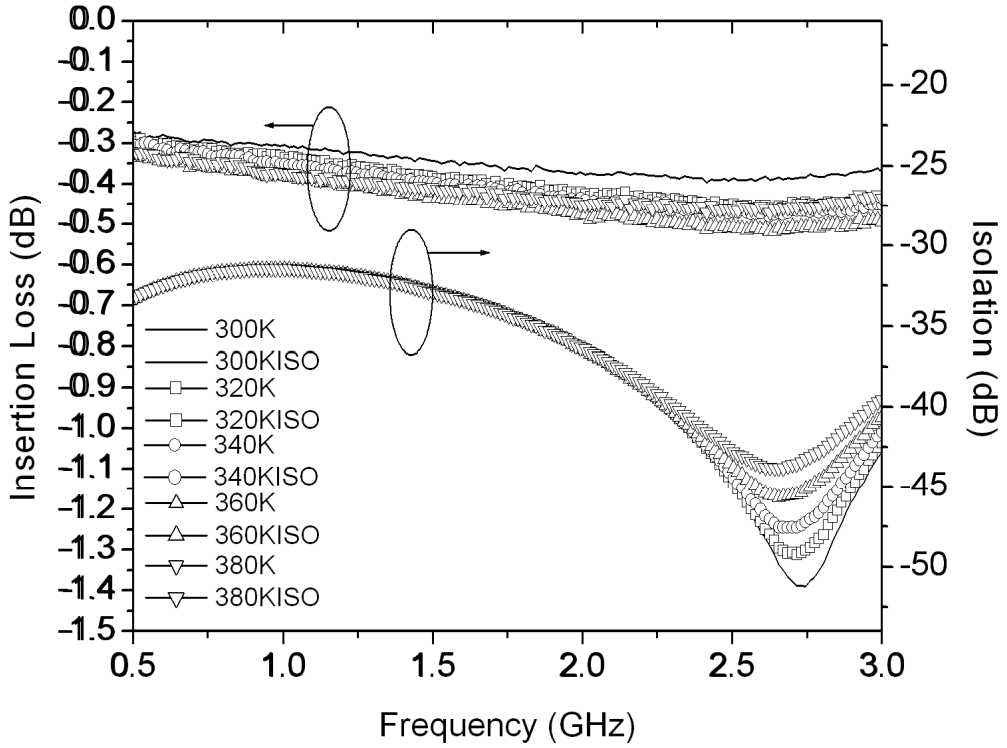


Figure 5.9 Insertion loss and isolation versus frequency of the Cu-metallized SPDT switches measured from 300 °K to 380 °K.

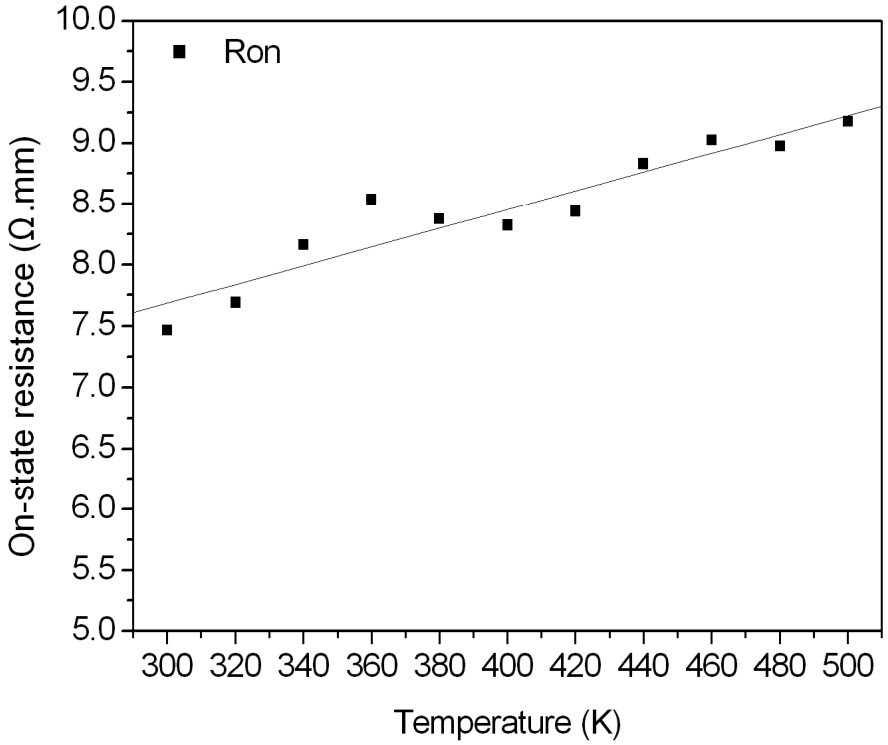


Figure 5.10 On-state resistance as a function of temperature for the SPDT switches.

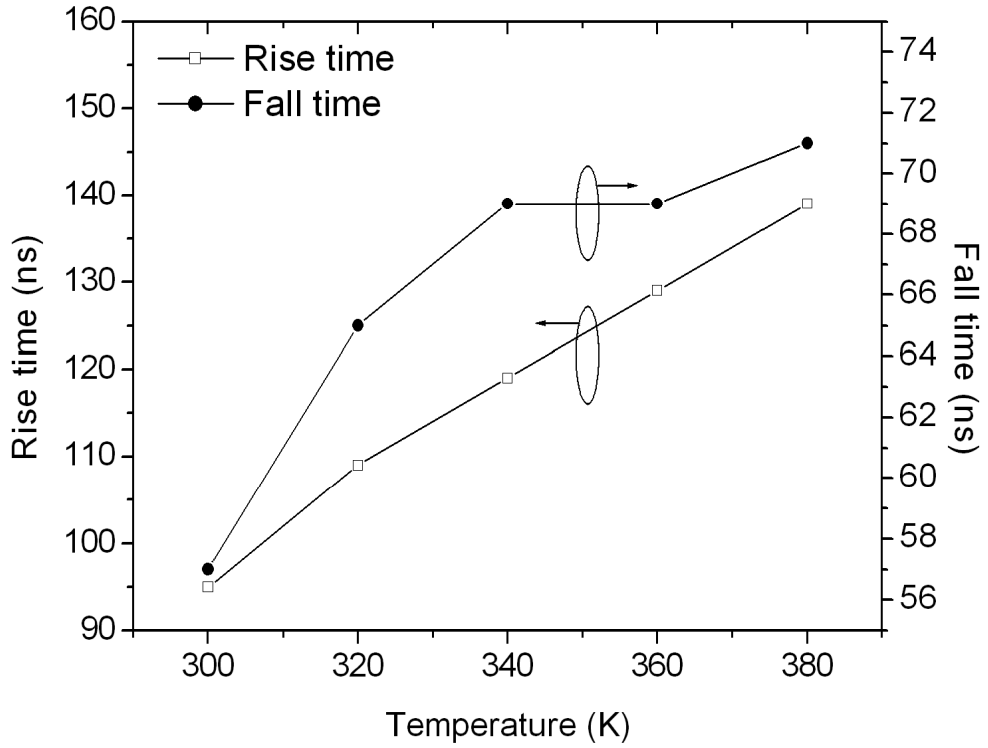


Figure 5.11 Switching time as a function of temperature at 2.5 GHz for the SPDT switches.

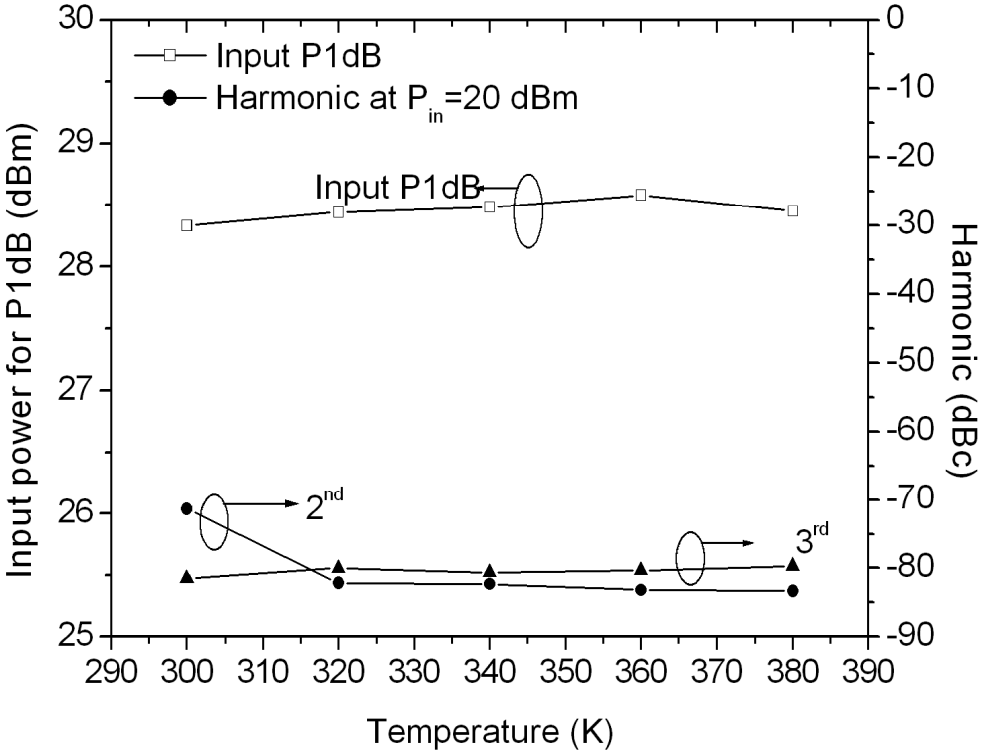


Figure 5.12 Input power 1-dB compression and second and third harmonic characteristics for the SPDT switches as a function of temperature when tested at 2.5 GHz.

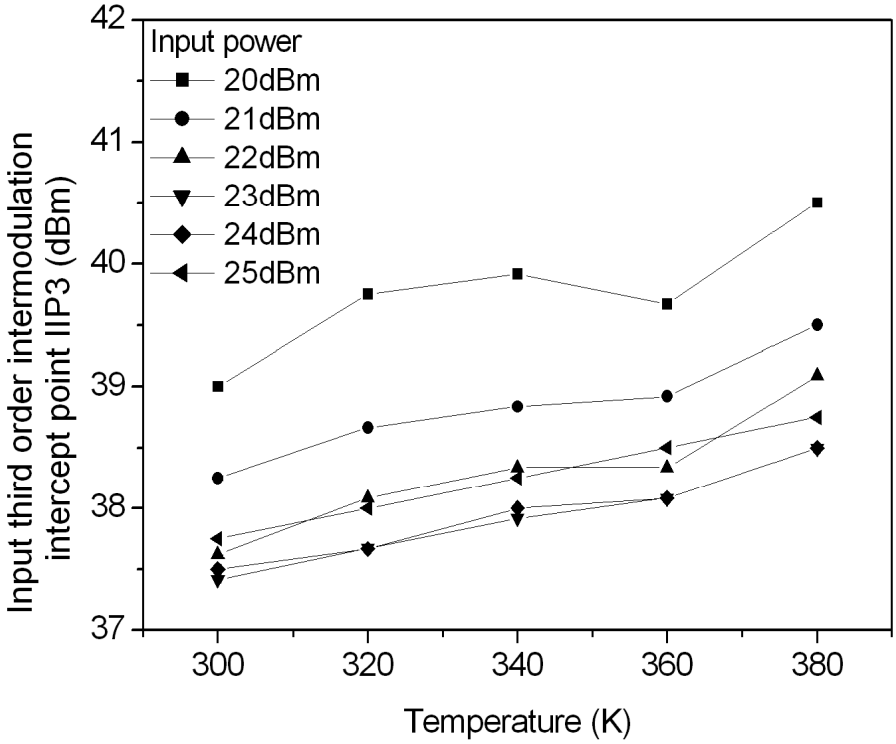


Figure 5.13 Input IIP3 as a function of temperature under different input power conditions at 2.5 GHz.

Chapter 6

An Al_2O_3 AlGaAs/InGaAs Metal-Oxide-Semiconductor PHEMT SPDT Switches with Low Control Currents for Wireless Communication Applications

6.1 Introduction

HEMT devices are widely used for RF switch applications. GaAs PHEMT based switches, which demonstrate low gate current, have an obvious advantage over Si PIN diode based switches due to lower DC power consumption [15]. Overall, GaAs switches have lower control voltage, higher power handling capability, and higher electron mobility compared to other solid-state switches, which makes them suitable for cellular handset, WLAN, and bluetooth applications. However, III-V HEMT using Schottky gate for current modulation usually results in higher gate leakage current as compared to MOSFET using high-κ dielectric for device modulation. The use of high-κ gate dielectric for III-V HEMT can significantly suppress direct-tunneling gate current and results in considerable reduction in power consumption.

In this study, ALD Al_2O_3 with a high dielectric constant (8.6-10) and a high breakdown field (5~10 MV/cm) was used as high-κ material for AlGaAs/InGaAs MOS-PHEMT switches [16]. The major requirements for good RF switch are low insertion loss, high isolation, high power handling capability and low control current [17]. To achieve low control current, the methods include reducing the gate current and the size of devices. The MOS-PHEMT switches with extra high resistance between control electrode and signal path provide good isolation and results in much lower control current as compared to conventional PHEMT switches.

6.2 Results and discussion

Fig. 6.1 shows the circuit schematic of the MOS-PHEMT SPDT T_x/R_x (transmitting/receiving) switch, and the R_g between the signal and control terminal has a value of 3 kΩ to provide extra isolation between the signal and control path. In the receiving, the V_{CTRL1} is biased at 3 V and the V_{CTRL2} at 0 V, and the RF signal is flowing from RF_{in} to RF_{out1}. In the transmitting, the RF signal path is from RF_{out2} to RF_{in} as V_{CTRL1} is biased at 0 V and V_{CTRL2} at 3 V.

Fig. 6.2 shows the DC characteristics of the MOS-PHEMT used in the switches. The electrical characteristics of the PHEMT with the same epi-structure but without top gate oxide are also shown in the same figure for comparison. The drain-to-source saturation current density (V_{DS} = 2 V, V_{GS} = 0 V) of 167 mA/mm, the on-state resistance (V_{DS} = 0.5 V, V_{GS} = 0 V) of 3.75 Ω · mm, the threshold voltage (V_{th}) of -0.98 V, and the peak extrinsic transconductance of 248 mS/mm (V_{DS} = 2 V) were achieved for MOS-PHEMT. As shown in Fig. 6.3, the MOS-PHEMT with the Al_2O_3 gate dielectrics demonstrated much lower gate current as compared to the conventional PHEMT [43, 44]. Therefore, it appears that the application of Al_2O_3 gate dielectric for MOS-PHEMT can obtain the comparable DC performance and effectively lower the gate leakage current for the switch application [44].

As exhibited in Fig. 6.4, the MOS-PHEMT switch has an insertion loss of 0.3 dB, an isolation of 33.4 dB, and a return loss of 18.5 dB (control voltage = +3/0 V, input power = 0 dBm) at 2.5 GHz. The RF characteristics of the MOS-PHEMT switches were comparable to those of the PHEMT switches. The small deviations of the RF results from these two switches were primarily due to the insertion of Al_2O_3 gate dielectric.

Fig. 6.5(a) shows the MOS-PHEMT switches had comparable input P_{1dB} of 31.4 dBm at 2.5 GHz as compared to PHEMT switches. Considering the switch power

limitation, the maximum input power is described as in Chapter 2:

$$P_{\max} = \frac{(V_c - V_{th})^2}{2Z_0} \tag{2.7}$$

where Z_0 is the line impedance, V_{th} the threshold voltage, and V_c the absolute control voltage [17, 37, 45, 46]. The input P_{1dB} for switches with and without Al_2O_3 were identical because the V_{th} shift was very small (V_{th}, MOS-PHEMT = -0.98 V, PHEMT = -1 V). Based on Eq. (2.7) above and the test results, it can be seen that the power handling capability was closely related to the threshold characteristics, and Al_2O_3 did not affect the power handling capability. Fig. 6.5(b) compares the control currents of MOS-PHEMT switches and PHEMT switches at different control voltage levels. For MOS-PHEMT switch, the control current remained steady around 10 μA due to the combination of the 3 kΩ gate resistor and Al_2O_3 gate dielectric between control electrode and signal path, while the control current of PHEMT switches only with the 3 kΩ gate resistor increased from 21 μA to 51 μA when the control voltage increased from 1.5 V to 5 V. The control current of the GaAs PHEMT switch is five times higher than that of the GaAs MOS-PHEMT switch. It implies that the MOS-PHEMT switches can improve the control current due to the insertion of Al_2O_3, and the switches have a significant advantage of very low DC power consumption for energy saving. It's demonstrated that the MOS-PHEMT switches with Al_2O_3 gate dielectric and with series/shunt layout have comparable RF performance with much lower DC power consumption compared to conventional PHEMT switches.

The MOS-PHEMT was annealed at 200 ℃ for 240 h for thermal stability test. After thermal annealing, the devices exhibited less than 3 % difference in saturation drain current, transconductance, and threshold voltage. The result demonstrates that ALD Al_2O_3 and the interface are thermally quite stable.

6.3 Conclusions

The AlGaAs/InGaAs MOS-PHEMT SPDT switch with ALD Al_2O_3 gate dielectric was fabricated for the first time. Gate current was improved as compared to the conventional PHEMT. The RF characteristics of the MOS-PHEMT switch exhibited an insertion loss of 0.3 dB, an isolation of 33.4 dB, a return loss of 18.5 dB, and a high input P_{1dB} of 31.4 dBm at 2.5 GHz. Much lower control current of less than 10 μA when biased from 1.5 V to 5 V was achieved. It's evident that MOS-PHEMT can be used for MMIC switch applications with excellent RF performance and low DC power consumption.

FIGURES

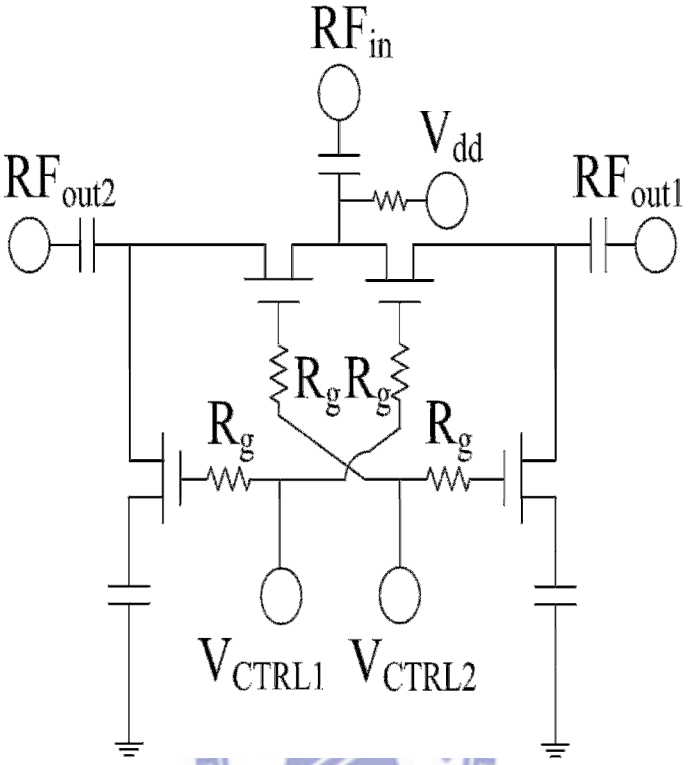
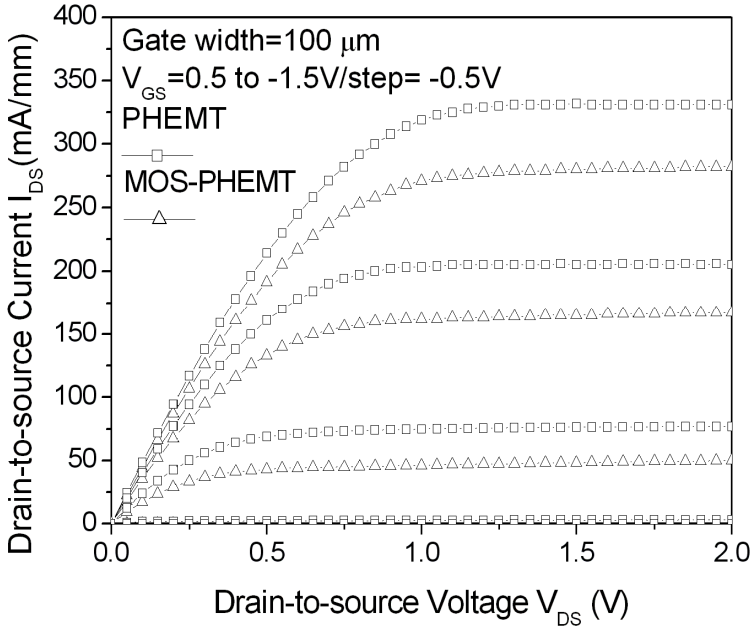
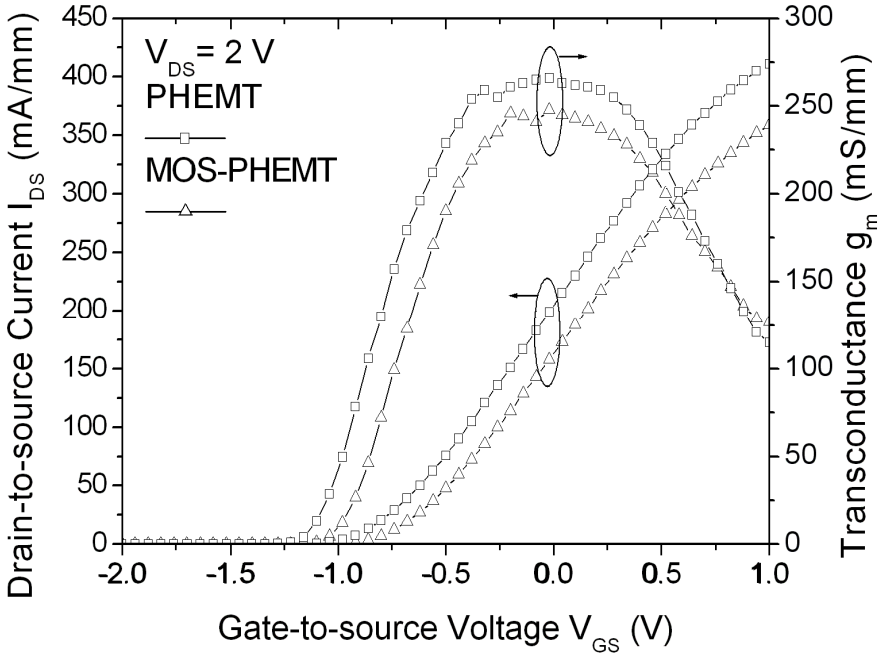


Figure 6.1 The circuit schematic of the series/shunt AlGaAs/InGaAs MOS-PHEMT SPDT switch.



(a)



(b)

Figure 6.2 (a) I-V characteristics of the 0.5 μm gate length MOS-PHEMT and PHEMT. (b) Transconductance and drain-to-source current vs V_{GS} characteristics of the 0.5 μm gate length MOS-PHEMT and PHEMT.

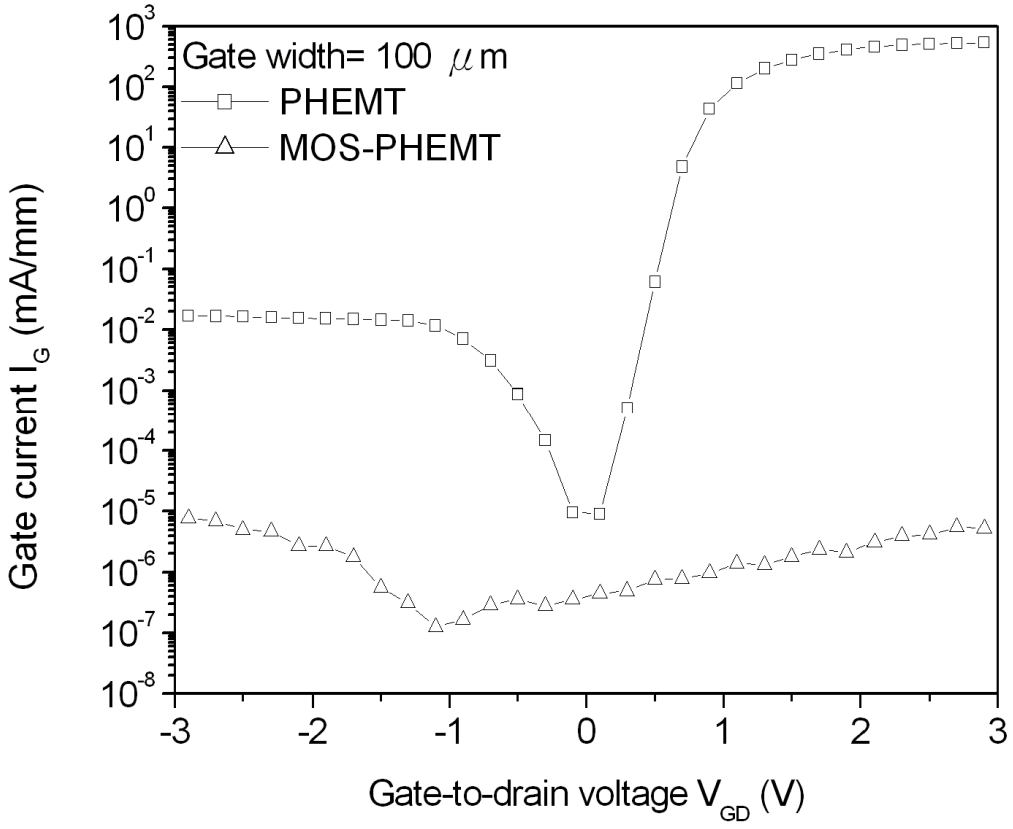
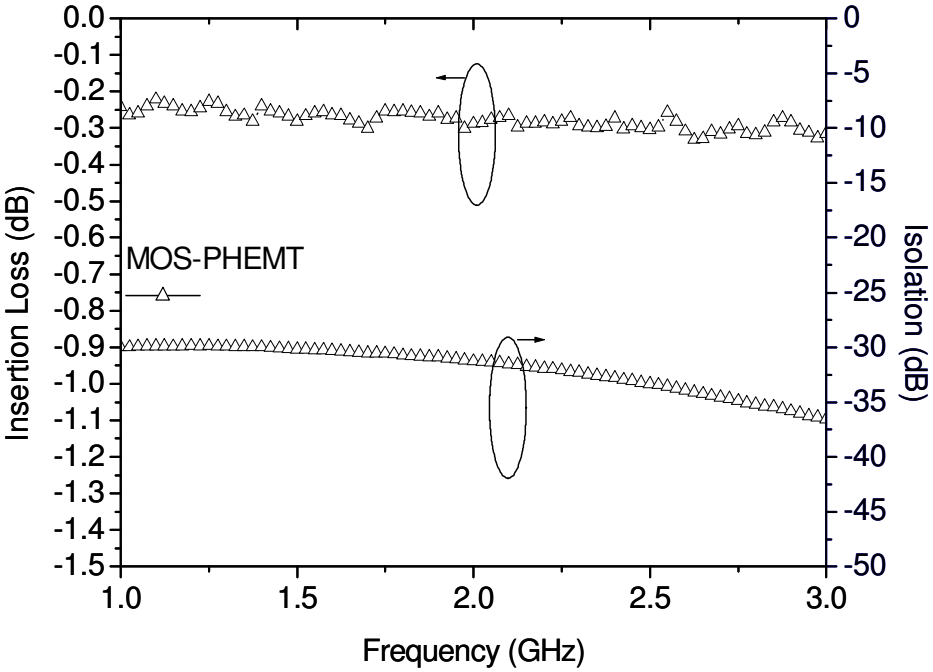
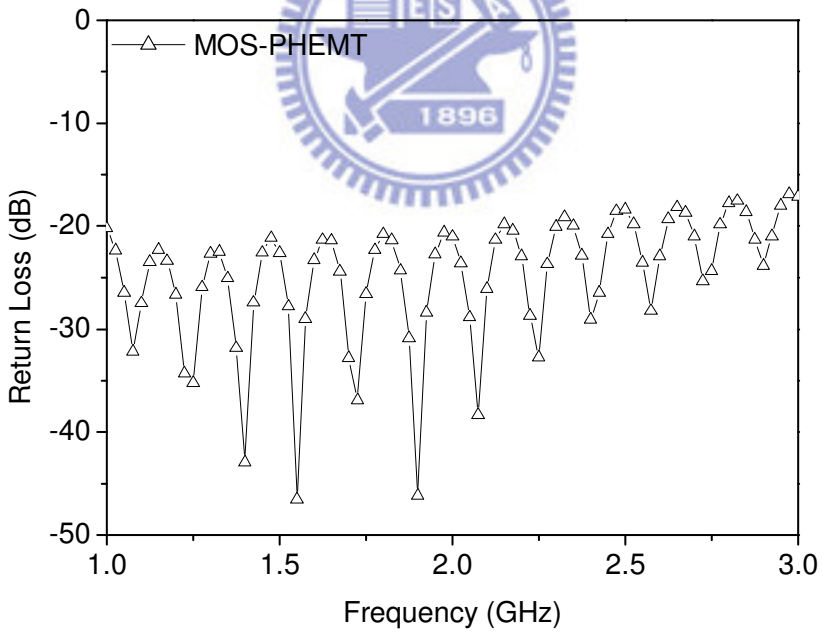


Figure 6.3 Gate leakage current (I_G) as a function of the gate-to-drain voltage (V_{GD}) for the MOS-PHEMT and the PHEMT.

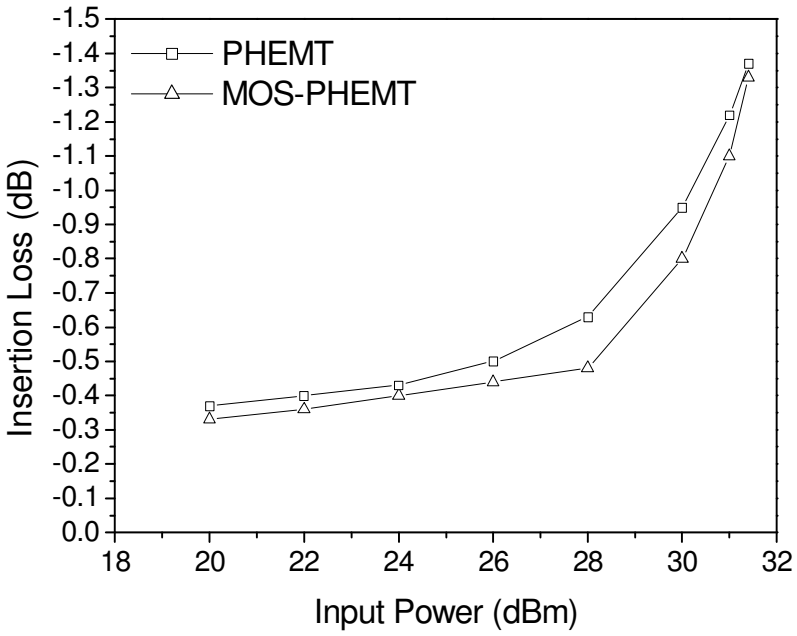


(a)

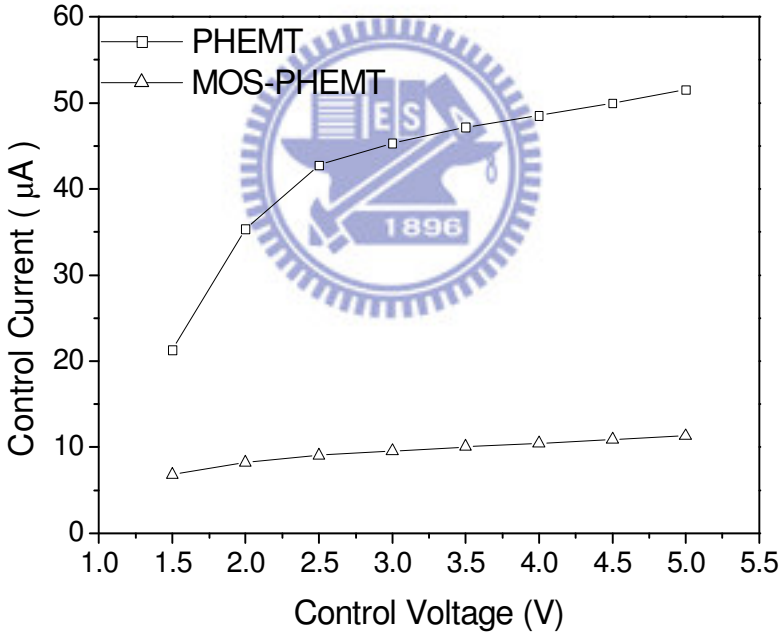


(b)

Figure 6.4 (a) Insertion loss, isolation, and (b) return loss of the MOS-PHEMT SPDT switch.



(a)



(b)

Figure 6.5 (a) Insertion loss of the MOS-PHEMT SPDT switch and the PHEMT SPDT switch with different input power levels at 2.5 GHz. (b) Control currents of the MOS-PHEMT SPDT switch and the PHEMT SPDT switch at different control voltage levels.

Chapter 7

Conclusions

In this dissertation, the electrical performances of the Cu-metallized AlGaAs/InGaAs PHEMT SPDT switches and the AlGaAs/InGaAs MOS-PHEMT SPDT switches with Al_2O_3 were evaluated.

It is reported for the first time the fabrication and electrical performances of the SPDT GaAs switch fabricated with Cu-metallized interconnects using Pt as the diffusion barrier. The RF characteristics of the Cu-metallized SPDT switch exhibited an insertion loss of 0.33 dB and an isolation of 36.7 dB at 2.5 GHz, the performance is comparable to the SPDT switches fabricated using conventional Au interconnects. High power handling capability was achieved with input P_{1dB} of 27 dBm and IIP3 of 50 dBm. Based on the high temperature reliability tests including thermal stress test (annealing at 250 ℃ for 20 h) and HTSL environment test, no significant changes in the DC and RF characteristics were observed for the SPDT switches after these tests. To test the operation reliability of the Cu-metallized switches, the Cu-metallized switches were subjected to an on/off stress test for 24 h at room temperature and showed very little change of the insertion loss and isolation. It is evident from these data that the Cu metallization process developed is very reliable and can be used for the GaAs MMICs fabrication.

In order to evaluate the temperature-dependent impact on DC and RF characteristics of the Cu-metallized switches for high-temperature applications, the evaluation of electrical characteristics of the Cu-metallized SPDT GaAs switches using Pt as the diffusion barrier at elevated temperatures has also been investigated. The Cu-metallized switches have been tested at different temperatures, and the device

exhibits low thermal threshold coefficients ($\delta V_{th}/\delta T$) of −0.25 mV/°K from 300 °K to 500 °K. Furthermore, the Cu-metallized SPDT switch exhibited an insertion loss of 0.33 dB, a return loss of 23.3 dB, and an isolation of 36.7 dB at 2.5 GHz; the performance is comparable with the performance of the traditional Au-metallized SPDT switches. The input P_{1dB} of 28.3 dBm at 2.5 GHz was obtained for these switches. Moreover, the temperature-dependent effects on the insertion loss, isolation, switching characteristics, and power handling capability of the Cu-metallized switches using Pt as the diffusion barrier have also been investigated. The RF characteristics of the Cu-metallized SPDT switch still remained quite stable and exhibited a low insertion loss of 0.46 dB, an excellent isolation of 42.79 dB, a high input P_{1dB} of 28.45 dBm, and a high IIP3 of 40.5 dBm at 2.5 GHz when tested at 380 °K. These results demonstrate that the Cu metallization process using Pt as the diffusion barrier is a very reliable process and can be applied to the GaAs MMIC switch fabrication.

In addition, the AlGaAs/InGaAs MOS-PHEMT SPDT switch with ALD Al_2O_3 gate dielectric was fabricated for the first time. Gate current was improved as compared to the conventional PHEMT. The RF characteristics of the MOS-PHEMT switch exhibited an insertion loss of 0.3 dB, an isolation of 33.4 dB, a return loss of 18.5 dB, and a high input P_{1dB} of 31.4 dBm at 2.5 GHz. Much lower control current of less than 10 μA when biased from 1.5 V to 5 V was achieved. It's evident that MOS-PHEMT can be used for MMIC switch applications with excellent RF performance and low DC power consumption.

Overall, in this study, the application of the novel semiconductor technologies of the Cu metallization and the high-κ dielectric deposition to the GaAs PHEMT switches have been demonstrated for low cost, low power consumption, and good high-frequency performances in the future.

REFERENCES

[1] K. Holloway and P. M. Fryer, "Tantalum as diffusion barrier between copper and silicon," *Appl. Phys. Lett.*, 57, 1736, 1990.

[2] K. Holloway, P. M. Fryer, C. Cabral, Jr., J. M. E. Harper, P. J. Bailey, and K. H. Kelleher, "Tantalum as a diffusion barrier between copper and silicon: Failure mechanism and effect of nitrogen additions," *J. Appl. Phys.*, 71, 5433, 1992.

[3] D. S. Yoon, H. K. Baik, and S. M. Lee, "Effect on thermal stability of a Cu/Ta/Si heterostructure of the incorporation of cerium oxide into the Ta barrier," *J. Appl. Phys.*, 83, 8074, 1998.

[4] E. R. Weber, "Transition metals in silicon," *Appl. Phys. A, Solids Surf.* 1, 1, 1983.

[5] A. Cros, M. O. Aboelfofotoh, and K. N. Tu, "Formation, oxidation, electronic, and electrical properties of copper silicides," *J. Appl. Phys.* 67, 3328, 1990.

[6] C. A. Chang, "Formation of copper silicides from Cu(100)/Si(100) and Cu(111)/Si(111) structures," *J. Appl. Phys.* 67, 556 , 1990.

[7] P. H. Wohlbier, *Diffusion and Defect Data*. Zürich, Switzerland: Trans Tech 10, 89, 1975.

[8] S. W. Chang, The Study of Copper-Metallized GaAs and InP Heterojunction Bipolar Transistors. 2005.

[9] C. Y. Chen, E. Y. Chang, L. Chang, and S. H. Chen, "Backside copper metallization of GaAs MESFETs using TaN as the diffusion barrier," *IEEE Trans. Electron Devices*, 48, 1033, 2001.

[10] C. Y. Chen, E. Y. Chang, L. Chang, and S. H. Chen, "Backside copper metallisation of GaAs MESFETs," *Electron. Lett.*, 36, 1317, 2000.

[11] H. C. Chang, E. Y. Chang, Y. C. Lien, L. H. Chu, S. W. Chang, R. C. Huang, and H. M. Lee, "Use of WN_x as diffusion barrier for copper airbridged low noise

GaAs PHEMT," *Electron. Lett.*, 39, 1763, 2003.

[12] S. W. Chang, E. Y. Chang, D. Biswas, C. S. Lee, K. S. Chen, C. W. Tseng, T. L. Hsieh, and W. C. Wu, "Gold-free fully Cu-metallized InGaP/GaAs heterojunction bipolar transistor," *Jpn. J. Appl. Phys.*, 44, 8, 2005.

[13] Y. C. Wu, E. Y. Chang, Y. C. Lin, H. T. Hsu, S. H. Chen, W. C. Wu, L. H. Chu, and C. Y. Chang, "SPDT GaAs switches with copper metallized interconnects," *IEEE Microw. Wireless Compon. Lett.*, 17, 133, 2007.

[14] S. W. Chang, E. Y. Chang, C. S. Lee, K. S. Chen, C. W. Tseng, Y. Y. Tu, and C. T. Lee, "A gold-free fully copper-metallized InP heterojunction bipolar transistor using non-alloyed ohmic contact and platinum diffusion barrier," *Jpn. J. Appl. Phys.*, 44, 899, 2005.

[15] L. Devlin, "The design of integrated switches and phase shifters". Essex: Plextek communications technology consultants.

[16] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H.J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. K. Ng, and J. Bude, "GaAs MOSFET with oxide gate dielectric grown by atomic layer deposition," *IEEE Electron Device Lett.*, 24, 209, 2003.

[17] S. Makioka, Y. Anda, K. Miyatsuji, and D. Ueda, "Super self-aligned GaAs RF switch IC with 0.25 dB extremely low insertion loss for mobile communication systems," *IEEE Trans. Electron Devices*, 48, 1510, 2001.

[18] F. Gao, "Reliability evaluation on dual-etch-stop InGaAs PHEMTs," *JEDEC*, 95, 2002.

[19] H. Ishida, Y. Hirose, T. Murata, Y. Ikeda, T. Matsuno, K. Inoue, Y. Uemoto, T. Tanaka, T. Egawa, and D. Ueda, "A high-power RF switch IC using AlGaN/GaN HFETs with single-stage configuration," *IEEE Trans. Electron Devices*, 52, 1893, 2005.

[20] K. H. Lee, Z. Jin, and K. H. Koo, "High linearity SPDT switch for dual band wireless LAN applications," in *Proc. IEEE APMC'05 Conf.*, 2005, [CD ROM].

[21] F. Ellinger, *Radio Frequency Integrated Circuits and Technologies*. New Jersey: Springer, 651, 2008.

[22] I. D. Robertson, *MMIC design*. United Kingdom: The institution of electrical engineers, 305, 1995.

[23] I. Bahl and P. Bhartia, *Microwave solid state circuit design*. New Jersey: Wiley, 631, 2003.

[24] M. Golio, *The RF and microwave handbook*. New York: CRC Press, 5, 2001.

[25] M. M. Radmanesh, *Radio Frequency and Microwave Electronics Illustrated*. New Jersey: Prentice Hall PTR, 2001.

[26] K. Miyatsuji and D. Ueda, "A GaAs high power RF single pole dual throw switch IC for digital mobile communication system," *IEEE J. Solid-State Circuits*, 30, 979, 1995.

[27] Y. C. Lin, Linearity Improvement of Low Noise HEMT for Wireless Communication Applications. 2006.

[28] R. Williams, *Modern GaAs processing methods*. Boston • London: Artech House, 199, 1990.

[29] G. A. Nagu, Amarnath, and T. K. G. Namboodhiri, "Effect of heat treatments on the hydrogen embrittlement susceptibility of API X-65 grade line-pipe steel," *Bull. Mater. Sci.*, 26, 435, 2003.

[30] D. Kwon, H. Park, S. Ghosh, C. Lee, H. T. Jeon, and J. G. Lee, "Recrystallization of the copper films deposited by pulsed electroplating on ECR plasma-cleaned copper seed layers," *J. Korean Phys. Soc.*, 44, 1108, 2004.

[31] P. Singer, "Copper CMP: A question of tradeoffs," *Semiconductor International*, 73, 2000.

[32] C. K. Lin, W. K. Wang, Y. J. Chan, and H. K. Chiou, "BCB bridged distributed wideband SPST switch using 0.25-μm $In_{0.5}Al_{0.5}As$-$In_{0.5}Ga_{0.5}As$ metamorphic HEMTs," *IEEE Trans. Electron Devices*, 52, 1, 2005.

[33] Y. Xuan, H. C. Lin, and P. D. Ye, "Simplified surface preparation for GaAs passivation using atomic layer-deposited high-κ dielectrics," *IEEE Trans. Electron Devices*, 54, 1811, 2007.

[34] H. Sik, Y. Feurprier, C. Cardinaud, G. Turban, and A. Scavennec, "Reduction of recombination velocity on GaAs surface by Ga-S and As-S bond-related surface states from $(NH_4)_2S_x$ treatment," *J. Electrochem. Soc.*, 144, 2106, 1997.

[35] C. S. Lee, Y. J. Chen, W. C. Hsu, K. H. Su, J. C. Huang, D. H. Huang, and C. L. Wu, "High-temperature threshold characteristics of a symmetrically graded InAlAs/$In_xGa_{1-x}As$/GaAs metamorphic high electron mobility transistor," *Appl. Phys. Lett.*, 88, 223506, 2006.

[36] W. C. Liu, K. H. Yu, K. W. Lin, J. H. Tsai, C. Z. Wu, K. P. Lin, and C. H. Yen, "On the InGaP/GaAs/InGaAs camel-like FET for high breakdown, low-leakage, and high-temperature operations," *IEEE Trans. Electron Devices*, 48, 1522, 2001.

[37] J. H. Jang, S. Kim, and I. Adesida, "Enhancement-mode high electron mobility transistors lattice-matched to InP substrates utilizing Ti/Pt/Au metallization," *Jpn. J. Appl. Phys.*, 45, 3349, 2006.

[38] C. D. Wilson, A. G. O'Neill, S. M. Baier, and J. C. Nohava, "High temperature performance and operation of HFETs," *IEEE Trans. Electron Devices*, 43, 201, 1996.

[39] F. S. Shoucair and P. K. Ojala, "High-temperature electrical characteristics of GaAs MESFETs (25–400 ℃)," *IEEE Trans. Electron Devices*, 39, 1551, 1992.

[40] M. Dammann, A. Leuther, R. Quay, M. Meng, H. Konstanzer, W. Jantz, and M.

Mikulla, “Reliability of 70 nm metamorphic HEMTs,” *Microelectron. Reliab.*, 44, 939, 2004.

[41] T. Ytterdal, B. J. Moon, T. A. Fjeldly, and M. S. Shur, “Enhanced GaAs MESFET CAD model for a wide range of temperatures,” *IEEE Trans. Electron Devices*, 42, 1724, 1995.

[42] S. A. Hanka, C. H. Chen, P. Vold, and T. Akinwande, “GaAs MODFET transconductance stability,” *IEEE Trans. Rel.*, 39, 571, 1990.

[43] R. J. W. Hill, D. A. J. Moran, X. Li, H. Zhou, D. Macintyre, S. Thoms, A. Asenov, P. Zurcher, K. Rajagopalan, J. Abrokwah, R. Droopad, M. Passlack, and I. G. Thayne, “Enhancement-mode GaAs MOSFETs with an $In_{0.3}Ga_{0.7}As$ channel, a mobility of over 5000 $cm^2/V•s$, and transconductance of over 475 μS/μm,” *IEEE Electron Device Lett.*, 28, 1080, 2007.

[44] H. C. Lin, T. Yang, H. Sharifi, S. K. Kim, Y. Xuan, T. Shen, S. Mohammadi, and P. D. Ye, “Enhancement-mode GaAs metal-oxide-semiconductor high-electron-mobility transistors with atomic layer deposited Al_2O_3 as gate dielectric,” *Appl. Phys. Lett.*, 91, 212101, 2007.

[45] H. Tosaka, T. Fujii, K. Miyakoshi, K. Ikenaka and M. Takahashi, “An antenna switch MMIC using E/D mode p-HEMT for GSM/DCS/PCS/WCDMA bands application,” *IEEE Radio Frequency Integrated Circuits Symposium*, 519, 2003.

[46] H. C. Chiu, T. J. Yeh, Y. Y. Hsieh, T. Hwang, P. Yeh, and C. S. Wu, “Low insertion loss switch technology using 6-inch InGaP/AlGaAs/InGaAs pHEMT production process,” *IEEE CSIC Digest*, 119, 2004.

簡歷

姓名：吳雲驥

性別：男

生日：民國 67 年 09 月 02 日

籍貫：嘉義市

學歷：

私立大同大學材料工程學系學士

（民國 85 年 9 月－民國 89 年 6 月）

國立交通大學材料科學與工程研究所碩士

（民國 89 年 9 月－民國 91 年 6 月）

國立交通大學材料科學與工程研究所博士

（民國 93 年 9 月－民國 98 年 12 月）

博士論文題目：

銅金屬化製程及閘極介電層於低成本、低功率損耗 AlGaAs/InGaAs 假晶高電子遷移率電晶體單刀雙擲開關之應用

Low Cost, Low Power Consumption SPDT GaAs Switches with Copper Metallization and Gate Dielectric

Publication List

Journal Papers

1. **Y. C. Wu**, E. Y. Chang, Y. C. Lin, H. T. Hsu, S. H. Chen, W. C. Wu, L. H. Chu, and C. Y. Chang, "SPDT GaAs switches with copper metallized interconnects," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 2, pp. 133–135, Feb. 2007.
2. **Yun-Chi Wu**, Edward Yi Chang, Yueh-Chin Lin, and Li-Han Hsu, "Evaluation of Electrical Characteristics of the Copper-Metallized SPDT GaAs Switches at Elevated Temperatures", *IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY*, VOL. 8, NO. 3, SEPTEMBER 2008.
3. **Yun-Chi Wu**, Edward Yi Chang, Yueh-Chin Lin, Chi-Chung Kei, Mantu. K. Hudait, Marko. Radosavljevic, Yuen-Yee Wong, Chia-Ta Chang, Jui-Chien Huang and Shih-Hsuan Tang, "Study of the Inversion Behaviors of $Al_2O_3/In_xGa_{1-x}As$ Metal-Oxide-Semiconductor Capacitors with Different In Contents", *Solid-State Electronics* 54 (2010) 37–41.
4. Wei-Cheng Wu, Li-Han Hsu, Edward Yi Chang, Camilla Kärnfelt, Herbert Zirath, J. Piotr Starski, and **Yun-Chi Wu**, "60 GHz Broadband MS-to-CPW Hot-Via Flip Chip Interconnects", *IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS*, VOL. 17, NO. 11, NOVEMBER 2007.
5. Li-Han Hsu, Wei-Cheng Wu, Jian Zhang, Edward Yi Chang, Herbert Zirath, Chen-Hua Huang, Yin-Chu Hu, Chin-Te Wang, Szu-Ping Tsai, Wee-Chin Lim and **Yun-Chi Wu**, "60 GHz Flip-Chip Packaged SPDT MMIC Switch with Suppression of Performance Deviation", *IEEE Transactions on Advanced Packaging*, Accepted 2009.

Conference Papers

1. **Y. C. Wu**, E. Y. Chang, Y. C. Lin and W. C. Wu, "High-Temperature Electrical Characteristics of SPDT GaAs Switches with Copper Metallized Interconnects", *CS MANTECH Conference*, May 14-17, 2007, Austin, Texas, USA.
2. Li-Han Hsu, Wei-Cheng Wu, Edward Yi Chang, Herbert Zirath, **Yun-Chi Wu**, and Chin-Te Wang, "Fabrication Process of MS-to-CPW RF-Via Transition for RF-MEMS Devices Packaging Applications", *CS MANTECH Conference*, 2009.
3. Edward Yi Chang, **Yun-Chi Wu**, Yueh-Chin Lin, Yuen-Yee Wong, Chia-Ta Chang, and Jui-Chien Huang**,** and Chi-Chung Kei, "Study of the Inversion Behaviors of Al_2O_3/n-$In_{0.7}Ga_{0.3}As$ Metal-Oxide-Semiconductor Capacitors", *IUMRS-ICA*, 2008.
4. Wei-Cheng Wu, Li-Han Hsu, Edward Yi Chang, Yin-Chu Hu, **Yun-Chi Wu**, and Yu-Min Teng, "DC and RF Characterizations of Flip-Chip Packaged Low-Noise GaAs PHEMT towards Multi-chip Modules (MCMs) for Microwave Applications", *MMS 2007 Mediterranean Microwave Symposium*.