

國立交通大學
光電工程研究所
碩士學位論文

矽基板上矽奈米柱的形成與特性分析

Characteristics of Si nanopillars
Formatted on Si Substrate



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摘要

論文名稱：矽基板上矽奈米針的形成與特性分析

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關鍵詞：矽、奈米針、自我凝聚、鎳、活化性離子蝕刻、光激發、奈米、光性、反射率、量子侷限

在本論文中，我們成功地利用二氧化矽薄膜當緩衝層，使得鎳的奈米顆粒成功地快速凝聚在矽的基板上。因為矽的高熱導 148 W/m-K 造成熱快速散逸，所以奈米鎳顆粒很難直接地聚集在矽的基板上。藉由厚度 200 \AA 且熱導只有 1.35 W/m-K 的二氧化矽當緩衝層，阻止了 NiSi_2 化合物的產生，和讓奈米鎳顆粒因為在鎳和矽界面之間吸附力減小與熱的累積，更容易形成自我凝聚。因此，奈米鎳顆粒可以加速形成，退火時間大大縮短到 22 秒。奈米顆粒的大小和密度平均是 30 奈米和 $7 \times 10^{10} \text{ cm}^{-2}$ 。利用鎳在二氧化矽層上自我凝聚成的奈米粒當奈米遮罩，經過活化離子式蝕刻後，可以在矽的基板上製造出大面積的矽奈米針陣列，而針的大小可以被控制到小於 50 奈米。在我們的實驗中，矽奈米針的最理想高寬比是 8。此時，針的平均大小和高度分別是 40 奈米和 400 奈米。去除掉在矽的基板上的奈米粒和二氧化矽後，從矽奈米柱發出的光激發可以發現到 400 到 600 奈米的可見波段和 750 奈米的近遠紅外波段。400 奈米到 600 奈米的可見波段主要源自於氧的弱鍵結 (WOB)、中性的氧化缺陷 (NOV) 與 E' 缺陷。更進一步地，因為矽奈米針持續氧化產生在光激發譜上的藍位移現象和產生在變功率光激發譜上的強度飽和現象，所以成功地證實 750 奈米波段是量子侷限效

應。其他在電性上，相較於矽的靶材，矽奈米針擁有較快的充放電速度、較低的電阻和超低漏電流，而在光性，則明顯有較低的反射率。



ABSTRACT

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In this essay, rapid self-aggregation of Ni nanodots on Si substrate covered with a thin SiO₂ buffered layer is investigated. Ni nanodots are hard to self-aggregate on highly heat dissipated Si substrate with a thermal conductivity of 148 W/m-K. Adding 200Å-thick SiO₂ buffer with an ultralow thermal conductivity of 1.35 W/m-K prevents the formation of NiSi₂ compounds, facilitates the self-assembly of Ni nanodots from enhanced heat accumulation and released Ni adhesion with Si. Formation of Ni nanodots can therefore be accelerated with size and density of 30 nm and $7 \times 10^{10} \text{ cm}^{-2}$, respectively, under an annealing time greatly shortened to 22 sec. With the advantage of the self-assemble Ni/SiO₂ nano-dots based nano-mask, a large-area Si nano-pillar array with rod size of <50 nm can be formatted on Si substrate through the induced coupled plasma reactive ion etching (ICP-RIE) procedure. In our experiment, the optimum aspect ratio of the Si nanopillars is 8 with the average diameter of 40 nm and the average height of 400 nm. After removing Ni dots and the SiO₂ film on the Si substrate, both the visible 400 nm-600 nm and near infrared 750nm photoluminescence from the Si nano-pillar sample were observed and analyzed. The visible emission 400 nm to 600 nm mainly originated from the weak oxygen bond

(WOB) the neutral oxygen vacancy (NOV) defects, and the E' defects. Moreover, the peak wavelength of 750 nm is emitted from the quantum confining centers proven by the blue shift of the oxidizing Si nanopillars in the μ PL and the saturating peak intensity in the power dependent μ PL. Comparing to the bulk structure, the Si nanopillars owned the high charging and discharging speed 、 low resisters and no leakage current in electrics and the low reflectance in optics.



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CHAPTER 1

Introduction

1.1 Review of Metallic Mask

In order to produce Si nanopillar array, the E-beam lithography was the most common way to fabricate the nano mask. However, the process of the E-beam lithography is high cost and low efficiency. Nowadays, the metallic nanodot arrays such as Au, Al, Ni or Ag [1.1-1.4] have been extensively used as nanoscale masks to fabricate quantum confined Si nanodots, or been employed in resonant surface-plasma-wave based bio-photonic sensing applications. In particular, the self-assembly of Ni nanodots has also caused researching interests due to its potential applications in field-emission and bio-magnetic sensing. Previously, Lee et al. [1.2] employed the Ni nanodot mask with diameter and density of about 41 nm and $5.3 \times 10^9 \text{ cm}^{-2}$ to form Si nanorods. However, the disadvantage is that the self-aggregation of the Ni nanodots from Ni film coated on Si substrate usually takes up to 10 min even by rapid thermal annealing (RTA) process at 700°C in N₂ ambient. It was mentioned in previous experiment that the self-aggregation of evaporated Ni film on pure Si wafer is hard to initiate without long-term annealing process, and the density of the formatted Ni nanodots is too sparse for applications. Such a long-term annealing inevitably leads to an unintentional doping or diffusion of the coated Ni into Si substrate during self-assembly procedure. On account of the larger thermal conductivity, the Si substrate that reduces the heat accumulating on the interface of Ni and Si, and the self-aggregating speed is slowed down due to the relatively good adhesion between the Ni and Si interface. It is noticed that the thin nitride layer such as Si₃N₄ [1.3] or TiN [1.5-1.6] layers could prevent the formation of NiSi₂ compounds [1.7] and retain the thermal power on the Si surface. In this essay, we propose for the first time the quick

formation of Ni nanodots on Si substrate covered with a thin buffered SiO₂ layer because the insufficient heat accumulation and strong adhesive problems happened at the Ni/Si interface can be solved by depositing a thin layer of SiO₂ on Si substrate prior to the Ni evaporation and RTA processes.

1.2 Formation of Si nanopillars

The Si nano-pillar array has been shown to have the potential for many applications such as being photonic crystals [1.8], data storage [1.9], field electron emitter [1.10], nanoscale transistors [1.11-1.12] and light emitting devices [1.13]. The reactive ion etching [1.14] and thermal growth with the catalyst [1.15] were employed as two major procedures to obtain Si nano-pillar array with the aid of self-assembled metal nano-dot mask patterns such as Au, Ag or Ni. However, the diameter and the growing direction of Si nanowires are hard under the control. The etching procedure is the only choice to form not only straight but also thin Si one dimension structures. With the novel approach, the formation of the Si nanopillar array can be mostly realized by the induced coupling plasma reactive ion etching (ICP-RIE) of oxide-covered Si substrate capped with the mask of self-assembled Ni nanodots. Yoo *et al.* have made use of Ni nano-dot mask to form Si nano-pillars with diameter and height of about 41nm and 472nm, respectively. Nevertheless, the disadvantage of their results is that the density is too sparse to enhance the luminescence, and the self-aggregation of the Ni nano-dot from a Ni film coated on a Si substrate usually takes up to 10 min even by a rapid thermal annealing (RTA) process at 700°C in the N₂ ambient [1.2]. The

1.3 Photoluminescence of Si Nanopillars

The possible applications in optoelectronics of the low dimensional structures

have extended by the construction of one-dimension silicon structures. [1.16-1.20] Theoretical studies of realized Si quantum wires confirm that there is a transition from the indirect to a direct gap material in Si, induced by electron confinement in nanostructures. [1.21-1.23] The theoretical result may be tested by the fabrication of well controlled and ordered nanostructures which are expected to give luminescence too, if the theoretical results are valid. The fabrication of this type of nanostructure presents the additional interest that they are produced by technology, so an additional step is made towards Si based optoelectronic devices, integrated on the same substructure with the microelectronic circuit. Early in 1996, Nassiopoulou *et al.* has been invented the electroluminescent device based on Si nanopillars. [1.24] The Light emission in the visible range was observed in forward bias when the voltage exceeded 12–14 V. The characteristics of this EL signal were similar to the PL signal observed from the same sample. A mechanism of EL emission related to high electric field electronic transport through the wires is suggested. In 1998, Papadimitriou *et al.* also fabricated highly anisotropic Si nanopillar array with the aspect ratio 25:1 and the diameters <100 nm by lithography and etching and also by several cycles of thermal oxidation and oxide removal by HF dip.[1.25] The anisotropic Si nanopillar array emitted photoluminescence in the range of 500-600nm. Moreover, the photoluminescence efficiency and energy position depended on the wavelength and the polarization state of the initial laser beam. This dependence was explained as originating from quantum confinement effects. In 2004, Yanagiya *et al.* tried to grow Si nanowires on sapphire with the width 50nm and the height 1nm by using disilane (Si_2H_6) gas-source molecular beam epitaxy (MBE). [1.26] The visible photoluminescence from the Si quantum wires was observed at the peak wavelength 750nm at 9 and 300 K. However, the PL intensity at 9 K is over 20 times larger than that of 300 K and the PL emission peak barely shifts between 9 and 300 K.

1.4 Motivation

The main motivation in our experiment is to form dense Si nanopillars with high aspect ratio on Si substrate and to research the most appealing topic----the Si emission. Instead of the e-beam or lithographic techniques, the sample and cheap way was realized by using the self-assembled metal dots. From section 1.1, it was obvious that many metals can conglomerate to dot form after annealing such as Au 、Al 、Ag 、Ni and so on. We took advantage of Ni dots as our mask for its hardness and low cost comparing to Au 、Ag and Al during the etching process. In 2005, proposed by Lee et al. [1.2], Ni nanodot array was utilized as a mask and the Si nanopillar array was manufactured successfully. However, the process of Ni dot formation took 10 min that was a long period and the density of the Ni dots wasn't dense enough. Since the diameter and density of Si nanopillars are both controlled by ones of the Ni nanodots, we investigated a special way to fabricate the dense and small Ni nanodots without taking long period. By consulting the method in ref. 1.4, we inserted the buffer layer of SiO₂ between the Ni film and Si substrate.

1.5 Structures of this essay

The main topics of this essay are the formation of the Ni nanodots 、the process of the Si nanopillar array 、the optics and electrics of the Si nanopillars that separately are discussed in chapter2 、chapter3 and chapter4. In chapter2, we will study how to achieve the dense and small-sized Ni dots aggregated on Si substrate inclusive the impacts of annealing temperature 、annealing time 、Ni thickness and the most weighty buffer layer----SiO₂. In chapter3, we will debate the conditions for getting Si nanopillars with the high aspect ratio including the discussion of the etchant gas flowing 、pressure 、

power and time. After the manufacture of the Si nanopillars, the following mission is to make a understanding of it in the optical and electrical aspects that is arranged in chapter4. Depending on these special characteristics of Si nanopillars, we must be able to improve the medical or communicating technologies such as bio-sensors 、emitters or memory and then rich our life.

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CHAPTER 2

Study of Ni Self-assembly

2.1 Introduction

The key issue about the formation of Si nanopillar array is how to fabricate the nanomask. Many kinds of fabrication processes have been proposed particularly using electron beam (e-beam) lithography [2.1-2.3]. However, e-beam lithography is a time-consuming, complicating and expansive process. Recently, the Al, Au or Ag based metallic nanodot arrays [2.4-2.7] have been extensively used as nanoscale masks to replace the e-beam lithography for fabricating quantum confined Si nanowires, or been employed in resonant surface-plasma-wave based bio-photonic sensing applications [2.8]. In particular, the self-assembly of Ni nanodots has also caused researching interests due to its potential applications in field-emission, nanomagnetic materials and bio-magnetic sensing. Previously, Lee et al. [2.5] employed the Ni nanodot mask with diameter and density of about 41 nm and $5.3 \times 10^9 \text{ cm}^{-2}$, respectively, to form Si nanorods. Nevertheless, the disadvantage is that the self-aggregation of the Ni nanodots from Ni film coated on Si substrate usually takes up to 10 min even by rapid thermal annealing (RTA) process at 700°C in N₂ ambient [2.6]. It was mentioned in previous experiment that the self-aggregation of evaporated Ni film on pure Si wafer is hard to initiate without long-term annealing process. Besides, the density of the formatted Ni nanodots is too sparse for applications. This is mainly due to the larger thermal conductivity of the Si substrate that reduces the heat accumulating on the interface of Ni and Si, and due to the relatively good adhesion between the Ni and Si interface that slows down the self-aggregating speed. Besides, such a long-term annealing inevitably leads to an unintentional doping or diffusion of the coated Ni into Si substrate during self-assembly procedure. It is noticed that the thin nitride layer

such as Si_3N_4 [2.7] or TiN [2.9, 2.10] layers could prevent the formation of NiSi_2 compounds [2.11] and retain the thermal power on the Si surface. Huang et al. proposed that the Ni cluster became smaller and denser at the same annealing condition as the Ni initial thickness decreases and that the dimension of the GaN nanorods would be smaller with the aid of the Si_3N_4 layer than the one without the Si_3N_4 layer [2.7]. D. Aurongzeb et al. declared that the presence of the native oxide plays a key role in Ni dot formation and that the activation energies of 0.09 ± 0.02 and $0.31\pm0.05\text{eV}$ are observed to form Ni cluster [2.11]. In this experiment, we propose for the first time the quick formation of Ni self-assembly on Si substrate covered with a thin buffered SiO_2 layer. The insufficient heat accumulation and strong adhesive problems happened at the Ni/Si interface can be solved by depositing a thin layer of SiO_2 on Si substrate prior to the Ni evaporation and RTA processes.

In experiment, the RCA cleaning process is employed to completely remove the dusty particles and native oxide from the p-type [100] Si wafer. Subsequently, a buffered SiO_2 layer with thickness of 200 \AA is deposited by plasma enhanced chemical vapor deposition (PECVD) under standard recipe. A 50 \AA -thick Ni film is thermally evaporated on the SiO_2 covered Si substrate using an E-beam evaporating system with Ni deposition rate of 0.1 \AA/s at an applied current of 70 mA . Afterwards, the rapid thermal annealing (RTA) process is performed at 850°C under flowing N_2 ambient with a fluence of 5 sccm to form randomized Ni nanodot pattern on the SiO_2 covered Si substrate. The morphology of Ni nanodot array is analyzed using scanning electron microscope (SEM, Hitachi FE-SEM S-5000).

In this chapter, besides the thickness of SiO_2 , there are other parameters that control the distribution of Ni dots -- the thickness of Ni layer 、 annealing holding temperature and annealing holding period. Especially, the thickness of Ni layer affects the size distribution of Ni dots the most.

2.2 SiO₂ Thickness

From the introduction, we know Lee et al. [2.6] have employed the Ni nanodot mask with diameter and density of about 41 nm and $5.3 \times 10^9 \text{ cm}^{-2}$, to form Si nanorods, but the disadvantage was that the self-aggregation of the Ni nanodots from Ni film coated on Si substrate usually takes up to 10 min even by rapid thermal annealing (RTA) process at 700°C in N₂ ambient [2.6]. In order to improve the self-assembling process, we propose the quick formation of Ni nanodots on Si substrate covered with a thin buffered SiO₂ layer. Figure 2.1 is the SEM image of the Ni nanodots self-aggregated on the SiO₂ covered Si substrate with different SiO₂ layer thickness under RTA at 850°C for 120 sec. As expected, Fig. 2.1(a) confirms that the Ni nanodots are unable to self-aggregate on pure Si wafer during such a short-term RTA process. On the contrary, we observe the apparent self-assembly of Ni nanodots on all of the SiO₂ covered Si substrates. With a SiO₂ thickness of 100 Å, the Ni layer initiates its self-aggregation to form a long strip, as shown in Fig. 2.1(b). However, the heat accumulation on such a thin SiO₂ layer during RTA is still insufficient to complete the reshaping of Ni nanodots. By increasing the thickness of SiO₂ layer from 100 Å to 200 Å, a coherent aggregation of Ni nanodots with almost half-sphere morphology can be seen in Fig. 2.1(c). Besides, the average diameter and the density of the Ni nanodots are around 30 nm and 10^{11} cm^{-2} with the 200 Å SiO₂ under the Ni layer. If the thickness of the SiO₂ layer enlarges to 1000 Å in Fig. 2.1(d), the size of Ni nanodots becomes larger about 40 nm than those obtained on thinner SiO₂ film covered Si substrate in Fig. 2.1(c), whereas the Ni nanodot density greatly reduces to 10^{10} cm^{-2} . It is thus concluded from the aforementioned results that the self-aggregation of Ni nanodots can be completed as the thickness of SiO₂ increases to >200 Å, which is mainly attributed to the enhanced

heat accumulation effect happened in the thicker SiO_2 layer during RTA. Apparently, the self-aggregation of Ni on SiO_2 covered Si substrate is better than that on pure Si substrate due to their distinguishable difference in thermal conductivity (Si of 148 W/m-K and SiO_2 of 1.35 W/m-K) [2.13]. Therefore, the SiO_2 buffered layer can efficiently terminate the thermal dissipating from Ni layer to Si substrate such that the self-assembly of Ni nanodots can finished at a shorter annealing period. Therefore, the insufficient heat accumulation and strong adhesive problems happened at the Ni/Si interface can be solved by depositing a thin layer of SiO_2 on Si substrate prior to the Ni evaporation and RTA processes. Comparing to the precious Korean results [2.6], we successfully increased the Ni dot density and shorten the annealing time.

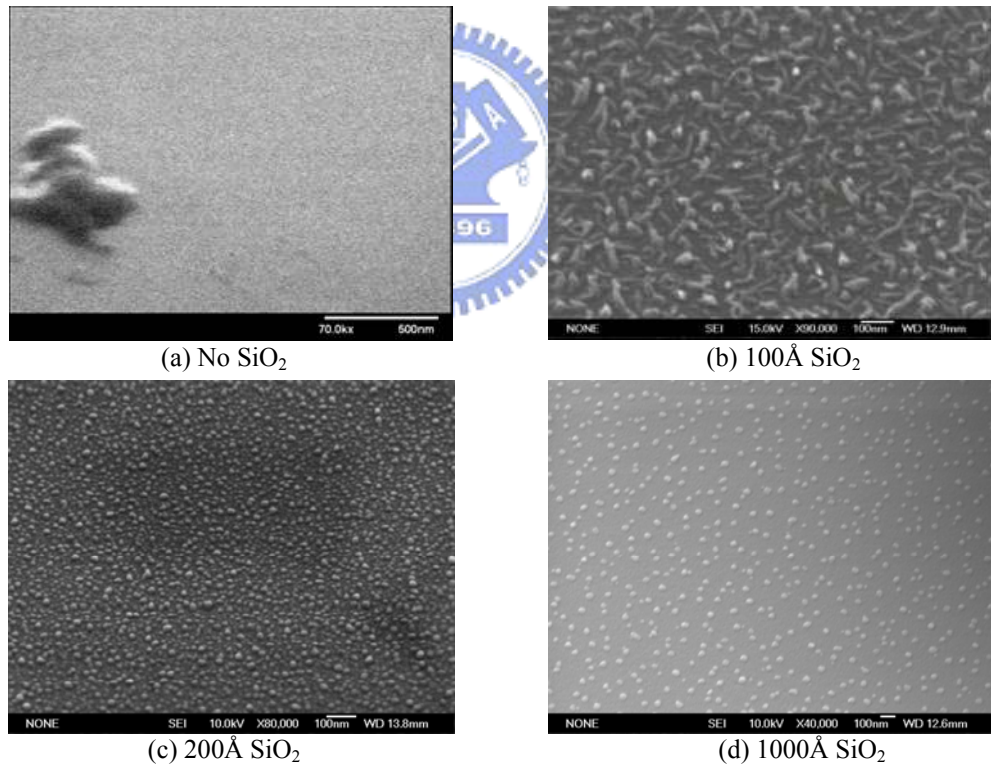


Fig. 2.1 Self-aggregation of Ni nanodots on Si substrates without or with SiO_2 buffered layer of different thickness.

2.3 RTA Temperature and time (Rapid Thermal Annealing)

The thin Ni film evaporated on the SiO₂ film can easily to be conglomerated, resulting in the formation of Ni nanodot array on SiO₂ substrate. Whether we change the annealing temperature or annealing time, both the thermal energy of annealing can be adjusted. From our experimental results, 850°C is the proper temperature for RTA annealing. As if the annealing temperature is too high, the Ni and Si atoms could obtain sufficient power to compose the SiNi₂ compounds [2.12]. However, if the annealing temperature is too low, it spends more annealing time to congregate Ni film into randomized two-dimensional nanodot array. In the following experiments, we choose to fix the annealing temperature and vary the annealing time during RTA process.

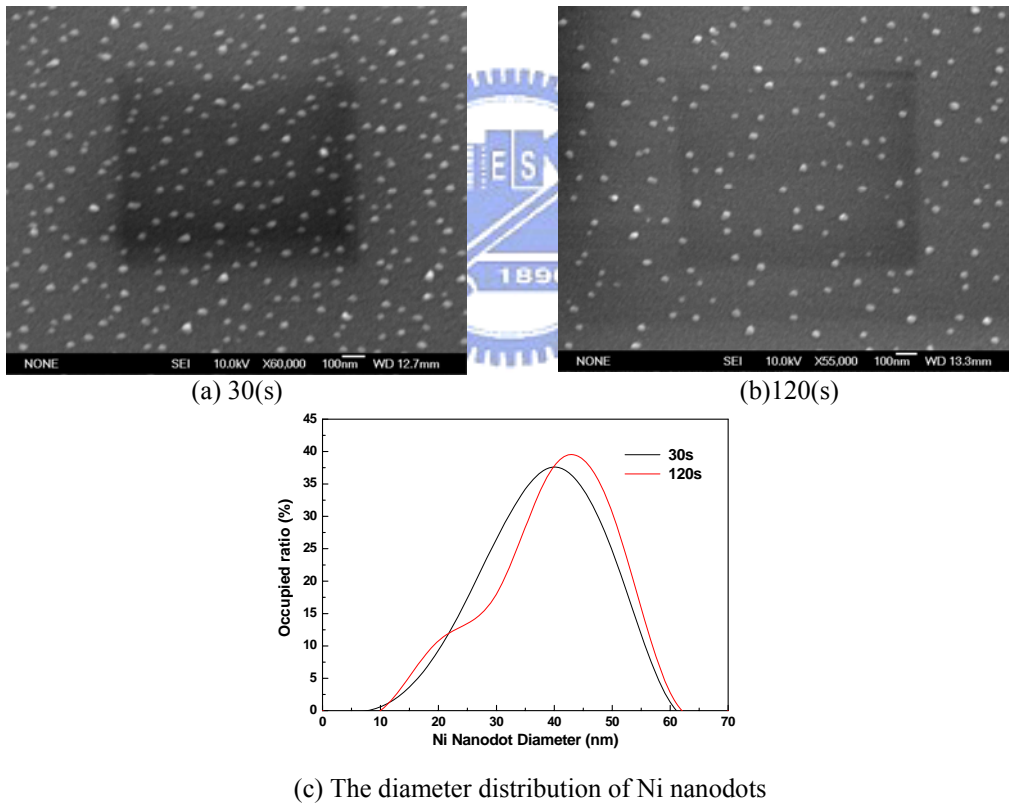


Fig. 2.2 SEM images of Ni nanodots after annealing for 30s and 120s at 850°C shown in 2.2(a) and 2.2(b). Apparently the density of dots for shorter annealing time is denser by comparing the plots in 2.2(c).

As shown in Fig. 2.2, we compare the variation in size and density of Ni dots assembling on 1000Å SiO₂ layer under two different annealing periods. The average

size and density of Ni nanodots annealing at 850°C for 30 sec are 37 nm and $1 \times 10^{10} \text{ cm}^{-2}$, respectively. Nonetheless, the average size and density of Ni nanodots annealing at 120 sec significantly increase to 40 nm and $7 \times 10^9 \text{ cm}^{-2}$. Fig.2.2(c) showed the peak Ni nanodots diameter shifted from 40 nm to 45 nm when the annealing time increased from 30 sec to 120 sec. This again confirms the trend of enlarging size and decreasing density under long annealing time. The Ni atoms can get more thermal energy to complete their precipitation process under longer annealing time. However, after rapid thermal annealing at 850°C between 20 and 26 sec, the Ni dots were formed on the 200Å SiO₂ film shown in Fig.2.3.

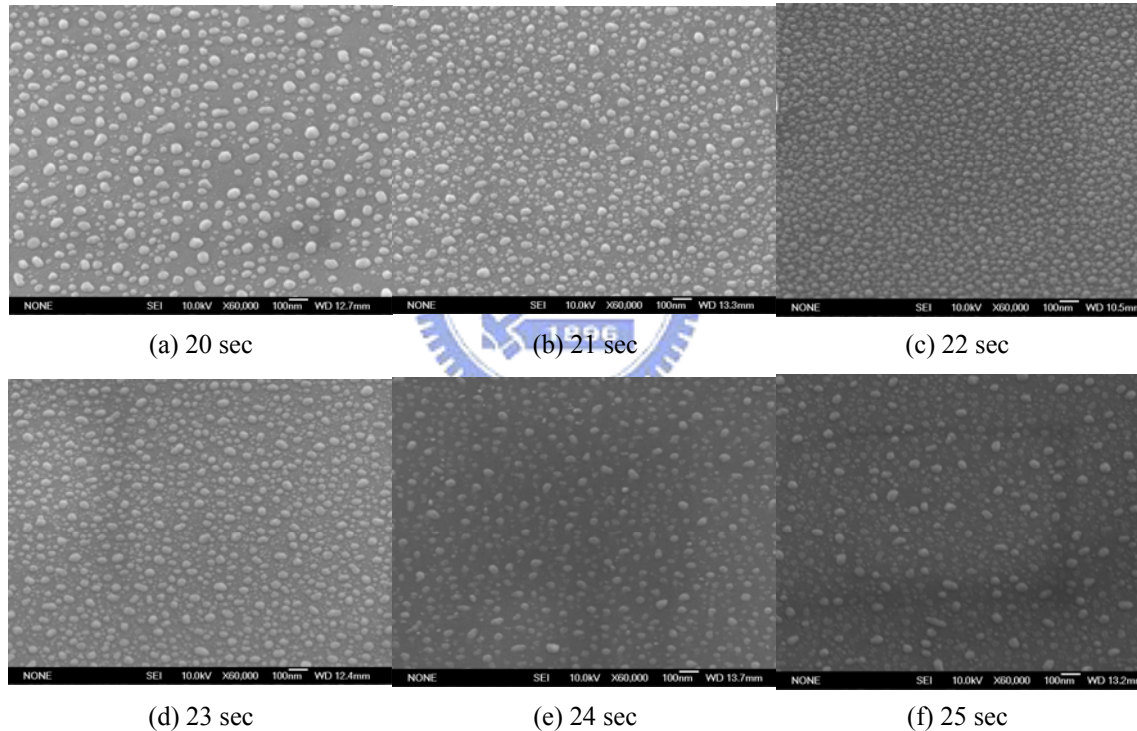


Fig. 2.3 The size and density of Ni dots as a function of the annealing time when the thickness of SiO₂ is 200Å. The 22 sec annealing time at 850°C is the optimum item for the densest density and the smallest diameter.

The shape of Ni nanodots becomes hemisphere-like with an average diameter varying from 33 nm to 75 nm, respectively. A largest density of $7.2 \times 10^{10} \text{ cm}^{-2}$ for the Ni nanodot with smallest size of 33 nm can be obtained after annealing at 850°C for 22 sec. Figure 4 interprets the variation SEM image of Ni nanodot self-assembled at gradually lengthened annealing durations. The Ni film initially breaks into large strips

and slowly approaches a hemispheric shape with increasing RTA time, eventually these small Ni nanodots would conglomerate to larger nanodots if the annealing time prolongs to >30 sec. At annealing time between 22 and 26 sec, there is also a similar tendency on the size and density of Ni nanodots as compared to those shown in Fig. 2.3.

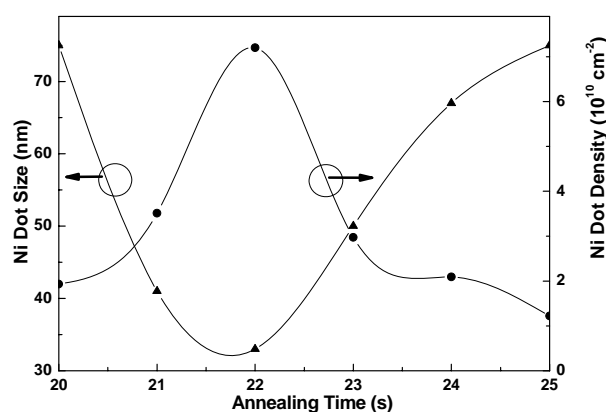


Fig. 2.4 The size and density of self-aggregated Ni nanodot as a function of RTA annealing time.

In more detail, the size and distribution of the Ni nano-dots on the SiO_2 film are mainly determined by thin oxide film thickness, RTA temperature, RTA time and Ni thickness. From the diagram of curves of Fig. 2.4, the optimum time is 22 seconds. The optimum annealing condition for Ni nanodot formation with highest density and smallest size are therefore set as 850°C for 22 seconds in our RTA annealing process. Such a sample has also been chosen as the Ni nano-mask for etching Si-nano-pillars. In addition, we also observe that the diameter of Ni nanodots becomes smaller with a decrease in the thickness of the deposited Ni layer [2.14].

Following the annealing time, the annealing temperature is also a key point to aggregate Ni dots. A suitable annealing temperature can save annealing time and make the self-assembled Ni nanodots small and dense enough at the same time. In order to prove our intuition, we fixed the annealing time at 120 seconds, the thickness of Ni layer at 50\AA , the thickness of SiO_2 at 200\AA and studied the effect of annealing temperature for Ni self-assembling. Then, the SEM images in Fig. 2.5 show the result that the Ni would gather to larger dots after the higher temperature annealing. However,

the density of Ni dots would decrease with the higher annealing temperature. So, too high annealing temperature such as 950°C would be hard to control the dense and small Ni dots. On the contrary, the small-sized and dense Ni dots could be obtained after the lower temperature annealing but the annealing time needs to increase for completing the Ni self-assembling. As known from our experiment, it would take 100 seconds、60 seconds and 20 seconds at least to self-assemble Ni separately at the annealing temperature 650°C、750°C and 850°C. The most appropriate annealing temperature is 850°C because Ni can self-assemble into the small size and high density the most quickly.

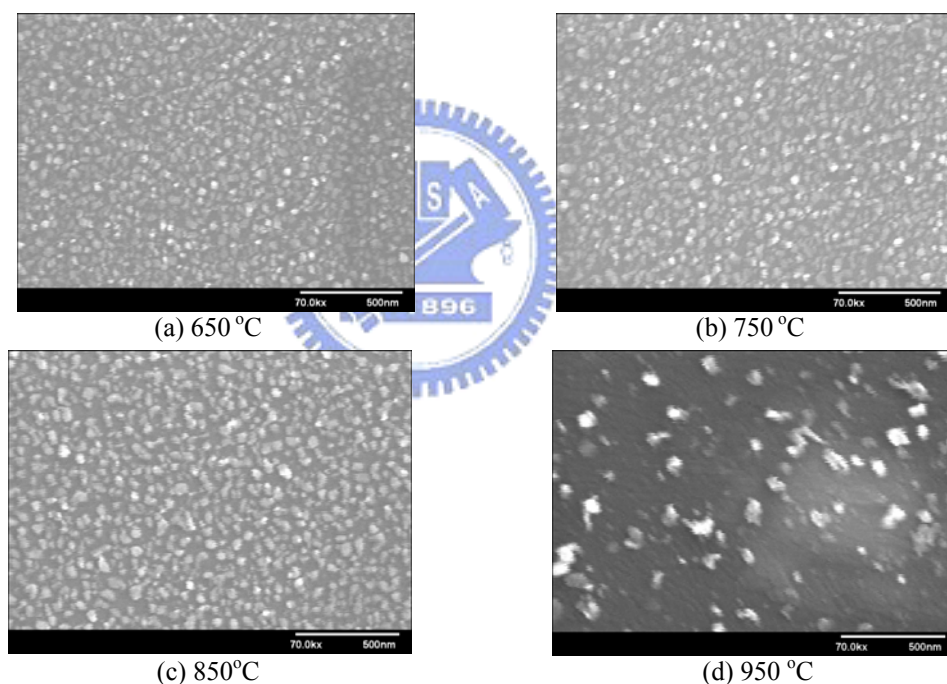


Fig. 2.5 SEM images of Ni dots after different annealing temperature for 120 s. Apparently the density of dots at lower annealing temperature is denser.

In more detail, the size and distribution of the Ni nano-dots on the SiO₂ film are mainly determined by thin oxide film thickness, RTA temperature, RTA time and Ni thickness. From the diagram of curves of Fig. 2.4, the optimum time is 22 seconds. The optimum annealing condition for Ni nanodot formation with highest density and smallest size are therefore set as 850°C for 22 sec in our RTA annealing process.

Such a sample has also been chosen as the Ni nano-mask for etching Si-nano-pillars. In addition, we also observe that the diameter of Ni nanodots becomes smaller with a decrease in the thickness of the deposited Ni layer [2.14].

2.4 Ni thickness

Besides the factors of the SiO₂ thickness 、annealing time and annealing temperature, we also observed that the diameter of Ni nanodots varied in the different thickness of the deposited Ni layer [2.7]. After analyzing the SEM images in Fig. 2.6, there is an apparent trend about the size and the density of Ni dots. When the Ni deposition is thicker under the same annealing conditions, the Ni would aggregate into larger dots and the dot number would decrease. Otherwise, the diameter of Ni dots exist a slight linear relation with the deposited Ni thickness. The approximately average diameters of Ni dots in Fig. 2.6(a) 、 (b) 、 (c) 、 (d) separately are 60nm 、 50nm 、 100nm and 200nm. Between the Fig 2.6(a) and Fig 2.6(b), the average diameters of Ni dots are nearly the same but the Ni dot number in Fig 2.6(a) is enormously smaller than in Fig 2.6 (b). This phenomenon is possibly caused by the uniformity of Ni deposition by e-beam evaporation. The depositing uniformity will be hard to control if the thickness of the deposited layer is small and close to the deposition rate. In addition, the information given by the SEM image in Fig 2.6 is that the shape of Ni dots will approach to circle if the thickness of Ni deposition is thinner. This is because the Ni self-assembling is more complete. The thicker the Ni deposition, the more time it will take to finish the Ni self-assembling. Eventually, the conclusion is that the optimum Ni thickness is 50Å to form the densest and smallest Ni nanodots as the etching mask.

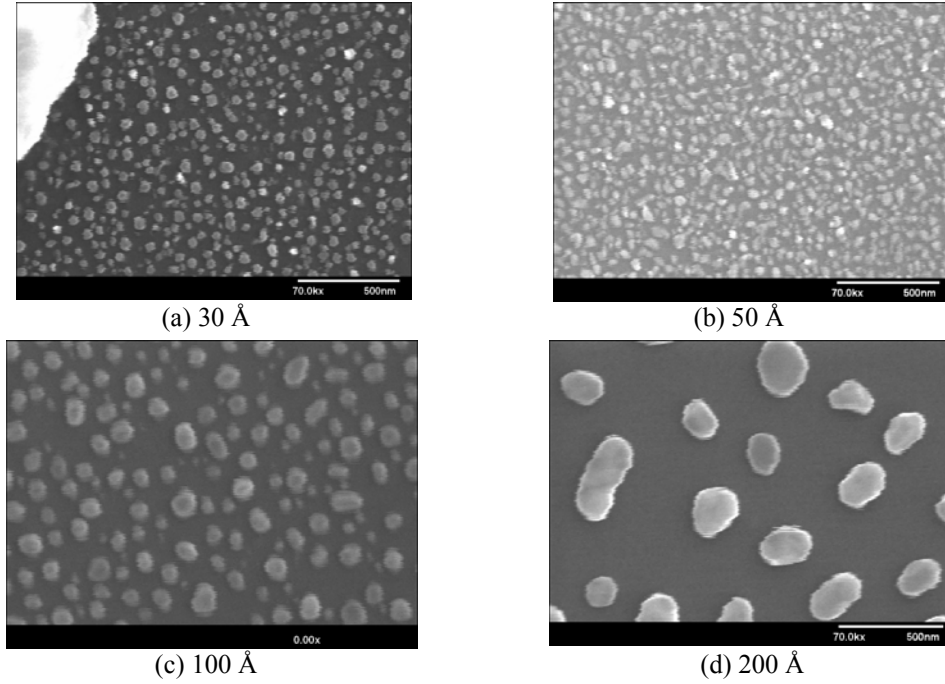


Fig. 2.6 SEM images of Ni dots formed from different thick Ni layer at 850 °C for 120 s. Apparently the density of dots with the thinner deposition of Ni layer is denser.

2.5 Conclusion

In conclusion, we successfully demonstrate a rapid self-assembly method for aggregating Ni nanodots on Si substrate by using a highly heat-accumulated and less-adhesive SiO₂ buffered layer. The Ni nanodot is relatively difficult to be self-aggregated on the Si substrate without SiO₂ buffered layer due to the highly heat dissipated feature of Si substrate with a thermal conductivity of 148 W/m-K. The 200Å thin SiO₂ layer prevents the formation of NiSi₂ compounds and facilitates the self-assembly of Ni nanodots from retaining the thermal power on the SiO₂ layer due to its ultralow thermal conductivity of only 1.35 W/m-K. The required annealing time for synthesizing the Ni nanodots with comparable density and size is greatly shortened to <30 seconds. The self-aggregated Ni nanodots with highest density and smallest size of $7.2 \times 10^{10} \text{ cm}^{-2}$ and 33 nm, respectively, are obtained at the optimized RTA condition at 850°C for 22 sec. The larger size and smaller density of Ni nanodots will be obtained after RTA if the SiO₂ film or the Ni layer becomes thicker. Raising the RTA

temperature, lengthening the RTA time and depositing thick SiO₂ film or Ni layer will concurrently cause the effects of size enlargement and density dilution.

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CHAPTER 3

Formation of Si Nanopillars

3.1 Introduction

Because of the using variety, Si one dimensional structures were extensively researched in the fabrication and analysis.[3.1-3.3] There are two major ways to form the Si one dimensional structure which are the thermal growth with the catalysis Au or Fe [3.4-3.5] and the dry etching by reactive ion etching [3.6-3.8]. The disadvantages of the thermal growth are the unable control for the diameter and the growing direction comparing to the dry etching. The reactive ion etching and electrochemical etching were employed as two etching procedures to obtain Si nano-pillar array. Traditional approaches for fabricating sub-micron or nano- Si structures, such as the Si nano-pillars, mainly rely on the electron-beam (E-beam) lithography [3.9], which provides accurate size and shape control. The production of <10-nm nano-pillar array under the assistance of E-beam lithography has been reported by Toshihiko and Papadimitriou. However, it is impractical to employ the E-beam lithography for large-scale fabrication due to its high cost and low writing speed. Nowadays, noble metal (Au or Ag) based nano-dot arrays have been extensively used as nano-masks to replace the E-beam lithography. Recently, Ni has been considered as an alternative to the noble metals. The Ni nano-dot mask is not only easy to control its size but also cheap in its formation process as compared to that of the e-beam lithography. In ref. 3.3, using the Ni nanodots as an etching mask, the Si nanopillars were performed by ICP-RIE with the etching gases carbon tetrafluoride (CF_4) and sulfur hexafluoride (SF_6). The diameter and height of the formed Si nanopillars are about 41 nm and 472 nm with the aspect ratio higher than 10. Nevertheless, their results can be improved that the density is too sparse to enhance the luminescence, and the self-aggregation of the Ni nano-dot from a

Ni film coated on a Si substrate usually takes up to 10 min even by a rapid thermal annealing (RTA) process at 700°C in the N₂ ambient. With the novel approach, the formation of the Si nano-pillar array can be mostly realized by the reactive ion etching of oxide-covered Si substrate capped with the mask of self-assembled Ni nanodots. A Si nano-pillar array has been shown to have the potential for many applications such as being photonic crystals [3.10], data storage [3.11], field electron emitter [3.12], nanoscale transistors [3.13-3.14] and light emitting devices [3.15]. Otherwise, the light emitting efficiency could also be enhanced with the aid of the quantum confined Si nano-pillars.

3.2 Experimental Process

In previous experiment, it is hard to achieve the aggregation of evaporated Ni film on pure Si wafer. This is because the adhesion between Ni and Si is too good to be make Ni self-assembled. Such a problem can be solved by depositing a thin layer of SiO₂ between Ni and Si. In our case, a buffered layer of 200Å-thick SiO₂ is deposited by plasma enhanced chemical vapor deposition (PECVD) under standard recipe. Afterwards, a 50nm-thick Ni film is evaporated on the SiO₂/Si substrate using an E-beam evaporating system with Ni deposition rate of 0.1 Å/s at an applied current of 70 mA. Subsequently, the rapid thermal annealing (RTA) process at 850°C for 22 seconds under the N₂ flowing gas of 5 sccm is performed to format randomized Ni nanodot pattern on SiO₂/Si substrate. The average diameter and density of Ni nanodots are 33nm and $7.2 \times 10^{12} \text{ cm}^{-2}$. By using the Ni nano-dot pattern as an etching mask, the Si substrate is dry-etched in a planar type ICP-RIE system (SAMCO ICP-RIE 101iPH) at RF frequency of 13.56 MHz. The ICP has a reactive chamber connected to a load-lock chamber, wherein the etching gas mixture of CF₄ and Ar gases were introduced into the reactive chamber through individual electronic mass flow

controllers (MFCs). The flowing rate of each gas is adjusted within an accuracy of about a standard cubic centimeter min (sccm). An automatic pressure controller is placed near the exhaust end of the chamber to control the chamber pressure. The gas mixture condition of $\text{CF}_4/\text{Ar} = 40/40$ sccm with the ICP/Bias powers set at 100W/50W and chamber pressure of 0.66 Pa during an etching duration of 5~7 minutes. If the etching parameters such as source power, bias power, and pressure and gas composition are investigated and optimized, Si nano-pillar arrays with tunable diameters of smaller than 100 nm can be formed. The fabricating process is shown in Fig. 3.1. After etching by ICP-RIE, the SiO_2 and Ni on the Si nanopillars would be removed by dipping in the HF solution and HNO_3 solution. Then, the pure Si nanopillar sample must be stored in the methyl alcohol to avoid the oxidation day by day. For analyzing the morphology of Ni nano-dot, the dimension and density of the Si nano-pillar array were estimated by the scanning electron microscope (SEM, Hitachi FE-SEM S-5000) and the standard atomic force microscopy (AFM).

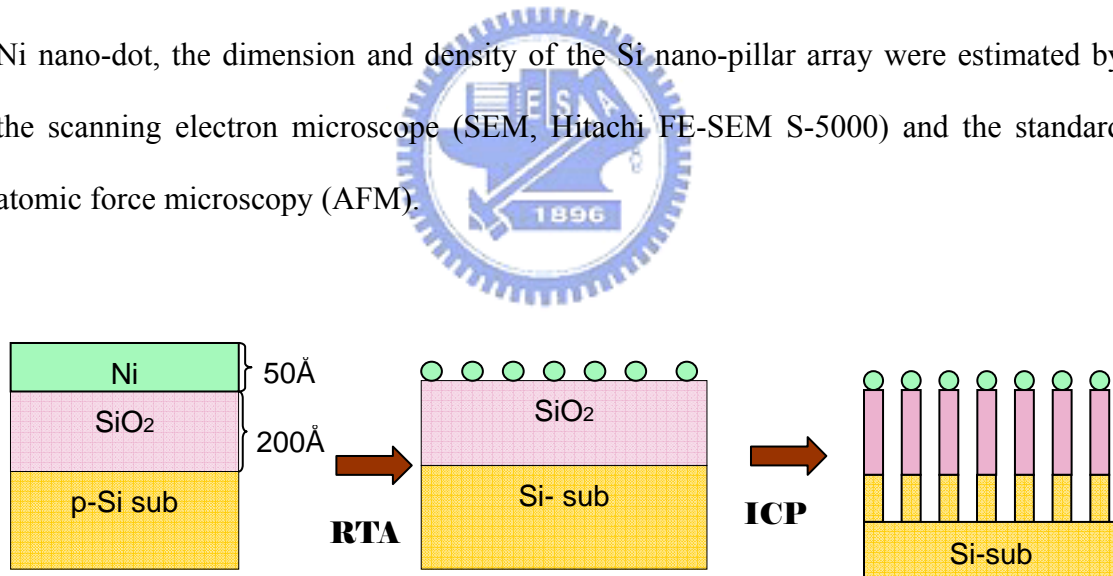


Fig. 3.1 Schematic illustration of Si nano-pillar arrays using Ni/SiO₂ as nano-masks formation. The reaction products after RTA and ICP-RIE etching, leading to the formation of Si nano-pillar arrays.

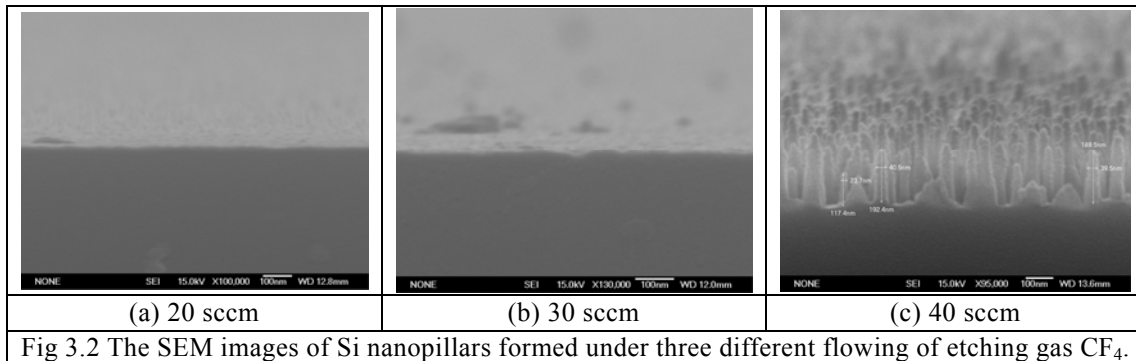
3.3 Results & Discussions

3.3-1 Gas flowing

The choices of gases for etching are very weighty because the etching rate and selectivity are extremely distinct by using the different etching gases. [3.15] In the

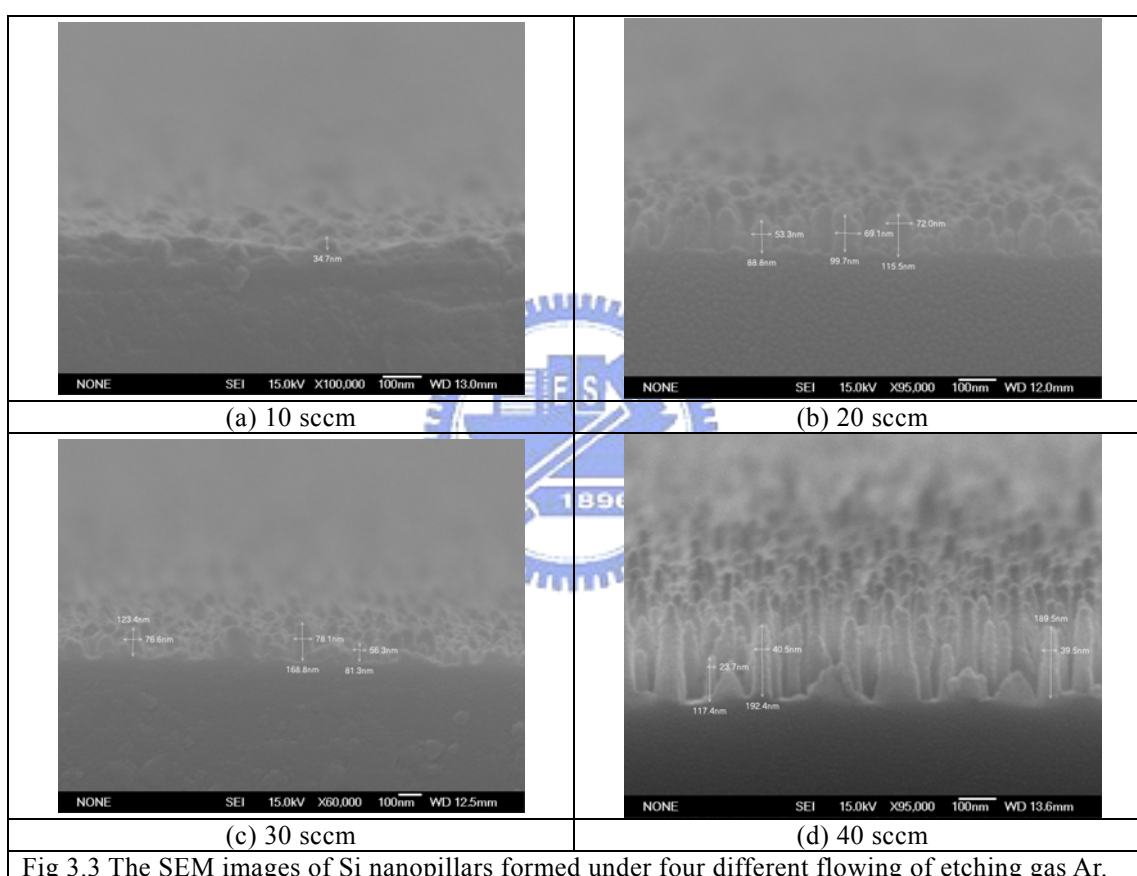
magnitude and ratio of the mixing gases are also the key point to get high etching rate and selectivity. SF_6 、 CF_4 、 CHF_3 、Ar、 O_2 and N_2 are the gases mainly to etch Si and SiO_2 . [3.6-3.8] SF_6 、 CF_4 and CHF_3 are the major etching sources and the etching rate can be enhanced by addition of Ar、 O_2 and N_2 . As for etchant gas, we chose the O_2 , CF_4 and Ar at the beginning of experiment. CF_4 is the main gas for etching SiO_2 and Si. Ar is also main gas able to increase the vertical-etching potential. In our opinion, O_2 is the mirror gas which should speed up the etching rate. Nevertheless, the aid of O_2 isn't apparent and the oxygen plasma causes a lot of defects such weak oxygen bond and the neutral oxygen vacancy in the Si nano-pillars analyzed from the photoluminescence. On account of the above reason, we have not used O_2 as etchant gas.

In our all etching process, the gaseous mixture of CF_4 and Ar were adopted. If the etching pressure、rf power、bias power、etching time and Ar flowing are fixed at 0.66 pa、100 W、50 W、7 minutes and 40 sccm (standard cubic centimeter), we can clearly observe that the optimum etching depth of Si nanopillars occurred at the CF_4 flowing 40sccm from Fig. 3.2. The average diameter and length of the Si nanopillars are 35 nm and 170nm and the aspect ratio is nearly 5.



Besides varying the CF_4 flowing, we also tried to study the etching results with the

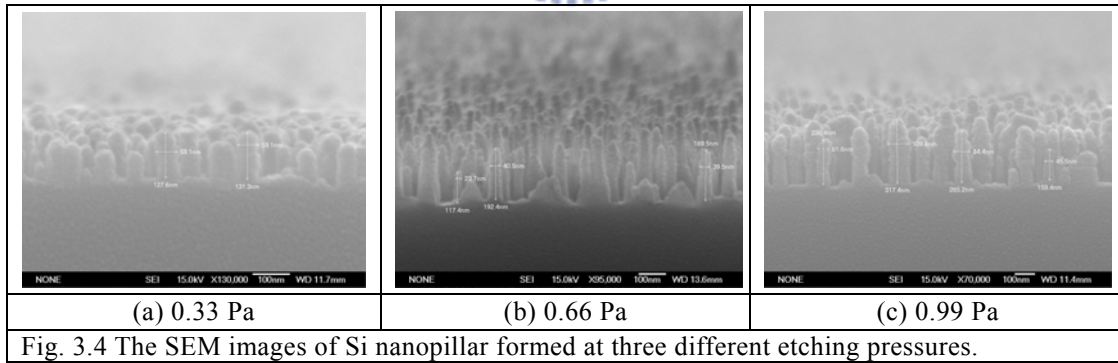
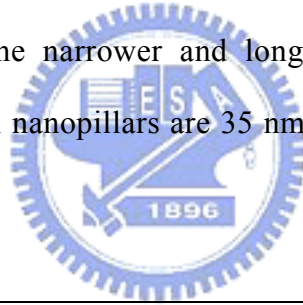
various Ar flowing from 10sccm to 40sccm. From Fig. 3.2, we can find that the etching depth of Si nanopillars would be shallow if the Ar flowing were too small. So we can get the optimum depth of Si nanopillars happened with the Ar flowing 40 sccm in our experiment because the etching rate can be enhanced by addition of Ar. The average diameter and length of the Si nanopillars are 35 nm and 170nm and the aspect ratio is nearly 5.



3.3-2 Chamber Pressure

One of the major factors affecting the etching results is the etching pressure during the etching process. If the pressure is too high, the etching rate will becomes too fast. If the etching rate is too high, the selectivity between the mask and the Si

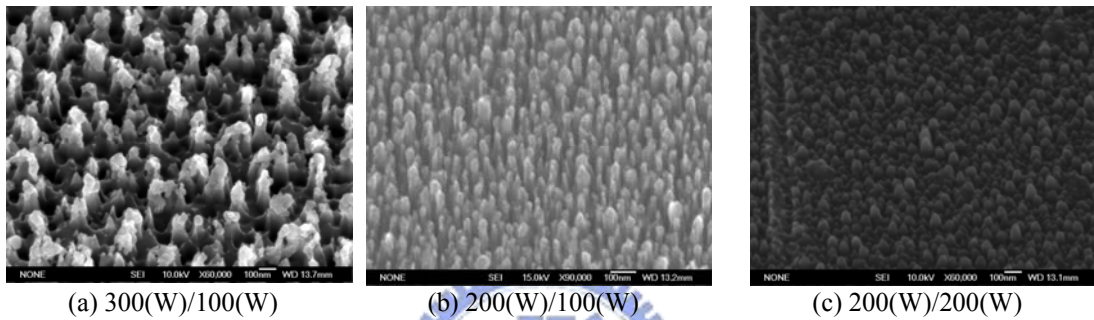
will decline and the side etching will also be serious to cut the Si nanopillars. So, the Si nanopillar won't be formed under the high etching pressure. As our experience, the etching pressure can't be more than 1.5 pa. On the contrary, the etching rate is too slow to etch Si in a few periods under the high etching pressure. In a conclusion, the appropriate etching pressure is very significant during the etching process. As shown in Fig. 3.4, we can observe that the etching depth is proportion to the etching pressure but not linearly. But the diameter of the Si nanopiliars is the smallest at the 0.66 pa pressure. This is mainly resulted from the side etching. The diameter of the Si nanopillars would be decreased by the highly side effect, but too high side effect would cut the Si nanopillars with the small diameter and leave the Si nanopillars with larger diameter. Analyzing Fig. 3.4, we can get the most proper etching pressure 0.66 pa to form the narrower and longer Si nanopillars. The average diameter and length of the Si nanopillars are 35 nm and 170nm and the aspect ratio is nearly 5.



3.3-3 Etching Power

To perform the Si nanopillar formation, the key issue is the proper magnitude of the etching power. There are two kinds of powers included in the ICP-RIE equipment that are the rf and bias power. The rf power decides the isolating level of the etching gases

and the dc bias power controls the vertical level of the side wall. In this experimental process, the experimental tests for the two powers are the ratio and magnitude. From the 45° view angle of the SEM images in Fig. 3.5, we can compare the different formation of Si nanopillars at the instinct power ratio. In this comparison, we chose the optimum results which are the largest length. So, the etching time is also different for the different power ratio. The etching time is 3 min、5min and 50 s when the rf/bias power is 300(W)/100(W)、200(W)/100(W) and 200 (W)/200(W).



(a) 300(W)/100(W) (b) 200(W)/100(W) (c) 200(W)/200(W)
Fig. 3.5 (a) shows the apparently triangle shape of Si nano-pillar. (b) The sharper sidewall of Si nanopillar. (c) A sharp side-wall of Si pillar with insufficient height.

Figure 3.5(a) shows that the by-product appears and the shape of Si nano-pillar resembles a pyramid when the ratio is 3. Then the density is the smallest and the diameter is the largest. The cause is isotropic etching erodes the smaller pillar, and the reason for a pyramid shape is that the vertical etching-rate is not bigger than the side etching-rate so the diameter of the pillar becomes bigger after longer etching time. Finally, the etching rate is dominated by the power. So we are sure the ratio of 3 is too big to get a straight pillar. Figure 3.5(b) shows the success of the formation of Si nanopillars with a perpendicular sidewall at the ratio of 2. The density and diameter of Si nanopillars are $2.8 \times 10^{10} \text{ cm}^{-2}$ and 29 nm. Figure 3.5(c) shows the straight but short Si nanopillars at the ratio of 1. This is because the vertical etching is too big to balance the etching selection between Ni and Si, we can see the Ni mask disappeared during the etching.

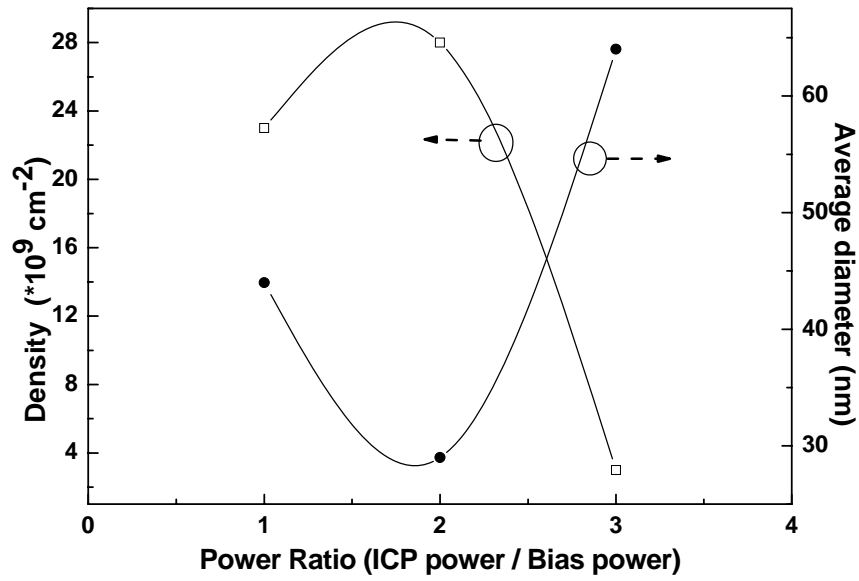


Fig. 3.6 Different ratio of ICP power over bias power has different influence on the vertical level of Si pillars' side-wall.

In another word, the appropriate ratio of bias and ICP power is the key point to get sharp sidewall and large height of Si nanopillars. After analyzing the SEM data in Fig. 3.6, we can know the ratio of bias power over ICP power had great influence on the character of Si nano-pillars such as the diameter and the density. In summary, we know that the ratio of 2 is the most suitable for the formation of Si nanopillars. From Fig. 3.7 we can know if the magnitude is bigger, the Si nano-pillars will be longer and the size of them will be wider. The average size of bias/ICP power at 100(W)/200(W) is 29 nm and the average one at 50(W)/100(W) is 44nm. The average height of 100(W)/200(W) is 150nm and the one of 50(W)/100(W) is 250nm. From the cross-session image in Fig. 3.7, Si nanopillars with high aspect-ratio were formed at the bias/ICP power of 2 whatever the magnitude of the powers is.

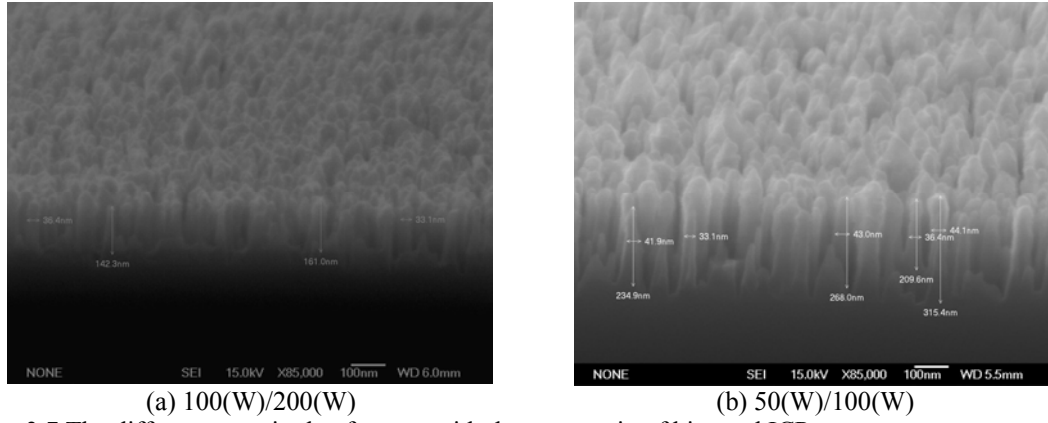
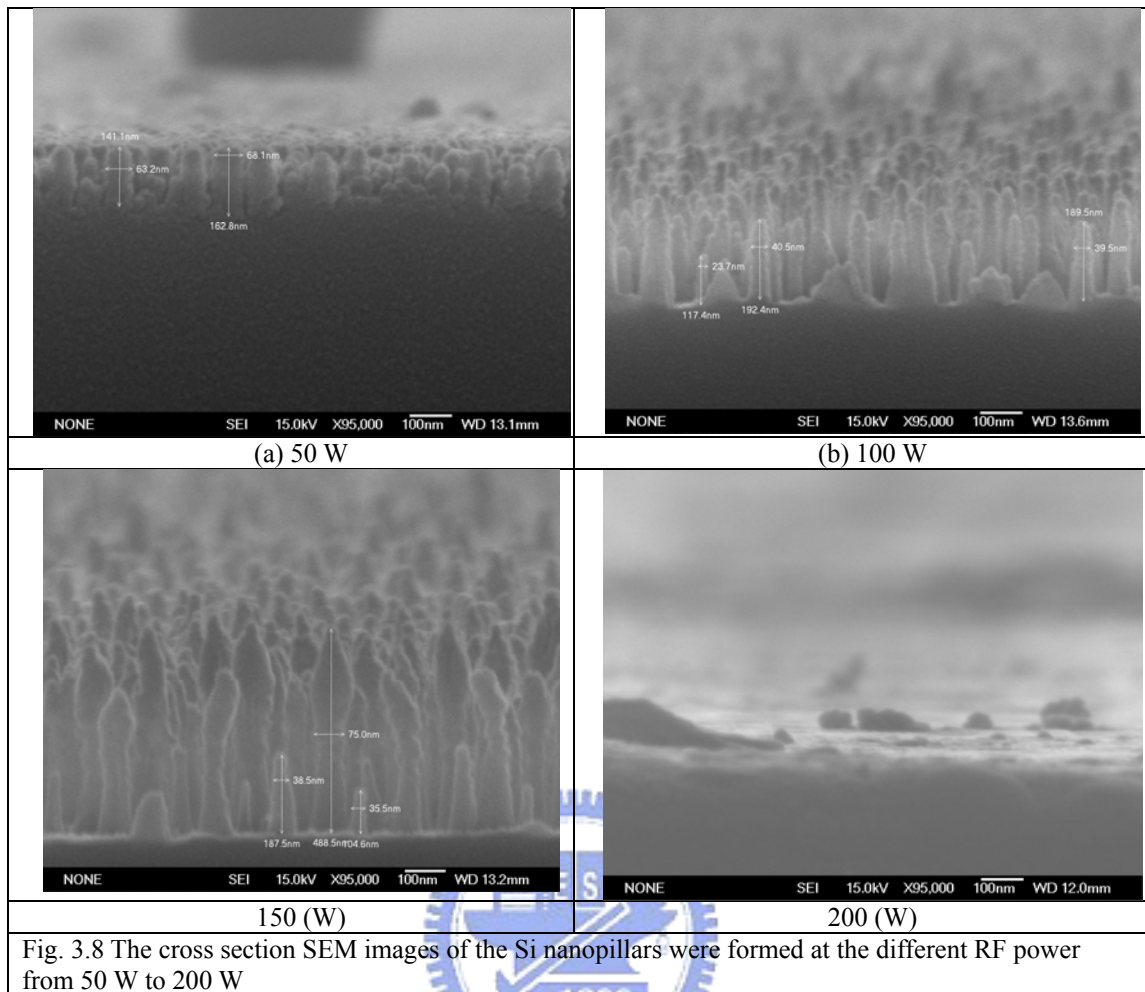
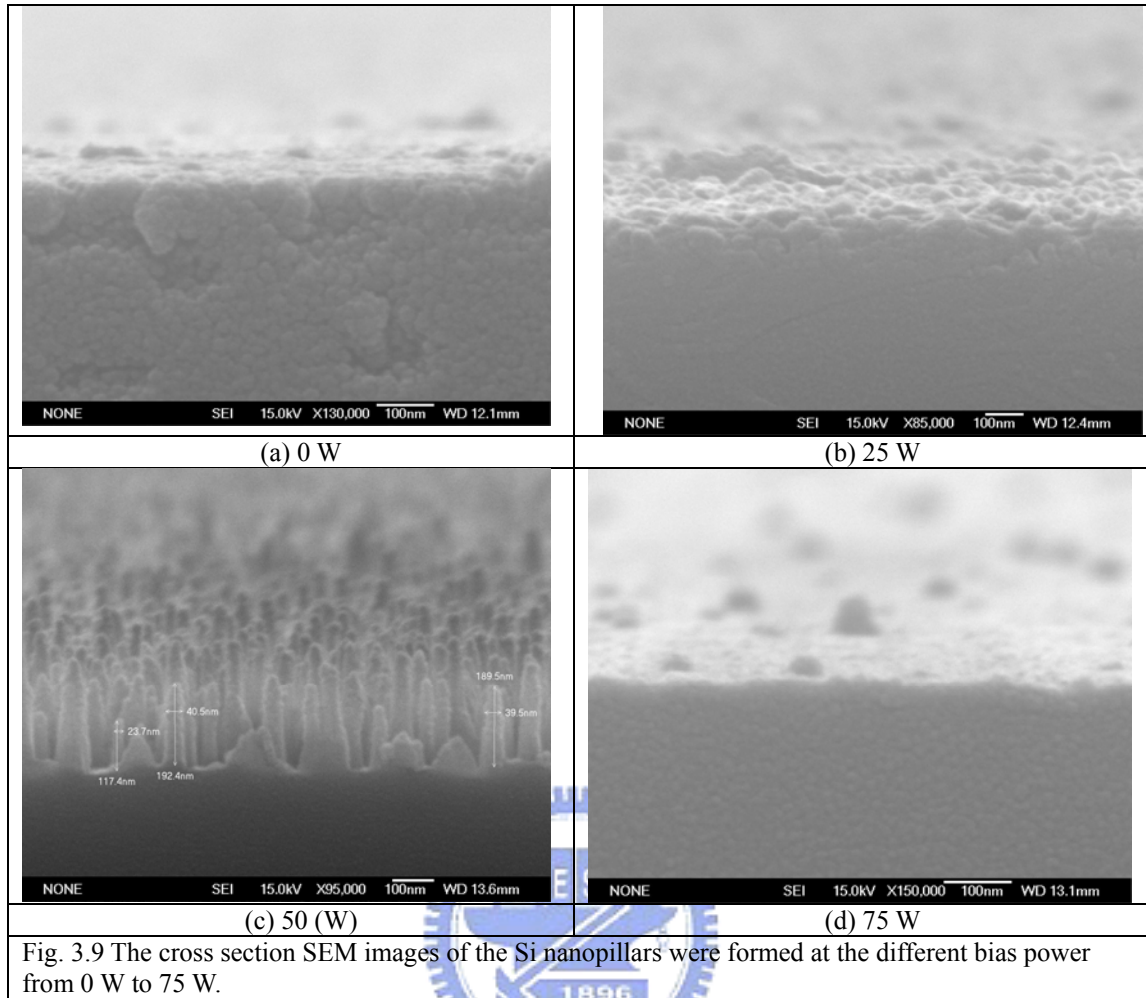


Fig. 3.7 The different magnitude of power with the same ratio of bias and ICP power.

After testing the generally proper rf / bias power ratio and magnitude, the individual effect of the rf and bias powers were also studied. In this part, the etching mask is the Ni nanodots forming after the RTA at 850°C for 120 s and the density of Ni nanodots is about $5 \times 10^{11} \text{ cm}^{-2}$. Analyzing from Fig 3.8, it is clearly that the magnitude of rf power affects the etching rate and selectivity a lot. Nevertheless, the etching rate is tradeoff with the etching selectivity. In Fig. 3.8 (a), the etching selectivity is high but the etching rate is very low when the rf power is 50 W. The average depth is about 100 nm. In Fig. 3.8 (b), the etching selectivity and rate are good and the average depth is 170 nm when the rf power is 100 W. In Fig. 3.8 (c), the etching selectivity and rate are the optimum tradeoff for the largest depth of 400 nm when the rf power is 150 W. In Fig. 3.8(d), the Si nanopillars disappeared for the low etching selectivity and high etching rate. So, the rf power of 150 W is the most appropriate for balancing the etching selectivity and rate. The average diameter and length of the Si nanopillars are about 50 nm and 400 nm, so the aspect ratio is about 8.

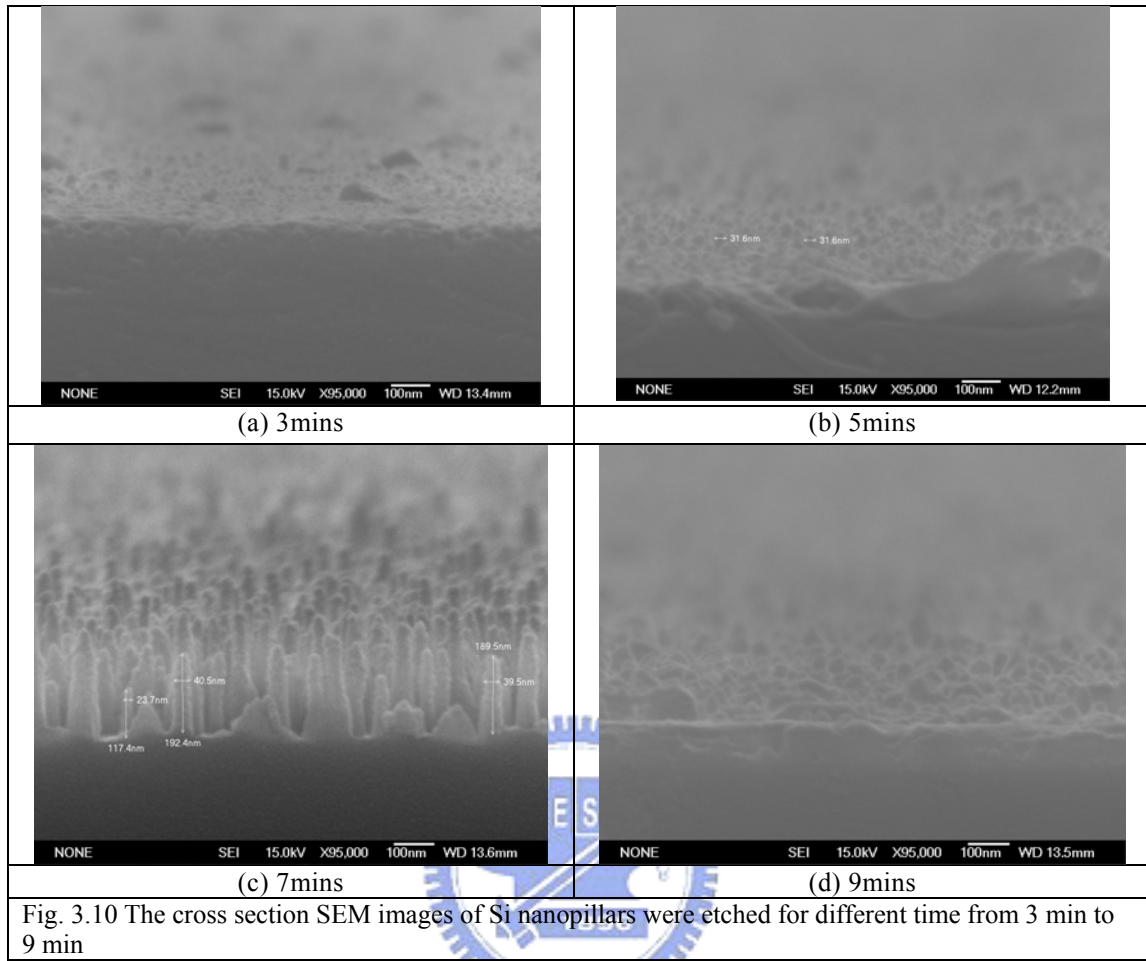


For the dry etching by ICP-RIE, the vertical etching is controlled by the bias power. And it affects the etching rate and selectivity more sensitively than rf power. After observing the SEM images in Fig. 3.9, the Si nanopillars were almost formed at the bias power of 50 W. In Fig. 3.9 (a), the etching depth is nearly 0 nm at the bias power 0 W. From Fig. 3.9(a)-(c), the etching depth is proportion to the magnitude of the rf power. But, the Si nanopillars were etched over on the account of too huge power in Fig. 3.9 (d). Finally, we get the most suitable magnitude of bias power is 50 W. The average diameter and length of the Si nanopillars are 35 nm and 170nm and the aspect ratio is nearly 5.



3.3-4 Etching Time

By the intuition, the etching depth will be longer if the process takes more time to etch. From Fig. 3.10 (a)-(c) the etching result matches the intuition. However, the etching time extending over the optimum time would over etch the Si nanopillars. Because the Ni mask also etched by plasma, the long-timed etch would remove the Ni completely. The Si nanopillars without Ni cap would shorten during the etching process. In our etching process, the optimum etching time is 7 min when the pressure 、CF₄/Ar flowing and rf/bias power are 0.66 pa 、40(sccm)/40(sccm) and 100(W)/50(W). The average diameter and length of the Si nanopillars are 35 nm and 170nm and the aspect ratio is nearly 5.



3.4 Conclusion

Si nanopillars with high aspect ratio were formed on Si substrate with the self-assembled Ni nanodots by ICP-RIE. The etching depth was proportion to the magnitude of CF_4 flowing、Ar flowing、the chamber pressure、the etching time、the bias power and the rf power, but the etching selectivity between the Si and Ni dots is completely opposite. Because of the tradeoff of the etching depth and the etching selectivity, there is an optimum value to every etching parameter. In our experiment, the optimum aspect ratio of Si nanopillars happened with the average diameter and depth of 50 nm and 400 nm in our experiment when the gas flowing of CF_4 and Ar、the bias/rf power、the chamber pressure、the etching time were set at

40sccm、40sccm、50(W)/150(W)、0.66pa and 7 min. Comparing to the results of the Korean [3.7], the density of the Si nanopillars in our experiment is over ten times larger than the Korean because of the Ni nanodot mask of the high density. Limited to the size of the Ni nanodots, the average diameter of the Si nanopillars is in the range of 30 nm to 50 nm.

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Chapter 4

Optical and Electrical Characteristics of Si nanopillars

4.1 Introduction

The increasing interest in low dimensional Si structures for potential applications in optoelectronics has given rise to significant progress on the development of both the fabrication process and the related physical mechanisms for versatile Si nanostructures. [4.1-4.5] Theoretical studies of Si quantum wires confirm that there is a transition of the band structure from indirect to direct bandgap in Si nanostructures due to the electron confinement in nanostructures, [4.6-4.8] which may be corroborated by characterizing the luminescent spectroscopy of the well controlled and ordered nanostructures. The intriguing electrical, optical, mechanical, and chemical properties, suggest that Si quantum wires may be used for developing field emitting devices [4.9] 、surrounding gate transistors [4.10] 、2-D photonic crystal slab [4.11] and bio-sensors, [4.12] etc.

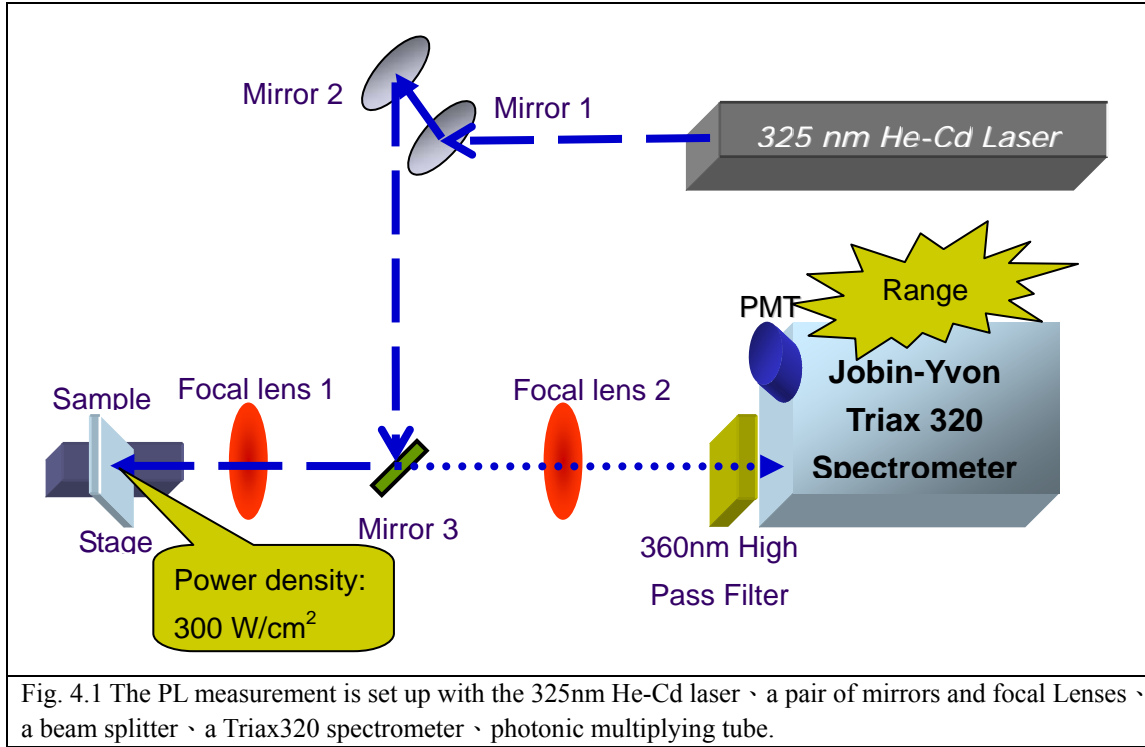
In 1998, Papadimitriou et al. fabricated highly anisotropic Si nanopillar array with an aspect ratio of 25:1 and a diameter <100 nm by using nano-lithography and dry-etching after several cycles of thermal oxidation and oxide removal procedure.[4.13] The anisotropic Si nanopillar array emits photoluminescence (PL) at wavelength of 500-600nm, while the PL efficiency and wavelength were found to be corrected with the wavelength and the polarization state of the pumping laser. Such a dependence was attributed to the quantum-confined polarization effects In 2004, Yanagiya et al. tried to grow Si nanowires on sapphire with a diameter of 50 nm and a height of 1 μ m by using a disilane (Si_2H_6) gas-source based molecular beam epitaxy (MBE). [4.14]. Visible

low- and room-temperature PL from the Si quantum wires was observed at central wavelength of 750 nm. The PL intensity at 9 K is blue-shifted and is 20 times larger than that at 300 K. On the other hand, Nassiopoulos et al. have implemented the electroluminescent (EL) device based on Si nanopillars in 1996. [4.15] Visible light emission was observed under a forward bias the voltage exceeding of 12–14 V. The EL characteristics were similar to the PL, which is attributed to a high electric field electronic transporting through the Si nanowires.

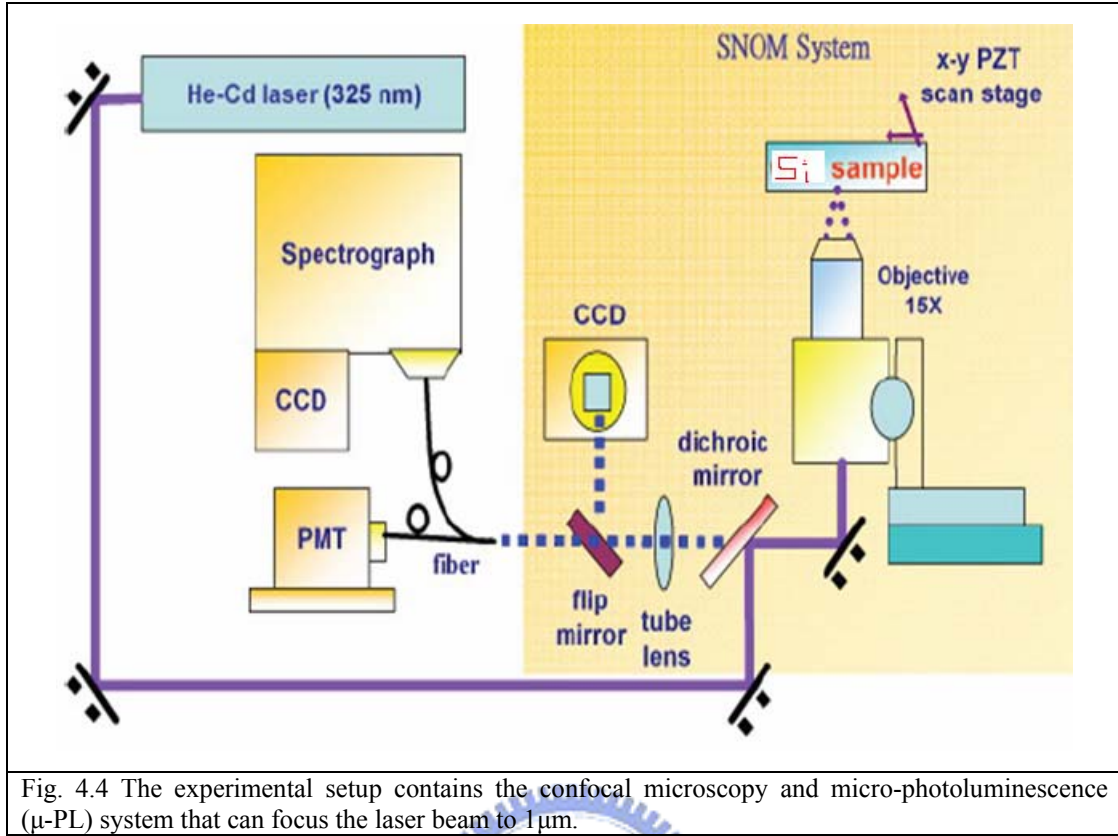
In this chapter, we discuss the power dependent PL of the original and oxidized Si nanopillar array. The surface reflection of Si nanopillar array on Si substrate are analyzed and compared with that of the bulk Si wafer. Furthermore, the current-voltage and capacitance-voltage characteristics of Si nanopillar array are also studied.

4.2.1 Experimental

The measuring setup is shown in the Fig. 4.1. A HeCd laser at 325 nm employed as the pumping source, and a Triax 320 spectrometer, with a photomultiplier tube (PMT) are employed to analyze the PL of Si nanopillars. The spot size and pumping power of the laser are set as 100 μm and 25 mW, respectively. A notch filter is installed to reject the scattered pumping laser from sample surface. To avoid the gradual oxidation effect, the Si nanopillar sample is dipped in methyl alcohol before diagnosis. The sample is dried in the air for 2 minutes prior to the measurement.



To pump the Si nanopillar array at higher intensity, a confocal microscope based micro-photoluminescence (μ -PL) system is introduced. The sample is placed on a 2-D stage that can be scanned by a piezoelectric feedback controller with a position accuracy of less than 3 nm. A 3-D stepping motor controlled stage was used to align the microscopes collinearly. A 15x UV objective lens with a numerical aperture 0.32 is used to collect the PL from the sample into a monochromator-PMT link through an optical fiber with core diameter of 25 μ m and 600 nm, respectively. A high-resolution digital camera is used to record the microscopic images of the sample. The optical resolution of the confocal microscope is about 1 μ m and determined by the core-diameter of the optical fiber. The pumping power of 25 mW corresponds to an intensity of 31800 W/mm² under a strongly focused condition.



4.2.2 Structural Damage Dependent PL

After removing the mask made by Ni nanodots and SiO₂ film on Si substrate, the height and density of the Si nanopillars are measured as 30-100 nm and about $5.4 \times 10^{10} \text{ cm}^{-2}$ by using atomic force microscopy and scanning electric microscopy. The as-etched Si nanopillars exhibit strong PL at blue-green wavelength instead of near-infrared region due to the strong surface damage occurred during the ICP-RIE process with the etching gas O₂. Such a visible PL has previously been attributed to the oxygen defects accompanied with the oxygen plasma destruction.

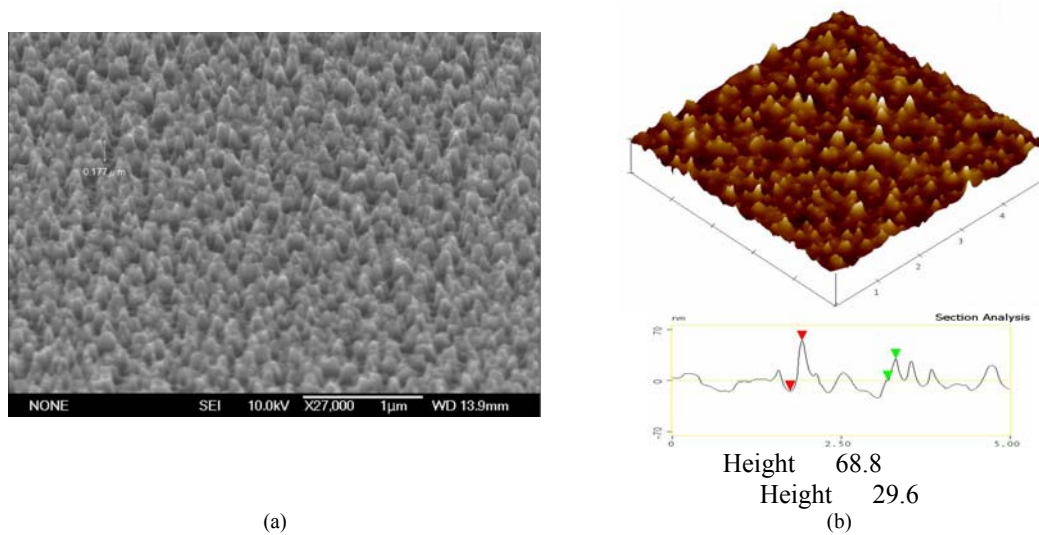


Fig. 4.2 (a) SEM image of Si nano-pillars after removing the Ni and SiO₂ layers at the etching-power ratio of 2 for 3 min. (b) AFM data including 3-D 45° view angle image and the height profile.

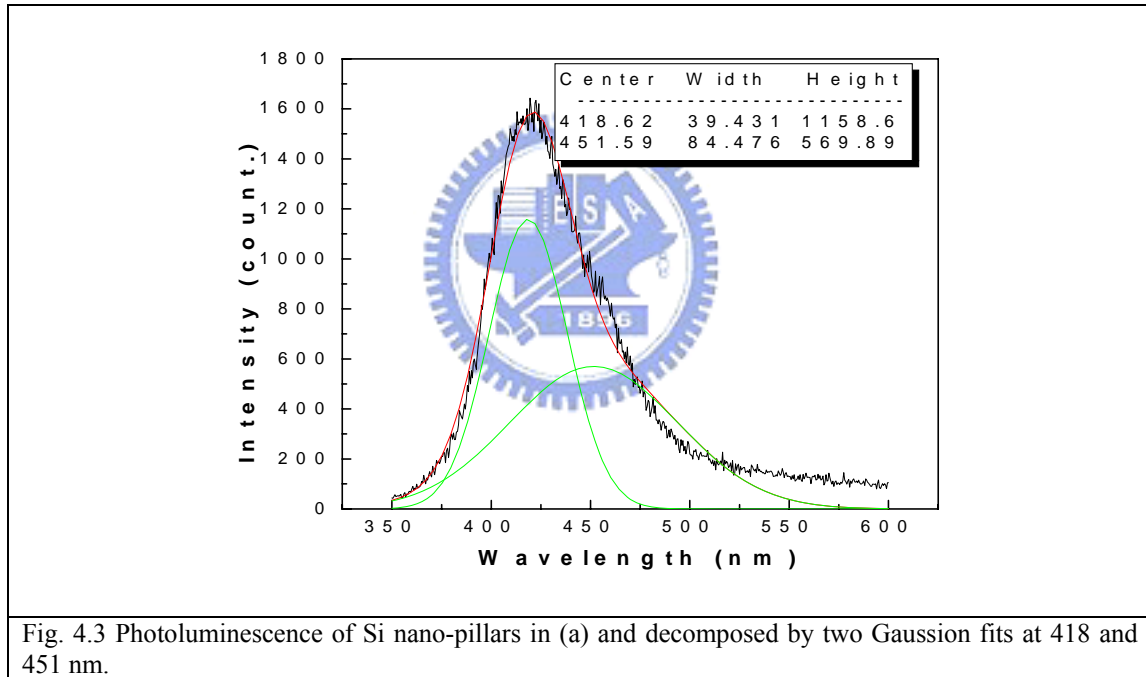


Fig. 4.3 Photoluminescence of Si nano-pillars in (a) and decomposed by two Gaussian fits at 418 and 451 nm.

Previously, the luminescent centers in the SiO₂: Si⁺ corresponding to the visible PL was comprehensively investigated which the weak oxygen bond (WOB) and the neutral oxygen vacancy (NOV) defects at emitting wavelengths of around, 415 nm and 455 nm, respectively [4.16-4.19]. The Si nano-pillar sample presents a strong and broad PL spectrum between 400 and 450 nm. After decomposing with a multi-Gaussian function, two principle luminescent centers at 418 and 451 nm with corresponding linewidths of

39 and 84 nm, respectively, are shown in Fig. 4.2(c). These PL components are very similar to those obtained by Nishikawa *et al.* [4.16], and Bae *et al.* [4.17], which has been attributed to the transition between the ground state (singlet) and the elevated state (triplet) of the NOV defects. During the ICP-RIE process, the ionized O₂ impact the surface of the Si substrate. Raising the pumping power density didn't change the PL shape except the saturation in PL intensity under the high pumping power, as shown in Fig. 4.3 (a). In principle, the quantum confined phenomenon occurs as the size of nanostructure becomes less than 10 nm.

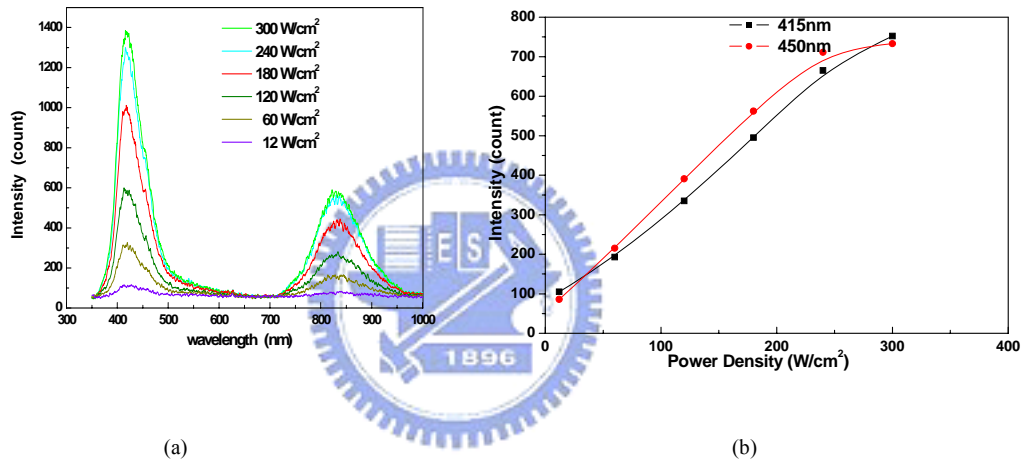
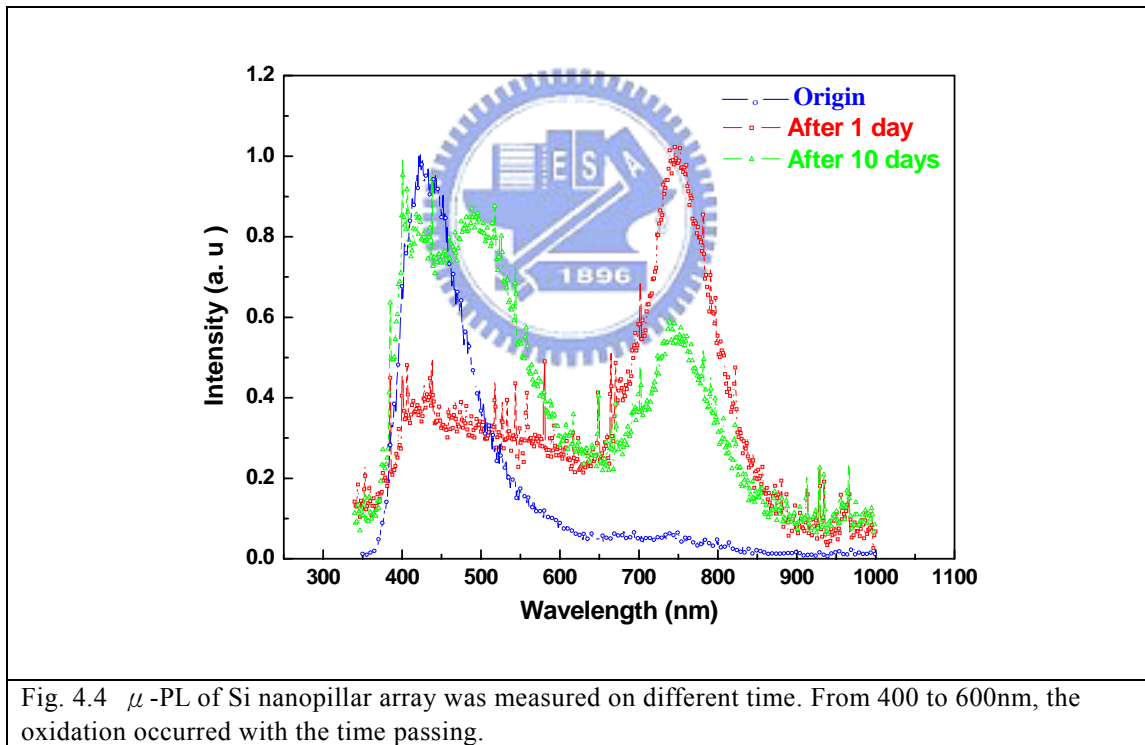


Fig. 4.3 (a) Photoluminescence of Si nano-pillars for different pumping power densities. (b) Peak intensity for different pumping power densities.

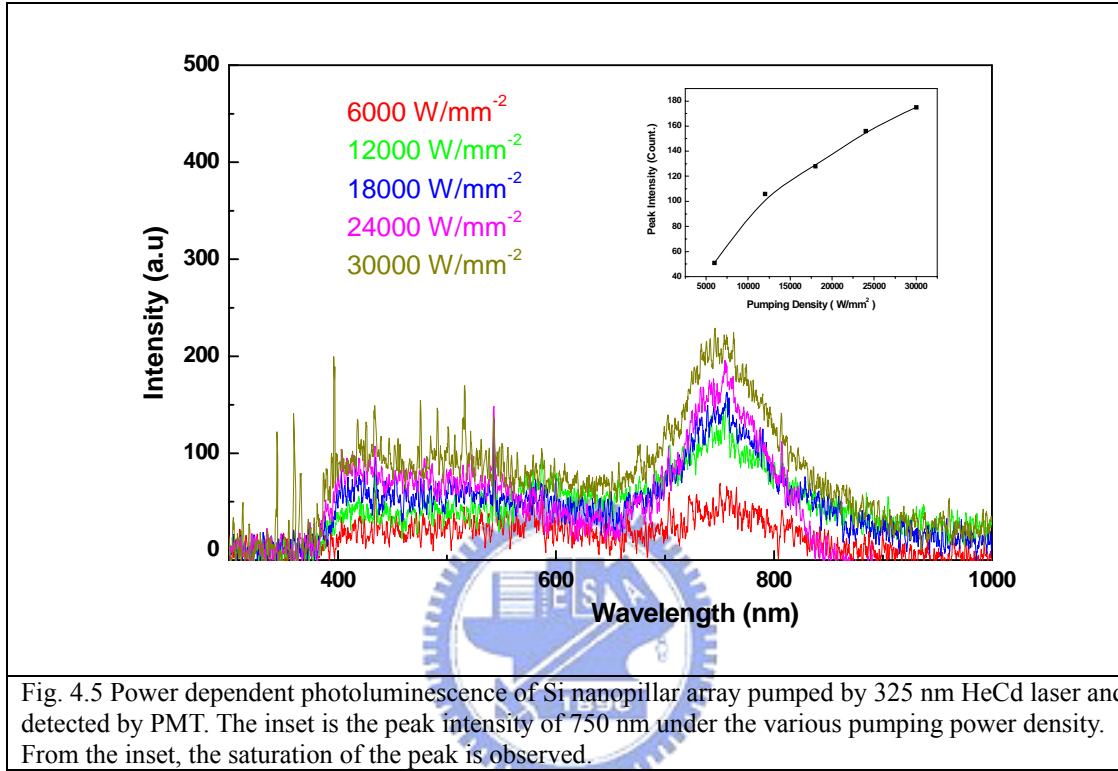
By using μ -PL, the pumping density can be increasing to four order magnitude larger than that used in general PL system. As a result, the μ -PL spectrum of Si nanopillars reveals at two peak wavelengths at 500 and 750 nm, in which the signal at 750 nm is not observed in previous PL result. Increasing the pumping intensity could pump more emitting centers in the Si nanopillars. Yanagiya *et al.* [4.14] has previously discovered the similar PL component of 750 nm peak from 1 nm-wide Si nanowires. In our case, the size of the Si nanopillars can be reduced through the natural oxidation process, which enhances the PL at 750 nm after one-day exposure in atmosphere. However, the PL intensity decreases again as the exposure time extends to 2 days or

longer. As an evidence, the PL of the original Si nanopillars ranged from 400 to 500 nm. After one-day oxidation, the PL at wavelength of 750 nm is enhanced as most of the Si nanopillars shrink their size to quantum confined scale. As the oxidation duration lengthens to 10 days, the near-infrared PL decreases. In contrast, the blue-green PL increases as the oxidation of Si nanopillars become serious. Another evidence for the quantum confinement is the blue shift of the near-infrared peak from 759 to 754 nm as the duration of oxidation lengthens. According to the quantum confinement theory [4.8], the bandgap of Si nanowires with a diameter $< 5\text{nm}$ will be significantly enlarged with the reducing wire size.



To investigate the oxidation effect of the Si nanopillar, the pumping power density was varied to study the change of the 750 nm peak of the Si nanopillars oxidized in atmosphere for different durations. Figure 4.5 illustrates that the peak wavelength remains unchanged, however, the PL intensity saturates with increasing

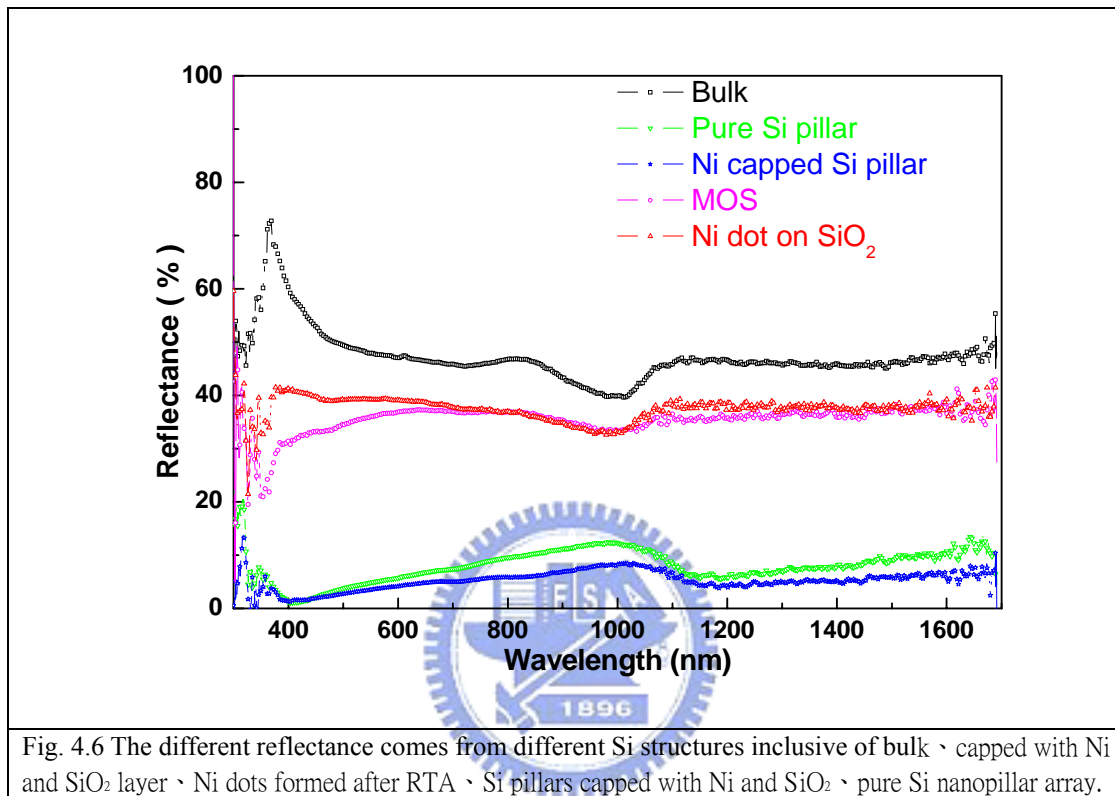
the pumping power density due to finite density of the Si nanopillars. The inset of Fig. 4.5 reveals the saturation of the PL peak intensity at 750 nm when the pumping power density enlarges to 12000 W/mm^2 .



4.3 Reflection

The Si nanopillar roughened surface inevitably causes a reflectance lower than that of the Si substrate [4.20], which has been characterized by using a white light source based reflectometry from 300 to 1700 nm. The reflectance of an aluminum sheet is set as 1 and the reflectance of a black cloth is set at 0, which are treated as the reference during measurements. As a result, the reflectance of Si wafer decreases after depositing Ni and SiO_2 , which further decreases after nano-mask formation and nanopillar etching. In the same way, the reflectance of the pure Si nanopillar roughened surface is larger than that of the Si nanopillars capped with Ni and SiO_2 . The result is agreed with our

hypothesis that the reflectance of the pillar form is smaller than the smooth surface because of the roughness. This is in Si solar cell because of the enhancement on absorption with the Si nanopillar structure. [4.21] 證據



After analyzing the angular dependent reflectance shown in Figs. 4.6 and 4.7, similar phenomenon has also been observed by Xi *et al.* [4.20] that the reflectance of the pure Si substrate is larger than the pure Si nanopillars. Nevertheless, the polarization dependent reflection was also found due to Si nanopillars with highly aspect ratio.

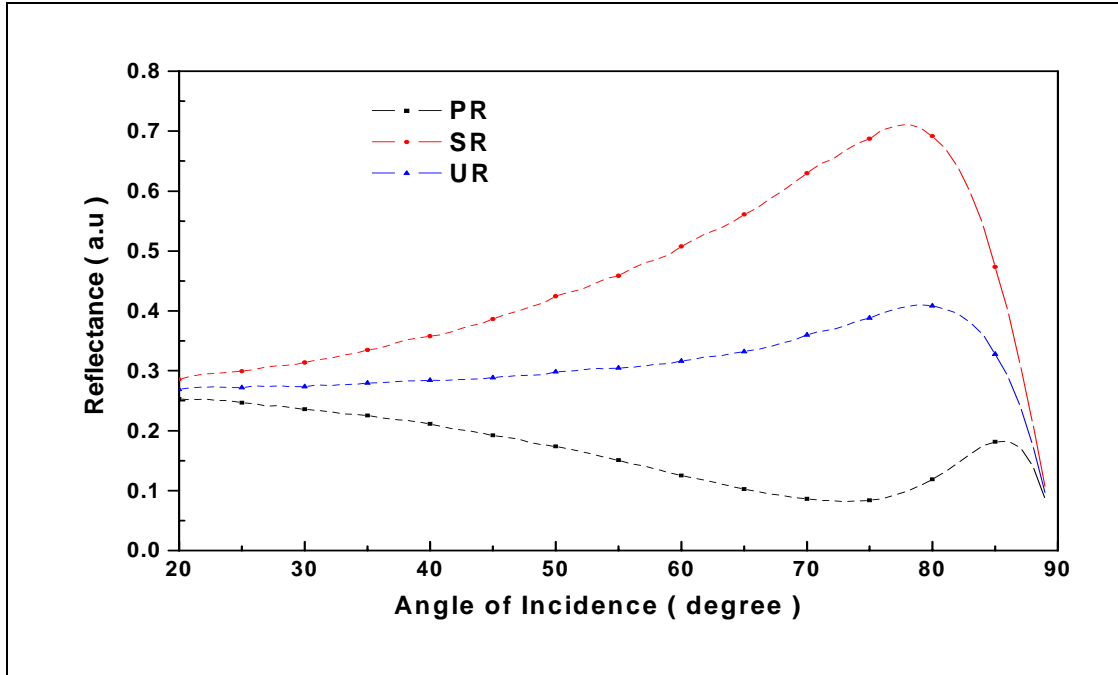


Fig. 4.6 The reflections of Si substrate were measured from the 20 degree to 89 degree for 632.8 nm. The pR stands for p-polarization (TM mode) ; the sR stands for s-polarization ; the uR stands for circle-polarization.

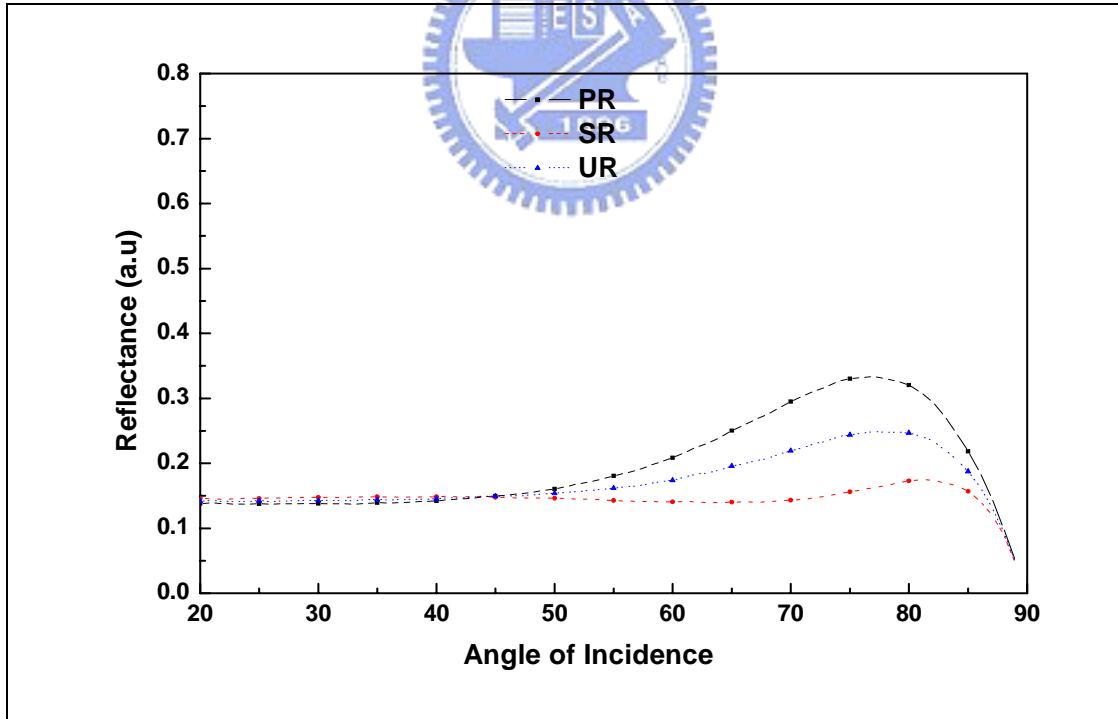


Fig. 4.6 The reflections of Si nanopillar array were measured from the 20 degree to 89 degree. The pR stands for p-polarization (TM mode) ; the sR stands for s-polarization ; the uR stands for circle-polarization.

4.4 Current-Voltage and Capacitance-Voltage Curve

In addition to the optical characteristics of the Si nanopillar, the characterizations on its electrical properties are also important to realize the application of the Si nanopillar emitters in IC industry. Because the Si substrate is p-type, the Ni nanodots can be treated as n-type contact similar with the MOS structure during the I-V measurement. The resistance of Si wafer is decreasing from 41.6 k Ω to 1.92 k Ω after depositing SiO₂ and Ni films. As the Ni self-aggregates during thermal annealing, the resistance is increased from 1.92 k Ω to 4.8 k Ω . Moreover, the resistance further increases from 4.8 k Ω to 11.8 k Ω after etching formation of the Si nanopillars. After removing the Ni and SiO₂ covering layers, the resistance increases again from 11.8 k Ω to 22.6 k Ω .

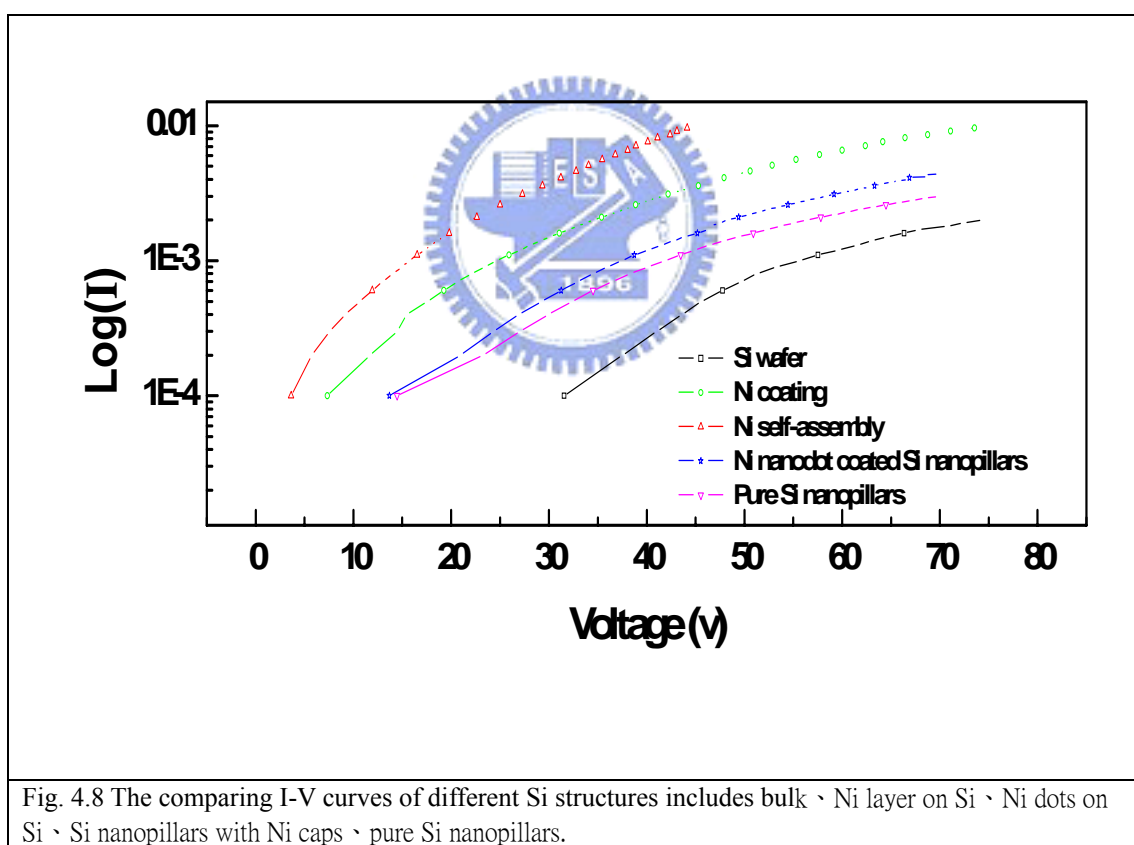


Fig. 4.8 The comparing I-V curves of different Si structures includes bulk, Ni layer on Si, Ni dots on Si, Si nanopillars with Ni caps, pure Si nanopillars.

Structures	Bulk	Before RTA	After RTA	Pillars with Ni	Pure pillars
Resister (Ω)	41.6 K	1.92 K	4.8 K	11.8 K	22.6 K

Table. 4.1 The resister values of the different Si structures are listed.

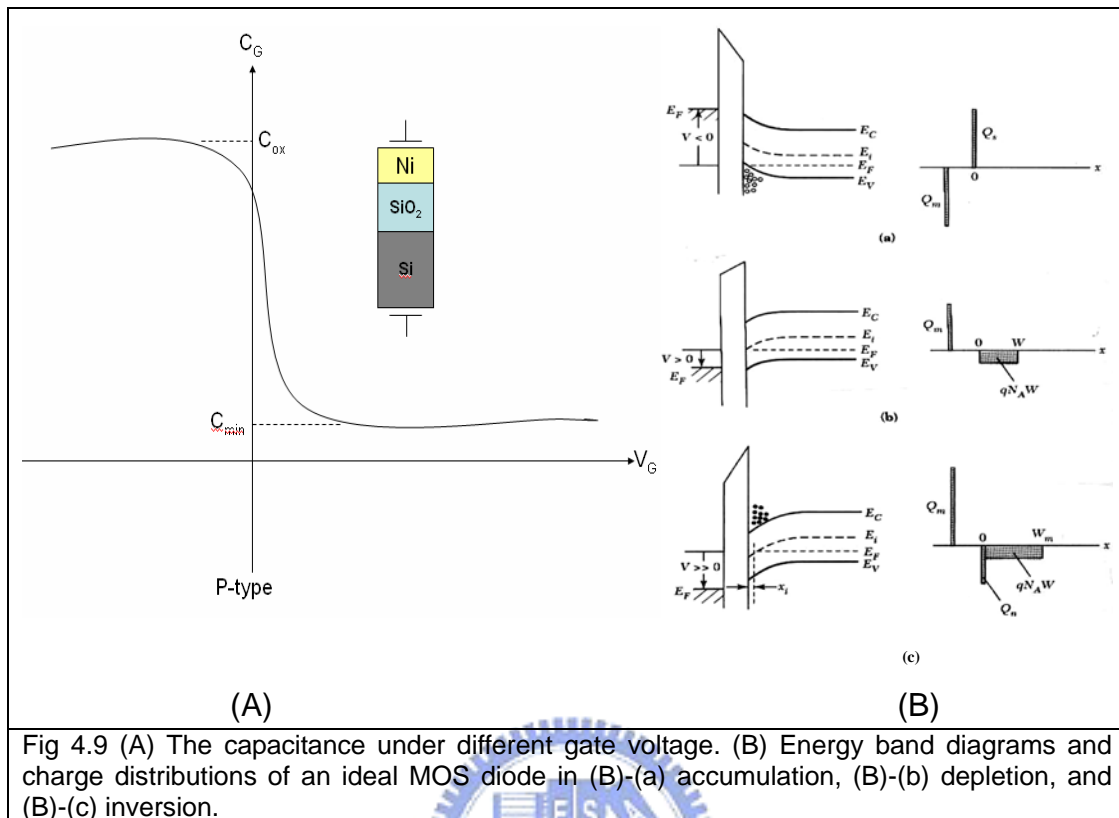


Fig 4.9 (A) The capacitance under different gate voltage. (B) Energy band diagrams and charge distributions of an ideal MOS diode in (B)-(a) accumulation, (B)-(b) depletion, and (B)-(c) inversion.

Another important electrical property is the capacitance-voltage characteristic that stands for the ability of catching electrical charges and the curves are shown in Fig 4.9 -A. According to the Sze' Semiconductor Devices in p.172, $p_p = n_i e^{(E_i - E_F)/kT}$, the upward bending of the energy band at the semiconductor surface causes an increase in the energy $E_i - E_F$, ($V_G < 0$) which in turn gives rise to an enhanced concentration, an accumulation of holes near the oxide-semiconductor interface. This is called the accumulation case shown in Fig 4.9-B-a. When a small positive voltage ($V_G > 0$) is applied to an ideal MOS diode, the energy bands near the semiconductor surface are bent downward, and the majority carriers (holes) are depleted. This is called the depletion case shown in Fig 4.9-B-b. When a larger positive voltage is applied, the energy bands bend even more so that the intrinsic level E_i at the surface crosses over the Fermi level as shown in Fig 4.9-B-c. That means the positive gate voltage starts to induce excess negative carriers at the SiO₂-Si interface. The electron concentration in

the semiconductor is given by $n_p = n_i e^{(E_F - E_i)/kT}$. Because the electrons (minority carriers) at the surface is greater than holes (majority carriers), the surface is inverted that is called inversion case. However, the simple criterion for the onset of strong inversion is that the electron concentration at the surface is equal to the substrate impurity concentration, i.e. $n_s = N_A$ ($E_i = E_F$). Since $N_A = n_i e^{q\phi_B/kT}$, (ϕ_B is the energy difference between E_F and E_i), the surface potential $\phi_s(\text{inv}) \doteq 2\phi_B = 2kT * (\ln(N_A/n_i))/q$. In the other extreme, when strong inversion occurs, the width of the depletion region will not increase with a further increase in applied voltage. This condition takes place at a metal-plate voltage that causes the surface potential ϕ_B to reach $\phi_s(\text{inv})$. At the onset of strong inversion, the voltage is called threshold voltage $V_T = (qN_A W_m / C_0) + \phi_s(\text{inv}) = (((2q\epsilon_s N_A (2\phi_B))^{1/2} / C_0)) + 2\phi_B$. For p-type Si substrate, V_T is positive because the bias voltage of the Si substrate must be on the negative region to get electrons for inversion. On the contrary, V_T is negative for n-type Si substrate.

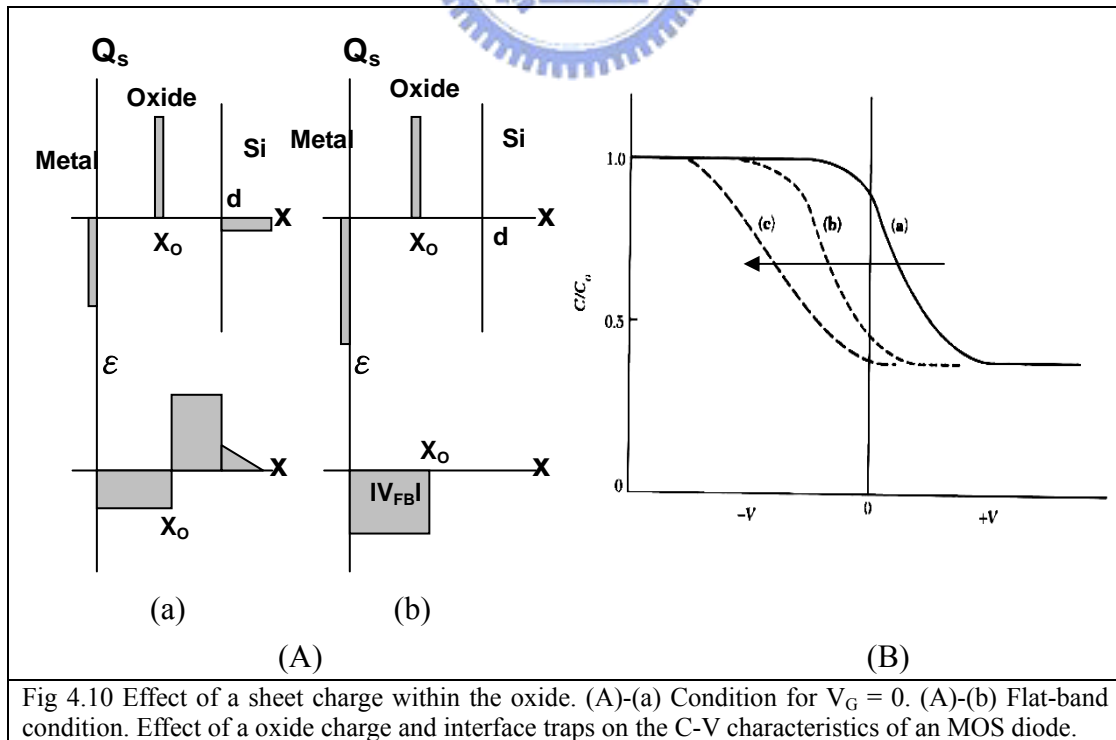


Fig 4.10 Effect of a sheet charge within the oxide. (A)-(a) Condition for $V_G = 0$. (A)-(b) Flat-band condition. Effect of an oxide charge and interface traps on the C-V characteristics of an MOS diode.

However, consider a positive sheet charge Q_0 within the oxide and this charge will induce negative charges partly in the metal and partly in the semiconductor as shown in Fig. 4.10-A-a. To reach the flat-band condition (i.e. no charges induced in the semiconductor), we must apply a negative voltage to the metal, as shown in Fig. 4.10-A-b. Until the electric field at the semiconductor surface is zero, the flat-band voltage $V_{FB} = -\epsilon_0 X_0 = -Q_0 X_0 / \epsilon_{ox} = -Q_0 X_0 / C_0 d$. Due to Q_0 , the c-v curve will be parallel-shifted that is illustrated from the c-v curve (a) to (c) in Fig. 4.10-B. In this condition, the threshold voltage $V_T = V_{FB} + (((2q\epsilon_s N_A (2\phi_B))^{1/2} / C_0)) + 2\phi_B$.

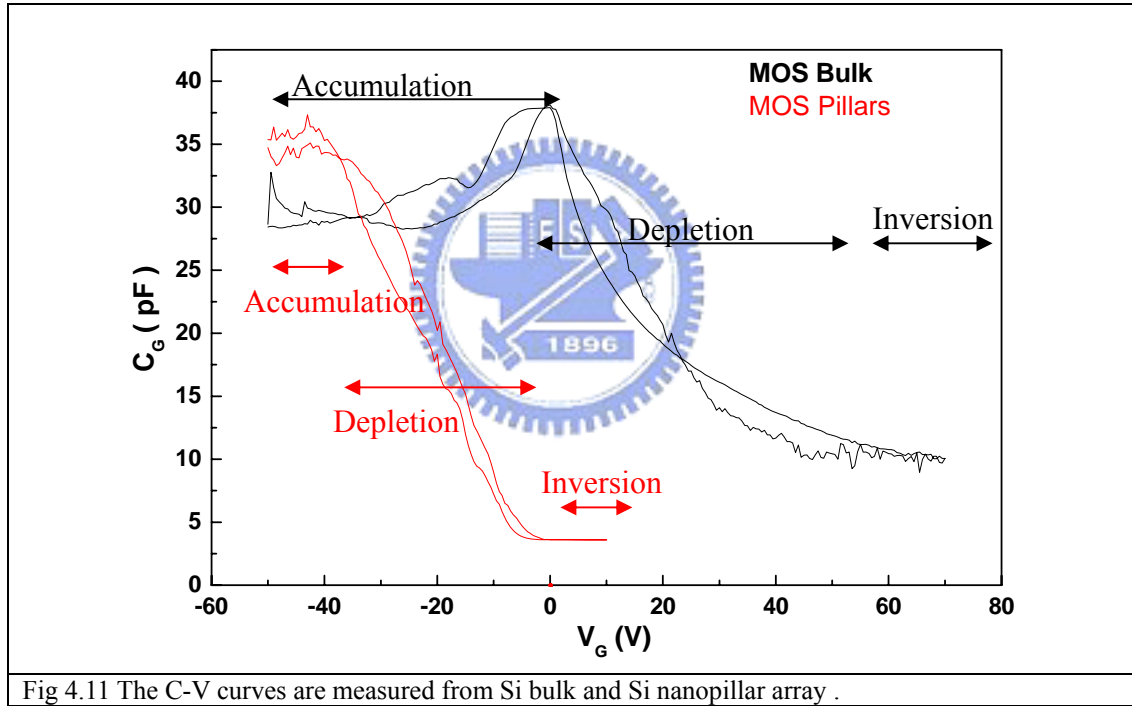


Fig 4.11 The C-V curves are measured from Si bulk and Si nanopillar array .

In this essay, we measured the c-v curves of bulk and pillar MOS (metal-oxygen-semiconductor) structures shown in Fig.4.11. The scanning rate is 1 s/point and the step point is 0.5 V/point in the c-v measurement. The apparent c-v curve shift from the bulk MOS diode to the nanopillar MOS diode is about 60 V that is surely caused by the positive defect charges resulting in the variation of V_T base on the MOS capacitance rule in Sze's Semiconductor Devices. The positive-charged defects might

be activated during RTA and etching process. According to E. H. Poindexter in 1988, the charge hysteresis in the Si nanopillar is mainly produced by the neutral oxygen vacancy (NOV) because NOV defect will catch positive charge and become positive charges. The reactive equation $O_3 \equiv Si-Si \equiv O_3 + hole \rightarrow O_3 \equiv Si^+ \cdot Si \equiv O_3$ and this kind of defects is almost induced at the high temperature annealing.[4.22] As the rule $C = \epsilon A / X_{ox}$, the capacitance should decrease in the small area. However, the accumulation region, the C_{ox} of the MOS diode made on Si-nanopillar roughened substrate is about 35 pF which is slightly larger than that made on the Si substrate deposited with 200-Å SiO_2 and 50-Å Ni film 27.5 pF. This is caused by the current leakage resulted from the bad insulating quality of SiO_2 film. However, the current leakage can be deduced by the nanopillar form possibly because of the air-filled area in the structure. And due to the oxidation of the Si nanopillars, this stores more electric charges and thus increases the capacitance. In the inversion region, the C_G of the MOS diode made on Si-nanopillar roughened substrate is about 3 pF which is slightly smaller than that made on the Si substrate deposited with 200-Å SiO_2 and 50-Å Ni film 10 pF. From the Fig 4.9(B)-(c), the $C_G = C_{ox} C_s / (C_{ox} + C_s)$. According to the above description that the C_{ox} of the MOS diode made on Si-nanopillars is slightly larger than that made on the Si substrate deposited with 200-Å SiO_2 and 50-Å Ni film, the C_G of Si pillar MOS diode should be larger than the Si bulk MOS diode. Nevertheless, the small area decrease the C_s largely and in trade-off condition C_G decreases finally. Besides, the switching time of pillar MOS diode of 1mins is smaller than the bulk MOS diode of 2 mins. Owing to this advantage, the Si-nanopillar structure has been used in many transistor devices such as MOSFETs (metal-oxide-semiconductor field effect transistor) [4.23] and SGTs (surrounding gate transistors) [4.10] due to its low threshold voltage and low parasitic capacitance. Comparing with the bulk Si structure, the Si nanopillars owned the high-speed charging and discharging features but possess the problem of relatively large

leakage current.

4.5 Conclusions

The Si nanopillars with diameter 30-70nm presents a strong and broad PL spectrum where the peaks at 415-455 nm with linewidths of 35-50 nm were originated from the transitions of the weak oxygen bond, and the NOV defects. The saturating peak of 450 nm under high pumping power density 300 W/cm^2 is due to the finite luminescent centers in this defect. These two defects are mainly produced from the RTA (thermal activation) and etching process (O_2 ionized). The $\mu\text{-PL}$ at wavelength of 750 nm appeared under a pumping density that is 10^4 times larger than that used in the common PL system. A blue-shift from 759 nm to 754 nm in $\mu\text{-PL}$ after the oxidizing period from 1 day to 10 days and this peak saturating under larger pumping power density has proved the existence of quantum confined phenomenon in Si nanopillars. The long-term oxidization (up to 10 days) of Si nanopillars degrades the Si quantum confining centers and increases the luminescent centers of the oxygen defects in opposite. In the aspect of reflectance, the Si-nanopillars exhibit a smaller reflectance than the Si substrate because of the highly roughened surface. In electrics, pillar MOS diode owns a lower resistance of $11.8 \text{ k}\Omega$ than bulk MOS diode $1.92 \text{ K}\Omega$ because of the current leakage proven by the c-v analysis. Finally, comparing the bulk and pillar MOS diode, there are some good performances for the pillar MOS diode including lower threshold voltage V_T · high charging and discharging speed · higher C_{\max} and lower C_{\min} . After analyzing the flat-band voltage V_{FB} , the V_T shift from bulk MOS diode and pillar MOS diode is about -60 V mainly due to the positive charge defects (NOV defects : $\text{O}_3\equiv\text{Si}-\text{Si}\equiv\text{O}_3 + \text{hole} \rightarrow \text{O}_3\equiv\text{Si}^+\text{Si}\equiv\text{O}_3$) which were originating in the SiO_2 during RTA process. Moreover, the charge hysteresis of pillar MOS diode c-v curve

is also affected by the NOV defects. [4.22] Because the current leakage can be deduced by pillar structure, C_{ox} of pillar MOS diode 35 pF is larger than bulk MOS diode 27.5 pF. However, the smaller surface area of pillar MOS diode decrease the surface capacitance C_s resulted in the smaller C_{min} 3 pF than bulk MOS diode 10pF.

4.6 References

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Chapter 5

Summary

5.1 Summary

By using a highly heat-accumulated and less-adhesive SiO₂ buffered layer, we successfully demonstrated a rapid self-assembly method for aggregating Ni nanodots on Si substrate as the etching mask. Due to the highly heat dissipated feature of Si substrate with a thermal conductivity of 148 W/m-K, the 200Å thin SiO₂ layer with the ultralow thermal conductivity of only 1.35 W/m-K facilitates the self-assembly of Ni nanodots from retaining the thermal power on the SiO₂ layer. The required annealing time for synthesizing the Ni nanodots with comparable density and size is greatly shortened to <30 seconds. The self-aggregated Ni nanodots with highest density and smallest size of $7.2 \times 10^{10} \text{ cm}^{-2}$ and 33 nm, respectively, are obtained at the optimized RTA condition at 850°C for 22 sec. The larger size and smaller density of Ni nanodots could be obtained after RTA if the SiO₂ film or the Ni layer becomes thicker. Raising the RTA temperature 、lengthening the RTA time and depositing thick SiO₂ film or Ni layer will concurrently cause the effects of size enlargement and density dilution.

Si nanopillars with the high aspect ratio were formed on Si substrate with the self-assembled Ni nanodots annealing at 850°C for 120 sec by ICP-RIE. Limited to the size and the density of the Ni nanodots, the average diameter of the density Si nanopillars are nearly 50 nm and 10^{10} cm^{-2} . Comparing to the results of the Korean [5.1], the density of the Si nanopillars in our experiment is over ten times larger than the Korean because of the Ni nanodot mask of the high density. The etching depth was proportion to the magnitude of CF₄ flowing 、Ar flowing 、the chamber pressure 、the etching time 、the bias power and the rf power, but the etching

selectivity between the Si and Ni dots is completely opposite. Because of the tradeoff of the etching depth and the etching selectivity, there is an optimum value to every etching parameter. In our experiment, the optimum aspect ratio of Si nanopillars happened with the average diameter and depth of 50 nm and 400 nm in our experiment when the gas flowing of CF_4 and Ar 、 the bias/rf power 、 the chamber pressure 、 the etching time were set at 40sccm 、 40sccm 、 50(W)/150(W) 、 0.66pa and 7 min.

The Si nanopillar sample presents a strong and broad PL spectrum where the peaks at 415-455 nm with linewidths of 35-50 nm were originated from the weak oxygen bond, and the peak at 455 nm was attributed to the transition between the ground state (singlet) and the elevated state (triplet) of the NOV defects. The changeless peak and the defect peak saturating in the dependent-power PL were because the density of the pumped energy level saturated under the high pumping power. This is also a proof that the two peaks are from the defects not from the Si quantum confine. The peak wavelength of 750nm appeared in the μ -PL pumped by the 10^4 times larger power density than the PL that could pump more emitting centers in the Si nanopillars. The quantum effect was proven by the 750 nm peak shifting from 759 nm to 754 nm after the oxidation and saturating under the larger pumping power density. The oxidizing of Si nanopillars decreased the Si quantum confining centers and it also increased the luminescent centers of the oxygen defects. The reflectance of the pure Si nanopillars was smaller than the Si bulk because of the highly rough surface. Otherwise, the Si nanopillar structure owns a low resister 22 $\text{K}\Omega$ and a good protection against the current leakage comparing to the Si bulk structure.

According to the special characteristics in electrics and in optics, the Si nanopillars can be used extensively as sensors 、 field emitter to pump phosphors 、 highly dense memory and solar cells.

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矽半導體之光激螢光光譜特性分析

目前已投稿及發表的國際期刊論文與研討會論文

研討會

1. Huang-Shen Lin, Chih-Chiang Kao, Chun-Jung Lin, Gong-Ru Lin, Hao-Chung Kuo, and Shing-Chung Wang, “Self-Assembled Ni Nanodot on SiO₂ Film—A Novel Reactive Ion Etching Mask for Si Nanopillar Formation on Si Substrate”, Photonics Europe 2006, paper, Strasburg, France, April 3-7, 2006.
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