CHAPTER 4

Failure Analysis

Based on the HBM and MM ESD robustness experimental results mentioned in chap 3, some results are analyzed and concluded but some results are not clear. In order to clarify the failure current paths and failure locations for reasonable explanation, we do some further failure analysis of these zapped ICs.

4.1 Failure Analysis Procedure

Once all experimental devices have been tested, the devices failing the electrical testing acceptance criteria were submitted for failure analysis. So the failed packages are decapitated, and then top layers including BPSG, metal, poly, and oxidation layer are removed to substrate layer with chemical processes. The failure locations are verified using optical microscopy, and scanning electron microscopy (SEM).

4.2 HBM Results and Discussion

The SEM failure pictures of dummy-gate structure transistors with drain contact to dummy-gate spacing of S = 0.4 μm, and drain contact to dummy-gate spacing of S = 1 μm after HBM ESD zapping are shown in Fig. 4.1, and Fig. 4.2. The failure pattern of dummy-gate structure transistors with drain contact to dummy-gate space of S = 1 μm is uniform, but that of dummy-gate structure transistors with drain contact to dummy-gate space of S = 0.4 μm is relatively non-uniform. So, the failure mechanism is attributed by small drain contact to dummy-gate spacing, which is matched with the data in Chap 3.

The SEM failure pictures of dummy-gate structure transistors with dummy-gate

length of L = 0.5 μm under HBM ESD zapping is shown in Fig. 4.3. Compared to dummy-gate structure transistor with dummy-gate length of L = 2.2 μm, the failure pattern of dummy-gate structure transistor with dummy-gate length of L = 0.5 μm is non-uniform and crowed in spots. The HBM ESD robustness of dummy-gate structure transistor with dummy-gate length of 2.2 μm is 2.1 kV. However, the HBM robustness of dummy-gate structure transistor with dummy-gate length of 0.5 μm is 1.2 kV.

The SEM failure pictures of transistors with FOX structure, fully-salicided structure, and salicide blocking structure under HBM stress are shown in Fig. 4.4, Fig. 4.5, and Fig. 4.6. The failure locations of NMOS transistors with FOX structure and fully-salicided structure are non-uniform but failure locations of NMOS transistor with salicide-blocking structure is relatively uniform. So, that's the reason why the ESD robustness of GGNMOS with salicide-blocking structure is higher than that of conventional fully-salicided structure and FOX structure transistors.

4.3 MM Results and Discussion

The SEM failure pictures of dummy-gate structure transistors with drain contact to dummy-gate space of S = 0.4 μm and drain contact to dummy-gate space of S = 1 μm under MM ESD stress are shown in Fig. 4.7 and Fig. 4.8, respectively. The failure patterns of dummy-gate structure transistors with drain contact to dummy-gate space of S = 1 μm under MM ESD stress is slightly more uniform than that with drain contact to dummy-gate space of S = 0.4 μm. So, MM ESD robustness levels of dummy-gate structure transistors with drain contact to dummy-gate spacing of S = 1 μm and transistors with drain contact to dummy-gate spacing of S = 0.4 μm are 500 V, 575 V, respectively.

The SEM pictures of dummy-gate structure transistors with dummy-gate length of L = 0.5 μm under MM ESD stress is shown in Fig. 4.9. The failure patterns on

SEM pictures of transistor with dummy-gate length of L = 0.5 μm is non-uniform and crowed in spots. The MM ESD robustness of dummy-gate structure transistor with dummy-gate length of 2.2 μm is 575 V. However, the MM ESD robustness of dummy-gate structure transistor with dummy-gate length of 0.5 μm is 175 V.

The SEM failure pictures of transistors with FOX structure, fully-salicided structure and salicide blocking structure under MM ESD stress are shown in Fig. 4.10, Fig. 4.11, and Fig. 4.12, respectively. The failure patterns of NMOS transistors with FOX structure and fully-salicided structure are non-uniform, and failure pattern of NMOS transistor with salicide-blocking structure is relatively uniform. So, that's why the ESD robustness of GGNMOS with salicide-blocking structure is higher than that of conventional fully-salicided structure and FOX structure transistors.

Comparing SEM failure pictures of dummy-gate structure and FOX structure transistors under MM ESD stress with those under HBM ESD stress shown in Fig. 4.2 ~ Fig. 4.12, the failure locations of transistors under MM ESD stress are more uniform than that of transistors under HBM stress. Relatively, failure locations of transistors with fully-salicided and salicide-blocking structures under MM ESD stress are similar with that of transistors under HBM stress. So, That's why MM ESD robustness of transistors with dummy-gate and FOX structures have better performance compared with that using fully-salicided structure. But HBM ESD robustness of transistors with dummy-gate and FOX structures are lower than that of transistor with fully-salicided structure. Summary of SEM failure locations of different structure of GGNMOS transistors are shown in Table 4.1.

4.4 Discussion

The SEM failure pictures of transistors with salicide-blocking structure, and fully-salicided structure under MM and HBM ESD stress show that the current paths

of transistors with fully-salicided structure are underneath the channel. Because the failure patterns of transistors with salicide blocking are crowed in top and bottom sides of fingers, failures of transistor with salicide blocking structures are caused by N+ to P-sub current path stress.

Failure patterns of devices with dummy-gate and FOX structures under MM ESD stress are relatively uniform compared with those of devices under HBM ESD stress. Fig. 4.13, and Fig. 4.14 show the waveforms of fully-salicided structure transistor and dummy-gate structure transistor under 1.1 kV HBM ESD zapping, and the peak voltages are 12.4 V and 12.3 V, respectively. Because the transformation ratio of current probe is 5 mV-to-1 mA, the corresponding currents are 2.48 A, 2.46 A, respectively. Because the resistance of HBM equivalent circuit is 1.5 kV, the turn-on resistances of all types of devices are much smaller than total resistance. So the ESD currents of different types of devices are almost the same. However, the turn-on resistance of transistors with dummy-gate and FOX structures are greater than that of fully-salicided structure transistor and salicide-blocking structure transistor. The power dissipations of those devices are proportional to turn-on resistance. That's why HBM ESD robustness of devices with dummy-gate and FOX structures are smaller than those with fully-salicided structure and silicide-blocking structure.

Fig. 4.15, and Fig. 4.16 show the discharge waveforms of fully-salicided structure transistor and dummy-gate structure transistor under 130 V MM ESD zapping. The peak voltages of fully-salicided structure transistor and dummy-gate structure transistor are 14 V and 11 V, respectively. Because the transformation ratio of current probe is 5 mV-to-1 mA, the corresponding currents are 2.8 A, 2.2 A, respectively. Because resistance of MM equivalent circuit is 0, the turn-on resistances of all types of devices are much greater than that of wires. So the ESD currents of different types devices are inverse proportional to their own turn-on resistances. The

stress voltages across devices are almost constant due to the smaller wire resistance of system. So, the power dissipation of device decreases with increasing resistance. That's why MM ESD robustness of devices with dummy-gate structure is greater than that with fully-salicided structure.

4.5 Conclusion

Failure patterns of MM ESD zapped devices with dummy-gate and FOX structure are relatively uniform compared with those of HBM ESD zapped devices. Failure pattern of devices with drain contact to dummy-gate spacing of S = 1 μm is relatively uniform comparing with those with drain contact to dummy-gate space of S = 0.4 μm. On the whole, the SEM failure pictures of ESD zapped devices are coincided with TLP, HBM and MM measured results.

Table 4.1. Summary of SEM failure locations of different structures of NMOS transistors under HBM and MM ESD zapping**.**

	HBM PS-mode	MM PS-mode
Failure locations of GGNMOS with dummy-gate structure after ESD stress (W/L = 240 μm/0.25 μm, drain contact to dummy-gate spacing = 0.4 μm, and dummy gate length = 2.2 μm)	HBM ESD robustness is 2.1 kV, Failure locations are top and bottom of drain sides.	MM ESD robustness is 500 V, failure locations are uniform in drain sides of fingers.
Failure locations of GGNMOS with dummy-gate structure after ESD stress (W/L = 240 μm/0.25 μm, drain contact to dummy-gate spacing = 1 μm, and dummy gate length = 2.2 μm)	HBM ESD robustness is 4 kV, failure locations are uniform in drain sides of fingers.	MM ESD robustness is 575 V, failure locations are uniform in drain sides of fingers.
Failure locations of GGNMOS with dummy-gate structure after ESD stress (W/L = 240 μm/0.25 μm, drain contact to dummy-gate spacing = 0.4 um, and dummy gate length = 0.5 μm)	HBM ESD robustness is 1.2 kV, failure locations are in gates and dummy gates.	MM ESD robustness is 175 V, failure locations are in gates and dummy gates.
Failure locations of GGNMOS with FOX structure after ESD stress (W/L = 240 μm/0.25 μm, drain contact to FOX spacing = 0.4 μm , FOX length = 2.2 μm)	HBM ESD robustness is 1.2 kV, failure locations are through gates.	MM ESD robustness is 175 kV, failure locations are located in some drain sides of fingers.
Failure locations of GGNMOS with fully-salicided structure after ESD stress (W/L = 240 μm/0.25 μm)	HBM ESD robustness is 5 kV, failure locations are uniform in drain and source sides of fingers.	MM ESD robustness is 225 V, failure locations are in gates.
Failure locations of GGNMOS with salicide blocking structure after ESD stress (W/L = 240 μm/0.25 μm, drain contact to salicide blocking = 0.4 μm and salicide blocking length = 2.2 μm)	HBM ESD robustness is 7.8 kV, Failure locations are top and bottom of drain sides.	MM ESD robustness is 550 V, failure locations are top and bottom of drain sides.

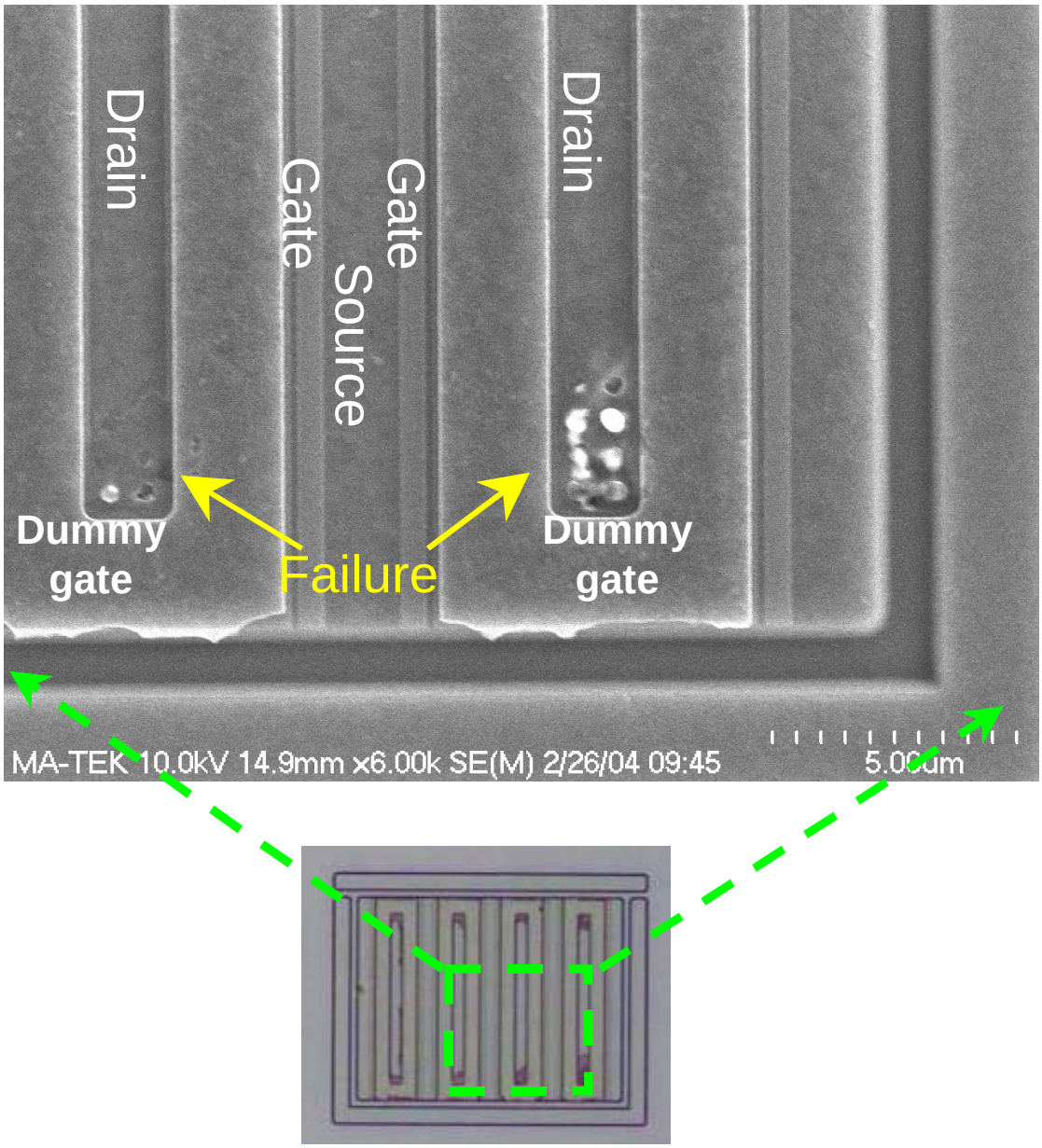

Fig. 4.1 SEM failure picture of dummy-gate structure NMOS transistor with drain contact to dummy-gate spacing of S = 0.4 μm under HBM ESD zapping. (HBM ESD robustness = 2.2 kV, W/L = 240 μm/0.25 μm, dummy-gate length = 2.2 μm)

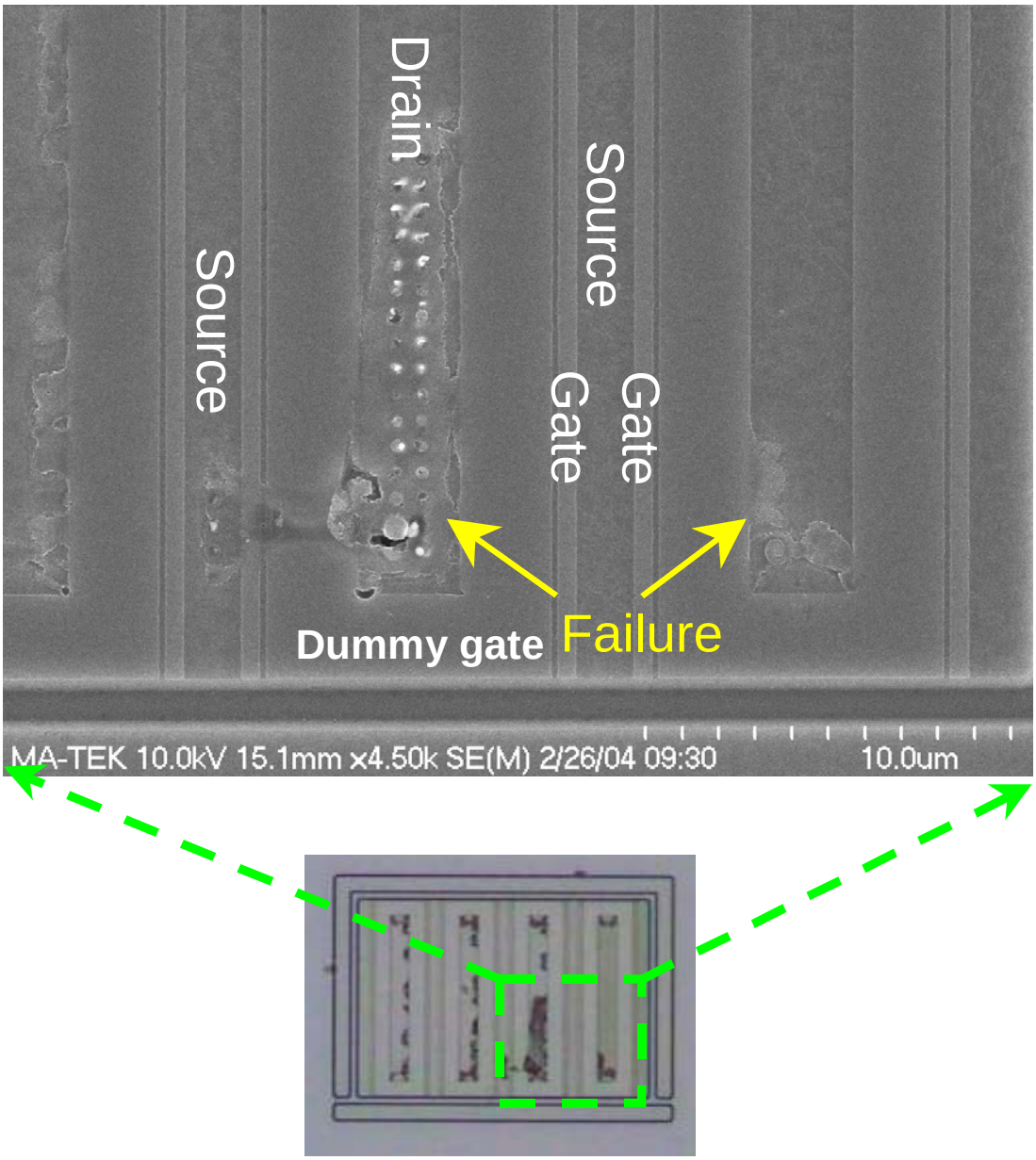

Fig. 4.2 SEM failure picture of dummy-gate structure NMOS transistor with drain contact to dummy-gate spacing of S = 1 μm under HBM ESD zapping. (HBM ESD robustness = 4 kV, W/L = 240 μm/0.25 μm, dummy-gate length = 2.2 μm)

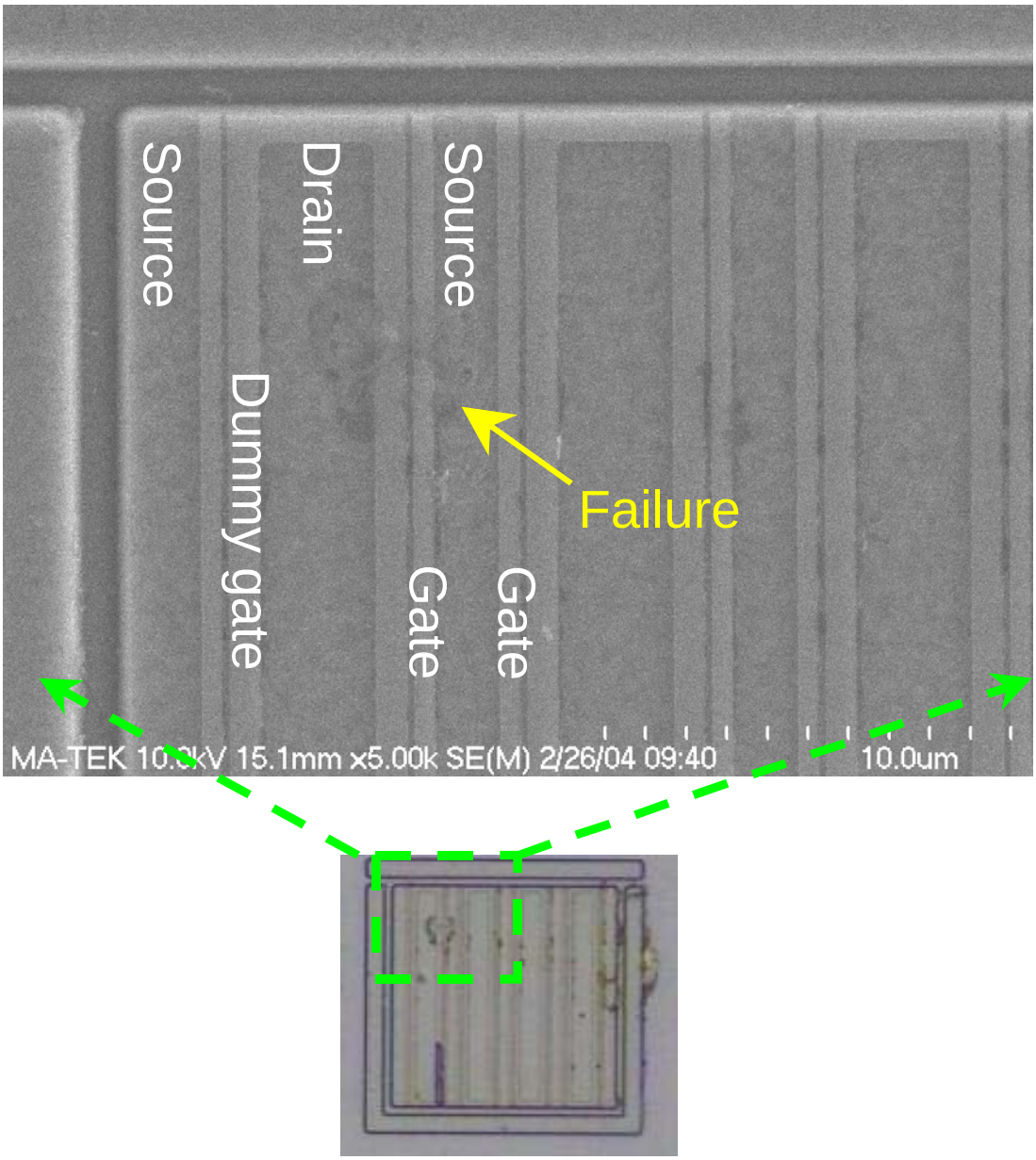

Fig. 4.3 SEM failure picture of dummy-gate structure NMOS transistor under HBM ESD zapping. (HBM ESD robustness = 1.2 kV, W/L = 240 μm/0.25 μm, dummy-gate length = 0.5 μm)

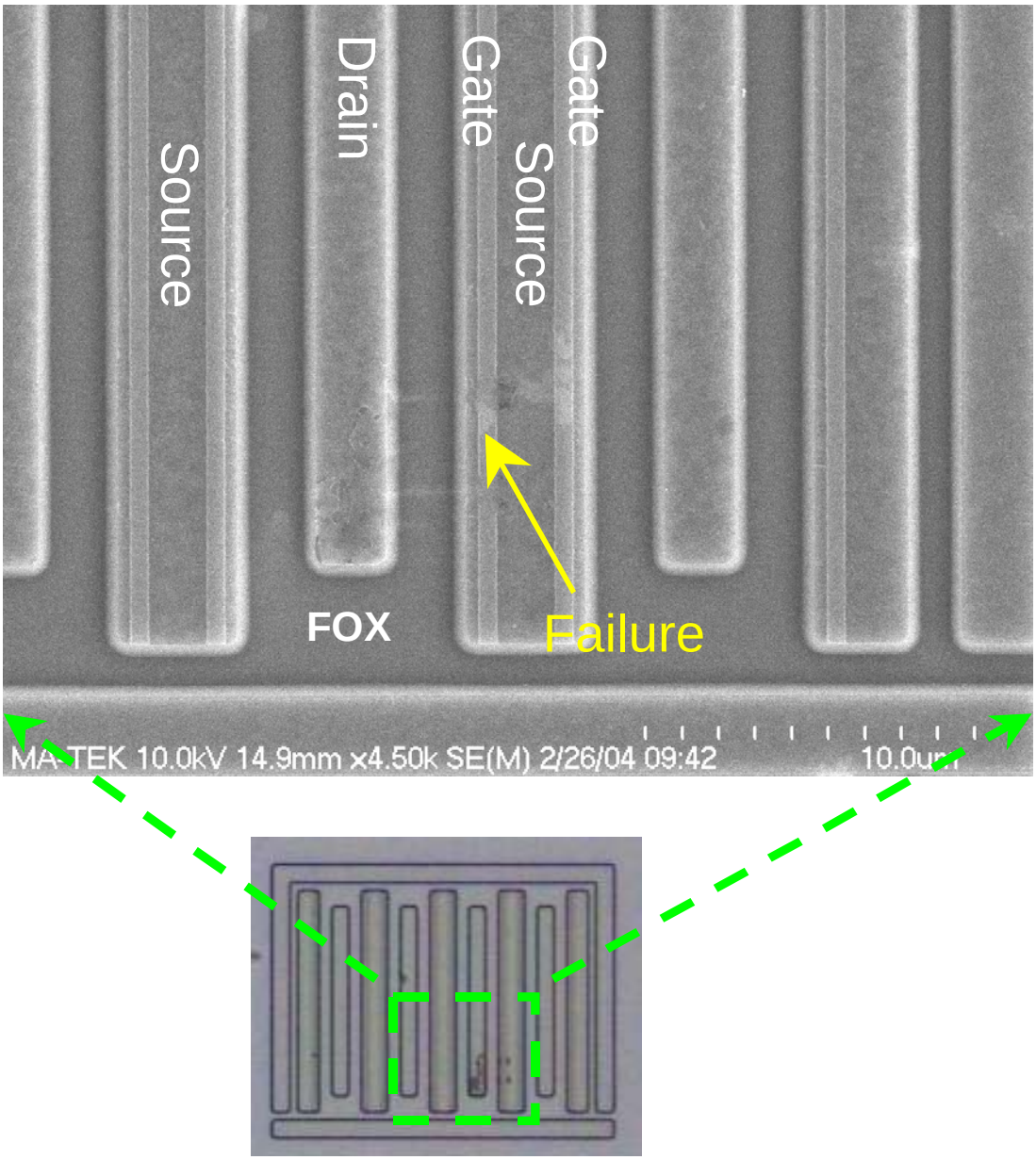

Fig. 4.4 SEM failure picture of FOX structure NMOS transistor under HBM ESD zapping. (HBM ESD robustness = 1.2 kV, W/L = 240 μm/0.25 μm)

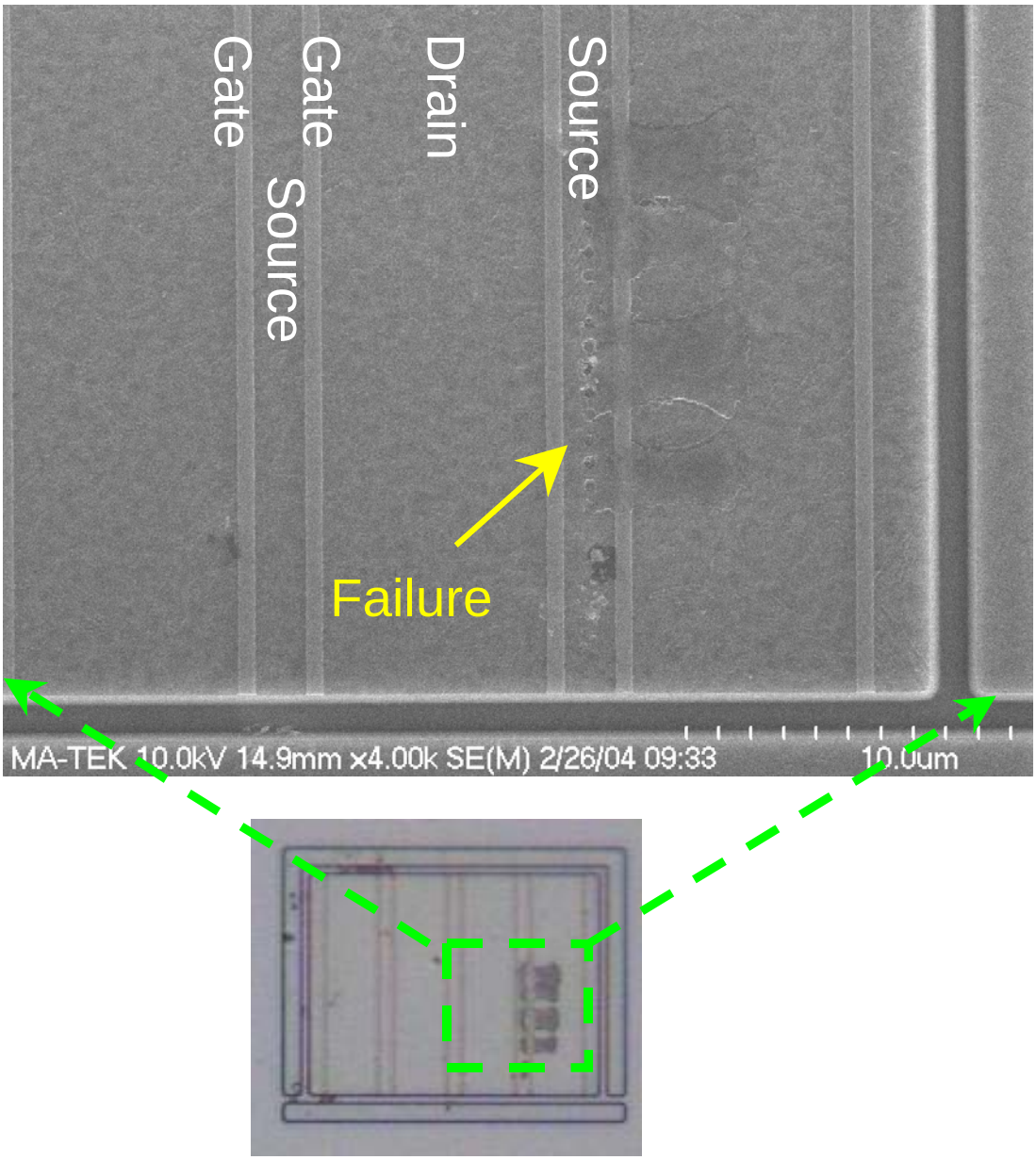

Fig. 4.5 SEM failure picture of fully-salicided structure NMOS transistor under HBM ESD zapping. (HBM ESD robustness = 5 kV, W/L = 240 μm/0.25 μm)

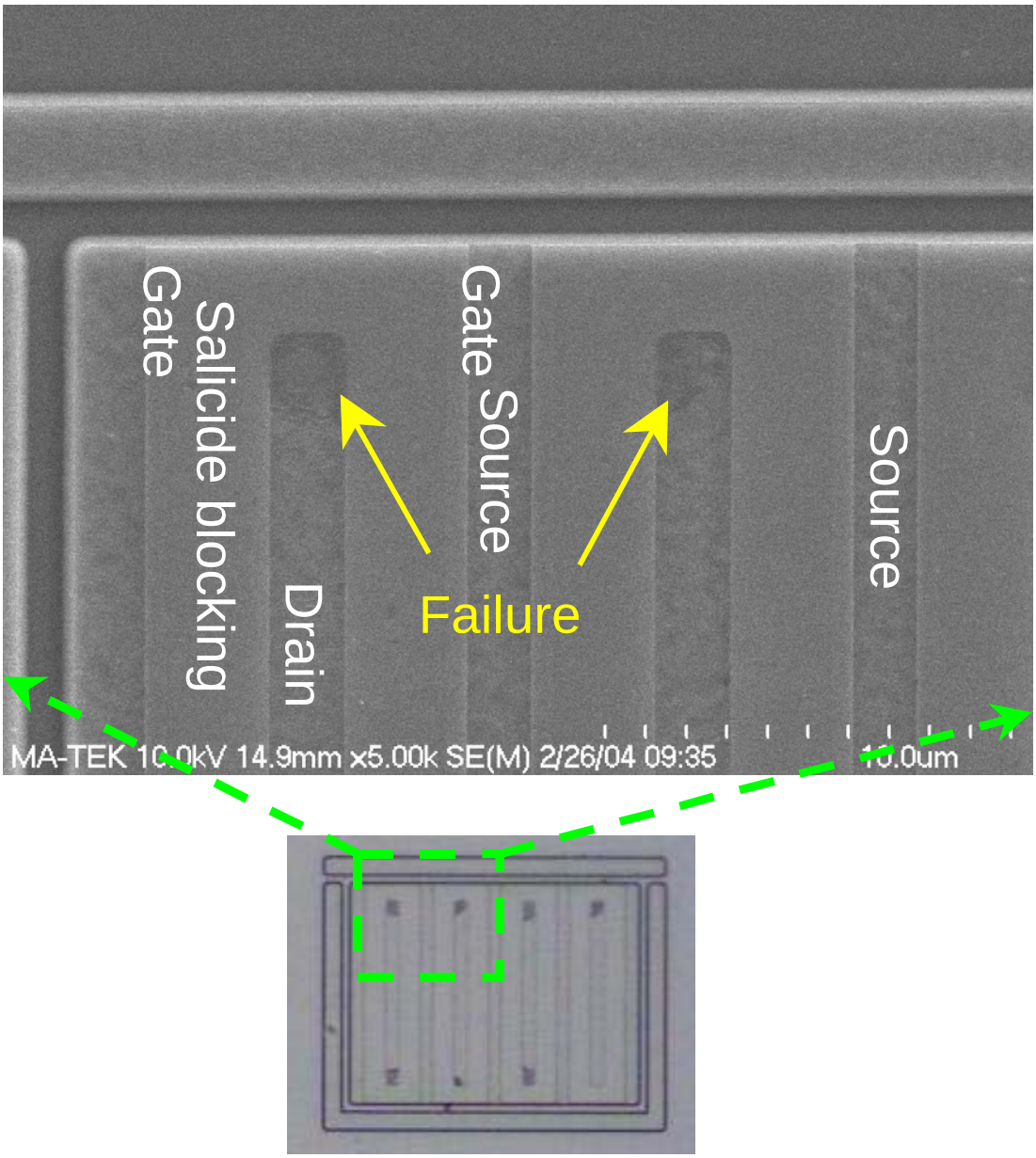

Fig. 4.6 SEM failure picture of salicide-blocking structure NMOS transistor under HBM ESD zapping. (HBM ESD robustness = 7.8 kV, W/L = 240 μm/0.25 μm)

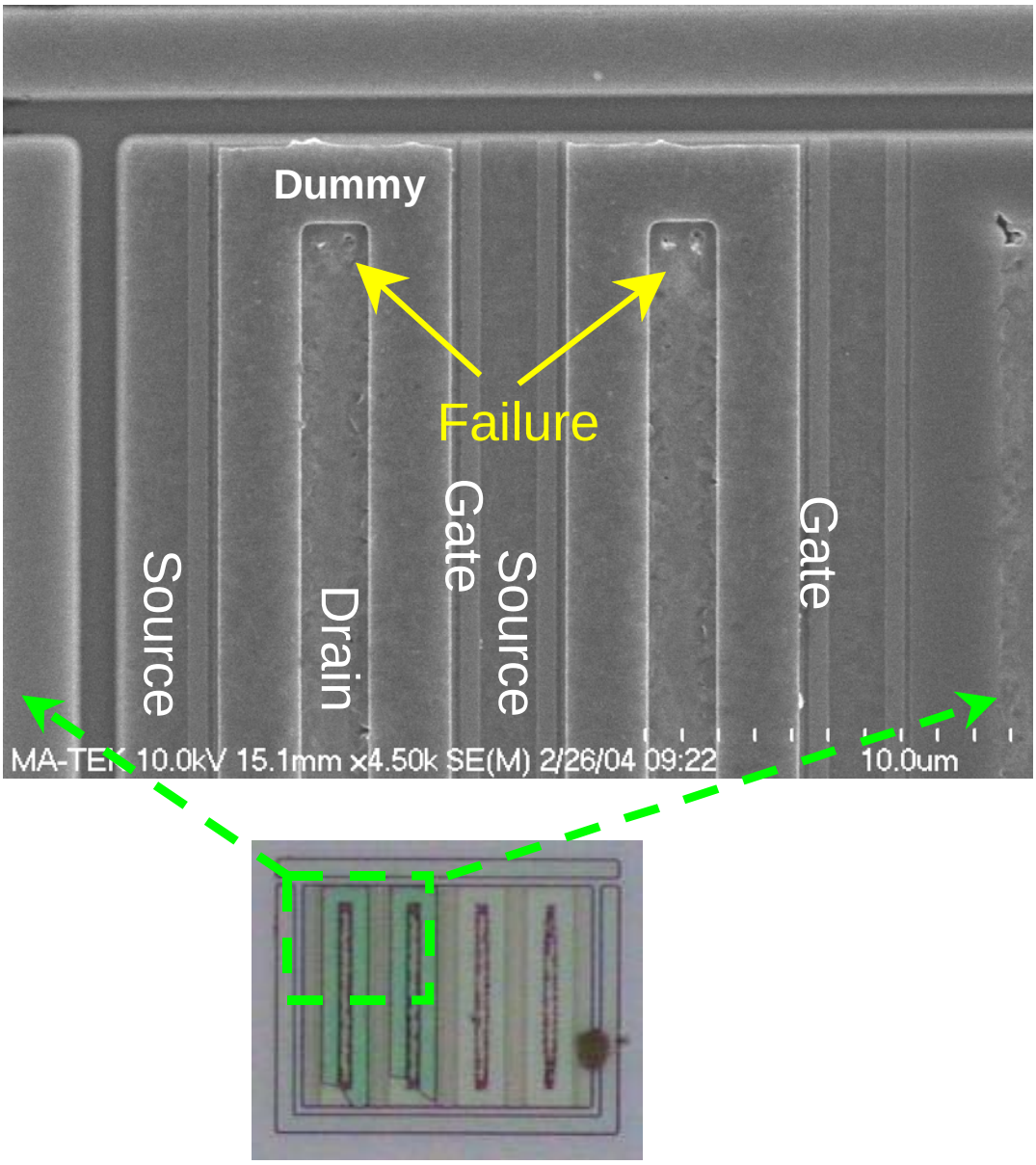

Fig. 4.7 SEM failure picture of dummy-gate transistor with drain contact to salicide block spacing of S = 0.4 μm under MM ESD zapping. (MM ESD robustness = 500 V, W/L = 240 μm/0.25 μm, dummy-gate length = 2.2 μm)

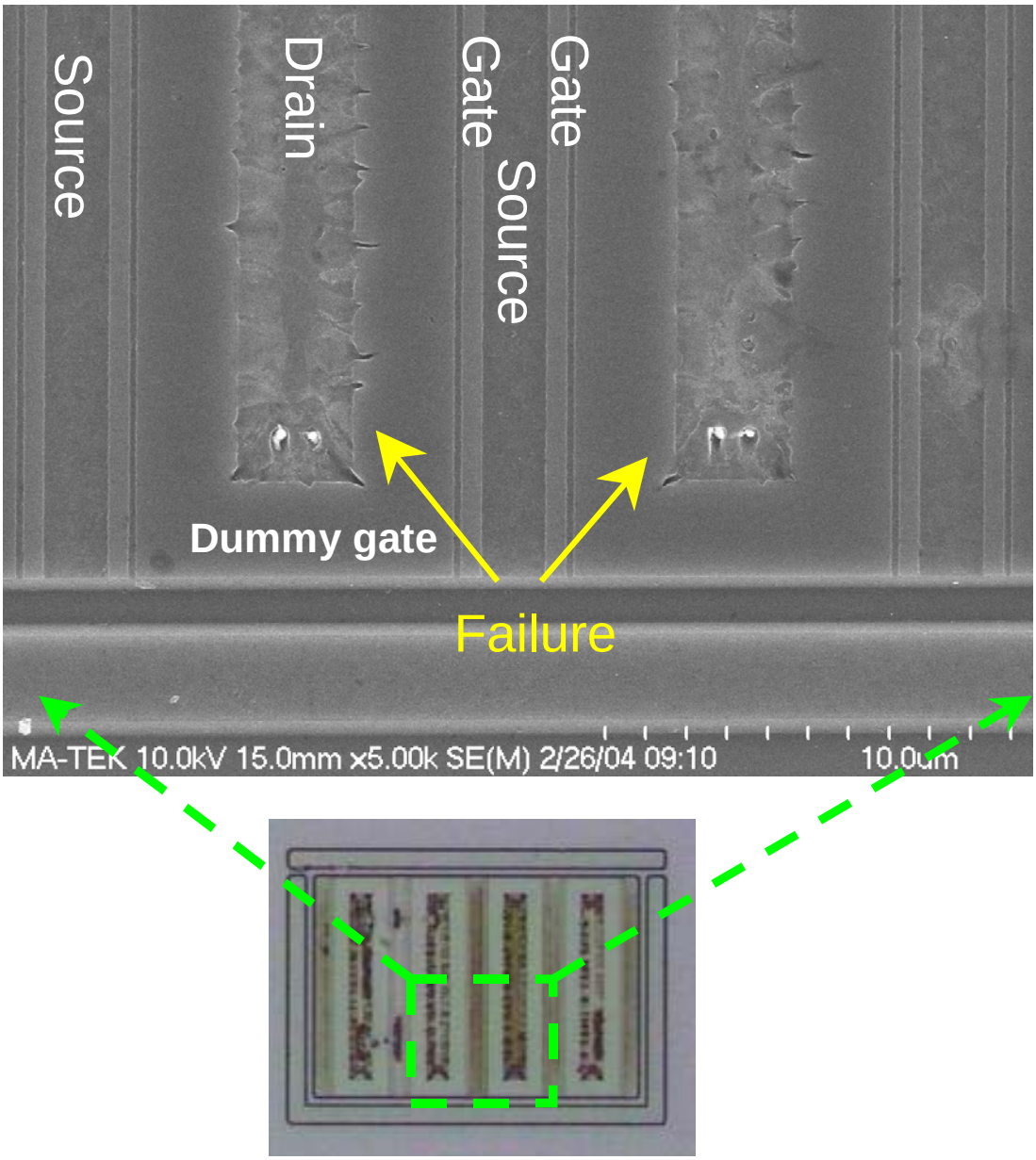

Fig. 4.8 SEM failure picture of dummy-gate transistor with drain contact to dummy-gate spacing of S = 1 μm under MM ESD zapping. (MM ESD robustness = 575V, W/L = 240 μm/0.25 μm, dummy-gate length = 2.2 μm)