國 立 交 通 大 學

電機學院微電子奈米科技產業研發碩士班

碩 士 論 文

具有氮化矽覆蓋層之形變 N 型金氧半場效電晶體之性能及可靠度

Performance and Reliability of Strained NMOSFETs with SiN Capping Layer

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摘要

在本論文中，我們主要探討在 N 型金氧半場效電晶體中，利用電漿化學氣相沈積系統(PECVD)沈積不同厚度的氮化矽覆蓋層來分別對元件通道產生應力時，元件的各項特性。我們發現較厚的氮化矽覆蓋層可以對在下方的元件通道產生較高的舒張應力，並且造成了更高的元件載子遷移率。因此，沈積較厚的氮化矽覆蓋層的元件會擁有較好的元件性能。然而，提高的元件載子遷移率和氮化矽沈積過程會使得元件的熱載子退化效應變得嚴重，而隨著沈積氮化矽覆蓋層的厚度越厚，熱載子退化效應也越嚴重。我們也探討了傅立葉轉換紅外光儀的分析結果。在元件中發現有額外的矽-氫鍵結，代表了電漿化學氣相沈積系統沈積的氮化矽覆蓋層的確含有大量的氫。

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Abstract

In this thesis, we investigated the characteristics of strained-channel NMOSFETs with different thickness of silicon nitride (SiN) capping layer deposited by plasma enhanced chemical vapor deposition (PECVD) system. We found that thicker SiN capping would result in higher tensile stress in the underlying channel and leading to a higher mobility. Therefore, higher performance enhancement was observed for devices with thicker SiN capping. However, the increased mobility and the SiN deposition process would aggravate the hot carrier reliability, resulting in the severest hot carrier degradation for the samples with the thickest SiN capping. The analysis of Fourier transform infrared spectrometer (FTIR) was also investigated. The extra Si-H bonds were observed, indicating that PECVD SiN indeed has abundant hydrogen species.

誌 謝

在短短的研究所求學過程中，能夠一路順順利利的完成實驗，並且完成這篇論文，首先要感謝的，是我的指導教授黃調元教授和林鴻志教授。兩位教授有著豐富的經驗以及淵博的知識，並且悉心的教導使我能夠在研究上能有成果，並且獲益匪淺。在此我要向黃教授和林教授致上最誠摯的敬意及謝意。

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Chapter 1
Introduction

1-1 General Background

1-1.1 Strained Channel Technology

In the past few decades, semiconductor fabrication technology has been evolving rapidly with technology generation progressing from micro to nano regime. Such progress provides enough momentum to retain the well-known "Moore's Law" [1]. However, the tasks needed to overcome the challenges for further shrinkage of devices increase and become much more difficult.

In order to increase the operation speed and density of devices, and to decrease the device operation voltage, shrinkage of gate dielectric oxide as well as channel length of the devices are essential [2-4]. However, short channel effects, gate leakage current and subthreshold swing worsen with the shrinkage process [5]. All of the above issues surely needed to be addressed carefully.

As a number of fundamental physics constraints limit the expected performance improvement by scaling down of device size. One of those is the carrier mobility: it seems more and more difficult to maintain good mobility in scaled devices because of heavier substrate doping. In this regard, strain channel engineering is a possible solution and has actually been implemented in manufacturing for overcoming the difficulties. It has been demonstrated that strained-Si technology provides an enhanced mobility and thus drive current improvement of MOSFETs by altering the energy band structures of the surface channel [6-8].

Introduction of bi-axial [9] and uni-axial [10-12] channel stress are the two major ways adopted in strained channel engineering. Bi-axial tensile strained channels are

formed by growing a Si channel layer on a relaxed SiGe substrate [9]. Bi-axial tensile strain improves the drive current of both NMOSFETs and PMOSFETs because the mobility enhancement of electrons and holes is available simultaneously when the strain level is sufficiently high. It is thus well suited to applications of CMOSFETs. Since Si layer is growing epitaxially on a relaxed SiGe buffer layer to form a strained-Si layer, it is noticed that the thickness of the upper Si layer must be thinner than a critical thickness that depends on the Ge content of the underlying relaxed SiGe substrate to avoid the generation of dislocations [13]. Moreover, some yield issues of technologies such as surface roughness [14], diffusion of n-type dopants [15], increasing parasitical resistance owing to agglomeration of SiGe, Ge out diffusion [16], self-heating [17], and expensive wafer cost, hinder this technology from being used in real VLSI fabrication.

Uni-axial strained channels are induced by forming certain strain boosters to uni-axially promote the stress [10-12]. Examples include contact-etch-stop-layer (CESL) [18,19], shallow trench isolation (STI) [20,21], source/drain material [22], silicidation [23], packing process [24], and so on. Generally this kind of approach is free from the aforementioned concerns for bi-axial counterpart, thus much more suitable for practical manufacturing. When a uni-axial stress is introduced in the device's channel, behavior of carrier transport depends on several factors including the channel length and the channel orientation [25]. Different behaviors of electrons and holes under the complex three-dimensional strain result in the different response on the characteristics of NMOS and PMOS devices. Each direction of the devices has its own preferred stain type (e.g., compressive or tensile), as shown in Fig.1.1. For example, along the longitudinal direction (i.e., the channel- or x-direction in Fig.1.1), tensile and compressive strain are preferred for NMOS and PMOS, respectively, to enhance performance. Note that a SiN capping layer provides both tensile and compressive

stresses, depending on the deposition conditions and the tools (i.e., LPCVD or PECVD).

The formula of carrier mobility is given by $\mu=\frac{q\tau}{m^*}$, where $1/\tau$ is the overall scattering rate and m^* is the conductivity effective mass. According to the formula, strain applied on the device enhances the mobility by reducing the conductivity effective mass and/or the scattering rate. Both of them are important, but only the scattering rate is a significant factor to enhance hole mobility for the bi-axial strain case [26]. This will be elaborated below.

The conduction band of unstrained Si is composed of six degenerate valleys (Δ6) with the same energy (as shown in Fig.1.2). For bi-axial tensile strain, because of the lattice mismatch with the relaxed SiGe substrate, the strain splits the six-fold degenerate conduction band into a two-fold (Δ2) out-of plane valley and a four-fold (Δ4) in-plane degenerate valley. Δ2 band energy is lower than the Δ4 band energy, and the energy splitting ΔEs between the Δ2 and Δ4 bands is proportional to the Ge content, x, of the relaxed buffer with the relation: ΔEs = 0.67x (eV), which determines the electron mobility enhancement in strained Si devices. Splitting of the sub-bands in an MOS inversion layer is schematically shown in Fig.1.3 [27]. As shown in the figure, the inversion electrons will occupy the Δ2 ground sub-band preferentially owing to its much lower energy. Since Δ2 band has a smaller effective mass than Δ4 band, Δ2 band can be considered as a high electron mobility band as compared with Δ4 band. Thus the mobility enhancement will be related to the relative electron population of Δ2 and Δ4 bands in the strained Si as compared with the bulk Si devices. In addition, the splitting of conduction band can suppress inter-valley phonon scattering. Reduction of the electron scattering rate ($1/\tau$) also enhances the electron mobility.

The valence band structure of Si is more complex than the conduction band

structure. Holes occupy the two upside valence bands in unstrained Si devices. These two bands are the heavy- and light-hole bands, which degenerate at gamma-point (k=0). Under bi-axial tensile strain, the valence bands will split at gamma-point, as shown in Fig.1.4. The light-hole (with smaller effective mass) band lies upper than the heavy-hole band in out-of plane band diagram. Upper band represents lower energy for holes, thus the holes prefer to assemble in light-hole band. The strain removes the degeneracy and reduces the band-to-band coupling, and the effective mass is roughly constant for both bands. However, it should be noted that the effective mass is heavier than unstrained case. The strain thus reduces the scattering rate by altering the light- and heavy-hole band density of states and reducing inter band optical phonon scattering through light-to-heavy hole band splitting, thus increasing the mobility. Under bi-axial tensile strain condition, since there is no mass reduction, only the reduction of the scattering rate can enhance the mobility. For this purpose, an estimation of 25-30% Ge contents is necessary to induce more than 1G Pa stress. Such stress level leads to a splitting energy greater than 60meV of optical phonon energy in Si, and the inter-valley phonon scattering may be greatly suppressed under low electric field.

The variation of the scattering rate and effective mass which depends on the valance band structure of strained Si are taken to quantify and compare the hole mobility enhancement due to uni-axial and bi-axial stress. From the work of C. W. Leitz et al. [28], the uni-axially compressive strained MOSFETs may have lighter in-plane effective mass from the analysis of full-band Monte Carlo simulation, thus the hole mobility is enhanced.

When the factor of high vertical electric field is considered rather than the low electric field we've mentioned above, it is found that the mobility enhancement of uni-axial strain is higher than bi-axial strain. Hole mobility between bi-axial tensile

and uni-axial compressive strain have different behaviors at high vertical field. The splitting of light and heavy hole band caused by bi-axial tensile stress would be ineffective at high electric field owing to the strong surface confinement. Contrary to the situation, in the uni-axial strain case hole mobility enhancement is not influenced by surface confinement, thus it becomes a major advantage of the uni-axial strain over the bi-axial strain for PMOSFETs operating at high electric field. The magnitude of splitting level under the influence of surface confinement depends on the relative magnitude of the strain altering light- and heavy-hole out-of-plane effective mass. It is reported that the out-of-plane effective mass of light hole is heavier than that of heavy hole for uni-axial strain, and causes the increase of the light and heavy hole band splitting[29] . On the contrary, the case of bi-axial strain causes the opposite results.

For strained Si NMOSFETs, the strain will induce additional valence band offset. The decrease in threshold voltage resulting from shallower channel depletion is due to the fact that Fermi level moves closer to the conduction band caused by the negative valence band offset. The bi-axial tensile strain induces more band-gap narrowing than uni-axial tensile strain, thus the threshold voltage shift caused by bi-axial tensile strain is larger than that by uni-axial tensile strain [30].

1-1.2 Hot Carrier Effects

While the MOSFETs' dimension continues shrinking with the evolvement of the VLSI technology, one of the critical reliability issues is the hot carrier effect. If the device dimension is reduced while the supply voltage remains unchanged, the lateral electrical field in the channel of the device will increase. The inversion layer carriers will be accelerated more significantly, resulting in the generation of hot carriers. These

energetic hot carriers will cause undesirable damage in the device when they release energy at the Si/SiO_2 interface and/or in the oxide. The mechanism mentioned above is called hot carrier effect, which causes a time-dependent degradation of various MOSFET characteristics, for example, threshold voltage shift (ΔV_{th}), drain current degradation (ΔI_{DS}), transconductance degradation (ΔG_m), and worsened subthreshold swing.

The location of damaged region by the hot carrier stress is near the drain of the device. The range of the damaged region is dependent on the device geometry, the duration and conditions of stress, and spatial distribution of gate oxide and interfacial defects. The lifetime of the device is impacted by the spatial non-uniformity of the damage. It has been reported that the length of damaged region is independent of the channel length. Thus the damaged region becomes a larger fraction of the channel length as the device is shrunk. The performance degradation of the device is aggravated more as the channel length becomes shorter under the same stress condition.

1-2 Motivation

In our group's previous studies [38], we have characterized NMOS devices with SiN capping deposited by LPCVD system. Although the tensile strain indeed improves the device performance, the reliability degradation remains as a serious issue. Moreover, the thermal budget associated with the LPCVD SiN deposition causes the undesirable poly depletion effect. Therefore, in this work, we employed a PECVD system to deposit tensile SiN capping films at low temperature of 300°C. SiN of

various thicknesses was capped over the gate of NMOSFETs in order to investigate their impacts on the performance and hot carrier reliability.

1-3 Organization of This Thesis

In addition to this chapter, this thesis is divided into the following chapters.

In Chapter 2, we briefly describe the process flow for fabricating the NMOS devices with SiN capping layer. Furthermore, we present the characterization method, measurement setups, and the stress conditions.

In Chapter 3, we present and compare characteristics of devices with and without the SiN capping layer. Results of hot carrier reliability characterization of the strained devices are also presented.

Finally, in Chapter 4, we summarize the important conclusions derived from the work.

Chapter 2
Device Fabrication and Measurement Setup

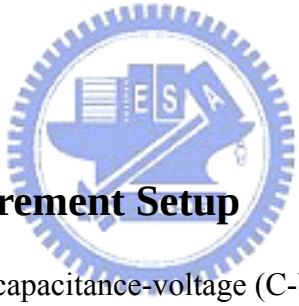
2-1 Device Fabrication and Process Flow

The NMOSFETs were fabricated on 6-inch p-type (100) Si wafers with resistivity of 15~25Ω-cm. The p-type well was formed first by BF_2^+ implantation at 100 keV and 1×10^{-13} cm^{-2}. Next, a standard local oxidation of silicon (LOCOS) process with channel stop implant (by BF_2^+ implantation at 120 keV and 4×10^{-13} cm^{-2}) was used for device isolation. Threshold voltage adjustment and anti-punch through implantation were done by implanting 40 keV BF_2^+ and 35 keV B^+, respectively. After the growth of 3nm-thick thermal gate oxide, a 150nm amorphous Si layer was deposited by low-pressure chemical vapor deposition (LPCVD), followed by gate etch process to pattern the film. The Source/drain (S/D) extension regions were then formed by As^+ implantation at 10 keV and 5×10^{-14} cm^{-2}. After a 150nm oxide spacer formation by HDPCVD, S/D regions were formed by P^+ implantation at 15 keV and 5×10^{-15} cm^{-2}. Afterwards, the substrate electrode patterning was performed through lithography and etching processes, and the substrate junction was formed by BF_2^+ implantation at 40 keV and 5×10^{-15} cm^{-2}.

Next, most samples were capped with a SiN capping layer (simulating the contact-etch-stop-layer, CESL, in practical manufacturing) with different thickness (20nm, 100nm and 300nm) by using a plasma enhanced chemical vapor deposition (PECVD) system. The SiN deposition was performed at 300 ℃ with SiH_4, N_2 ,and NH_3 as the reaction precursors. Then an oxide layer with different thickness (280nm, 200nm and 0nm) was deposited for passivation by HDPCVD system. Some wafers were

deliberately skipped of the SiN deposition step to serve as the controls. The thickness of the oxide layer was adjusted according to the thickness of the SiN capping layer in such a way that all wafers end up with the same thickness of the final passivation layer.

Rapid thermal anneal (RTA) was then carried out in a nitrogen ambient at 900°C for 30 sec to activate dopants in the gate, S/D, and substrate regions. After contact hole etching, normal metallization scheme was carried out. The final step was a forming gas anneal performed at 400°C for 30 min to mend dangling bonds and reduce interface state density at the gate oxide/Si interface. Cross-sectional view of the fabricated device is showed in Fig.2.1. NMOSFETs with three different capping layers have been fabricated as summarized in Table 2.1.



2-2 Electrical Measurement Setup

Current-voltage (I-V) and capacitance-voltage (C-V) characteristics were evaluated by an HP4156A precision semiconductor parameter analyzer and an HP4284 LCR meter, respectively. Temperature-regulated hot-chucks were used to control the temperature at a fixed temperature of 25°C.

2-3 Charge Pumping Measurement Setup

2-3.1 Basic Theory

The charge pumping method was first proposed by Brugler and Jespers [32], and then further developed by Heremans [33]. This technique has been widely used to

characterize the interface state density in MOSFETs. It is based on the recombination process at the Si/SiO_2 interface involving the surface traps. When the gate oxide is thick (e.g., > 2nm), the measurement allows the exclusion of gate leakage contribution to the calculated interface state densities presented in thin gate oxides. Typical measurement setup grounds the substrate, and biases the drain and source to a small fixed reversed bias. The measurement proceeds by recording the substrate current while a voltage pulse train is applied to the gate. The pulse train is with fixed amplitude (low and high levels are also fixed), rise time, fall time, frequency, and duty cycle ratio. The AC voltage levels to the gate of the test device can modulate the surface potential of the channel from a low accumulation level to a high inversion level. When the base (low) level is lower than the flat-band voltage while the top level of the pulse is higher than the threshold voltage, the maximum charge pumping current occurs. This condition means that when the device is pulsed from inversion toward accumulation, the net amount of charges will be transferred from the drain and source to the substrate via the fast interface traps. The repetitive recombination at interface traps leads to the charge pumping current. As a result, the recombination current extracted from the substrate is called the charge pumping (CP) current [34]. On the contrary, when the base level is higher than the threshold voltage or the top level of the pulse is lower than the flat-band voltage, the fast interface traps are permanently filled with electrons in the inversion level or holes in the accumulation level for NMOSFETs. Therefore, there is no charge pumping current detected because of the nonexistence of recombination current.

The charge pumping current is given by:

$$I_{cp} = qA_G fN_{it}$$

where A_G is the gate area (W*L) of an MOSFET. The interface trap density (N_{it}) can be calculated from this equation.

2-3.2 Basic Measurement Setup

There are three conventional types of the voltage pulse train to the gate electrode, as depicted in Fig.2.2, which are named as followed: (a) fixed amplitude sweep, (b) fixed base sweep, and (c) fixed peak sweep.

In this thesis, “fixed amplitude sweep” mode was used to calculate interface trap density, and “fixed base sweep” mode was used to analyze the lateral distribution of interface trap, respectively. The basic setup of charge pumping measurement is shown in Fig. 2.3. The drain and source are biased at 50mV. The substrate electrodes are connected to ground. Square-wave waveforms (f = 1MHz) provided by HP8110A with fixed amplitude of 1.5V are applied to the gate of the NMOSFET, while the base voltage is varied to change the surface condition from inversion to accumulation. In our measurement setup, V_{base} is varied from -2V to -0.2V in step of 0.05V. A parameter analyzer HP4156A is used to measure the charge pumping current (I_{CP}).

2-4 Hot Carrier Reliability Measurement Setup

In the reliability measurements, we first measured I_{sub}-V_G characteristics with drain biased at a specific voltage to find V_G at maximum absolute value of I_{sub}. Then the device was stressed with drain voltage set at a highly positive voltage, and the gate terminal biased at the voltage V_G where maximum I_{sub} happened to accelerate the degradation.

To monitor the degradation caused by the hot electrons, the I_D-V_G characteristics at V_{DS} = 0.05 V (linear region) and charge pumping current were measured before and after the stress. The degradations in terms of threshold voltage shift (ΔV_{th}), generation

of interface trap density (ΔN_{it}), and transconductance degradation (ΔG_m), were observed and recorded in the accelerated stress measurements.

2-5 Extraction Procedure of Lateral Distribution of N_{it}

The lateral distribution of interface state after hot carrier stress of all splits was also discussed in this work. This method was built on [36] and the measurement setup is shown in Fig. 2.4. The experimental procedures of this method are described below.

(1) Measure Icp-V_h curve on a virgin MOSFET from the drain junction (with the source junction floating), and from which the relationship between V_h and $V_{th}(x)$ near the junction of interest is established [37].

(2) Record Icp-V_h curve after hot carrier injection.

(3) The hot-carrier-induced interface state distribution, $N_{it}(x)$, is obtained from the difference of Icp-V_h curves before and after the stress.

Chapter 3
Results and Discussion

3-1 Electrical Characteristics of Locally Strained NMOSFETs

Measurements of the stress level induced by the capping dielectrics were performed on Si wafers capped with a blanket SiN/SiO_2 stacked layer with a total thickness of 3000Å. The results are shown in Fig.3.1. It can be seen that the stress level is compressive (negative) in nature as the capping layer is pure oxide. The adding of a SiN tends to shift the stress level to a more positive value, and becomes more tensile with increasing SiN capping layer thickness. Figure 3.2 shows the I_D-V_D characteristics of NMOSFETs for all splits with channel length of 0.5μm. It can be seen that the SiN-capped splits all show drain current enhancement as compared with the control (oxide-capping) split, and the enhancement increases with increasing SiN thickness. The transconductance of the devices depict similar enhancement trends, as shown in Fig. 3.3, extracted from the transfer characteristics shown in Fig. 3.4. It is observed that the subthreshold slope of all devices does not seem to be influenced by the thickness of SiN capping layers and SiO_2 layer, as evidenced by the extracted subthreshold slope of the devices shown in Fig. 3.5.

Figure 3.6 shows the percentage increase of Gm for all SiN-capping samples compared with the SiO_2-3kÅ samples as a function of channel length. We can see that Gm enhancement ratio reaches about 5%, 19%, and 29% at a channel length of 0.4μm for devices with SiN thickness of 200Å, 1000Å, and 3000Å, respectively. It can also be seen that when the channel length decreases, the strain effect enhances. This is reasonable since the strain is distributed locally near the source and drain, and becomes

more pronounced in the channel as the channel length is reduced. The Gm ratio thus increases with decreasing channel length, a unique feature of uniaxial strain by SiN capping.

Capacitance-voltage characteristics for all splits are shown in Fig. 3.7(a). These C-V curves coincide together, implying that oxide thickness difference among these samples is negligible, indicating that the aforementioned results are not caused by the oxide thickness difference. The poly depletion effect is not observed in the SiN-capped devices. From our group's previous studies [38], when tensile stress was exerted with an LPCVD SiN capping, poly depletion effect was observed clearly (as shown in Fig. 3.7(b)). Note that, as referring to Fig. 3.8, the temperature of the LPCVD process is 780℃ which had a much lower solid solubility in thermal equilibrium than the high temperature of 950℃ used in RTA process to activate the dopants in the poly. As a result the poly depletion effect occurred. Since the temperature of PECVD process in this study was only 300℃ which was so low that the associated thermal budget was too small to affect the activated carrier concentration, therefore the poly depletion effect is negligible, as shown in Fig.3.7(a).

Threshold voltage (V_{th}) roll-off characteristics for all splits of devices are shown in Fig. 3.9. The results are obtained at V_{DS} = 0.05V. With increasing SiN capping layer thickness, threshold voltage shift (ΔV_{th}) is getting larger. This is mainly ascribed to the band-gap narrowing effect caused by channel stress.

3-2 Hot-carrier Degradation of Locally Strained NMOSFETs

Although the device performance is improved by applying channel strain induced

by the SiN capping layer, however, these devices could encounter serious hot carrier degradation. A hot carrier with sufficient energy could create more charge carriers through impact ionization. For NMOSFETs, holes generated by impact ionization are collected by the substrate. Figure 3.10 shows the substrate current (I_{sub}) versus gate voltage for all splits of devices at V_{DS} = 4.5 V. It can be seen clearly that the substrate current of SiN-capped splits is larger than the control. Such result is related to the channel strain closely. Generation of channel hot electrons and the associated impact ionization process are affected by the channel strain caused by SiN capping layers. The band-gap narrowing and carrier mobility enhancement owing to the channel strain are the two major contributors to the enhancement of the ionization rate. Therefore, as the SiN capping layer becomes thicker, larger substrate current is observed owing to the increasing mobility with increasing strain.

Based on the I_{sub} measurements mentioned above, all splits of samples were stressed at V_{DS} = 4.5V and V_G of maximum I_{sub}. The channel length and width of the test devices were 0.5μm and 10μm, respectively. The I_D-V_G characteristics at V_{DS} = 0.05 V and charge pumping current were measured before and after the stress to observe the degradation caused by hot carriers. As shown in Fig. 3.11, the degradation of I_D and Gm aggravate with increasing thickness of SiN capping layers. The threshold voltage shift (ΔV_{th}) and generated interface state density (ΔN_{it}) as a function of stress time for all splits of devices are shown in Fig. 3.12 and Fig. 3.13, respectively. The device with the thickest SiN capping layer (SiN-3kÅ) depicts the most aggravated degradation in term of the largest ΔV_{th} and ΔN_{it}. The increased carrier mobility and the accompanying band-gap narrowing effect in the strained channel devices are two of the primary factors for aggravated hot carrier degradation. In addition, the SiN deposition process itself may result in the enhanced damage effect. Since the PECVD SiN deposition employs H-containing precursors, e.g., SiH_4 and NH_3, voluminous H contained in the deposited

films is expected. This is confirmed by the FTIR measurements and the results are shown in Fig. 3.14(a), together with that of LPCVD SiN films in Fig. 3.14(b) for comparison purpose. Obviously, the PECVD one shows much more significant H-related bonding signals, implying a higher H content. This is reasonable, since less dissociation processes of the precursor gases occur in the low temperature deposition. The H-related species may diffuse to the oxide/channel interface and form Si-H bonds wherein. During the stressing, extra interface states can be generated during the breaking of Si-H bonds by the hot electrons, and cause the performance degradation. The thicker SiN layer needs longer deposition time, and therefore more hydrogen species may diffuse into the channel region. Figures 3.15 and 3.16 show the charge pumping current for all splits of samples before and after 5000-seconds hot carrier stressing. Figure 3.17 shows the increase in charge pumping current after stressing. As mentioned above, devices with thicker SiN capping layer may contain a larger amount of Si-H bonds at the channel/oxide interface, and more interface states are generated during hot-carrier stressing, resulting in a larger increase in charge pumping current.

3-3 Analysis of the Distribution of Interface Trap Density

The lateral distribution of interface trap states was also extracted. The local V_{th} and V_{fb} across the MOSFETs are not uniform due to the lateral doping variation, as shown in Fig. 3.18. Schematics of the measurements could be found in Sec. 2-3.2. Note that the source is floating during the measurements. In order to detect the interface states, the pulse train during the measurements must undergo alternate accumulation and inversion cycles. As shown in Fig. 3.19, before the high voltage (V_h) exceeds the

minimum V_{th} under the gate, there should be no Icp. When V_h starts to exceed V_{th} at certain channel locations under the gate, Icp begins to grow. Before V_h reaches the maximum local V_{th} in the channel, the interface states residing near the drain side contribute to Icp, owing to the fact that the trapped electrons near the source cannot not flow easily to the drain side.

We use the control sample as an example. If we assume that interface state density is spatially uniform along the channel, which can be written as

$$I_{cp,\max} = q\, f\, N_{it}\, W\, L, \tag{3-1}$$

where f is the gate pulse frequency, W the channel width, and L the channel length. Since V_{th} is not uniform, so when V_h reaches the maximum local V_{th} in the channel, the interface states residing near the drain side (the shadow region in Fig. 3.18) will contribute to Icp. In Fig. 3.19, the corresponding Icp(V_h) comes from the interface states distributed between the gate edge and the position where its local V_{th} is equal to V_h, i.e.,

$$I_{cp}(V_h) = q\, f\, N_{it}\, W\, x \tag{3-2}$$

where x represents the distance from the gate edge to the position where $V_{th}(x) = V_h$. Comparing (3-1) and (3-2), we can derive

$$x = \frac{L I_{cp}(V_h)}{I_{cp,\max}} \tag{3-3}$$

Figure 3.20 shows the local V_{th} versus distance x of the control sample. The local V_{th} decreases sharply as x is smaller than 0.07 μm. We can assume that the drain junction is near x = 0.07 μm.

After 100 seconds of hot carrier stressing (V_G@$Isub_{max}$ and V_{DS} = 4.5 V), the incremental charge pumping current (ΔIcp) at a certain V_h is proportional to the number of generated interface traps from the gate edge to the point x (as shown in Fig. 3.21). ΔIcp can be written as

$$\Delta I_{cp} = q\, f\, W \int_0^x N_{it}(x)\, dx \tag{3-4}$$

Therefore, the $N_{it}(x)$ generated by the hot carrier stress can be extracted by using the following formula:

$$N_{it}(x) = \frac{d\Delta I_{cp}}{dx}\frac{1}{q\, f\, W} = \frac{d\Delta I_{cp}}{dV_h}\frac{dV_h}{dx}\frac{1}{q\, f\, W} \tag{3-5}$$

The relationship of $\frac{dV_h}{dx}$ versus x can be derived from V_h versus x, so that the lateral distribution, $N_{it}(x)$, can be obtained from the measurements mentioned above.

The derived lateral profiles of the interface state distribution for all splits of devices extracted by Eq. (3-5) are shown in Fig. 3.22. It is obviously seen that interface state generation sharply increases near the drain region in the SiN-capped samples. With increasing SiN thickness, larger degradation occurs, so that the SiN-3kÅ sample has the worst result. From these results, we can confirm that the hot-carrier degradation is highly localized and the major damage region is within 0.1μm near the drain edge.

The above results are consistent with the results and discussion mentioned in Section 3-2. The hot carrier degradation in SiN-capped samples is caused by the channel strain, as well as the higher hydrogen species at the channel/oxide interface.

Chapter 4
Summary and Conclusion

In this thesis, the effects of capping a PECVD SiN layer over the gate of NMOSFETs on the device characteristics and hot-carrier degradation are investigated. Several important phenomena are observed and summarized as follows.

The channel strain induced by the SiN capping layer over the gate enhances the device performance greatly by boosting the drive current. As SiN capping layers increases, the device performance becomes better due to the increase of tensile stress exerted on the channel. For example, in the device with the thickest SiN capping layer (SiN-3kÅ) explored in this study, drain current enhancement ratio of more than 17% and the transconductance enhancement ratio of more than 29% are achieved at a channel length of 0.4μm. The poly depletion effect, a phenomenon that we encountered in previous study on devices capped with LPCVD SiN, is eliminated in this work with the PECVD process. This is attributed to the negligible thermal budget of the PECVD deposition so that the activated carriers concentration in the poly-Si gate is not affected. However, the band-gap narrowing effect caused by channel strain will result in worsened threshold voltage roll-off characteristics.

The hot carrier degradation is greatly affected by the channel strain level of the SiN capped devices. With the increasing channel strain associated with increasing SiN thickness, the accompanying band-gap narrowing and the increasing carrier mobility will tend to worsen the hot carrier reliability in the SiN capped devices. The interface states caused by the breaking of Si-H bonds at the oxide/channel interface by hot carriers also lead to performance degradation.

In this work, tensile stress could be enhanced by increasing SiN thickness and

therefore device performance could be boosted, especially for short channel devices. However, the hot carrier reliability was also degraded owing to the increase in mobility and the use of hydrogen-containing precursors during the deposition of SiN capping layers. How to reduce the hydrogen content in the SiN without compromising the tensile stress is essential to the implementation of uniaxial-strain NMOS devices.

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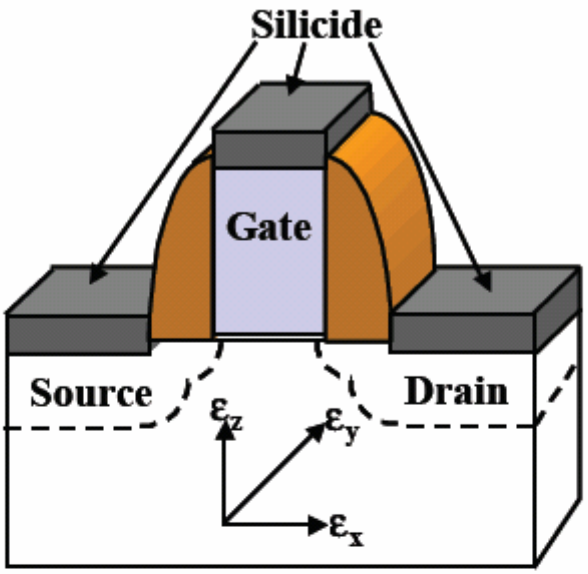


Schematic view of 3D process-induced strain components.

Impact of 3D Strain Effects on CMOS Performance.

***Strain change=Increased tensile of decreased compressive strain.**

Direction of Strain Change*	CMOS Performance Impact	
	NMOS	PMOS
X	Improve	Degrade
Y	Improve	Improve
Z	Degrade	Improve

3D Strain Sensitivity of CMOS Current Drive

Fig.1.1 Schematic illustration of 3D process-induced strain components [25].

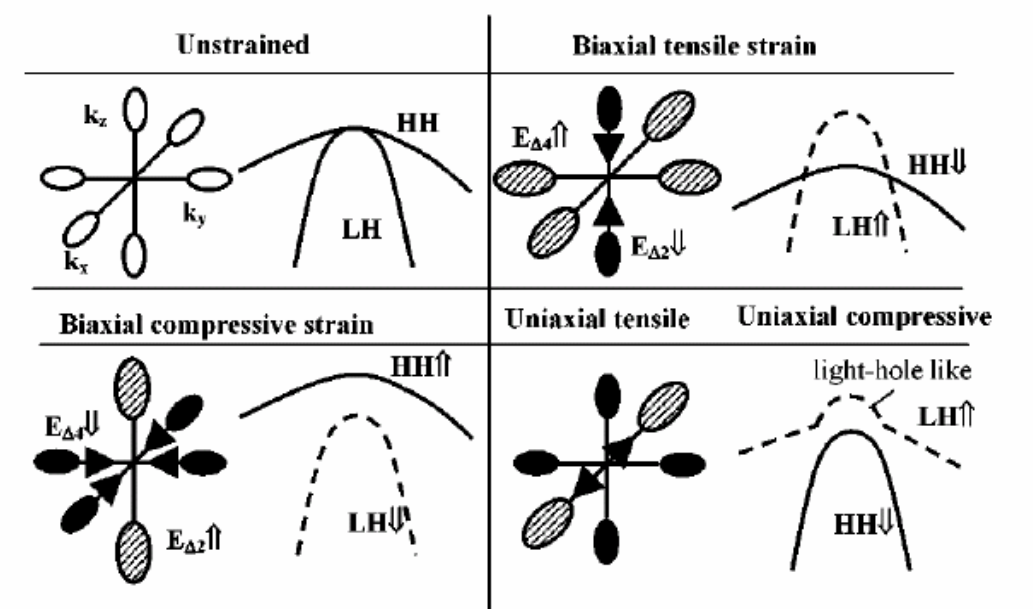


Fig.1.2 Simple schematic of conduction and valence band structures with and without strain [35].

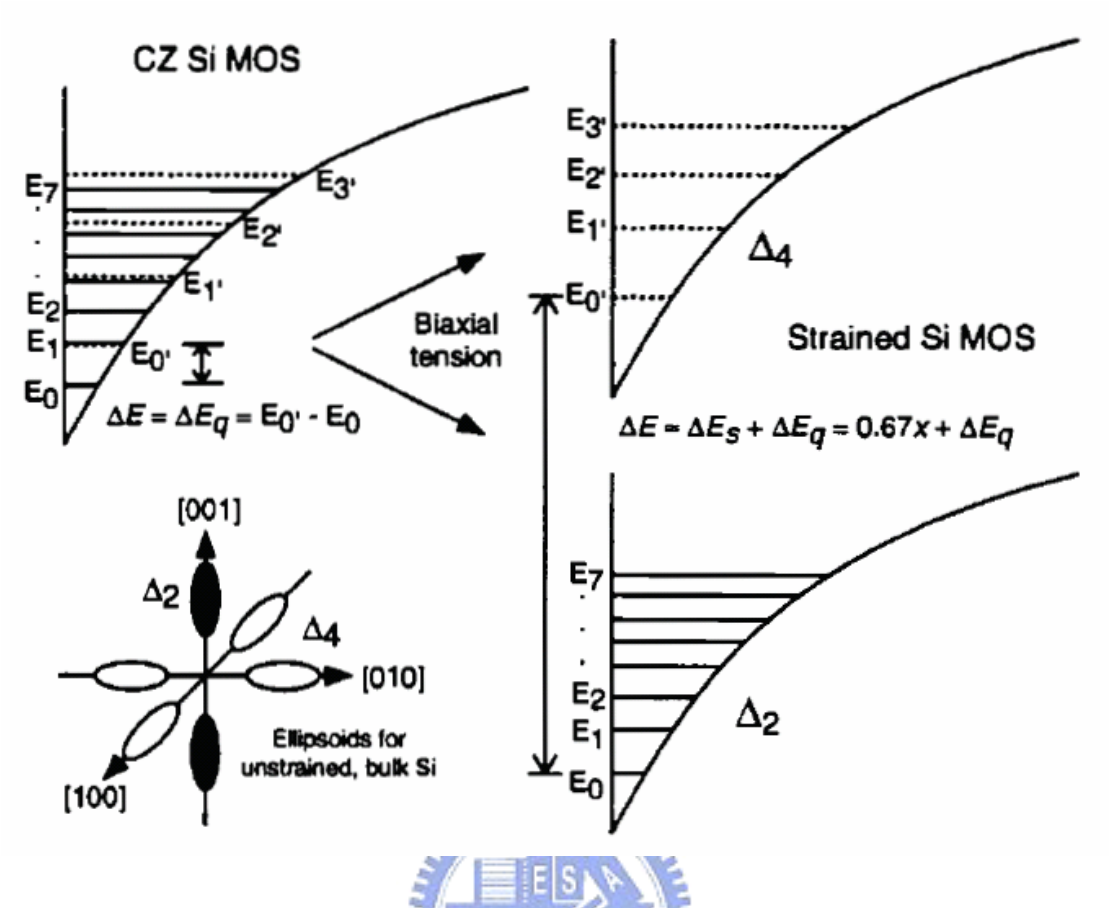


Fig.1.3 Schematic diagram of the energy sub-bands without strain and with bi-axial strain in an MOS inversion layer [27].

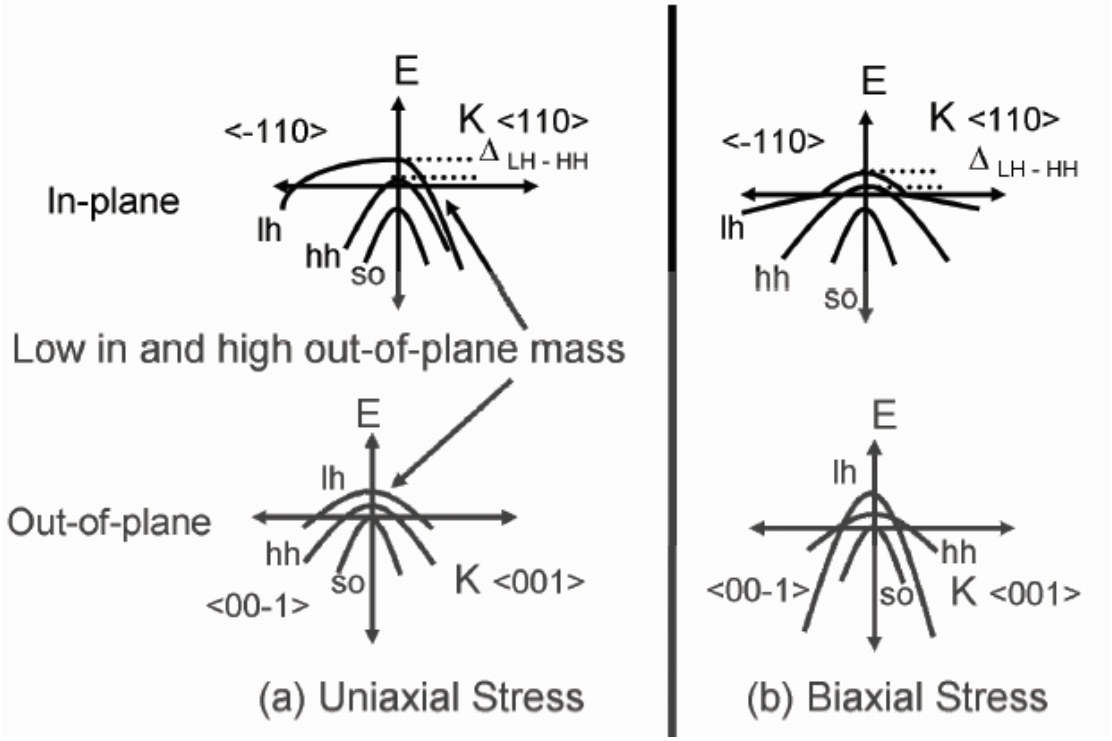


Fig.1.4 Schematic diagram of the valence bands E vs. k in uni-axially tensile strain and bi-axially tensile strain Si layers [29].

Gate		SiN Stress Layer	Oxide Passivation Layer
Oxide 30Å	α-Si 1500Å	SiN 0Å	Oxide 3000Å
		SiN 200Å	Oxide 2800Å
		SiN 1000Å	Oxide 2000Å
		SiN 3000Å	Oxide 0Å

Table.2.1 Split conditions of oxide and capping layer thickness.

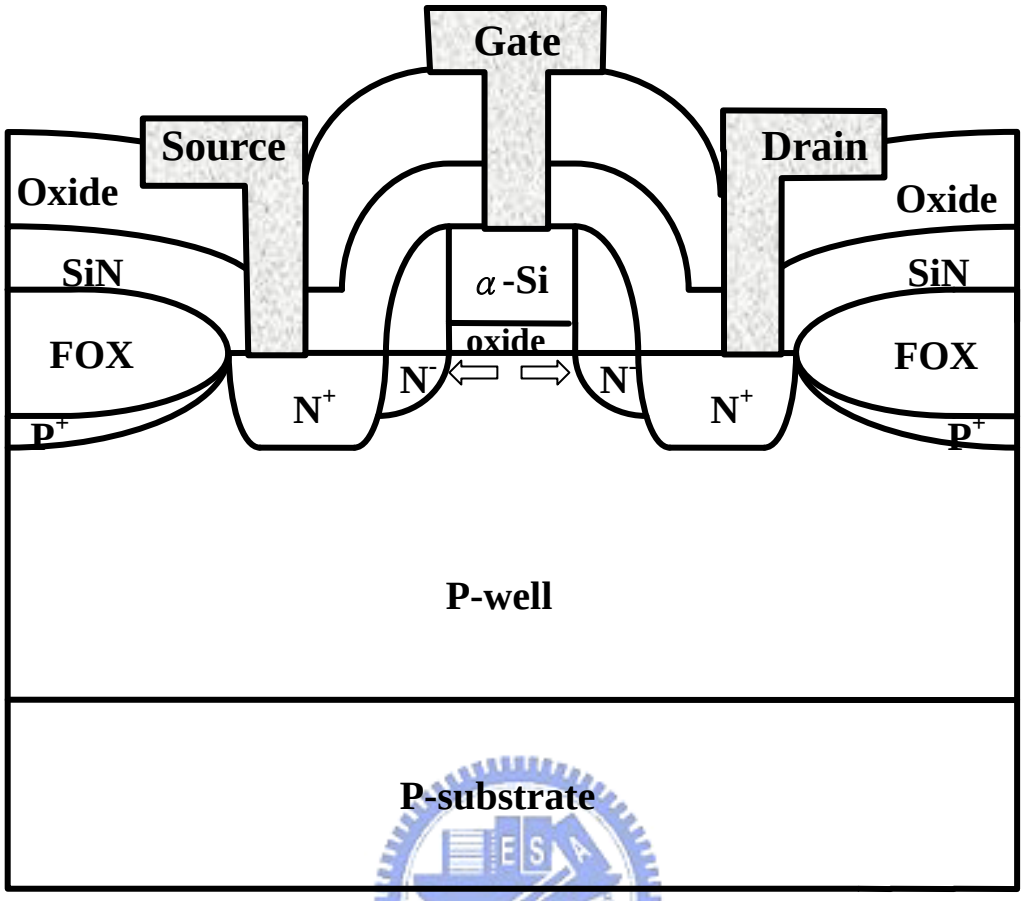


Fig.2.1 Schematic cross section of the locally-strained-channel NMOSFET.

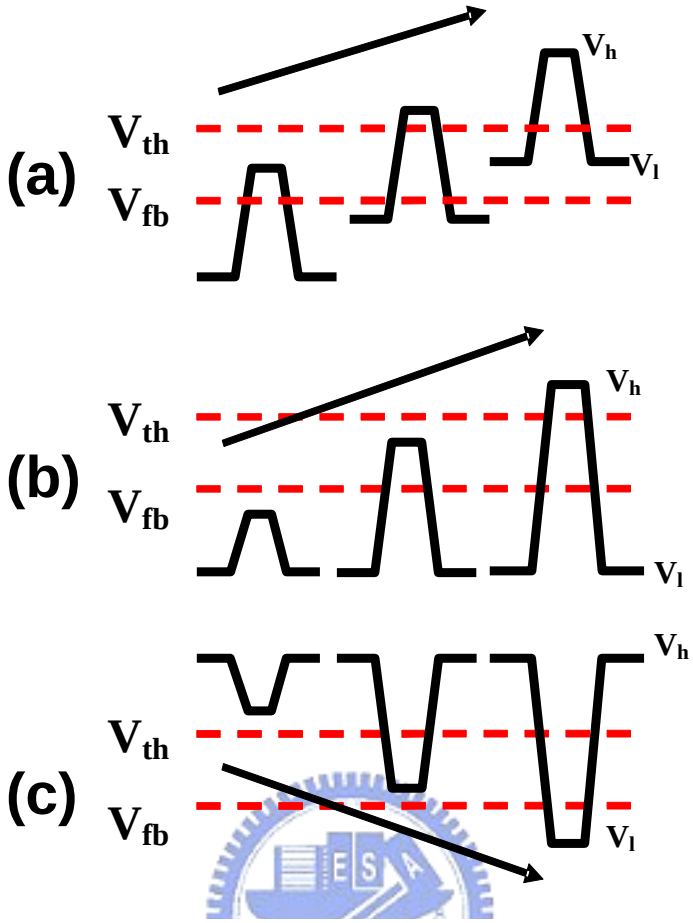


Fig.2.2 Schematic illustrations for the charge pumping measurements with (a) fixed amplitude, (b) fixed base sweep, and (c) fixed peak sweep. The arrows indicate the sweep directions.

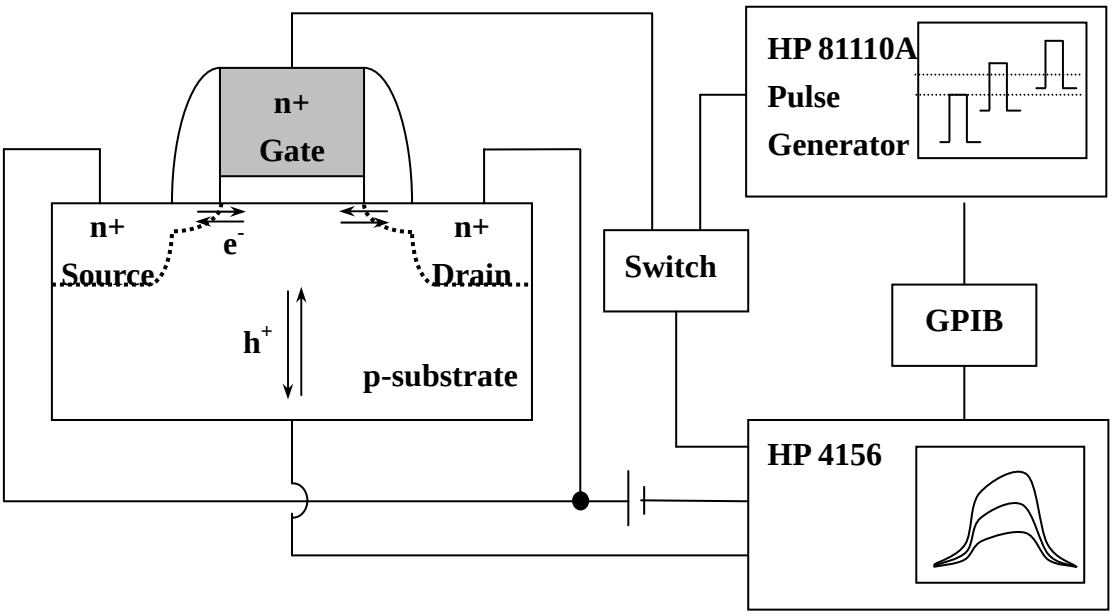


Fig.2.3 Setup structure for charge pumping measurements.

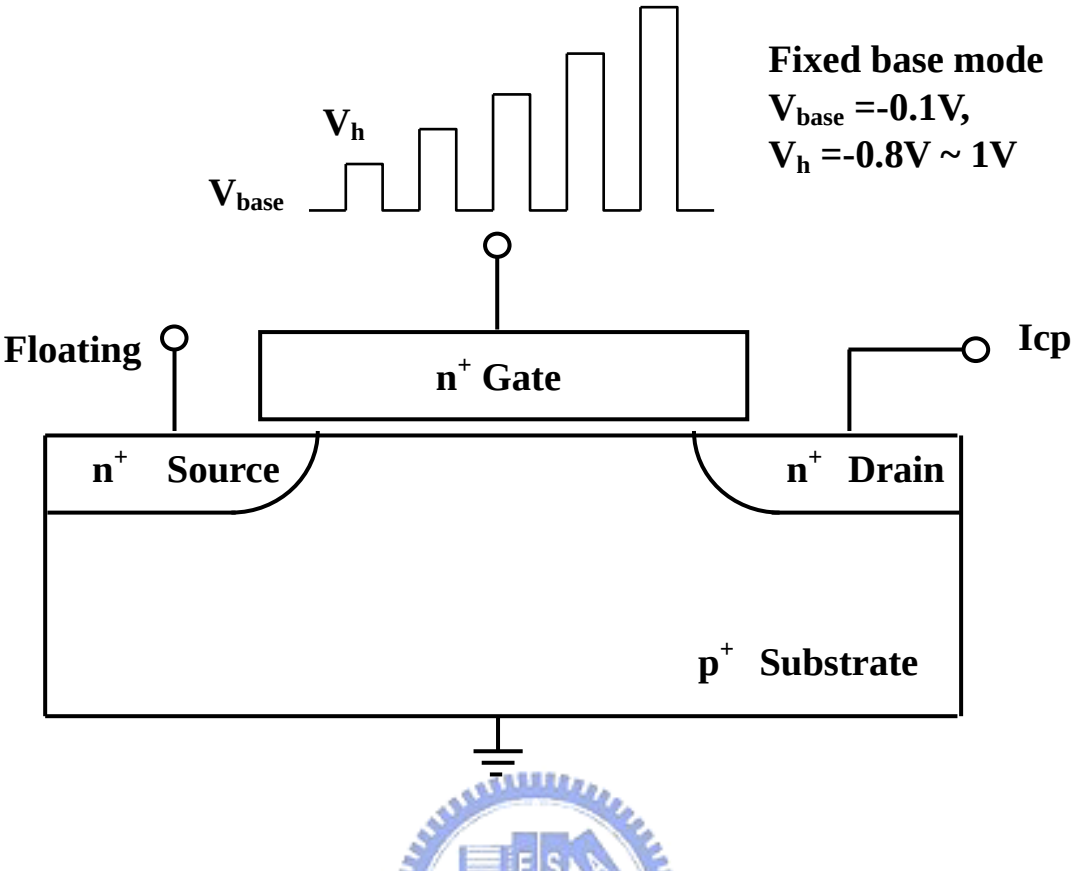


Fig.2.4 The measurement setup of single-junction charge pumping measurement.

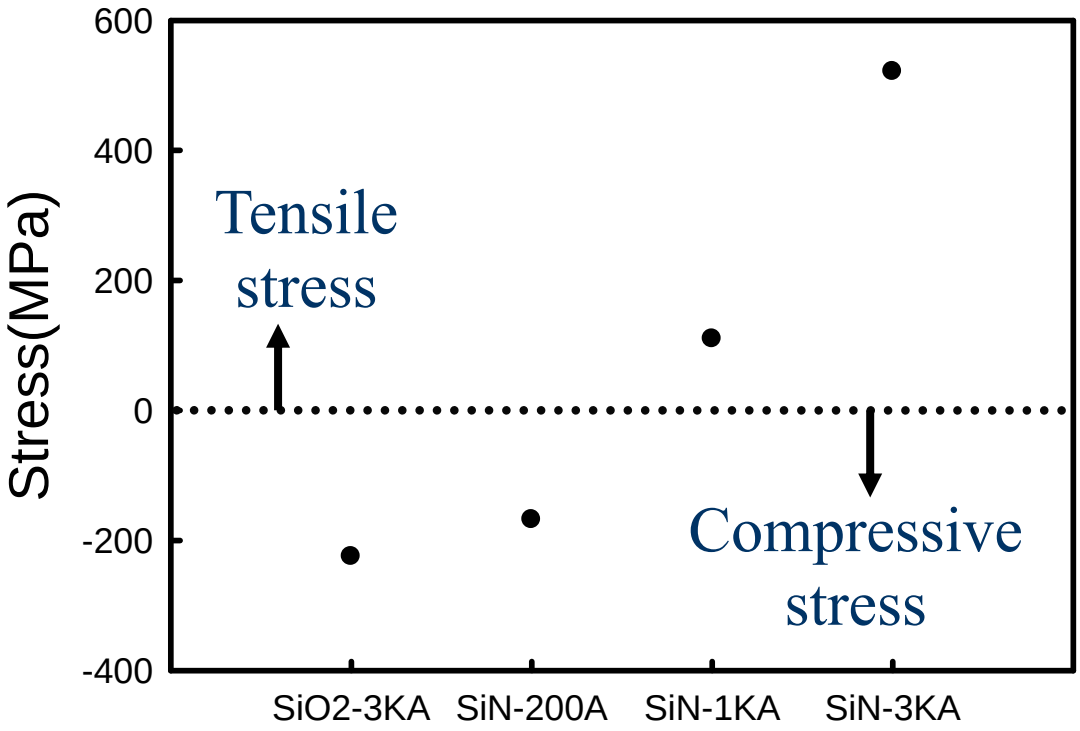


Fig. 3.1 Tensile strain for different SiN thickness.

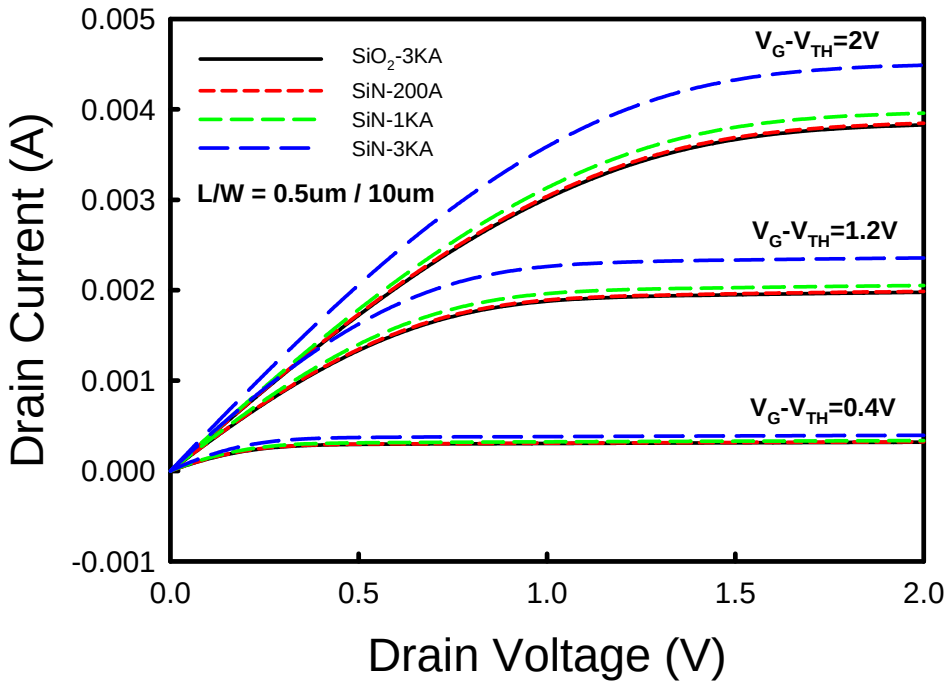


Fig. 3.2 I_D-V_D characteristics of different splits of NMOSFETs. Channel length/width = 0.5μm / 10μm.

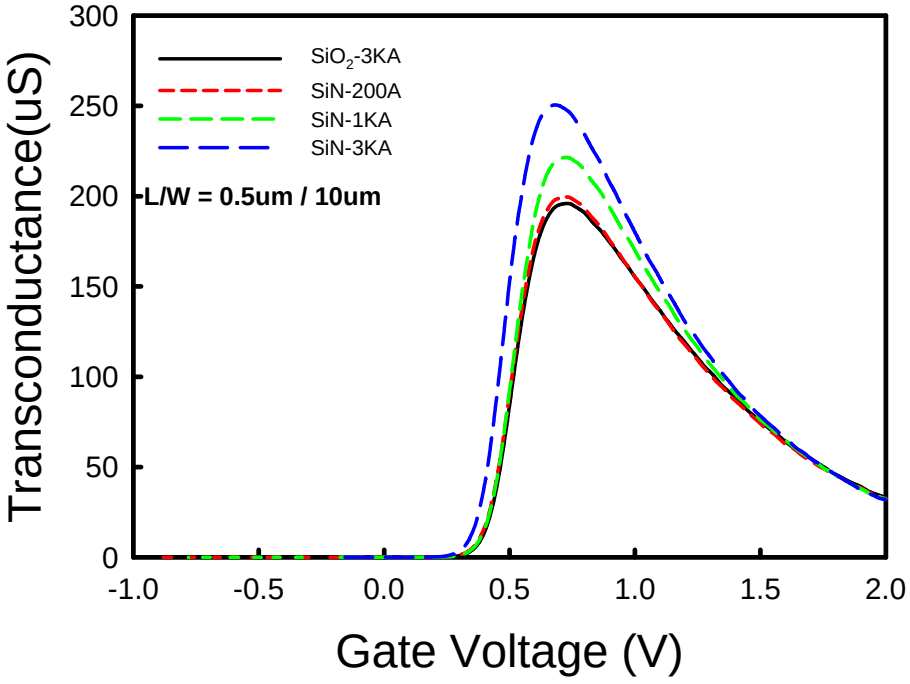
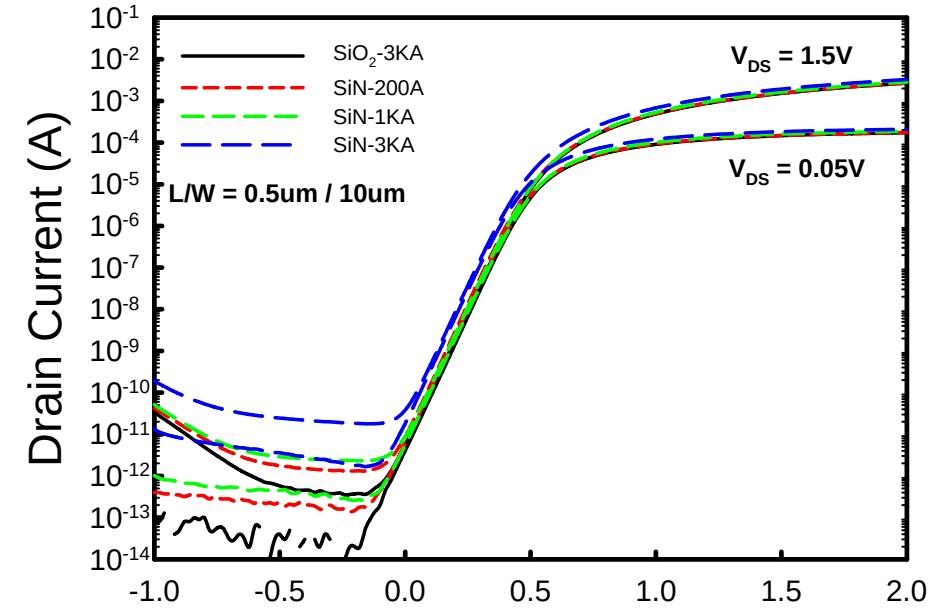
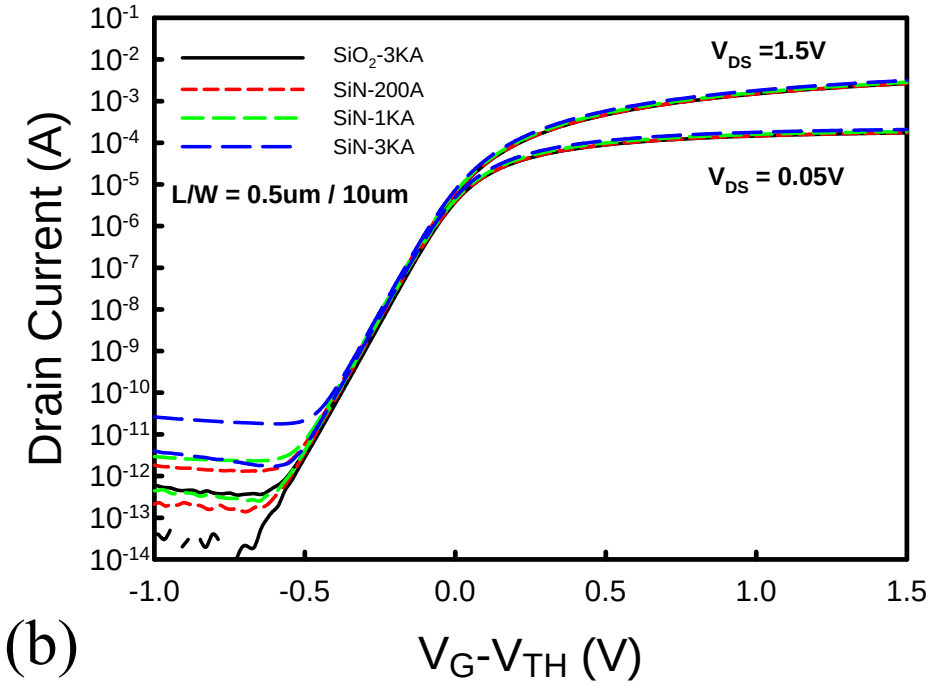


Fig. 3.3 Transconductance of different splits of NMOSFETs. Channel length/width = 0.5μm / 10μm.



(a)



(b)

Fig. 3.4 Subthreshold characteristics of different splits of NMOSFETs. Channel length/width = 0.5μm / 10μm. (a) I_D versus V_D (b) I_D versus $V_D - V_{TH}$.

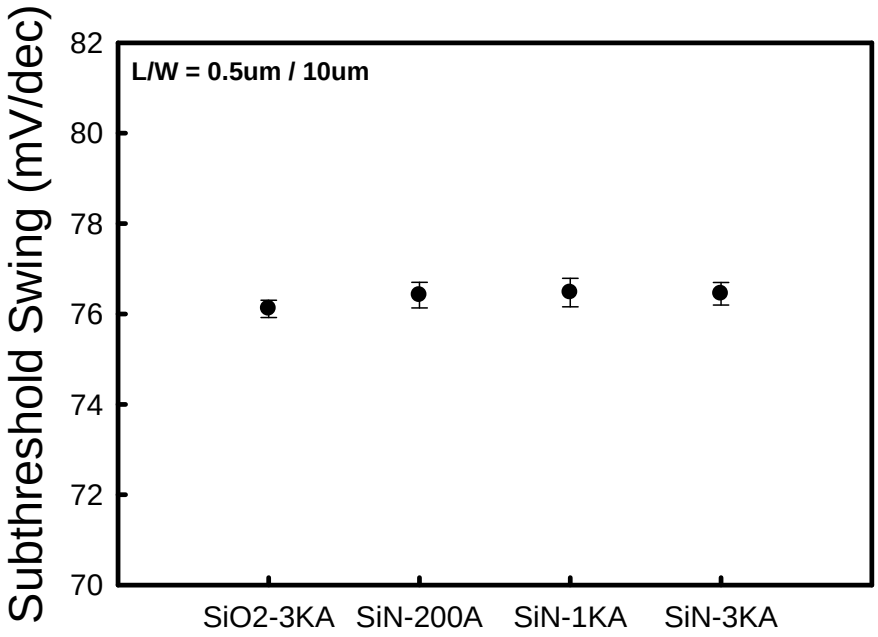


Fig. 3.5 Subthreshold swing of different splits of NMOSFETs. Channel length/width = 0.5μm / 10μm.

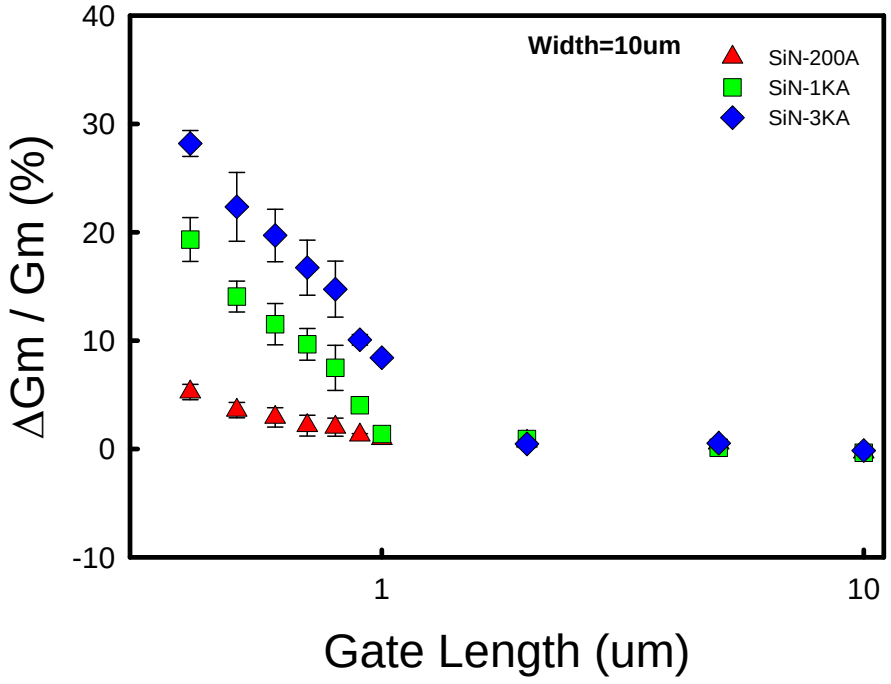


Fig. 3.6 Increase in transconductance versus channel length for different splits of SiN-capped NMOSFETs with respective to the control devices.

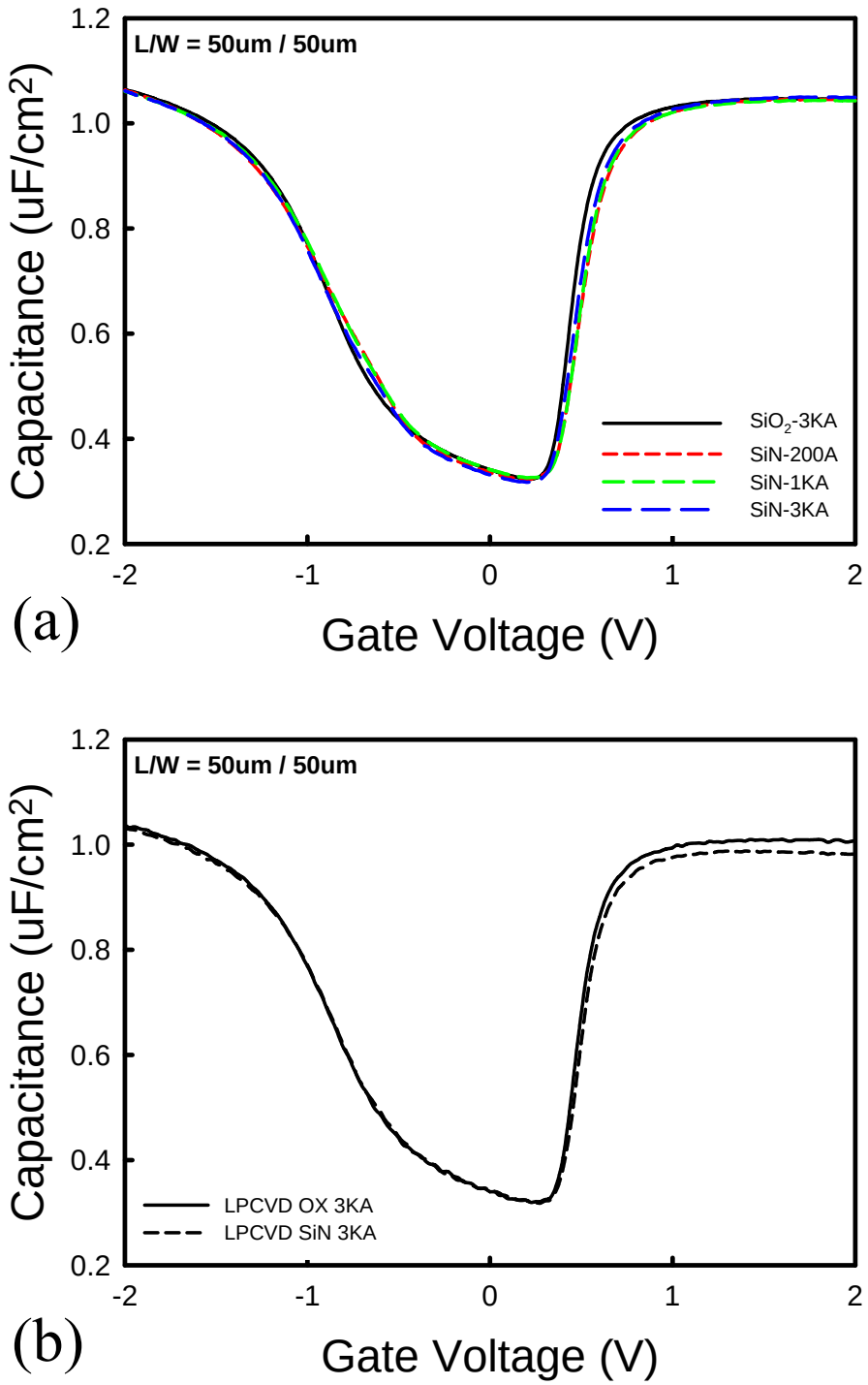


Fig. 3.7 Capacitance-Voltage characteristics for different splits of NMOSFETs. Channel length/width = 50μm / 50μm. (a) Devices with PECVD capping (b) Poly depletion effect in devices with LPCVD capping [38].

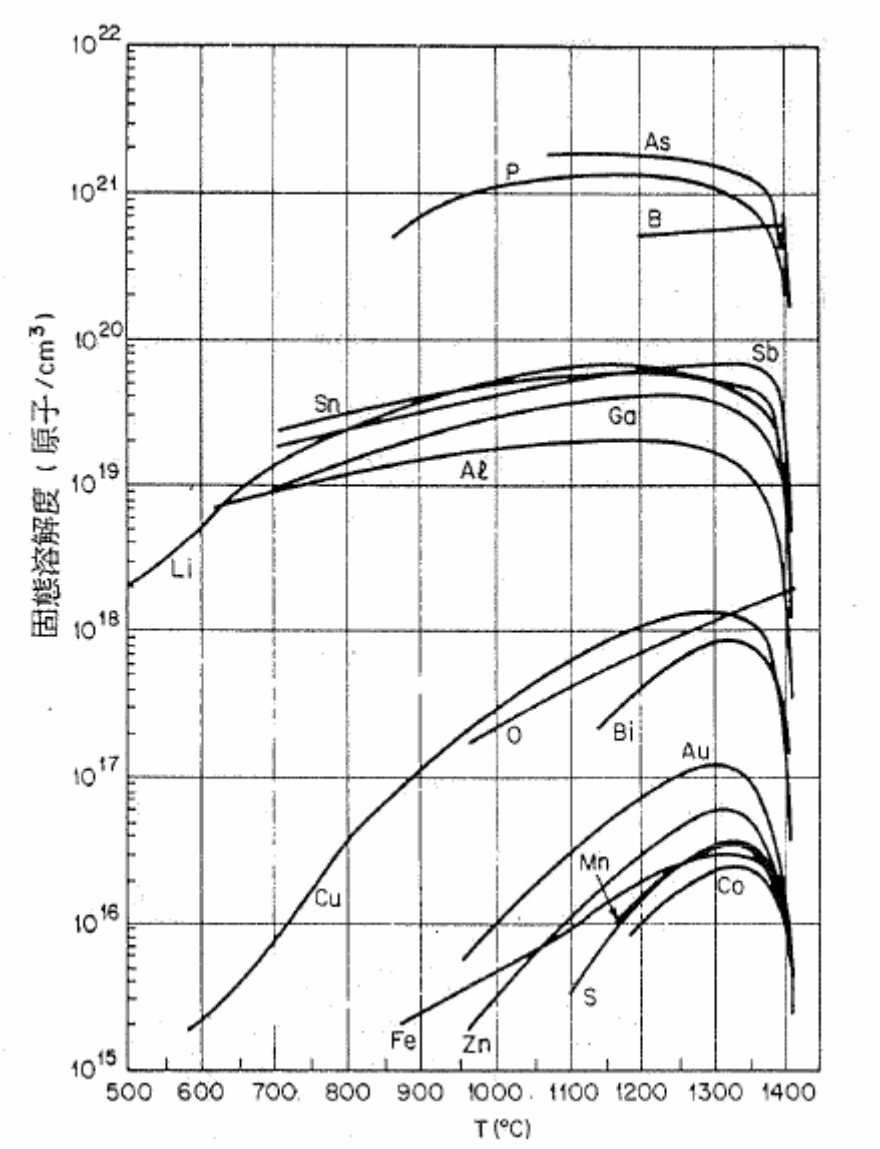


Fig. 3.8 Solid solubility of various elements in Si as a function of temperature[39].

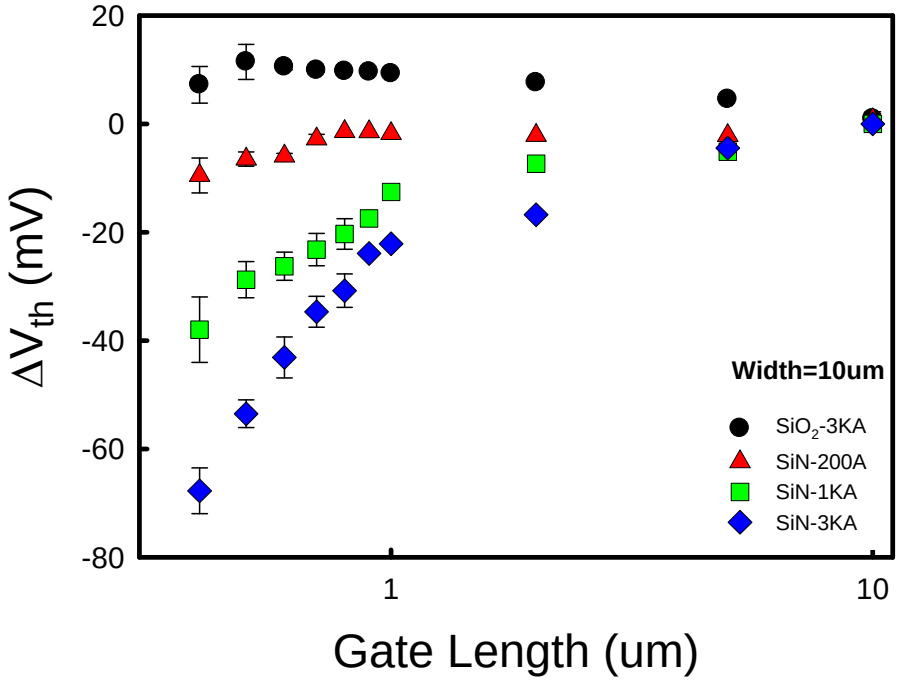


Fig. 3.9 Threshold voltage roll-off as a function of channel length for different splits of NMOSFETs.

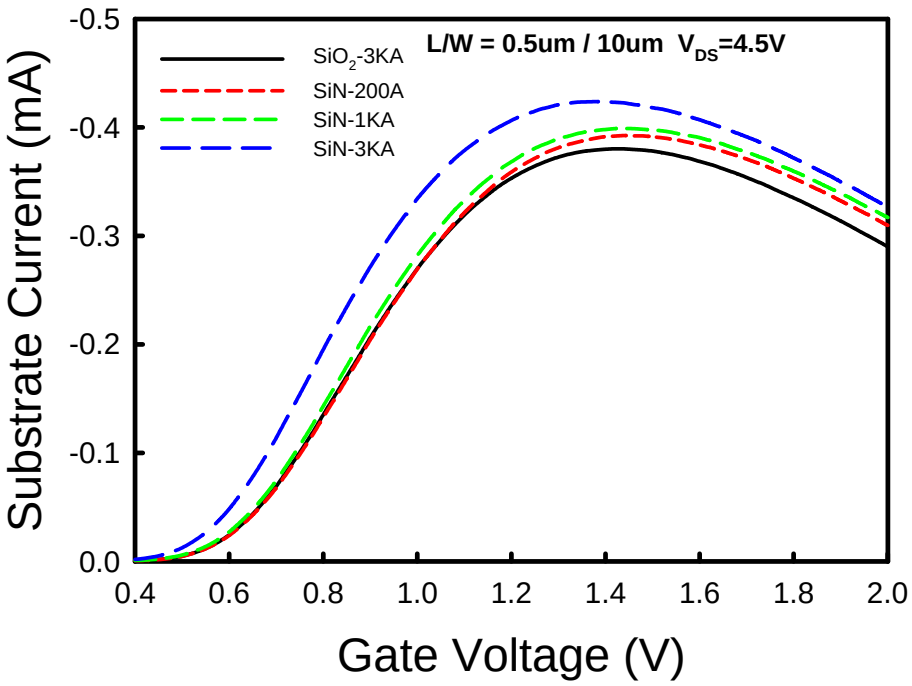
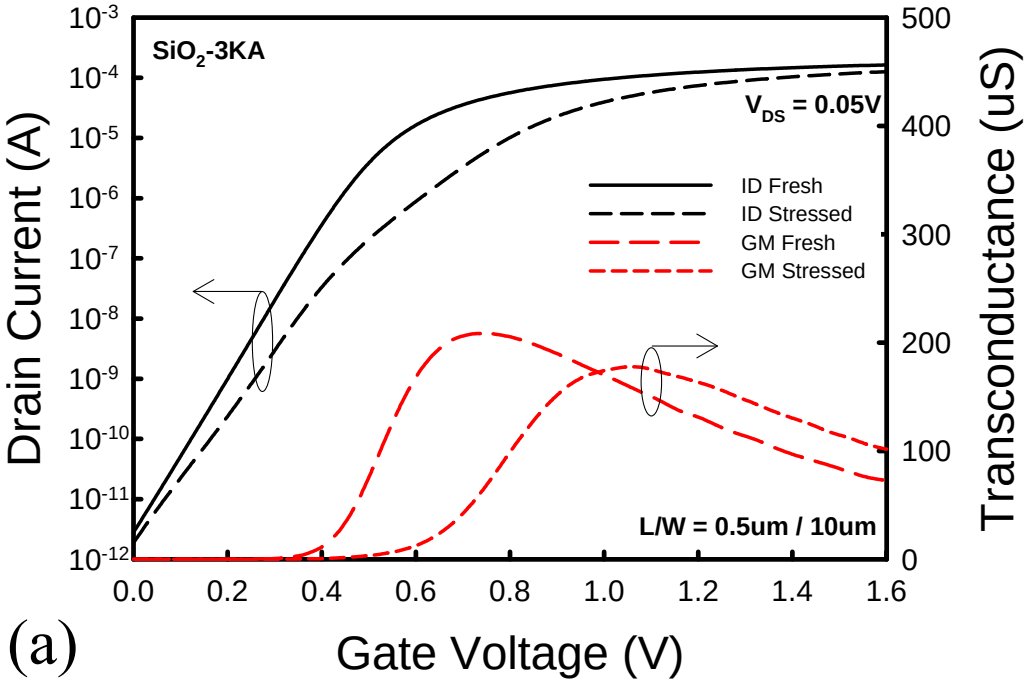
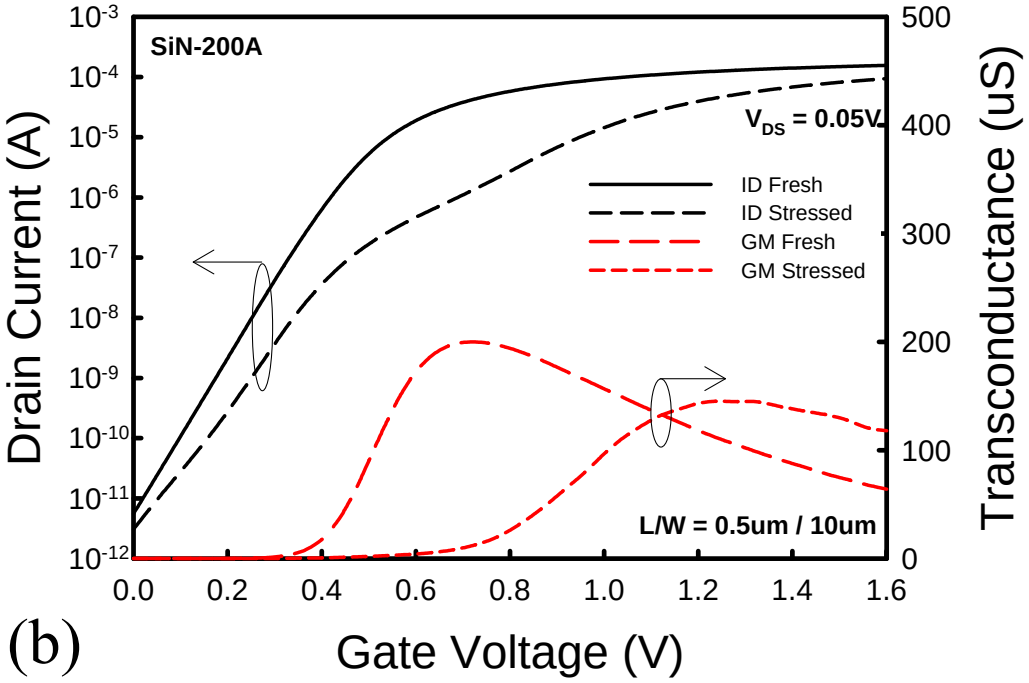


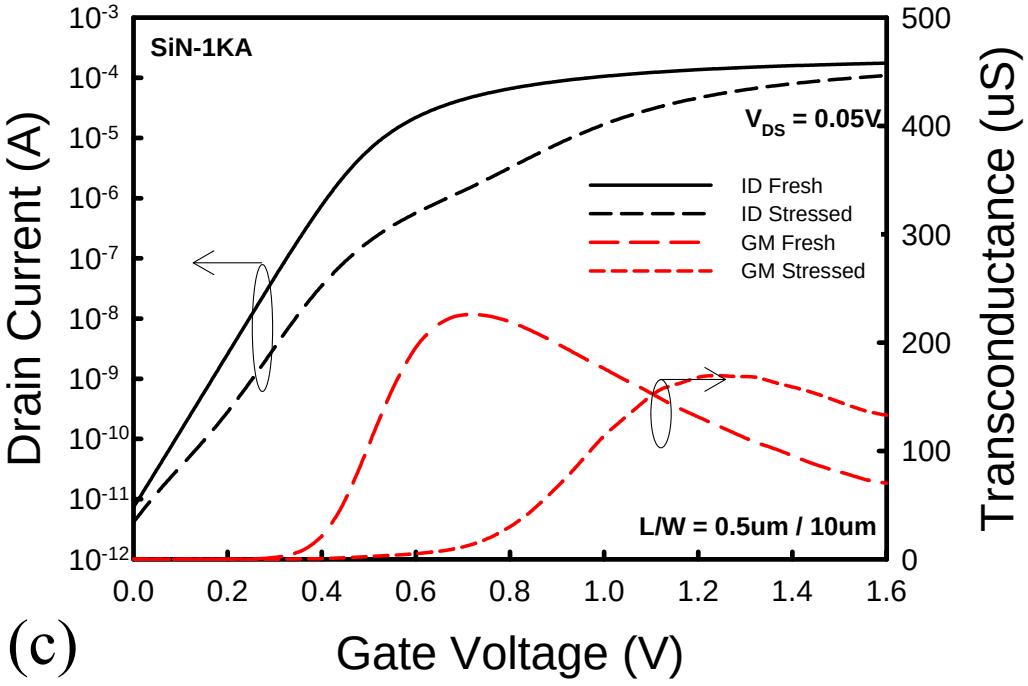
Fig. 3.10 Substrate current versus gate voltage for different splits of NMOSFETs. Channel length/width = 0.5μm / 10μm.


SiO2-3KA
VDS = 0.05V
ID Fresh
ID Stressed
GM Fresh
GM Stressed
L/W = 0.5um / 10um
Drain Current (A)
Transconductance (uS)
Gate Voltage (V)
10-3
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
10-12
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
500
400
300
200
100
0

(a)


SiN-200A
VDS = 0.05V
ID Fresh
ID Stressed
GM Fresh
GM Stressed
L/W = 0.5um / 10um
Drain Current (A)
Transconductance (uS)
Gate Voltage (V)
10-3
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
10-12
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
500
400
300
200
100
0

(b)



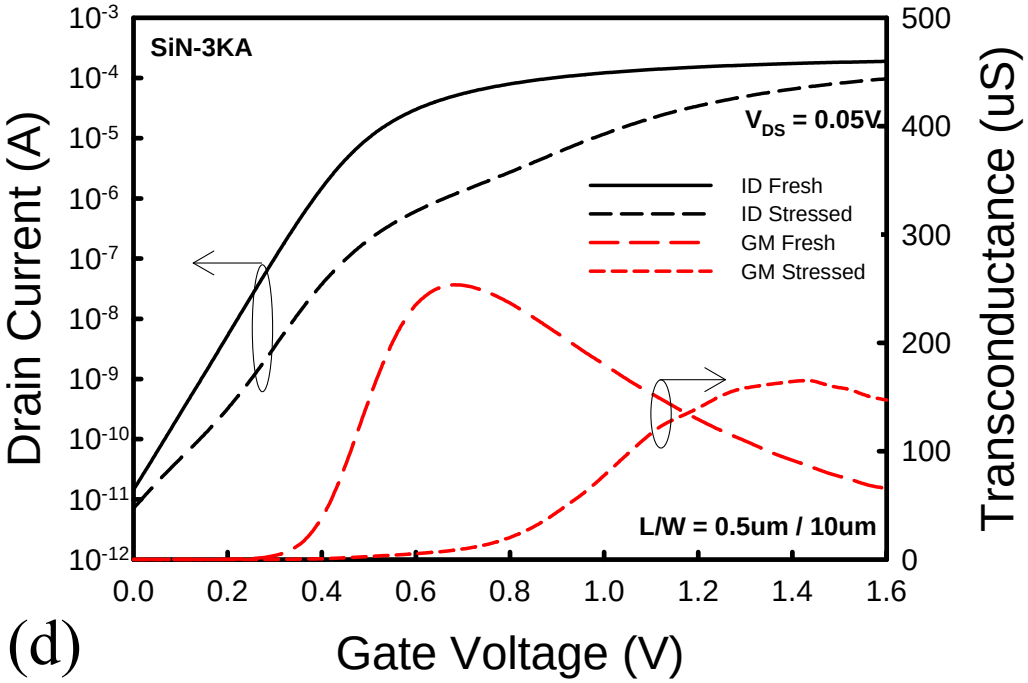


Fig. 3.11 Drain current and transconductance of devices before and after 5000 seconds hot-carrier stressing. Channel length/width = 0.5μm / 10μm. (a) SiO_2 sample (b)SiN-200Å sample (c)SiN-1kÅ sample (d)SiN-3kÅ sample.

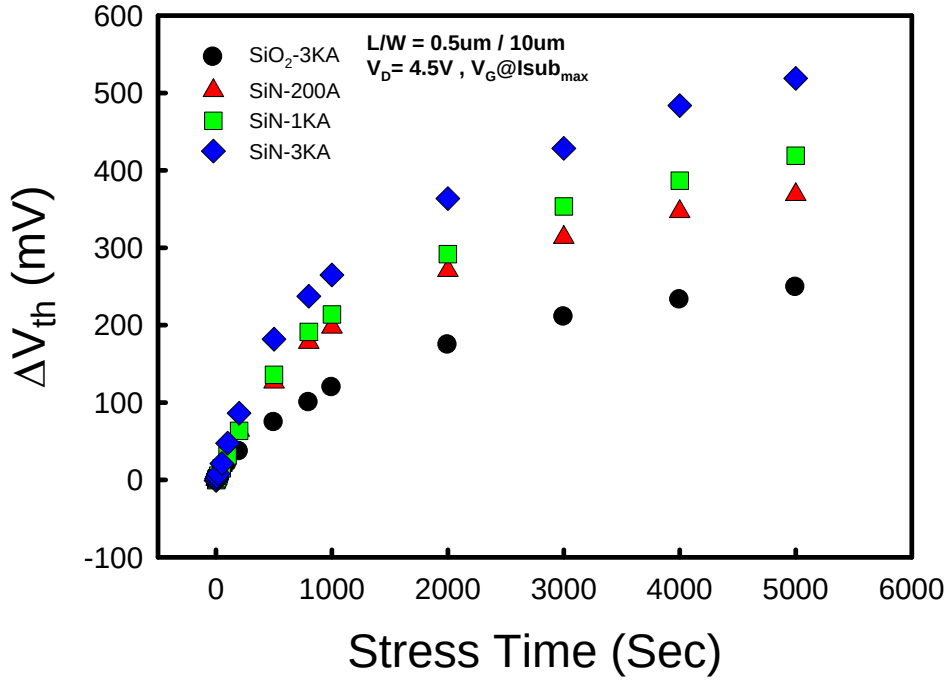


Fig. 3.12 Threshold voltage degradation after hot-carrier stressing. Stress voltage V_{DS} = 4.5V and V_{GS} at peak substrate current. Channel length/width = 0.5μm / 10μm.

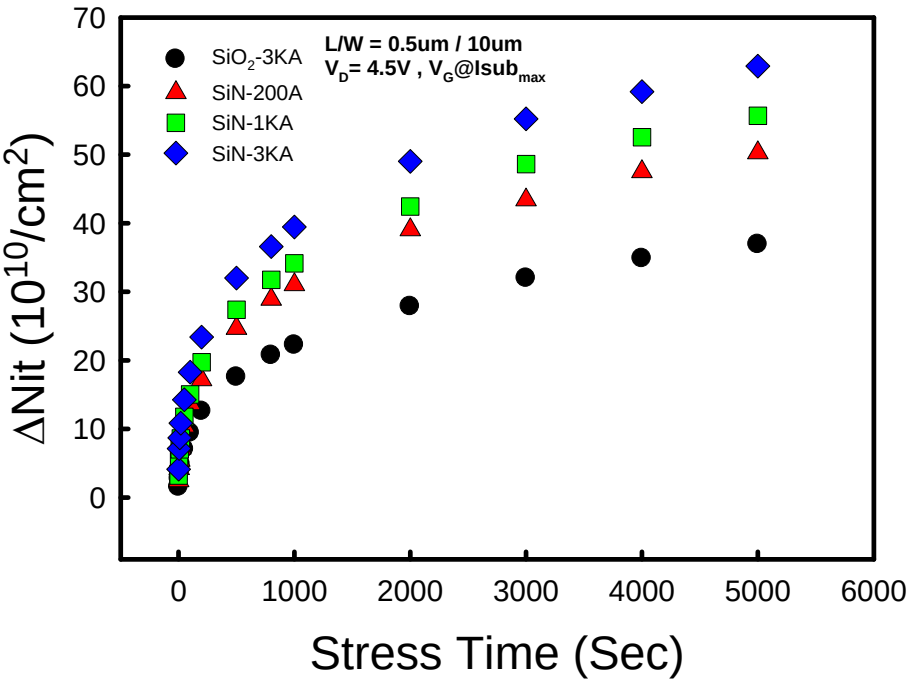


Fig. 3.13 Interface trap density degradation after hot-carrier stressing. Stress voltage V_{DS} = 4.5V and V_{GS} at peak substrate current. Channel length/width = 0.5μm / 10μm.

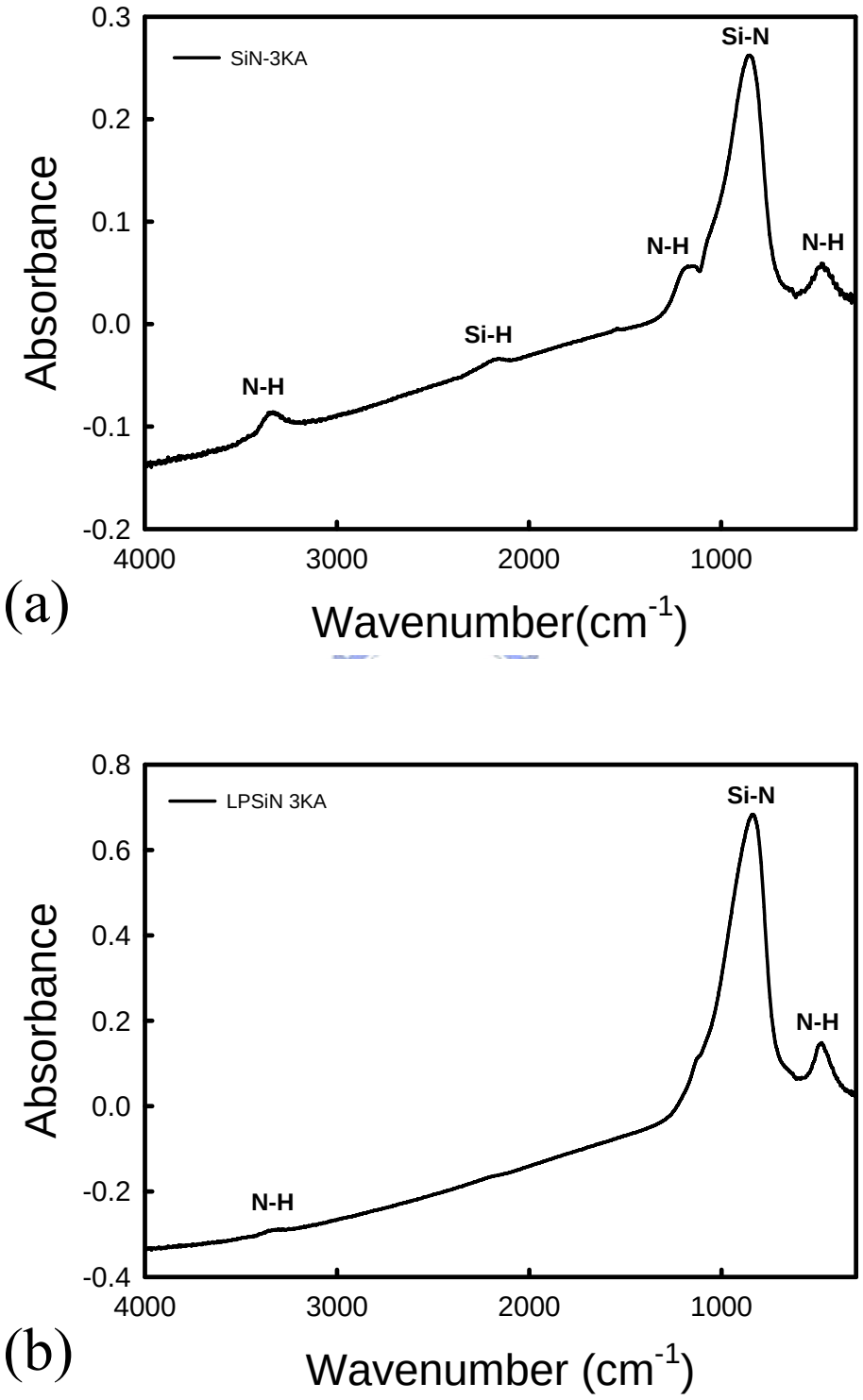


Fig. 3.14 Bonding signals of (a) PECVD (b) LPCVD SiN layers measured by FTIR.

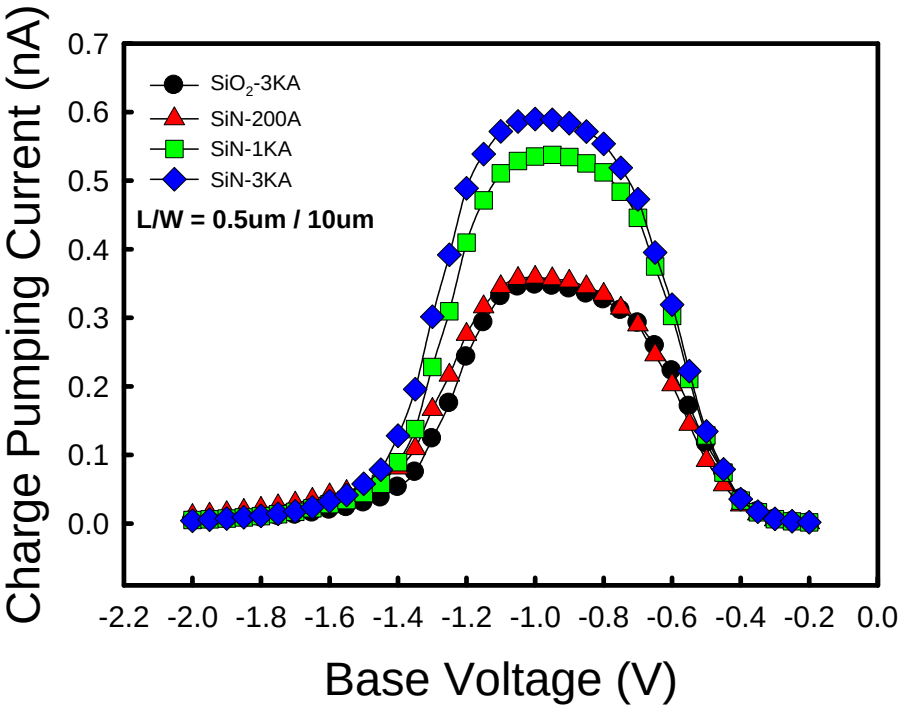


Fig. 3.15 Fresh charge pumping current of different splits of NMOSFETs. Channel length/width = 0.5μm / 10μm.

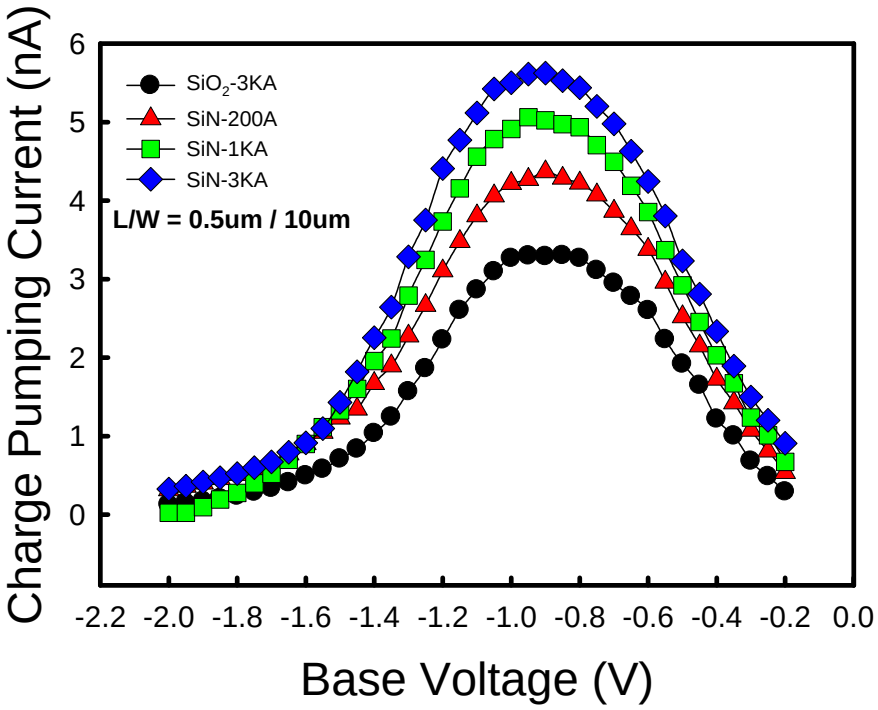


Fig. 3.16 Charge pumping current of different splits of NMOSFETs after 5000 seconds of hot carrier stress. Stress voltage V_{DS} = 4.5V and V_{GS} at peak substrate current. Channel length/width = 0.5μm / 10μm.

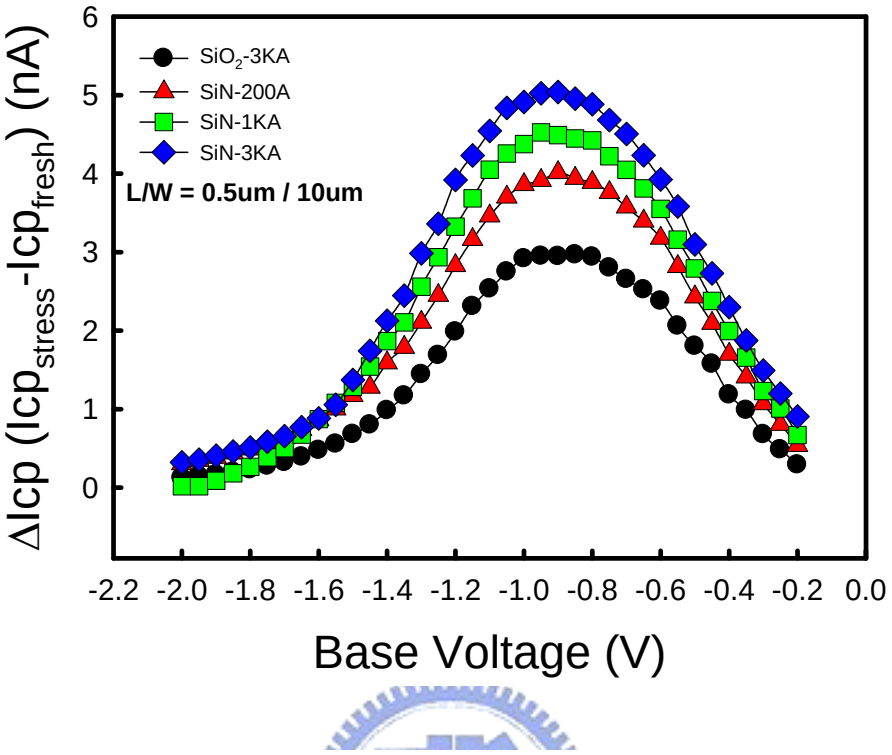


Fig. 3.17 Increase in charge pumping current after 5000 seconds hot carrier stress of different splits of NMOSFETs. Stress voltage V_{DS} = 4.5V and V_{GS} at peak substrate current. Channel length/width = 0.5μm / 10μm.

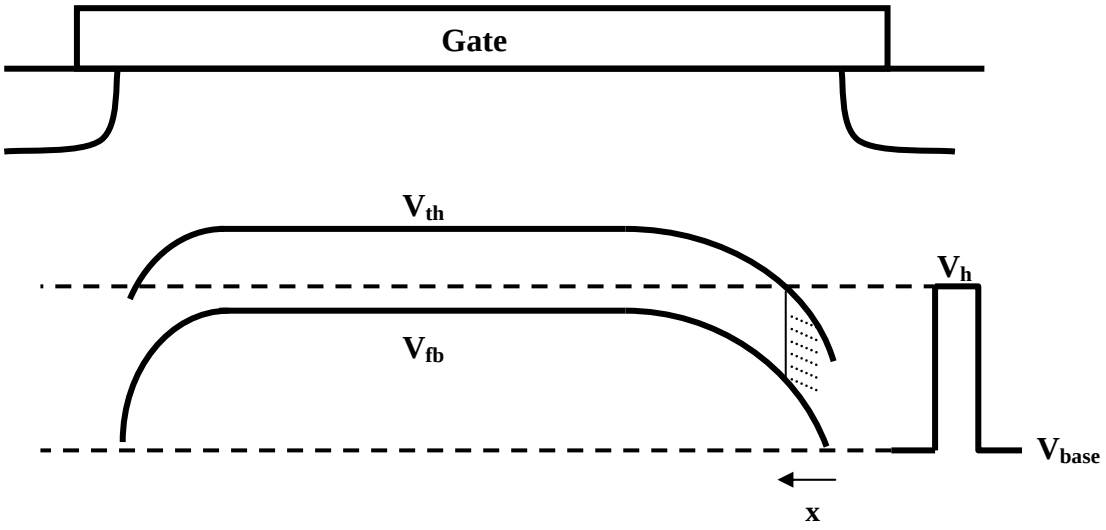


Fig. 3.18 Non-uniform distribution of local threshold voltage and flat-band voltage across the device caused by variation of lateral doping concentration.

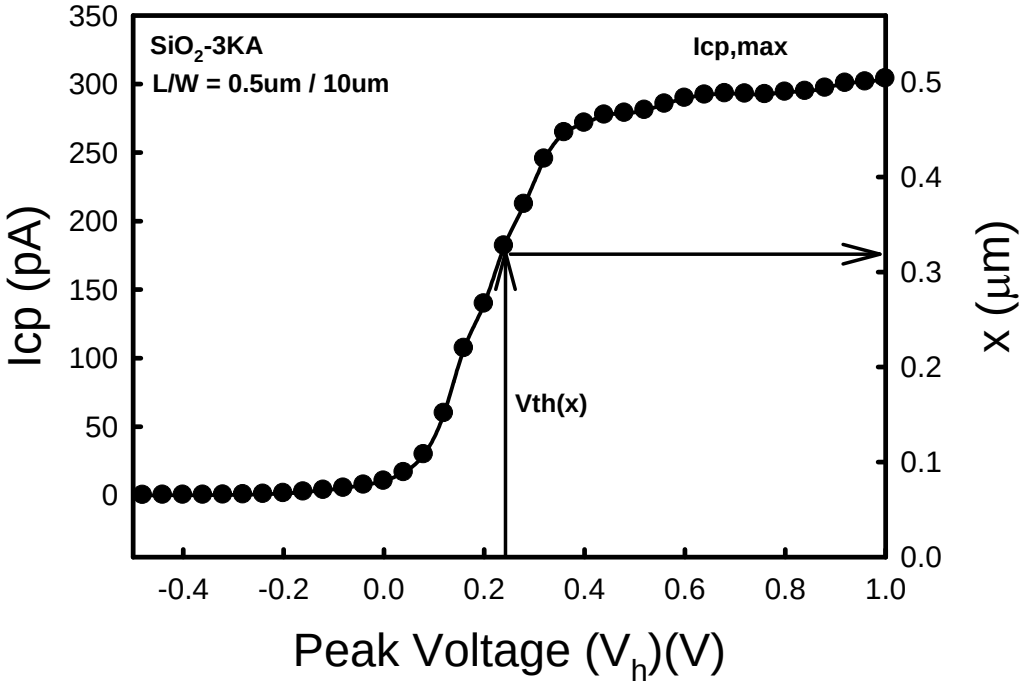


Fig. 3.19 Derivation of the relationship between local threshold voltage and lateral distance x from the single junction charge pumping data of the control device.

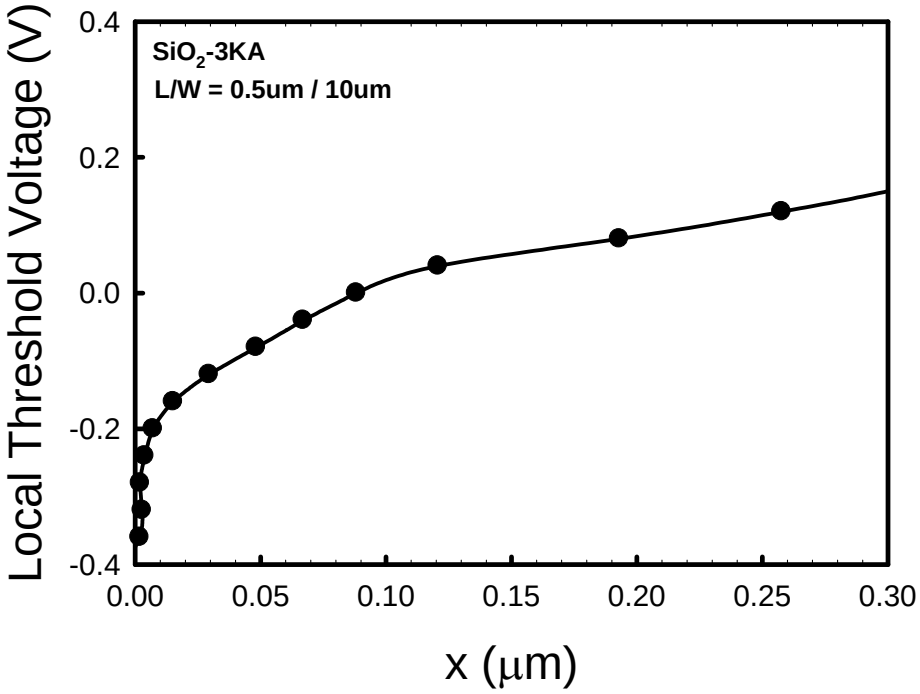


Fig. 3.20 Extracted lateral profile of local threshold voltage near the graded drain junction in the control sample.

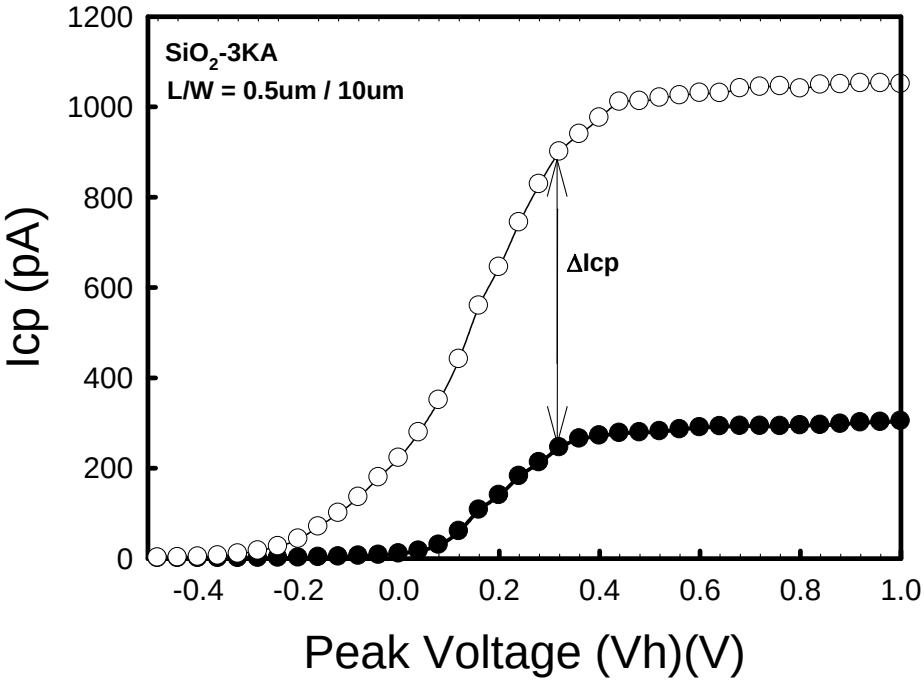


Fig. 3.21 Charge pumping current before and after 100 seconds hot carrier stress. Stress voltage V_{DS} = 4.5V and V_{GS} at peak substrate current occurred. Channel length/width = 0.5μm / 10μm.

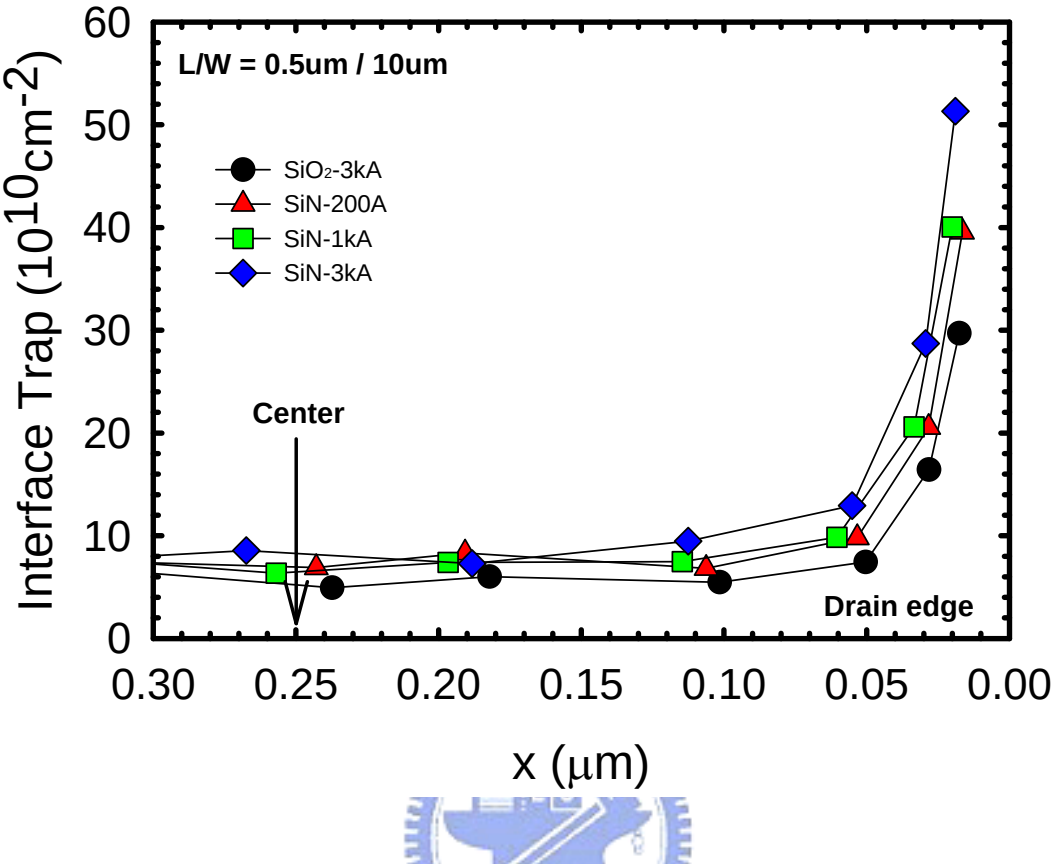


Fig. 3.22 Lateral profile of interface state generation after hot-carrier stress for all splits.

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論文題目：

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