國 立 交 通 大 學

電機學院 IC 設計產業研發碩士班

碩 士 論 文

內建自我測試電路之管線式類比數位轉換器

Built-in Self-test Circuit for Pipelined Analog to Digital Converter

研 究 生：任慶霖

指導教授：蘇朝琴　教授

中 華 民 國 九十七 年 十 月

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A Thesis

Submitted to College of Electrical and Computer Engineering

National Chiao Tung University

In partial Fulfillment of the Requirements

for the Degree of

Master

in

Industrial Technology R & D Master Program on
IC Design

October 2008

Hsinchu, Taiwan, Republic of China

中 華 民 國 九十七 年 十 月

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摘要

近年來由於積體電路製程的進步以及離散時間數位信號處理技術的發展，同時，在解析度、速度、和功率消耗的彈性，管線式類比數位轉換器被廣泛的應用在許多不同的領域。在傳統轉換器的靜態測試中，測試時間消耗及測試設備的需求是主要成本。在這篇論文裡，我們實現一個管線式類比數位轉換器以及其內建自我測試電路。

利用單一管線級的優點，我們使用後一級的比較器來掃描前一級的轉換曲線，掃描的結果配合信心區間的機率分析，可以得到單一級的增益誤差以及偏移誤差；我們設計一個 8 位元每秒 100 百萬取樣的管線式類比數位轉換器來驗證這個新的測試方式，而這個轉換器由七個每級 1.5 位元解析度和 1 位元解析度的最後一級組成。

所提出的電路架構將被實現在 TSMC 1P6M CMOS 0.18μm 的製程，其晶片面積為$0.58mm \times 0.66mm$ (不包含 PAD)，在正常模式輸入信號是 20.9 百萬赫茲的情況下，最高 SNDR 是 47.09dB，總共的功率消耗為 110 mW；在自我測試模式下，刻意再第一二級加入已知的增益誤差，讓內建自我測試電路來量測，而其結果符合已知的增益誤差量，同時利用軟體 Matlab 來消除已知的增益誤差。

索引詞彙—管線式、類比數位轉換器、自我內建測試、自我測試

Built-in Self-test Circuit for Pipelined Analog to Digital Converter

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Industrial Technology R & D Master Program of Electrical and Computer Engineering College

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Abstract

New CMOS and digital signal processing techniques have a great variety of applications in recent years. Pipelined ADC is wildly utilized for its flexibility in speed, resolution, and power. In traditional converter's static testing time consumption and hardware overhead of test equipment are still the prime concerns. In the thesis, a simple built-in self test is proposed for pipelined analog to digital converters.

By taking the advantages of the structure in pipelined stage, we use the next stage comparators to scan the transfer curve of the previous stage. The stage gain error and offset error can be estimated. With certain confidence interval analysis reliable results can be achieved. A 8-bit 100MS/s pipelined ADC is realized to verify the algorithm. It is made of seven stages of 1.5-bit sub-converters and an 1-bit back end stage.

The proposed pipelined ADC and BIST circuit are designed using TSMC 1P6M $0.18um$ CMOS process with an active die area of $0.58mm \times 0.66mm$. In normal operation the peak SNDR is $47.09\,dB$ with the input signal frequency of $20.9Mhz$. The total power consumption of the proposed modulator is $110mW$. In BIST mode, with intentional mismatch added into stage one and stage two, gain errors can be estimated correctly. Finally the Matlab is used to correct the error.

Index Terms – pipelined ADC, BIST, 100 MS/s, confidence interval, probability.

誌謝

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Chapter 1

Introduction

1.1 Motivation

In order to take the advantage of digital technique, more and more signal are processed in digital domain. Analog to digital converter (ADC) is the bridge between our analog world and digital domain. Although the digital field extends greatly ADC can never be substituted. It has wild applications such as wireless communication system, cellar phone, digital video system, high speed modem, Ethernet system, and etc.

Different types of converters are developed for different specifications. In Figure 1-1 a sketch map of different architecture and requirement is presented. Among those converters pipelined ADCs provide good trade-off between sample rate, resolution, power, and chip area. With increasing resolution and speed, the error effects arise. It is believed that nonlinearity of pipelined stage gain induces most linearity problem of

entire converter. The stage gain error results from finite amplifier gain, capacitor mismatch, or accuracy of reference voltage. Some trimming or calibration techniques are used to deal with it. It is necessary for pipelined ADC over 12 bits resolution.

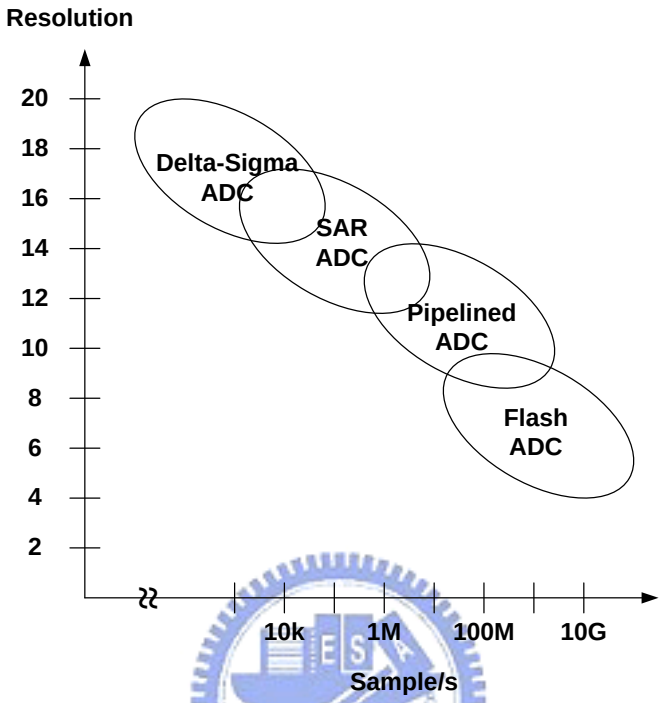


Figure 1-1 ADC architecture vs. speed and resolution

ADC testing can be categorized into two categories, dynamic testing and static testing. By sending single tone or multi-tone sinusoidal signal into ADC, dynamic testing includes signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), signal-to-noise and distortion (SINAD), and intermodulation distortion (IMD). By histogram method, static testing obtains integral nonlinearlity (INL) and differential nonlinearlity (DNL).

With regard to static testing, a new method is proposed for pipelined ADC. It uses of the structure property of a pipelined ADC. Linearity of the converter can be estimated with some simple digital circuit utilization. With the scaled technologies, the cost of additional digital circuit is decreased.

1.2 Thesis Organization

This thesis is organized into six chapters. In Chapter 1, this thesis and ADC application are briefly introduced. In Chapter 2, the fundamentals of pipelined ADC

are introduced. The effects of different errors are presented. Some of them can be ignored but others are not. Finally the development of 1.5-bit pipelined stage and its digital correction are introduced.

In Chapter 3, the concept of built-in self-test (BIST) is introduced with probability analysis. The essential accuracy requirement is also analyzed. Then whole architecture of BIST circuit is presented. It uses comparators of the next stage to scan previous stage. The calibration of the comparator become necessary although the pipelined ADC can tolerate large comparator offset originally. The calibration method is also introduced in this chapter. Triangular wave linearity and circuit are introduced. Finally the equation of off-chip correction is presented.

In Chapter 4, we design a 8-bit 100MS/s pipelined ADC to verify the BIST algorithm. The sample-and-hold (S/H) and multiplying digital-to-analog converter (MDAC) circuit is shown. The specification of the operational amplifier is analyzed. The bootstrapped switch is utilized. The bottom plate sampling technique is described. And the comparator and its Monte Carlo analysis are presented. The timing diagram of ADC is presented. Finally the clock generator circuit and its simulation result are presented.

In Chapter 5, all the simulation results are summarized in this chapter. In Chapter 6, the conclusions of this work are summarized.

Chapter 2

Fundamentals of Pipelined ADC

2.1 Introduction

Some of the fundament character of pipelined ADC will be reviewed in this chapter. The principles of pipelined ADC are presented in Section 2.2. Different kinds of stage transfer curve are shown here. In Section 2.3, the effects of error in pipelined stage are described [1][2]. Some of them aren't necessary to be deal with [3]. For example, nonlinearity of subADC induces decision level shift or offset error in a pipelined stage. In section 2.4, the development from 2-bit pipelined stage to 1.5-bit is introduced. At the same time the method and reasons for digital correction are presented.

2.2 The Principles of Pipelined ADC

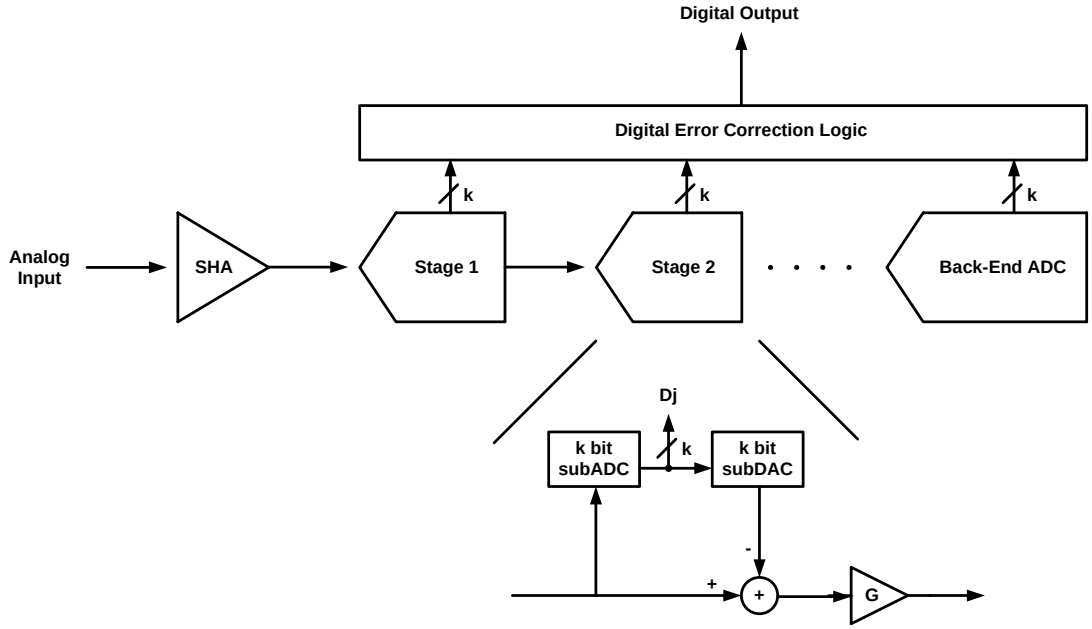


Figure 2-1 Structure of pipelined analog to digital converter

Figure 2-1 shows the block diagram of a pipelined ADC. It consists of a S/H, pipelined stages, and a digital correction circuit. Each stage except for the last stage includes a sub-analog-to-digital converter (subADC), a sub-digital-to-analog converter (subDAC), a subtracter, and a residue amplifier. The last stage just includes a subADC. The S/H samples analog signal and transfers it to the first pipelined stage. The subADC obtains a low resolution digital output. Then subtracting the held analog signal by the reconstructed analog signal from subDAC, the difference is amplified by the residue amplifier and sent to the next stage. The whole process can be treated as looking for a target on a map. In Figure 2-2 an area is located by the vertical and horizontal coordinates. In Figure 2-3 and Figure 2-4 the area is moved to the center and amplified to fit the coordinates. Then by using the same coordinates more accurate location can be specified. The subADC just represents the coordinates. The subtraction represents the operation of moving to the center. The residue amplifier performs the area enlargement. By this process the same coordinates can be used to locate a target more and more precisely. It is just the same as identical pipelined stages combination. In Figure 2-1 the MSB is specified from the first stage and the LSB is specified in the last stage. The operation of each stage can be divided into two phase,

sample phase and hold phase. When it is in the sample phase, it samples data from the previous stage. When it is in the hold phase it sends data to the next stage. Every adjacent stage must be in different phases. While S/H is receiving the new analog input the pipelined stages are processing previous data. With this character the pipelined ADC is well known for its high throughput.

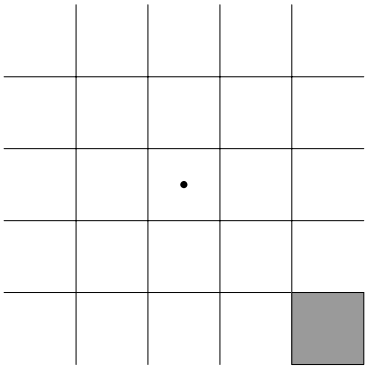


Figure 2-2 SubADC locate the target

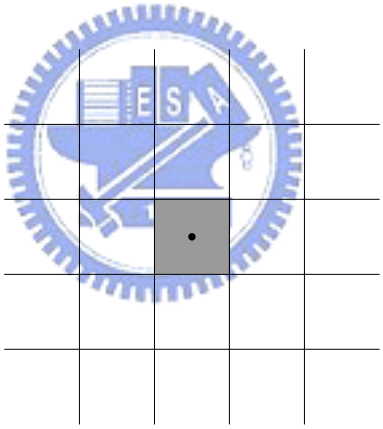


Figure 2-3 “subtraction” moves the target to the center

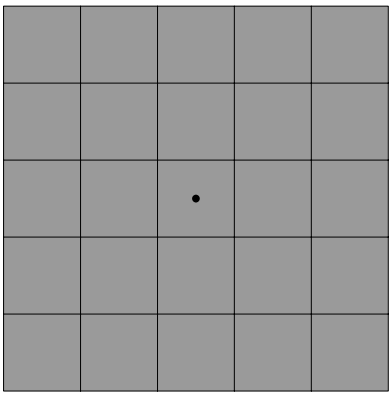


Figure 2-4 Residue amplifier enlarges the target

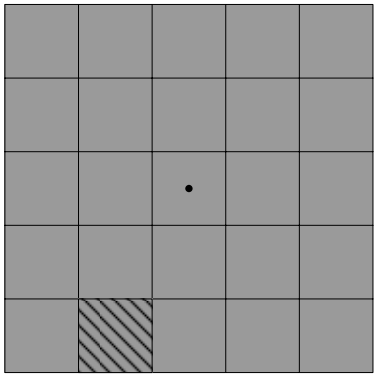


Figure 2-5 subADC of next stage “relocate” the target

There are a number of ways to define a single pipelined stage. They are the threshold levels of subADC, the digital codes, the corresponding subDAC levels, and the interstage gain. The interstage gain, G , can be any value greater than 1. Here shows some examples of pipelined stage transfer curve in Figure 2-6, Figure 2-7, and Figure 2-8 [4][5].

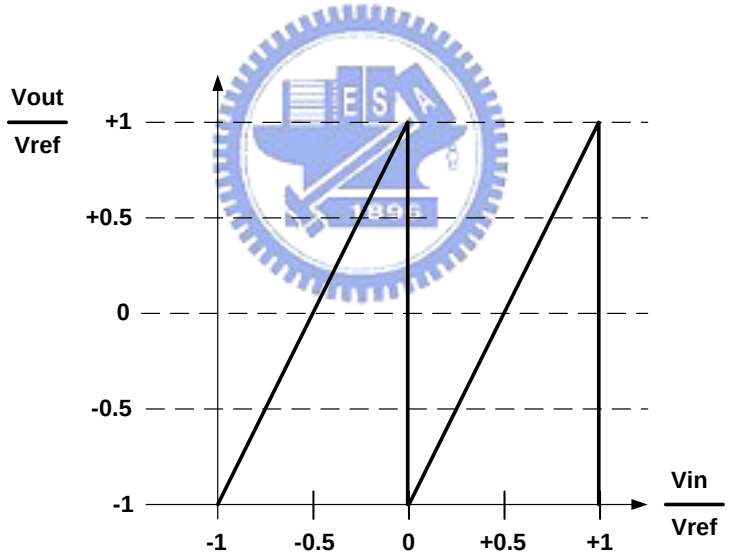


Figure 2-6 Ideal transfer curve of a 1-bit pipelined stage

Table 2-1 Static parameters of a 1-bit pipelined stage

input range	[-1,1]
subADC threshold levels	{0}
digital codes	{0 , 1}
subDAC levels	{-0.5 , +0.5}
interstage gain	G = 2
number of bits	k = 1

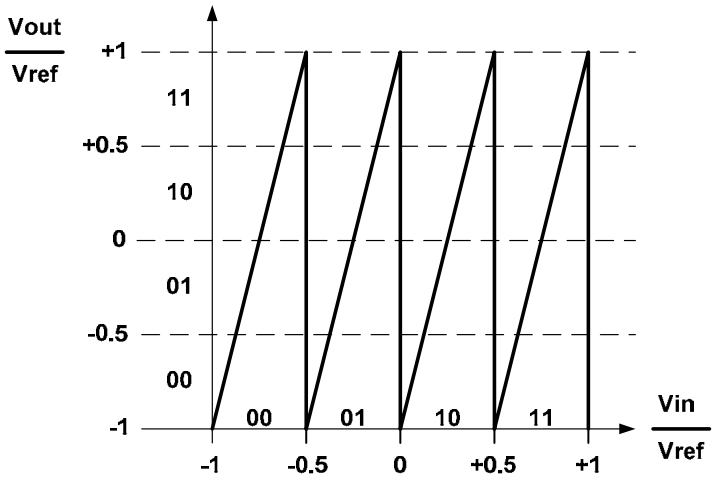


Figure 2-7 Ideal transfer curve of a 2-bit pipelined stage

Table 2-2 Static parameters of a 2-bit pipelined stage

input range	[-1,1]
subADC threshold levels	{-0.5 , 0 , +0.5}
digital codes	{00 , 01 , 10 ,11}
subDAC levels	{-0.5 , 0 , +0.5}
interstage gain	G = 4
number of bits	k = 2

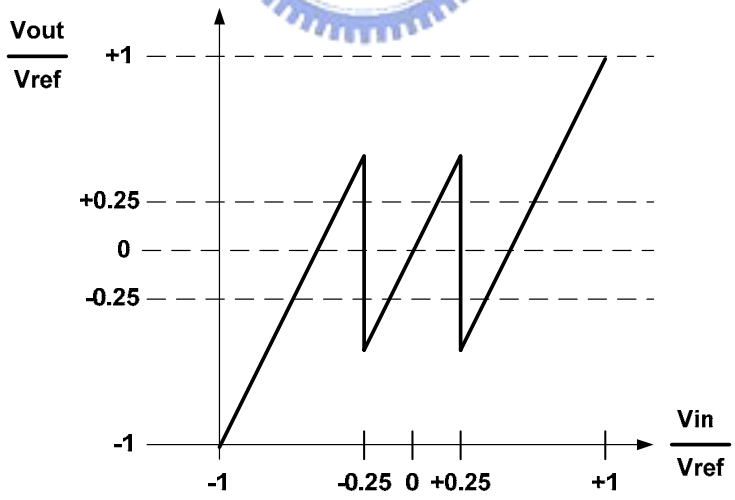


Figure 2-8 Ideal transfer curve of a 1.5-bit pipelined stage

Table 2-3 Static parameters of a 1.5-bit pipelined stage

input range	[-1,1]
subADC threshold levels	{-0.25 , +0.25}

digital codes	{00 , 01 , 10}
subDAC levels	{-0.5 , 0 , +0.5}
interstage gain	G = 2
number of bits	k = 2 (after digital correction k=1)

2.3 Errors in Pipelined ADC

2.3.1 Nonlinearity in SubADC

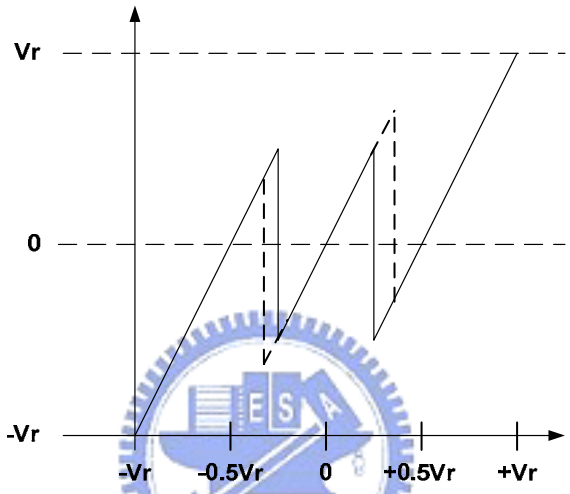


Figure 2-9 Ideal 1.5 bit/stage and decision level shift

The nonlinearity errors in subADC result in decision level movement shown in Figure 2-9 [6]. These errors induce wrong output code in a single stage. However a digital error correction technique is developed to deal with this problem. As long as the output values within the input range of the next stage, the digital code error can totally be restored. The details on digital error correction will be described in section 2.4.

2.3.2 Offset error in SubDAC

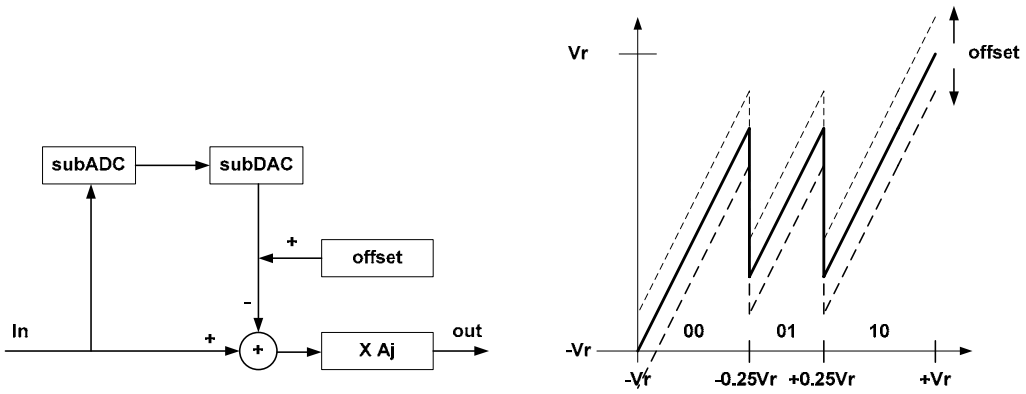


Figure 2-10 Ideal 1.5 bit/stage and offset error in subDAC

The offset in subDAC is equivalent to horizontal movement in the transfer curve shown in Figure 2-10 [7]. Moreover the stage offset error can be equivalently included in this part. The equation of the transfer curve can be expressed as

$$V_{j+1} = \left(V_j - V_j^{DA} - V_j^{OS}\right) \cdot A_j \tag{2-1}$$

or

$$V_j = \frac{V_{j+1}}{A_j} + V_j^{DA} + V_j^{OS}. \tag{2-2}$$

An ADC with L pipelined stages can be expressed as

$$V_1 = V_1^{DA} + \frac{V_2^{DA}}{A_1} + \frac{V_3^{DA}}{A_1 A_2} + \cdots + \frac{V_L^{DA}}{A_1 A_2 \cdots A_{L-1}} + \frac{V_{L+1}}{A_1 A_2 \cdots A_{L-1}} + OS \tag{2-3}$$

$$OS = V_1^{OS} + \frac{V_2^{OS}}{A_1} + \frac{V_3^{OS}}{A_1 A_2} + \cdots + \frac{V_L^{OS}}{A_1 A_2 \cdots A_{L-1}}.$$

It shows that the offset error in subDAC only contributes to the offset error of entire ADC. It can be easily removed in system level. So the effect can be ignored.

2.3.3 Gain Error in residue amplifier

The residue amplifier is implemented by switch capacitor (SC) circuit and operational amplifier (OP). The gain error mainly results from the finite gain of the OP and mismatch in capacitors. It changes the slope of stage transfer curve [8]. In Figure 2-11 shows the residue transfer curve when the interstage gain is greater than two. Stage gain error contributes to linearity problem of entire ADC. In Figure 2-12

the transfer curve of entire ADC is presented [9]. Assume the first stage has gain error (>0) and others are ideal. Figure 2-13 and Figure 2-14 show the opposite cases. In practical designs, all stages suffer from non-ideal interstage gain error. That decreases the linearity and resolution of the ADC seriously. A lot of calibration methods are developed to cancel the effect especially for high resolution pipelined ADCs.

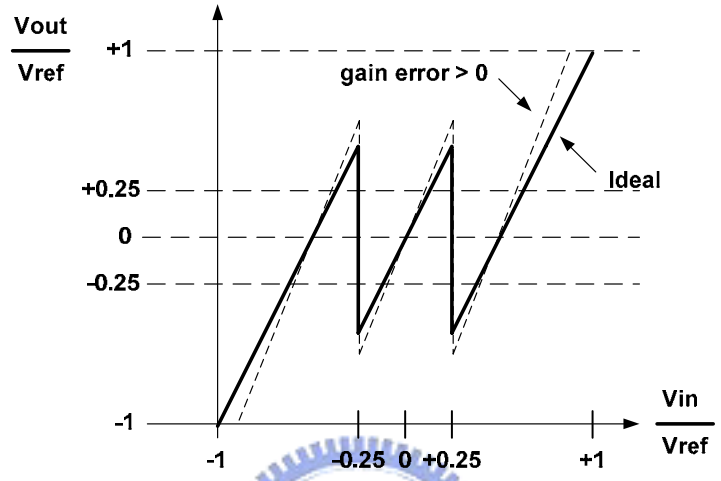


Figure 2-11 Transfer curve of 1.5 bit/stage with gain error (>0)

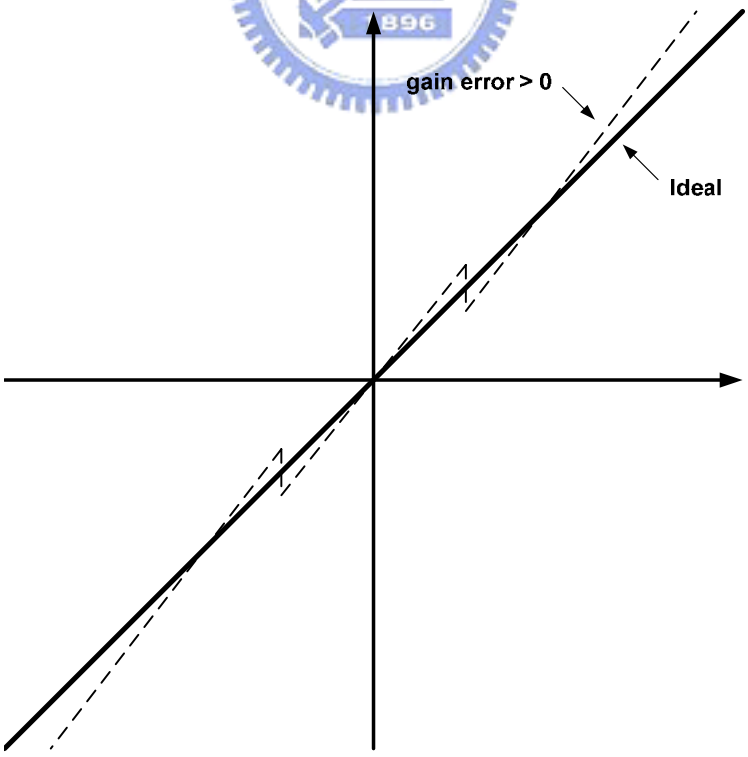


Figure 2-12 Transfer curve for 1.5 bit/stage pipelined ADC when interstage gain >2

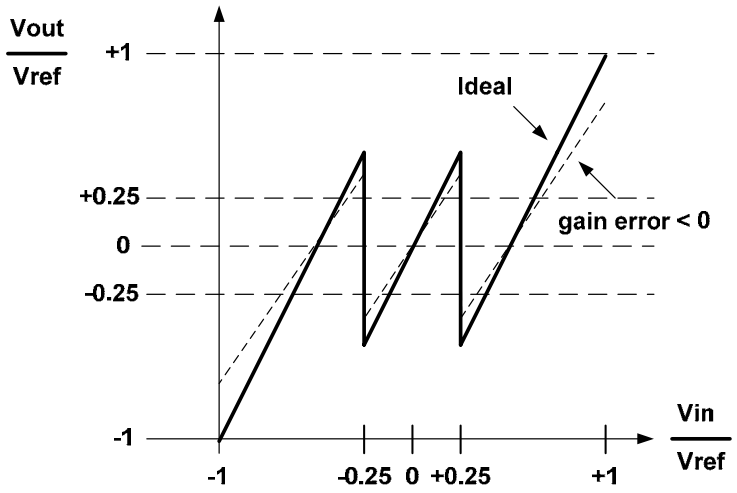


Figure 2-13 Transfer curve of 1.5 bit/stage with gain error (<0)

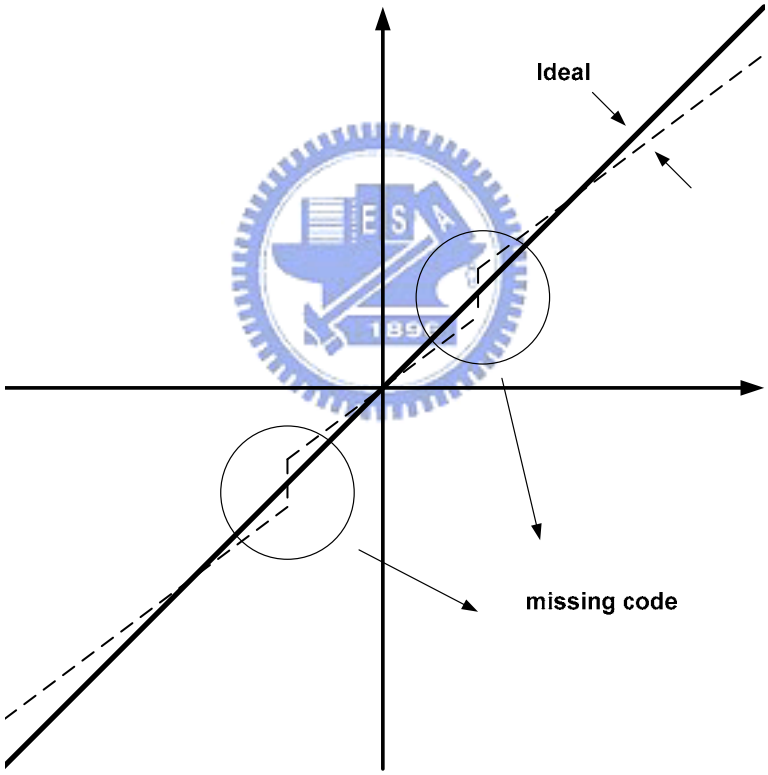


Figure 2-14 Transfer curve for 1.5 bit/stage pipelined ADC when interstage gain <2

2.4 Digital Error Correction

Digital error correction is developed to correct the error due to decision level shift in a pipelined stage. This effect results from the nonlinearity of subADC. With

this method, the cost is reduced by not generating precise decision levels. The correction range is defined under the condition that the decision level movement can be tolerated without error. In Figure 2-15, apparently the offset of subADC within $\pm 0.25Vr$ will not saturate the next stage. Then $\pm 0.25Vr$ is the correction range of a 1.5-bit pipelined stage.

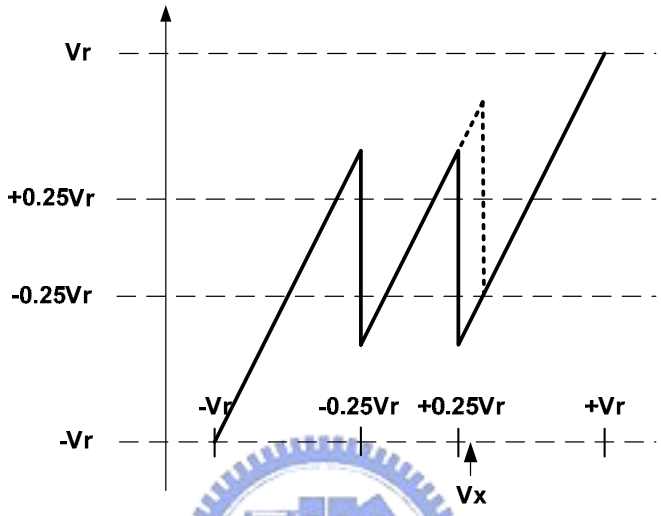


Figure 2-15 A 1.5-bit pipelined stage transfer curve with decision level shift

Here shows an example of digital error correction. In Figure 2-15, there is an ideal 1.5-bit pipelined stage transfer curve and the decision level offset of +0.25Vr as the dotted line goes. An input V_X is applied into a stage. The correction is performed with one bit overlapped addition in Figure 2-16. The ideal digital output eventually is identical to the corrected one.

Ideal	decision level shift
10	01
+ 00	+ 10
100	100

Figure 2-16 Digital correction performed

Let's see a 2bit pipelined stage transfer curve in Figure 2-17 to explain the origin of the digital correction [10].

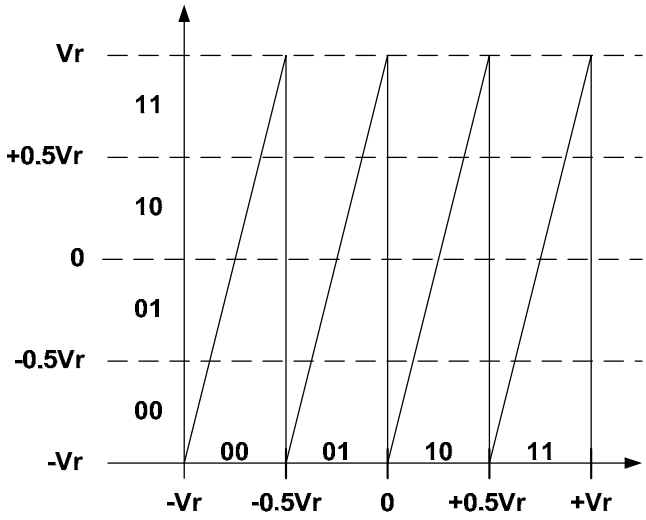


Figure 2-17 A ideal 2 bit/stage transfer curve

Apparently, any decision level shift in sub ADC would saturate the next stage. This results in unrecovered error in digital output. There are two methods to deal with this problem. The first, one is to increase the numbers of comparators. It causes the increase of the input range of the next stage. If the next stage is not saturated, the ADC can work normally in the following stages. Some digital circuit is needed for additional comparators. The second, instead of increasing comparator number, a modified transfer curve is shown in Figure 2-18 with reduced stage gain by a factor of two.

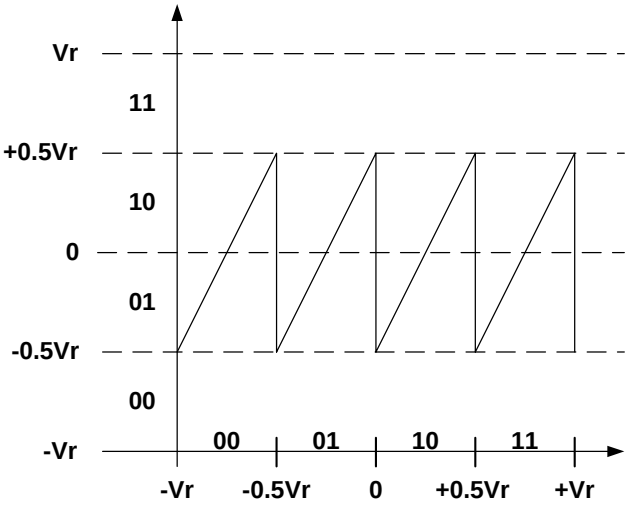


Figure 2-18 Transfer curve of 2 bit/stage with reduced stage gain

The curve with reduced gain allows the subADC has "margin" of offset without saturation in the next stage. Since the stage gain is reduced by two, the weight of the next stage digital output is increased by a factor of two. This is the reason why the correction is performed by an addition with one bit overlapped between adjacent stages. The reduction in stage gain also means the reduction in stage resolution. The cost is that more stages are needed to achieve the same resolution.

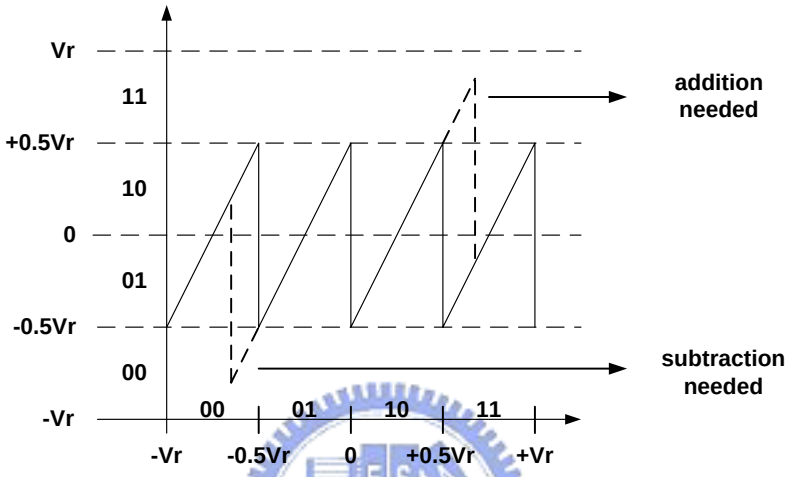


Figure 2-19 Transfer curve of reduced stage gain and decision level shift cases

When the decision level moves to the left in Figure 2-19, the correction obviously must be done with a subtraction [11]. When it moves to the right, an addition is needed. In order to reduce the design complexity of digital correction circuit, the subtraction is removed by modifying the transfer curve. A 0.5LSB offset (a 2-bit stage resolution) is introduced into the subADC and removed in subDAC. That shifts the transfer curve to the right by 0.5LSB as shown in Figure 2-20. It also changes the reconstructed analog signal from subDAC by 0.5LSB.

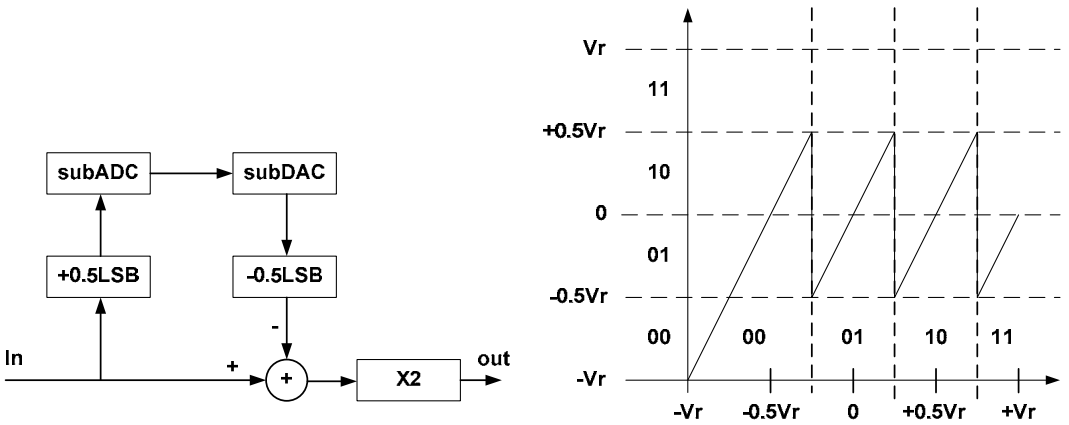


Figure 2-20 Transfer curve of reduced stage gain and intentionally shift to the right

One can compare Figure 2-20 with Figure 2-17. On the condition that the decision level shifts within $\pm 0.25Vr$, the digital output is always less than or equal to the original digital output in Figure 2-17. That means the subtraction is needless as shown in Figure 2-21.

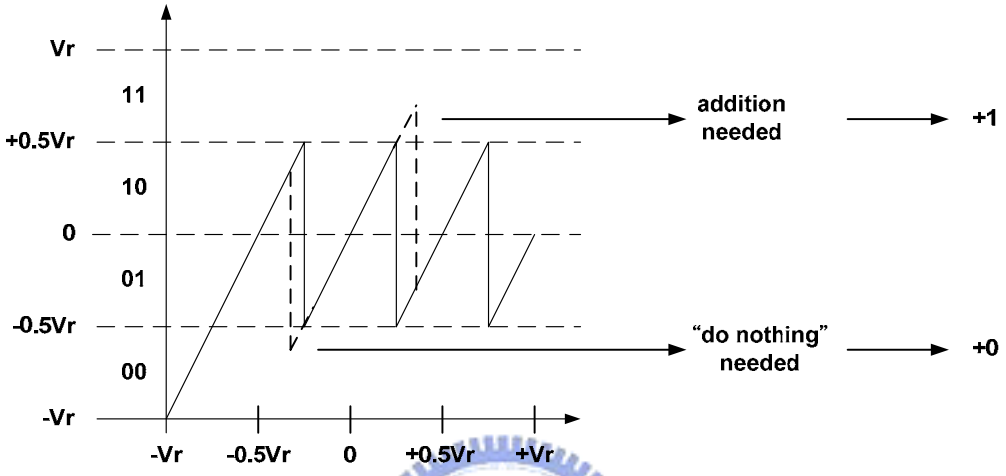


Figure 2-21 Shift to right transfer curve and decision level shift cases

Removing the top comparator increases the testability of the correction logic but not the maximum magnitude. The new transfer curve is shown in Figure 2-22 as standard 1.5-bit pipelined stage. The correction is performed as in Figure 2-16.

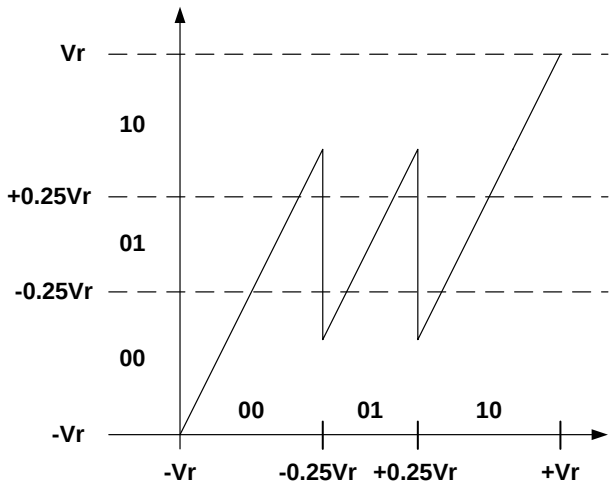


Figure 2-22 Ideal 1.5 bit/stage transfer curve

Chapter 3

The BIST Architecture

3.1 Introduction

In this chapter, the concept and realization of the BIST circuit is presented. We introduce the basic self test idea in Section 3.2. In Section 3.3, the probability in transfer curve is introduced. In Section 3.4, to achieve expected accuracy the confidence interval analysis is presented. The BIST circuit architecture is introduced in Section 3.5. The comparator is an important element in BIST circuit. Its offset calibration is presented in Section 3.6. The stimulation (triangular wave) linearity requirement and circuit are introduced in Section 3.7 and 3.8. After the probability analysis, the error in transfer curve is transformed into the result of counter. The table of gain error and corresponding counter result is presented in Section 3.9. Finally the mathematical description of correction is discussed in Section 3.10.

3.2 BIST Introduction

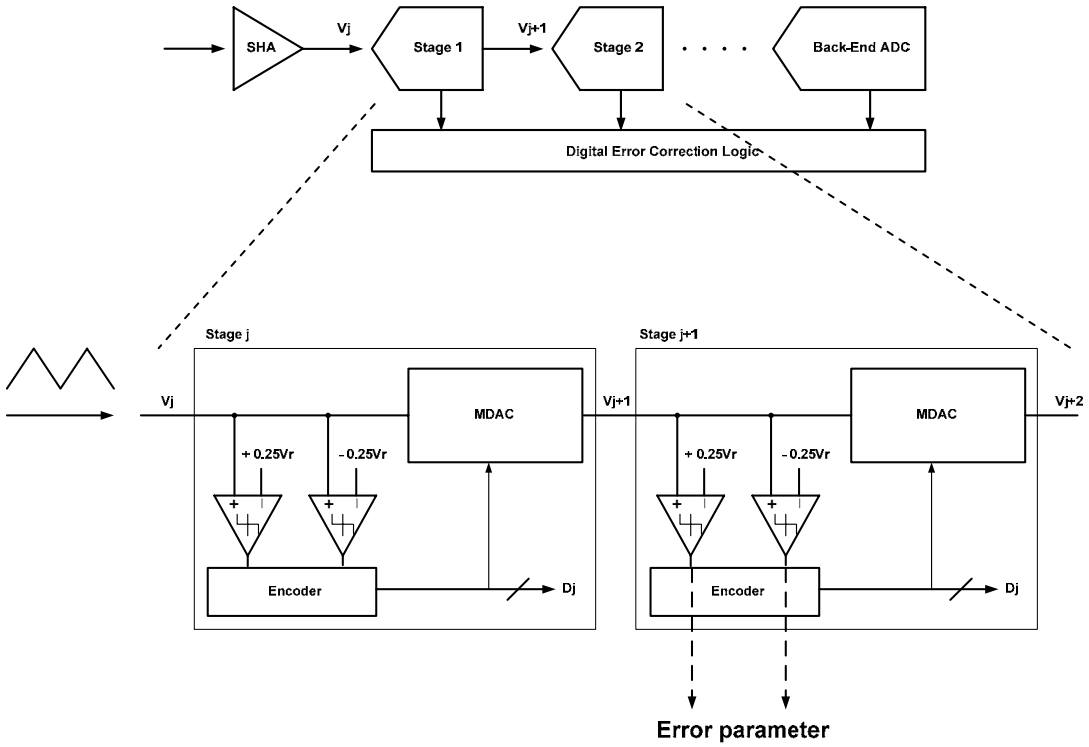


Figure 3-1 Structure of two adjacent stages

Observing the adjacent pipelined stages in Figure 3-1, the comparators of the next stage may be used as the test element to test the current stage. Scanning the transfer curve of the previous stage, the question becomes the relation between the scan results and the parameters that we interested in. In the next section, the probability analysis is presented and the relation is realized.

3.3 Probability Analysis of the Errors

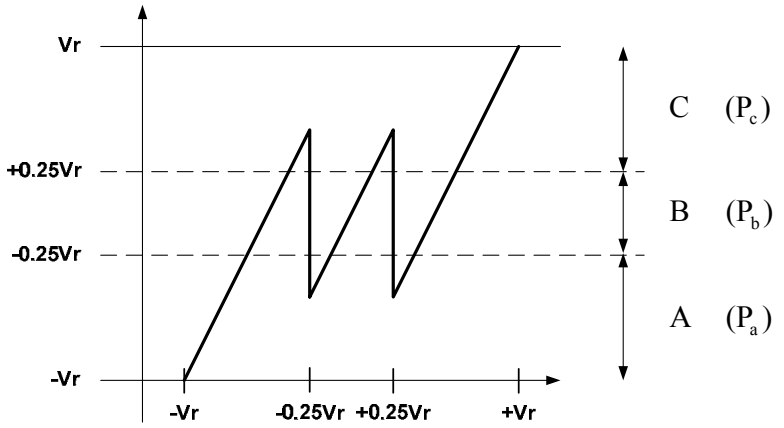


Figure 3-2 Ideal 1.5 bit/stage transfer curve and ideal probability distribution

In Figure 3-2, if a ramp signal from $-V_r$ to $+V_r$ is sent to an ideal 1.5-bit pipelined stage, P_a, P_b ,and P_c of three regions, A B and C, can be obtained from the stage output individually. Region A, B, and C are defined by the next stage comparators, $\pm\frac{V_{ref}}{4}$. Assume S represents the entire sample space. They are described below as an ideal case.

$$S = \frac{1.5}{4} + \frac{1}{4} + \frac{1.5}{4} = 1. \tag{3-1}$$

$$P_a = P_c = \frac{\left(\frac{0.5-0.25}{4}\right)\times 3 + \frac{0.5}{4}}{S} = \frac{1.25}{4} = 0.3125. \tag{3-2}$$

$$P_b = \frac{\frac{0.5}{4}\times 3}{S} = \frac{1.5}{4} = 0.375. \tag{3-3}$$

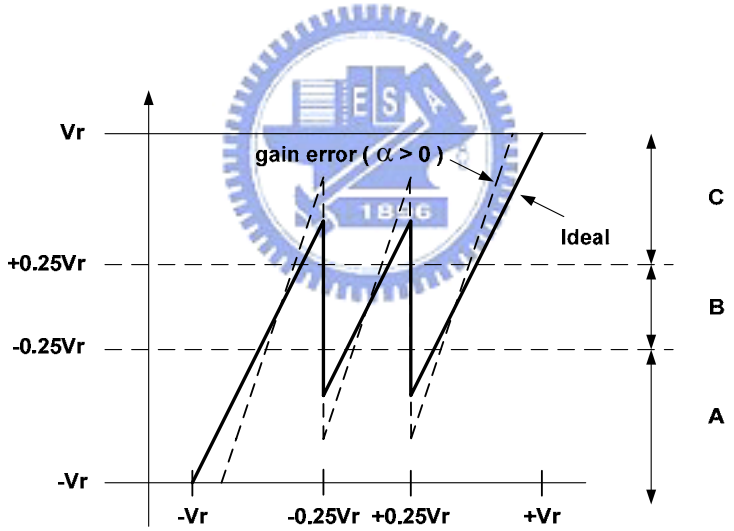


Figure 3-3 Ideal 1.5 bit/stage transfer curve and gain error (>0)

In Figure 3-3, when it comes to gain error case $P_a^{'}$, $P_b^{'}$ and $P_c^{'}$ represent new probability distribution in three region. Assuming $\alpha > 0$, the increase of probability in region A and C would be the same, but decrease twice in region B. Expressing as

$$P_a^{'} = P_a + y_b \qquad P_b^{'} = P_b - 2y_{b'} \qquad P_c^{'} = P_c + y_b. \tag{3-4}$$

From (3-3) , we have

$$P_b^{'} = \frac{\frac{0.5}{4} \times 3}{(1+\alpha) \times S}. \tag{3-5}$$

(3-3) divided by (3-5) obtains

$$\frac{P_b}{P_b^{'}} = 1+\alpha. \tag{3-6}$$

Rearranging (3-6), we obtain

$$\alpha = \frac{P_b - P_b^{'}}{P_b}. \tag{3-7}$$

The gain error α can be solved by probability shift from the ideal one.

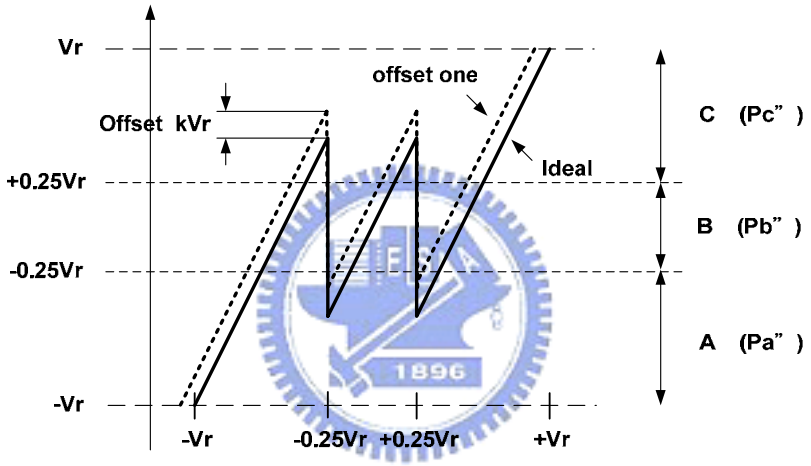


Figure 3-4 Ideal 1.5 bit/stage transfer curve and offset error

By a similar method, the offset error can be estimated. Figure 3-4 shows the transfer curve with an offset error. Assume $k > 0$, in a reasonable condition the probability decrease and increase of region A and C are the same in magnitude. The probability in B will not be affected. The offset estimation can be done from region A or C. Take probability in C for example, the variation is expressed as

$$\Delta P_c = P_c^{''} - P_c = \frac{\frac{1.25}{4} + \frac{3 \cdot k}{4}}{Set_{all}} - \frac{\frac{1.25}{4}}{Set_{all}} = \frac{3k}{4 \cdot Set_{all}}. \tag{3-8}$$

The offset is

$$k = \Delta P_c \cdot Set_{all} \cdot \frac{4}{3}. \tag{3-9}$$

3.4 Sample Number Analysis

From the previous section, the relationship between errors and output probability variation is defined. That means the accuracy of error estimation is dependent of the accuracy of the probability. The question comes to how many samples are necessary. Here, confidence interval analysis is required [12].

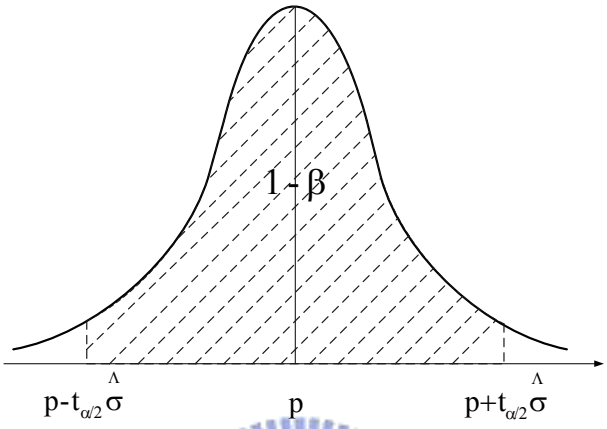


Figure 3-5 The error estimated probability distribution

It is reasonable to assume that the estimated probability is a normal distribution presented in Figure 3-5. The distribution is centered at p, the correct value of the estimated probability. While $\hat{p}$ represents the real probability we estimated the standard deviation, $\hat{\sigma}$, is expressed as

$$\hat{\sigma} = \frac{\sqrt{\hat{p}(1-\hat{p})}}{\sqrt{n}}. \tag{3-10}$$

The confidence interval equation is given by

$$P\left(\hat{p} - t_{\alpha/2} \cdot \hat{\sigma} \le p \le \hat{p} + t_{\alpha/2} \cdot \hat{\sigma}\right) = 1-\beta, \tag{3-11}$$

or

$$P\left(p - t_{\alpha/2} \cdot \hat{\sigma} \le \hat{p} \le p + t_{\alpha/2} \cdot \hat{\sigma}\right) = 1-\beta. \tag{3-12}$$

(3-12) represents that there is $100 \cdot (1-\beta)\%$ confidence about the real probability, $\hat{p}$. The real probability would be $\pm t_{\alpha/2} \cdot \hat{\sigma}$ around correct probability

p. $t_{\alpha/2} \cdot \overset{\Lambda}{\sigma}$ results from test uncertainty or non-ideal test circuit. As $t_{\alpha/2} \cdot \overset{\Lambda}{\sigma}$ being small enough, $\overset{\Lambda}{p}$ can represents correct p . Defining $t_{\alpha/2} \cdot \overset{\Lambda}{\sigma}$ as

$$\Delta p = t_{\alpha/2} \cdot \overset{\Lambda}{\sigma}. \tag{3-13}$$

From (3-3) and (3-7), we obtain

$$\alpha = \frac{1.5}{4 \cdot \overset{\Lambda}{p}} - 1. \tag{3-14}$$

The expression between α and $\overset{\Lambda}{p}$ can be extended to

$$\alpha + \Delta\alpha = \frac{1.5}{4 \cdot \left(\overset{\Lambda}{p} + \Delta p \right)} - 1. \tag{3-15}$$

The additional gain error $\Delta\alpha$ is from Δp .

From (3-14) and (3-15) $\Delta\alpha$ can be express as

$$\Delta\alpha = \frac{1.5}{4}\left(\frac{1}{\overset{\Lambda}{p} + \Delta p} - \frac{1}{\overset{\Lambda}{p}} \right) = \frac{1.5}{4}\left(\frac{\Delta p}{\left(\overset{\Lambda}{p} + \Delta p \right) \cdot \overset{\Lambda}{p}} \right) \underset{p >> \Delta p}{\overset{\Lambda}{\approx}} \frac{1.5}{4} \cdot \frac{\Delta p}{\overset{\Lambda}{p}^2}. \tag{3-16}$$

From Matlab analysis, a 8-bit pipelined ADC would cause linearity problem if gain error of a pipelined stage be greater than 0.005. So the error tolerance is the value of 0.001. That means $\Delta\alpha \le 0.001$ .Using (3-10), (3-13), and (3-16) we have

$$\frac{1.5}{4} t_{\alpha/2} \frac{\sqrt{\overset{\Lambda}{p}(1 - \overset{\Lambda}{p})}}{\sqrt{n \overset{\Lambda}{p}^2}} \le 0.001. \tag{3-17}$$

For simplicity, let us take the correct value p to replace $\overset{\Lambda}{p}$. For a 99% confidence level, $t = 2.58$, we have

$$n \ge 8970666 . \tag{3-18}$$

As long as the sample number is larger than this value, we have 99% confidence that the differance between the measured gain error and the correct one is smaller than 0.001 . In circuit design, we use a 25-bit counter to ensure this sample number.

3.5 BIST Architecture

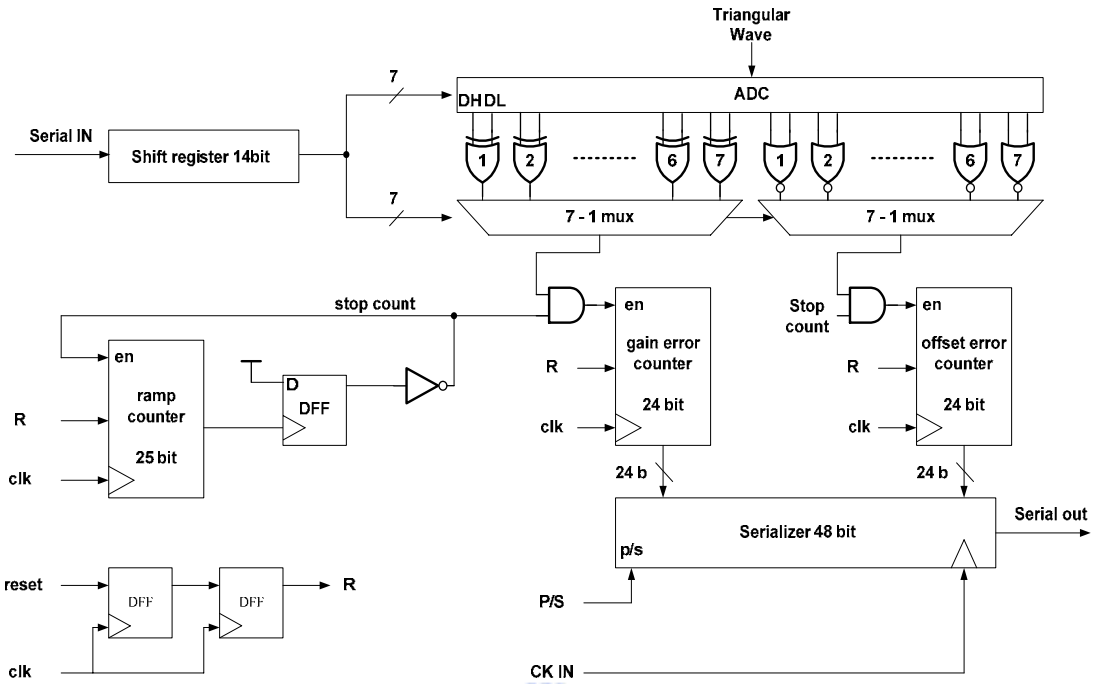


Figure 3-6 BIST circuit architecture

Figure 3-6 shows the architecture of BIST circuit. It consists of a shift registers, three asynchronous counters, two 7-1 multiplexeres (MUX), and a serializer. The 14-bit shift register is used to decide which stage's transfer curve should be scanned. Seven bits of the shift register, sel1~sel7 in Figure 3-7, control where the triangular wave goes to, and other seven bits control two 7-1 MUXes. Two 7-1 MUXes receive error data from the stages and transfer the data to the

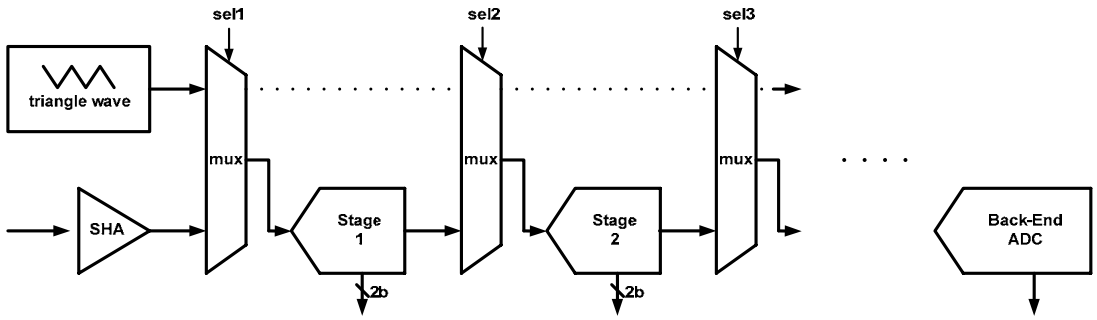


Figure 3-7 MUXs between pipelined stages

two error counters. XOR gate is used to trigger gain error counter while the stage

output code falls in region B. NOR gate is used to trigger the offset error counter while the stage output code belongs in region A. A 25-bit counter is used to make sure that 2^{24} samples are sent to the stage under test [13]. The other two 24 bit counters count gain and offset errors individually. Finally a 48-bit serializer is used to send the result out of chip for reducing output pad numbers. It is shown in Figure 3-8 [14].

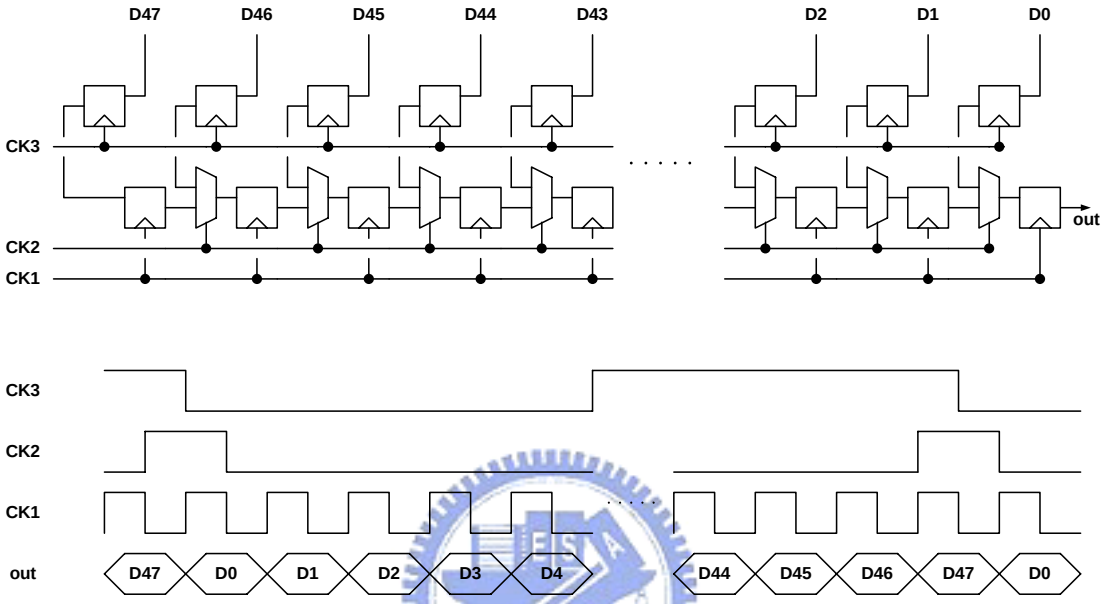


Figure 3-8 Shift-register type serializer

We use reset pin to switch operation mode. When reset = 0, ADC is in normal operation made that converts analog signal to digital code. When reset=1, circuit become in BIST mode described below. First the stage under test information is assigned into 14-bit shift register from outside. Reset pin is set from high to low to reset all counters. Then triangular wave signal is sent into the stage. Error counters start counting. After ramp counter counts 2^{24} samples. Error counters stop counting. Gain error and offset error parameters are loaded into 48-bit serializer and then sent to logic analyzer through serial output pin.

3.6 Comparator Offset Calibration

Once it is decided to utilize comparator to estimate errors, comparator offset become a serious problem that will affect error detection result directly. But this problem can be solved easily with the original BIST circuit. In Figure 3-1, when the triangular wave is sent into stage j, error counter reads error parameter from stage j

instead of stage j+1. By analyzing probability in three regions, the value of comparator offset is understood.

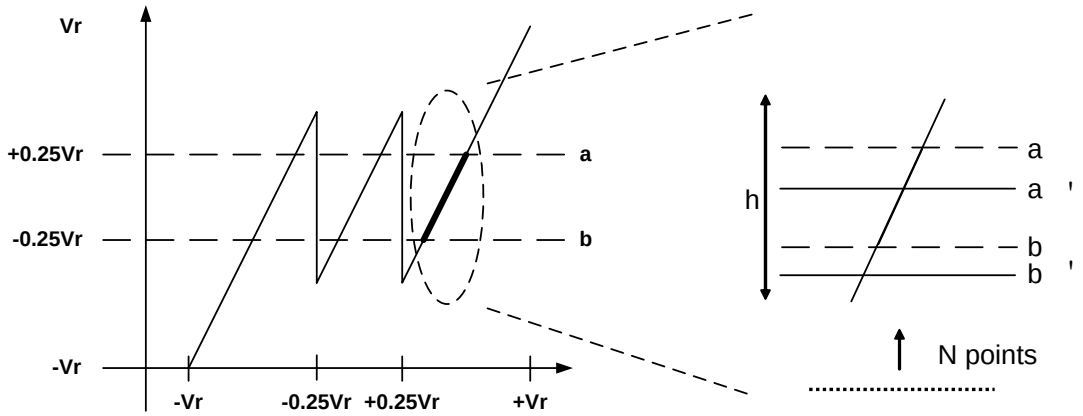


Figure 3-9 Example of comparator offset

Here is a calibration example of the gain error. In Figure 3-9, a and b are ideal comparator value. Because of offset, a moves to a' and b moves to b'. Offset Calibration is done by

$$Correct\ error\ count = Original\ error\ count + \frac{\overline{aa'}}{h} \times N - \frac{\overline{bb'}}{h} \times N . \qquad (3\text{-}19)$$

3.7 Triangular Wave Generator Linearity

Take advantage of random sample the start or stop point of the ramp can be ignored. Just make sure enough sample numbers are taken. However the linearity of the triangular wave is important.

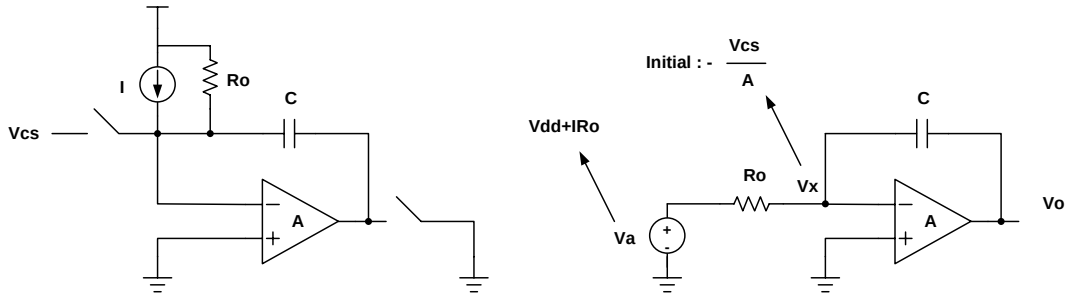


Figure 3-10 Simplified triangular wave generator circuit and the Thevenin equivalent

Figure 3-10 shows a simplified triangular wave generator [15]. And the Thevenin equivalent is shown. Open loop gain of the amplifier is A. Current source output impedance is R_o. From Figure 3-10

$$V_o = -2AV_x, \tag{3-20}$$

$$V_x = V_a - \left(V_a + \frac{V_{cs}}{A}\right) \cdot e^{\frac{t}{R_o C(1+A)}}. \tag{3-21}$$

Substituting (3-20) into (3-21) gives

$$-\frac{t}{R_o C(1+A)} = ln\left[\frac{V_a + \frac{V_o}{2A}}{V_a + \frac{V_{cs}}{2A}}\right] = ln\left[\frac{AV_a + V_o}{2AV_a + 2V_{cs}}\right]. \tag{3-22}$$

Rearranged

$$t(V_o, A) = ln\left[\frac{AV_a + V_o}{2AV_a + 2V_{cs}}\right]^{-\frac{1}{R_o C(1+A)}}. \tag{3-23}$$

"t" is function of output voltage and amplifier gain.

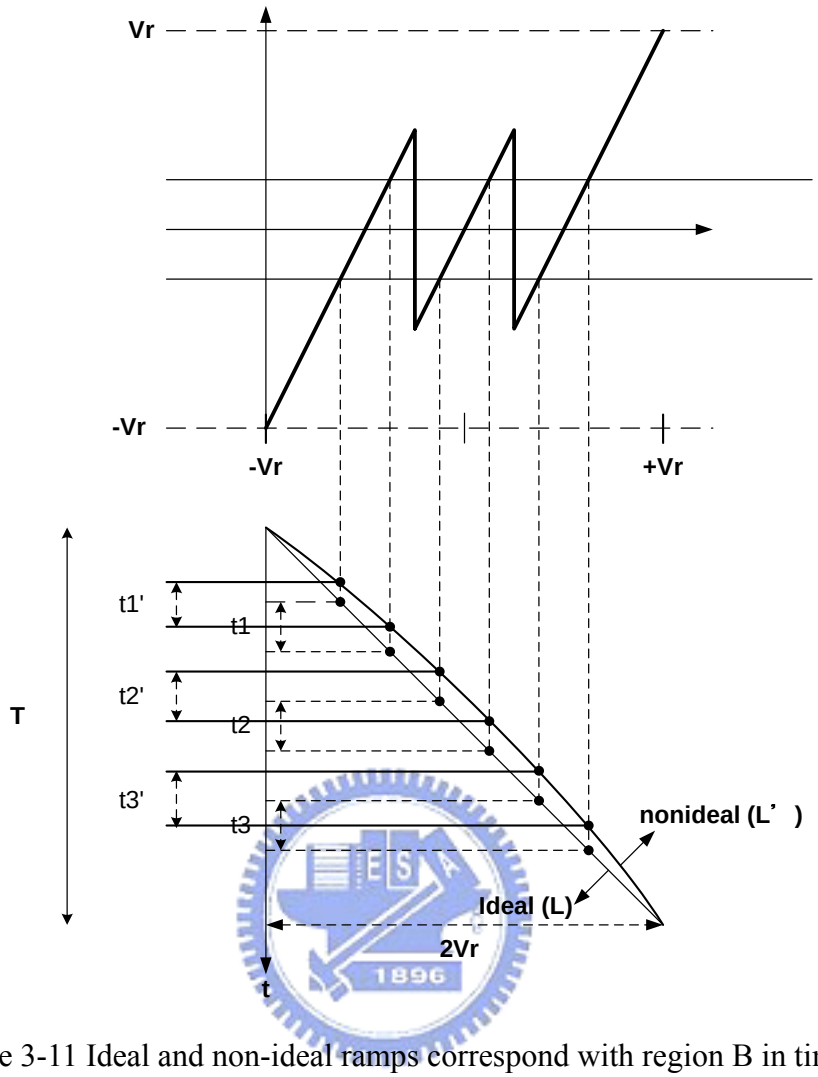


Figure 3-11 Ideal and non-ideal ramps correspond with region B in time

Send a ramp from $-V_r$ to $+V_r$ into the stage in a period of T. L represents the ideal curve and L' is the nonlinear one. Three time periods in region B in Figure 3-11, $t1\ t2\ t3$, correspond to L curve, and periods, $t1'\ t2'\ t3'$, correspond to L' curve. We can write the probability of the ideal curve L in region B.

$$P = \frac{t_1 + t_2 + t_3}{T} = \frac{3}{8}. \tag{3-24}$$

Nonlinear L' induces probability change. Expressing as

$$P + \Delta P = \frac{t_1' + t_2' + t_3'}{T}. \tag{3-25}$$

Substitute (3-23) into $t1'\ t2'\ t3'$

$$P+\Delta P=\frac{\left[t\left(-\frac{3V_r}{8}\right)-t\left(-\frac{5V_r}{8}\right)\right]+\left[t\left(\frac{V_r}{8}\right)-t\left(-\frac{V_r}{8}\right)\right]+\left[t\left(\frac{5V_r}{8}\right)-t\left(\frac{3V_r}{8}\right)\right]}{t(V_r)-t(-V_r)}$$

$$=\frac{ln\left[\frac{AV_a-\frac{3V_r}{8}}{AV_a-\frac{5V_r}{8}}\times\frac{AV_a+\frac{V_r}{8}}{AV_a-\frac{V_r}{8}}\times\frac{AV_a+\frac{5V_r}{8}}{AV_a+\frac{3V_r}{8}}\right]}{ln\left[\frac{AV_a+V_r}{AV_a-V_r}\right]}. \quad (3\text{-}26)$$

From (3-24) and (3-26) with $\Delta P<0.001$, $I=6uA$, $T=1.28us$ and $C=10\,p$ gives

$$A>60\,dB\,. \quad (3\text{-}27)$$

3.8 Triangular Wave Generator Circuit

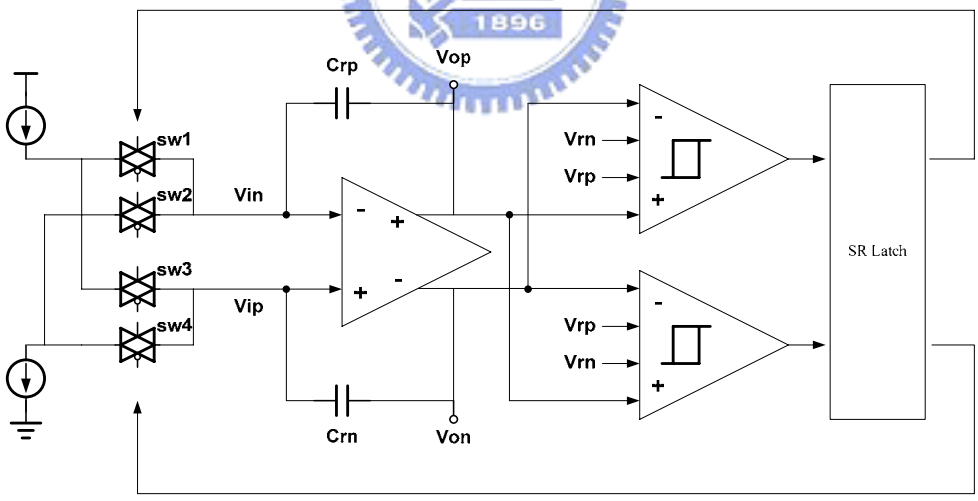


Figure 3-12 Triangular wave generator circuit

In Figure 3-12, the triangular wave generator circuit is presented [16]. The OP is same as being used in ADC. The high gain of OP ensures output linearity. Capacitors, C_{rp} *and* C_{rn} , are discharged before starting the BIST mode by short V_{ip}, V_{in}, V_{op}, *and* V_{on} to common mode voltage. The threshold voltages of

comparators are $\pm 1.6\,v$. When output voltage arrives at $+1.6\,v$ or $-1.6\,v$, charge and discharge paths exchange. Then output voltage starts to ramp down or up. Cascade current source is used to increase the output impedance and presented in Figure 3-13. The current sources are designed in the value of $6.2\,\mu A$. For slowly ramping up and down C_{rp} and C_{rn} in Figure 3-12 are selected in the value of $10\,pF$. The triangular simulated waveform is shown in Figure 3-14. It has a swing of $\pm 1.6\,v$ and a duty cycle of $2.57\,us$.

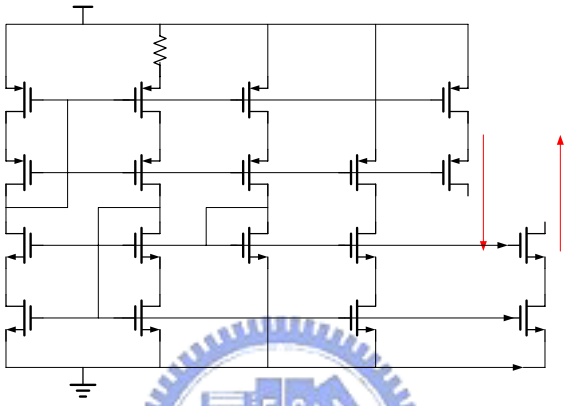


Figure 3-13 Constant gm current source

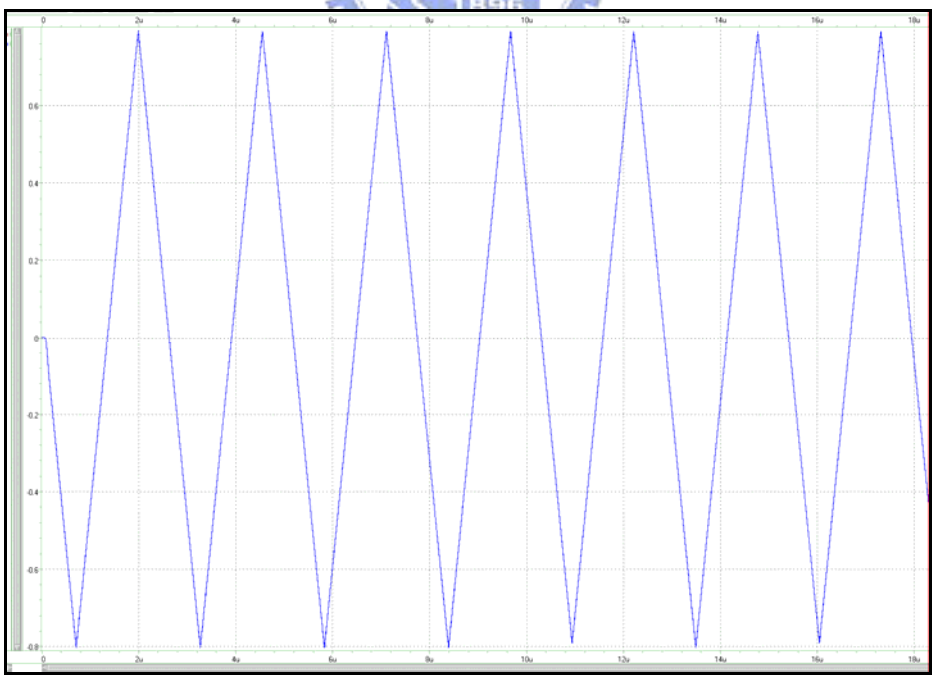


Figure 3-14 Simulation result of triangular wave

3.9 Error Count Reference (Matlab Simulation)

By counting the sample number in region B of all stages, the linearity of ADC can be analyzed. Here shows INL errors due to gain error in the single stage (other stages are ideal) and the corresponding sample numbers. For the ideal case without gain error, it should be *6291456* .

Table 3-1 INL due to first stage gain error (>0)

	S1	S2	S3	S4	S5	S6
INL=0.5	0.006	0.011	0.022	0.047	0.109	0.322
INL=1	0.011	0.022	0.046	0.099	0.248	1
INL=1.5	0.017	0.033	0.07	0.157	0.429	3
INL=2	0.022	0.045	0.095	0.221	1	-

Table 3-2 Corresponding sample number with gain error (>0)

	S1	S2	S3	S4	S5	S6
INL=0.5	6253932	6223003	6156023	6009032	5673089	4759044
INL=1	6223003	6156023	6014776	5724710	5041231	3145728
INL=1.5	6186289	6090470	5879865	5437732	4402698	1572864
INL=2	6156023	6020532	5745622	5152708	3145728	-

Table 3-3 INL due to first stage gain error (<0)

	S1	S2	S3	S4	S5	S6
INL=0.5	-0.006	-0.011	-0.021	-0.043	-0.09	-0.2
INL=1	-0.011	-0.021	-0.041	-0.083	-0.166	-0.332
INL=1.5	-0.016	-0.032	-0.064	-0.13	-0.272	-0.6
INL=2	-0.021	-0.041	-0.083	-0.167	-0.333	-

Table 3-4 Corresponding sample number with gain error (<0)

	S1	S2	S3	S4	S5	S6
INL=0.5	6329433	6361432	6426411	6574144	6913688	7864320
INL=1	6361432	6426411	6560434	6860912	7543712	9418347
INL=1.5	6393756	6499438	6721641	7231559	8642110	15728640
INL=2	6426411	6560434	6860912	7552768	9432468	-

3.10 Correction

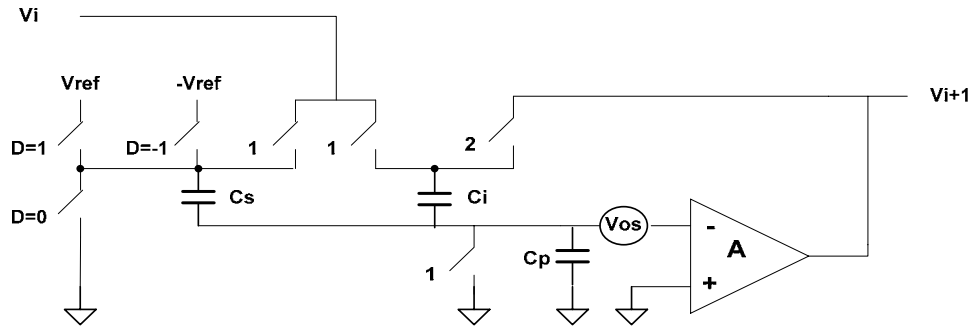


Figure 3-15 Simplified MDAC circuit

With the estimated error parameter, the correction is feasible to remove the error. A simplified MDAC with input offset is shown in Figure 3-15 [17]. Its transfer function is expressed as ($C_{tot} = C_i + C_s + C_p$)

$$V_{i+1} = \frac{C_i + C_s}{\frac{C_{tot}}{A} + C_i} V_i - \frac{C_s}{\frac{C_{tot}}{A} + C_i} \cdot D \cdot V_{ref} + \frac{C_{tot}}{\frac{C_{tot}}{A} + C_i} V_{os} . \tag{3-28}$$

If $A >> 1$, (3-28) can be rewrote as

$$V_{i+1} = \frac{C_i + C_s}{C_i} V_i - \frac{C_s}{C_i} \cdot D \cdot V_{ref} + \frac{C_{tot}}{C_i} V_{os} . \tag{3-29}$$

For a 1.5-bit pipelined stage, capacitors C_i and C_s should be identical ideally. Assume $C_s = (1+\varepsilon) C_i$. The mismatch of ε is substituted into (3-29)

$$\begin{aligned} V_{i+1} &= \frac{2+\varepsilon}{1} V_i - \frac{1+\varepsilon}{1} \cdot D \cdot V_{ref} + \frac{C_{tot}}{1+C_i} V_{os} \\ &= 2\left(1 + \frac{\varepsilon}{2}\right) V_i - (1+\varepsilon) \cdot D \cdot V_{ref} + \frac{C_{tot}}{1+C_i} V_{os} . \end{aligned} \tag{3-30}$$

The offset term can be easily removed from the system. So we focus on the gain error that stemed from capacitor mismatch. (3-30) can be reduced to

$$\begin{aligned} V_{i+1} &= 2\left(1 + \frac{\varepsilon}{2}\right) V_i - (1+\varepsilon) \cdot D \cdot V_{ref} \\ &= 2\left(V_i - D\frac{V_{ref}}{2}\right)(1+\varepsilon) - \varepsilon \cdot D \cdot V_{ref} . \end{aligned} \tag{3-31}$$

The correction is performed off-chip or in other DSP unit. By the use of (3-31) it is performed stage by stage from back-end to the first stage. The measured gain error

and output code are used. Finally we can drive corrected data without gain error.

Chapter 4

A 8-bit 100MS/s CMOS Pipelined ADC

4.1 Introduction

In this chapter, a 8-bit pipelined ADC realization is presented. In Section 4.2, the capacitor value is decided from the thermal noise limitation. In Section 4.3, S/H and bootstrapped switch are introduced. In Section 4.4, two types of MDAC are compared and flip around MDAC is introduced. In Section 4.5, S/H and MDAC are analyzed to specify the gain, speed, and linearity requirement for OP amplifier. The circuit of OP is also presented. Section 4.5 introduces the comparator circuit and its Monte Carlo analysis. In Section 4.6, the timing diagram of the entire ADC is presented. Section 4.7 introduces the clock generator circuit.

4.2 Capacitor Selection

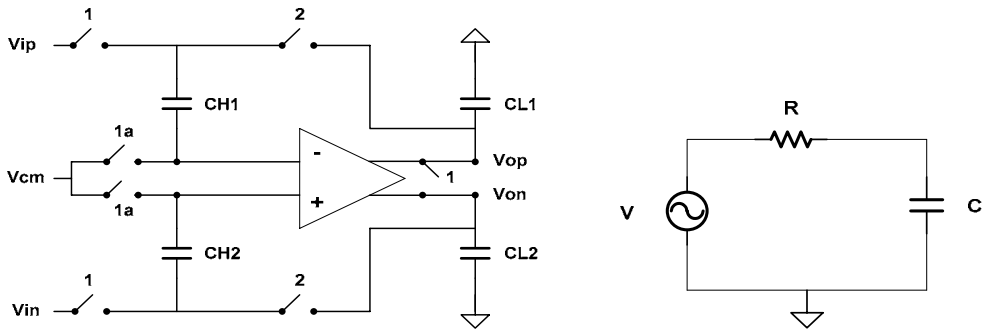


Figure 4-1 Circuit of S/H and simplified RC model

We use S/H circuit to select the value of capacitors. From Figure 4-1 shows

$$SNR = 10\log\frac{Power\_signal}{Power\_quantization\ noise + Power\_thermal\ noise}$$

$$(RC\ total\ noise\ power = \frac{kT}{C} \quad k = 1.38\times10^{-23}\ joules/kelvin)$$

$$= 20\log\frac{\frac{V_{ref}}{\sqrt{12}}}{\sqrt{\frac{V_{LSB}^2}{12}+\frac{kT}{C}}} = 20\log\frac{\frac{2V_{FS}}{\sqrt{12}}}{\sqrt{\frac{(2V_{FS}/2^8)^2}{12}+\frac{kT}{C}}}. \qquad (4\text{-}1)$$

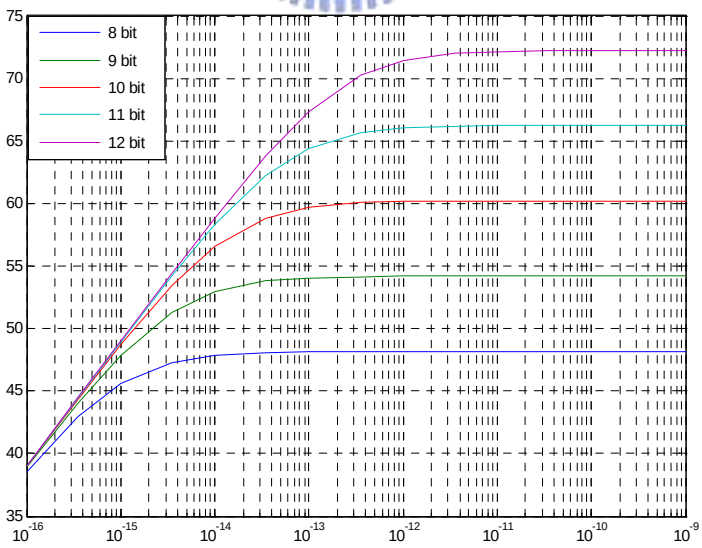


Figure 4-2 Capacitor value vs. SNR

As the curve shows, 10^{-12} farad is appropriate for a 8-bit ADC.

4.3 Sample and Hold Circuit

4.3.1 S/H Circuit

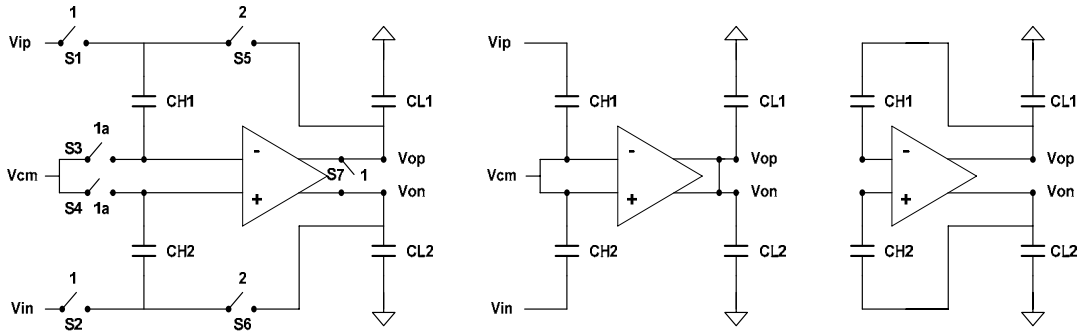


Figure 4-3(a) S/H circuit (b) Sample mode (c) Hold mode

Figure 4-3 shows the sample and hold circuit [18]. $S1$ and $S2$ are the most critical switch of all. Because their switching noise affects the quality of that the signal is sampled. The bootstrapped switch is utilized in $S1$ and $S2$, to make sure that $S1$ and $S2$ are turn on in constant voltage. That represents the switching noise is signal independent. The bottom plate sampling technique (presented in Section 4.7) is also applied to avoid switching noise. $S3$ and $S4$ are always turn off before $S1$ and $S2$. When in phase 1 S/H samples signal and transmit it to the first pipelined stage in phase 2.

4.3.2 Bootstrapped Switch

In Figure 4-4, when $ck = 0$ C_b is charged up to VDD, M_s is turned off [19]. When $ck = 1$, input signal is applied. Gate of M_s rises to $V_{DD} + V_i$ because of charge in C_b. By this way M_s is always turned on in V_{DD}. It results in input independent switching noise.

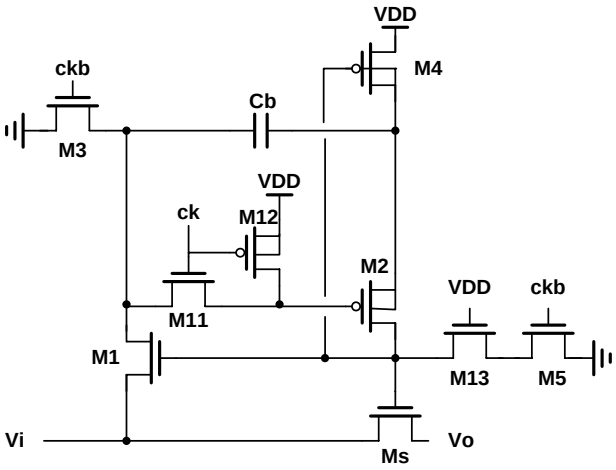


Figure 4-4(a) Bootstrapped Switch

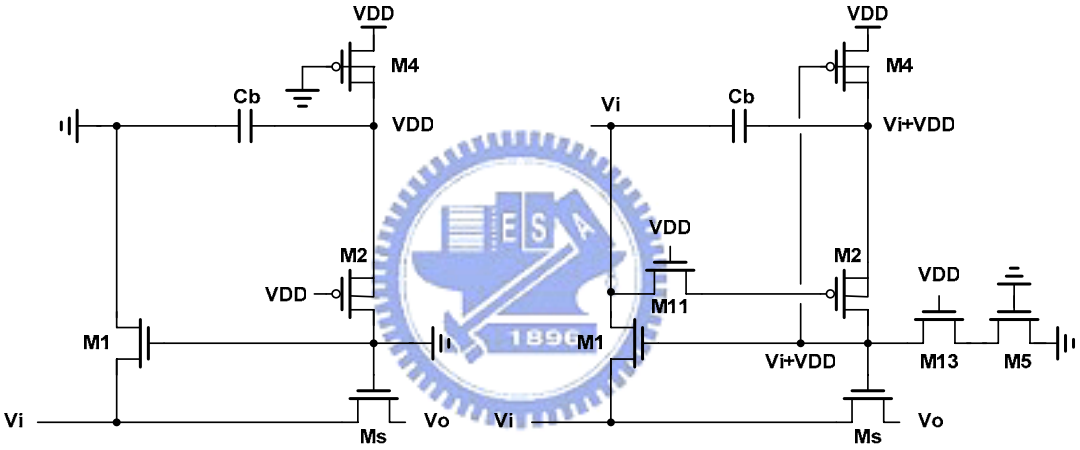


Figure 4-4(b) $ck = 0$

Figure 4-4 (c) $ck = 1$

4.4 MDAC

4.4.1 MDAC Selection

Multiplying digital-to-analog converter is constructed of subDAC, subtractor, and residue amplifier. There are two types of MDAC for consideration [20]. For high speed operation, feedback factor of the closed loop affects the unit gain frequency criterion of the OP design. So compare their feedback factor and choose the higher one to reduce the difficulties of OP design.

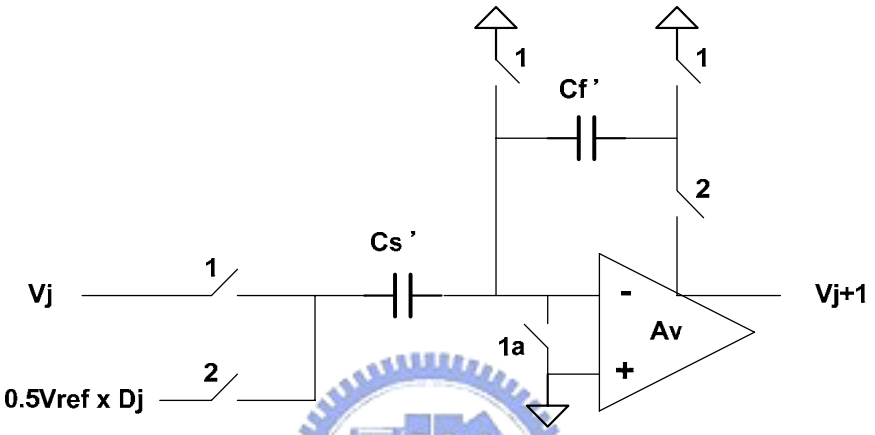


Figure 4-5 Switch capacitor MDAC

The feedback factor is $\beta' = \frac{C_f'}{C_s' + C_f'} = \frac{1}{3}$ $C_s' = 2C_f'$ *(for 1.5bit / stage)*

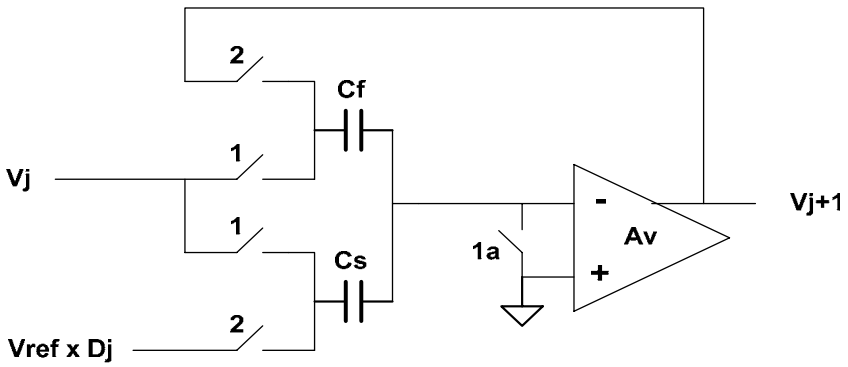


Figure 4-6 Flip around MDAC

This feedback factor gives $\beta = \frac{C_f}{C_s + C_f} = \frac{1}{2}$ $C_s = C_f$ *(for 1.5bit / stage)*.

So the flip around type MDAC is chosen.

4.4.2 MDAC Circuit

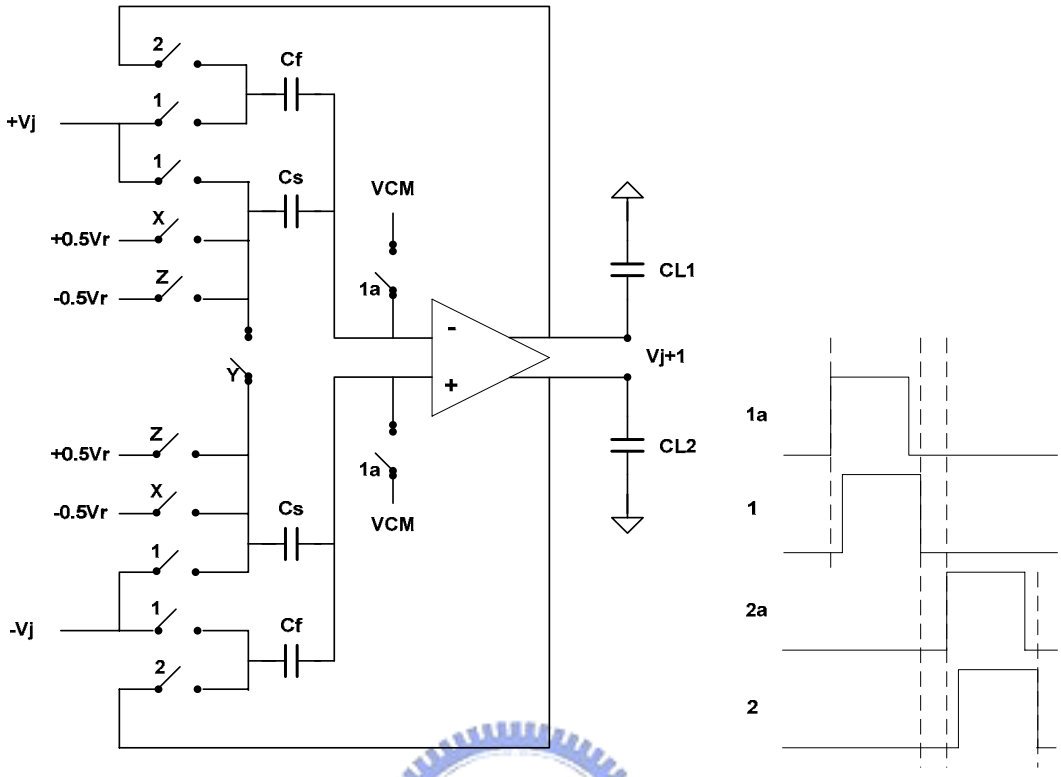


Figure 4-7 MDAC circuit

The MDAC is shown in Figure 4-7. Switches are utilized by transmission gates. The bottom plate sampling technique is also applied to avoid charge injection. In phase 1, four capacitors sample signal from previous stage and OP is reseted to common mode voltage. In phase 2, Cf connect to output to send signal to next stage. At the same time $X\,Y\,Z$ are active dependent on the value of V_j.

$$V_{j+1} = (V_j - D_j \cdot \frac{V_{ref}}{2}) \cdot 2 \tag{4-2}$$

$$\begin{cases} V_j > \dfrac{V_{ref}}{4} & D_j = 1 \quad X = 1 \quad Y = 0 \quad Z = 0. \\ \dfrac{V_{ref}}{4} > V_j > -\dfrac{V_{ref}}{4} & D_j = 0 \quad X = 0 \quad Y = 1 \quad Z = 0. \\ V_j < -\dfrac{V_{ref}}{4} & D_j = -1 \quad X = 0 \quad Y = 0 \quad Z = 1. \end{cases}$$

4.4.3 Intentional Stage Gain Error

In order to verify the BIST circuit, a known quantity of stage gain error is added into MDAC in stage1- stage4. The mechanism is controlled by cap_sel signal

presented in Figure 4-8. C_{ad} is in the value of $20\,fF$. It represents the mismatch of 0.04. By comparing the known value with the estimated error we can identify whether the estimation is correct.

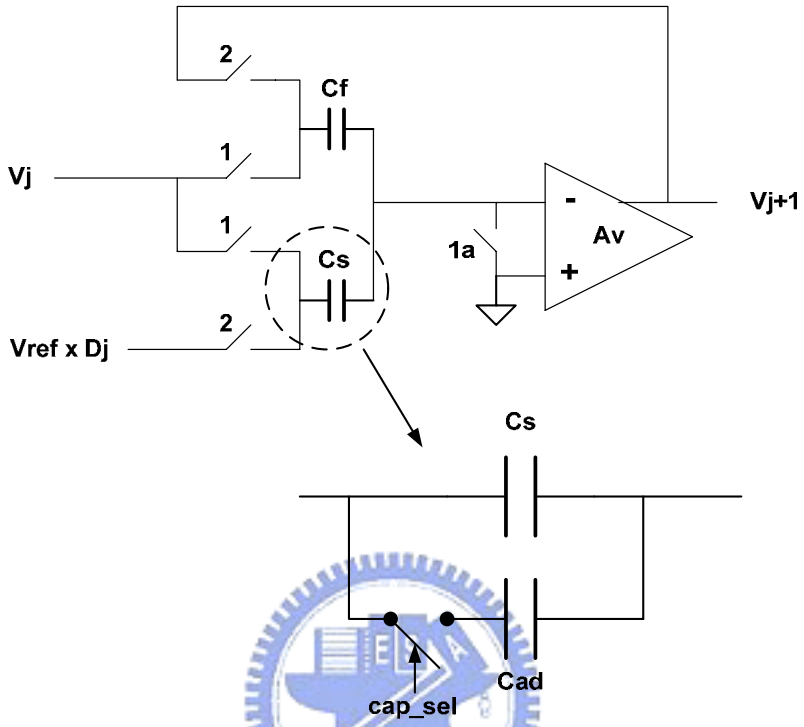


Figure 4-8 MDAC with intentional capacitor mismatch added

4.5 OP Specification

For simplicity, the OP of S/H is the same as the one used in MDAC. The best performance is limited by the amplifier closed loop behavior. We analyze the closed loop circuit of the S/H and the MDAC to realize OP specification.

4.5.1 OP consideration in S/H

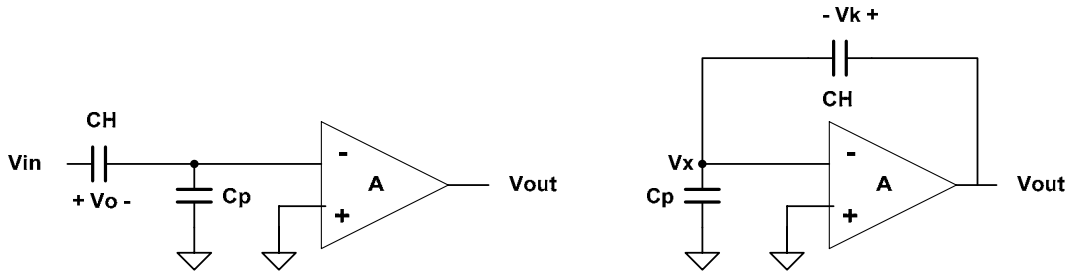


Figure 4-9 (a) Simplified S/H in sample mode (b) In hold mode

For analysis, the simplified circuit is shown in Figure 4-9 [21][22]. The equations are

$$V_k = \frac{C_H V_0 + C_p V_x}{C_H} = V_{out} - V_x \tag{4-3}$$

$$V_x = -\frac{V_{out}}{A_{SH}}. \tag{4-4}$$

From (4-2) and (4-3)

$$V_{out} = \frac{V_0}{1+\frac{1}{A_{SH}}\left(\frac{C_p}{C_H}+1\right)}$$

$$\approx V_0\left[1-\frac{1}{A_{SH}}\left(\frac{C_p}{C_H}+1\right)\right]. \tag{4-5}$$

Assume $C_H = 0.5p$ $C_p \approx 0.3p$ and error term $< 0.5\,LSB$. From (4-4)

$$\frac{1}{A_{SH}}\left(\frac{C_p}{C_H}+1\right) < \frac{1}{2}\frac{1}{2^8}. \tag{4-6}$$

So

$$A_{SH} \geq 58dB. \tag{4-7}$$

For a closed-loop amplifier, the step response is

$$V_{out}(t) = V_{step}(1-e^{-\frac{t}{\tau}}). \tag{4-8}$$

Consider the unit gain frequency specification. For error term $< 0.5\,LSB$,

$$e^{-\frac{t}{\tau}} \leq \frac{1}{2}\frac{1}{2^8}$$

$$\Rightarrow\ t > 6.2\tau\ . \tag{4-9}$$

Assume $t = \frac{3}{4}\,hold\ time = 3.5ns$,

$$\tau \leq \frac{3.5}{6.2}ns. \tag{4-10}$$

At the same time [23]

$$\tau = \frac{1}{\omega_{3dB}\big|_{closed\ loop}} = \frac{1}{\beta\omega_t\big|_{open\ loop}} = \frac{1}{2\pi\beta_{SH}f_t}. \tag{4-11}$$

From (4-9) and (4-10),

$$f_{t\_SH} \geq 451\ MHz \qquad (\ \beta_{SH} = \frac{C_H}{C_H + C_p} = 0.625\ ). \tag{4-12}$$

4.5.2 OP consideration in MDAC

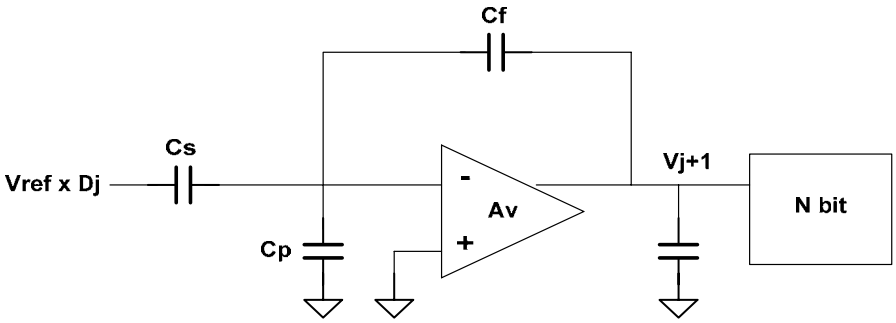


Figure 4-10 Simplified MDAC circuit

Consider the simplified MDAC in Figure 4-10. In the same way for error term $< 0.5\ LSB$,

$$\varepsilon_{error} = \frac{1}{A_{MD}\beta_{MD}} = \frac{1}{A_{MD}} \cdot \frac{C_f + C_s + C_p}{C_f} \leq \frac{1}{2}\frac{1}{2^8}. \tag{4-13}$$

Assume $C_f = C_s = 0.5p\ \ and\ \ C_p = 0.3p$. Then

$$\beta_{MD} = \frac{C_f}{C_f + C_s + C_p} = 0.384 \tag{4-14}$$

$$A_{MD} \geq 62.4\ dB. \tag{4-15}$$

Considering the unit gain frequency specification, for error term $< 0.5\ LSB$, (4-13) is substituted into (4-10). Gives

$$\tau = \frac{1}{2\pi\beta f_t} \leq \frac{4.5}{6.2} ns$$

$$\Rightarrow f_t \geq 571\ MHz. \tag{4-16}$$

Summarize the specification of OP and set up our design target below.

Table 4-1 Summarized OP specification

	S/H	MDAC	Design Target
Gain (dB)	58	62.4	> 70
Ft (MHz)	451	571	750
SR (v/ns)	0.2	0.2	0.2

Swing (Vpp)	1.6	1.6	1.6
CL (p)	1	1	1

4.5.3 Linearity of OP

It is known that OP gain is not constant in the entire output swing range. It is maxima as output voltage around the common mode voltage and decrease as the output voltage away from the common mode voltage. It is necessary to analyze how much the dc gain variation is acceptable. From (4-4),

$$error = \frac{1}{A_v}\left(\frac{C_p}{C_H}+1\right). \tag{4-17}$$

Assume $A_v = A - \Delta A$,

$$error = \frac{1}{A-\Delta A}\cdot\frac{C_p+C_H}{C_H} \approx \frac{1}{A}\cdot\left(1+\frac{\Delta A}{A}\right)\cdot\frac{C_p+C_H}{C_H}. \tag{4-18}$$

To achieve N-bit resolution

$$\frac{\Delta A}{A^2}\cdot\frac{C_p+C_H}{C_H} \le \frac{1}{2}\cdot\frac{1}{2^N}. \tag{4-19}$$

For 8-bit ADC gives (assume $C_H = 0.5p$ $C_p = 0.3p$ A = 90 dB)

$$\Delta A \le 9.88\,dB. \tag{4-20}$$

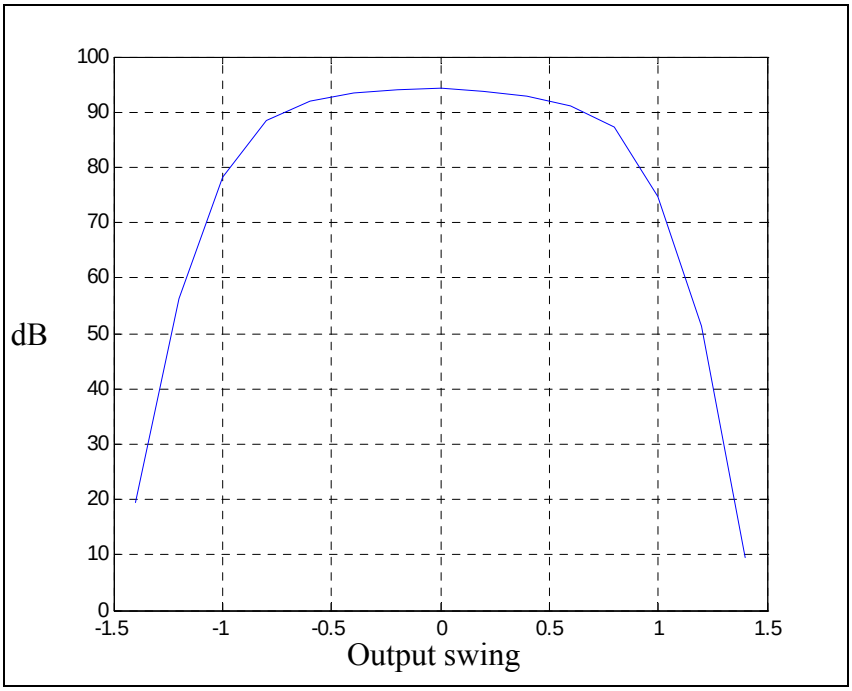


Figure 4-11 Output swing vs. dc gain

4.5.4 OP Design

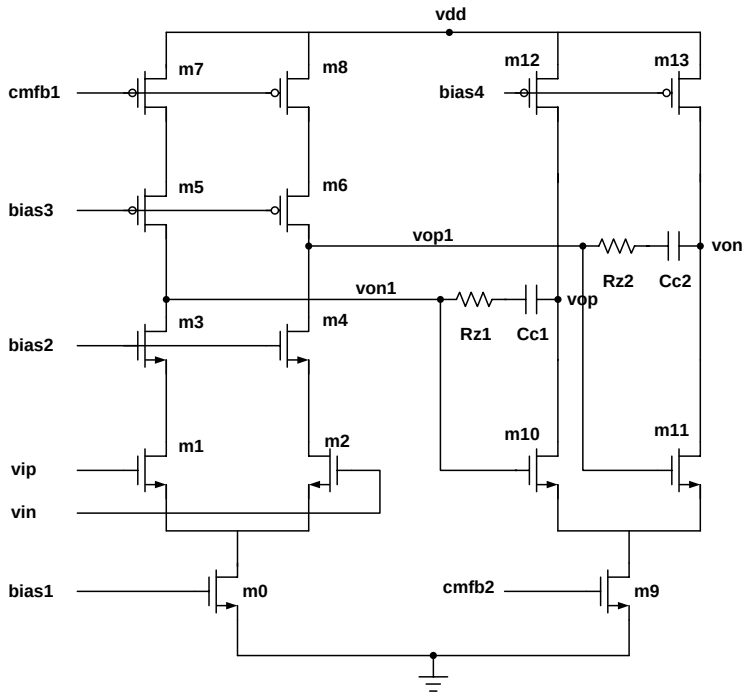


Figure 4-12 Operational amplifier circuit

The specification of OP is concluded in Table 4-1. For high gain and high speed OP design a two-stage OP is adopted as shown in Figure 4-12 [24]. The first stage is a telescopic amplifier offers high gain. It is followed by common source serves as the second stage that offers a large output swing. The dc gain is achieved over 90dB. NMOS input stage is used to maximize the speed. The overdrive voltage of transistors is about 200mV. For stability consideration the second pole needs to be push beyond the unit gain frequency. The location of the second pole is approximately $gm_{10,11}/C_L$. C_L includes the load capacitor of the next stage, the capacitor of common mode feedback (CMFB) circuit, and the parasitic capacitor at output node. The standard miller compensation is taken. The dominate pole is push to a lower frequency and the second pole is push to a higher frequency. R_{z1} *and* R_{z2} are realized by transistors in the triode region and carefully adjusted to get maximum phase margin.

Continuous type and SC type CMFB shown in Figure 4-13 and Figure 4-14. They are used to produce control voltage *cmfb1* and *cmfb2*. Common mode voltage is set to 0.9V. Without voltage swing issue at *vop1* and *von1* the scheme in Figure 4-13 is adopted. It offers lower parasitic capacitance at output of the first

stage. In Figure 4-14, SC CMFB is used for a large output swing. *C1* and *C2* are chosen carefully not to overloaded amplifier. *S1* and *S2* are realized by transmission gates to allow large swing. NMOS switches for other switches are appropriate.

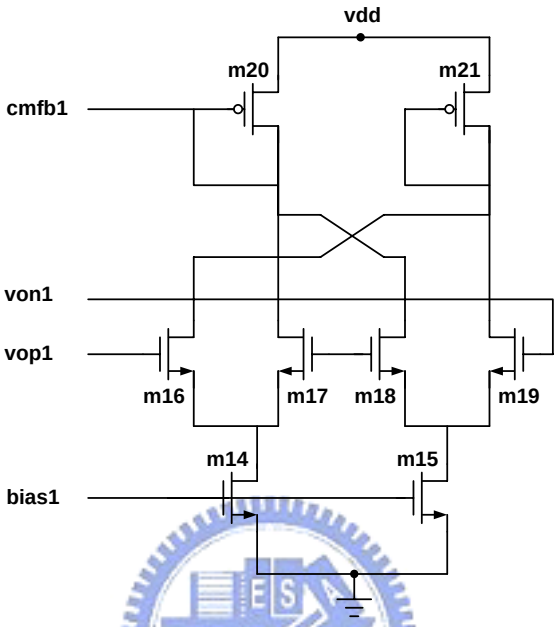


Figure 4-13 Continuous type CMFB

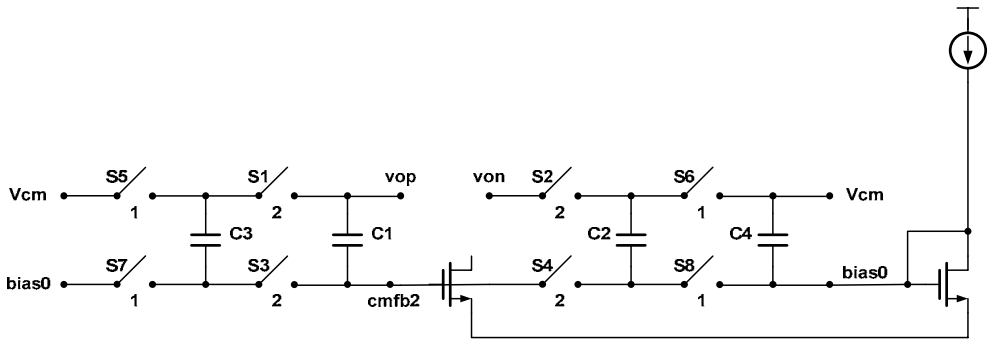


Figure 4-14 SC type CMFB

4.6 Comparator

4.6.1 Preamp

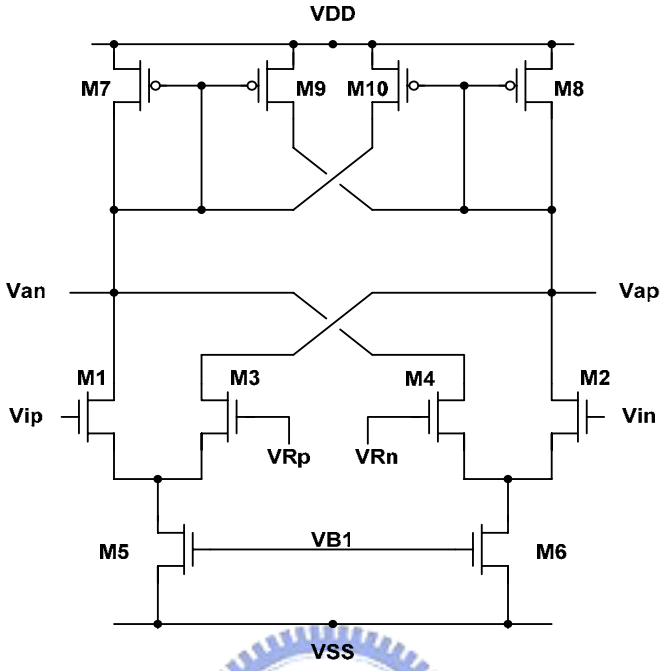


Figure 4-15 Preamp

Figure 4-15 shows the preamp of the comparator. The input stages are made of $M1,2,3,4$. They convert $(V_{ip} - V_{in}) - (V_{Rp} - V_{Rn})$ into a current. Active load , $M7,8,9,10$,are connected. Diode load, $M7,8$ offer positive impedance while cross couple pair, $M9,10$, appear as negative impedance. Being an active load $gm_{M7,M8}$ must be greater than $gm_{M9,M10}$ to increase the differential gain and decrease the common mode gain. For high speed operation, it is usually not designed with high gain, normally $10 \sim 20\ dB$ is enough. In our design it is $15dB$.

4.6.2 Low Offset Regenerative Latch

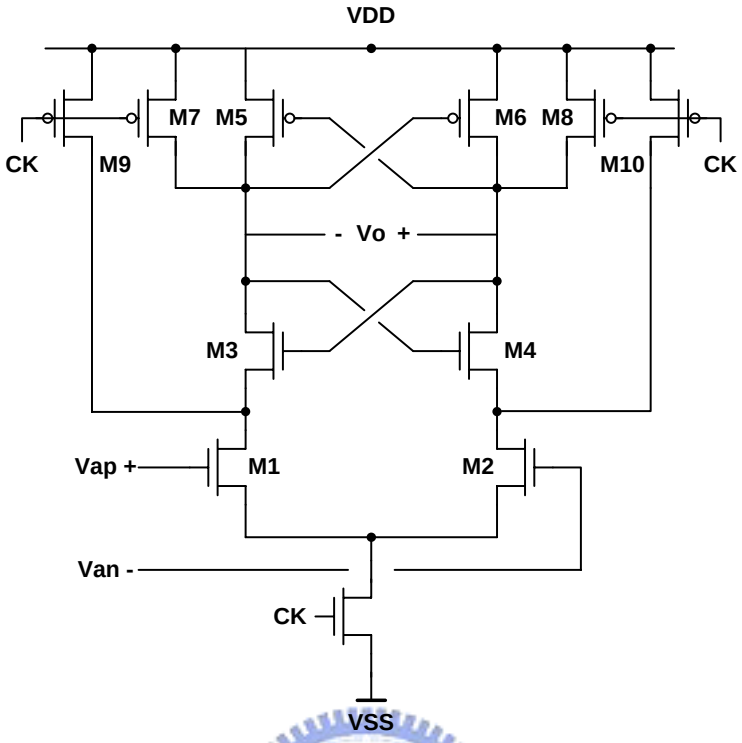


Figure 4-16 Regenerative latch

In Figure 4-16, when $CK = 0$, latch is in reset mode. $M7,8,9,10$ are turned on, source and drain of $M3,4$ are equal to VDD. When $CK = 1$, $M1,2$ $M3,4$ and $M5,6$ are activated in turns. Because the drain of $M1,2$ are equal to VDD at $CK = 0$. When $M1,2$ start to be activated they must be in saturation region. That means $M1,2$ have a great output impedance, so the latch is not influenced by the mismatch easily. It is the reason why this is called a low offset regenerative latch.

4.6.3 Monte Carlo Simulation of Comparator

Table 4-2 (from TSMC0.18 reference file) to induce mismatch in the comparator. Then we analyze the results by a probability method to determine if the comparator design is reasonable.

$$\sigma(\Delta V_t) = \frac{A_{V_t}}{\sqrt{WL}} + S_{V_t} \cdot D \tag{4-21}$$

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}} + S_\beta \cdot D\,. \tag{4-22}$$

Table 4-2 The sigma value for mismatch parameters

	1.8V NMOS	1.8V PMOS	3.3V NMOS	3.3V PMOS
σVth0 (mv)	3.635. geo	4.432. geo	6.227. geo	4.525. geo
σXL/L (%)	0.458. geo	0.396. geo	0.365. geo	0.247. geo
σXW/W (%)	0.373. geo	0.326. geo	0.298. geo	0.201. geo
σTox/Tox(%)	0.101. geo	0.0873. geo	0.0804. geo	0.0543. geo
geo=1/sqrt(N. Leff. Weff) (1/um)				

Because of the mismatch, the threshold voltage of the comparator is changed, like the dotted line shown in Figure 4-17. The black line represent the ideal threshold voltage, $0.25V_{ref}$. Input voltage is swept from $0.25V_{ref}+0.35$ to $0.25V_{ref}-0.35$. The value, 0.35 , is decided to cover whole possible offset voltage range.

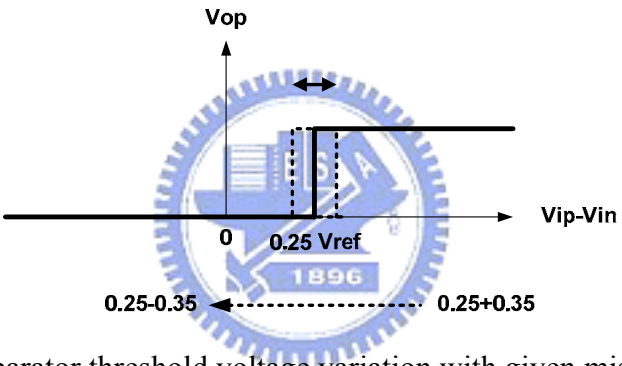


Figure 4-17 Comparator threshold voltage variation with given mismatch parameter

As the input swept, we calculate the number of error result in the comparator output. Then the results are cumulated, and the cumulated data are plotted, $C(i)$. The curve is shown in Figure 4-18.

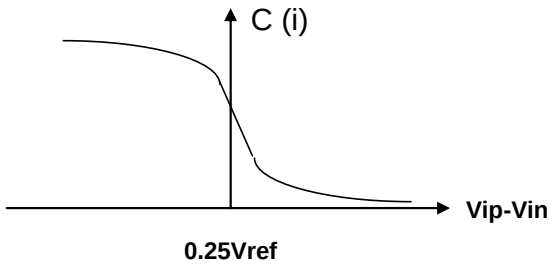


Figure 4-18 Cumulated number of error result

$C(n)$ subtract by $C(n-1)$ and then becomes the *PMF(probability mass function)* of the comparator offset voltage shown in Figure 4-19.

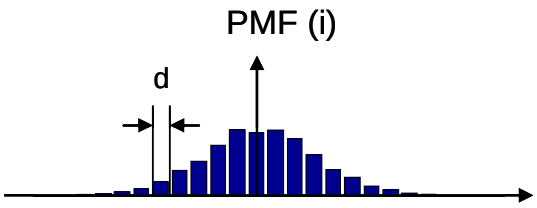


Figure 4-19 Probability mass function of comparator offset voltage

Finally *PMF(i)* is divided by d. The *PDF(probability density function)* of the offset is shown in Figure 4-20. We calculate the mean and standard deviation. They are *0.205mV* and *3.04mV* individually. That is smaller than 0.5 LSB. So the design is acceptable. We use the calculated mean and standard deviation to draw an ideal normal distribution curve shown in Figure 4-20. It fits the result of our simulation. That means the simulation is reasonable and correct.

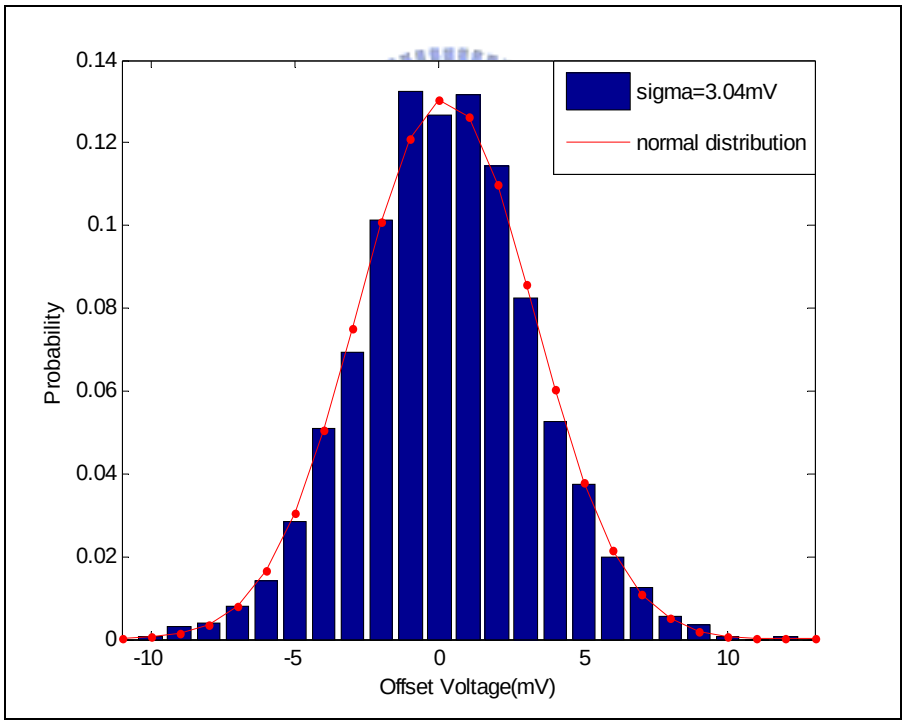


Figure 4-20 PDF of comparator offset voltage

4.7 ADC Timing Diagram

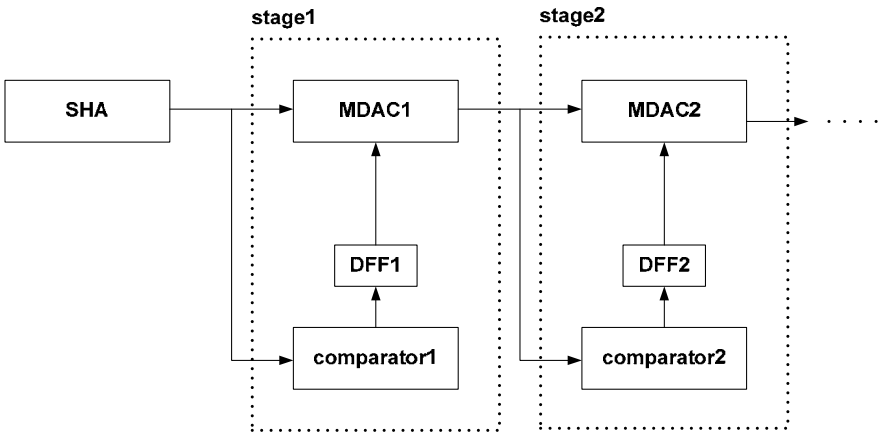


Figure 4-21 diagram of adjacent pipelined stages

Figure 4-21 shows the ADC structure. S/H samples the input signal and transfers it to the pipelined stage. Comparator and DFF serve as subADC. DFF is triggered in the rising edge. For high throughput, all adjacent stages are applied the opposite clocks include S/H. That is to guarantee the charge will not be lost in switch capacitor circuit and prevent from adjacent stages in the same residue received period.

Non-overlapping clocks, $ck1$ *and* $ck2$, are used in Figure 4-22. The $ck1$ is adopted in S/H, the $ck2$ is adopted in stage1, $ck1$ is adopted in stage2, and etc. When $ck1 = 0$, S/H is in hold phase. Comparator1 and MDAC1 receive data from S/H. The amplifier needs time to slew and settle its output voltage. There is another clock, comparator1 denoted in Figure 4-22, a 3ns delayed later than rising edge of $ck2$. It is used to turn on the regenerated latch in the comparator. It prevents the comparator from being activated by non-settled data. After the latch being turned on, DFF is triggered to output the result of the comparator. When $ck1$ is high, S/H is in the sample phase. MDAC1 transfers the residue to stage2. Stage2 just functions as stage1 with the opposite clock. As showing in Figure 4-22, the data is transferred stage by stage.

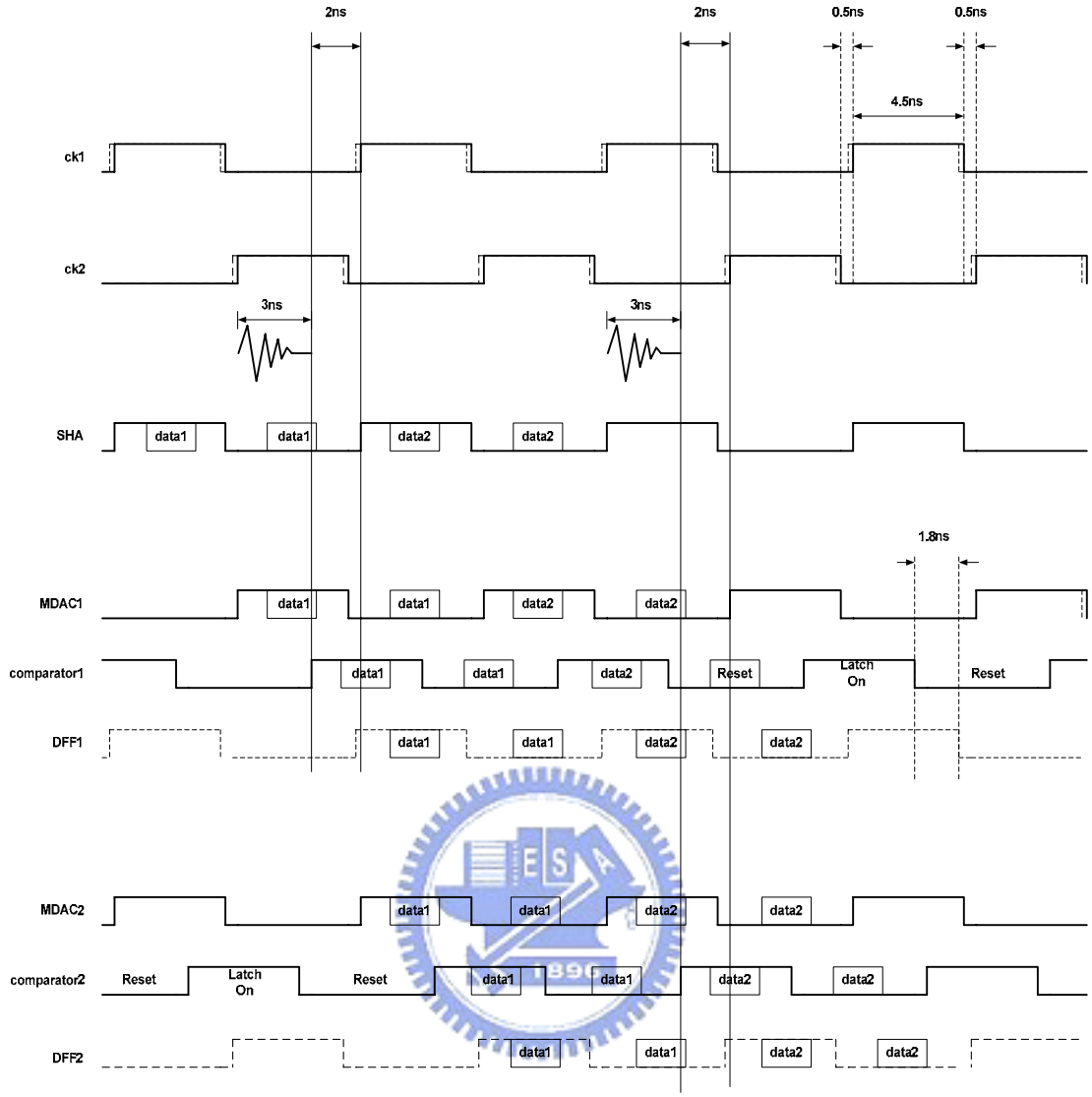


Figure 4-22 ADC timing diagram

4.8 Clock Generator

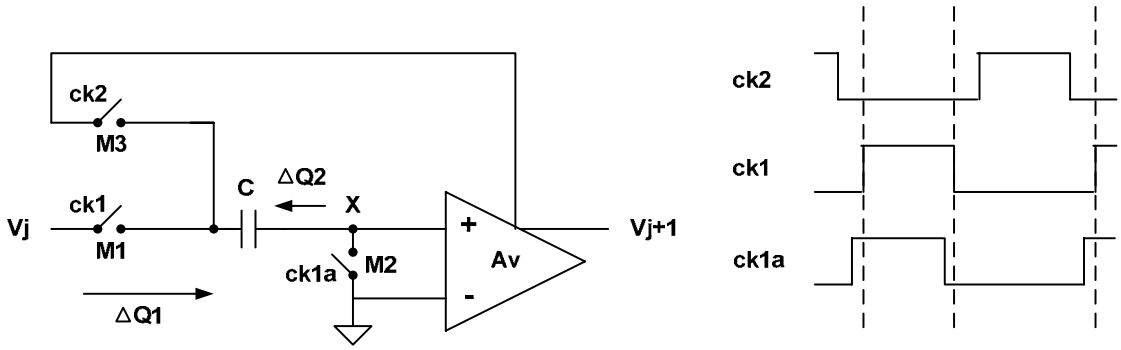


Figure 4-23 Switch capacitor circuit

It is necessary to make use of $ck1a$ that is the clock leading $ck1$ as shown in Figure 4-23. If $ck1a$ is replaced by $ck1$, the input dependent charge, $\Delta Q1$, is injected from M1. It occurs at the moment when $ck1$ falls from 1 to 0. Then the linearity is degraded in V_{j+1}. If $ck1a$ is used, the node X is floating at that moment The effect of $\Delta Q1$ is eliminated. Although the switching noise $\Delta Q2$ from $M2$ exists, it is independent of the input signal. At the same time, the bottom plate sampling technique is adopted. The bottom plate has larger parasitic capacitor than the top plate because of the substrate. Capacitor's left plate is connected to the bottom plate and the right plate is connected to the top plate. Smaller parasitic capacitor in node X reduces the effect of $\Delta Q2$. According to these two reasons above, $\Delta Q2$ influence can be ignored. The clock generator circuit is shown in Figure 4-24 [25]. The simulation results are shown in Figure 4-25.

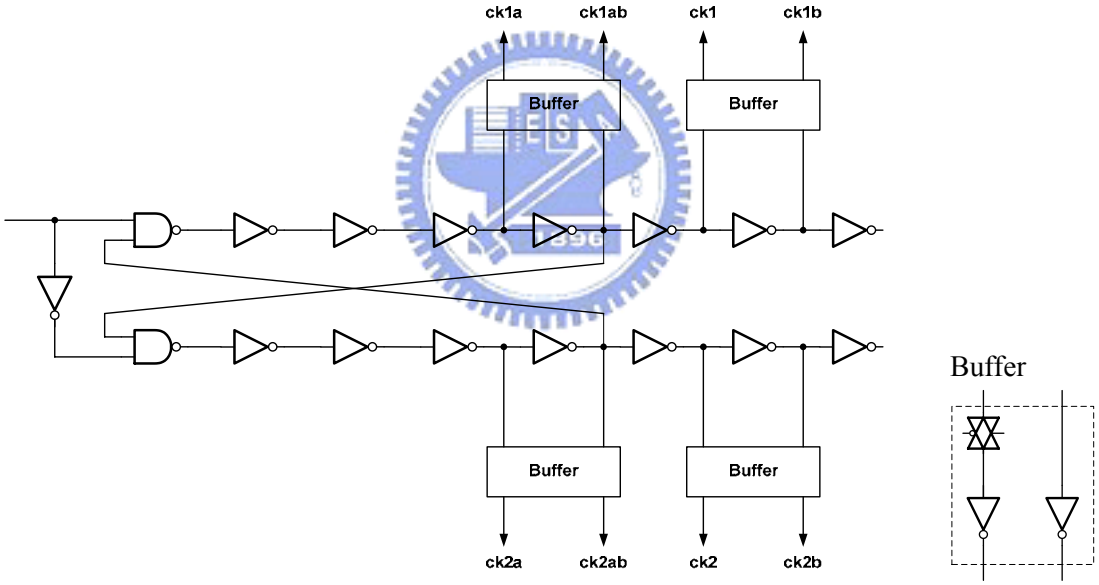


Figure 4-24 Clock generator circuit

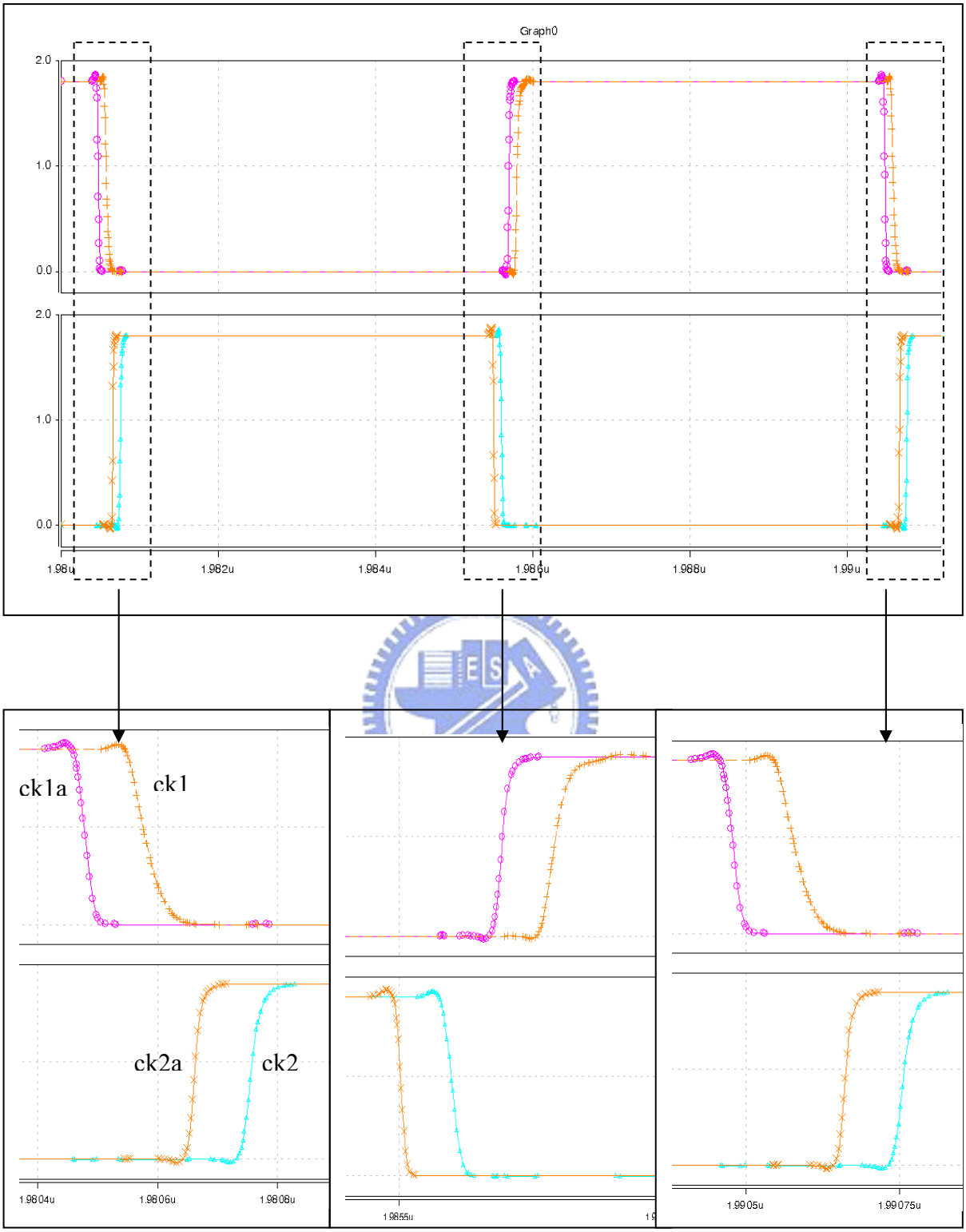


Figure 4-25 clock generator simulation result

Chapter 5

Simulation Result and Layout

5.1 Introduction

In this chapter the simulation result and layout are presented. In Section 5.2 and 5.3 OP and S/H results are shown. In Section 5.4, the ADC results are presented. Section 5.5 presents the error correction while ADC is intentionally added with mismatch. Finally in Section 5.6 and 5.7 the layout and the measurement setup are presented.

5.2 OP Simulation Result

The simulation results of OP are summarized in Table 5-1. They fit in with the specification in Table 4-1.

Table 5-1 Operational amplifier simulation result

	TT	FF	SS	SF	FS
Gain (dB)	90.3	80.8	92.6	87.4	87.2
Ft (MHz)	808.7	778.4	777.2	712	890.2
BW_3dB(kHz)	17.6	45.7	14.1	21.5	27.6
+SR / -SR(v/ns)	0.71 / 0.7	0.65 / 0.63	0.74 /0.72	0.65 / 0.63	0.71/0.71
Swing (Vpp)	>1.6	>1.6	>1.6	>1.6	>1.6
PM	63.8	68.9	63.4	67.5	61.3
Power Consumption(mW)	8.4	8.13	8.9	8.15	8.85

5.3 S/H Simulation Result

A $1.6\,V_{pp}$ sinusoidal signal with the frequency of $48.2\,MHz$ is sent into S/H. Under the clock rate of $100\,MHz$, the FFT outputs of corners are presented in Figure 5-1.

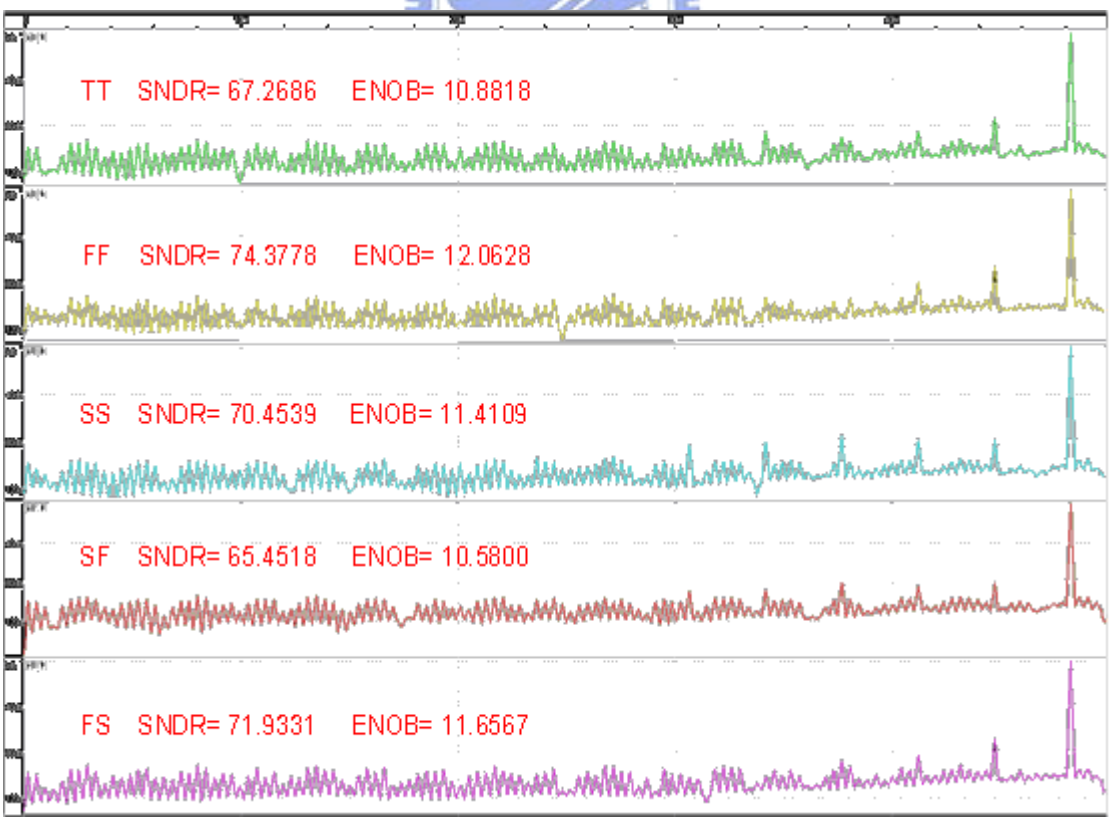


Figure 5-1 S/H simulation result

5.4 ADC Simulation Result

A $1.6\,V_{pp}$ sinusoidal input with frequency of $20.8\,MHz$ is sent to the pipelined ADC. Figure 5-2 presents the FFT result of TT corner. It has a SNR of $49.67\,dB$, a SNDR of $47.09\,dB$, and a SFDR of $63.2dB$. The SNDR of other corners are summarized in Table 2-1. Figure 5-3 presents the DNL and INL simulation result of the TT corner. Both of them are smaller than 0.7 LSB.

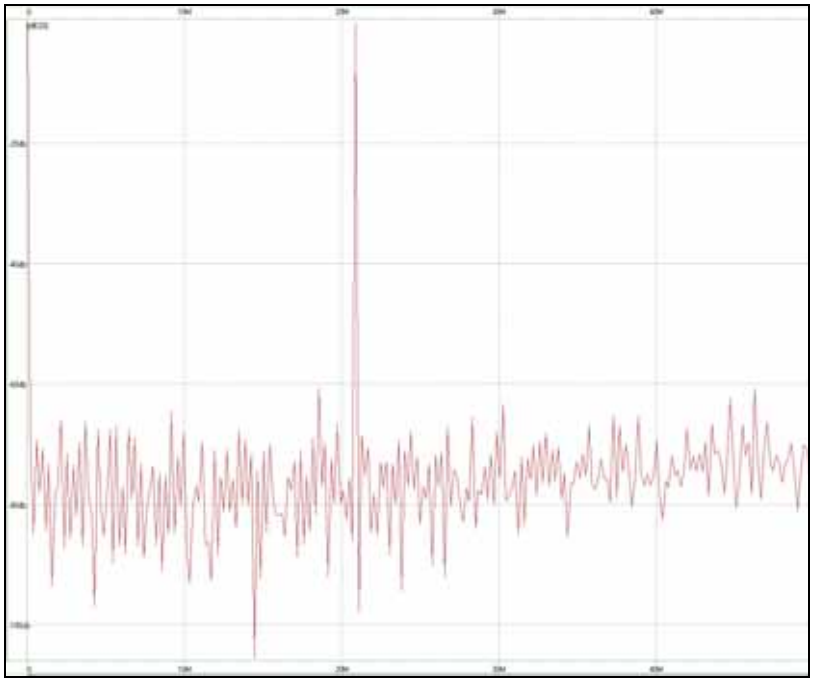


Figure 5-2 The ADC output with input frequency of $20.8\,MHz$ in TT corner

Table 5-2 ADC simulation of corner cases

	SNDR (dB)
TT	47.09
FF	47.67
SS	46.95
FS	47.73
SF	46.07

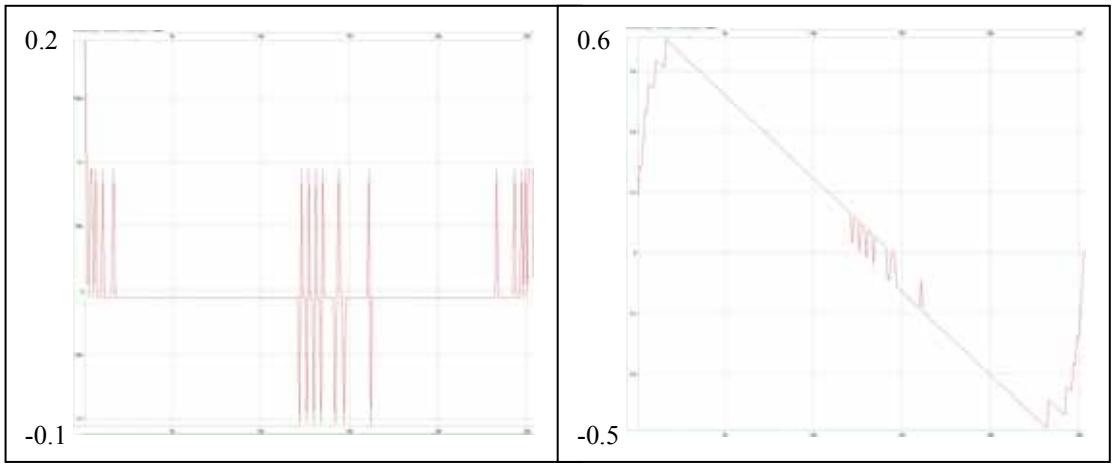


Figure 5-3 (a) DNL in TT case (b) INL in TT case

5.5 ADC with Mismatch

5.5.1 Simulation Result of intentional mismatch

With the 0.02 gain error added, the BIST circuit is simulated to count the error numbers. The simulation results of corners are summarized in Table 5-3.

Table 5-3 BIST circuit simulation result of corner cases

	Counted Number	Gain Error
TT	6143520	0.024
FF	6161823	0.021
SS	6125336	0.027
FS	6144006	0.024
SF	6150005	0.023

5.5.2 Simulation Result with Gain Error in Stage 1

With the results in Section 5.5.1 we build up a 8-bit pipelined ADC model in Matlab and set the gain error estimated in the first stage. Figure 5-4 represents the linearity simulation of the Spice with 0.02 gain error added in the first stage. Figure 5-5 presents the linearity analysis in Matlab. It is matched between Figure 5-4 and Figure 5-5. That represents the BIST estimation is correct.

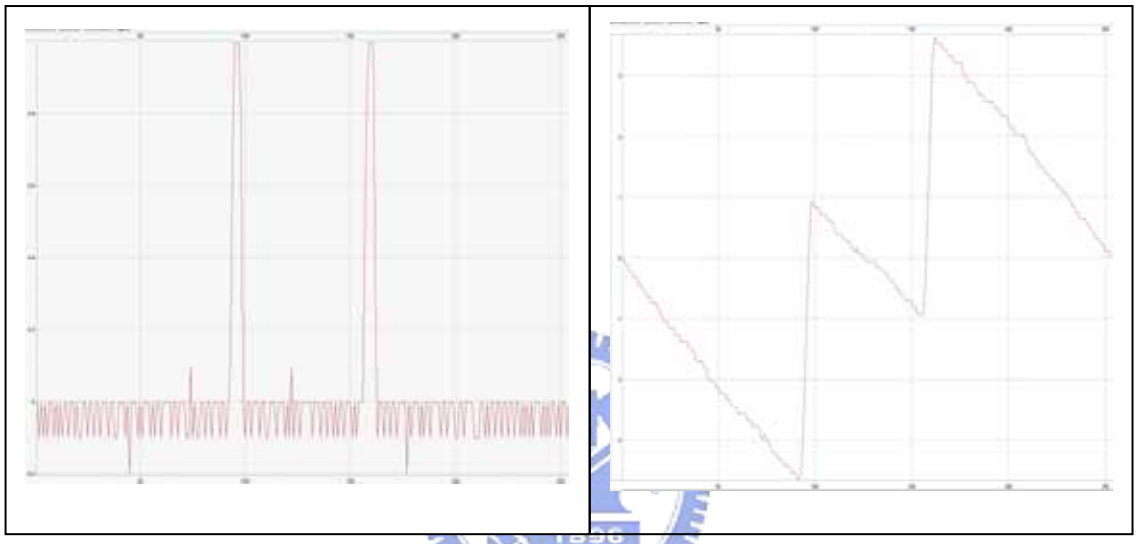


Figure 5-4 (a) DNL (Spice) (b) INL (Spice)

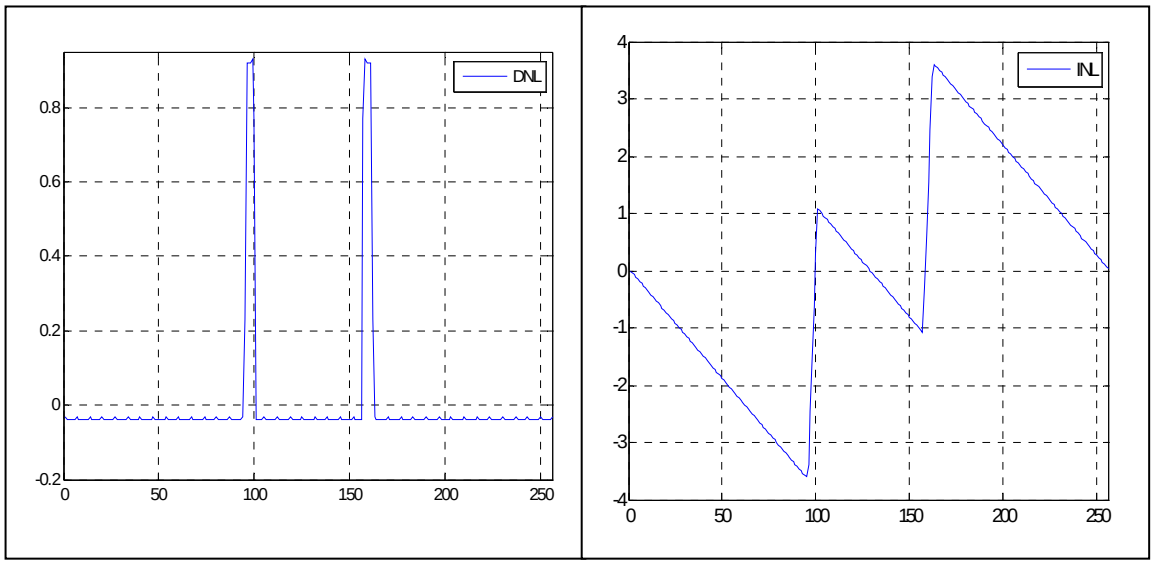


Figure 5-5 (a) DNL (Matlab) (b) INL (Matlab)

5.5.3 Simulation Result with Gain Error in stage 1 , 2

Figure 5-6 presents the linearity simulation of the Spice with *0.02* gain error added in the stage1 and the stage2. Figure 5-7 presents the linearity analysis in Matlab with the gain error parameter estimated in Section 5.5.1. Figure 5-6 is also similar to Figure 5-7.

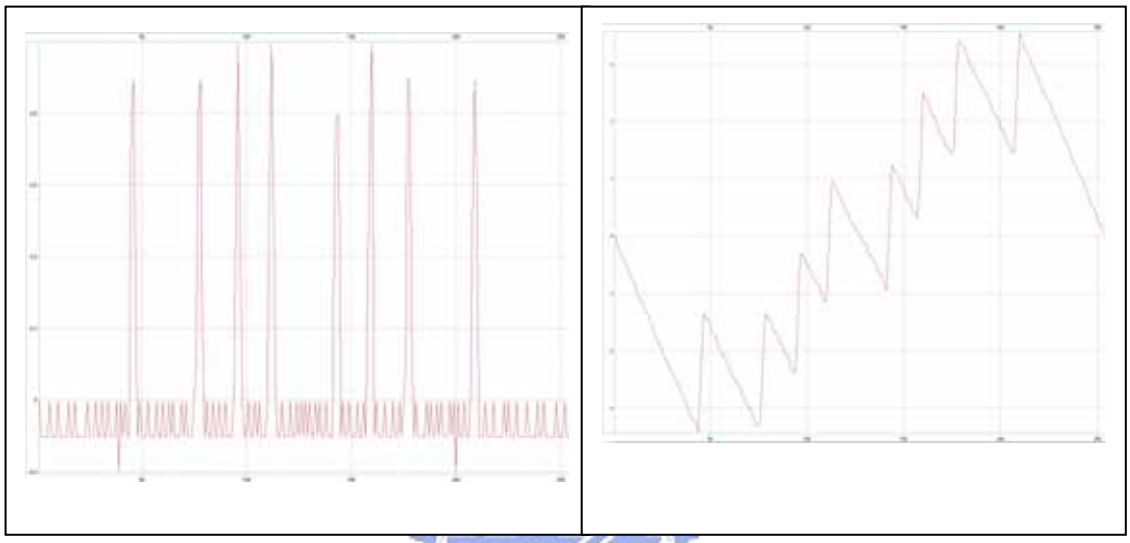


Figure 5-6 (a) DNL (Spice) (b) INL (Spice)

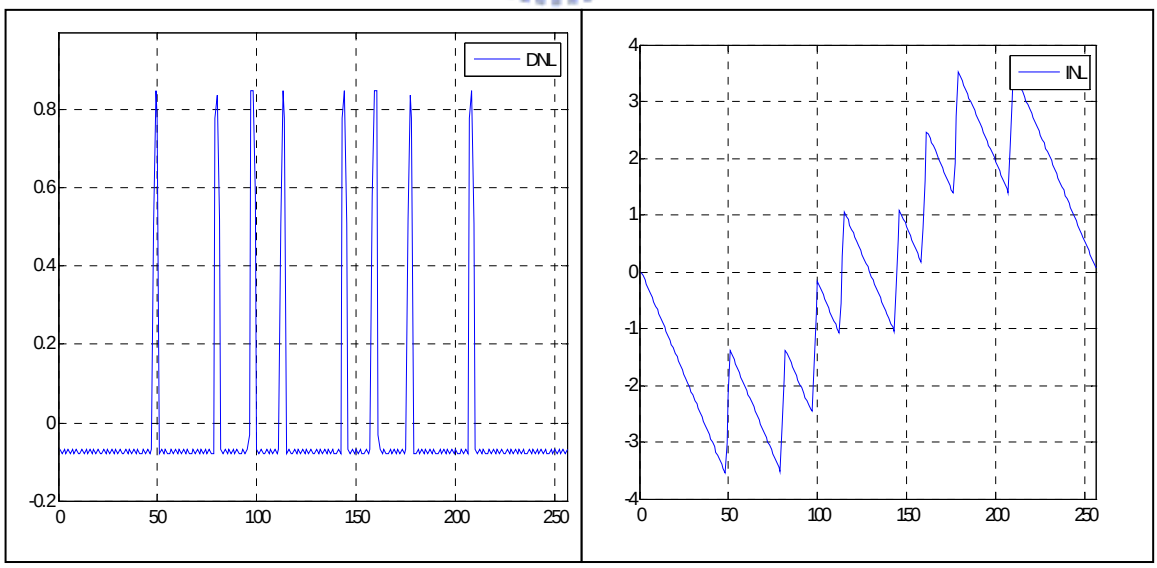


Figure 5-7 (a) DNL (Matlab) (b) INL (Matlab)

5.5.4 After Correction with Gain Error in Stage 1

The sinusoidal input with frequency of $20.8\ MHz$ is sent to the pipelined ADC. The ADC has gain error in the first stage. Figure 5-8 shows the FFT analysis of the ADC output. By the use of (3.31) and the estimated gain error, the corrected results are presented in Figure 5-9 and Figure 5-10.

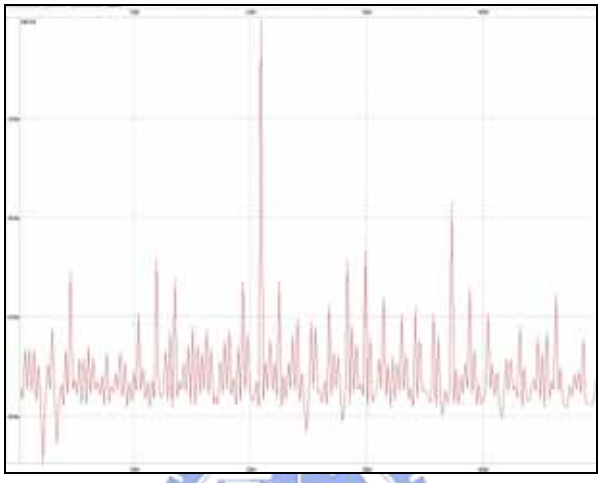


Figure 5-8 SNDR=34.99 dB (before correction)

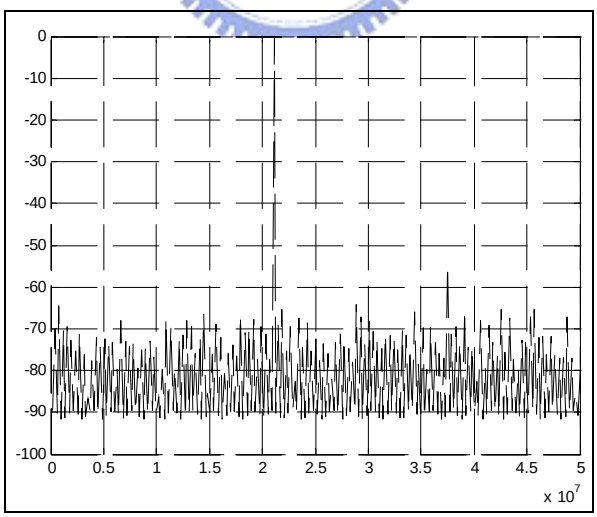


Figure 5-9 SNDR = 48.77dB (after correction)

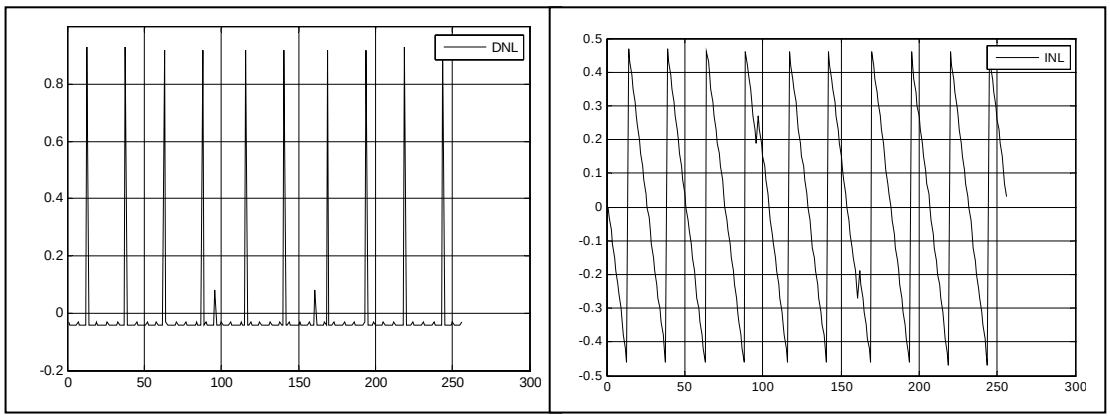


Figure 5-10 (a) DNL (after correction) (b) INL (after correction)

5.5.5 After Correction with Gain Error in Stage 1 , 2

The frequency of sinusoidal input is *20.8 MHz* , when the ADC has gain error in stage1 and stage2, the FFT analysis of it is presented in Figure 5-11. Figure 5-12 and Figure 5-13 presents the correction results by the use of (3.31).

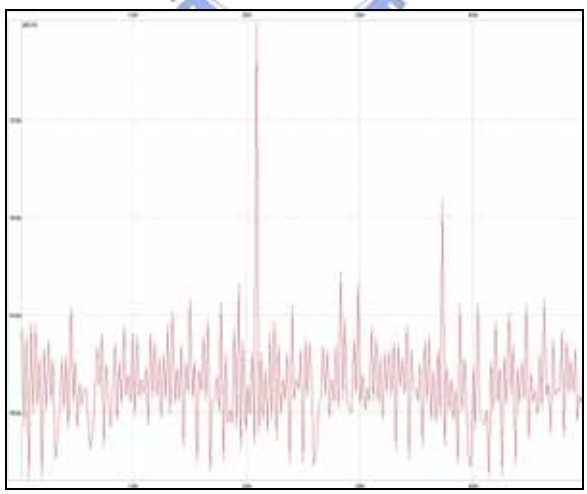


Figure 5-11 SNDR=35.35 dB (before correction)

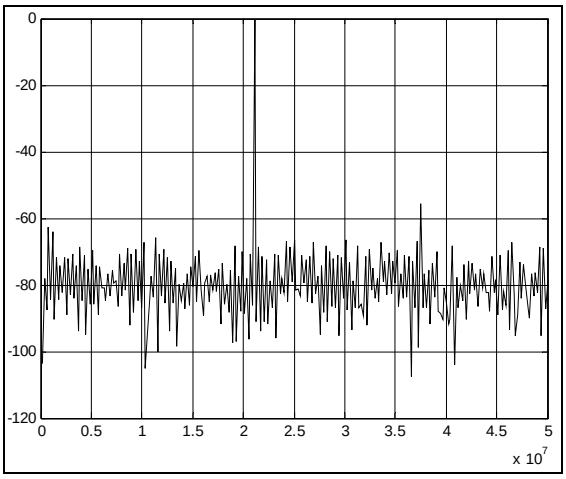


Figure 5-12 SNDR=49.18 dB (after correction)

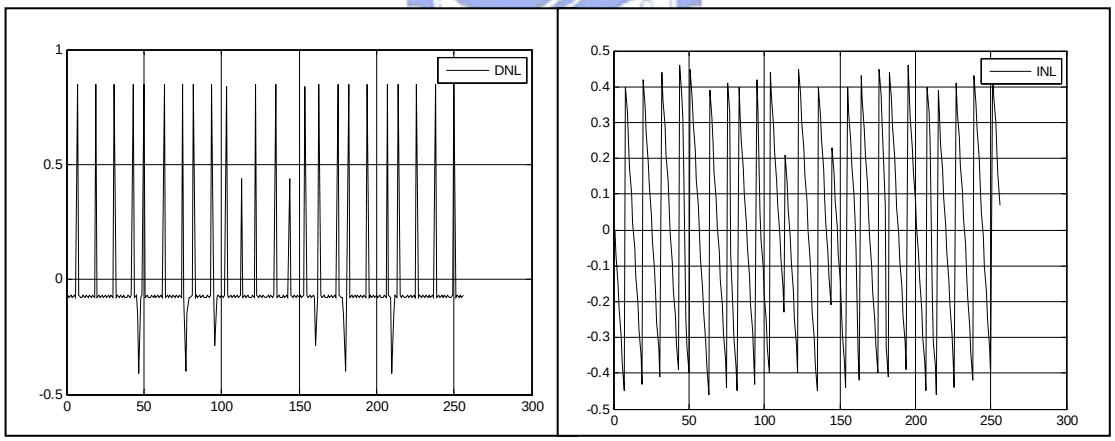


Figure 5-13 (a) DNL (after correction) (b) INL (after correction)

5.6 Layout and Measurement Setup

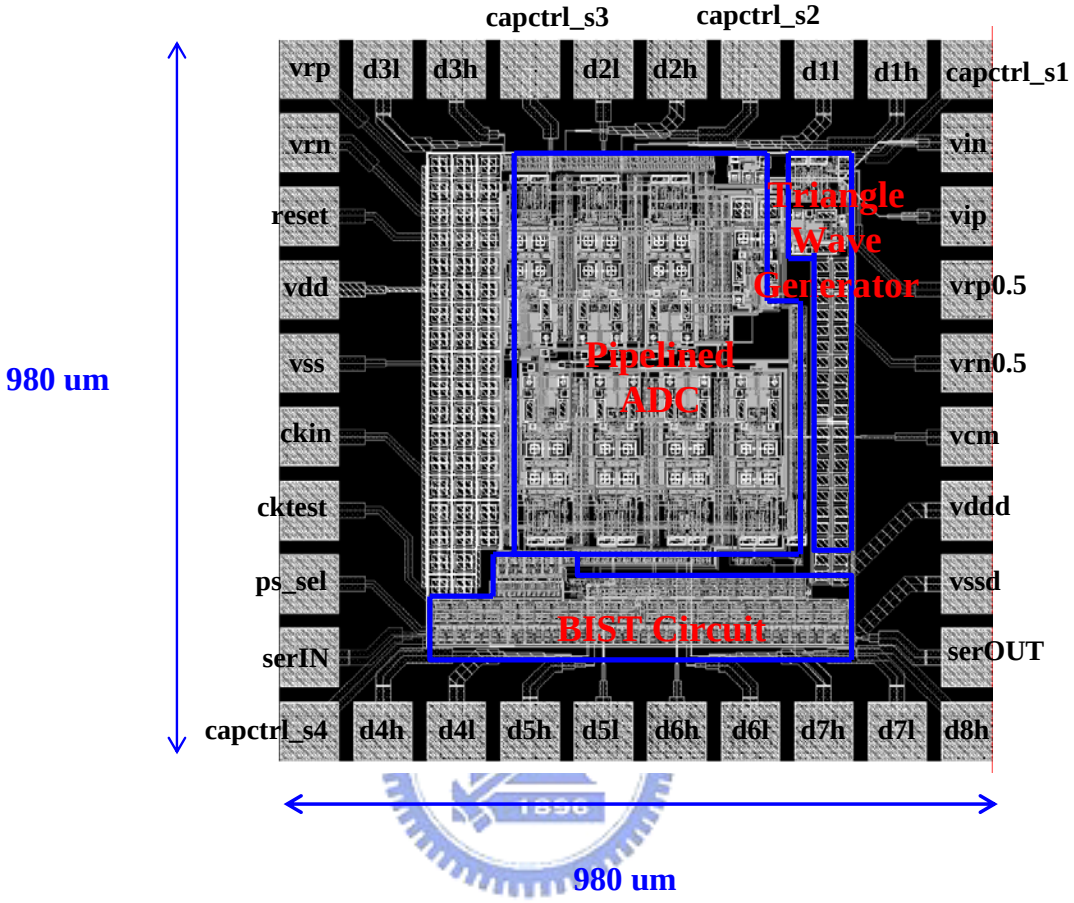


Figure 5-14 Chip layout

The chip shown in Figure 5-14 is fabricated in TSMC 0.18um RF1P6M process. The die size is 980um×980um. It consists of a 8-bit 100MS/s pipelined ADC with 1.5 bit/stage, the triangular wave generator, and a BIST circuit. The power is divided into two parts analog and digital. The rest area is filled with decoupling capacitor to filter noise from the power supply. The performance is summarized in Table 5-4.

Table 5-4 Summary of performance

Spec.	Performance Value	Unit
Supply Voltage	1.8	V
Sampling Frequency	100M	Hz
Resolution	8	Bit
Input Range	1.6	Vpp differential
Dynamic Range	47.79	dB
SNDR (@ fin=20.9Mhz)	47.09	dB
Power Dissipation	100	mW
Power Dissipation (with BIST)	110	mW
DNL	<0.2	LSB
INL	<0.6	LSB
Chip/core area	0.98x0.98 / 0.58x0.66	mm2
Technology	0.18	um (TSMC)

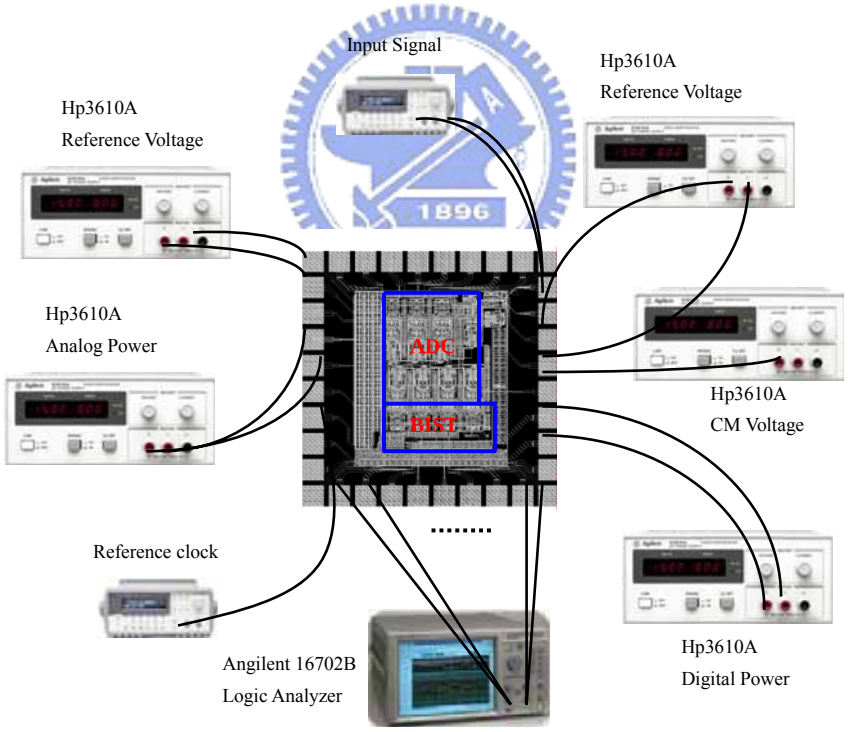
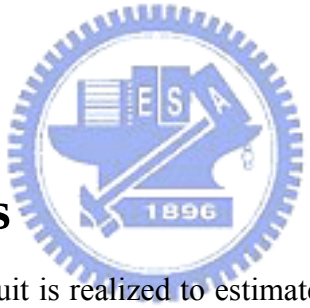


Figure 5-15 Measurement setup

Figure 5-15 introduces the measurement setup. Reset pin select the normal operation mode or BIST mode. In the normal operation mode, the logic analyzer receive the output from the ADC. In the BIST mode, the logic analyzer sends control signal to select the stage under test and receive ADC's error parameter from the chip.

Chapter 6

Conclusions



6.1 Conclusions

In this thesis a BIST circuit is realized to estimate the gain error and offset error for a pipelined ADC. By the probability analysis, 24-bit counter is necessary to measure the stage nonlinearity up to a resolution of 0.001. There are two 24-bit counters for gain error and offset error measurement. For reducing the number of pads, another 48-bit shift register is realized to transfer the results out of the chip. A 8-bit, 100MS/s pipelined ADC is designed to verify the BIST circuit.

The chip is implemented in TSMC RF0.18um technology. The ADC achieves a SNDR of $47.09\,dB$ in $100\,MS/s$, a DNL of $0.2\,LSB$, and an INL of $0.6\,LSB$. Intentional capacitor mismatch of 0.04 is induced into the pipelined stage. The linearity analysis with the BIST circuit measures the results that meet the traditional histogram method. So the BIST does work as expected.

This BIST algorithm has the potential to be the background calibration of high resolution pipelined ADC. But the hardware overhead of calibration might be a concern.

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