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碩 士 論 文

利用低溫多晶矽技術於製造具有多晶矽奈米線通道的薄膜電晶體之研究

A Study of Thin-Film Transistors with Poly-Si Nanowire Channels Fabricated by LTPS Technology

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中 華 民 國 九 六 年 五 月

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摘　要

在本論文中，我們採用兩種低溫多晶矽(LTPS)技術，來製造具有多晶矽奈米線 通道的薄膜電晶體。其中一種技術為固相結晶法(SPC)，由於此新穎的奈米線薄膜電晶體具有其特有的佈局，會使得閘極引致汲極漏電流(GIDL)成為主要的漏電機制；我們藉由引入一額外的深層離子佈植，可以有效地抑制 GIDL 的發生；另外，亦藉由活化能萃取和電場強度模擬來進一步討論其機制。另一種技術為金屬誘發側向結晶法(MILC)，和 SPC 的元件相比較，由於其通道內部結晶情形的改善，可以大幅增進元件特性；此外，在本研究中亦探討成核開口配置和退火溫度對元件特性的影響。

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ABSTRACT

In this thesis, two low-temperature poly silicon (LTPS) technologies are adopted to fabricate TFTs with poly-Si nanowire (NW) channels. One is solid phase crystallization (SPC), where gate-induced drain leakage (GIDL) is found to be the most dominant leakage mechanism due to the unique layout feature in the proposed NW-TFTs. By introducing an additional deep ion implantation (I/I), the undesirable GIDL mechanism can be suppressed effectively. Both activation energy extraction and electric field strength simulation are also investigated for further discussion. The other is metal-induced lateral crystallization (MILC). Compared with SPC device, the performance of the MILC device is dramatically enhanced owing to the improvement of the film crystallinity. Besides, the impacts of seeding window arrangement and annealing temperature are also explored in this study.

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新竹交大
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Chapter 1

Introduction

1.1 Overview of LTPS-TFTs

In the past several decades, amorphous silicon thin-film transistors (a-Si TFTs) were mainly applied to active-matrix liquid-crystal displays (AMLCDs) where each pixel contains a TFT and a capacitor in the intersection. In order to drive the AMLCDs, it is necessary to connect these pixel lines to single-crystal integrated circuits (IC's) in the periphery of the display, causing the issues of cost and reliability. Recently, polycrystalline silicon (poly-Si) TFTs become increasingly attractive owing to their higher carrier mobility compared with a-Si TFTs, allowing the fabrication of the driver circuits and the active matrix on the same substrate, thus eliminating the above-mentioned issues [1][2]. Moreover, for cost consideration, quartz should be replaced by glass as substrate by employing low-temperature poly silicon (LTPS) technology to transform a-Si into poly-Si through solid phase crystallization (SPC) [3], metal-induced lateral crystallization (MILC) [4] and excimer laser crystallization (ELC) [5]. A brief comparison between these methods is summarized in Table 1-1. Details would be explained as follows.

1.1.1 Solid Phase Crystallization (SPC)

Traditionally, the SPC process was carried out in a furnace with N_2 carrier gas at around 600 ℃ for several hours, to facilitate the crystallization of a-Si films deposited by low-pressure chemical vapor deposition (LPCVD). This is feasible because of the lower

Gibbs free energy of the crystalline phase compared with the amorphous phase [6]. Similar to most solid-state transformations, the crystallization process takes place from defects which serve as the nucleation centers, and then grows with nearby Si atoms, thus enlarging the grain size. Between two adjacent grains, a region called grain boundary (GB) is formed. It is important to note that there are GB dangling bonds and intra-grain strain bonds in poly-Si, so the conduction electron will be trapped, causing the degradation of the device performance. Hence, H_2 [7] and NH_3 [8] plasma treatments are widely applied to improve the device characteristics by repairing the trapping states with hydrogen, a process which is commonly known as hydrogenation.

1.1.2 Metal-Induced Lateral Crystallization (MILC)

Metal-induced crystallization (MIC) is a method of introducing metal as a catalyst for lowering the crystallization temperature of a-Si down to about 500 ℃. The crystallization mechanism can be classified into two types. One is using metals such as Au [9], Al [10] and Sb [11] to form eutectics with Si, and the other is using metals such as Pd [12], Ti [13] and Ni [14] to form silicides with Si. However, the MIC process has an undesirable drawback of incorporating undesirable metal impurities into crystallized Si, so it is not suitable for the fabrication of TFTs.

Recently, a novel technique called MILC was proposed to achieve the purpose of reducing the possibility of metal contamination and enlarging the grain size. In general, Ni was chosen as the catalytic material. During MILC process, $NiSi_2$ precipitate serves as heterogeneous nucleus and migrates laterally through a-Si without Ni coverage, leaving a trail of crystalline Si (c-Si). This is feasible because the chemical potential of the Ni atoms is lower at the $NiSi_2$/a-Si interface, whereas the chemical potential of the Si atoms is lower at $NiSi_2$/c-Si interface [15]. Furthermore, the lattice constant of Si and $NiSi_2$ is 5.430 Å and

5.406 Å, respectively, i.e., the lattice mismatch between Si and $NiSi_2$ is just only 0.44 %, thereby excluding the phenomenon of the misfit dislocation.

1.1.3 Excimer Laser Crystallization (ELC)

Recently, ELC has become the industrial choice for the mass production of small-sized flat-panel displays (FPDs). The standard gas mixtures and output wavelengths are ArF (193 nm), KrF (248 nm) and XeCl (308 nm). Because of the short-pulsed time and high absorption coefficient of a-Si in the UV light region, ELC can be considered as a low-temperature process by confining the heat to the silicon layer, avoiding the thermal shrinkage of the glass substrate [16].

The incident laser energy, an important parameter during ELC process, needs to exceed the threshold energy, so as to melt the surface of the a-Si film and then solidify into large grain. Several reports reveal that the crystallized silicon film is divided into two layers according to the microstructures. The upper layer is crystallized with a melt-growth process and the lower layer is crystallized with solid-phase growth process [17] [18]. Besides, with the increasing energy density, hillocks at the GBs are formed due to the mass of Si atoms transport toward GBs [19]. Owing to the interface roughness, the gate oxide integrity remains an issue.

1.2 Overview of Nanowires

The nanowire (NW), referred to a stripe structure with its cross-sectional dimension smaller than 100 nm, could be the ideal building blocks for nanoelectronics. Since the NWs possess a special feature of high surface-to-volume ratio, they are attractive for a number of applications, including nano CMOS [20], memories [21], NW-TFTs [22], biochemical sensors [23] [24] and light-emitting diodes (LEDs) [25].

Based on the fabrication method, the preparation of Si NWs could be categorized into two types, namely top-down and bottom-up, as described in the following.

(1) Top-down

This approach employs advanced lithography tools, such as deep UV, e-beam, and nanoimprint [26], to define the NW patterns, followed by an etching step to define the NW structures. Because of the excellent positioning and reproducibility of the NWs, this technique has great potential for mass production. Nevertheless, very expensive equipments and cutting-edge techniques are required. With the help of some special skills, such as thermal flow, chemical shrink and spacer patterning [27], the nano-scale patterns can also be generated indirectly by using conventional lithography tools (e.g., G-line and I-line steppers), thus reducing the cost of manufacture.

(2) Bottom-up

This approach generally utilizes the synthesis method based on vapor-liquid-solid (VLS) mechanism, including laser ablation catalyst growth [28] and chemical vapor deposition catalyst growth [29]. In VLS, liquid metal nanocluster acts as a favorite site for absorbing gas-phase reactants, and then grows into NWs as the supersaturation is reached. Afterwards, the NWs are harvested and dispersed into a solution, followed by the methods used to assemble and align the NWs on the desired substrate, such as electric-field-directed assembly [30], microfluidic channel [31] and Langmuir-Blodgett (LB) technique [32]. However, this approach is limited by complex integration that requires the transfer and positioning of individual NW and making reliable ohmic contacts.

1.3 Thesis Organization

In this thesis, NW-TFTs originally proposed by Advanced Device Technology Laboratory (ADTL), NCTU were adopted [33]. Both SPC and MILC techniques were utilized

to crystallize the a-Si channels. Without using expensive lithography equipments, TFTs with nano-scale channels can be prepared. Besides, this approach is compatible with modern semiconductor processing.

The overview of LTPS-TFTs and NWs is described in Chapter 1. In Chapter 2, we briefly explain the device structure and the process flow. In Chapter 3, we discuss the effect of an additional deep ion implantation (I/I) on the off-state leakage of the SPC NW-TFTs. In Chapter 4, the MILC NW-TFTs with different MILC open window arrangements and annealing temperatures were investigated. Finally, we summarize the conclusions and the suggested future work in Chapter 5.

Chapter 2

Device Fabrication and Measurement

2.1 Device Structure and Process Flow

6-inch (100)-Si wafers capped with 100 nm wet oxide were used as the starting substrates, followed by the definition of a 100 nm in-situ-doped n^+ poly-Si as gate electrode. After RCA clean, 38 nm TEOS and 100 nm a-Si were grown by LPCVD system sequentially. To reduce the S/D resistance, all wafers received a P_{31}^+ implant with a dose of $1x10^{15}$ cm^{-2} and a low implant energy of 15 keV. Wafers were then divided into two splits according to the crystallization method.

(1) SPC NW-TFTs

One of the splits was fabricated by SPC. Based on I/I condition, wafers were also classified into two splits. One split of wafers further received an additional P_{31}^+ implant with a dose of $3x10^{13}$ cm^{-2} at 40 keV, while the other split was skipped from receiving this extra implant. The purpose of the deep I/I is to increase the dopant concentration in the drain region near the gate oxide. Subsequently, S/D regions were defined by photolithography, and then etched by reactive ion etching (RIE), during which the NW channels abutting the sidewall of the gate were formed simultaneously. Wafers were then covered with a 300 nm low temperature oxide (LTO) as passivation layer. To transform the a-Si channels into polycrystalline state, SPC was performed in a N_2 ambient at 600 ℃ for 24 hr. After standard metallization, wafers were sintered in forming gas at 400 ℃ for 30 min. Fig. 2-1 illustrates the device structure of the NW-TFT (a) without and (b) with deep I/I, with labels of the

projected range of the implant (the dashed line) in the S/D regions as determined by the implant energy.

(2) MILC NW-TFTs

The other split was fabricated by MILC. Briefly, after S/D implantation, NW channels were defined by RIE etching. Wafers were then covered with a 100 nm LTO as Ni barrier layer. MILC open windows were defined by photolithography, and then etched by 50:1 HF for 4 min. Subsequently, 5 nm Ni was sputtered onto the wafers by physical vapor deposition (PVD) system. To transform the a-Si channels into polycrystalline state, MILC was performed in a N_2 ambient at 525 ℃ or 550 ℃ for 21 hr. The unreacted Ni was removed by H_2SO_4/H_2O_2 solution at 120 ℃ for 10 min, followed by 200 nm LTO as passivation layer. An additional annealing step in a N_2 ambient at 600 ℃ for 6 hr was adopted to ensure the activation of the dopants in the S/D regions. After standard metallization, wafers were sintered in forming gas at 400 ℃ for 30 min. Fig. 2-2 illustrates the (a) bird's view and (b) top view of the NW-TFT with asymmetric MILC open window at the source terminal. Note that a parameter called offset, OS, is defined as the shortest horizontal distance between the MILC open window and the channel. In this study, OS was split into 0.5, 1.5, 2.5, 4 and 5.5 μm.

In this experiment, the NW channels, like the spacers in the MOSFETs, are formed by RIE system. The feature size is determined by several factors, such as gate height, a-Si thickness and over-etching time. Two important parameters called channel width and thickness are 50 nm and 55 nm, respectively, as the transmission electron microscopy (TEM) image shown in Fig. 2-3.

2.2 Measurement Setup and Electrical Characterization

HP 4156A Semiconductor Parameter Analyzer was employed to perform the electrical characterizations of the NW-TFTs. During all measurements, the temperature was controlled

at a stable value by temperature-regulated hot chuck.

From the measured I_D-V_G curve at V_D = 0.5 V, the parameters of the NW-TFTs including threshold voltage (V_{th}), subthreshold swing (SS), field-effect mobility (μ_{FE}) can be extracted according to their definition.

Here, the threshold voltage (V_{th}), calculated by the constant current method, is defined as the gate voltage (V_G) needed to achieve a drain current (I_D) of (W/L)×100 nA, i.e.

$$V_{th} = V_G @ I_D = \frac{W}{L} \times 100nA \tag{2-1}$$

where W and L are the channel width and length, respectively.

The subthreshold swing (SS) can be calculated from the subthreshold current in the weak inversion region by

$$SS = \frac{\partial V_G}{\partial (\log I_D)} \tag{2-2}$$

Finally, the field-effect mobility (μ_{FE}) is determined by

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_D} \tag{2-3}$$

where g_m is the maximum transconductance and C_{ox} is the gate oxide capacitance per unit area.

Chapter 3

NW-TFTs Fabricated by SPC

3.1 Fundamental Characteristics of SPC NW-TFTs

The operational principles of the novel NW-TFTs are similar to those of the conventional TFTs. The n^+ ploy-Si side-gate is used to modulate the channel potential, thus controlling the switching behavior of the device. The transfer and output characteristics of SPC NW-TFTs are shown in Figs. 3-1(a) and (b), respectively. Fig. 3-1(a) reveals that good device performance with high on/off current ratio (6.23×10^5) and reasonable subthreshold swing (0.83 V/dec) is achieved. Since the cross-sectional area of the NW channel is quite small, low leakage current was originally expected. However, the off-state current is anomalous high and depends on both the gate and drain bias. The leakage mechanism will be carefully examined and analyzed in the following sections. In Fig. 3-1(b), a kink effect is observed. Under high electric field region, the grain barrier heights for both sides of the grain boundary become asymmetric and the grain barrier height near the source side will be lower than that near the drain side. There will be extra carriers injecting from the source through the side with lower grain barrier into the channel. This phenomenon is so called the drain-induced grain barrier lowering (DIGBL) effect [34] [35]. Furthermore, the impact ionization mechanism initiated by the DIGBL current may cause an anomalous current increase in the saturation region.

3.2 Leakage Mechanisms

In poly-Si channels, the band diagram modulated by the drain and gate bias would affect

the off-state characteristics of the devices. Fig. 3-2 illustrates two possible regions for leakage generation in our novel NW-TFTs. One occurs in the drain/channel junction, and the other occurs in the gate-to-drain overlap region. Detail mechanisms would be briefly discussed as followed.

3.2.1 Drain/Channel Junction

This mechanism occurs laterally from the channel to the drain via trap-assisted conduction and is strongly dependent on the magnitude of the drain bias. According to the electrical field strength at drain/channel junction, there are generally three cases as illustrated in Figs. 3-3(a), (b) and (c):

(a) Under low electric field regime: Electrons are thermally excited from valence band into midgap states located at the grain boundaries (GBs), and then the trapped electrons are emitted to the conduction band in the same way, i.e., the so called "pure thermal emission" or "thermal generation".

(b) Under medium electric field regime: Since the increasing drain bias pulls the energy band at the drain terminal down, the thermally excited electrons from the valence band to trap states can tunnel to the conduction band through the reduced barrier width. This is known as the thermionic field emission.

(c) Under high electric field regime: While the band-bending is pulled more severely, the electrons can easily tunnel from the valence band to the conduction band with the aid of the trap states. This is called field emission or tunneling.

In poly-Si channel, the presence of the trap states in the band gap plays an important role on the leakage current. The thermal emission current is proportional to the intrinsic carrier concentration of silicon (n_i), which is proportional to $\exp[-E_g/2kT]$ (where E_g is the energy band gap of silicon, k is the Boltzmann constant, and T is the temperature in Kelvin) [36]. For

this reason, the activation energy of the pure thermal emission current should be approximately equal to $E_g/2$. In addition, the pure thermal generation current is nearly independent of gate voltage. On the other hand, the activation energy should be approximately equal to E_g, if the channel is made up of ideal single crystal Si with no GBs [37].

3.2.2 Gate-to-Drain Overlap Region

This mechanism exists in the gate-to-drain overlap region and depends on both the magnitude of the gate and drain bias. According to the electrical field strength inside the drain terminal, there are generally three conduction cases as illustrated in Figs. 3-4(a), (b) and (c). In fact, this mechanism is similar to that described in Section 3.2.1.

For a fixed drain bias, as the gate is more negatively biased (or alternatively, for a fixed gate bias, the drain is more positively biased), i.e., increasing the voltage difference between the gate and drain ($|V_{GD}|$), a depletion region would be formed in the n-type drain overlapping the gate. Under high electric field regime (Fig. 3-4(c)), the quasi-Fermi level at the channel/oxide interface shifts nearer to the valance band edge. This results in the generation of electron-hole pairs via the tunneling of the valance band electrons into the conduction band, i.e., band-to-band tunneling. Here, it is important to emphasize that this mechanism entirely takes place in the Si drain region instead of tunneling through the gate oxide. This is known as the gate-induced drain leakage (GIDL) [38].

The electric field distribution inside the drain terminal that directly account for the GIDL mechanism can be modulated by two major processing parameters. One is the dielectric thickness between the gate and drain. Since the dielectric has the ability to sustain voltage drop, lower electric field strength would be achieved by increasing its thickness. The other is the drain doping concentration. This is because the doping level determines the position of the Fermi level and influences the depletion width. Besides, the gate-to-drain overlap area and

defects density are two important factors that need to be taken into consideration.

3.3 Effects of Deep Ion Implantation

In our previous work, we have identified that GIDL is the most dominant leakage mechanism in our novel NW-TFTs due to their unique layout feature [39][40]. It was found that this leakage current could be restrained by inserting a Si_3N_4 hard mask (HM) between the gate and drain to reduce the electric field strength in the drain region [41]. In this study, we show that by carefully adjusting the implant energy, the undesirable GIDL mechanism in NW-TFTs could also be effectively suppressed.

Fig. 3-5 compares the off-state currents between devices (a) without and (b) with deep I/I, with various gate widths (GW), a structural parameter defined in Fig. 2-2(b). Fig. 3-6(a) shows the leakage currents of NW-TFTs, extracted from Fig. 3-5, without and with deep I/I as a function of GW at $|V_{GD}|$ = 8V. Furthermore, in Fig. 3-6(b), a parameter called off-state current ratio (OSCR),

$$\text{OSCR} = \frac{I_D}{I_D(\text{GW} = 0.8\mu\text{m})} \tag{3-1}$$

which is the off-state current normalized to that with GW = 0.8 μm, is also shown as a function of GW. It is found that the off-state characteristics of NW-TFTs with deep I/I are nearly independent of the gate width. In our previous work, we have shown that the GIDL leakages are mainly constricted in the gate-to-drain overlap region with an area roughly proportional to the GW. The results shown in Figs. 3-5 and 3-6 indicate that the GIDL effect is greatly suppressed in devices with deep I/I. This is attributed to the increase of the dopant concentration in the drain region near the gate oxide, leading to the reduction in the depletion width and electric field strength.

Figures 3-7(a)~(f) show the dependence of the leakage current on the drain voltage for

devices without and with deep I/I at V_G = 0, -1, -2, -3, -4 and -5 V, respectively. It reveals that the output characteristics are essentially the same for both splits under low V_G, due to the low electric field strength. On the other hand, as a highly negative gate bias is applied, the GIDL mechanism becomes significant and the effect of the deep I/I becomes evident, as obviously shown in Fig. 3-7(f).

Based on the results presented above, Figs. 3-8(a) and (b) schematically depict the major leakage current paths in the drain side of the NW-TFTs (a) without and (b) with deep I/I, respectively. As shown in Fig. 3-8(a), Path A illustrates the occurrence of leakage current owing to the band-to-band or trap-assisted tunneling (GIDL) mechanism. These paths are easily turned on due to the very low dopant concentration in regions near the oxide interface, and can be shut off with the implementation of deep I/I in the drain side. When this is done, the leakage paths are then confined in a narrow region near the gate sidewall (Path B), as shown in Fig. 3-8(b). As a result, the off-state leakage becomes independent of the gate width, consistent with the experimental data observed in this work.

3.4 Activation Energy Extraction

In order to gain a deeper insight into the leakage mechanism, the off-state activation energy is obtained according to the governing equation of off-state current, activation energy and temperature [42], defined as

$$I_{off} = I_o \exp(-\frac{E_a}{kT}) \tag{3-2}$$

where I_o is the constant independent of temperature, E_a is the drain current activation energy, k is the Boltzman constant and T is the absolute temperature. The equation can also be expressed as

$$\ln(I_{off}) = \ln(I_o) + (-\frac{E_a}{kT}) \tag{3-3}$$

The off-state transfer characteristics of NW-TFTs (a) without and (b) with deep I/I measured at 25, 50, 75, 100, 125 ℃ are exhibited in Fig. 3-9. Next, we use equation (3-3) to plot the Arrhenius plots of off-state currents for NW-TFTs without and with deep I/I at various gate biases, which are shown in Figs. 3-10(a) and (b), respectively. From the date lines in Fig. 3-10, the activation energies (E_a) can be extracted from their slope, and are summarized in Fig. 3-11 for comparison. It indicates that the activation energy gradually decreases with a more negative gate bias due to GIDL mechanism. Moreover, it's worth noting that the activation energy of NW-TFTs without deep I/I shows a stronger dependence on the gate voltage, in contrast to that with deep I/I. It's because the electric field strength and depletion width are reduced by implanting an additional deep I/I, hence the undesirable GIDL mechanism can be suppressed effectively in NW-TFTs.

3.5 Electric Field Strength Simulation

ISE-TCAD, a powerful simulation tool for semiconductor process and device, was employed to simulate the electric field strength in the gate-to-drain overlap region at different dopant concentration in the drain terminal. We set the thickness of the drain and gate oxide to be 100 nm and 38 nm, respectively, the same as the experimentally measured thickness. For simplification, the dopant concentration was considered to be a uniform distribution. The gate and drain were then biased at -5 V and 3 V, respectively, i.e., in the off-state operation. After mesh and run step, the simulation results could be obtained.

Since we adopt n^+ poly-Si as the gate material, the voltage difference $|V_{GD}|$ should be ideally shared by the drain and gate oxide besides the gate. In Fig. 3-12, the dependence of the electric field distribution in the drain and gate oxide on the dopant concentration is shown. Specifically, the electric field strength inside the drain terminal is the most interesting parameter for understanding GIDL mechanism. For GIDL to take place, the drain doping level

should be modulated to about 10^{18} cm^{-3}. If the doping level is much lower than this, the depletion width and tunneling barrier are too wide, eliminating the probability of band-to-band tunneling. On the other hand, if the dopant concentration is very high, $|V_{GD}|$ drops most of its voltage in the gate oxide instead of drain, as shown in Fig. 3-13. Owing to the suppression of the band-bending in the drain region, the GIDL occurrence can also be excluded. Finally, with the help of simulation, we succeed in explaining why GIDL can be suppressed in the novel SPC NW-TFTs by introducing an additional deep I/I.

Chapter 4

NW-TFTs Fabricated by MILC

4.1 Basic Characteristics of MILC NW-TFTs

Based on either one-sided or two-sided open window for MILC, the NW-TFTs were classified as metal-induced unilateral crystallization (MIUC) or metal-induced bilateral crystallization (MIBC). Furthermore, the measurement setup can also be divided into two splits called “Forward” and “Reverse” modes based on the reversal of the S/D. Hence, as shown in Fig. 4-1, there are four different kinds of MILC open window arrangements, including (a) MIUC (Forward), (b) MIUC (Reverse), (c) MIBC (Forward) and (d) MIBC (Reverse). In fact, MIBC (Forward) and MIBC (Reverse) should show nominally identical performance.

The transfer characteristics of MIUC (Forward) and MIUC (Reverse) NW-TFT are shown in Figs. 4-2(a) and (b), respectively. In Fig. 4-2(a), the device performance is dramatically enhanced as compared with SPC NW-TFTs described in Section 3.1. Higher on/off current ratio (5.17×10^6) and better subthreshold swing (0.27 V/dec) are obtained. We believe it is due to the improvement of the crystallinity in the channel. Since the migration of the $NiSi_2$ precipitates is confined by the oxide around the NW channel, the crystallinity of the channel can be seen as a quasi-single-crystalline Si. Furthermore, the needle-like grain with crystallization direction along the NW channel is formed, so the number of barrier at the GBs where conduction electrons must overcome is reduced. As a result, the extracted field-effect mobility of MIUC (Forward) device is 60.25 cm^2/V-s, which is much higher than 5.82

cm^2/V-s of the SPC counterpart. In Fig. 4-2(b), anomalously high leakage current is observed in contrast to Fig. 4-2(a). The detail analysis will be described in the next section.

The GB trapping model proposed by J. Levinson et al. was used to determine the trap density [43]. When the current is governed by thermionic emission around GBs in poly-Si, the drain current in the linear region is given by

$$I_D = \frac{W}{L} V_D C_{ox} V_G \mu_o \exp\left(-\frac{q^3 N_t^{\,2} t}{8\varepsilon_s kTC_{ox} V_G}\right) \quad (4\text{-}1)$$

where μ_o is the pre-exponential factor, q is the electric charge, N_t is the carrier trap-state density per unit area, t is the channel thickness and ε_s is the semiconductor permittivity. In Fig. 4-3, the plot of $\ln(I_D/V_G)$ versus $(1/V_G)$ for SPC and MIUC (Forward) NW-TFTs is shown. According to equation (4-1), we can extract N_t from the slope of the data line. The result reveals that the N_t of MILC device is about one order smaller than that of SPC device. Therefore, MILC process can dramatically improve the crystallinity of the poly-Si NW channel and enhance the device performance. Finally, major device parameters are extracted and summarized in Table 4-1.

4.2 Effects of MILC Open Window Arrangement

Since MILC open window contains high undesirable Ni contamination, its location would greatly influence the off-state characteristics of the devices. From the configurations illustrated in Fig. 4-1, the effect of the seeding window arrangement on the leakage current can be carefully addressed.

In Fig. 4-4, the off-state leakage current as a function of the offset length for devices fabricated by MIUC (Forward) and MIUC (Reverse) is shown. It reveals that the leakage current of MIUC (Reverse) NW-TFTs is about two orders larger than that of MIUC (Forward) NW-TFTs. It's mainly due to the fact that the MIC region is just situated on the gate-to-drain

overlap region. The Ni-related species accumulated at the inter- and intra-grains may provide more deep states in the band gap of the Si, causing severe trap-assisted tunneling leakage mechanism. On the other hand, note that the leakage current of MIUC (Forward) and MIUC (Reverse) NW-TFTs is independent of and dependent on the offset length, respectively. From the SEM image shown in Fig. 4-5, a continuous boundary at MIC/MILC interface can be observed clearly after Secco etch [44]. If MILC open window is located at the source terminal, the highly defective MIC/MILC interface is located far away from the drain terminal. The trap states in the drain/channel junction are considered to be identical, so the leakage current is almost independent of the offset length. If MILC open window is located at the drain terminal, the leakage current caused by MIC/MILC interface can be effectively eliminated as long as the offset length is larger than 1.5 μm (Fig. 4-4). Even so, the most effective method to decrease the leakage current is by deliberately arranging MILC open window at the source terminal.

Fig. 4-6 compares the off-state leakage currents for devices fabricated by MIBC (Forward), MIBC (Reverse) and MIUC (Reverse) with different offset lengths. Note that these three splits have almost identical trend and the magnitude of the leakage current. It implies that the leakage current is not influenced by the existence of a MILC open window at the source terminal. After all, the electric field strength of the source side is quite small as compared with that of the drain side. There would be no leakage path induced by trap-assisted tunneling at the source terminal. Hence, the drain side seeding window plays an important role on the off-state performance.

4.3 Effects of Annealing Temperature

From the TEM image shown in Fig. 4-7, we can observe the crystallinity of the NW channel. The inserting figure shows the SPC occurrence in the MILC front. In fact, the

poly-Si NW channel contains grains formed by SPC and MILC simultaneously. It is because the a-Si channel can easily generate heterogeneous nucleus with surrounding oxide during MILC process. As time progresses, the migration of $NiSi_2$ precipitates can't be extended freely due to the occurrence of several small grains formed by SPC. Therefore, there exists a trade-off between the rate of MILC and SPC. Furthermore, owing to the difference between the activation energy for SPC and MILC occurrence, the length of MILC region can be optimized by modulating the annealing temperature.

In Fig. 4-8, on-current as a function of the channel length for devices annealed at 525 and 550 ℃ is shown. It is reasonable that the on-current increases with decreasing channel length. Moreover, note that devices annealed at 525 ℃ exhibit higher on-current than those annealed at 550 ℃. This can be explained with the illustrations of Fig. 4-9, which show the crystallinity of the NW channel performed at (a) 550 and (b) 525 ℃ during MILC process. By lowering the annealing temperature, SPC is suppressed effectively, and MILC length can be extended without the retardation of the SPC grains. As a result, the effective barrier number in NW channels can be reduced, so the on-current increases.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this study, the conduction mechanisms of off-state leakage in the new NW-TFTs are studied. Our results indicate that GIDL is the main origin of the leakage, and is sensitive to the area of gate-to-drain overlap region, the dopant concentration, and the strength of electric field near the oxide interface. We also demonstrate that such leakage can be suppressed effectively by introducing an additional high energy I/I. Moreover, both activation energy extraction and electric field strength simulation are investigated to further discuss the experimental results.

MILC method is employed to dramatically improve the film crystallinity of the NW channel. Because the needle-like grain has the same direction as the conduction electron, significant enhancement in device performance can be achieved. We also observe that MILC open window arrangement is important in affecting the off-state characteristics. The results indicate that the source side seeding window is a better choice than the drain side one owing to the elimination of the trap-assisted conduction. Besides, SPC occurrence in the MILC front would retard the grain growth. By lowering the annealing temperature, the suppression of SPC mechanism can extend MILC grain length and improve the on-current.

5.2 Future Work

The development and characterization of NW-TFTs with SPC and MILC channels have

been studied in this thesis. To further enhance the device performance, some suggestions for future work are listed below.

1. Several reports have revealed that MILC rate can be enhanced by incorporating boron into a-Si channel [45] [46]. It is interesting to explore the possibility of improving the characteristics of the long channel devices through implanting BF_2^+ into NW channel.
2. Both SPC and MILC techniques have succeeded in fabricating NW-TFTs with excellent performance. Another interesting method called ELC can also be explored to fabricate devices for comparison.
3. The proposed novel device has great potential for the application of biological and chemical sensor. In order to achieve the sensing purpose quantitatively, the device reliability mechanism still needs to be studied and identified.

References

[1] S. D. Brotherton, "Polycrystalline silicon thin film transistors," *Semicond. Sci. Technol.*, vol. 10, pp. 721-738, 1995.

[2] A. G. Lewis, D. D. Lee and R. H. Bruce, "Polysilicon TFT circuit design and performance," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1833-1842, 1992.

[3] A. Mimura, N. Konishi, K. Ono, J. I. Ohwada, Y. Hosokawa, Y. A. Ono, T. Suzuki, K. Miyata and H. Kawakami, "High performance low-temperature poly-Si n-channel TFT's for LCD," *IEEE Trans. Electron Devices*, vol. 36, pp. 351-359, 1989.

[4] S. W. Lee and S. K. Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *IEEE Electron Device Lett.*, vol. 17, pp. 160-162, 1996.

[5] T. Sameshima, M. Hara and S. Usui, "XeCl excimer laser annealing used to fabricate poly-Si TFT's," *Jpn. J. Appl. Phys.*, vol. 28, pp. 1789-1793, 1989.

[6] M. K. Hatalis and D. W. Greve, "Large grain polycrystalline silicon by low-temperature annealing of low-pressure chemical vapor deposited amorphous silicon films," *J. Appl. Phys.*, vol. 63, pp. 2260-2266, 1988.

[7] I. W. Wu, A. G. Lewis, T. Y. Huang and A. Chiang, "Effects of trap-state density reduction by plasma hydrogenation in low-temperature polysilicon TFT," *IEEE Electron Device Lett.*, vol. 10, pp. 123-125, 1989.

[8] H. C. Cheng, F. S. Wang and C. Y. Huang, "Effects of NH_3 plasma passivation on n-channel polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 44, pp. 64-68, 1997.

[9] L. Hultman, A. Robertsson, H. T. G. Hentzell, I. Engström and P. A. Psaras, "Crystallization of amorphous silicon during thin-film gold reaction," *J. Appl. Phys.*, vol. 62, pp. 3647-3655, 1987.

[10] G. Radnoczi, A. Robertsson, H. T. G. Hentzell, S. F. Gong and M. A. Hasan, "Al induced crystallization of *a*-Si," *J. Appl. Phys.*, vol. 69, pp. 6394-6399, 1991.

[11] S. F. Gong, H. T. G. Hentzell, A. E. Robertsson, L. Hultman, S. E. Hörnström and G. Radnoczi, "Al-doped and Sb-doped polycrystalline silicon obtained by means of metal-induced crystallization," *J. Appl. Phys.*, vol. 62, pp. 3726-3732, 1987.

[12] R. J. Nemanichi, C. C. Tsai, M. J. Thompson and T. W. Sigmon, "Interference enhanced Raman scattering study of the interfacial reaction of Pd on a-Si:H," *J. Vac. Sci. Technol.*, vol. 19, pp. 685-688, 1981.

[13] R. J. Nemanichi, R. T. Fulks, B. L. Stafford and H. A. Vander Plas, "Initial reactions and silicide formation of titanium on silicon studied by Raman spectroscopy," *J. Vac. Sci. Technol. A*, vol. 3, pp. 938-941, 1985.

[14] Y. Kawazu, H. Kudo, S. Onari and T. Arai, "Low-temperature crystallization of hydrogenated amorphous silicon induced by nickel silicide formation," *Jpn. J. Appl. Phys.*, vol. 29, pp. 2698-2704, 1990.

[15] C. Hayzelden and J. L. Batstone, "Silicide formation and silicide-mediated crystallization of nickel-implanted amorphous silicon thin films," *J. Appl. Phys.*, vol. 73, pp. 8279-8289, 1993.

[16] A. A. D. T. Adikaari and S. R. P. Silva, "Thickness dependence of properties of excimer laser crystallized nano-polycrystalline silicon," *J. Appl. Phys.*, vol. 97, pp. 114305, 2005.

[17] K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko and K. Hotta, "High-performance TFT's Fabricated by XeCl excimer laser annealing of hydrogenated amorphous-silicon film," *IEEE Trans. Electron Devices*, vol. 36, pp. 2868-2872, 1989.

[18] S. D. Brotherton, D. J. McCulloch, J. B. Clegg and J. P. Gowers, "Excimer-laser-annealed poly-Si thin-film transistors," *IEEE Trans. Electron Devices*, vol. 40, pp. 407-413, 1993

[19] C. T. Angelis, C. A. Dimitriadis, M. Miyasaka, F. V. Farmakis, G. Kamarinos, J. Brini

and J. Stoemenos, “Effect of excimer laser annealing on the structure and electrical properties of polycrystalline silicon thin-film transistors,” *J. Appl. Phys.*, vol. 86, pp. 4600-4606, 1999.

[20] F. L. Yang et al., “5nm-gate mamowire FinFET,” *VLSI Symp. Tech. Dig.*, pp.196-197, 2004.

[21] X. Duan., Y. Huang and C. M. Lieber, “Nonvolatile memory and programmable logic from molecule-gated nanowires,” *Nano Lett.*, vol. 2, pp. 497-490, 2002.

[22] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles and J. L. Goldman, “High-performance thin-film transistors using semiconductor nanowires and nanoribbons,” *Nature*, vol. 425, pp. 274-278, 2003.

[23] Y. Cui, Q. Wei, H. Park and C. M. Lieber, “Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species,” *Science*, vol. 293, pp. 1289-1292, 2001.

[24] Z. Li, Y. Chen, X. Li, T. I. Kamins, K. Nauka and R. S. Williams, “Sequence-specific label-free DNA sensors based on silicon nanowires,” *Nano Latt.*, vol. 4, pp. 245-247, 2004.

[25] M. C. McAlpine, R. S. Friedman, S. Jin, K. H. Lin, W. U. Wang and C. M. Lieber, “High-performance nanowire electronics and photonics on glass and plastic substrates,” *Nano Lett.*, vol. 3, pp. 1531-1535, 2003.

[26] M. D. Austin, H. Ge, W. Wu, M. Li, Z. Yu, D. Wasserman, S. A. Lyon and S. Y. Chou, “Fabrication of 5 nm linewidth and 14 nm pitch features by nanoimprint lithography,” *Appl. Phys. Lett.*, vol. 84, pp.5299-5301, 2004.

[27] Y. K. Choi, T. J. King and C. Hu, “A spacer patterning technology for nanoscale CMOS,” *IEEE Trans. Electron Devices*, vol. 49, pp. 436-441, 2002.

[28] A. M. Morales and C. M. Lieber, “A laser ablation method for the synthesis of crystalline semiconductor nanowires,” *Science*, vol. 279, pp. 208-211, 1998.

[29] D. Wang, Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P. McIntyre, T. Krishnamohan and K. C. Saraswat, "Germanium nanowire field-effect transistors with SiO_2 and high-κ H_fO_2 gate dielectrics," *Appl. Phys. Lett.*, vol. 83, pp. 2432-2434, 2003.

[30] X. Duan, Y. Huang, Y. Cui, J. Wang and C. M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," *Nature*, vol. 409, pp.66-69, 2001.

[31] Y. Huang, X. Duan, Q. Wei, C. M. Lieber, "Directed assembly of one-dimensional nanostructures into functional networks," *Science*, vol. 291, pp. 630-633, 2001.

[32] A. Tao, F. Kim, C. Hess, J. Goldberger, R. He, Y. Sun, Y. Xia and P. Yang, "Langmuir-Blodgett silver nanowire monolayers for molecular sensing using surface-enhanced Raman spectroscopy," *Nano Lett.*, vol. 3, pp. 1229-1233, 2003.

[33] H. C. Lin, M. H. Lee, C. J. Su, T. Y. Huang, C. C. Lee and Y. S. Yang, "A simple and low-cost method to fabricate TFTs with poly-Si nanowire channel," *IEEE Electron Device Lett.*, vol. 26, pp. 643-645, 2005.

[34] P. S. Lin, J. Y. Guo and C. Y. Wu, "A quasi-two-dimensional analytical model for the turn-on characteristics of polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 666-674, 1990.

[35] H. L. Chen, C. Y. Wu, "A new I-V model considering the impact-ionization effect initiated by the DIGBL current for the intrinsic n-channel poly-Si TFT," *IEEE Trans. Electron Devices*, vol. 46, pp. 722-728, 1999.

[36] S. M. Sze, "Physics of Semiconductor Devices," Wiley, New York, 1981.

[37] M. Yazaki, S. Takenaka and H. Ohshima, "Conduction mechanism of leakage current observed in metal-oxide-semiconductor transistors and poly-Si thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 31, pp. 206-209, 1992.

[38] T. Y. Chan, J. Chen, P. K. Ko and C. Hu, "The impact of gate-induced drain leakage current on MOSFET scaling," *IEDM Tech. Dig.*, pp. 718-721, 1987.

[39] H. C. Lin, M. H. Lee, C. J. Su, H. H. Tsai, J. J. Hung and R. C. T. Lin, "Off-state mechanism in novel Si nanowire transistors with solid-phase crystallized channels," *SNW*, pp. 75-76, 2006.

[40] H. C. Lin, M. H. Lee, C. J. Su and S. W. Shen, "Fabrication and characterization of nanowire transistors with solid-phase crystallized poly-Si channels," *IEEE Trans. Electron Devices*, vol. 53, pp. 2471-2477, 2006.

[41] M. H. Lee, H. H. Tsai, C. J. Su, J. J. Hung, H. C. Lin and T. Y. Huang, "Process and material modifications for leakage current reduction in poly-Si thin-film transistors with nanowire channels," *IEDMS*, pp. 19-20, 2006.

[42] K. R. Olasupo and M. K. Hatalis, "Leakage current mechanism in sub-micron polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 43, pp. 1218-1223, 1996.

[43] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.*, vol. 53, pp. 1193-1202, 1982.

[44] F. Secco d'Aragona, "Dislocation etch for (100) planes in silicon," *J. Electrochem. Soc.*, vol. 119, p. 948-951, 1972.

[45] T. Ma and M. Wong, "Dopant and thickness dependence of metal-induced lateral crystallization of amorphous silicon films," *J. Appl. Phys.*, vol. 91, pp. 1236-1241, 2002.

[46] J. S. Ahn, Y. G. Yoon and S. K. Joo, "The effect of dopants on the microstructure of polycrystalline silicon thin film grown by MILC method," *J. Crystal Growth*, vol. 290, pp. 379-383, 2006.

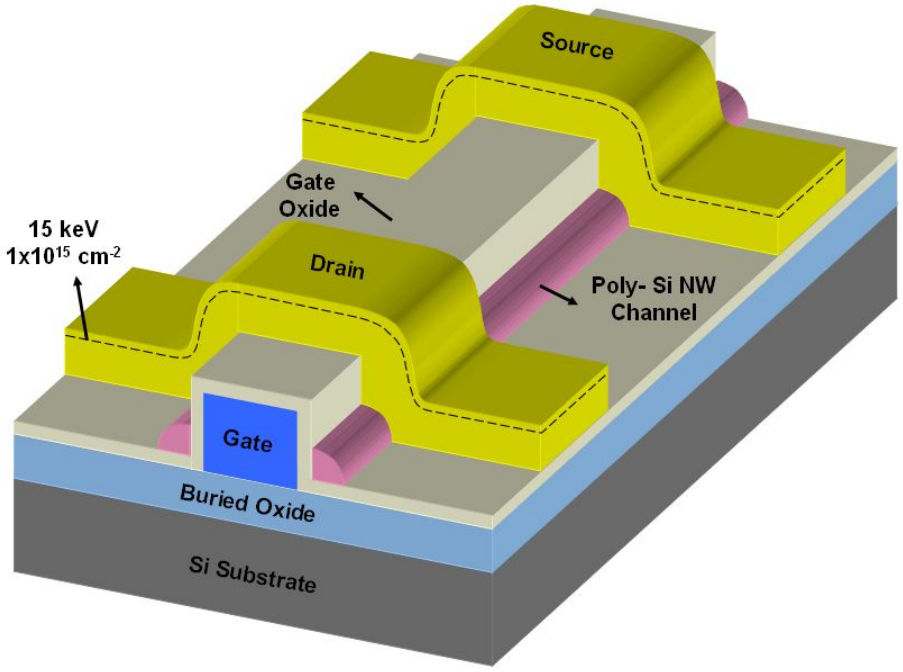
Table 1-1 The comparisons between SPC, MILC and ELC.

	SPC	MILC	ELC
Time	Long	Medium	Short
Temperature	High	Medium	Low
Parameter	Annealing temperature Deposition Condition	Annealing temperature Si film thickness	Energy density Light source
Grain size	Small	Large	Medium
Cost	Low	Low	High
Throughput	Batch	Batch	Single
Issue	Many defects	Metal contamination	Expensive

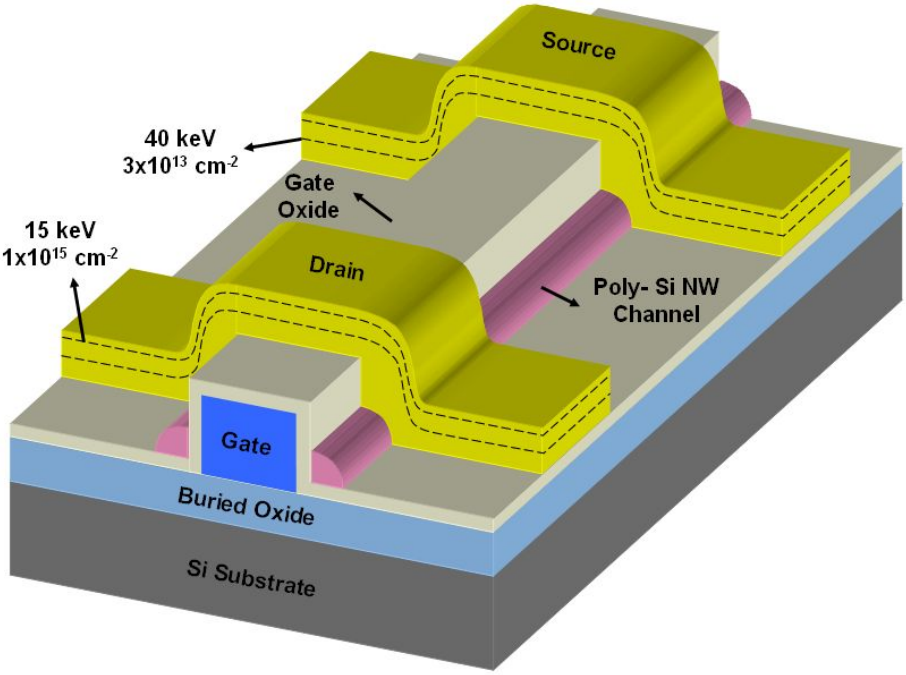
Table 4-1 Major parameters for SPC, MIUC (Forward) and MIUC (Reverse) NW-TFTs.

	SPC	MIUC (Forward)	MIUC (Reverse)
V_{th} (V)	4.19	0.13	0.53
SS (V/dec)	0.83	0.27	0.51
μ_{FE} (cm^2/V-s)	5.82	60.25	60.67
I_{on}/I_{off} (A/A)	6.23×10^5	5.17×10^6	3.82×10^4
N_t (cm^{-2})	1.77×10^{12}	2.48×10^{11}	3.28×10^{11}

* All parameters were extracted at V_D = 0.5 V except for the on/off current ratio, I_{on}/I_{off}, which was extracted at V_D = 3 V. I_{off} is defined as the minimum drain current for convenience.

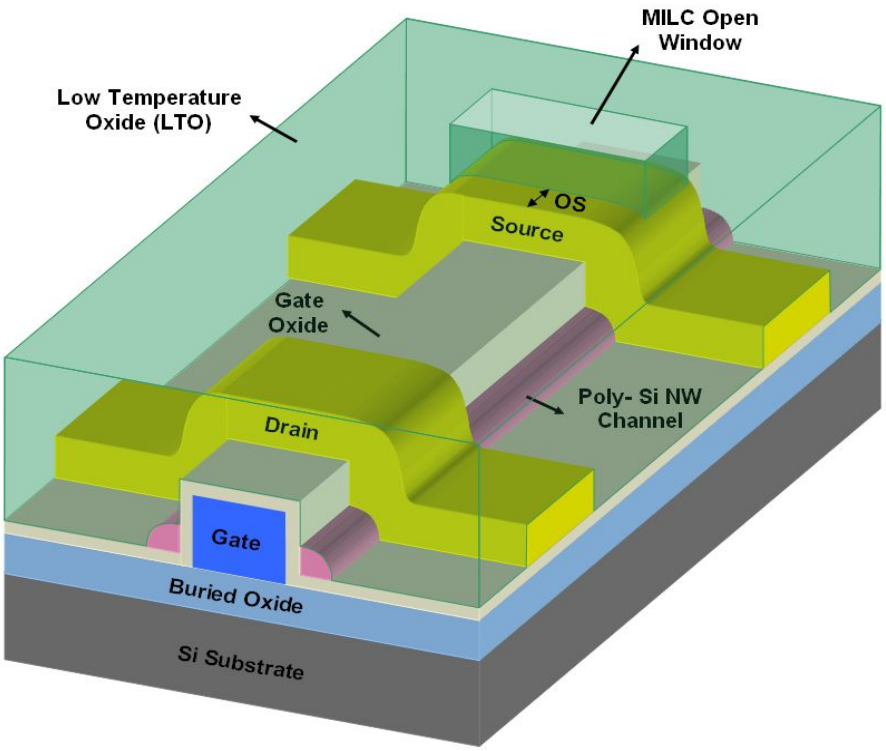


(a)

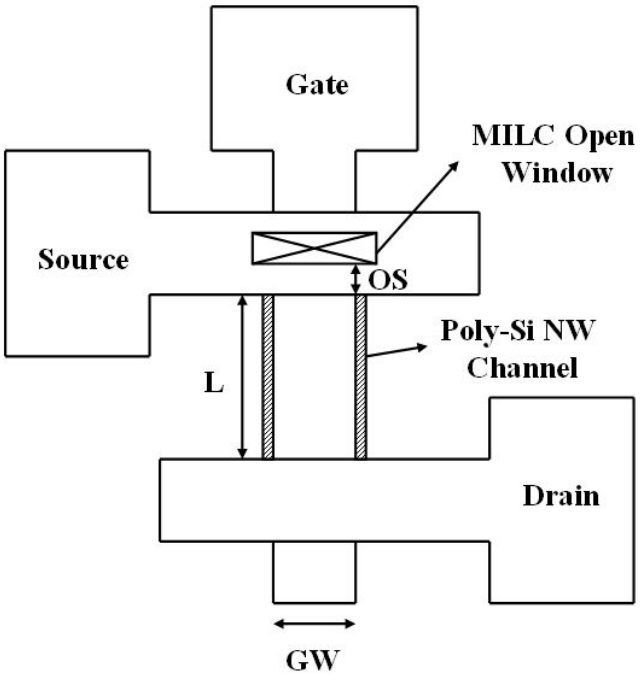


(b)

Fig. 2-4 Schematic diagram of the NW-TFT (a) w/o and (b) w/ deep I/I. The dash lines indicate the peak positions of the dopant concentration.



(a)



(b)

Fig. 2-2 (a) Bird's view and (b) top view of the NW-TFT with asymmetric MILC open window at the source terminal.

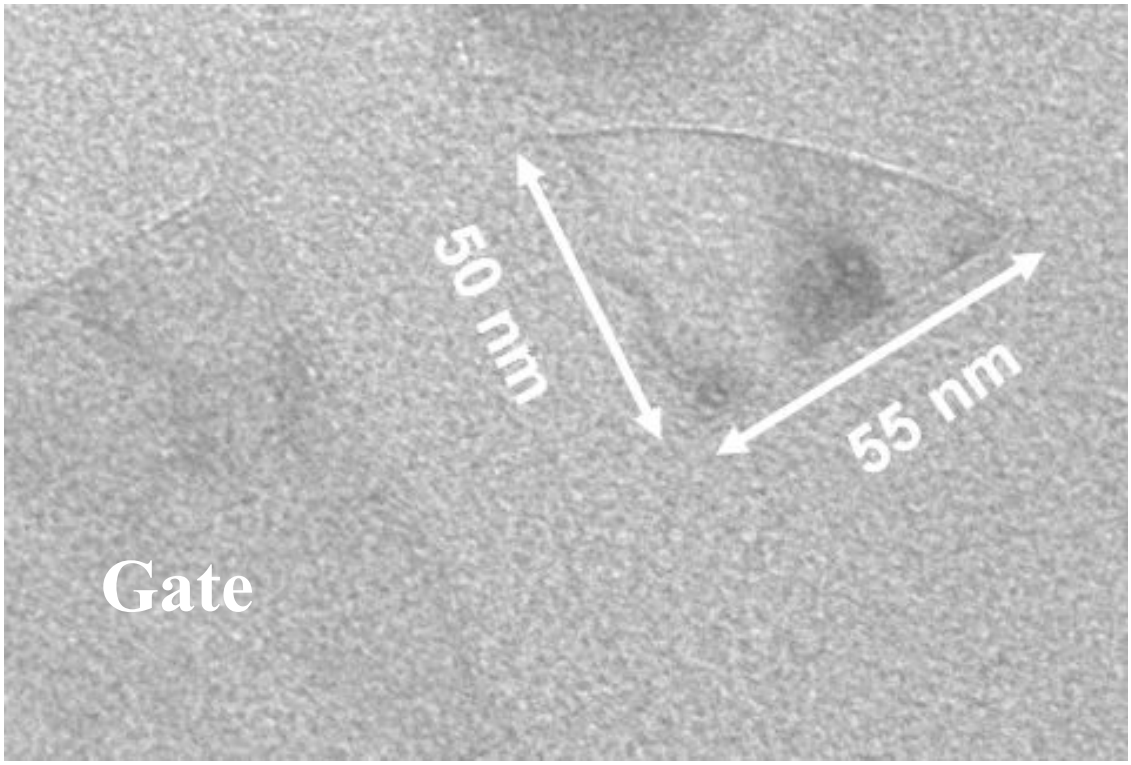
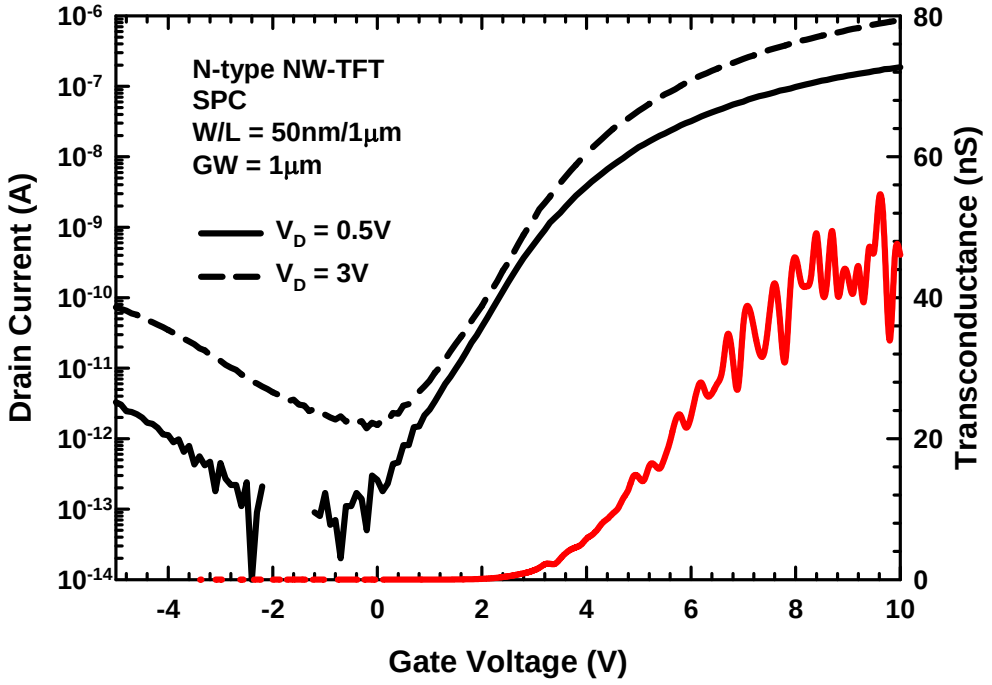
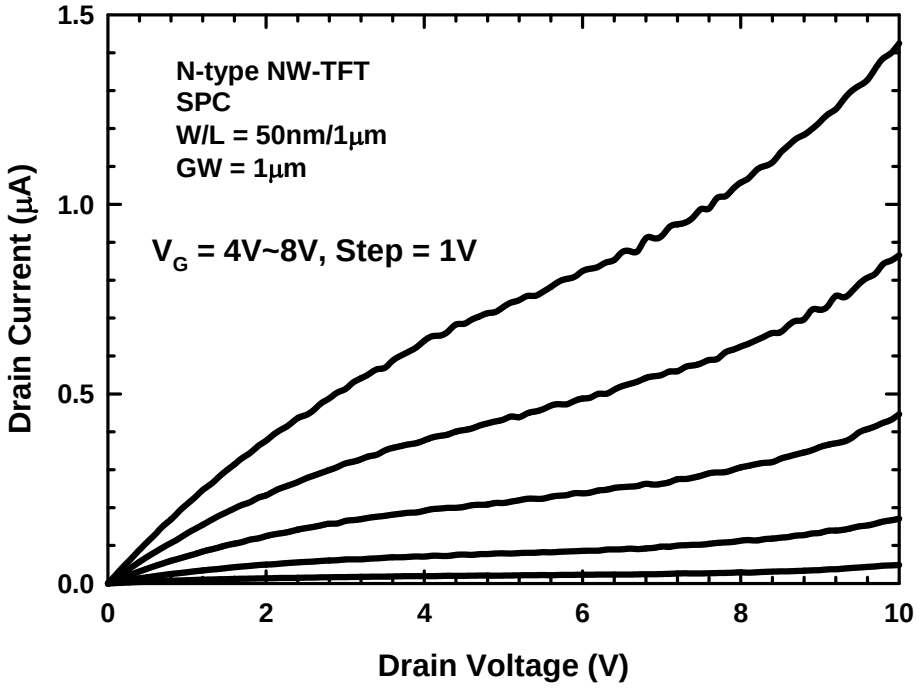


Fig. 2-3　TEM cross-sectional view of NW-TFT.



(a)



(b)

Fig. 3-1 (a) Transfer and (b) output characteristics of SPC NW-TFT.

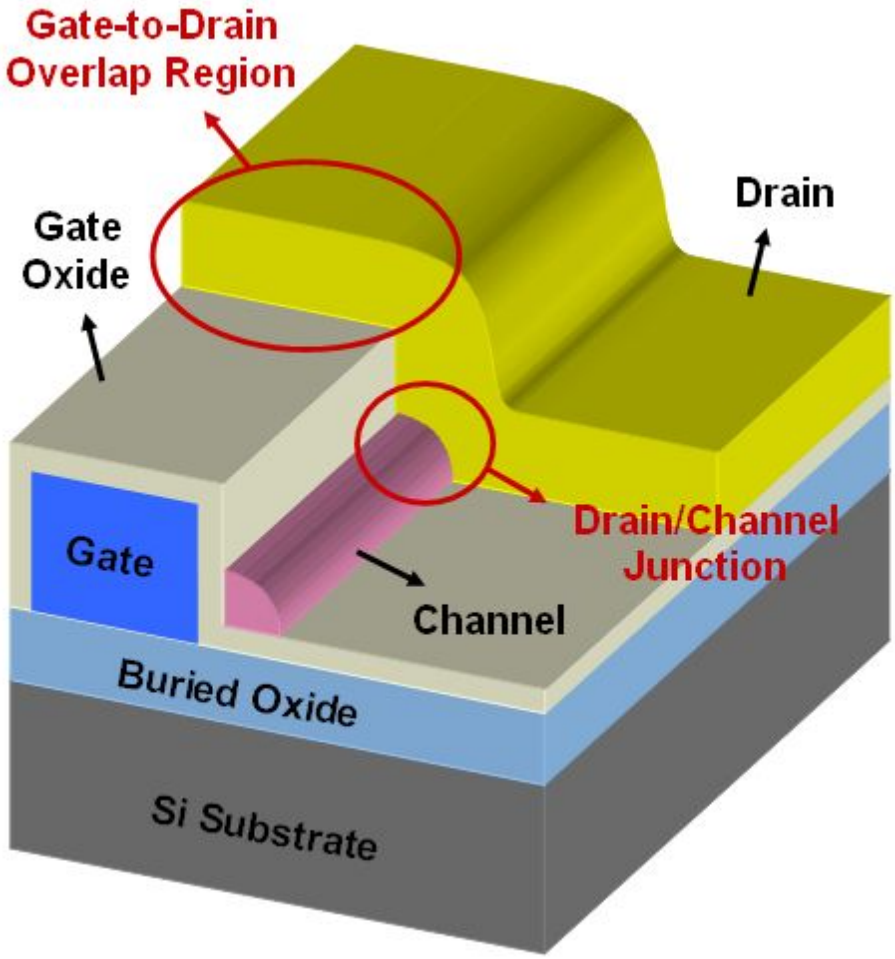


Fig. 3-2 Two possible regions for off-state leakage generation.

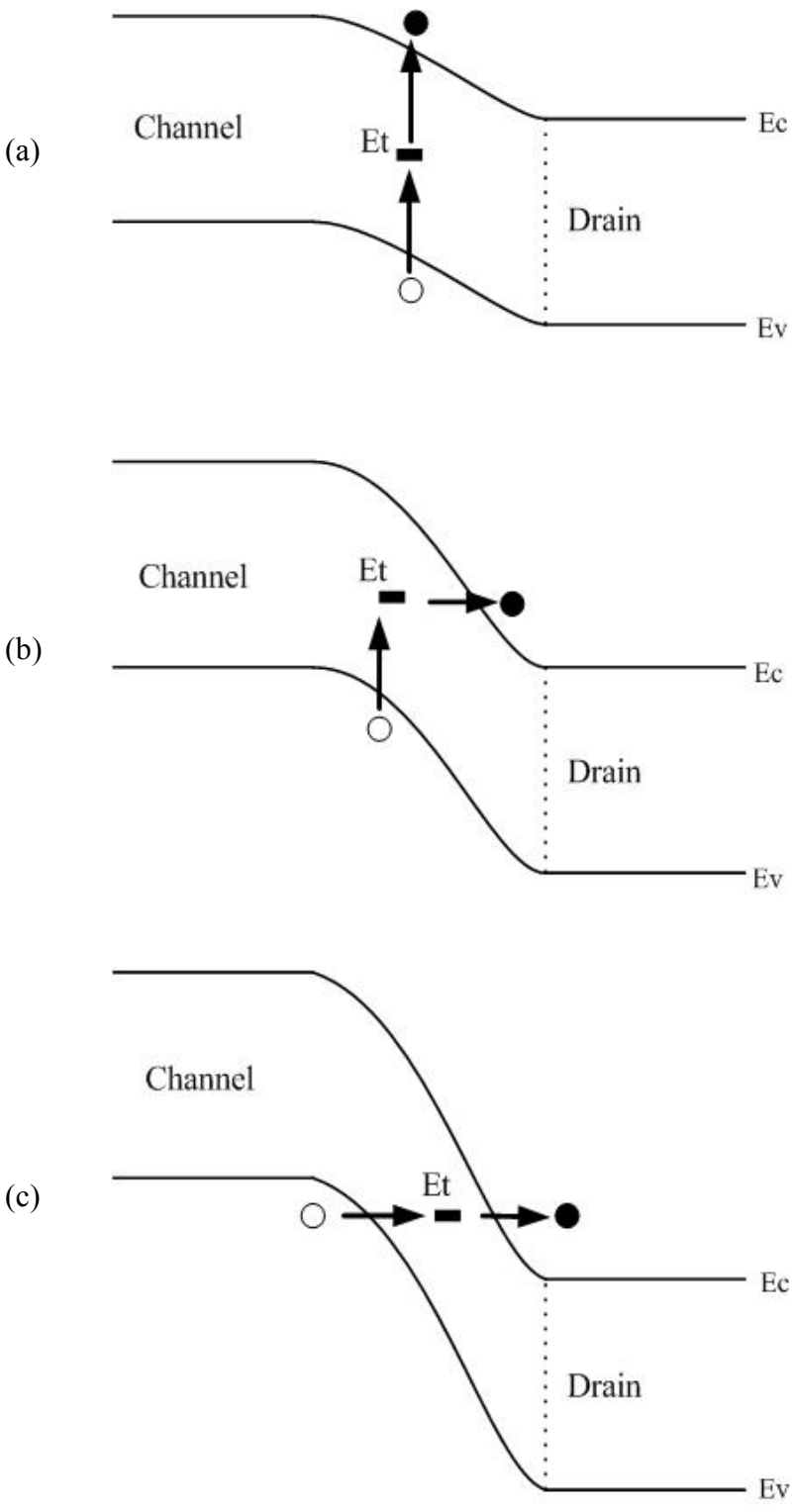


Fig. 3-3 Leakage mechanisms in drain/channel junction. (a) Thermal emission. (b) Thermionic field emission. (c) Band-to-band tunneling.

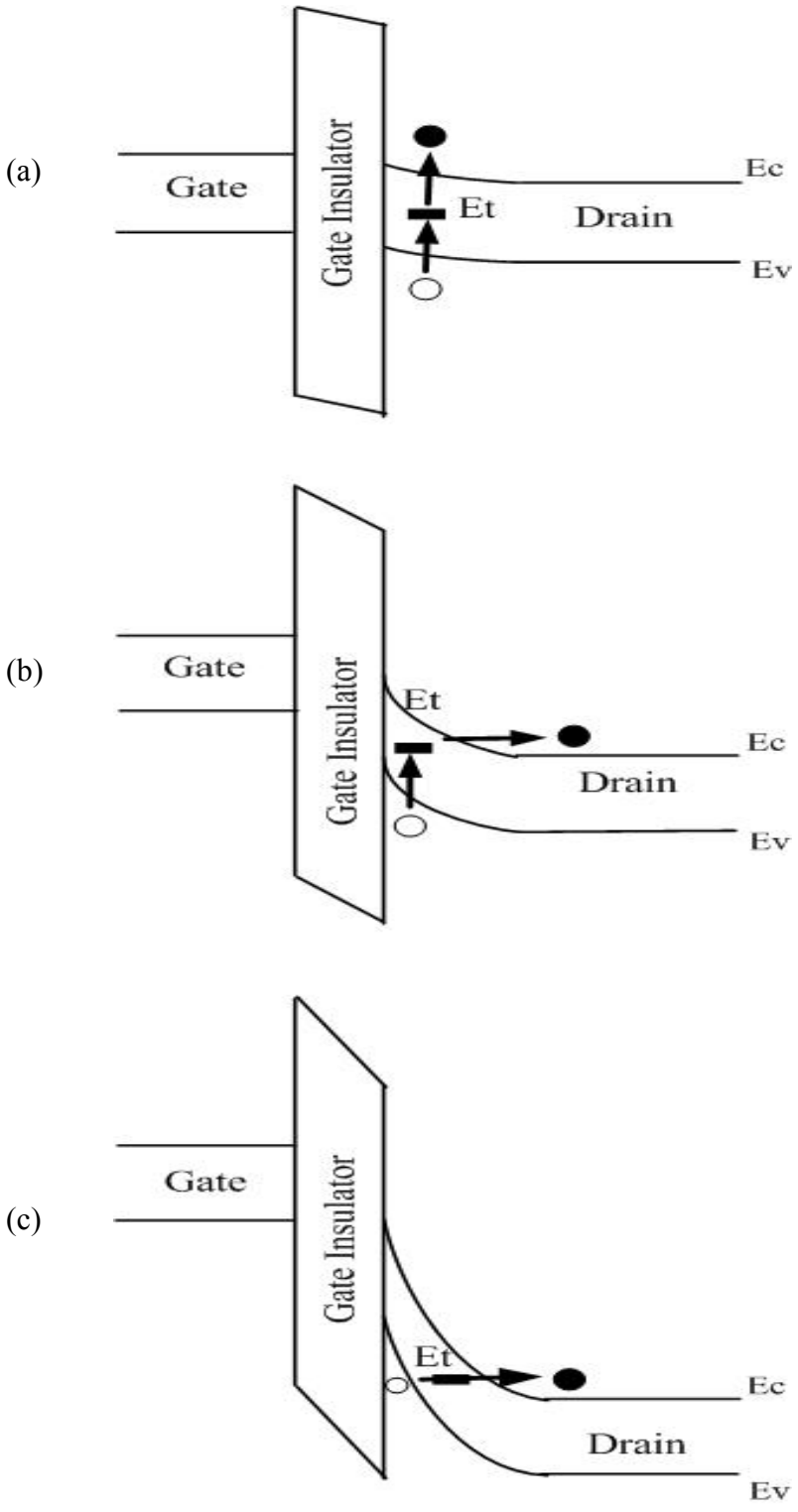
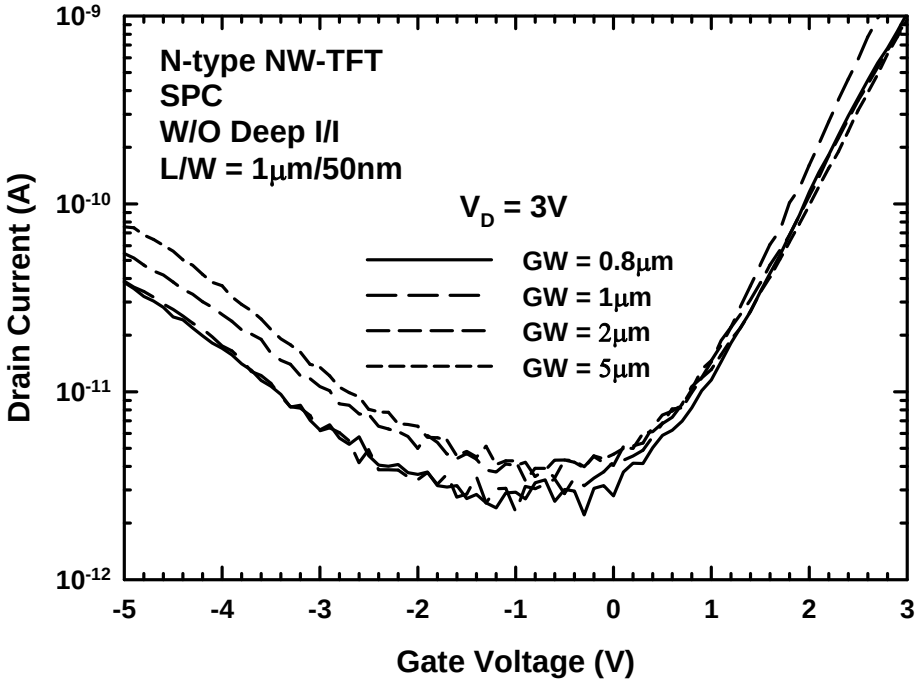
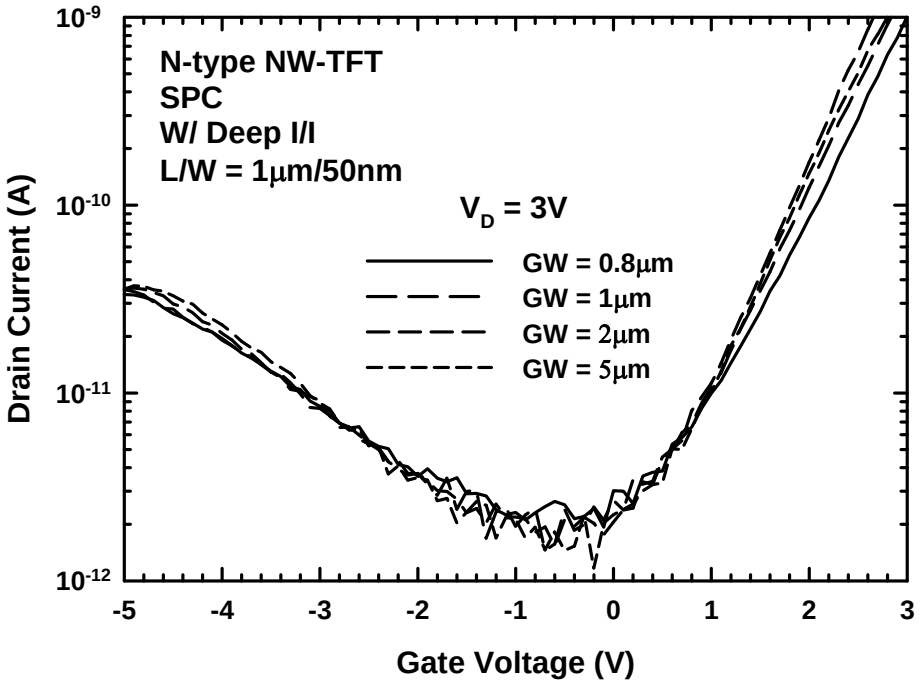


Fig. 3-4 Leakage mechanisms in gate-to-drain overlap region. (a) Thermal emission. (b) Thermionic field emission. (c) Band-to-band tunneling.

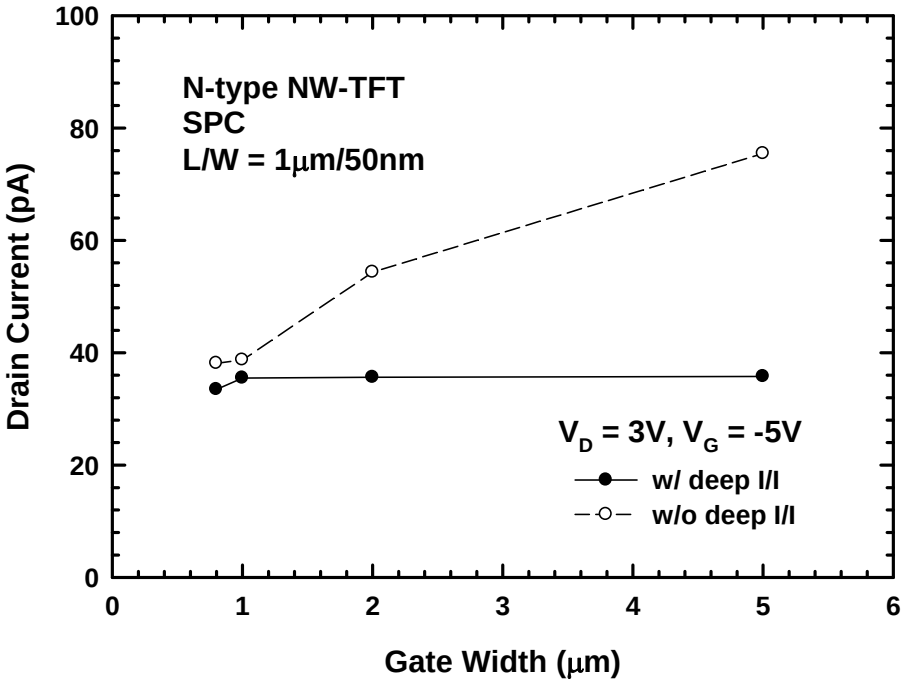


(a)

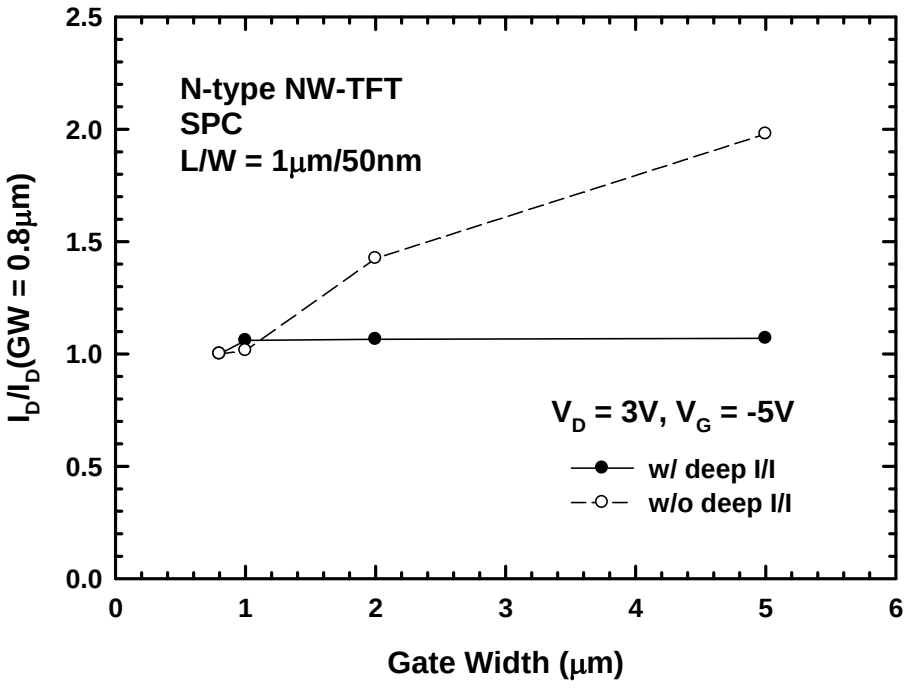


(b)

Fig. 3-5 Off-state characteristics of NW-TFTs (a) w/o and (b) w/ deep I/I having various gate widths.

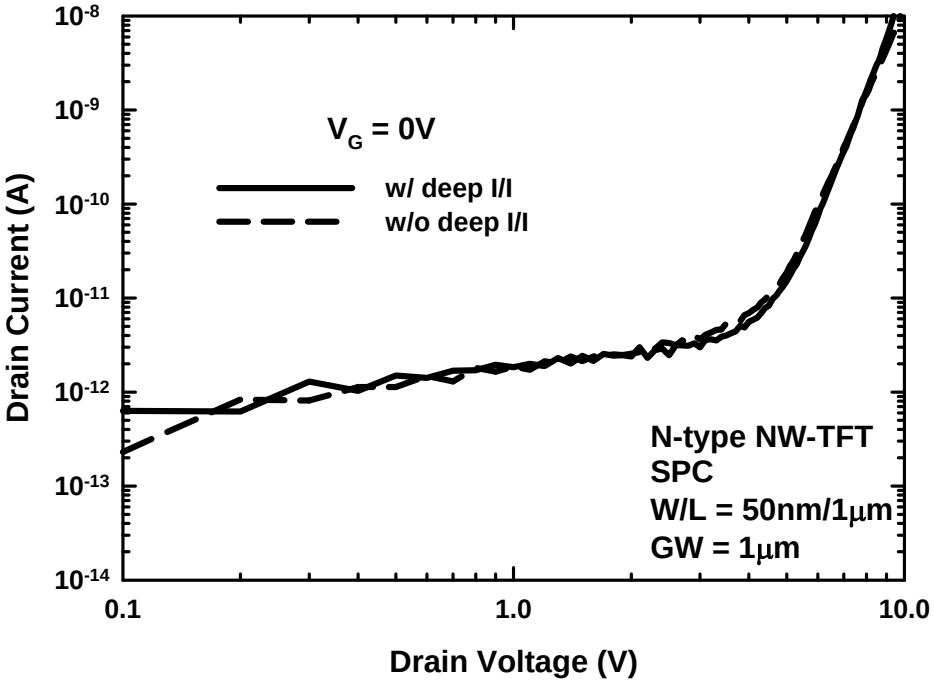


(a)

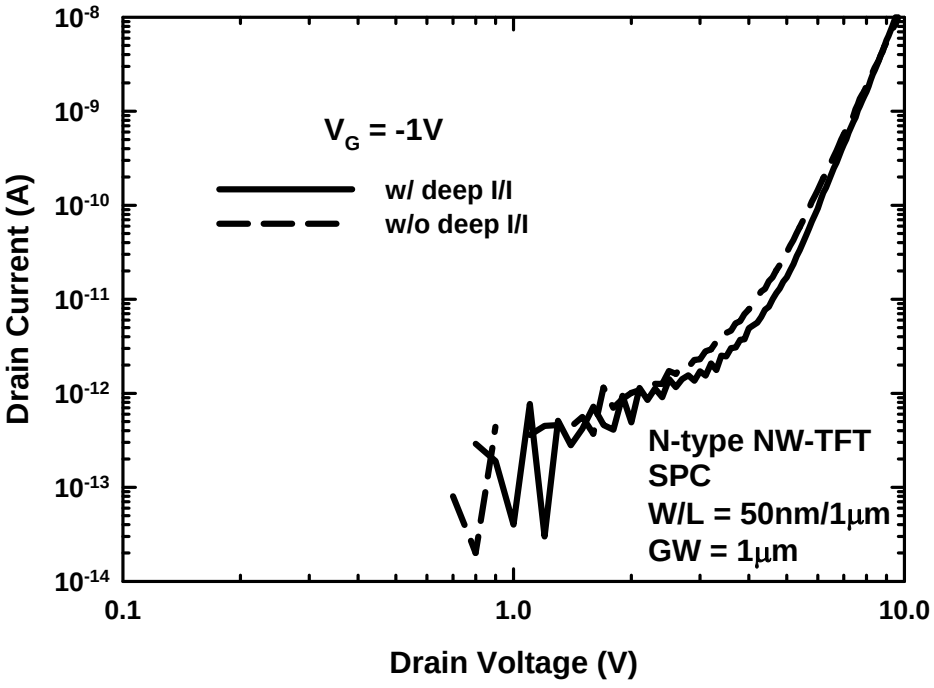


(b)

Fig. 3-6 (a) Comparisons of leakage current of NW-TFTs w/o and w/ deep I/I as a function of gate width at $|V_{GD}|$ = 8V. (b) OSCR of NW-TFTs with different I/I schemes.

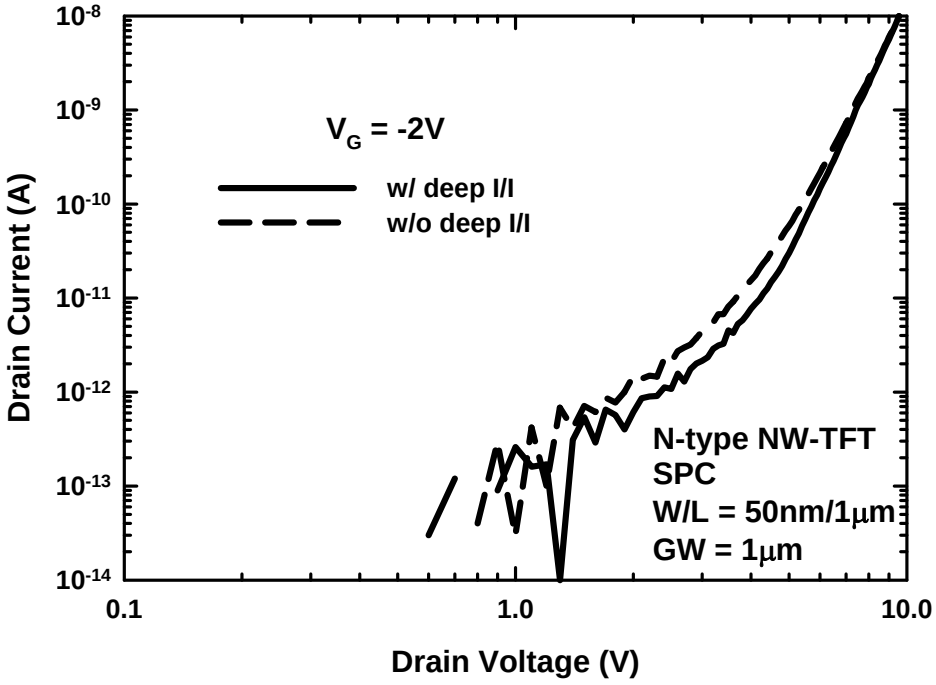


(a)

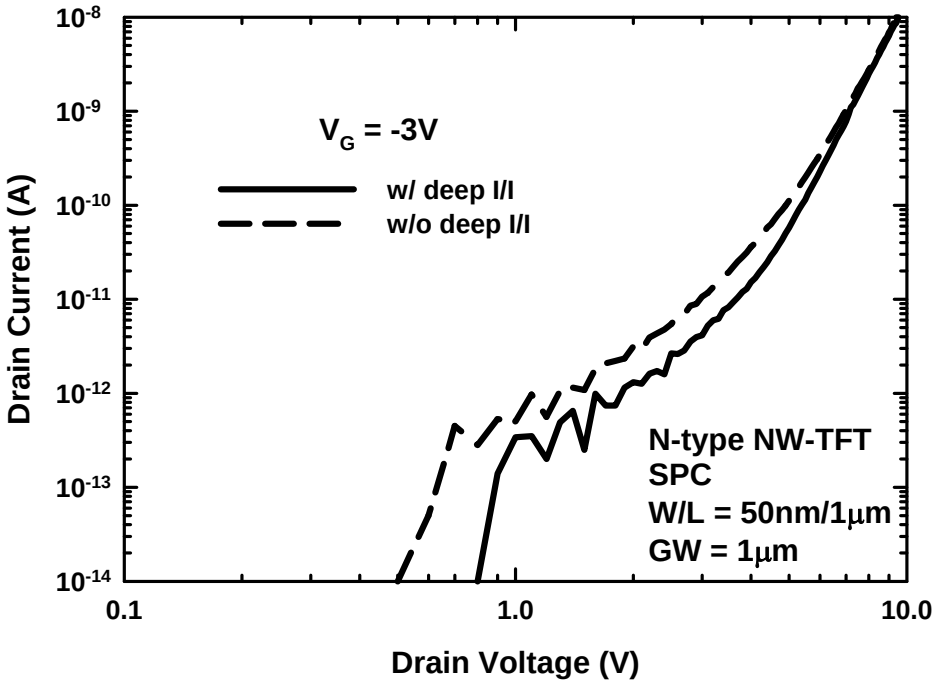


(b)

Fig. 3-7 (a)~(f) show the dependence of leakage currents of NW-TFTs w/o and w/ deep I/I on drain bias at V_G = 0, -1, -2, -3, -4 and -5 V, respectively.

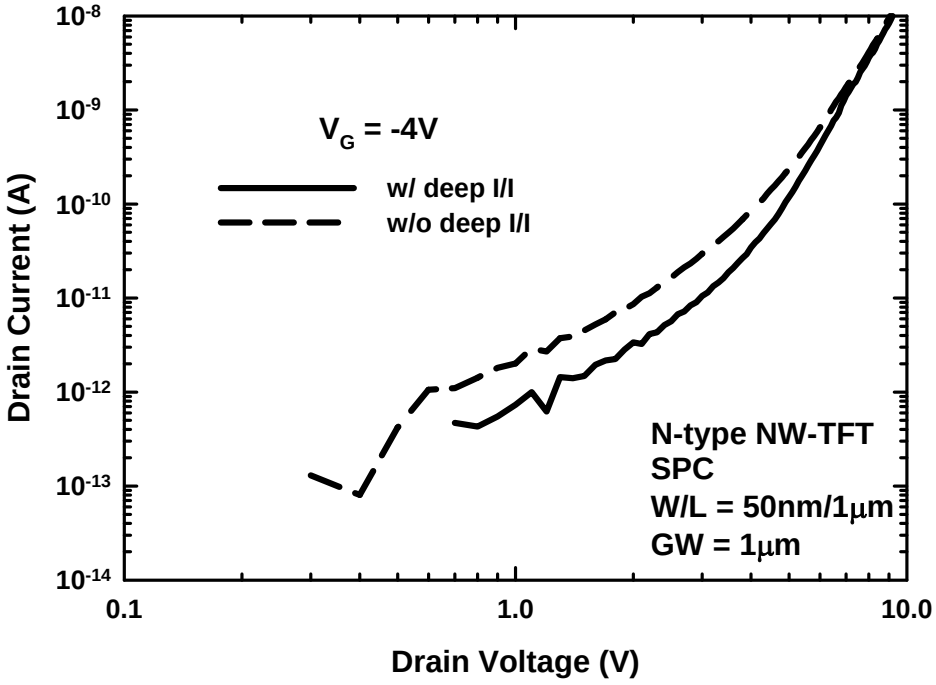


(c)

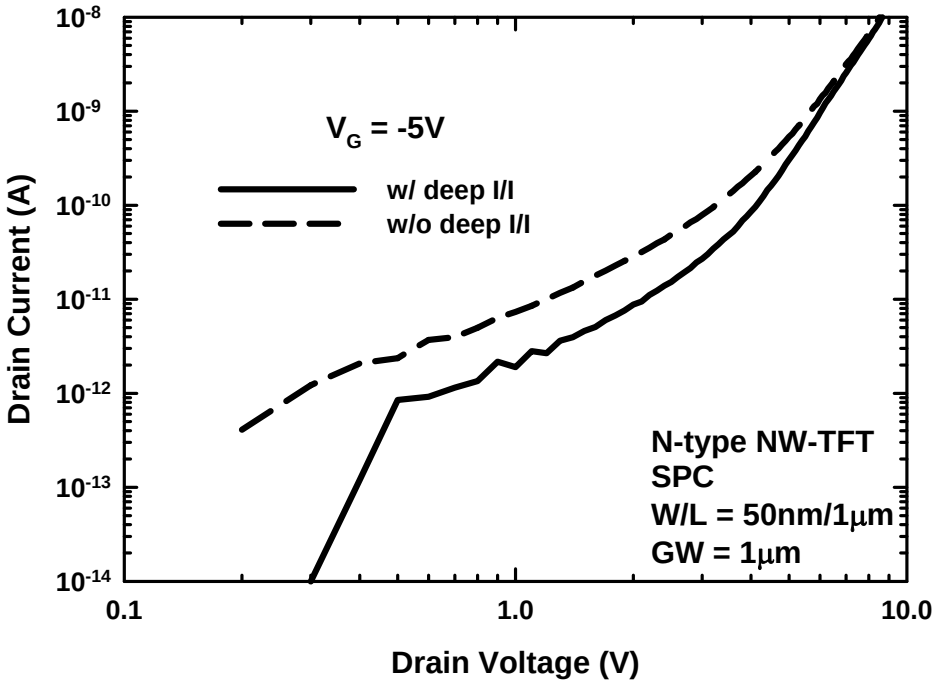


(d)

Fig. 3-7 Continued.

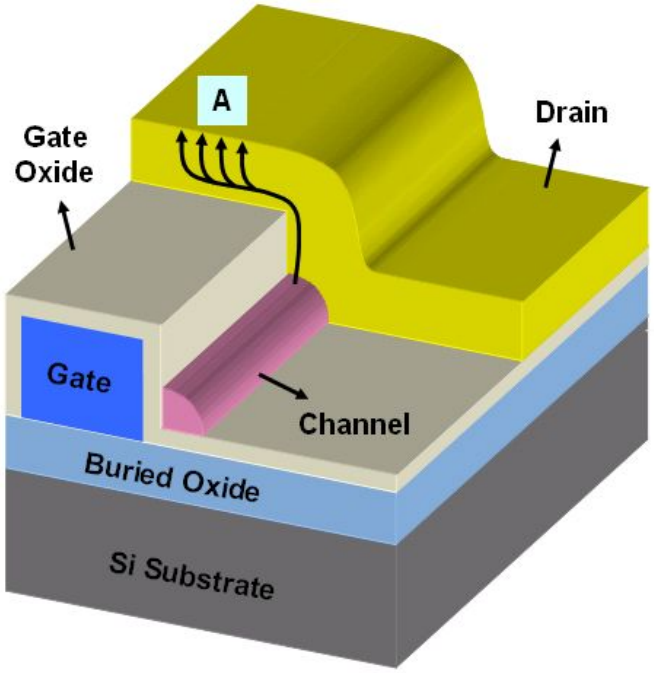


(e)

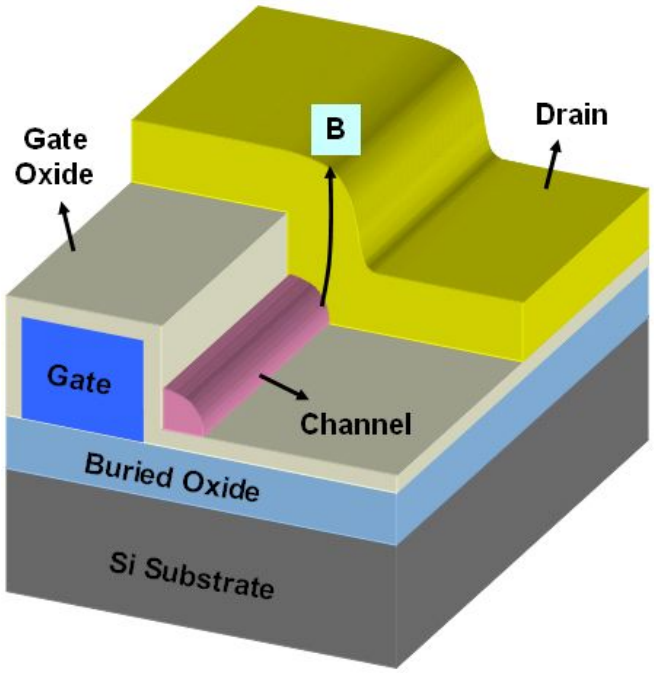


(f)

Fig. 3-7 Continued.

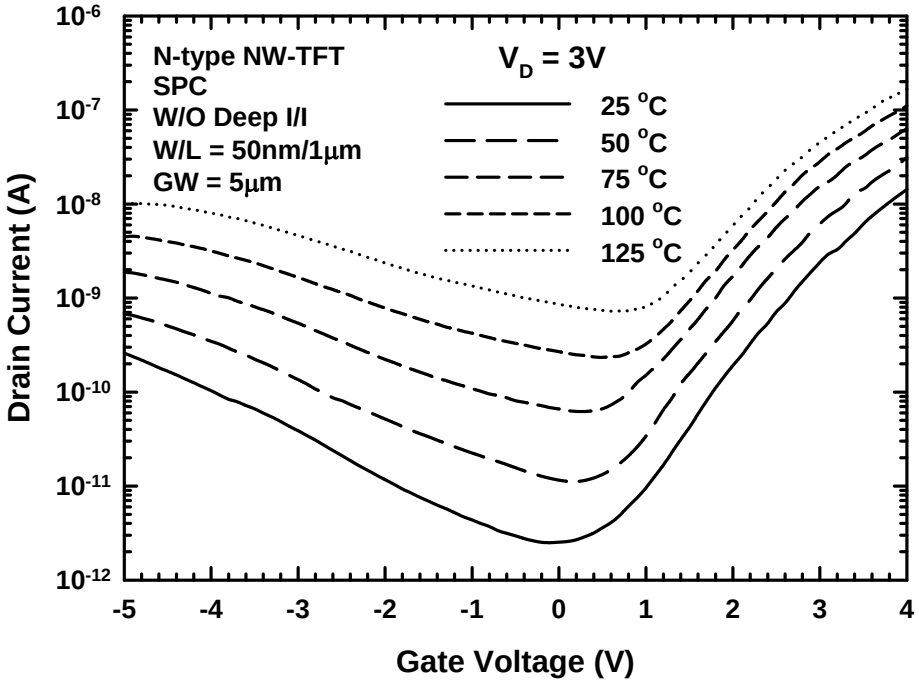


(a)

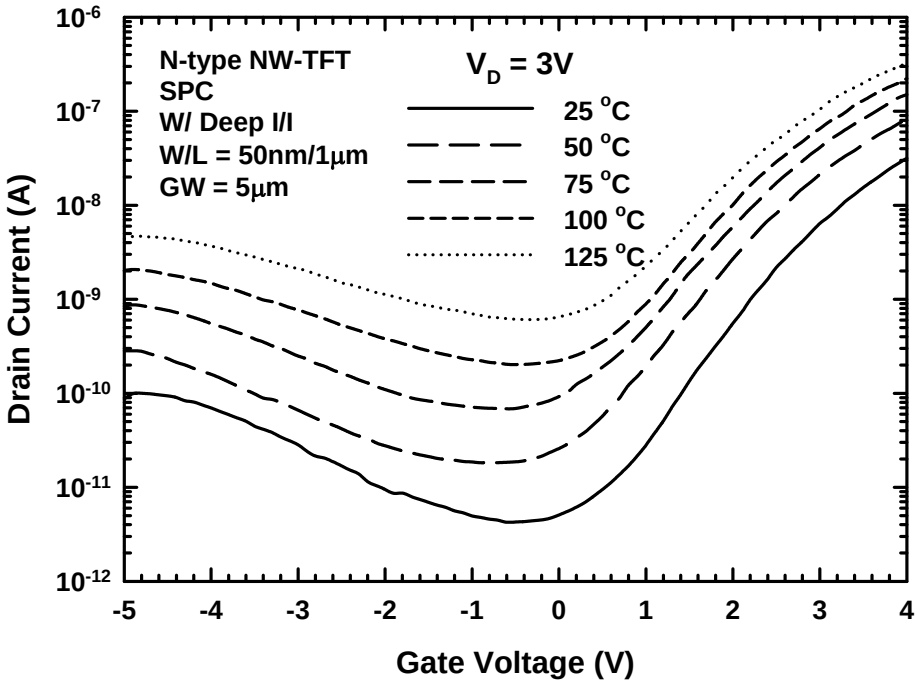


(b)

Fig. 3-8 Major leakage current paths near the drain side of NW-TFTs (a) w/o and (b) w/ deep I/I.

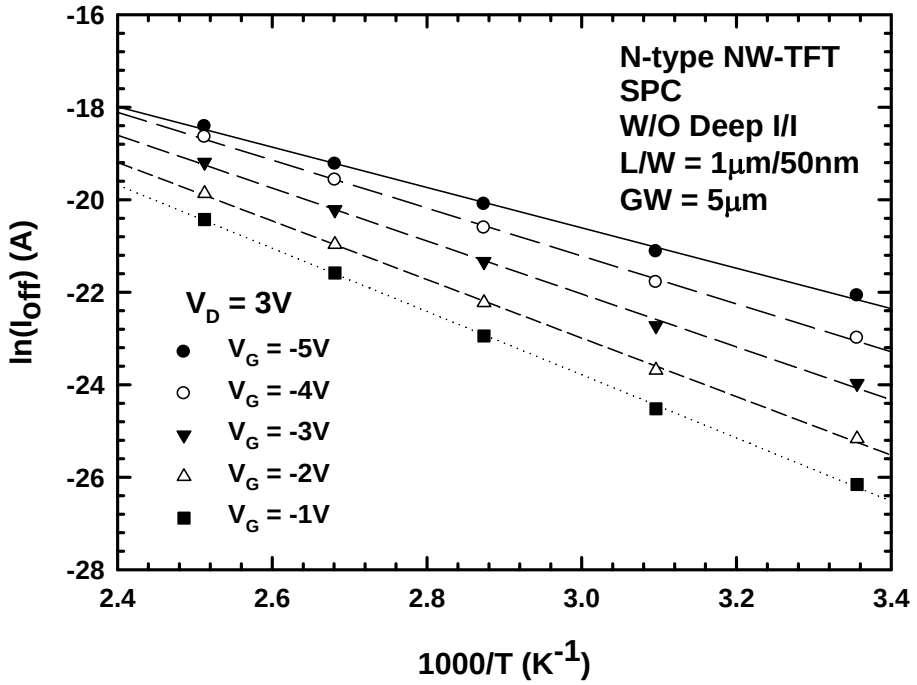


(a)

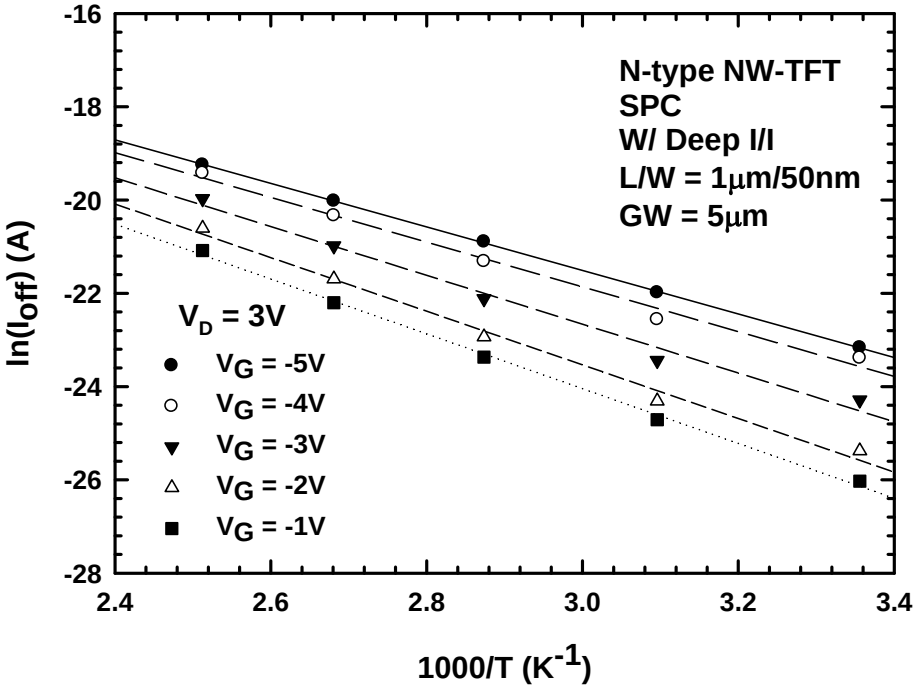


(b)

Fig. 3-9 Off-state transfer characteristics of NW-TFTs (a) w/o and (b) w/ deep I/I at various temperatures.



(a)



(b)

Fig. 3-10 Arrhenius plots of the off-state currents for NW-TFTs (a) w/o and (b) w/ deep I/I at various gate biases.

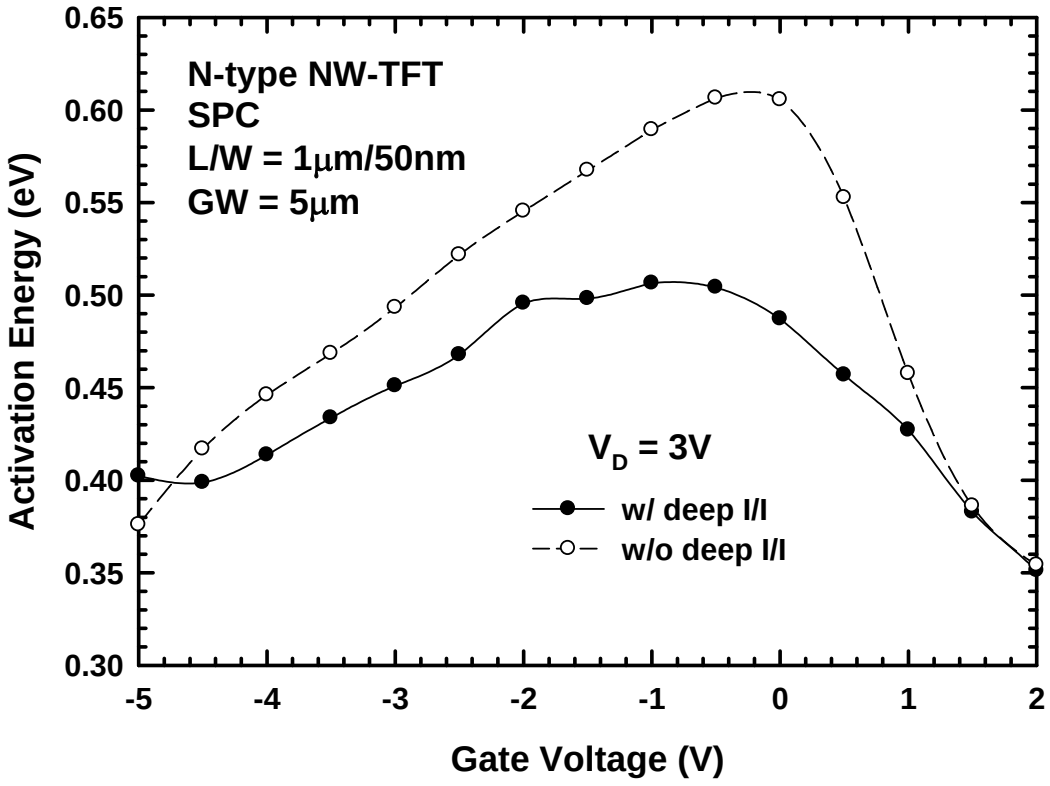


Fig. 3-11 Off-state activation energies of NW-TFTs w/o and w/ deep I/I.

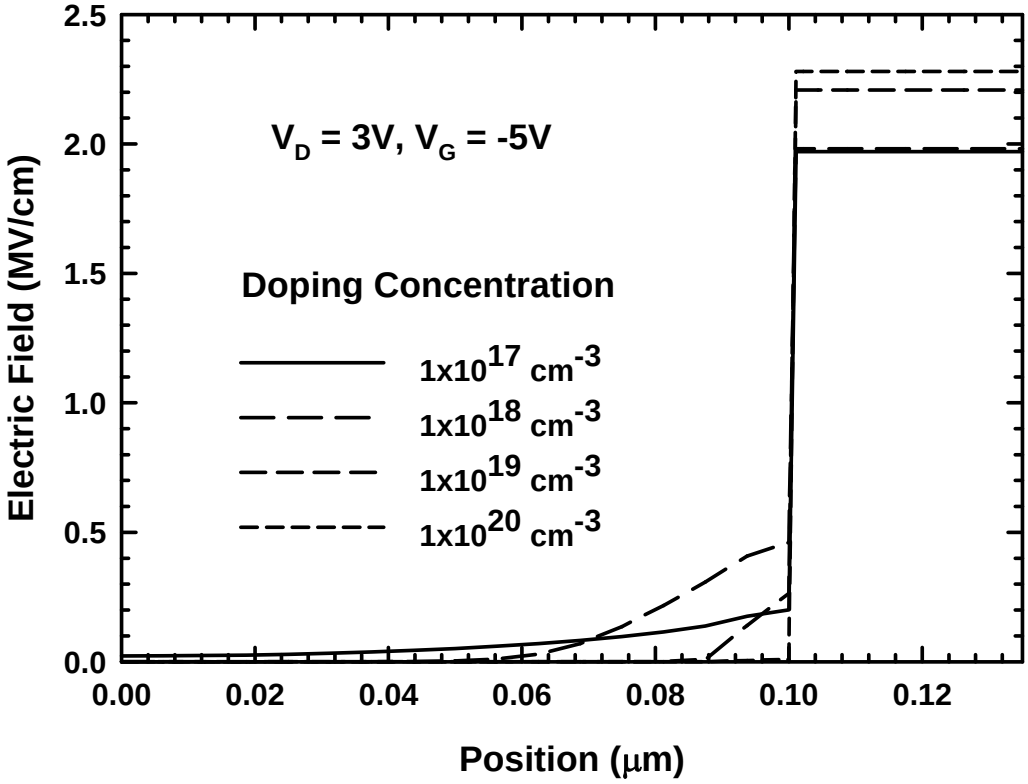


Fig. 3-12 The dependence of the electric field distribution in the drain and gate oxide on the dopant concentration in the drain terminal.

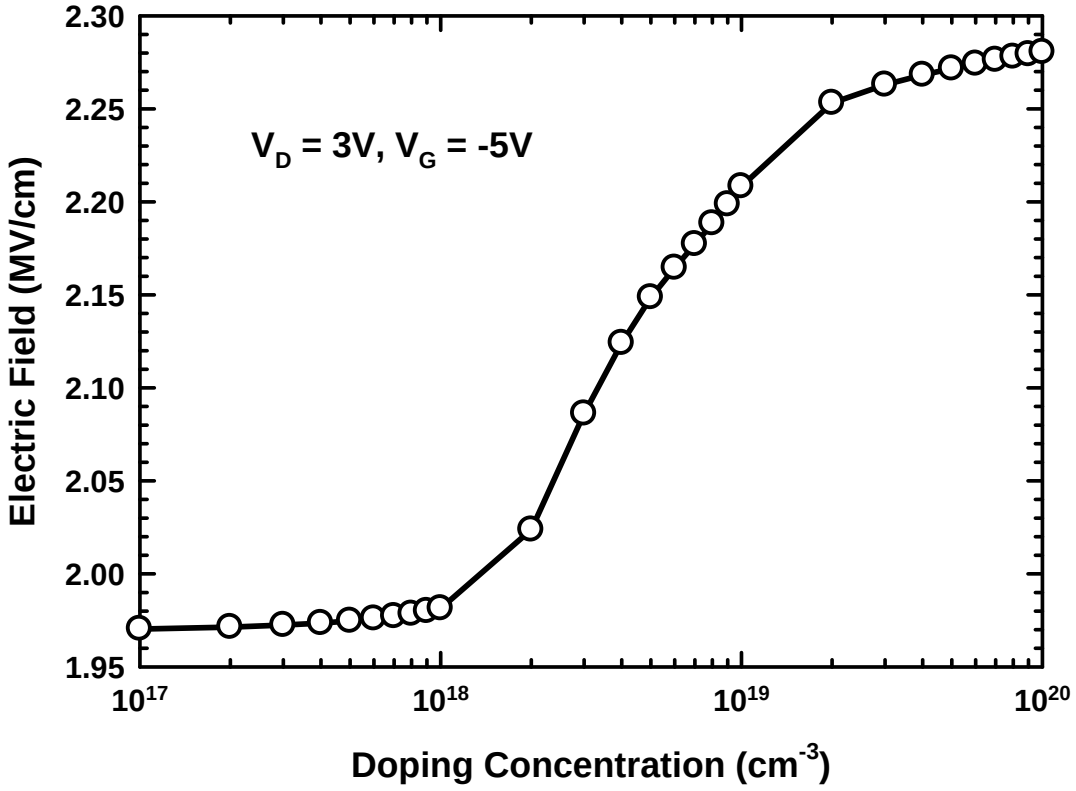


Fig. 3-13 The transformation of the electric field strength in the gate oxide as a function of the dopant concentration in the drain terminal.

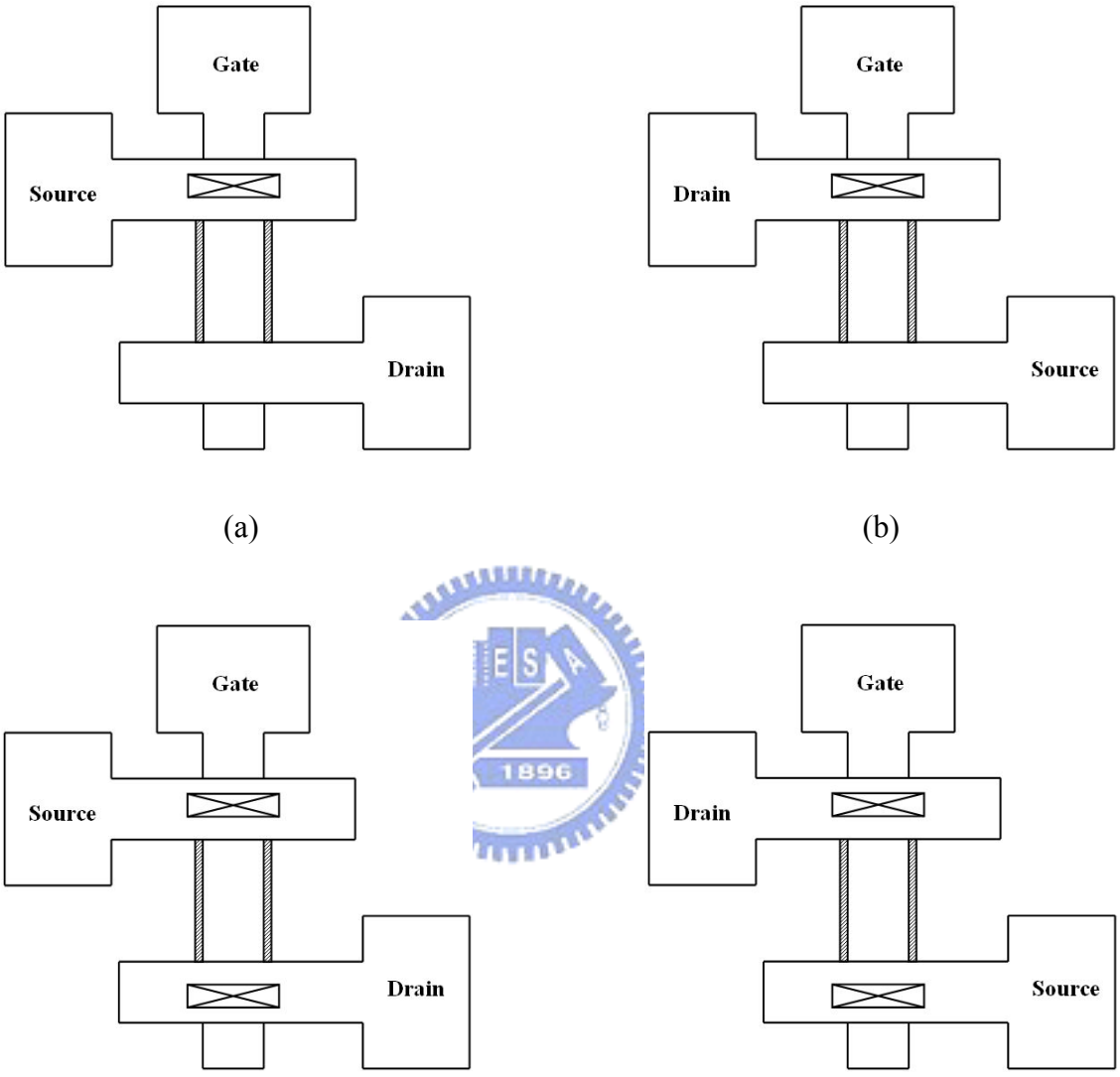
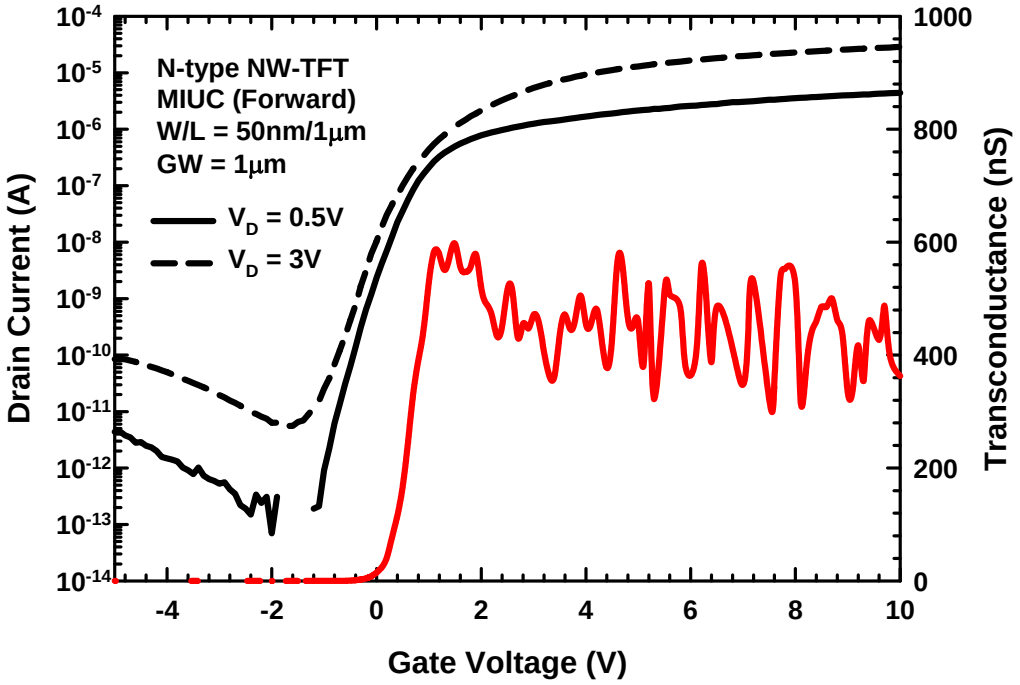
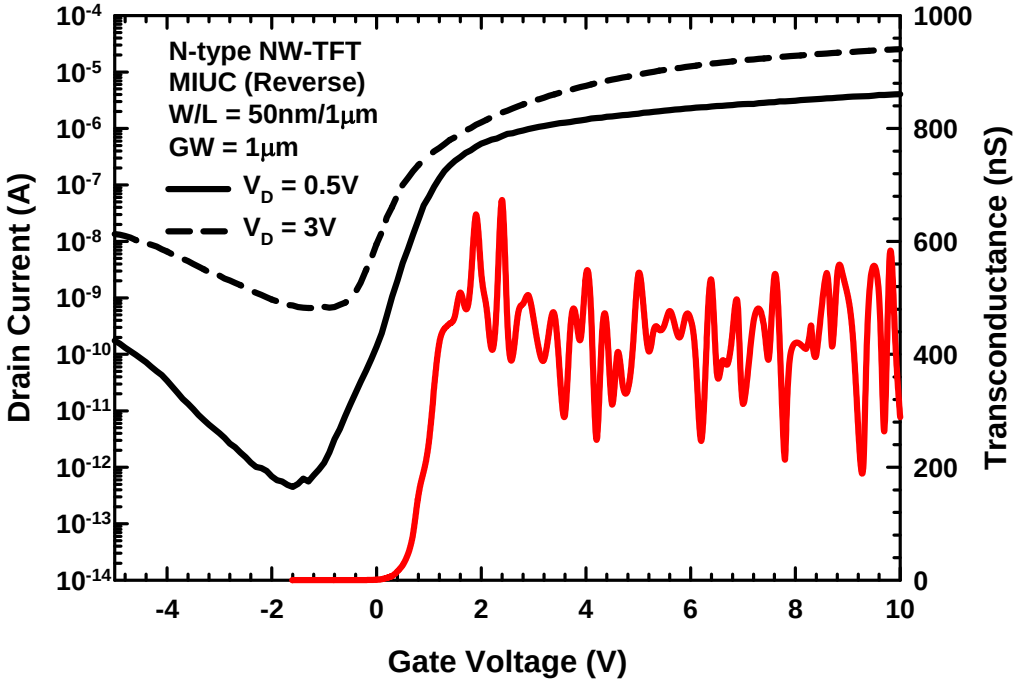


Fig. 4-1 Configurations of MILC open window. (a) MIUC (Forward). (b) MIUC (Reverse). (c) MIBC (Forward). (d) MIBC (Reverse).



(a)



(b)

Fig. 4-2 Transfer characteristics of (a) MIUC (Forward) and (b) MIUC (Reverse) NW-TFT.

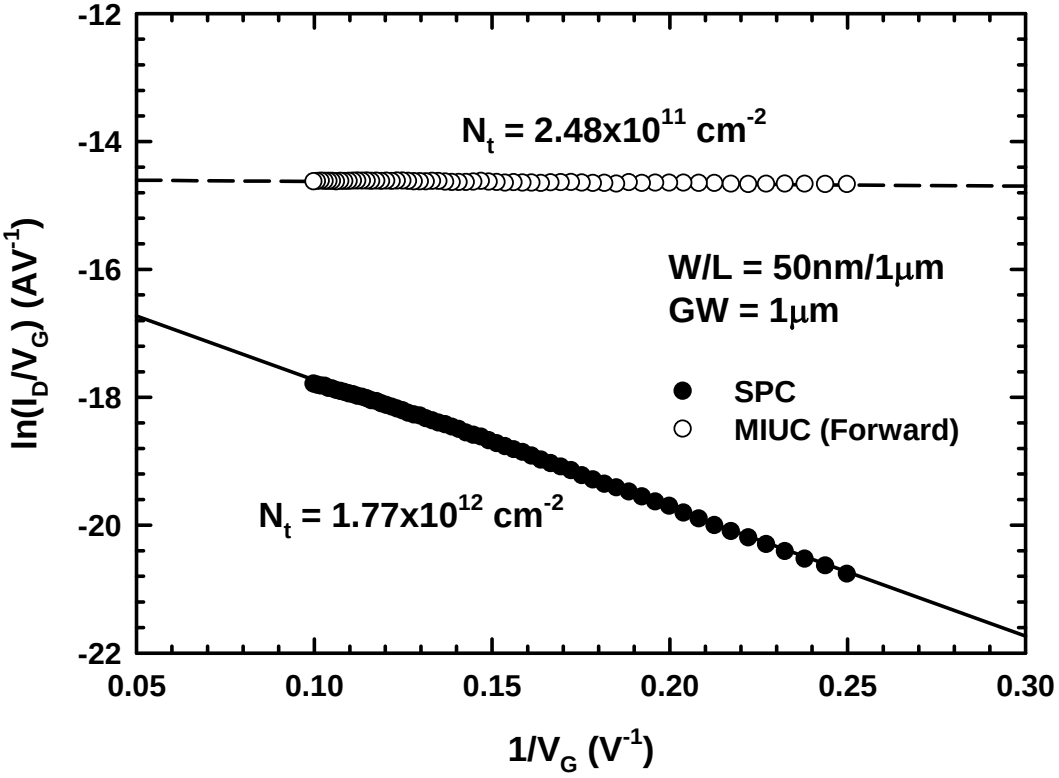


Fig. 4-3 Plot of $\ln(I_D/V_G)$ versus $(1/V_G)$ for SPC and MIUC (Forward) NW-TFTs.

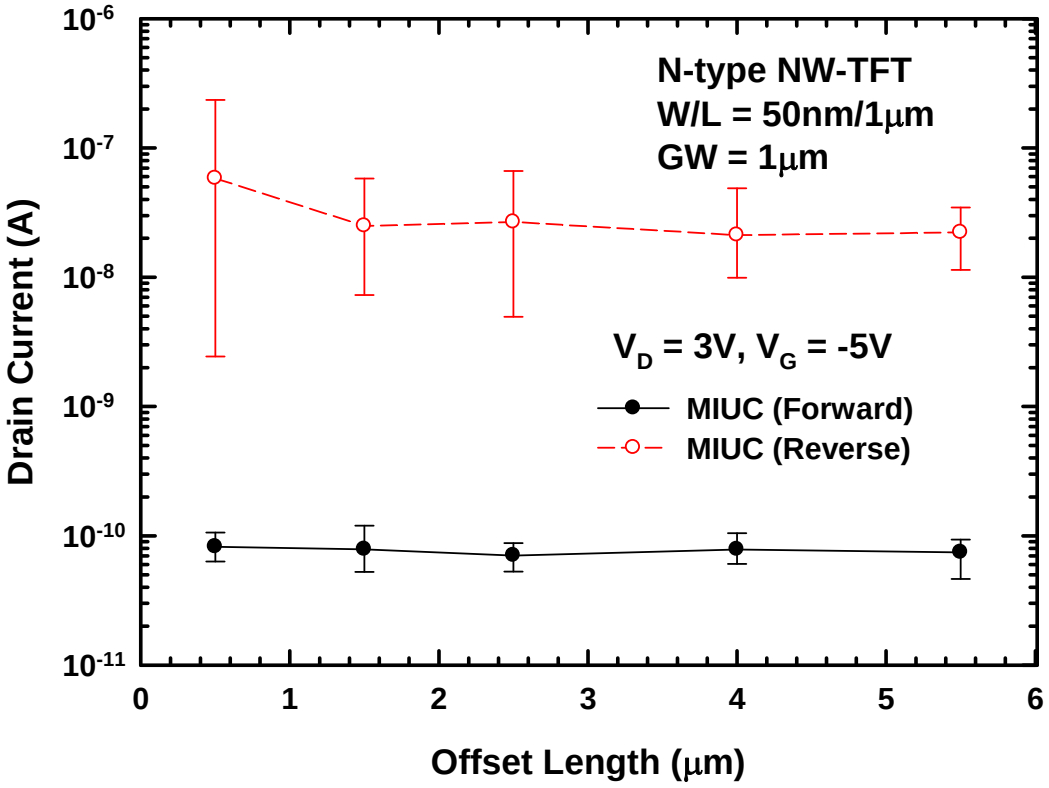


Fig. 4-4 Off-state leakage current as a function of the offset length for devices fabricated by MIUC (Forward) and MIUC (Reverse). The number of devices characterized for each condition is 20.

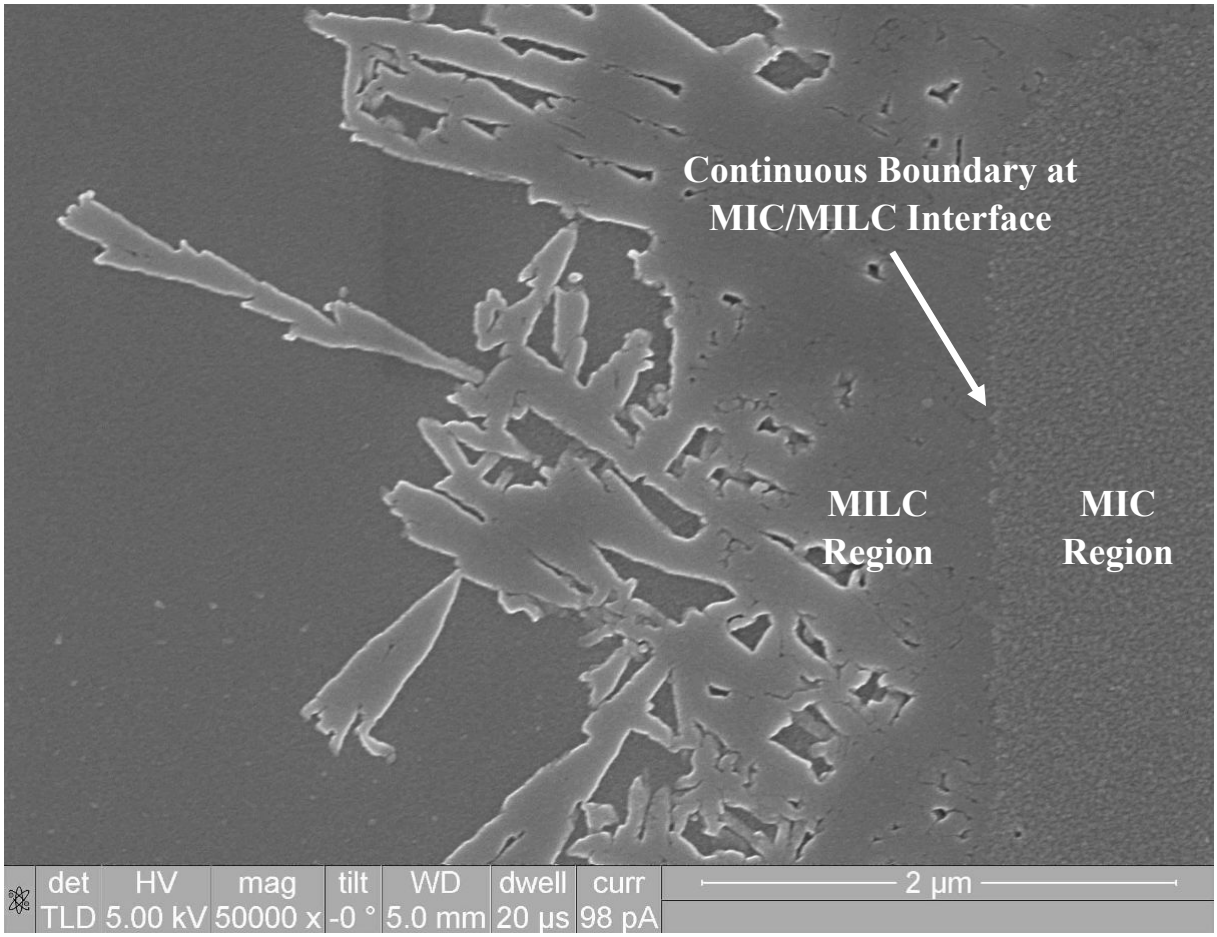


Fig. 4-5 SEM image showing the continuous boundary at MIC/MILC interface.

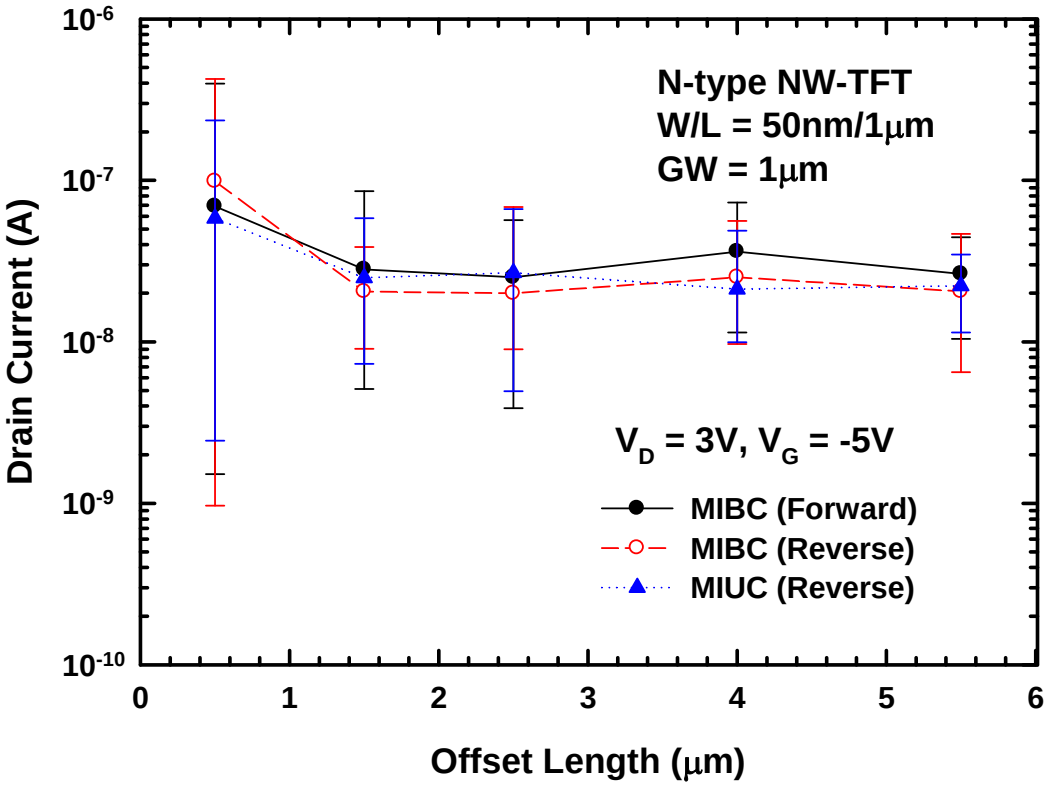


Fig. 4-6 The comparison of the off-state leakage currents for devices fabricated by MIBC (Forward), MIBC (Reverse) and MIUC (Reverse) with different offset lengths. The number of devices characterized for each condition is 20.

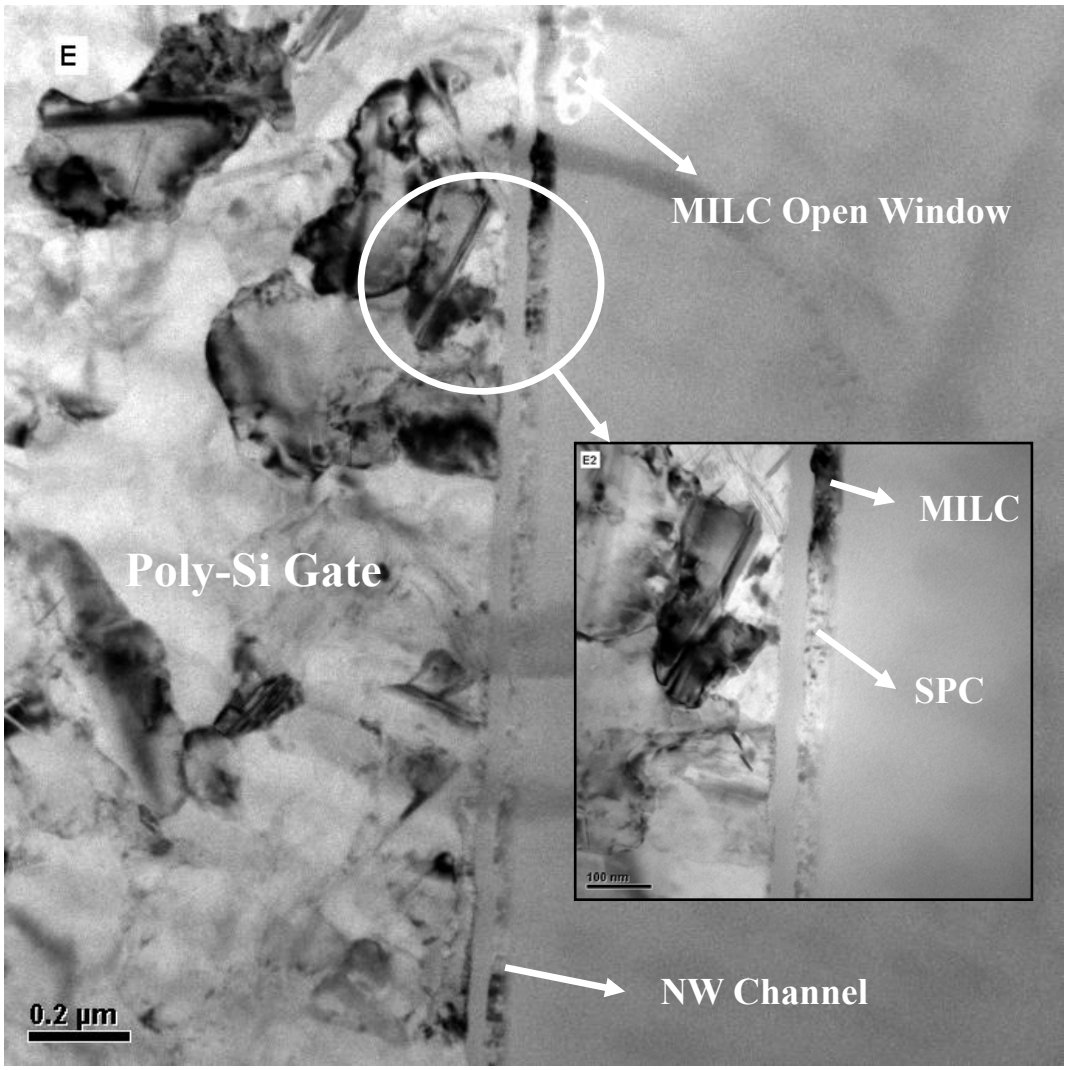


Fig. 4-7 The TEM image showing the crystallinity of the NW channel. The inserting figure shows the SPC occurrence in the MILC front.

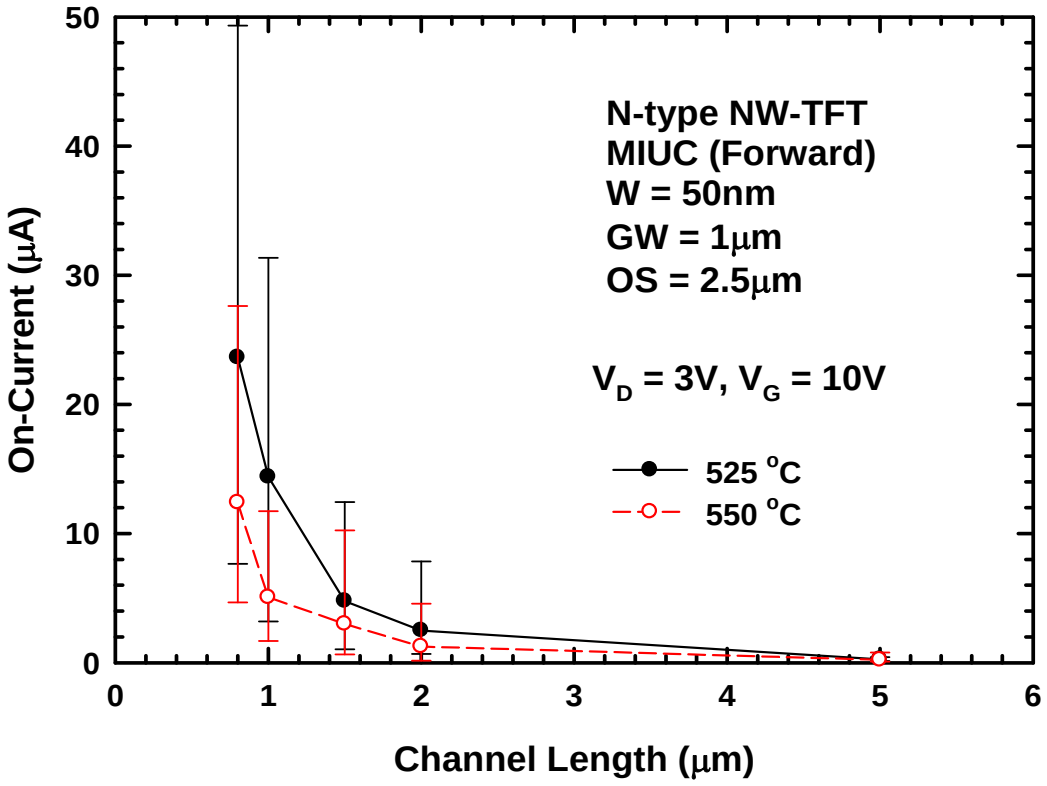


Fig. 4-8 On-current as a function of the channel length for devices annealed at 525 and 550 ℃. The number of devices characterized for each condition is 20.

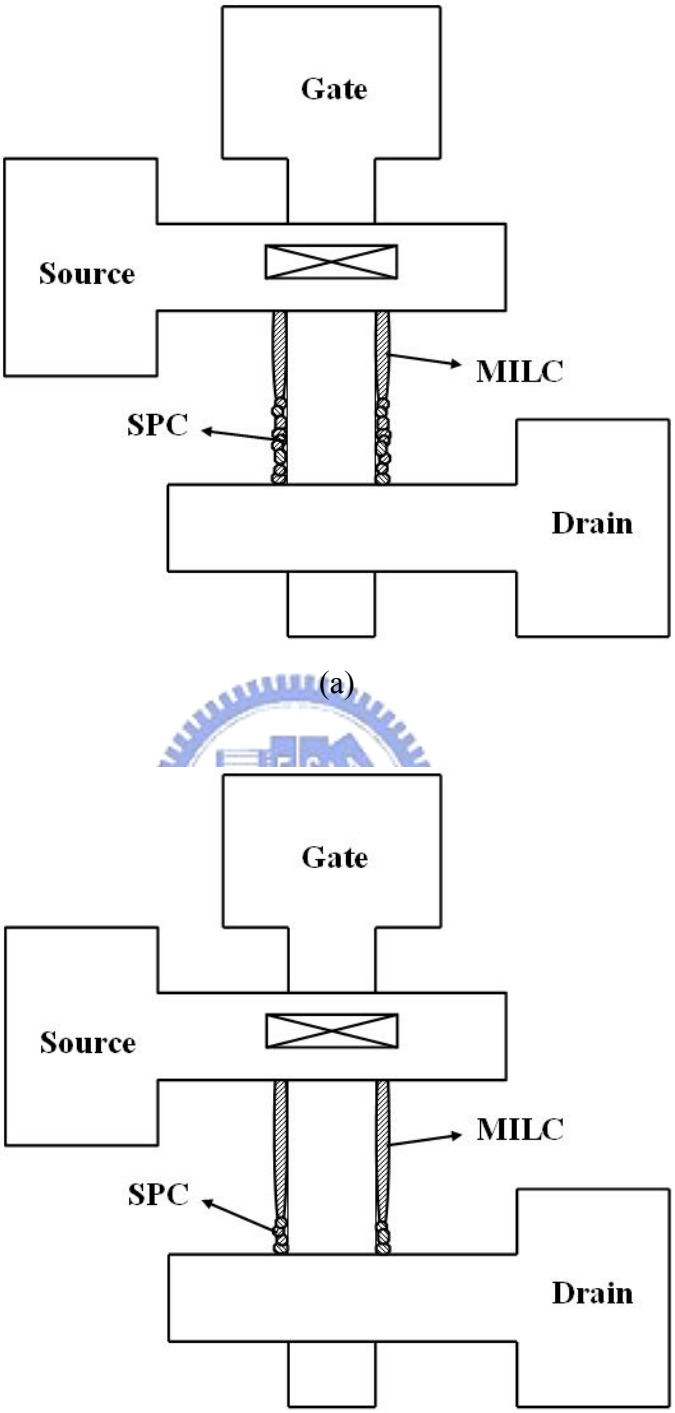


Fig. 4-9 Illustrations show the crystallinity of the NW channel at (a) 550 and (b) 525 ℃.

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論文題目：

利用低溫多晶矽技術於製造具有多晶矽奈米線通道的薄膜電晶體之研究

A Study of Thin-Film Transistors with Poly-Si Nanowire Channels Fabricated by LTPS Technology

著作：

Y. F. Huang, C. J. Su, M. H. Lee, H. H. Tsai, H. C. Lin and T. Y. Huang, "Suppression of off-state leakage in a novel poly-Si nanowire thin-film transistor," *IEEE Silicon Nanoelectronics Workshop*, pp. 49-50, 2007.