國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

利用特殊接觸電極研究橫向擴散元件之自發熱效應與可靠度

Investigation of Self-Heating and Reliability Issues in Lateral DMOS by Using an Additional Metal Contact Structure

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中華民國 九十六 年 六 月

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中華民國 九十六 年 六 月

利用特殊接觸電極研究橫向擴散元件之自發熱效應與可靠度

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摘要

隨著半導體業的發展，高功率金氧半場效電晶體被廣泛的應用在電力電子元件上，LDMOS(橫向兩次擴散之金氧半場效電晶體)通常在高壓積體電路中做驅動元件、電力切換元件、射頻功率電晶體。在本論文中，主要是利用特殊接觸電極來對 LDMOS 做可靠度分析。

在此論文中，主要討論在不同的熱載子加壓後，LDMOS 的電性退化程度，我們提出一個三區域的電荷幫浦實驗(three-region charge pumping technique)來觀察不同的區域有何不同的損害產生。同時利用特殊的金屬電極來研究 LDMOS 的低頻雜訊(Flicker Noise)，可以了解到不同的閘極電壓下所量到的低頻雜訊分別代表不同的區域，最後利用二維方向的模擬來解釋實驗上的結果。在實驗上發現，在最大閘極漏電流的加壓條件下，由於在 LDMOS 的通道部分有介面缺陷及在鳥嘴區有氧化層電荷的產生，所以造成最嚴重的集極電流退化以及低頻雜訊的增加，同時利用電荷幫浦實驗，可萃取介面缺陷以及氧化層電荷產生的速率。

接著，我們利用特殊的金屬接觸電極以及快速的暫態電路來研究 LDMOS 的自發熱效應(self-heating effect)。自發熱效應與瞬間熱載子加壓後的元件退化關係

亦在此論文中研究。研究發現，交流的加壓條件由於 LDMOS 沒有自發熱效應，所以會比直流的加壓條件有較嚴重的熱載子退化。交流加壓的頻率與退化程度同時也在此論文中研究。

Investigation of Self-Heating and Reliability Issues in Lateral DMOS by Using an Additional Metal Contact Structure

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Abstract.

Lateral Double-Diffused MOS (LDMOS) have been widely utilized in power electronics, for example, LCD drivers, power switch, and ratio frequency power transistor in high voltage integrated circuits. In this study, we will characterize the self-heating and hot carrier reliability issues in LDMOS by using an additional metal contact structure.

Degradation of electrical characteristics in LDMOS transistors in various hot carrier stress modes is investigated. A novel three-region charge pumping technique is proposed to characterize interface trap (N_{it}) and bulk oxide charge (Q_{ox}) creation in the LDMOS. A special metal contact structure is fabricated to identify the flicker noise in MOS and LDMOS. The correlation of flicker noise degradation and stress induced oxide damage region will be analyzed. A two-dimensional numerical device

simulation is performed to explain the measurement result. Our characterization shows that max. I_g stress causes largest drain current degradation and flicker noise degradation because of both interface trap generation in the channel and bulk oxide charge creation in the bird's beak region. The growth rates of N_{it} and Q_{ox} are extracted from the proposed charge pumping method.

Self-heating effect (SHE) in LDMOS is also investigated by using the special metal contact structure and a fast transient circuit. Transient hot carrier degradation in LDMOS is also investigated. Our characterization shows that drain current degradation in AC stress is more serious than in DC stress because of the elimination of self-heating effect. The stress-frequency dependence of device degradation mode due to self-heating effect will be analyzed.

Acknowledgement

本篇論文之所以能夠完成，乃是無數人合力研究與幫忙互助的結果。

首先，我要感謝我的指導教授－汪大暉老師，能夠提供一個設備完善的實驗資源，並細心與耐心的指導，讓我們得以在這浩瀚無涯的學術之海，一窺其神秘之處。另外，博士班學長－志昌學長、煥淇學長、俊榮學長，也都能在最適當的時間，給予我幫助與開導，尤其是志昌學長，兩年來的無私的指導，使我在實驗上能夠很容易就上手，並且學習到新的知識與觀念。已經畢業的 93 級學長姐－冠潔、強哥和至宸，則是帶領我進入實驗室，和教導我量測技術和實驗原理的大功臣。

在這兩年的時間裡，因為有同學－小鴨、阿雄、Adorken、馬克吳的陪伴，使得兩年的研究生活充滿著愉悅的氣氛。以及 95 學弟妹－元鵬、彥君、子華、佑亮、勖廷、柏凱的陪伴，這些都是不可磨滅的美好回憶。

最後，我要感謝我的父母以及女友依珊，在我漫長的求學期間給予我鼓勵與支持。讓我能沒有後顧之憂的情況下讀書，並完成碩士學位。

謝謝！

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Contents

Figure & Table Captions

observed in both channel region and drift region.

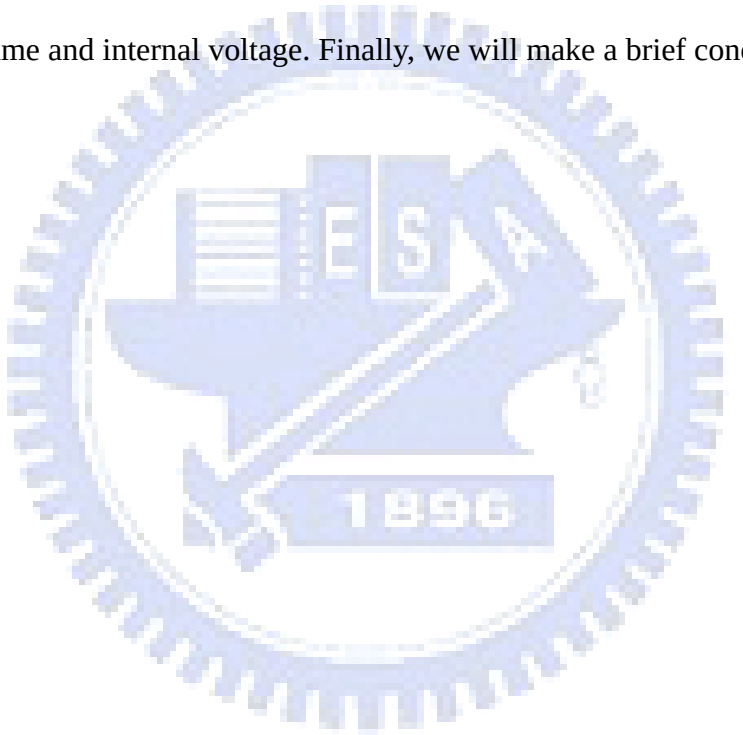
Chapter 1
Introduction

In recent years, power device are strongly demanded for the applications in driver circuits [1], power switches [2], and ratio frequency (RF) power amplifiers [3]. The integrated bipolar, complement metal-oxide-semiconductor (CMOS), and double-diffused metal-oxide-semiconductor (DMOS) process has been developed to realize complex single power ICs [4,5]. Among the candidates of high-voltage devices, lateral DMOS (LDMOS) transistors are most attractive because they can easily integrated with standard low-voltage CMOS process [2,4-5]. Since the LDMOS has been widely utilized in high-voltage and high-current output circuits [6,7], the reliability issues in both DC (Fig. 1.1) and AC (Fig. 1.2) conditions becomes more and more important.

Hot carrier effect, flicker noise, and self-heating effect are three major reliability issues in LDMOS. In driver application, LDMOS is biased at high drain voltage, which would result in serious hot carrier degradation. Various hot carrier stress modes may generate interface traps and oxide charge in different regions of the device. The profiling of trap distribution and characteristics is important to the study of the device reliability. For RF power amplifiers, the LDMOS is operated in high-power and high-frequency conditions. High-power would increase heat generation in LDMOS and thus the self-heating effect can be observed. In addition, as the LDMOS is used in amplifier application, low frequency noise (flicker noise) behavior would become important. In order to reduce the low frequency noise in LDMOS, the correlation between stress mode and flicker noise degradation must be studied. Since LDMOS is sometimes subjected to AC stress rather than DC stress, we also investigate the effect

of transient hot carrier degradation [10] especially for temperature-related reliability issues.

This thesis is organized as follows: Chapter1 is introduction. Chapter2 shows various DC hot carrier degradation modes and their corresponding flicker noise charcateristics. A three-region charge pumping technique and two-dimensional device simulation are used. Chapter3 shows the impact of self-heating effect on hot carrier degradation in LDMOS. Transient circuit measurement is used to characterize self-heating effect. A special metal contact structure is fabricated to characterize the self-heating time and internal voltage. Finally, we will make a brief conclusion.



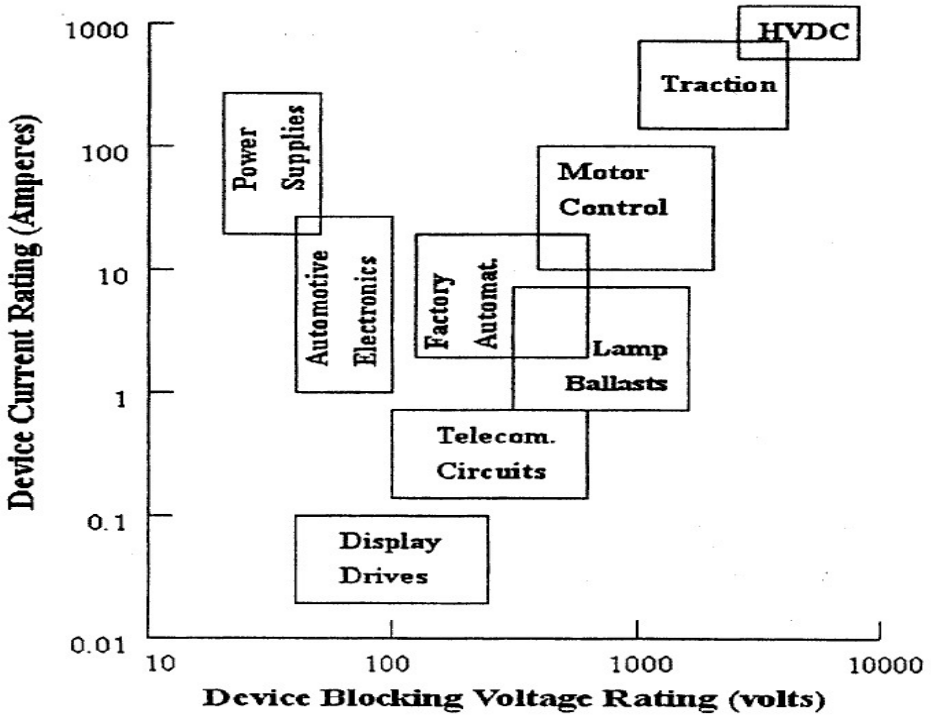


Fig. 1.1 Applications for power devices in relation to their voltage and current ratings

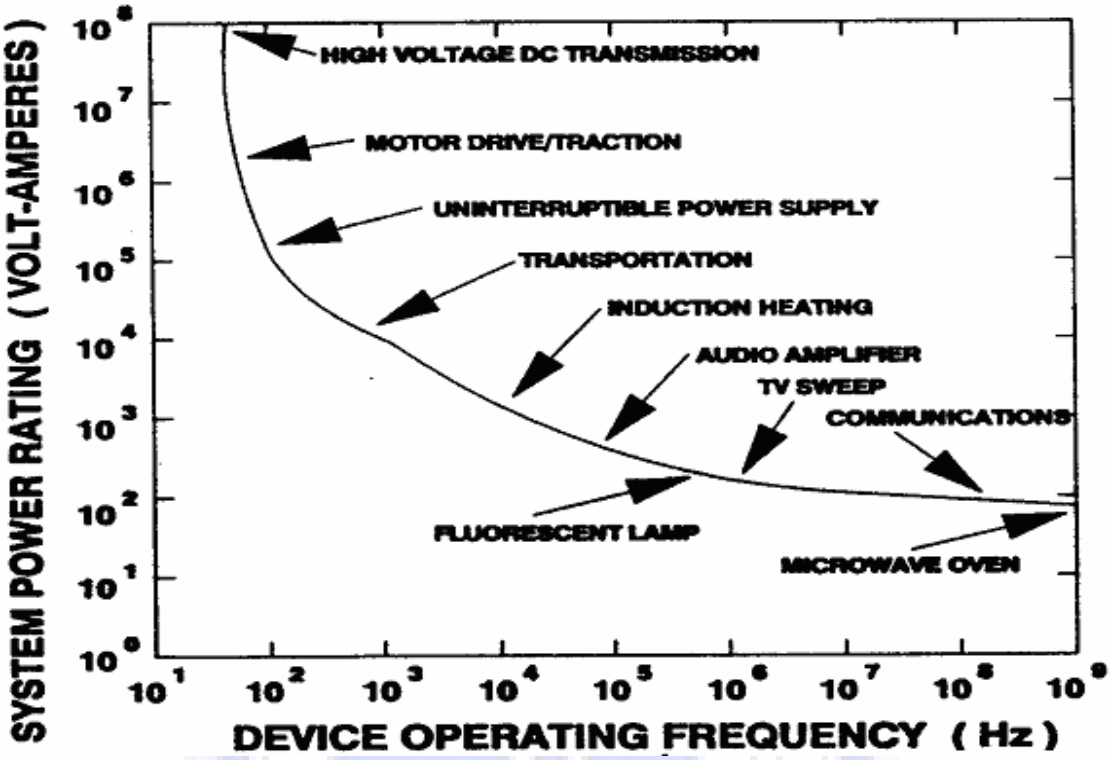


Fig. 1.2 Applications for power devices in relation to device operating frequency and system power rating.

Chapter 2

Drain Current Flicker Noise Degradation in Various Hot Carrier Degradation Modes

2.1 Introduction

Recently, LDMOS has been widely utilized in high-performance radio frequency (RF) components. The signal-to-noise ratio in RF power amplifiers will seriously affect the device performance. In order to reduce low-frequency noise in analog devices, the physical origin of flicker noise in LDMOS devices should be further explored. Since LDMOS is always biased at high drain voltage, hot carrier degradation would become a serious issue. Thus, various hot carrier stress modes induced oxide damage should be discussed.

In this chapter, we used a three-region charge pumping (CP) technique to probe hot carrier stress induced oxide damage in a LDMOS. The n-LDMOS used in this work was processed in a 0.18μm CMOS technology with a gate oxide thickness of 100nm and a field oxide thickness of 500nm. The operation voltages are V_g=40V and V_d=40V. Fig. 2.1(a) shows the cross-section of a LDMOS with an additional metal contact to sense an internal voltage. This small contact is arranged in a drift region with a n+ implant. The device is divided into three regions. Region (I) is the channel region. Regions (II) and (III) are the accumulation region and the field oxide region. The length of each region is denoted by L_{chan}(=3μm), L_{acc}, and L_{fox}, respectively. The gate width is 20μm and the threshold voltage is 1.5V. The device flat-band voltage (V_{FB}, solid line) and threshold voltage (V_T, dash line) distribution of the three regions are plotted in Fig. 2.1(a). A two-dimensional device simulation is performed to

identify an impact ionization generation (IIG) region in the device. In addition, two flicker noise measurements, low Vg (Vg=2V, Vd=0.1V) noise and high Vg (Vg=18V, Vd=0.1V) noise, are performed before and after hot carrier stress.

Three stress modes, mode A (max. I_b), mode B (V_g~1/2V_d), and mode C (max. I_g) are investigated. The I_g-V_g and I_b-V_g of a n-LDMOS are shown in Fig. 2.2(a). The maximum I_b (mode A) occurs in V_g/V_d=8V/50V and maximum I_g (mode C) occurs in V_g/V_d=50V/50V. The bias conditions of the three stress modes are also shown in the Fig. 2.2(b). Subthreshold slope and linear drain current (I_{dlin}) are measured to monitor device performance degradation.

2.2 Three-Region Charge Pumping Technique

The gate voltage waveform in CP measurement is illustrated in Fig. 2.1(b) with a fixed V_{gh}=12V and a variable V_{gl}. For the 100nm thick gate oxide, V_{gl} is switched from +3.6V to -40V without a significant gate oxide tunneling current. In this V_{gl} range, all the three regions of the device can be probed. The measurement frequency is 200 kHz. Typical CP measurement result is shown in Fig. 2.3. The charge pumping current (I_{cp}) exhibits three stages, corresponding to the three regions of a n-LDMOS respectively. It should be noticed that each stage has their corresponding threshold and flat-band voltage. By measuring the change of I_{cp} and V_{FB} after stress in each stage, we are able to separate N_{it} and Q_{ox} in each region of the device, for example, ΔN_{it}(channel)=ΔI_{cp}(stage 1)/$qfWL_{chan}$, ΔQ_{ox}(acc.)=ΔV_{FB} (stage 2)·C/q and so on.

2.3 Flicker Noise Measurement

A special device structure incorporating a metal contact in a drift region is fabricated, which allows us to separately measure the oxide degradation in each part

of a LDMOS. The channel region of LDMOS can be considered as an intrinsic MOS. The comparison between LDMOS and MOS is discussed in Fig. 2.4 and Fig. 2.5. The DC characteristic of MOS (Fig. 2.4(a)) is nearly the same as the LDMOS, indicating that the low Vg LDMOS current is mainly controlled by the channel region. Fig. 2.5(a) further shows a similar result. The flicker noise of LDMOS in low Vg operation is mainly controlled by the channel region. In high Vg measurement, the drift region limits the LDMOS current and a difference in current distribution is observed in Fig. 2.4(b). Thus, the flicker noise of LDMOS in Fig. 2.5(b) exhibits a smaller noise behavior.

2.4 Three Hot Carrier Stress Modes

2.4.1 Max. I_b Stress Mode

Fig. 2.6(a) shows the I_{cp} in a fresh device and after 1400 sec. max. I_b stress (@V_g/V_d =8V/50V). The post-stress I_{cp} in the first stage is nearly the same as the pre-stress one, indicating that region (I) oxide is not damaged by the stress. The post-stress I_{cp} in stage 2, however, exhibits an upward shift while the flat-band voltage keeps the same (no rightward shift in the I_{cp}). This feature suggests N_{it} generation in region (II) but no Q_{ox} creation. Numerical device simulation also shows the maximum IIG rate in region (II) (Fig. 2.6(b)). Although interface trap generation is observed from the I_{cp}, the subthreshold swing of the device is not affected because the generated N_{it} is distributed in region (II). In addition, I_{dlin} degradation is not observed either. Fig. 2.7(a) and (b) show the flicker noise of LDMOS in low Vg and high Vg measurement, respectively. A significant flicker noise increase is observed in high Vg measurement. Since gate voltage in high Vg measurement is higher than threshold voltage, the flicker noise would be mainly affected by interface state. Thus, an

increase flicker noise in Fig. 2.7(b) and no Idlin degradation are observed.

2.4.2 Vg~1/2Vd Stress Mode

The I_{cp} results before and after mode B stress (@V_g/V_d =30V/50V) are shown in Fig. 2.8(a). N_{it} generation in stress mode B is relatively small and can be realized due to a smaller substrate current (or a smaller IIG region in Fig. 2.8(b)), as compared to stress mode A. Unlike stress mode A, a distinct flat-band voltage shift in region (II) is noticed, which is manifested by a rightward shift of the I_{cp} in stage 2. An arrow is drawn in Fig. 2.8(a) to indicate the flat-band voltage shift (ΔV_{FB2}). The rightward shift of the slope is caused by negative Q_{ox} creation in region (II). As the stress time increase (Fig. 2.9), the slope in stage 2 keeps the same and ΔV_{FB2} versus stress time can be extracted. From the extracted ΔV_{FB2}, the average Q_{ox2} generation rate (Fig. 2.9) can be calculated by using the equation in section 2.2. Because of negative Q_{ox} creation, the resistance beneath the bird's beak increases. At a large V_g, region (I) resistance is relatively small and the resistance in the bird's beak region has a larger effect. Thus, I_{dlin} degradation at a higher measurement V_g =40V is observed (Fig. 2.10). The flicker noise results before and after stress are shown in Fig. 2.11. Since Nit generation in region (II), the flicker noise also increases in high Vg noise measurement (Fig. 2.11(b)).

2.4.3 Max. I_g Stress Mode

Fig. 2.12(a) shows the I_{cp} result before and after max. I_g stress (@V_g/V_d=50V/50V) for 1000 seconds. Significant N_{it} and Q_{ox} generation was noticed in region (I) and (II), respectively. It should be pointed out that a two-dimensional device simulation reveals that the IIG region splits into two parts (Fig. 2.12(b)); One is in the channel (region (I)) and the other is underneath the bird's beak. Two different stress induced oxide

degradation mechanisms are noticed; One is N_{it} generation in region (I) and the other is negative Q_{ox} creation in region (II). These two trap creation processes are reflected by an upward shift of the first stage I_{cp} denoted by ΔI_{cp1} and by a rightward shift of the second stage I_{cp} (ΔV_{FB2} in Fig. 2.12(a)). In contrast to stress mode A, N_{it} generation occurs in region (I) rather than in region (II), which results in a significant subthreshold swing degradation (Fig. 2.13) in stress mode C. In addition, Q_{ox2} creation results in a more serious I_{dlin} degradation (Fig. 2.14) in mode C than in mode B. Note that the I_{dlin} degradation in Fig. 2.14 is more apparent at a larger Vg. This is because the region (II) resistance occupies a larger part of the total resistance at a larger Vg.

The N_{it1} and Q_{ox2} growth rate in stress mode C are shown in Fig. 2.15 and Fig. 2.16, respectively. The growth rate obeys a power-law time dependence and the average power factor is around 0.25, which is in agreement with [11]. Due to oxide charge creation in region (II), a larger region (II) resistance results and the current flow in region (II) is pushed deeper into the substrate. Consequently, mobility exhibits a saturated effect and thus I_{dlin} degradation shows a tendency to saturate in Fig. 2.17. This mobility saturation model is also described in [12,13] for MOSFET and [14] for LDMOS structure. By comparing mode A and B, the post-stress flicker noise exhibits an increase in Fig. 2.18(a) and (b) because of the Icp increase in channel region and Nit generation in accumulation region.

2.5 Summary

Drain current flicker noise degradation in various hot carrier modes is investigated. Max. Ib stress mode shows a significant flicker noise increase in drift region but no Idlin degradation. The increased flicker noise is attributed to the interface trap generation in drift region. Max. Ig stress mode shows a degradation of flicker noise in

both channel region and drift region because of interface trap generation in these regions. The Idlin degradation in max Ig stress mode is worse than max. Ib stress mode, which is attributed to the negative oxide charge creation in drift region. The LDMOS degradation behavior and trap properties in the three stress modes are summarized in Table 2.1.

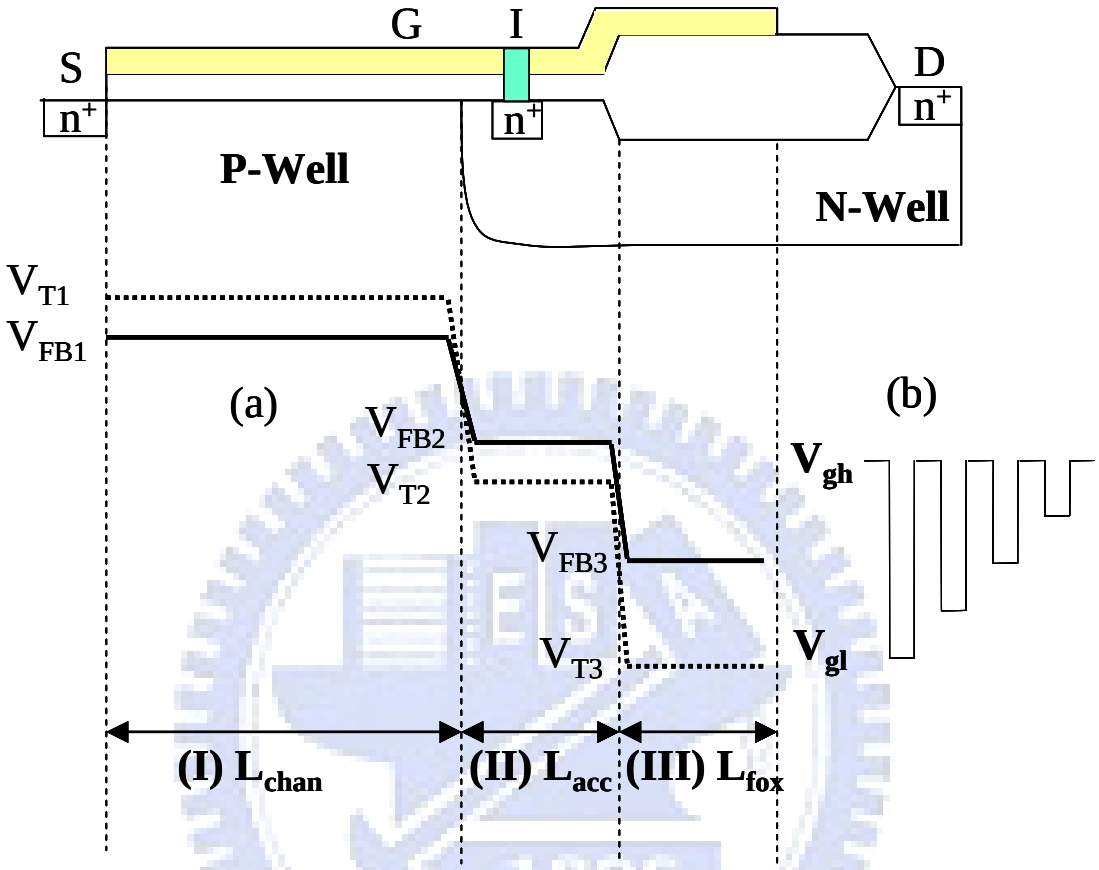
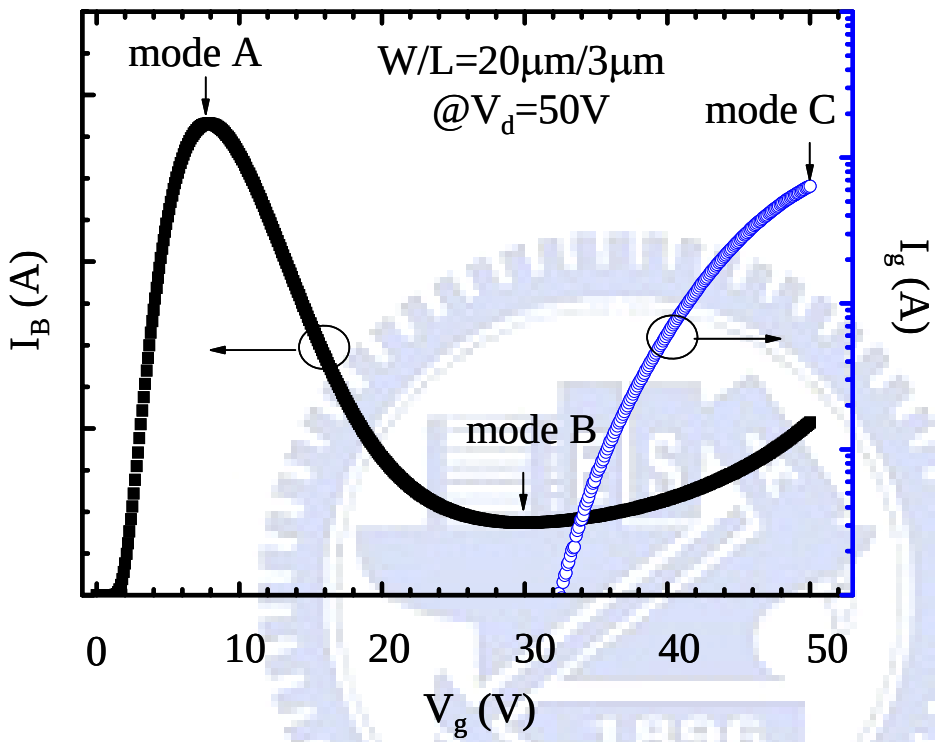


Fig. 2.1 (a) Cross-section of a metal contact n-LDMOS and corresponding flat-band (solid line) and threshold (dash line) voltage distribution. The device is divided into three parts, L_{chan} (channel region), L_{acc} (accumulation region), and L_{fox} (field oxide region).

(b) Illustration of a charge pumping measurement wave form. The V_{gh}=12V is fixed and V_{gl} varies from +3.6 to -40V.

(a)



(b)

mode	Vg/Vd
A	8 /50
B	30/50
C	50/50

Fig. 2.2 (a) Substrate current and gate current versus gate voltage in a LDMOS. Three different stress modes are shown in the figure, mode A (maximum I_b), mode B (V_g~1/2V_d), and mode C (maximum I_g).

(b) The bias conditions of the three stress modes.

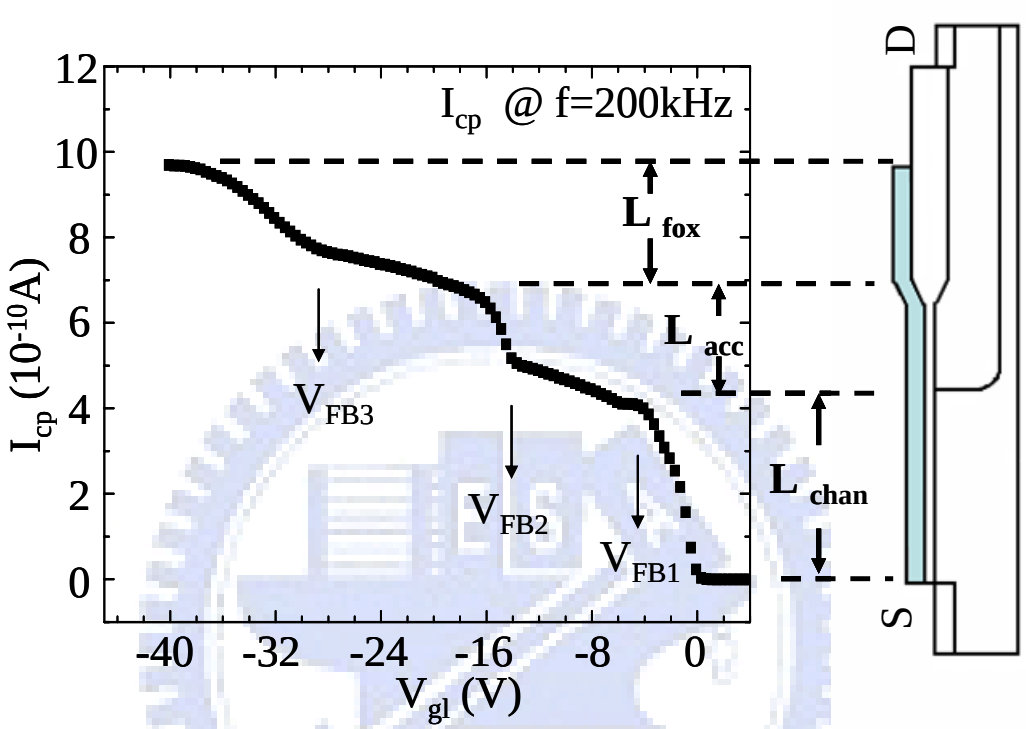


Fig. 2.3 Typical CP current in a n-LDMOS. The three stages of the CP current correspond to the three regions of the device. The flat-band voltage of each region is indicated in the figure. The frequency in charge pumping measurement is fixed at 200 KHz.

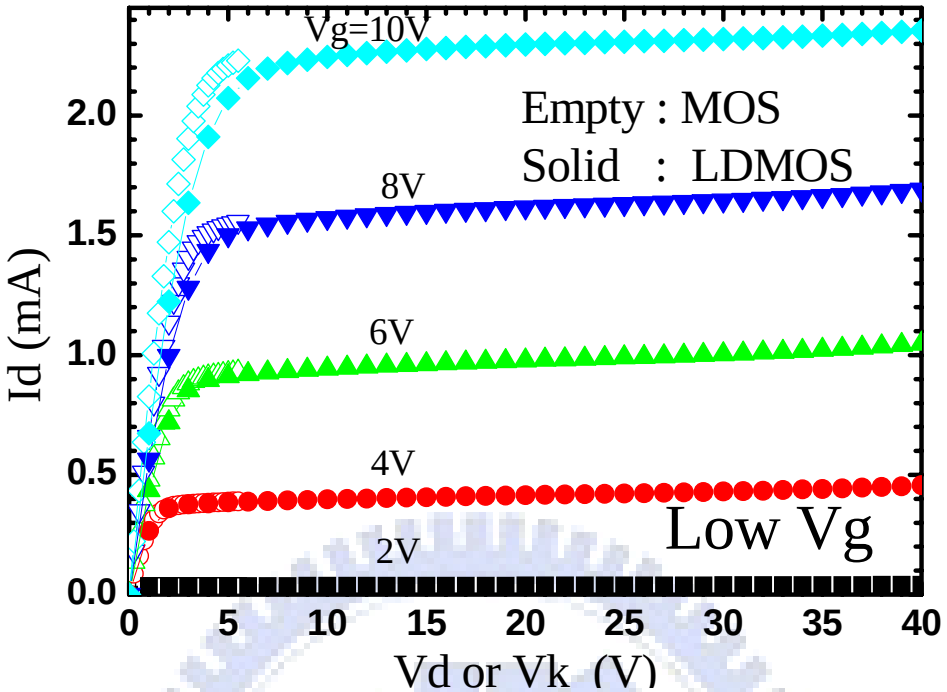


Fig. 2.4 (a) I-V characteristics in MOS and LDMOS at low gate voltage.

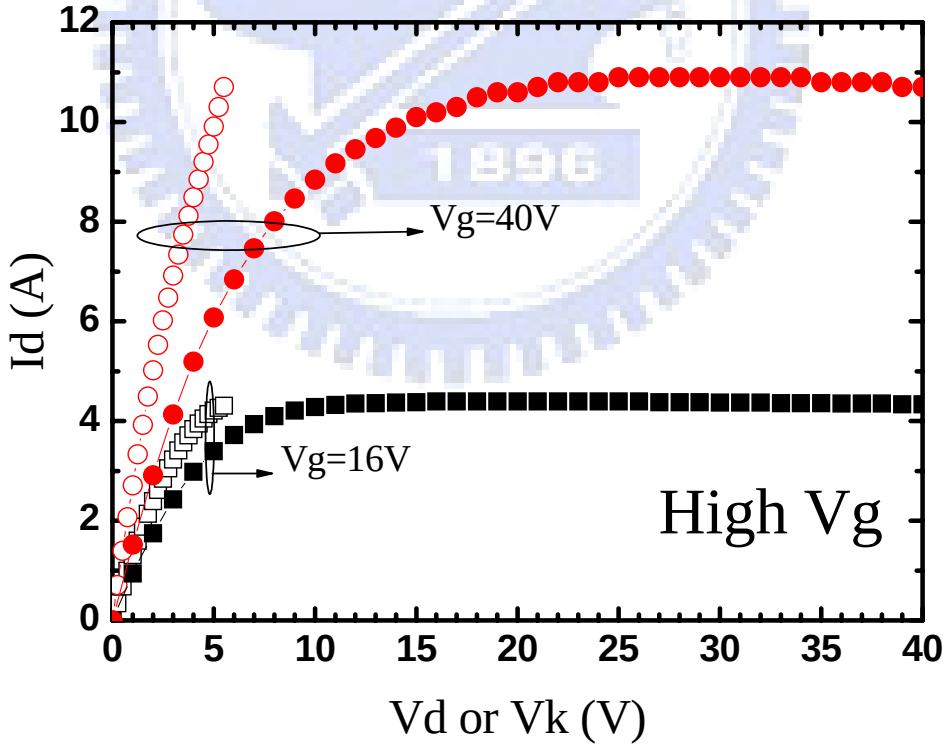


Fig. 2.4 (b) I-V characteristics in MOS and LDMOS at high gate voltage

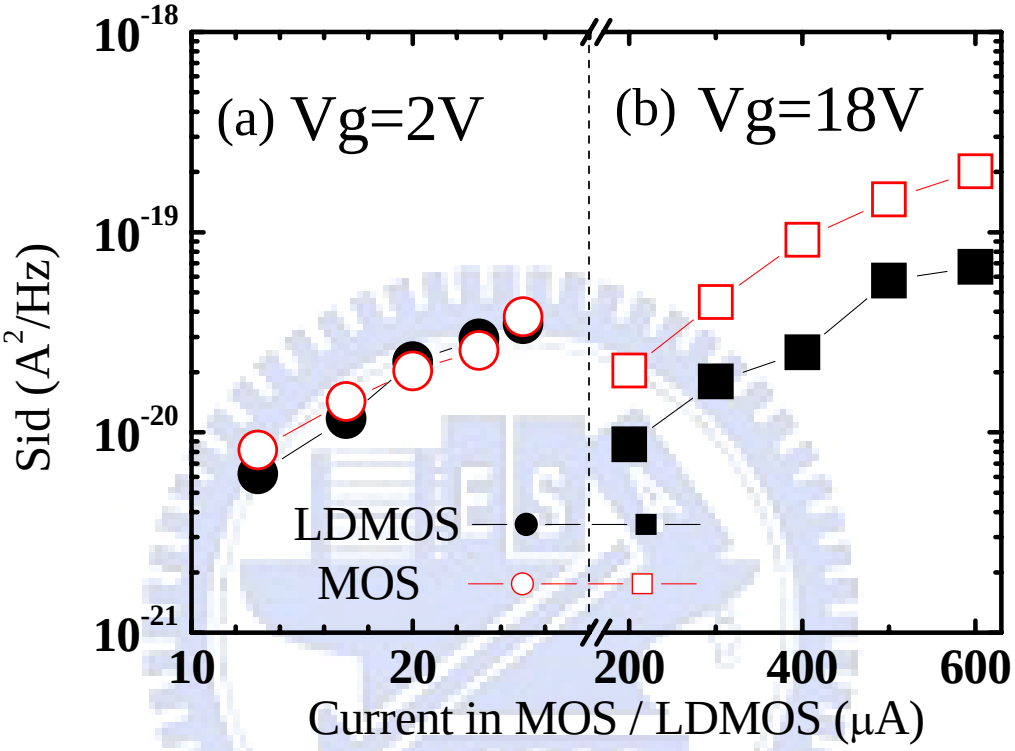


Fig. 2.5 Flicker noise in MOS and LDMOS at (a) low and (b) high gate voltage.

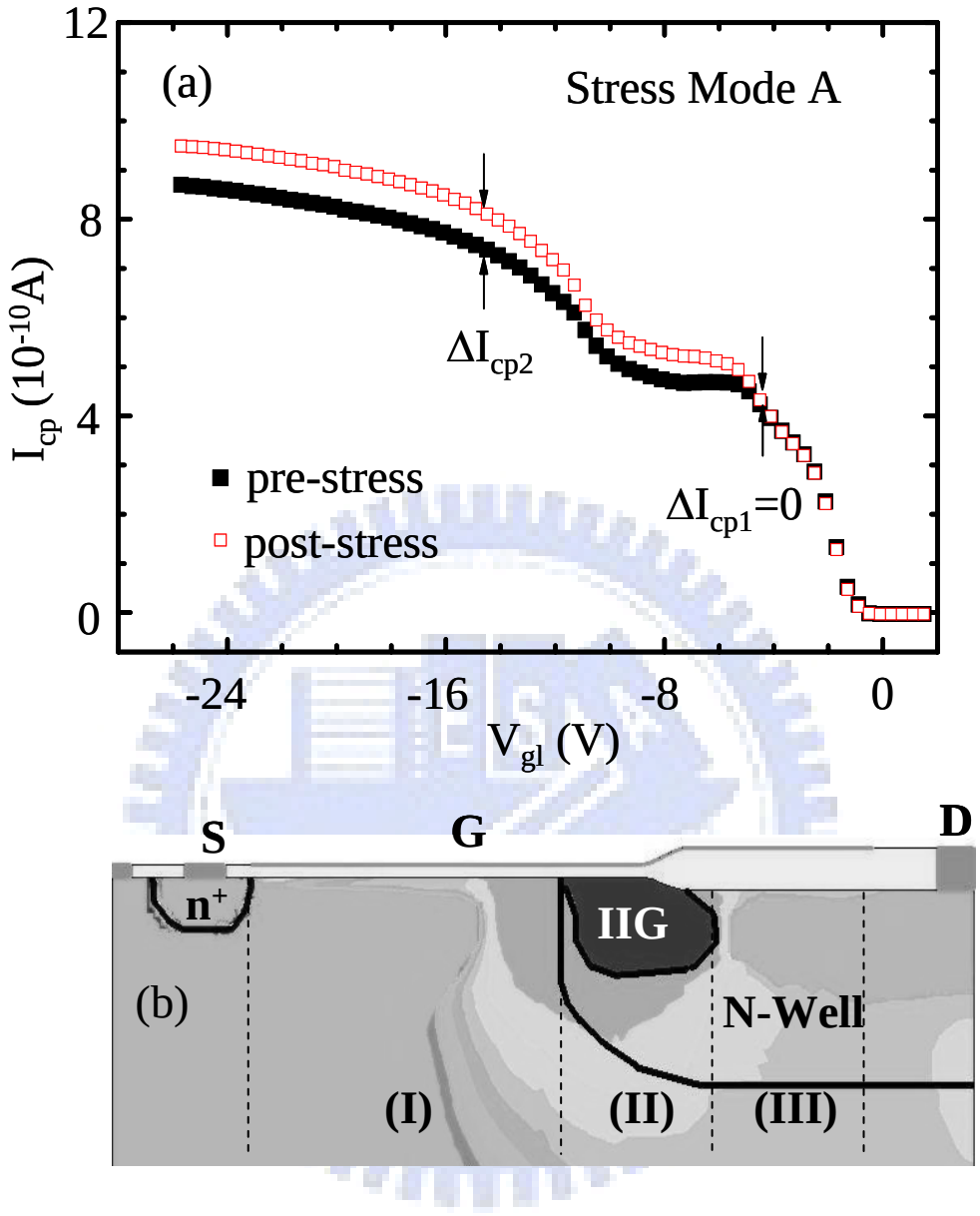


Fig. 2.6 (a) Charge pumping current versus V_{gl} before and after 1400 sec. mode A stress. Upward shift of the I_{cp} in stage 1 implies the generation of interface trap in the accumulation region.

(b) Two-dimension device simulation of impact ionization (IIG) distribution in stress mode A.

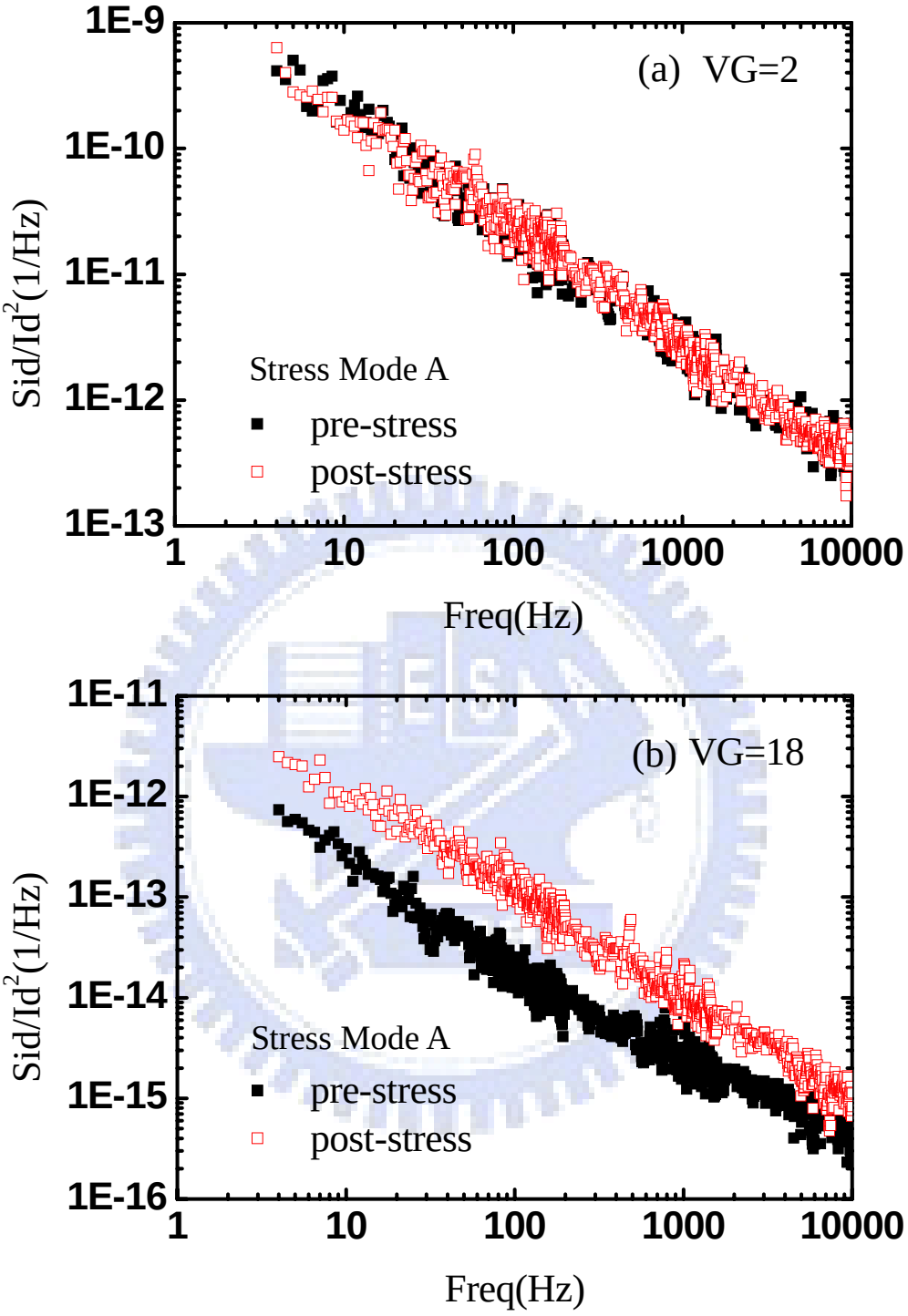


Fig. 2.7 (a) Low gate voltage and (b) High gate voltage flicker noise before and after mode A stress. The increase of high gate voltage flicker noise is caused by trap creation in the drift region.

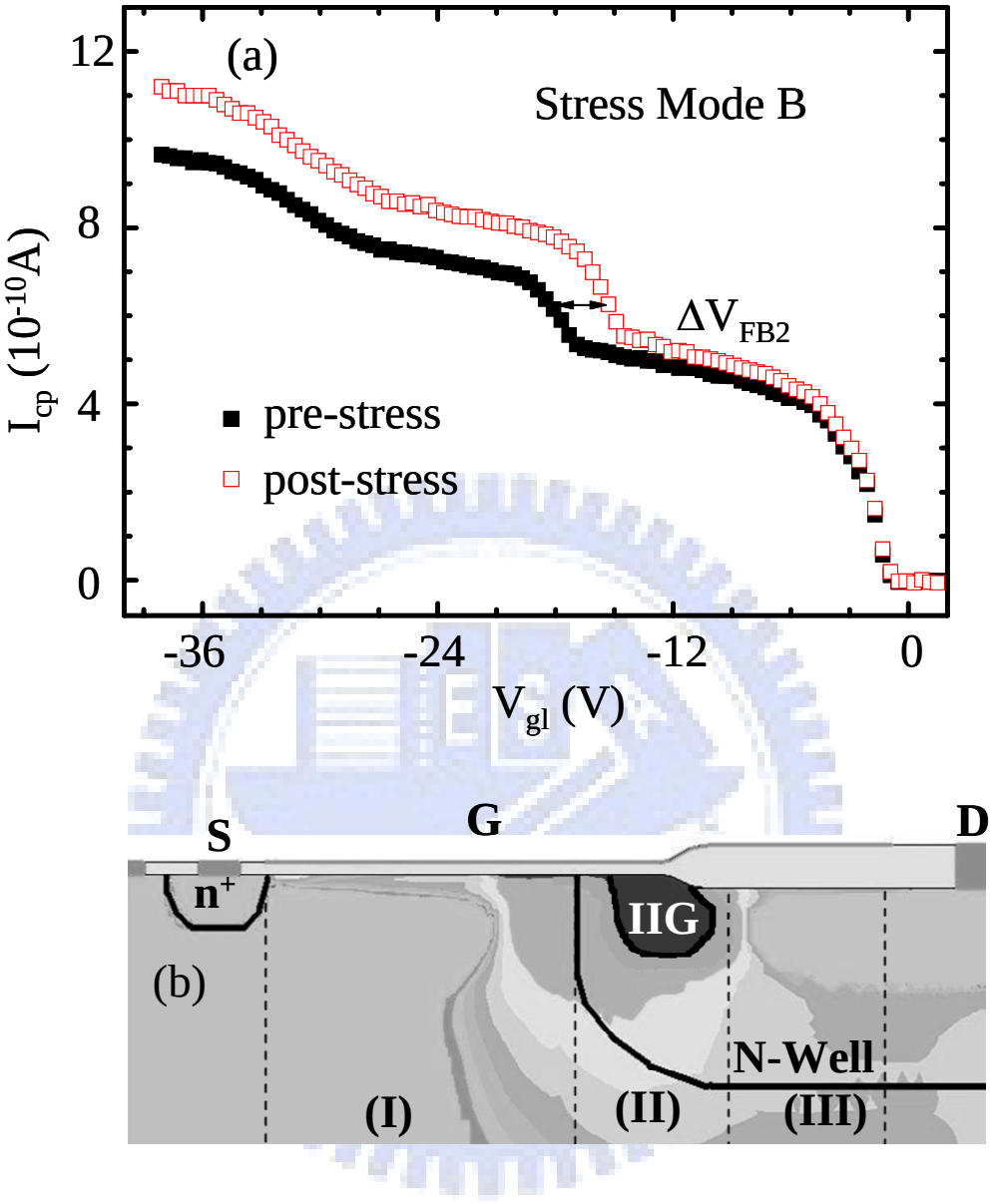


Fig. 2.8 (a) Charge pumping current versus V_{gl} before and after 1400 sec. mode B stress. The shift of the flat-band voltage in stage 2 implies the generation of negative oxide charge in the accumulation region. (b) Two-dimension device simulation of impact ionization (IIG) distribution in stress mode B.

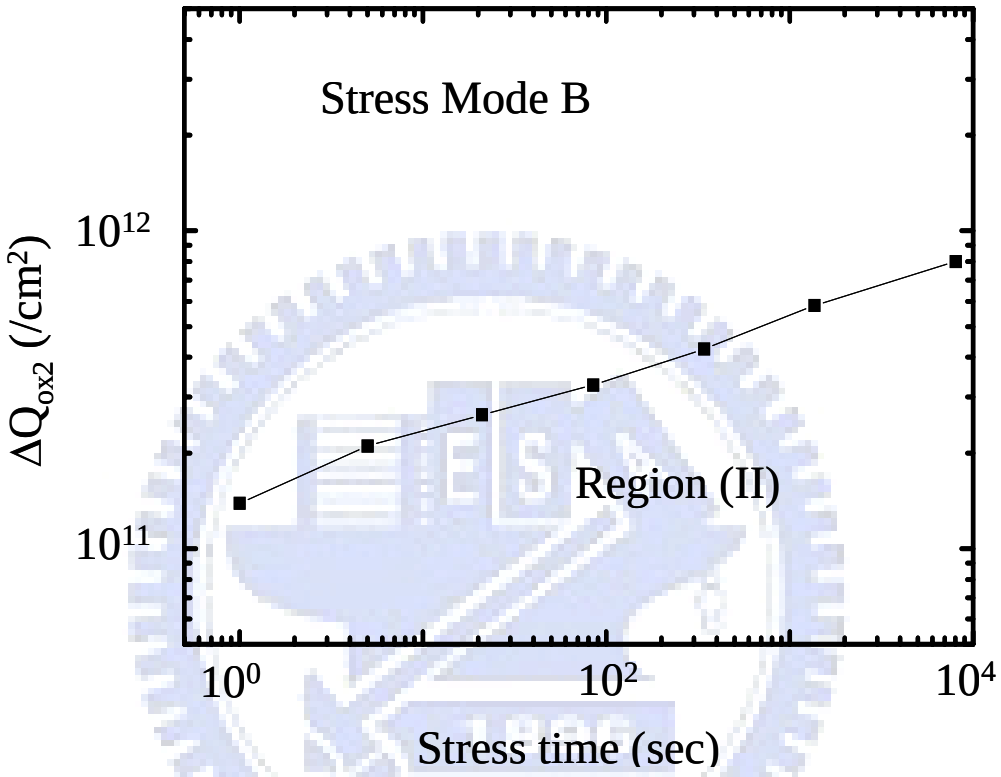


Fig. 2.9 Region (II) oxide trapped charge growth rate in stress mode B.

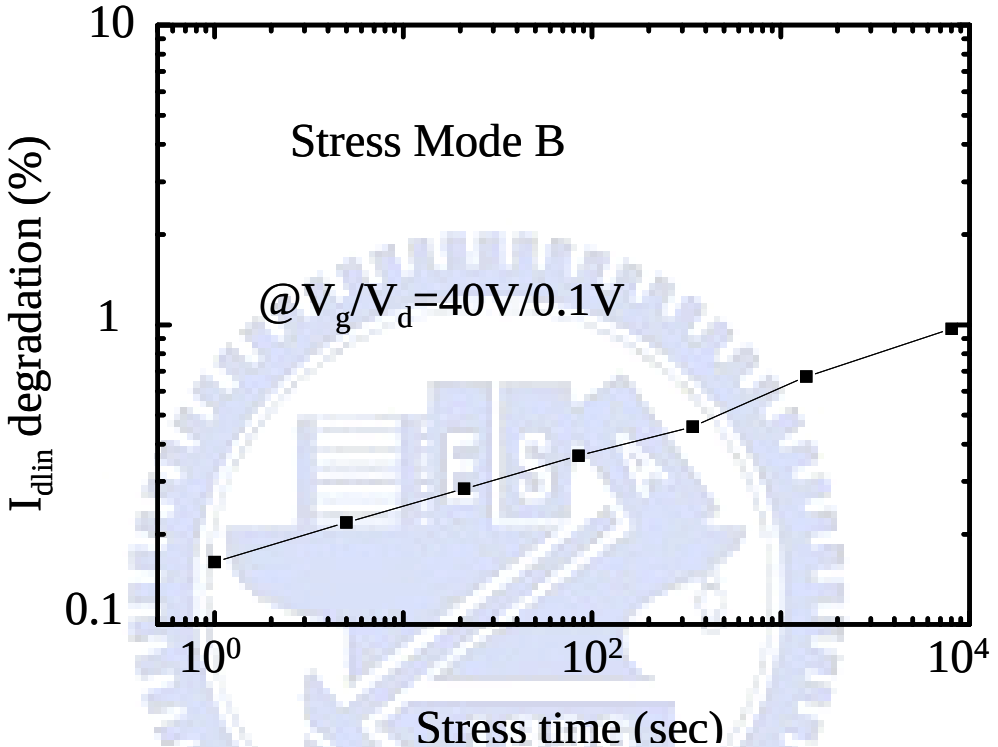


Fig. 2.10 Linear drain current (I_{dlin}) degradation rate measured at V_g/V_d=40V/0.1V in stress mode B.

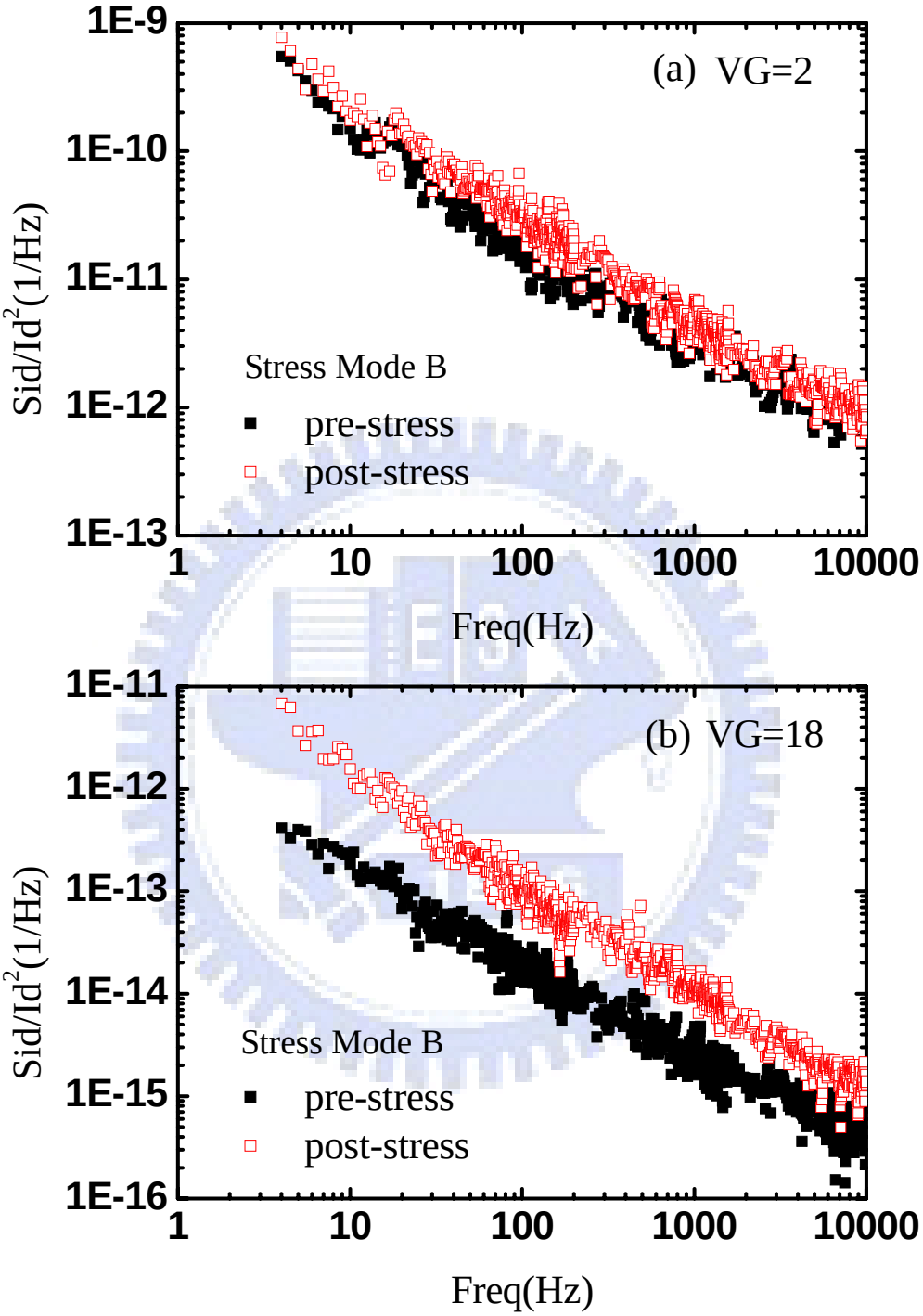


Fig. 2.11 (a) Low gate voltage and (b) High gate voltage flicker noise before and after mode B stress. The increase of high gate voltage flicker noise is caused by damage in the drift region.

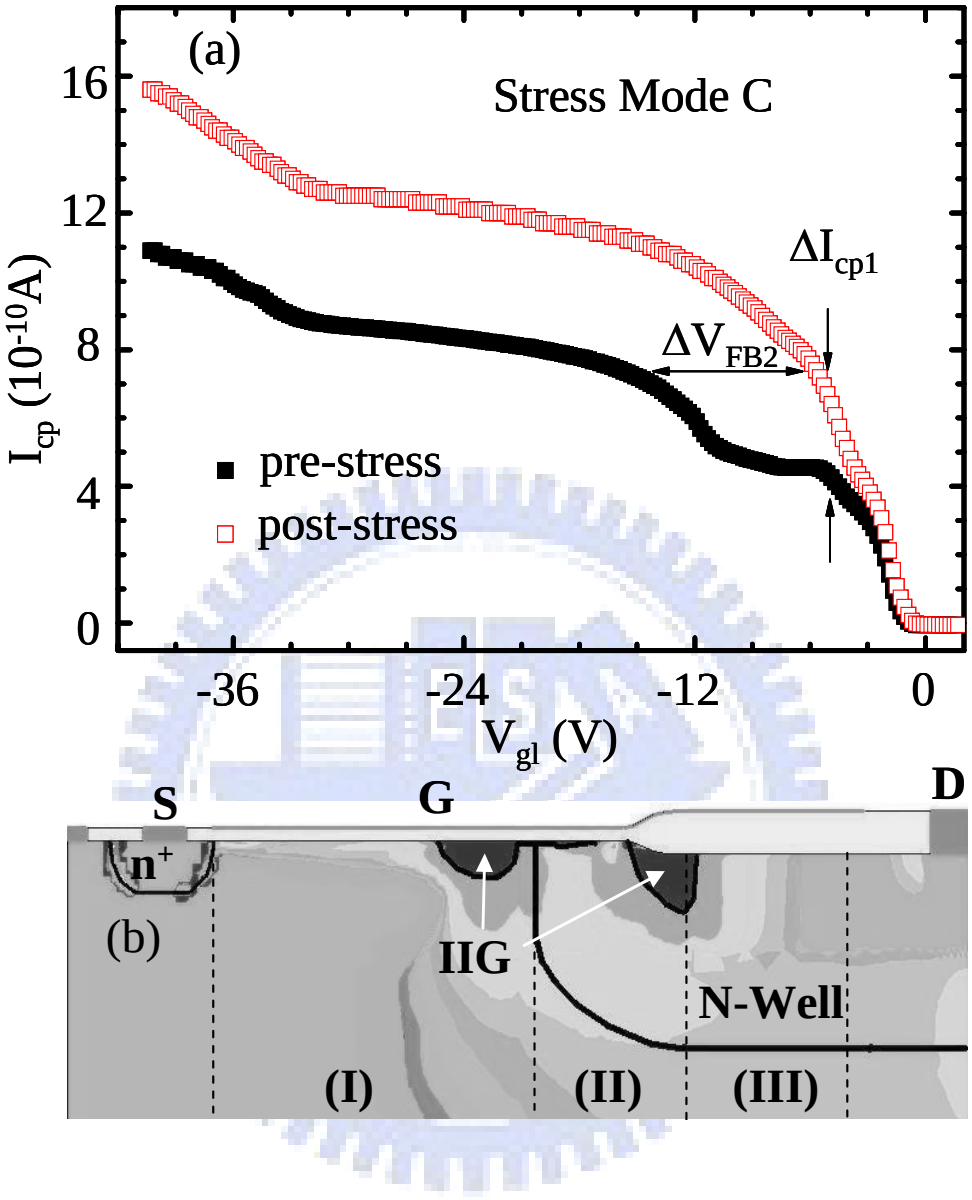


Fig. 2.12 (a) Charge pumping current versus V_{gl} before and after 1000 sec. mode C stress. Upward shift of the I_{cp} in stage 1 indicates interface trap generation in the channel region, and rightward shift of flat-band voltage in stage 2 implies oxide charge creation in the accumulation region.

(b) Two-dimension device simulation of impact ionization (IIG) distribution in stress mode C.

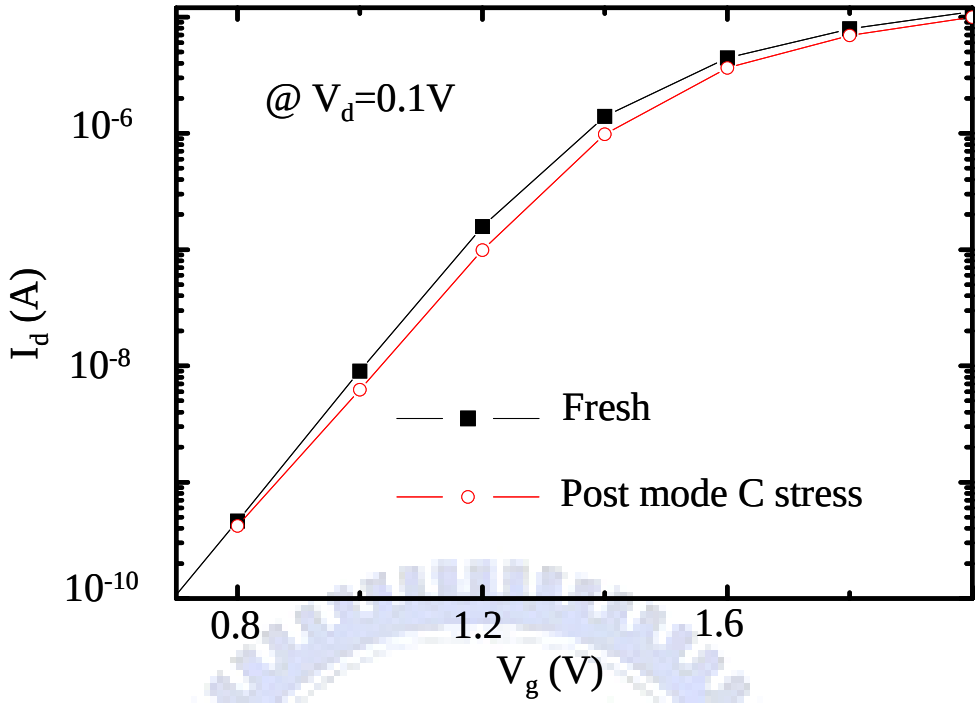


Fig. 2.13 Subthreshold characteristics before and after mode C stress. The swing degradation was attributed to interface trap generation in the channel region.

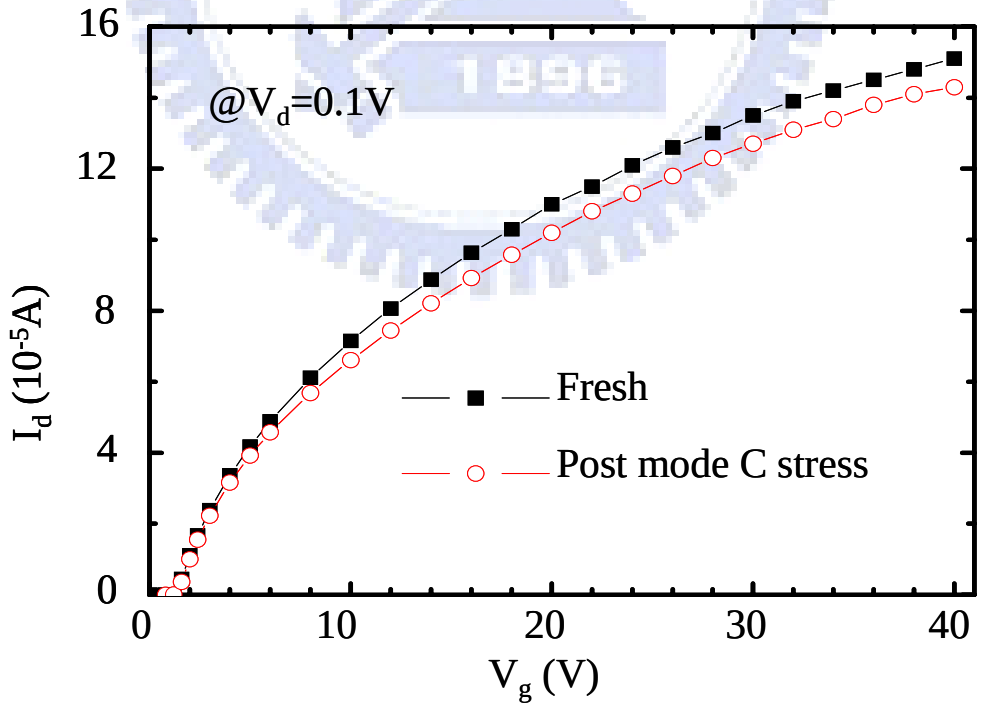


Fig. 2.14 Linear drain current versus V_g before and after mode C stress.

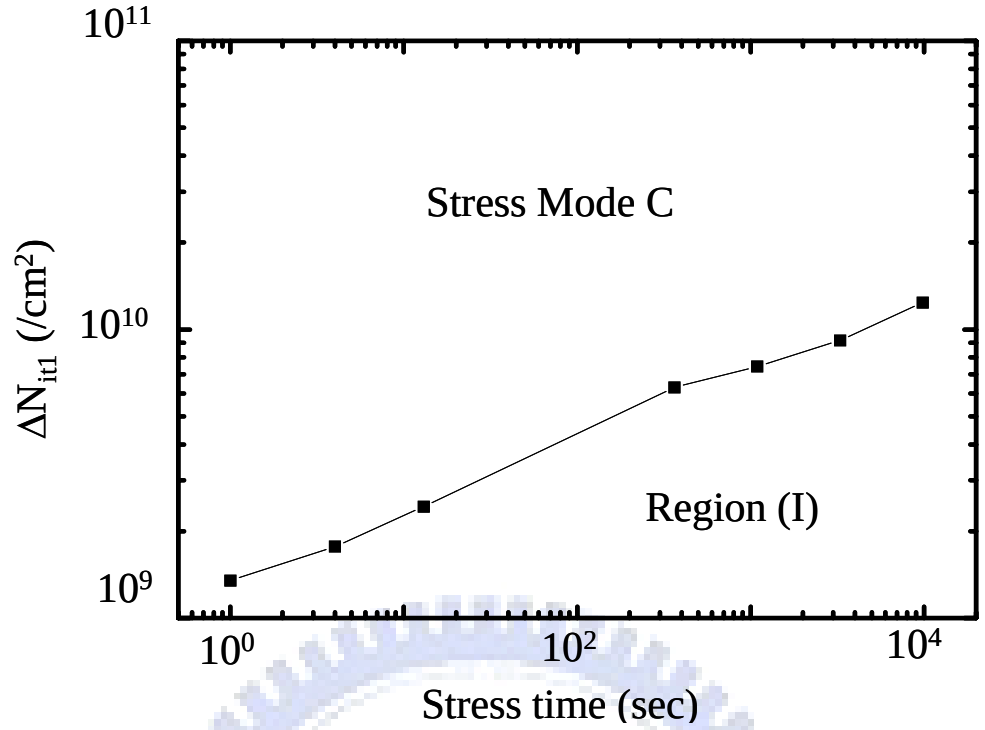


Fig. 2.15 Region (I) interface trap growth rate in stress mode C.

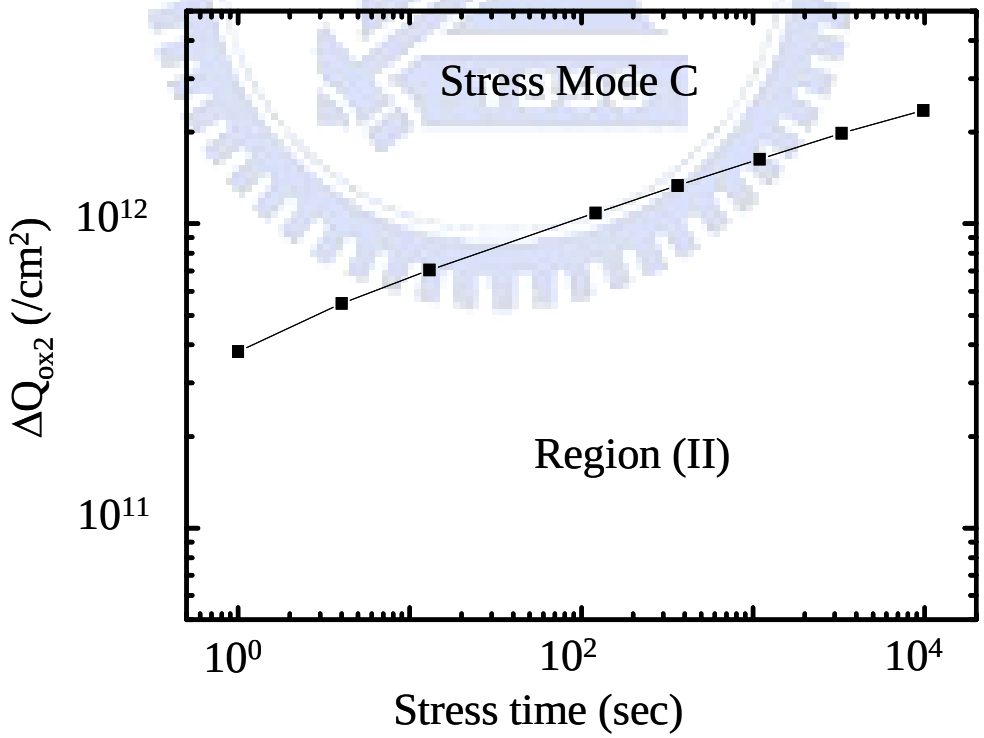


Fig. 2.16 Region (II) oxide charge growth rate in stress mode C.

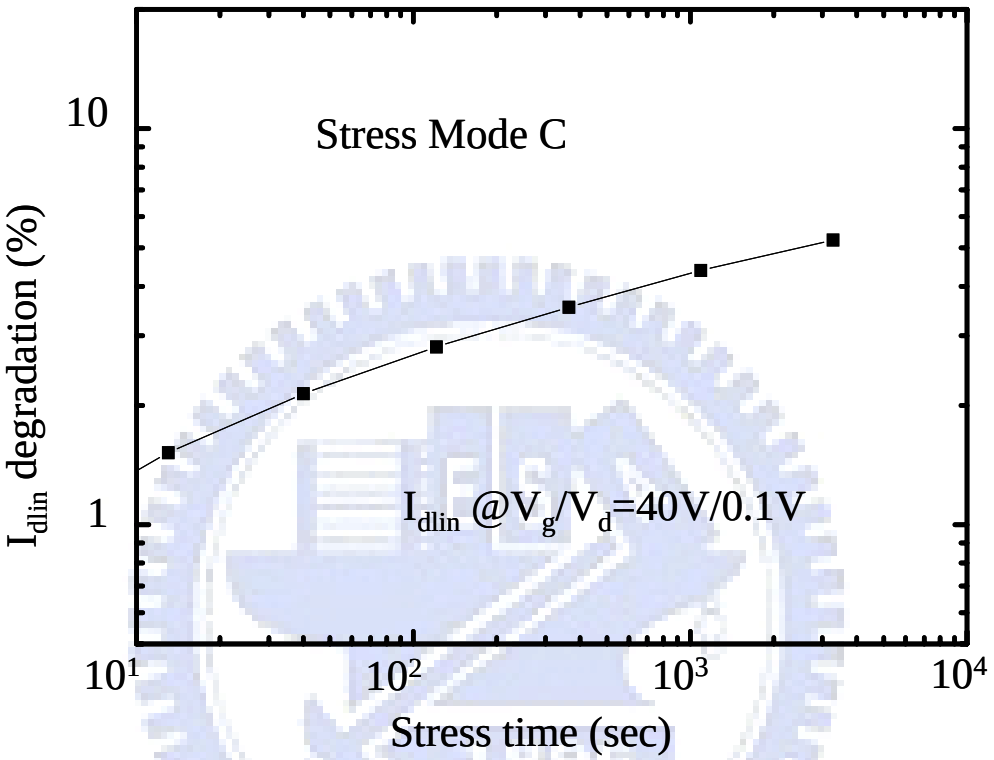


Fig. 2.17 I_{dlin} degradation versus stress time in stress mode C. The degradation is mainly caused by negative oxide charge creation in the drift region.

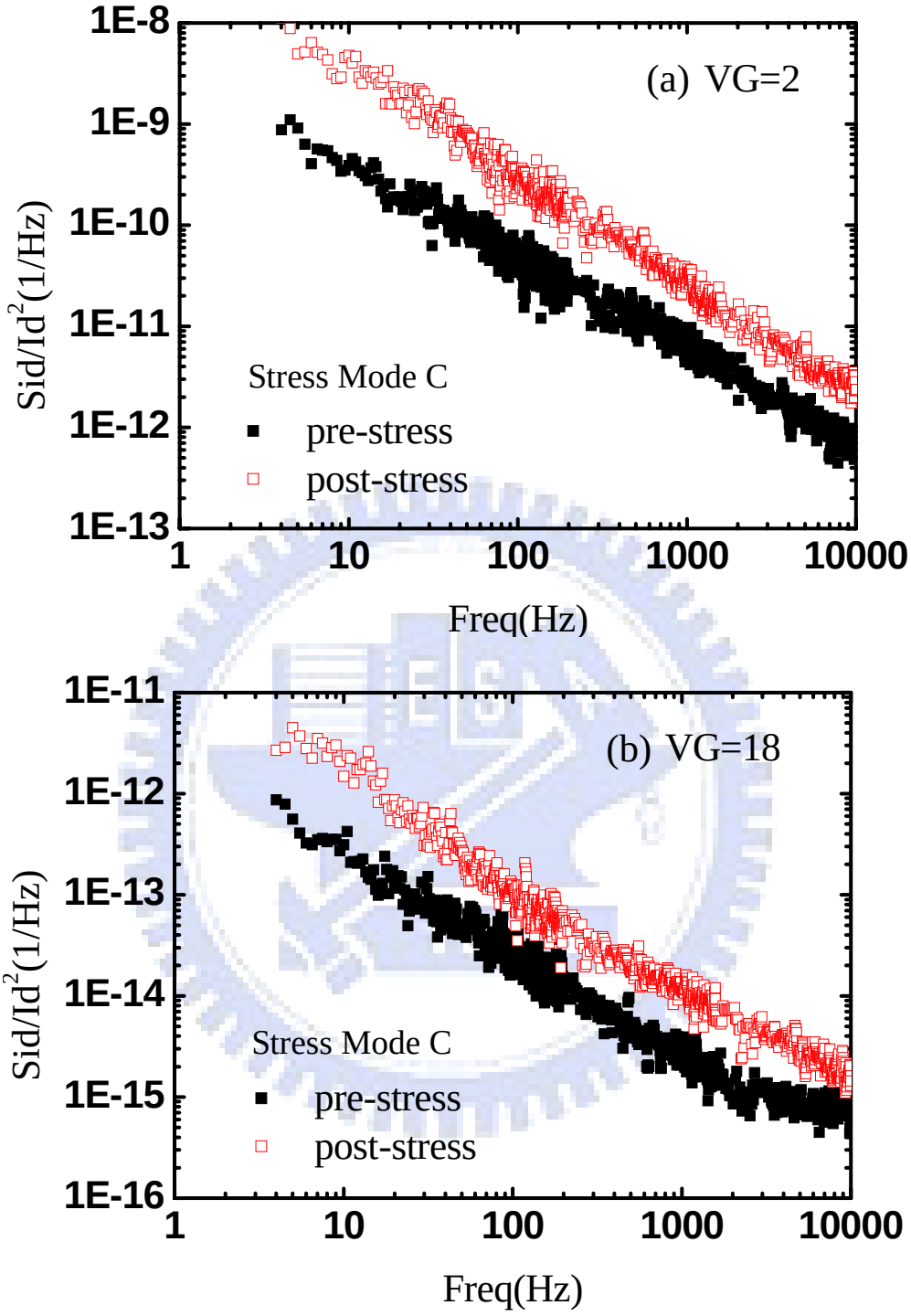


Fig. 2.18 (a) Low gate voltage and (b) High gate voltage flicker noise before and after mode C stress.

Table 2.1

Mode (Vg/Vd)	A (8V/50V)		B (30V/50V)		C (50V/50V)	
Trap Location	Region (I)	Region (II)	Region (I)	Region (II)	Region (I)	Region (II)
Trap Property	N/A	N_{it}	N/A	Q_{ox}	N_{it}	Q_{ox}
Device Deg.	N/A	N/A	N/A	I_{dlin}	$I_{subthreshold}$	I_{dlin}
Noise	N/A	Increase	N/A	Increase	Increase	Increase

Chapter 3
Impact of Self-Heating Effect on Hot Carrier Degradation

3.1 Introduction

Lateral diffused MOS (LDMOS) transistors have been widely utilized in today's high-voltage/high-current drivers and RF power amplifiers [3,10]. High power consumption would increase heat generation in LDMOS and thus the self-heating effect (SHE) can be observed. SHE would significant affect the drain current and result in a negative output conductance [15]. Since LDMOS is subjected to AC stress rather than DC stress in certain applications, it is imperative to investigate the SHE on transient hot carrier degradation. To the purpose, we fabricate a special LDMOS structure, which incorporates a metal contact in the drift region. Thus, an internal voltage transient due to SHE can be probed directly.

Linear drain current (I_{dlin}@V_g/V_d=40V/0.1V) is measured to monitor device degradation under AC or DC stress. A three-region charge pumping technique [16] is used to locate the damage area and corresponding trap properties. Two-dimensional device simulation is also performed to calculate impact ionization generation (IIG) rate in SHE and non-SHE conditions.

3.2 Self-Heating Effect

The setup for a transient measurement is shown in Fig. 3.1. A small resistance (10Ω) is arranged for the purpose of transient current measurement. The transient measurement of different device width and length is shown in Fig. 3.2. The SHE is

more serious in a larger (W/L) device due to a higher current density. Fig. 3.3(a) shows the normalized drain current (I_d/W) versus V_d in small and large width devices under DC (Agilent 4156) measurement. The I_d/W in linear region is nearly the same, indicating no process variations in these two devices. However, the larger width device exhibits a smaller I_d/W in the saturation region. The reduction of the saturation current is attributed to self-heating caused mobility degradation. Fig. 3.3(b) further shows the I_d/W in a DC and a fast transient measurement for a large width device. A larger I_d/W is noticed in the transient measurement because of the elimination of SHE.

A metal contact structure is used to probe the internal voltage (V_I) near the bird's beak, as shown in Fig. 3.4. Three-regions of a LDMOS are indicated, including channel region, accumulation region and field-oxide region. The contact is arranged in accumulation region with a n+ implant. Since the contact area is small enough that the device electrical characteristic would not be affected. A V_I-V_g measured by DC (Agilent 4156) and a fast transient setup is shown in Fig. 3.5. Note that SHE is negligible in the fast transient measurement. A larger internal voltage in non-SHE condition is observed, which implies a stronger hot carrier stress in the channel region. The larger V_I in a non-SHE condition is attributed to a higher mobility in accumulation region, and thus results in a smaller drift region resistance.

Fig. 3.6 shows a temperature distribution in LDMOS. Since the existence of field-oxide, heat could not be easily eliminated. Thus, field oxide region would exhibit a higher temperature distribution. Fig.3.6 also compared the temperature distribution in high Vg and low Vg operation. Since power consumption in high Vg is larger than in low Vg, a higher temperature can be observed. Fig. 3.7 shows the drain current increase versus power consumption. A linear function of power consumption is observed [17,18].

3.3 AC Hot Carrier Stress

Two stress modes (max. I_B, and max. I_g) [16] are chosen in the study of the transient hot carrier degradation. The I_g-V_g and I_B-V_g of a n-LDMOS are shown in Fig. 3.8 and corresponding stress modes are indicated. Fig. 3.9 shows the I_{dlin} degradations in AC and DC stress conditions at the above two stress modes. Max. I_B stress mode shows a slight difference in I_{dlin} degradation between AC and DC stresses, implying that SHE is not important at a lower Vg stress. However, in max. I_g stress mode, AC stress shows more serious I_{dlin} degradation than DC stress. Fig. 3.10(a) shows the I_{dlin} degradation versus stress frequency at max. I_g stress. The I_{dlin} degradation possesses a strong stress frequency dependence. The degradation increases with frequency and then becomes saturated. A corner frequency (f_1=20 KHz) is indicated in Fig. 3.10(a). In addition, the duty cycle dependence of I_{dlin} degradation is shown in Fig. 3.10(b). The I_{dlin} degradation decreases from duty cycle=10% to duty cycle=100% (DC stress).

Fig. 3.11(a) shows a V_I versus voltage pulse time. A SHE time constant is extracted to be around 5μs. We normalized the stress frequency and duty cycle dependence to on-sate stress time (=Duty cycle / frequency) and the correlation of them is shown in Fig. 3.11(b). The above result suggests that SHE becomes important as pulse time is longer than ~5μs.

3.4 Degradation Characteristics in AC/DC Stress

Max. Ig AC and DC stress are investigated in this section. A largest I_{dlin} degradation in AC stress phase is observed in Fig. 3.12 and corresponding I_{cp} result is shown in Fig. 3.13. Two different stress induced oxide degradation mechanisms are indicated; one is the I_{cp1} increase in channel region and the other is V_{FB2} shift in accumulation region. By comparing the pre-stress and post-stress I_{cp}, AC stress shows

more serious I_{cp1} increase and V_{FB2} shift than DC stress one. A two-dimensional device simulation is performed to calculate impact ionization rate with and without SHE (Fig. 3.14). The simulation also confirms that non-SHE condition (Fig. 3.14(b)) has a larger impact ionization rate.

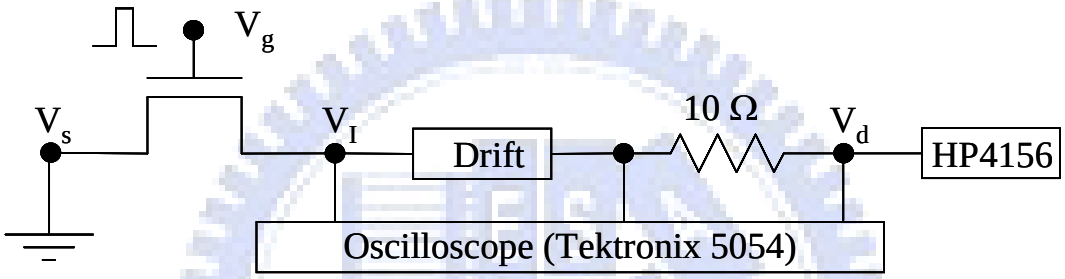


Fig. 3.1 Measurement circuit setup for transient drain current and internal voltage (V_I) measurement. The resistance (10Ω) is smaller than the total resistance (~40V/10mA~4kΩ).

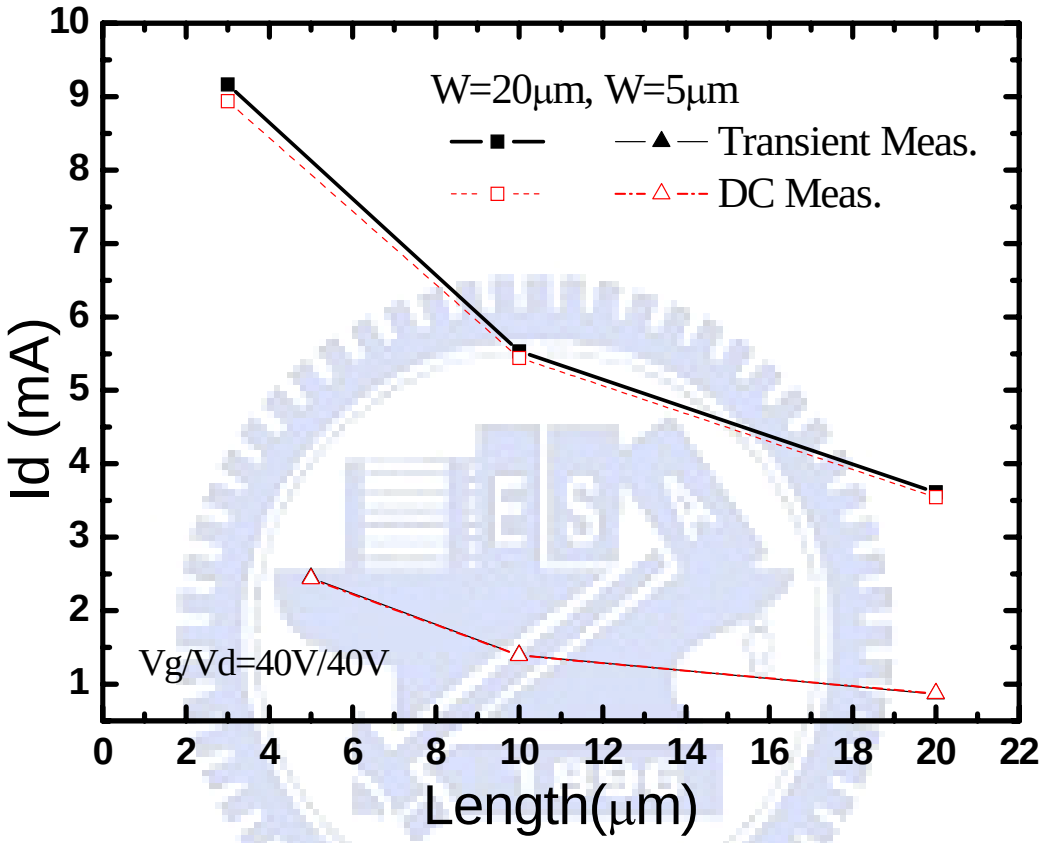


Fig.3.2 Comparison of drain current measured by Agilent 4156 (DC measurement) and an oscilloscope (transient measurement) for different device widths and lengths at Vg/Vd=40/40.

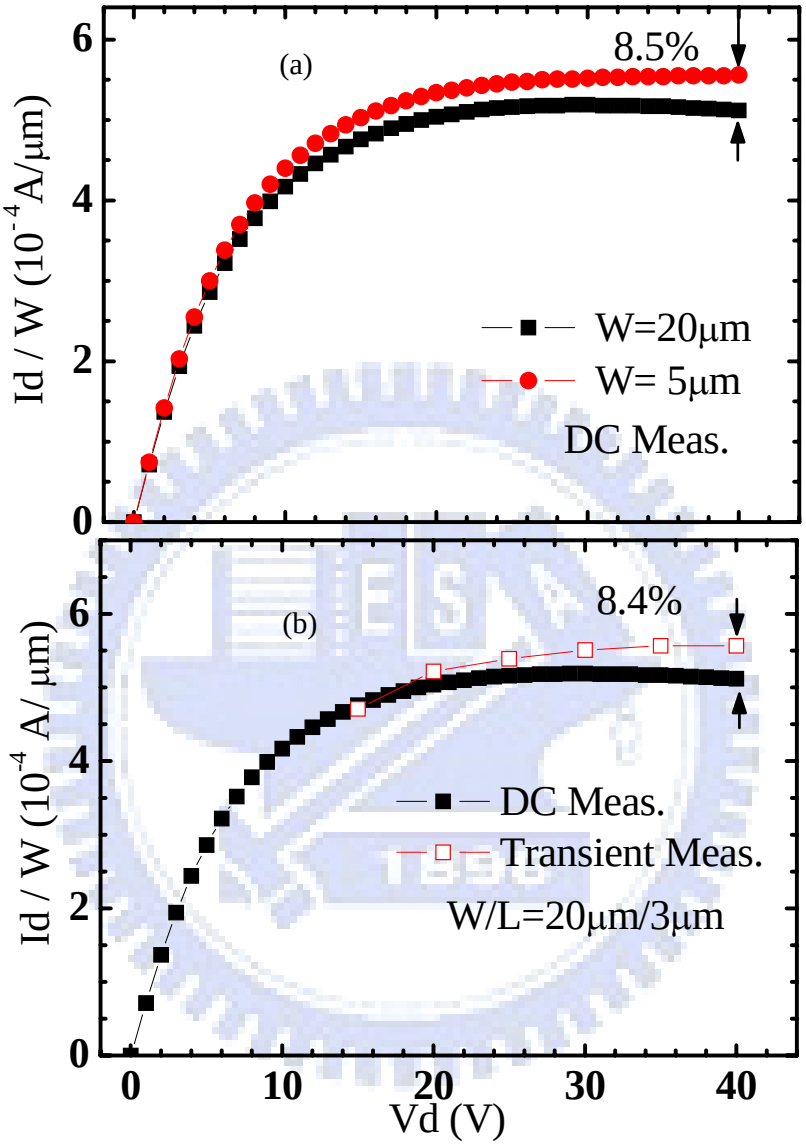


Fig. 3.3 (a) Normalized drain current versus drain voltage by DC measurement for two different gate widths (b) Comparison of normalized drain current versus drain voltage by DC and transient measurements. The measurement Vg is 40V.

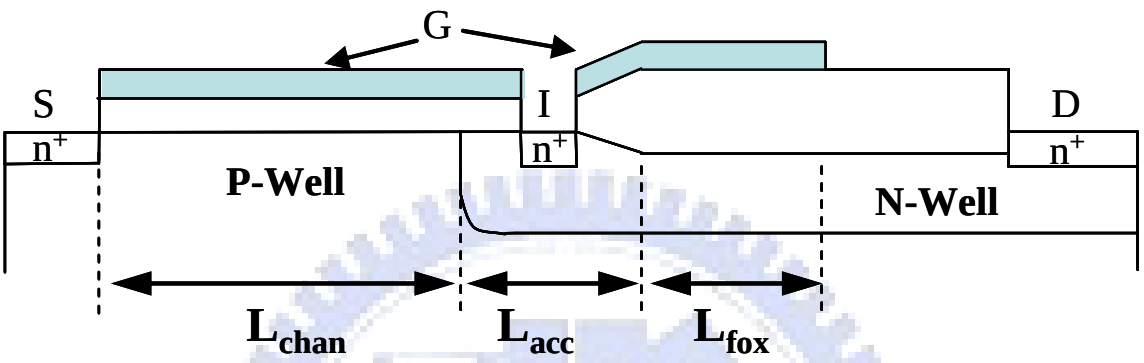


Fig. 3.4 The cross-section of a LDMOS and flat-band voltage distribution in each region. The metal contact (I) is arranged in the bird's beak region with a n+ implant. This metal contact is small enough that width it would not affect the electrical characteristics of a LDMOS.

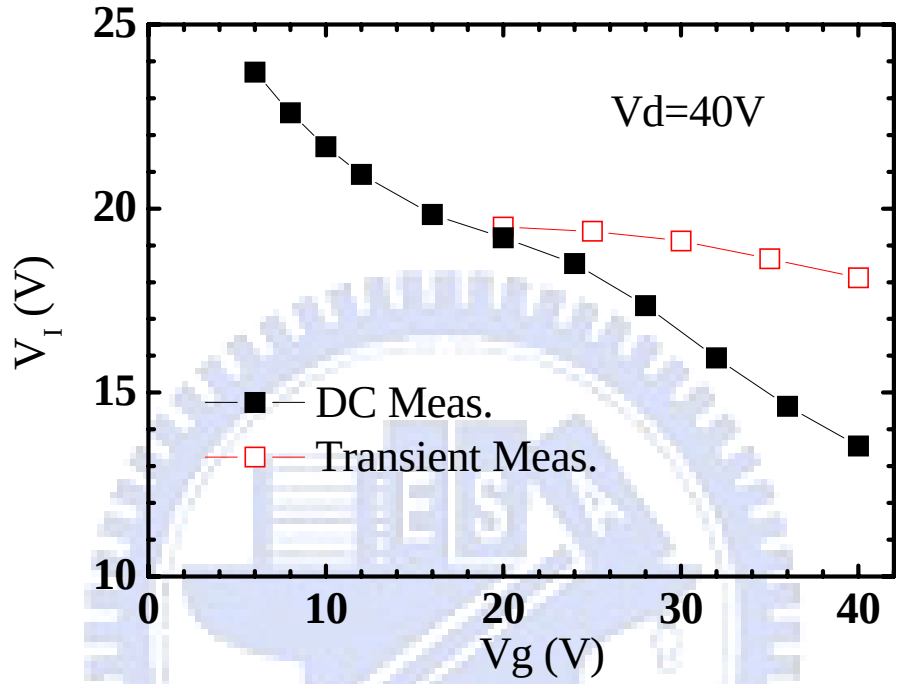


Fig.3.5 Internal voltage versus gate voltage in a LDMOS. An increase in an internal voltage is observed in the transient measurement.

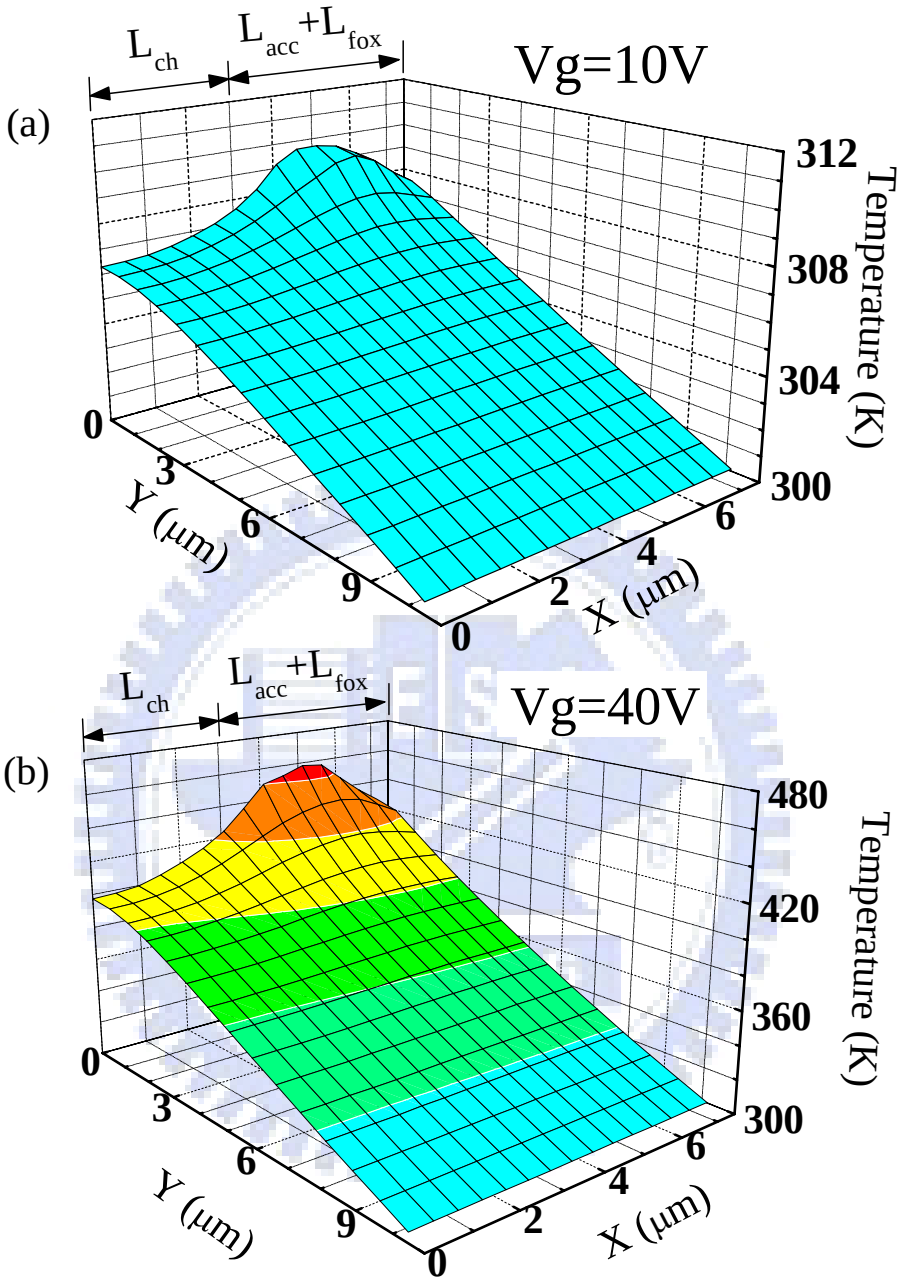


Fig.3.6 Simulation of temperature distribution in a LDMOS for (a) Vg=10V and (b) Vg=40V.

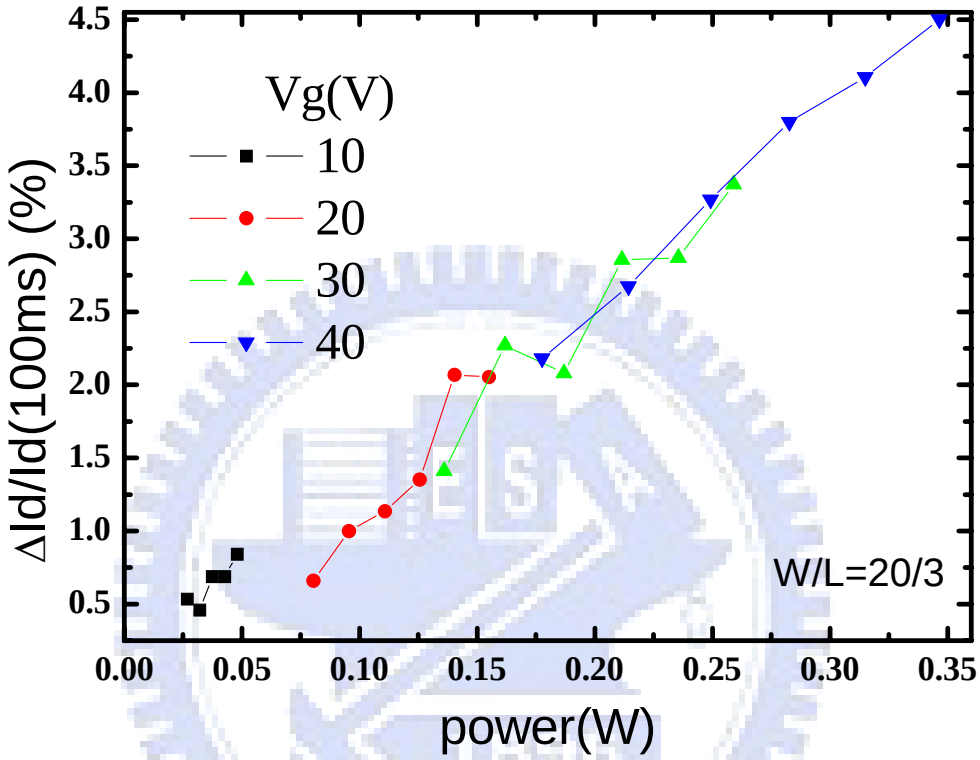


Fig. 3.7 Power consumption versus Id degradation.

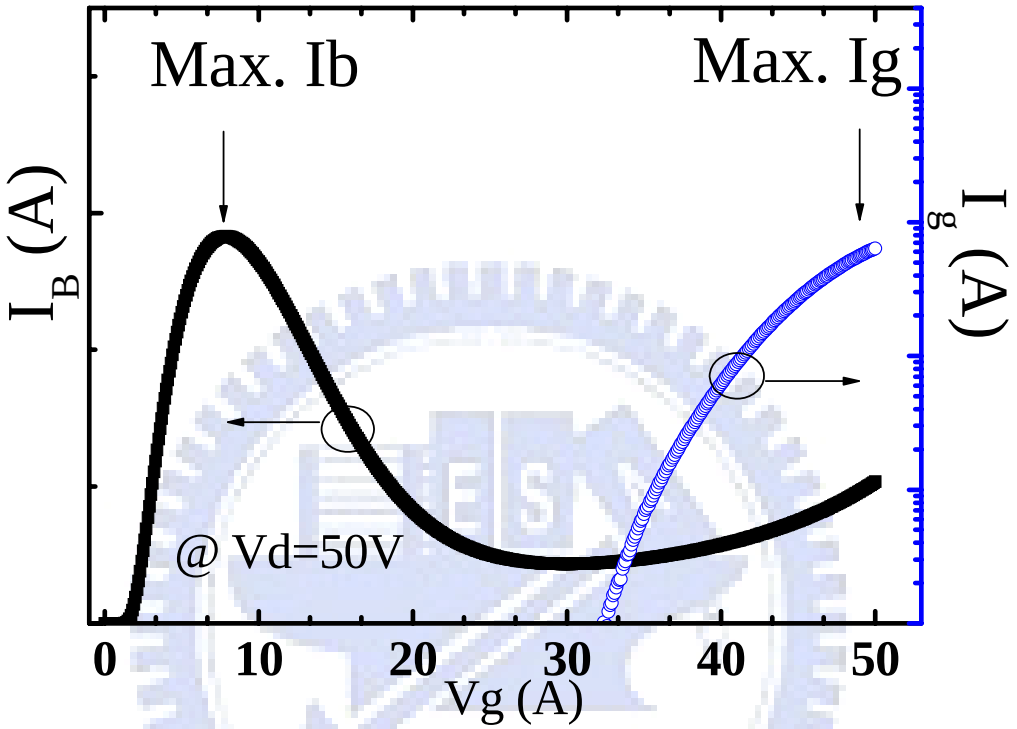


Fig. 3.8 Substrate current and gate current versus gate voltage in a LDMOS.

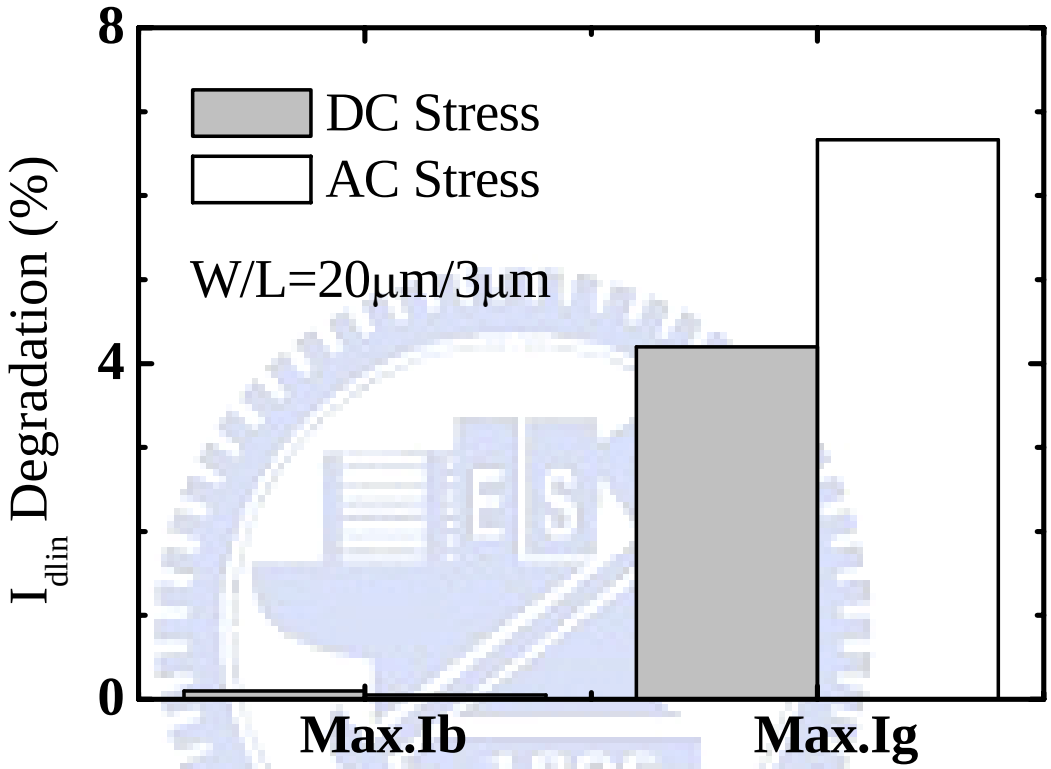


Fig.3.9 I_{dlin} degradations in AC and DC stress conditions in max. Ib and max. Ig stress modes.

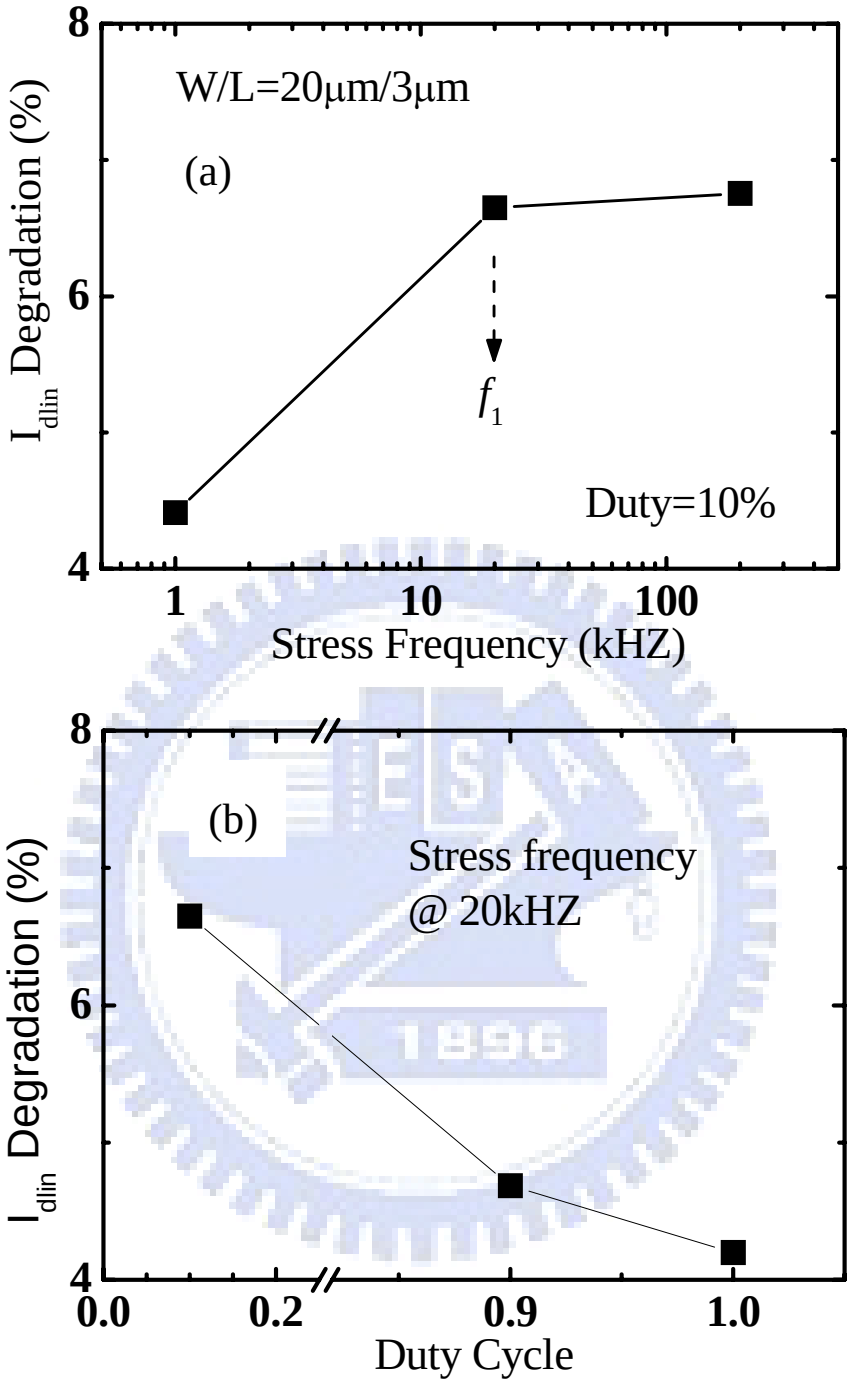


Fig. 3.10 (a) Idlin degradation versus stress frequency. A transition frequency is observed around f_1=20kHz. (b)Idlin degradation versus duty cycle.

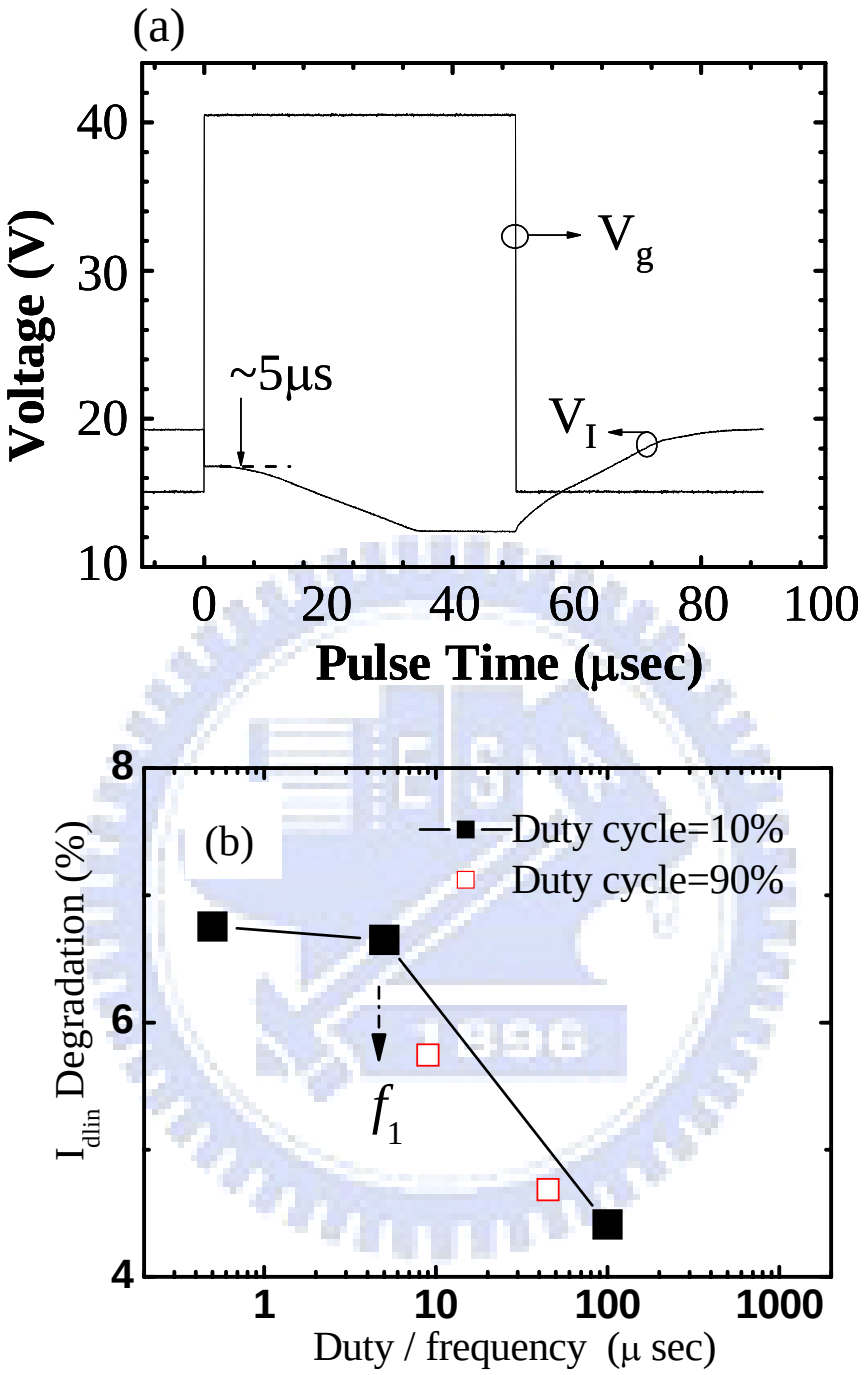


Fig. 3.11 (a) The transient of an internal voltage (V_I) for a gate pulse of 50μs with Vg/Vd=40V/40V. A decreasing V_I is observed after a heating time around 5μs.
(b) I_{dlin} degradation versus on-state pulse time (=duty cycle/frequency). The transition frequency (f_1) in Fig. 3.10(a) is also indicated in the figure, which corresponds to an on-state pulse time of 5μs.

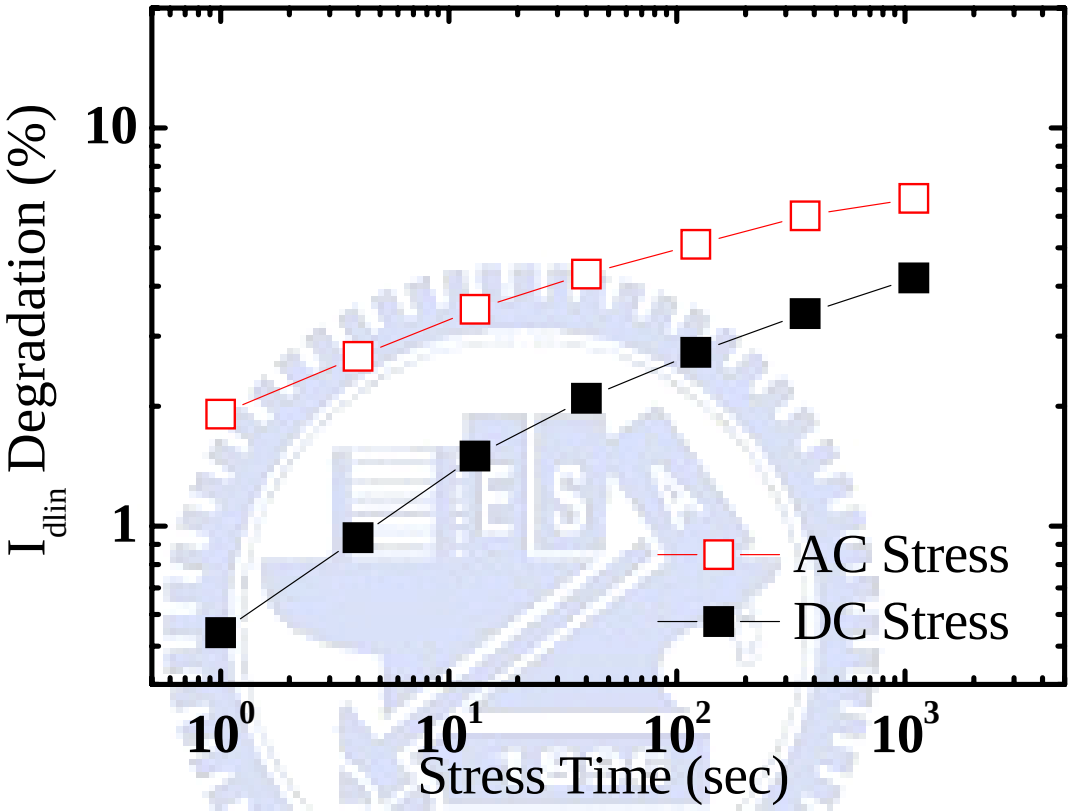


Fig. 3.12 I_{dlin} degradation rate after max. Ig AC and DC stress. The stress frequency =20kHz and duty cycle=0.1.

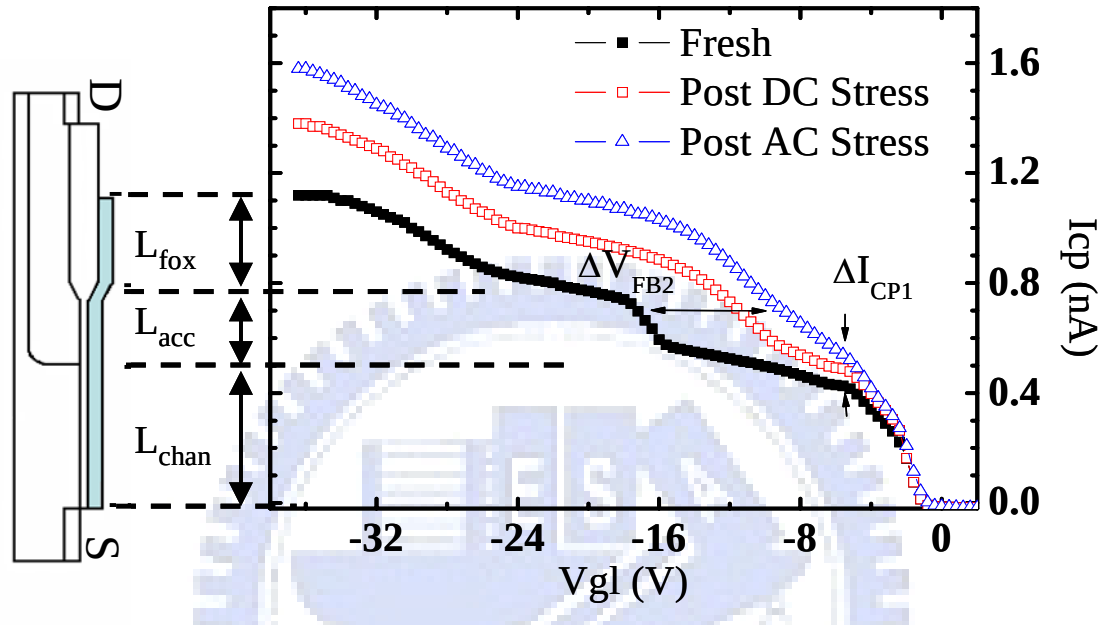


Fig.3.13 Threes region charge pumping measurement results after maximum Ig AC stress and maximum Ig DC stress. A flat-band voltage shift and an increased I_{CP} are observed in accumulation region and in channel region, respectively.

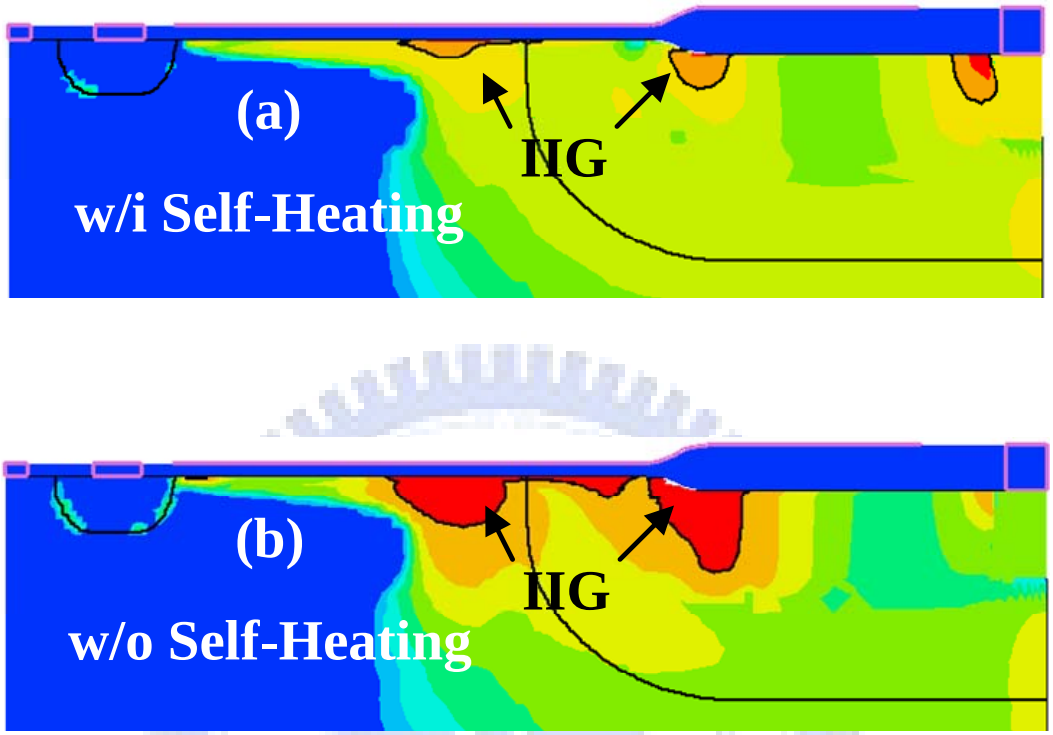


Fig. 3.14 Two-dimensional device simulation of impact ionization generation (IIG) distribution (a) with heat flow analysis (corresponding to max. Ig DC stress mode) and (b) without heat flow analysis (corresponding to max. Ig AC stress mode). A larger IIG region is observed in both channel region and drift region.

Chapter 4
Conclusions

In Chapter 2, a three-region CP technique has been developed to characterize hot carrier stress induced oxide degradation in each region of a LDMOS. The trap location and property in various stress modes are identified and their impact on device characteristics has been evaluated. Our study reveals that the device subthreshold swing degradation is mainly affected by interface traps in the channel region while the linear drain current degradation is dictated by oxide trapped charge in the drift region. Low-frequency noise characterization is also performed to investigate the hot carrier stress effects. Our study shows that the low Vg and high Vg flicker noise are affected by channel region and drift region, respectively. In addition, max. I_g stress results in the worst hot carrier degradation in a LDMOS, which is attributed to both N_{it} generation in the channel region and Q_{ox} generation in the bird's beak region.

In Chapter 3, the characterization of self-heating effect has been investigated. Self-heating effect on transient hot carrier behavior has been studied by measuring the internal voltage. The self-heating time (~5μs) is extracted. The max. I_g AC stress has the worst hot carrier degradation due to the elimination of self-heating effect. The charge pumping result shows that hot carrier degradations can be characterized by I_{cp1} increase (Nit generation) in the channel region and V_{FB2} shift (oxide charge creation) in the accumulation region.

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碩士論文題目:

利用特殊接觸電極研究橫向擴散元件之
自發熱效應與可靠度

Investigation of Self-Heating and Reliability Issues in Lateral DMOS by Using an Additional Metal Contact Structure