

(a)



(b)

Figure 1.1.3 The schematic plots of (a) pentacene molecular and (b) single crystal pentacene.

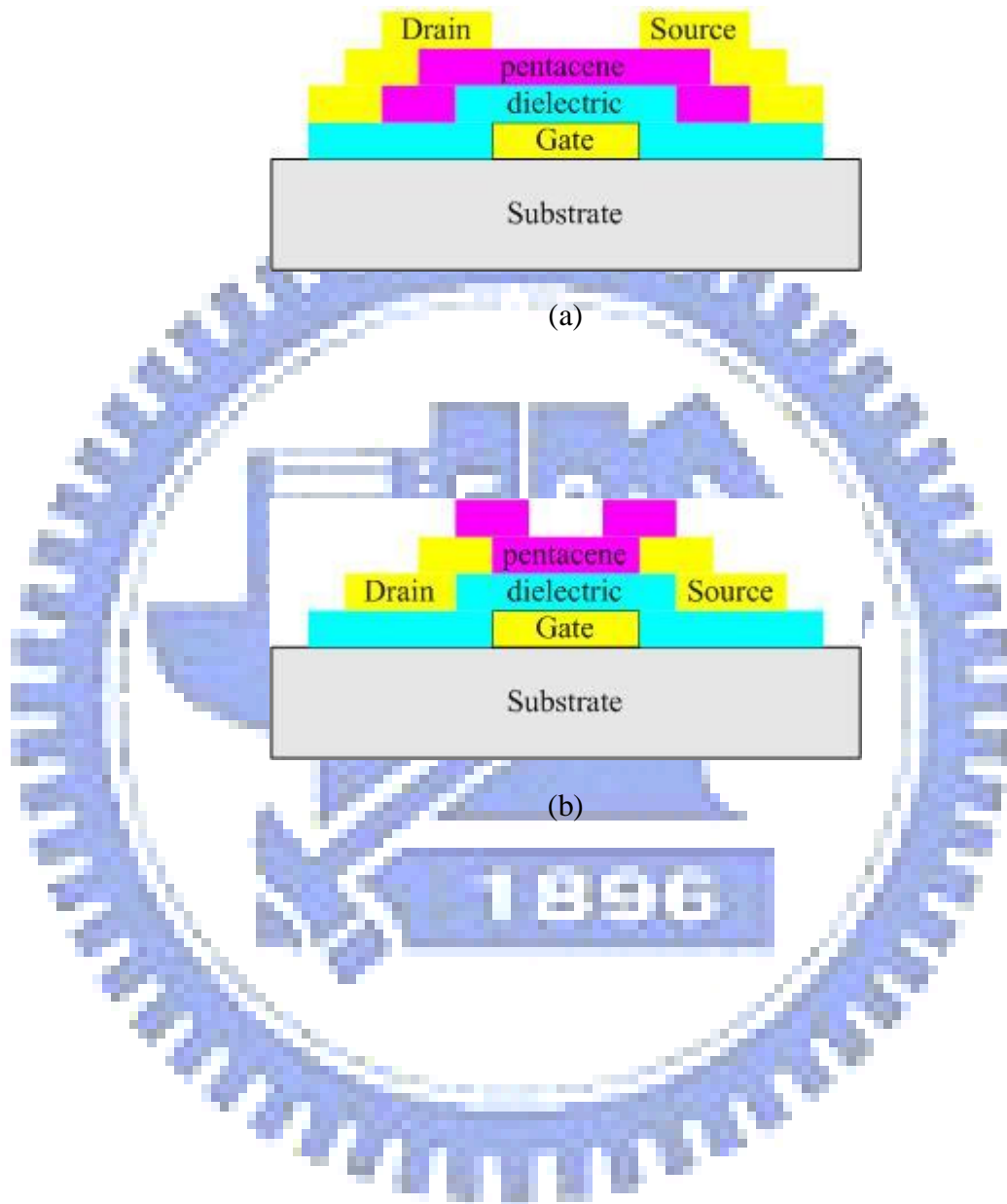


Figure 1.1.4-1 The schematic configurations of (a) top contact and (b) bottom contact pentacene TFTs structure with bottom gate.

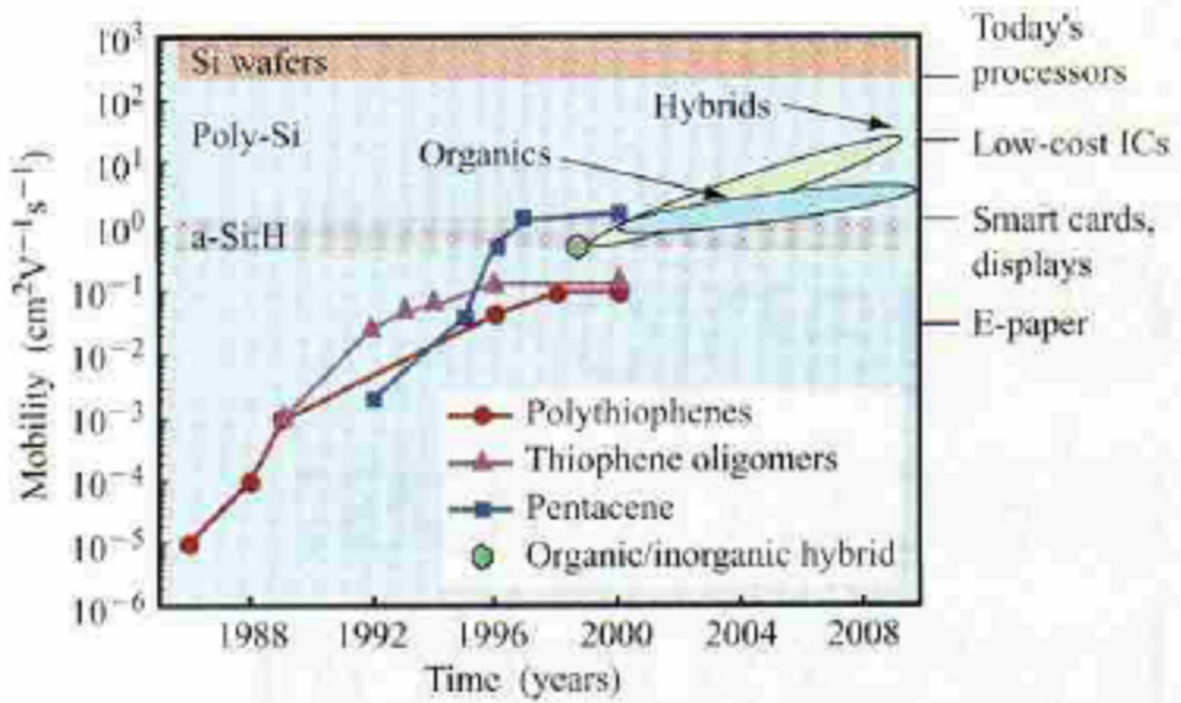


Figure 1.1.4-2 Performance of organic and hybrid semiconductor.[1.22]

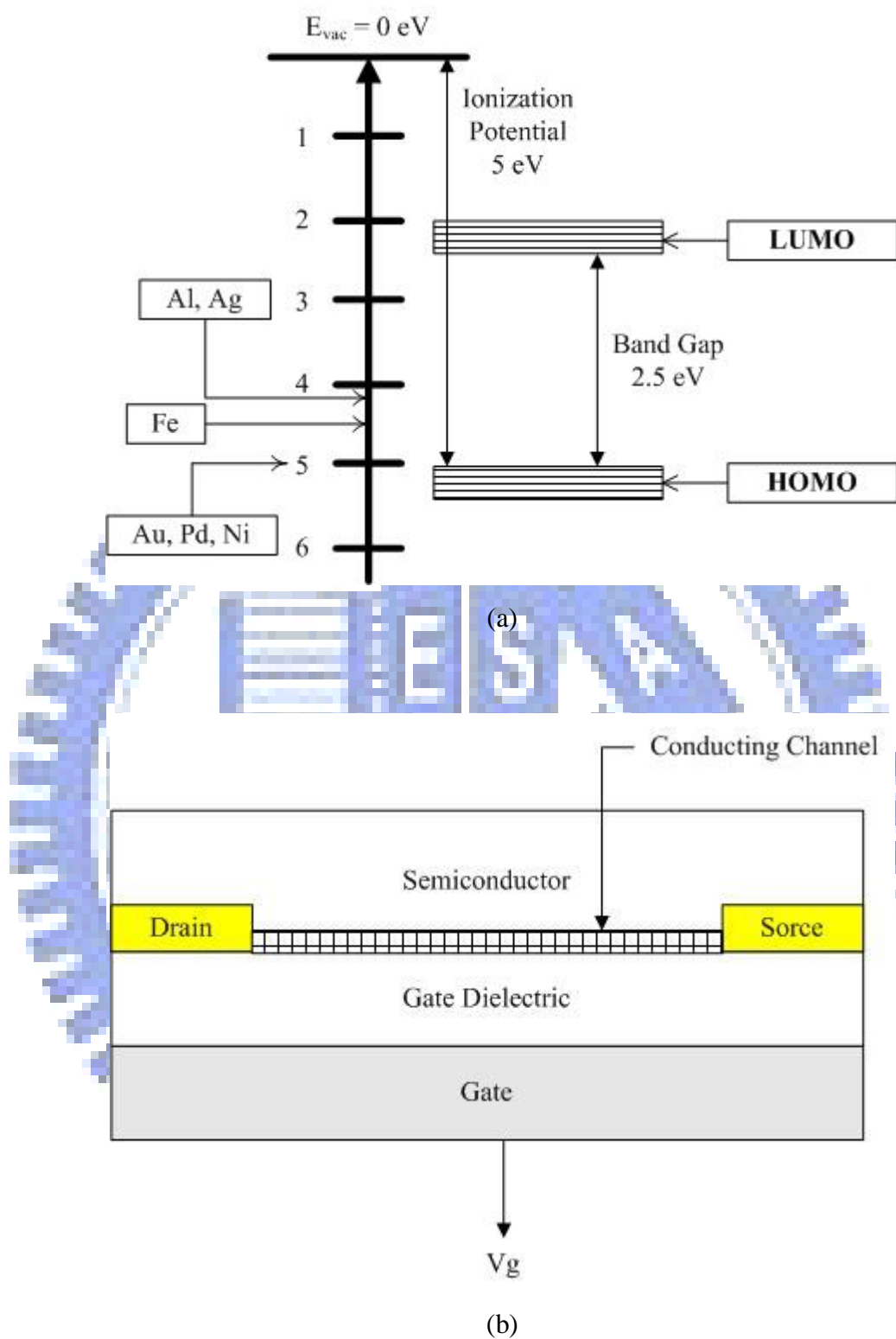


Figure 1.2.1-1 The schematic plots of (a) the Fermi level of electrodes and HOMO-LUMO levels of pentacene and (b) conducting channel formation proportional to the gate voltage.

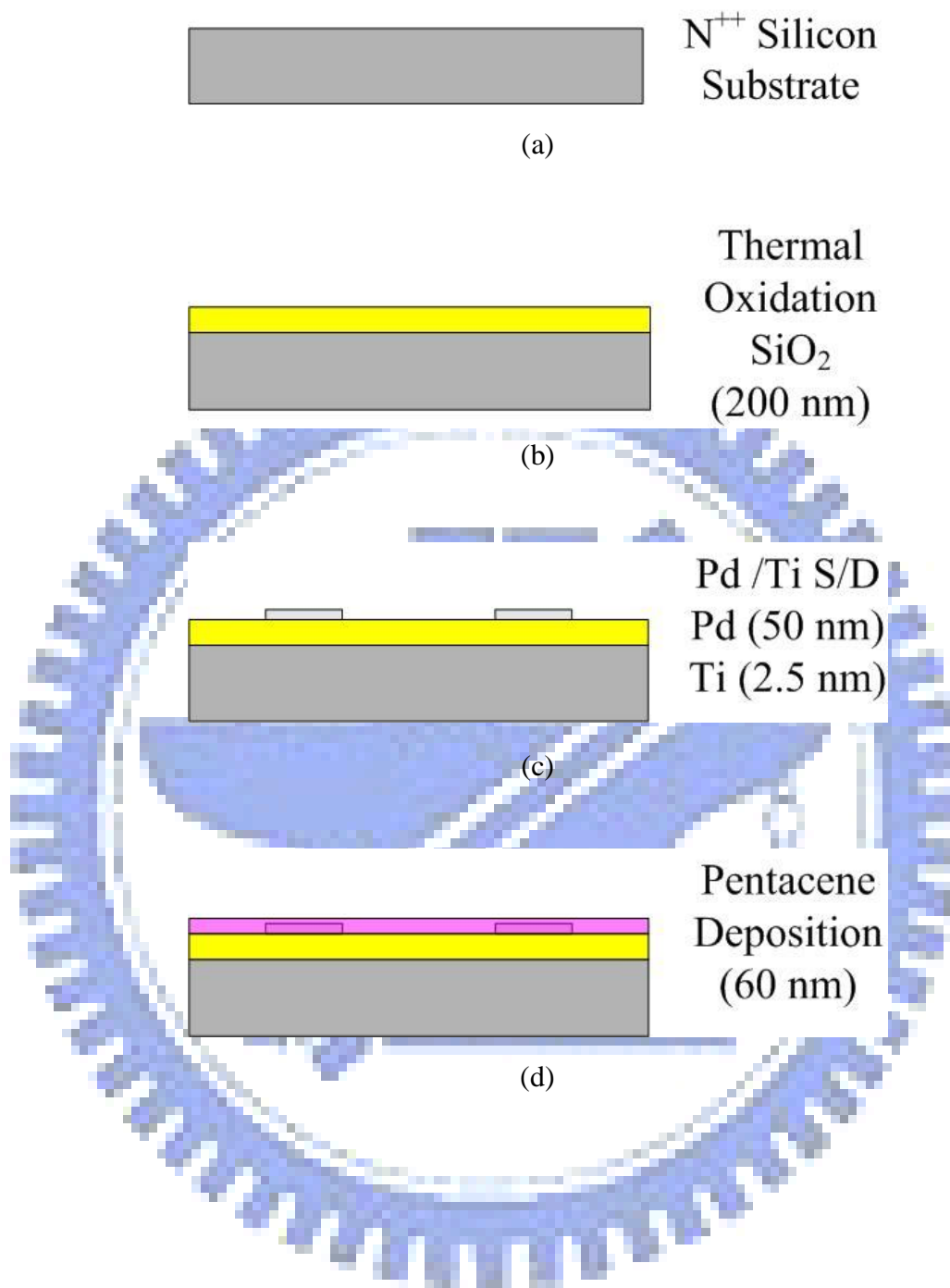


Figure 2.3-1 The Fabrication Procedures of Pentacene TFTs.

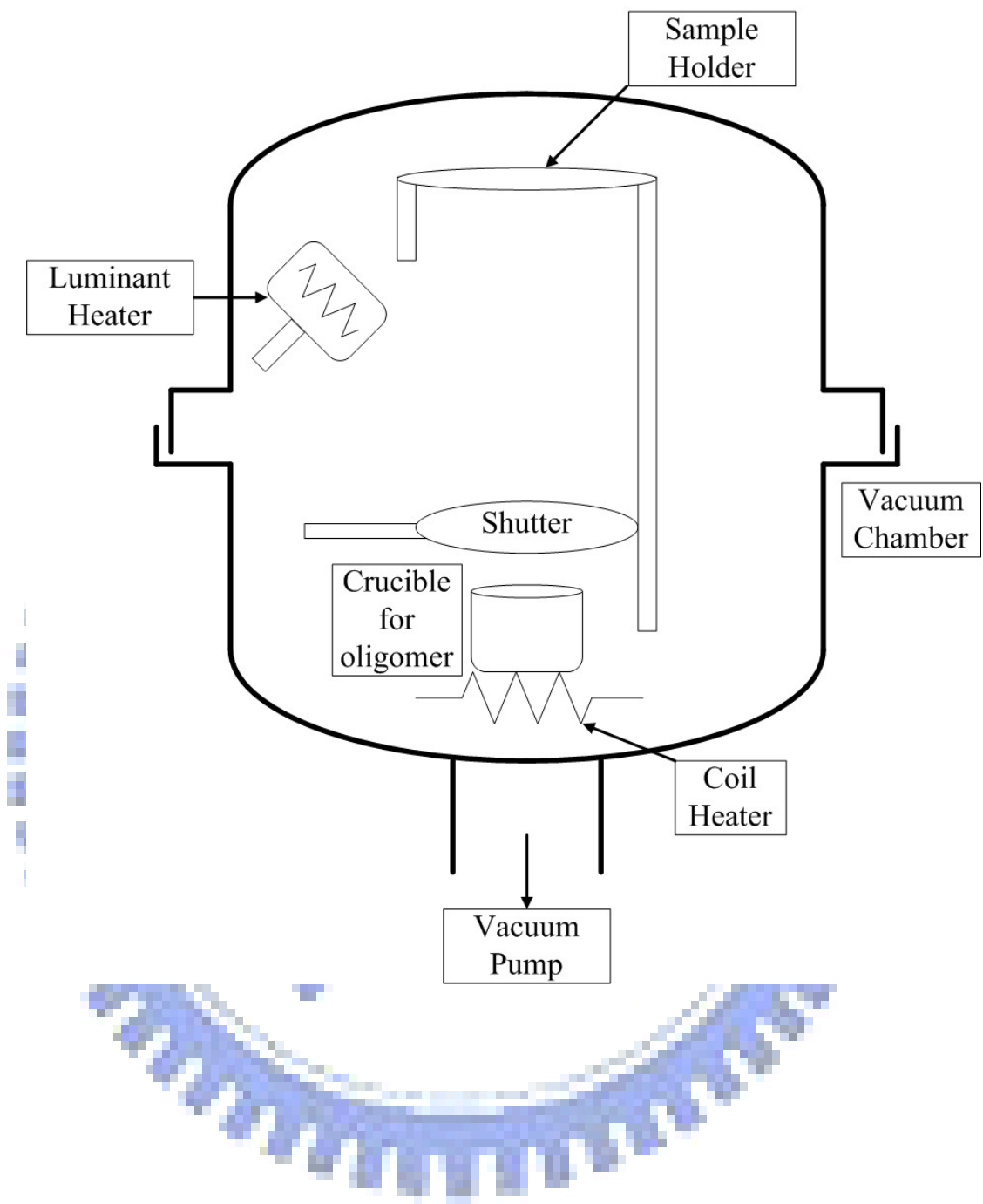


Figure 2.3-2 A schema of chamber of thermal evaporator

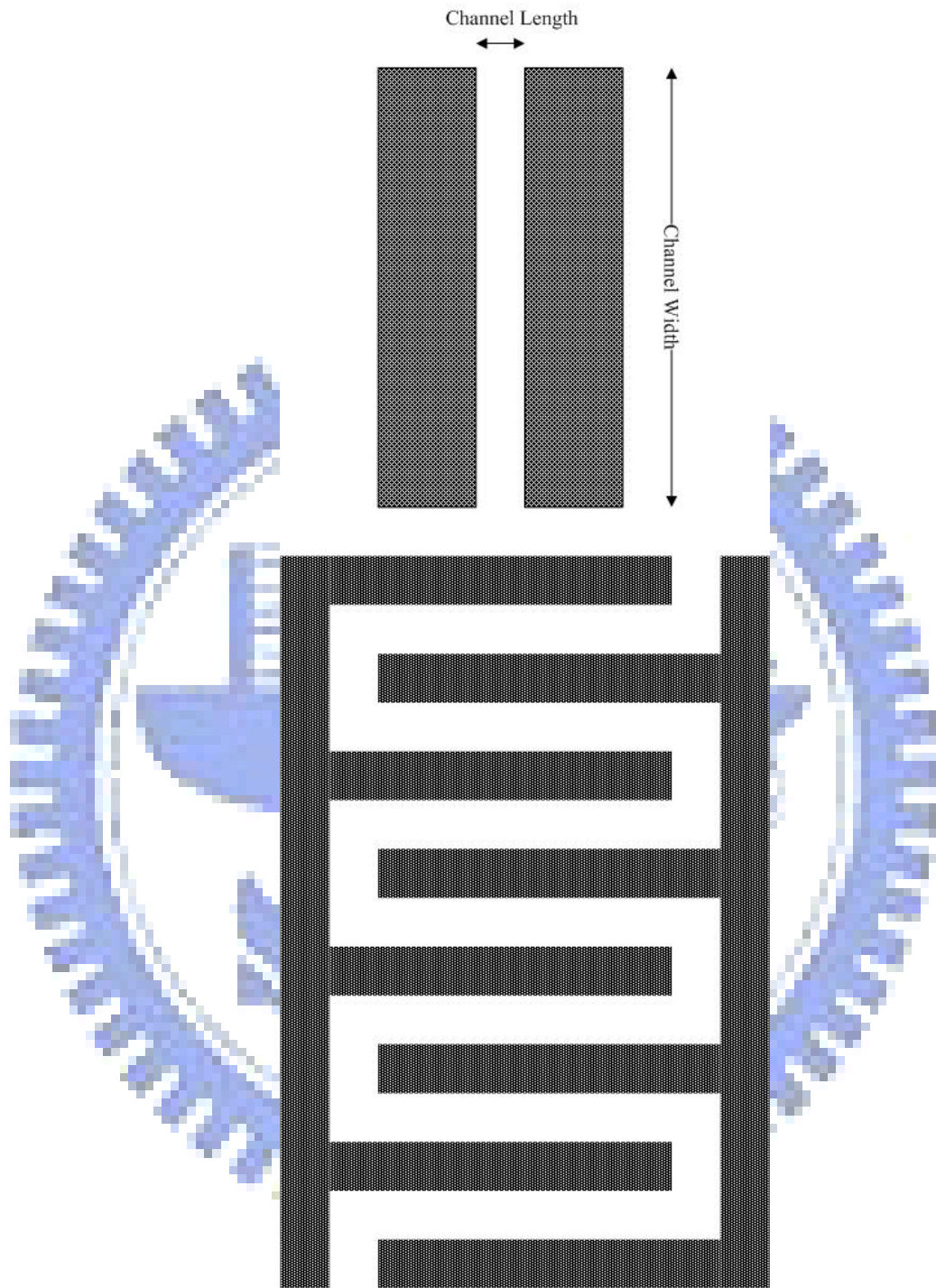
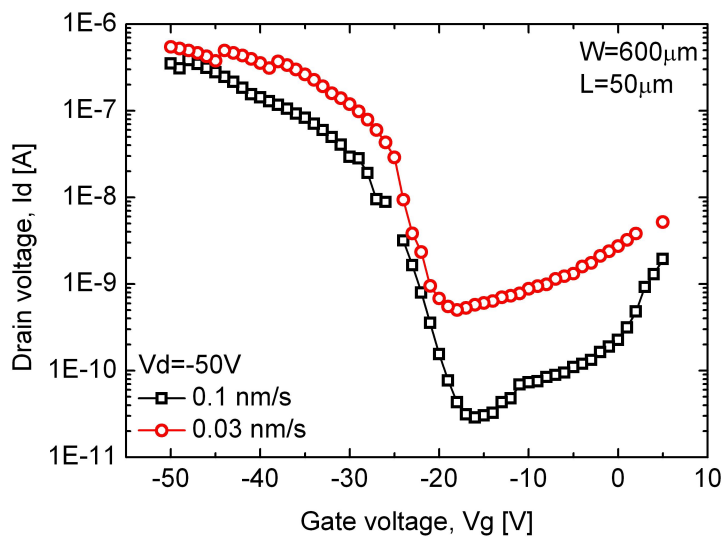
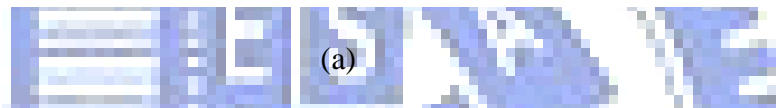
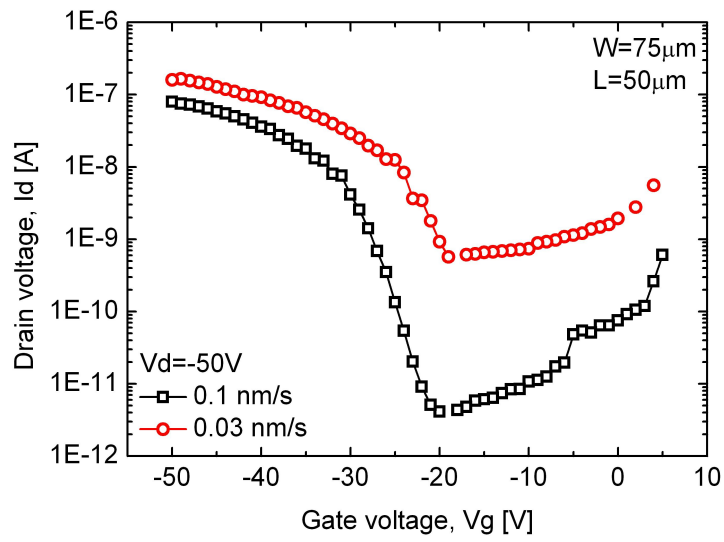
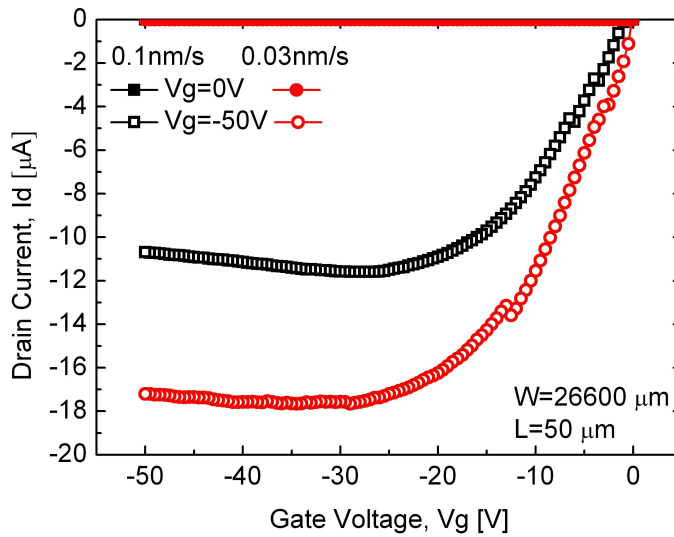
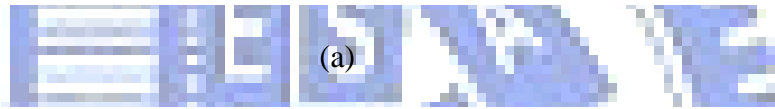
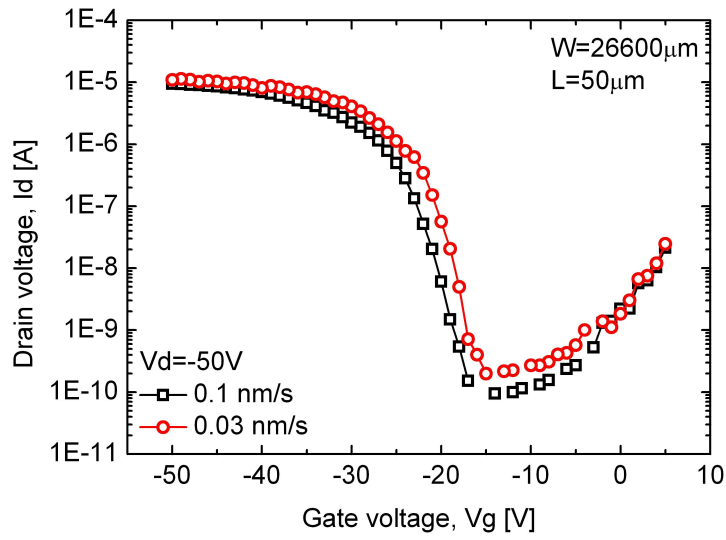


Figure 2.3-3 The schematic plots of linear like and finger type layout for bottom contact OTFTs.



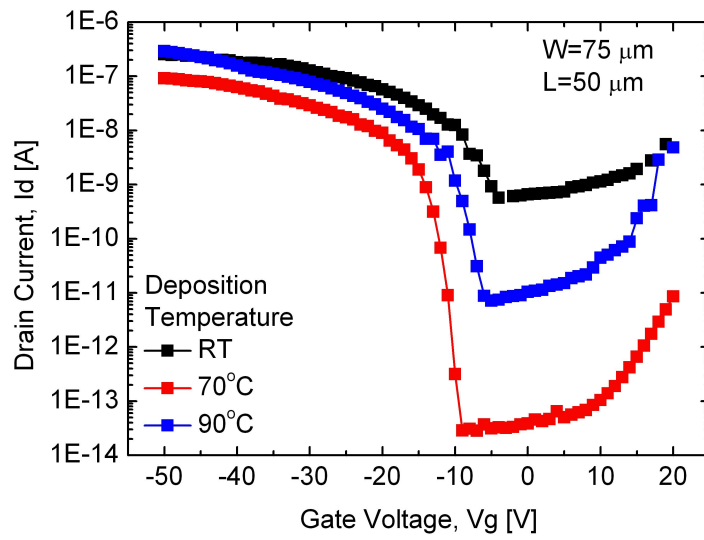
(b)

Figure 2.3.1-1 The I_d - V_g electrical characteristics of pentacene TFTs with different deposition rates. The channel width/length of devices are (a) 75/50 $\mu\text{m}/\mu\text{m}$ and (b) 600/50 $\mu\text{m}/\mu\text{m}$.

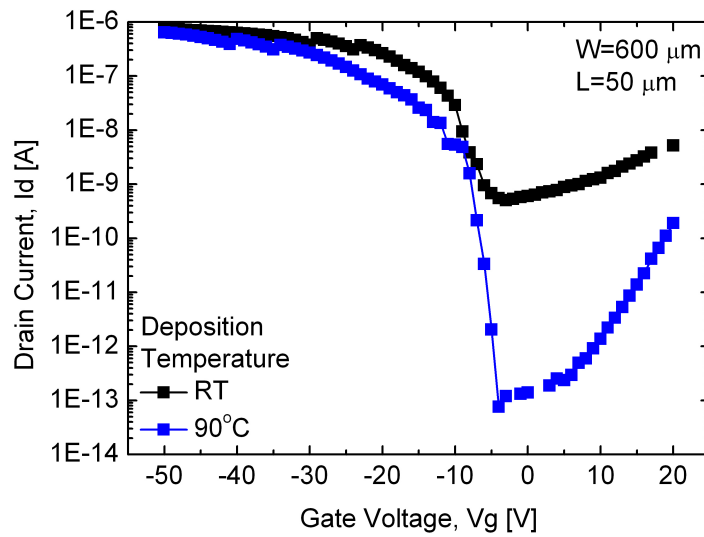


(b)

Figure 2.3.1-2 The (a) I_d - V_g and (b) I_d - V_d electrical characteristics of pentacene TFTs with different deposition rates. The channel width/length of devices are 26600/50 $\mu\text{m}/\mu\text{m}$.



(a)



(b)

Figure 2.3.1-3 The I_d - V_g electrical characteristics of pentacene TFTs with different deposition temperatures. The channel width/length of devices are (a) 75/50 $\mu\text{m}/\mu\text{m}$ and (b) 600/50 $\mu\text{m}/\mu\text{m}$.

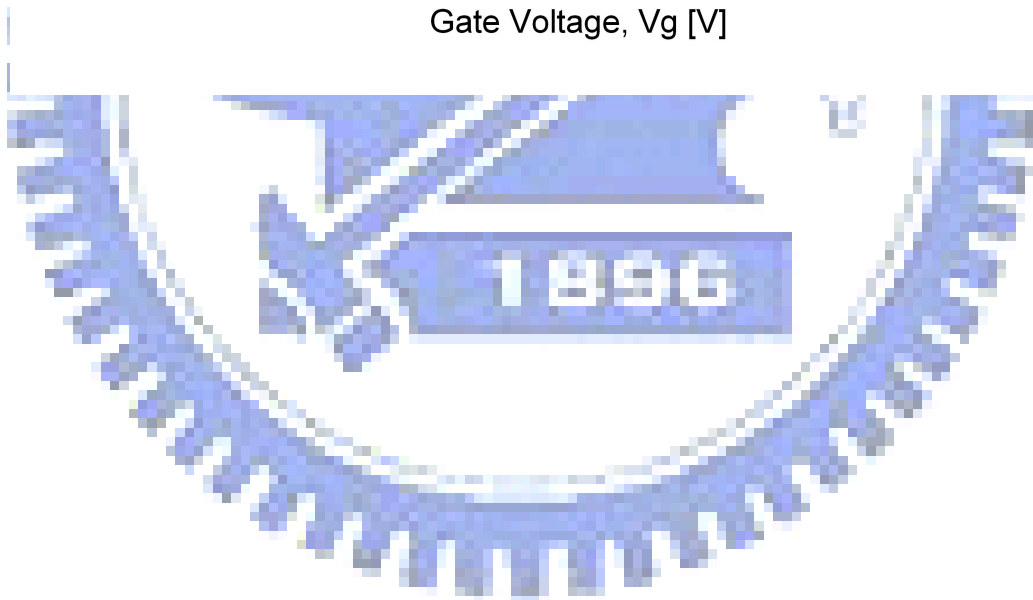
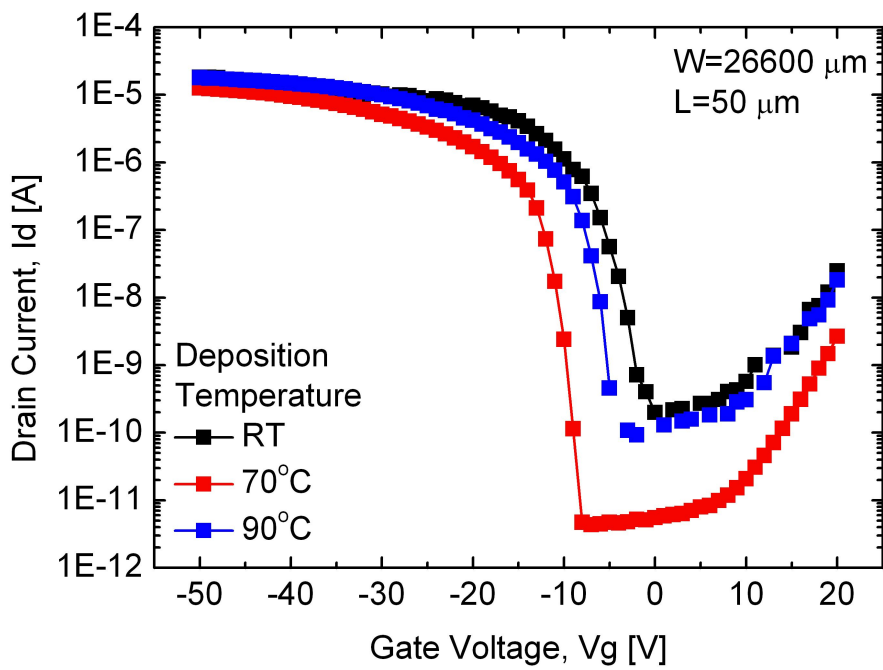


Figure 2.3.1-4 The I_d - V_g electrical characteristics of pentacene TFTs with different deposition temperatures. The channel width/length of devices are 26600/50 $\mu\text{m}/\mu\text{m}$.

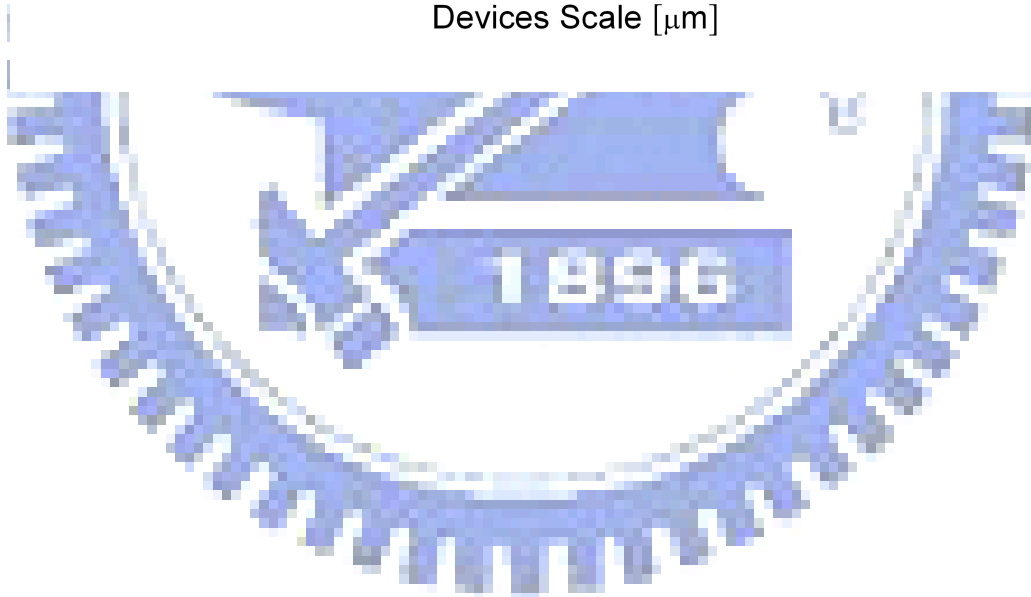
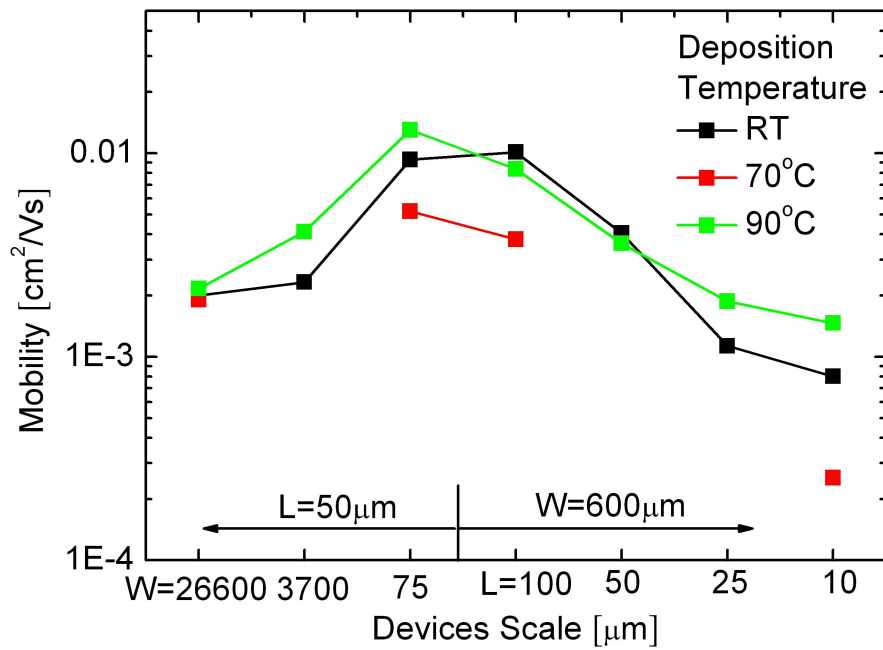


Figure 2.3.1-5 The extractions of saturation mobility of pentacene TFTs with different deposition temperatures and different device scales

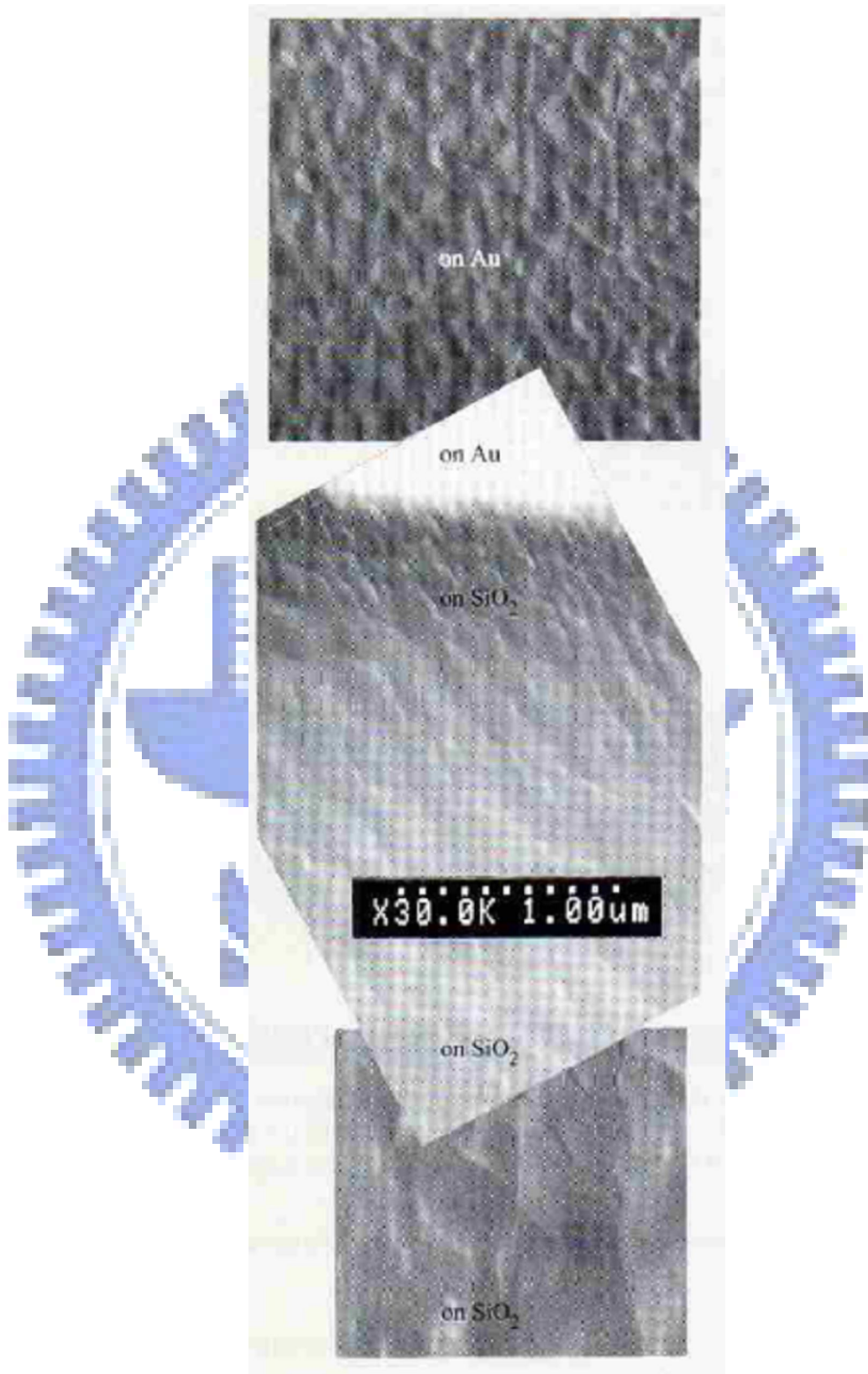
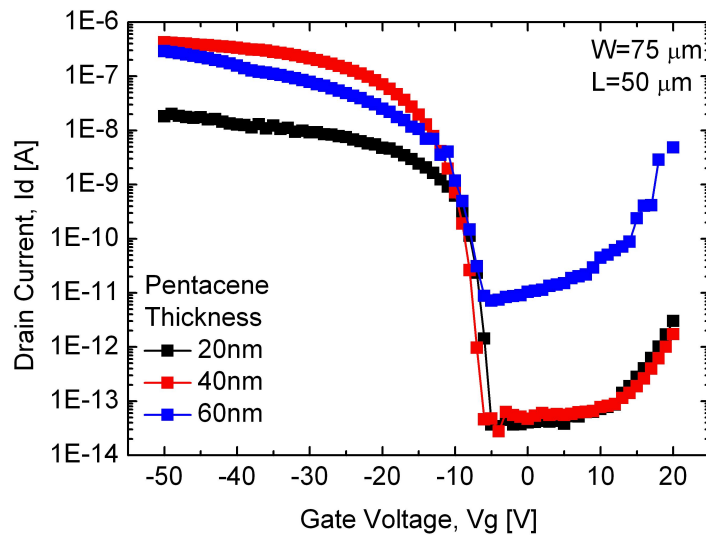
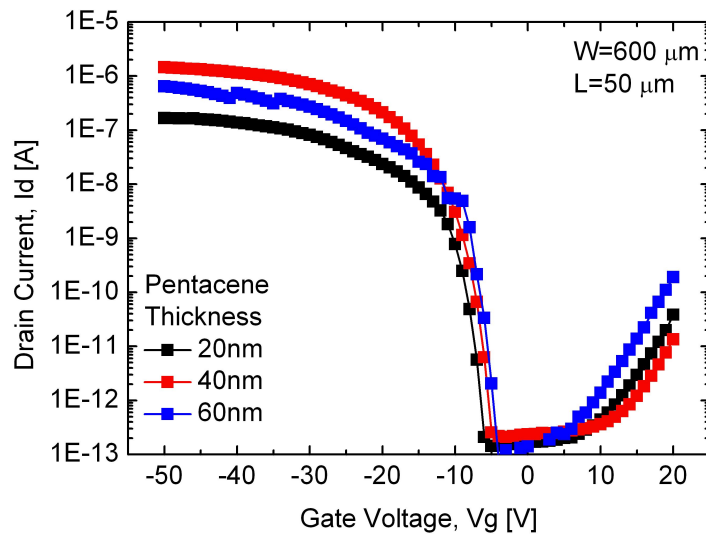


Figure 2.3.1-6 The SEM images of surface morphologies of pentacene active layer deposited on gate dielectric and contact metal.[1.1]



(a)



(b)

Figure 2.3.2-1 The I_d - V_g electrical characteristics of pentacene TFTs with different pentacene thicknesses. The channel width/length of devices are (a) $75/50\ \mu\text{m}/\mu\text{m}$ and (b) $600/50\ \mu\text{m}/\mu\text{m}$.

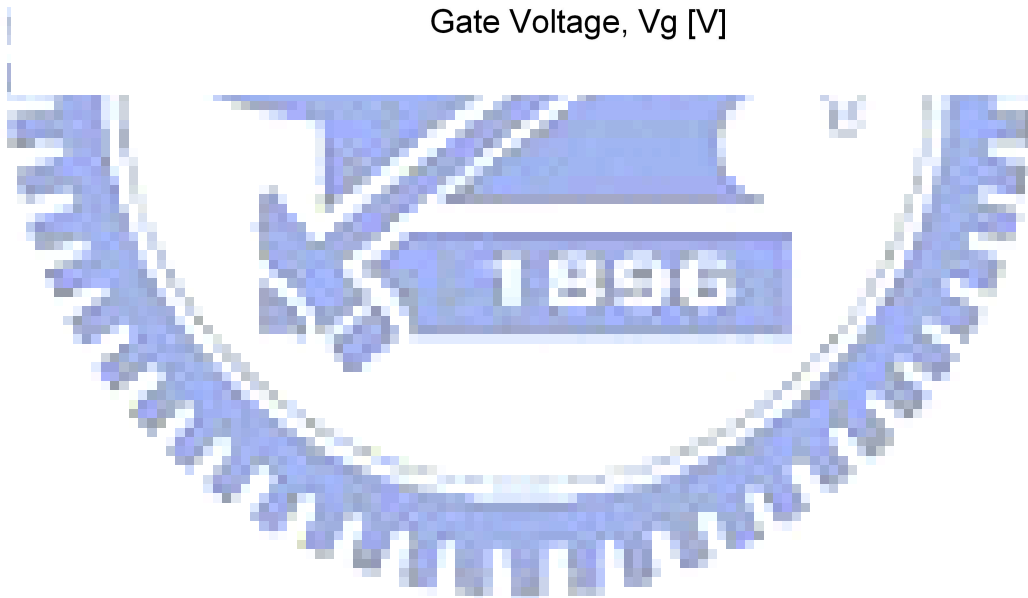
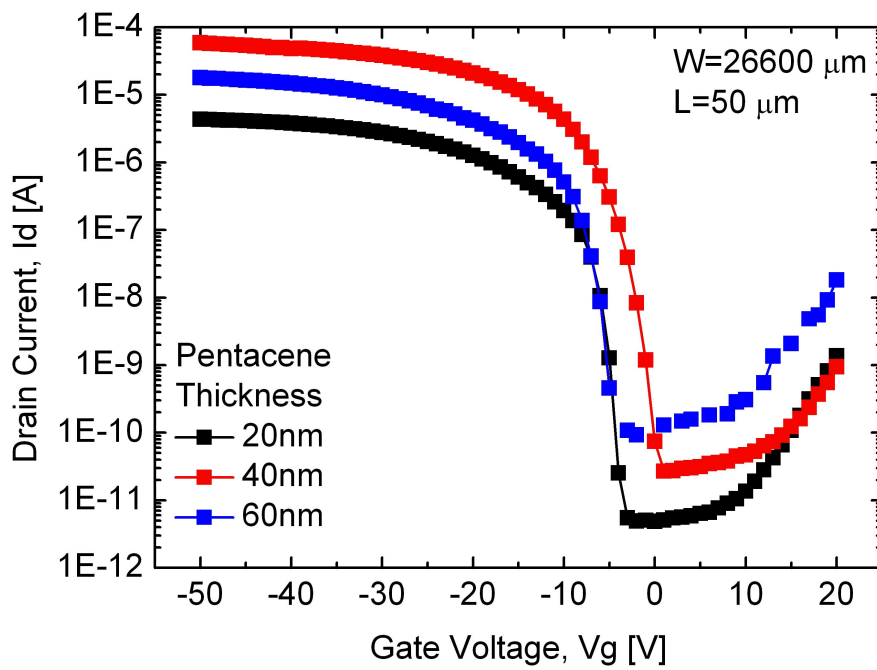


Figure 2.3.1-2 The I_d - V_g electrical characteristics of pentacene TFTs with different pentacene thicknesses. The channel width/length of devices are 26600/50 $\mu\text{m}/\mu\text{m}$.

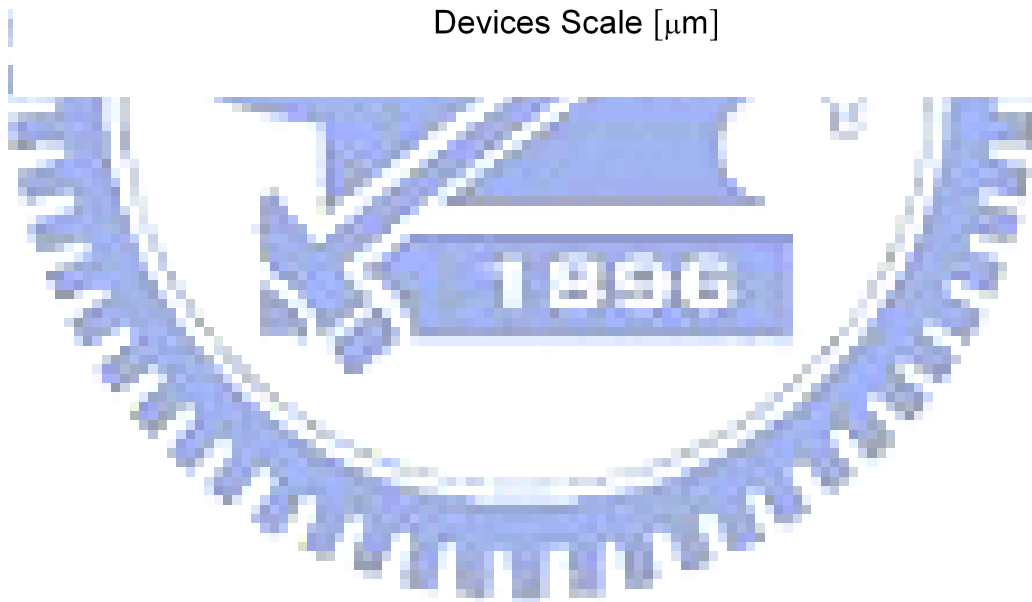
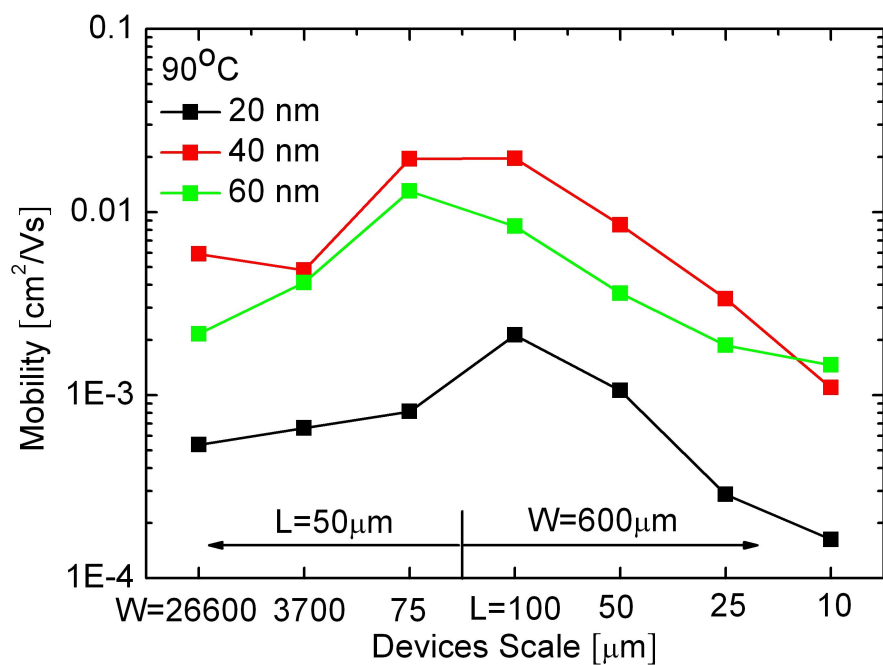
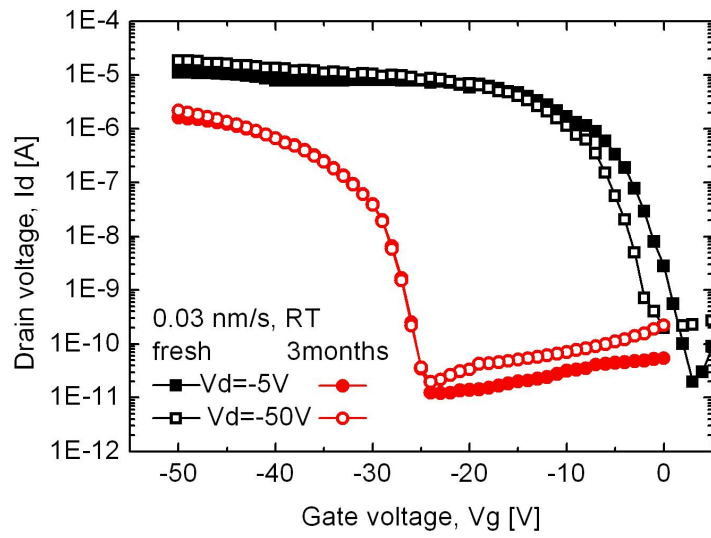
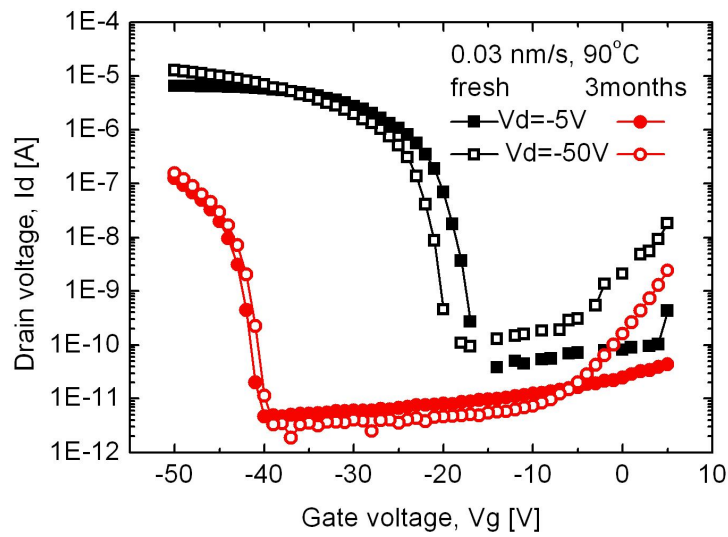


Figure 2.3.2-3 The mobility extractions of pentacene TFTs with different device scales and varied thickness of pentacene film.

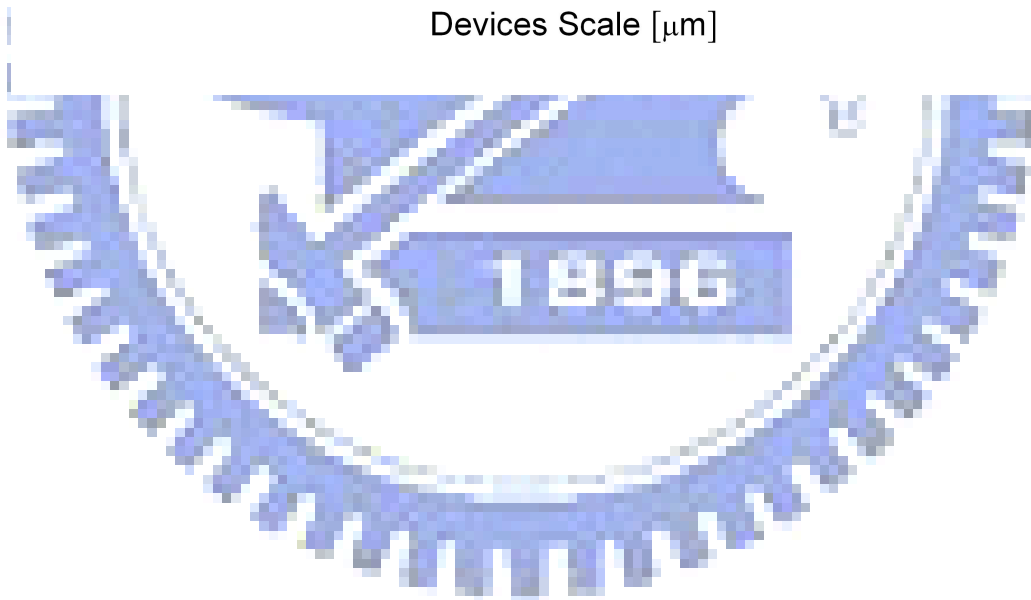
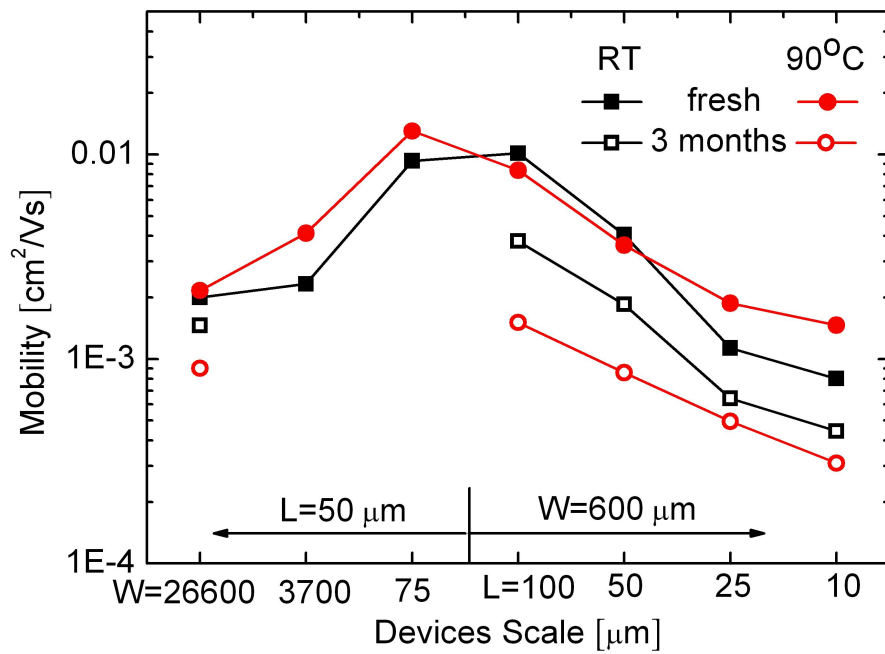


(a)



(b)

Figure 2.3.3-1 The degradation on electrical characteristics of pentacene TFTs with different deposition temperatures which are (a) RT and (b) 90 °C. The channel width/length of devices are 26600/50 $\mu\text{m}/\mu\text{m}$.



Figures 2.3.3-2 The degradation on mobility of pentacene TFTs with different pentacene deposition temperatures and device scales.