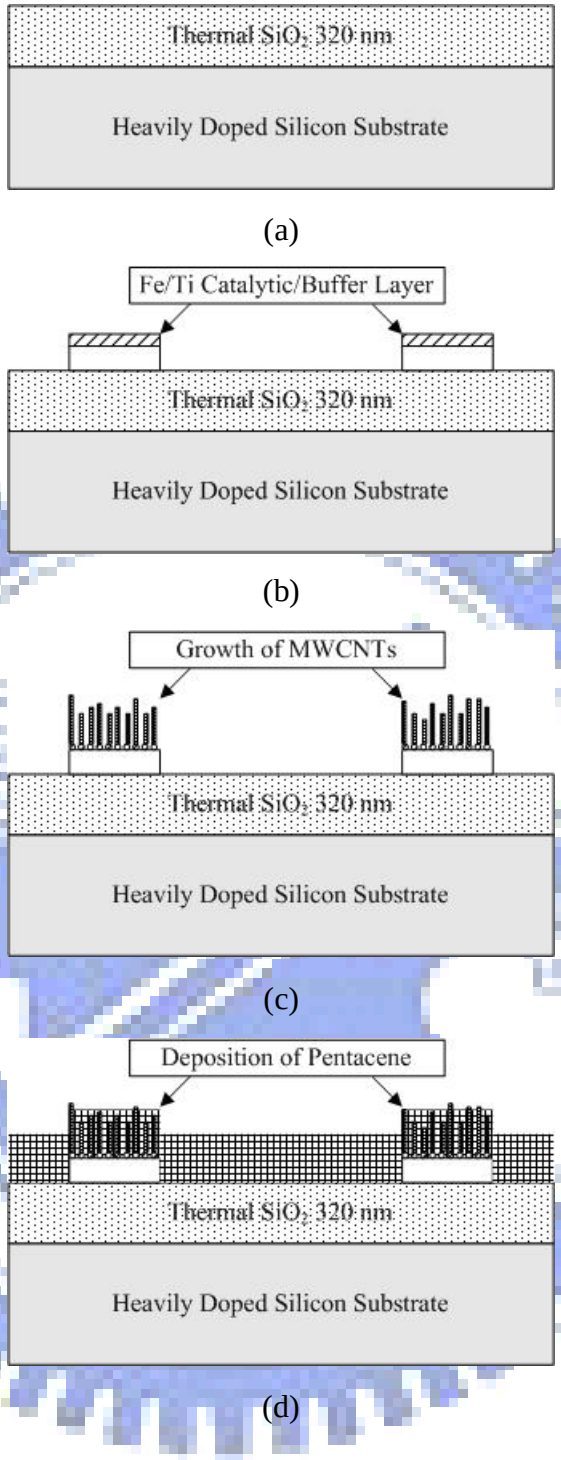


Figure 4.3-1 The schematic cross-section plots of fabrication procedure of a BC pentacene TFT possessing an MWCNT S/D.

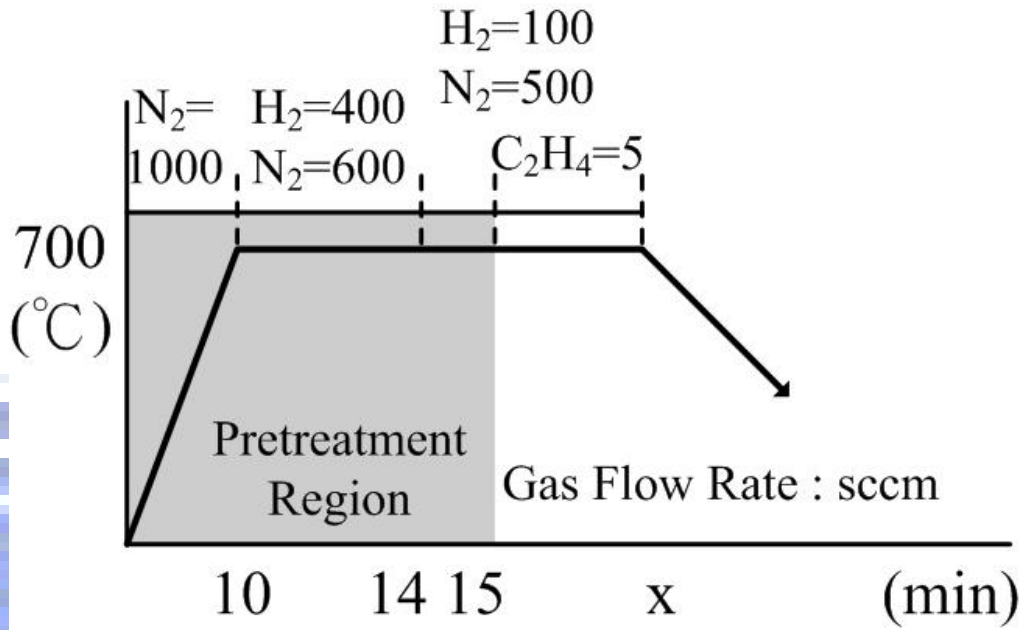
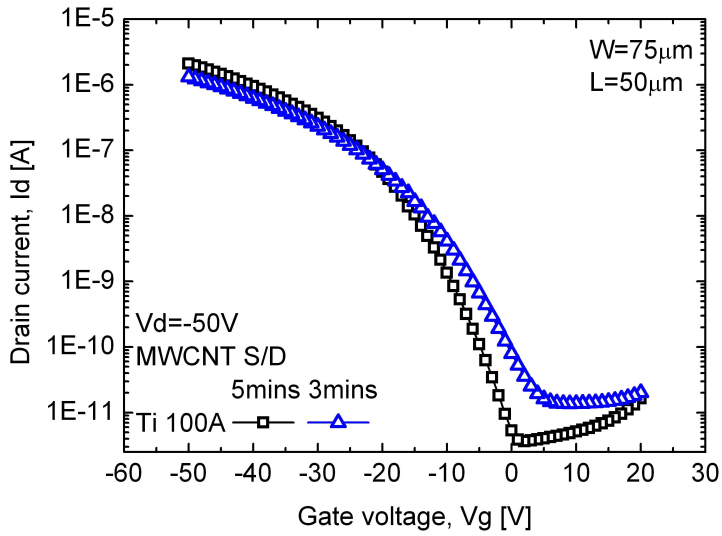
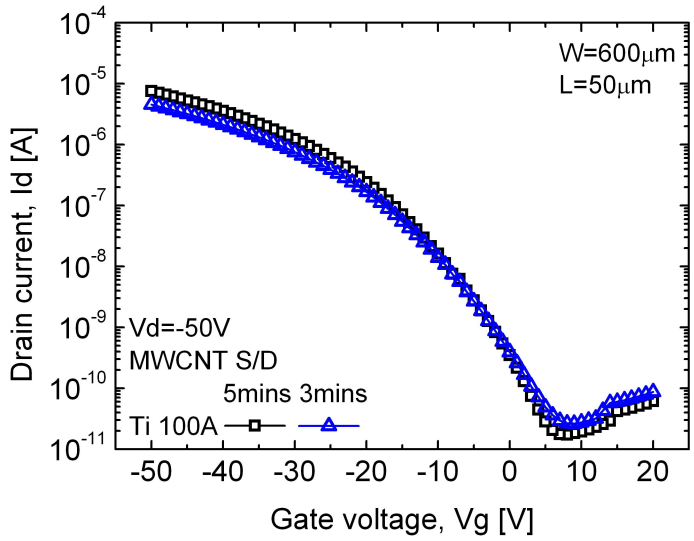


Figure 4.3-2 The MWCNT growth recipe of T-CVD.



(a)



(b)

Figure 4.3.1-1 The Id-Vg electrical characteristics of pentacene TFTs with MWCNT S/D and different MWCNT growth times. The channel width/length of devices are (a) 75/50 μm/μm and (b) 600/50 μm/μm.

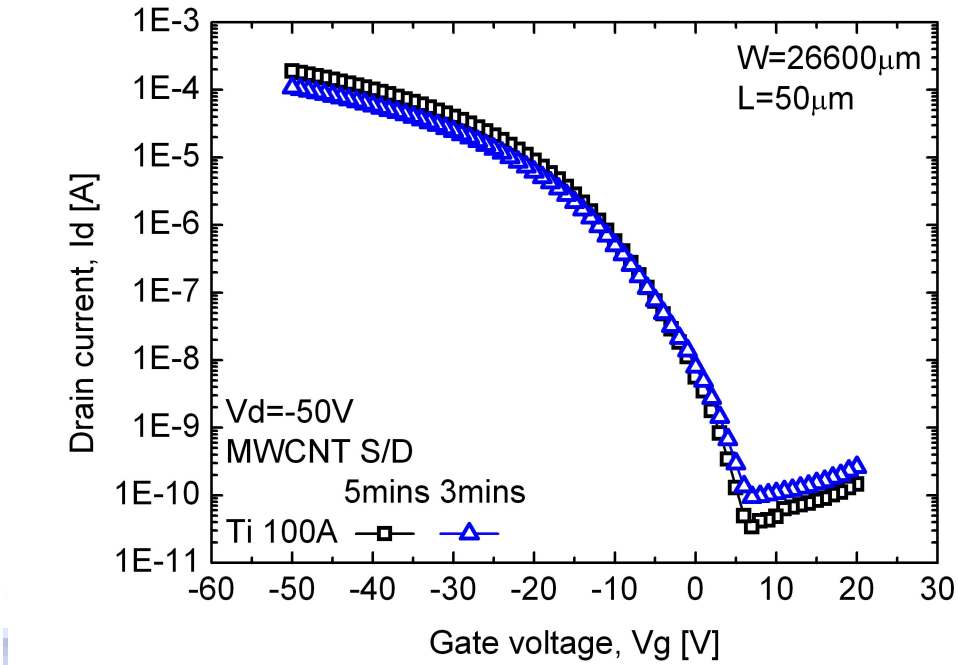
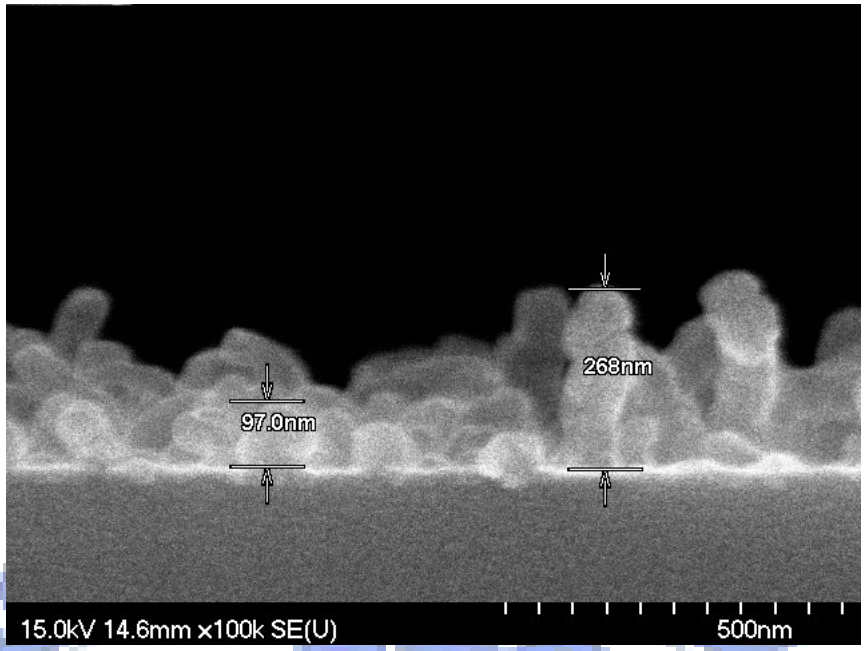
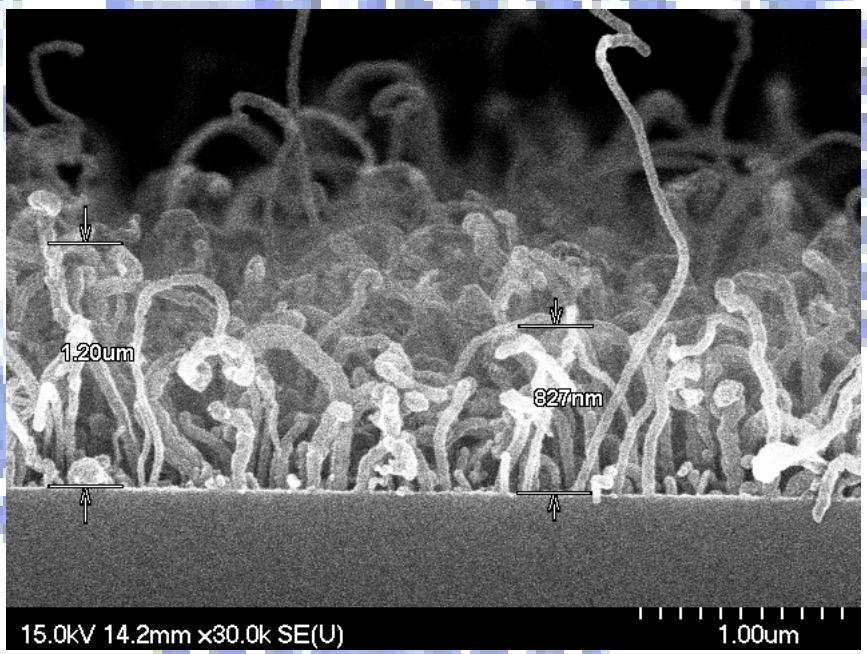


Figure 4.3.1-2 The Id-Vg electrical characteristics of pentacene TFTs with MWCNT S/D and different MWCNT growth times. The channel width/length of devices are 26600/50 μm/μm.

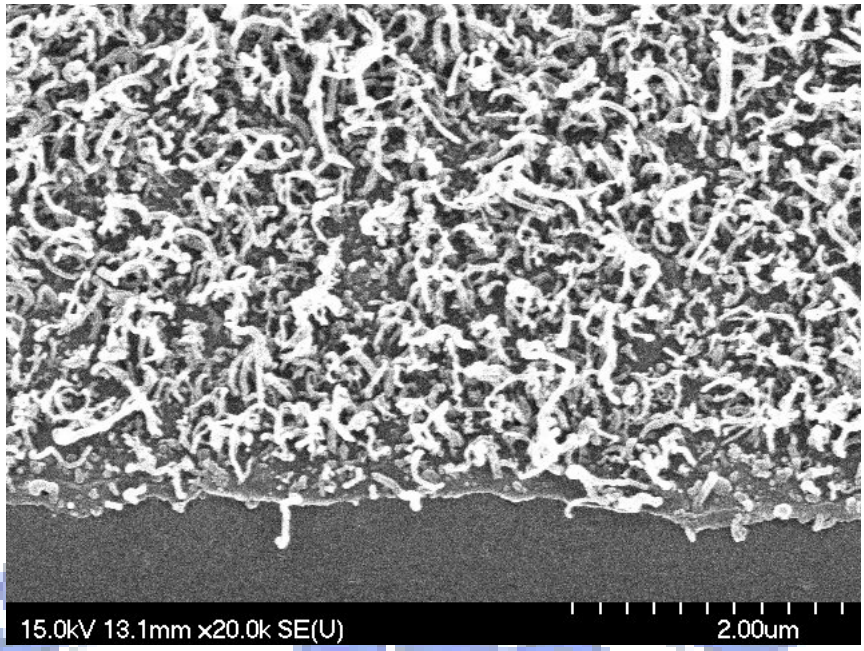


(a)

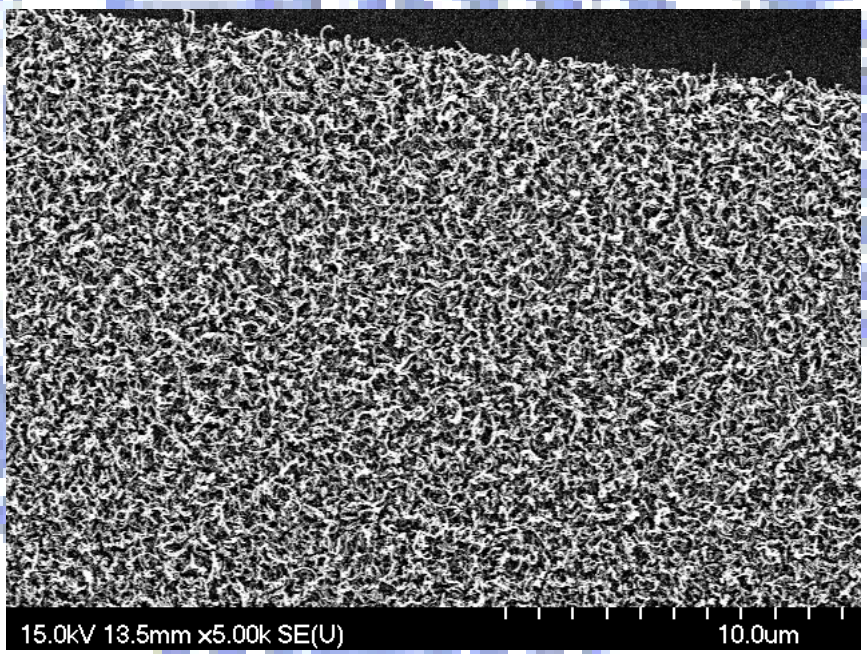


(b)

Figure 4.3.1-3 The SEM images to observe the lengths of MWCNTs which are (a) 300 nm and (b) 1 μm for 3-minute and 5-minute of growth times, respectively.

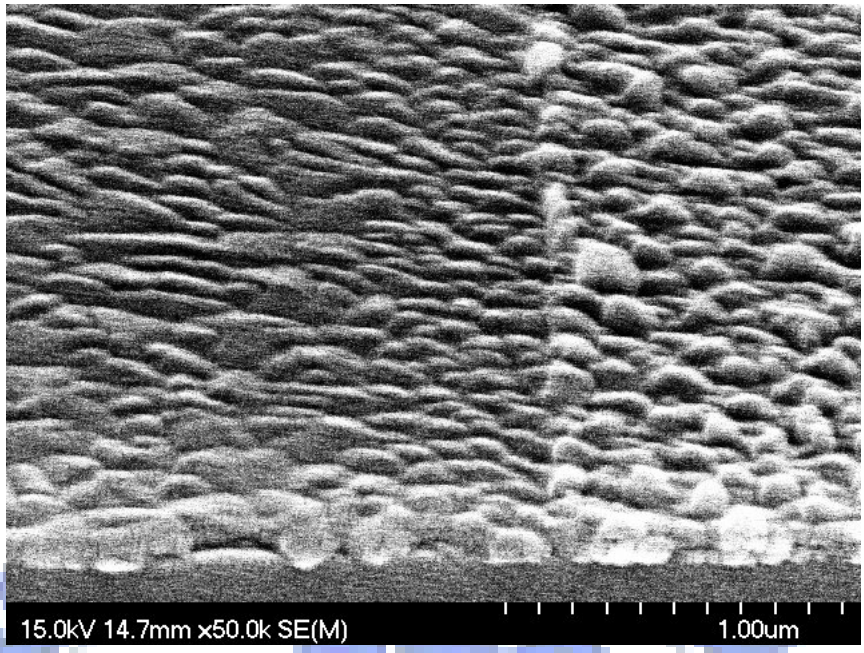


(a)

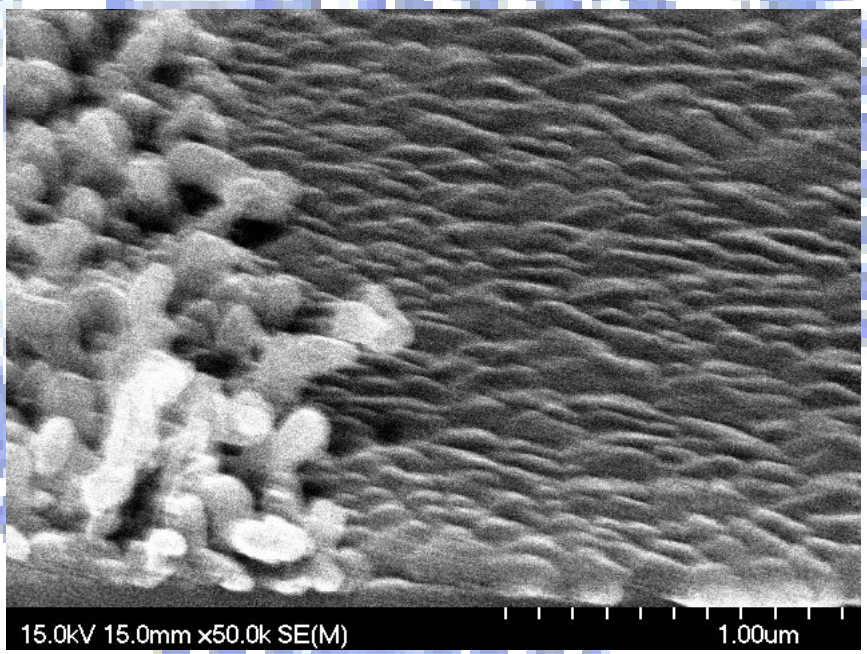


(b)

Figure 4.3.1-4 The SEM images of top view of MWCNT S/D which is at the junction of S/D and gate dielectric. The MWCNT growth times are (a) 3 minutes and (b) 5 minutes.

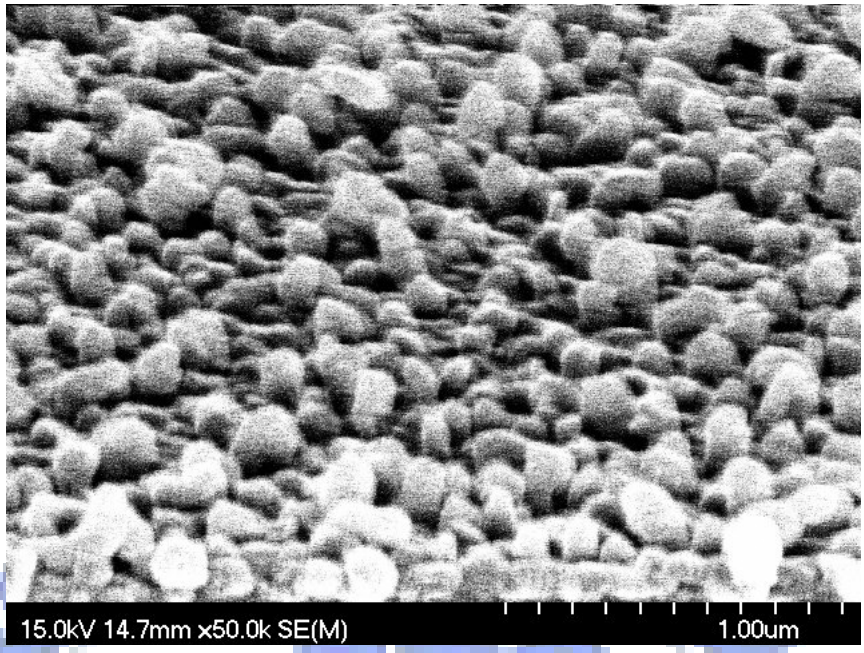


(a)

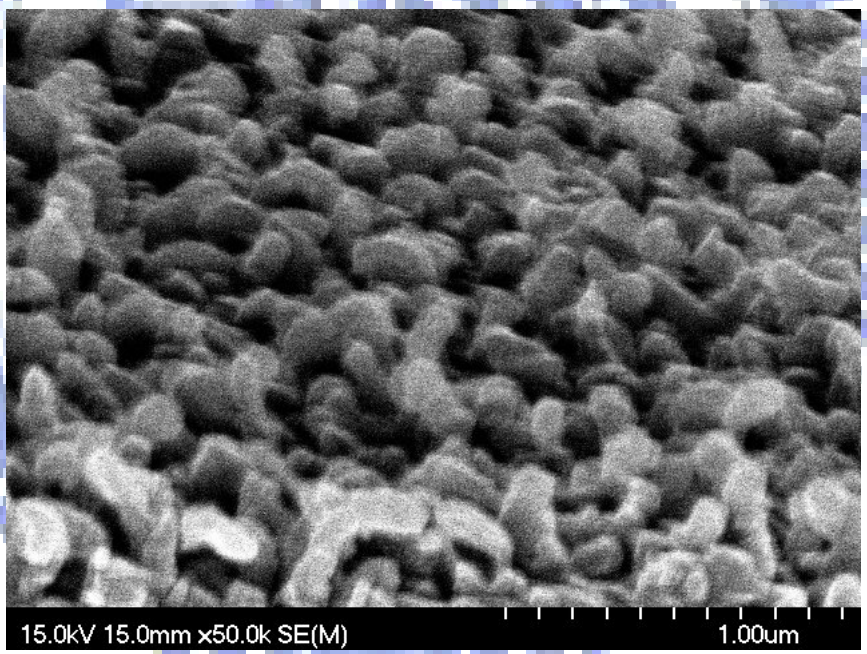


(b)

Figure 4.3.1-5 The SEM images of cross-section view of MWCNT S/D after pentacene deposition which is at the junction of S/D and gate dielectric. The MWCNT growth times are (a) 3 minutes and (b) 5 minutes.

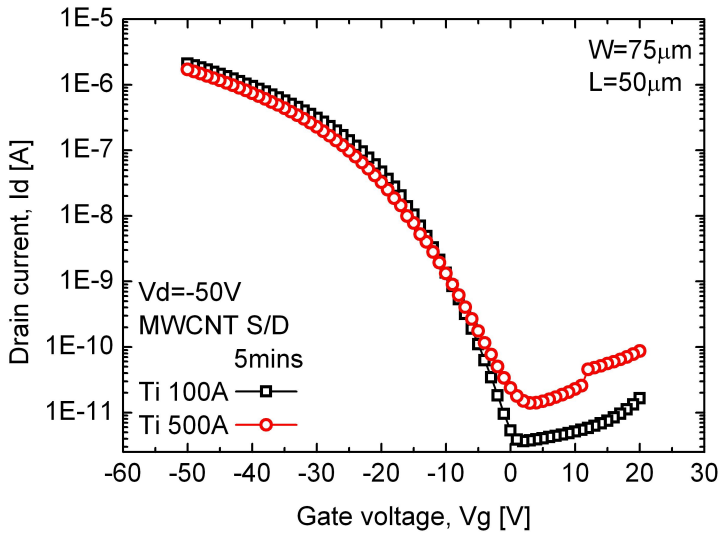


(a)

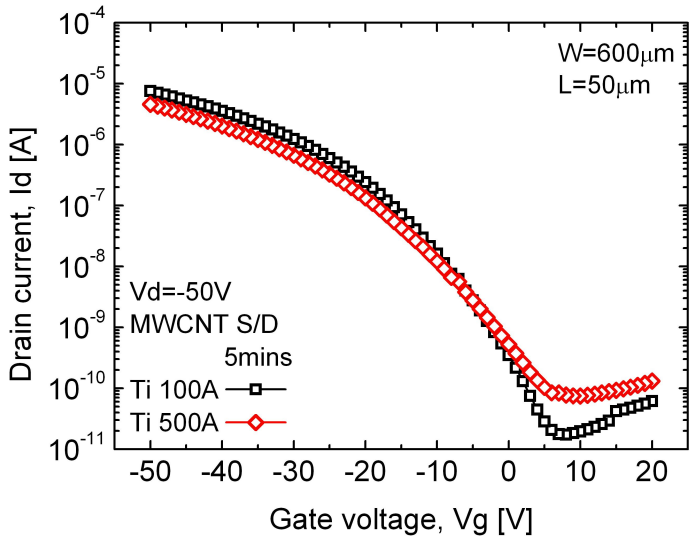


(b)

Figure 4.3.1-6 The SEM images of cross-section view of MWCNT S/D after pentacene deposition. The MWCNT growth times are (a) 3 minutes and (b) 5 minutes.



(a)



(b)

Figure 4.3.1-7 The Id-Vg electrical characteristics of pentacene TFTs with MWCNT S/D and different buffer layer thicknesses. The channel width/length of devices are (a) 75/50 μm/μm and (b) 600/50 μm/μm.

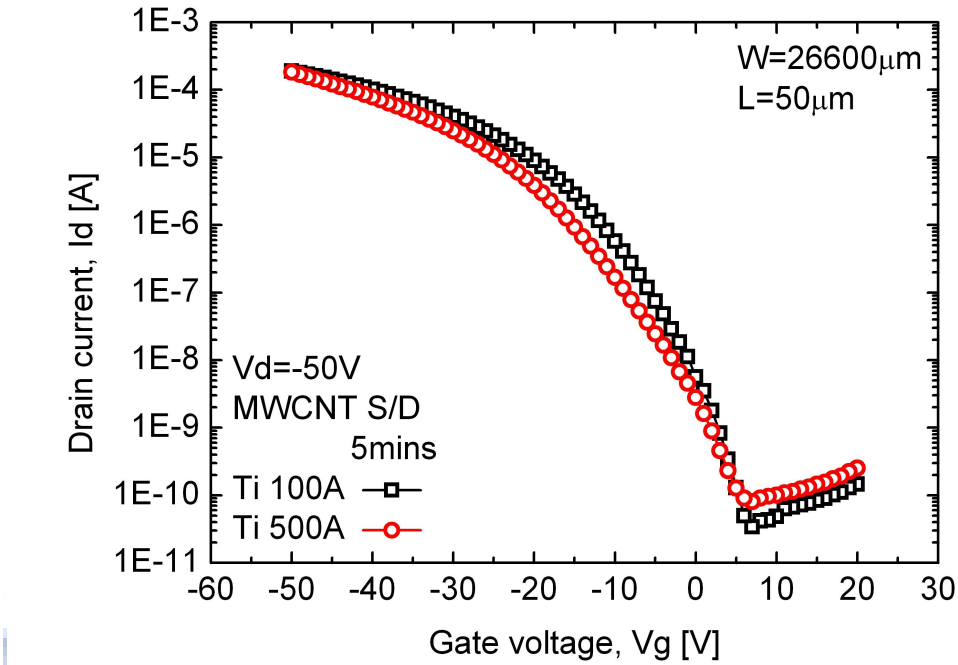
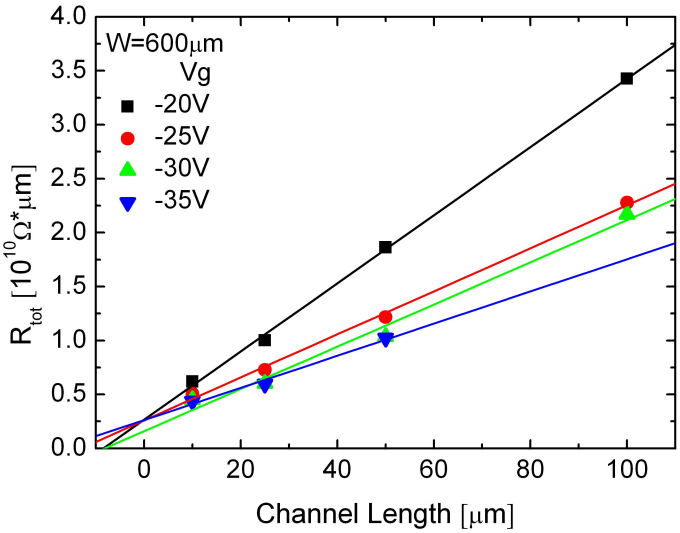
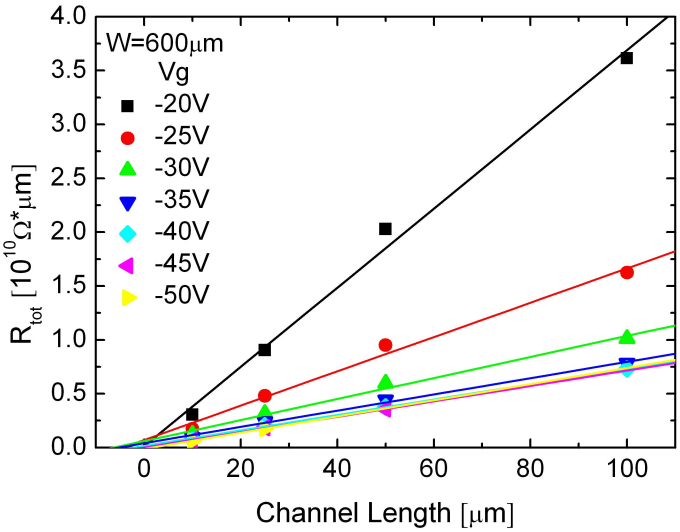


Figure 4.3.1-8 The Id-Vg electrical characteristics of pentacene TFTs with MWCNT S/D and different buffer layer thicknesses. The channel width/length of devices are 26600/50 μm/μm.

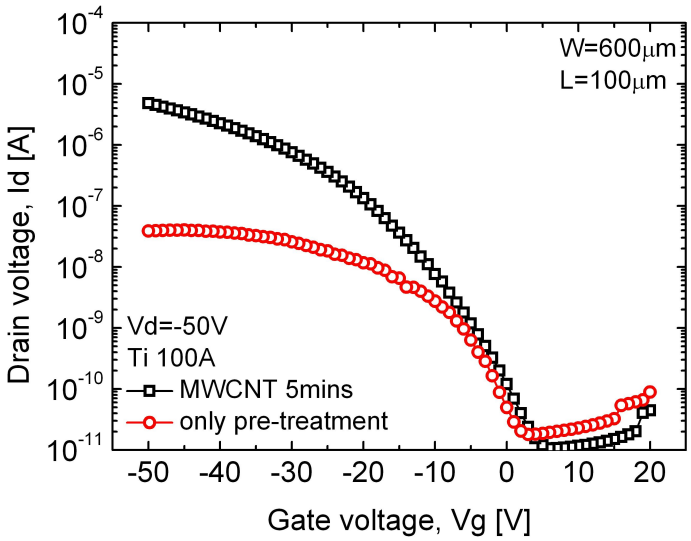


(a)

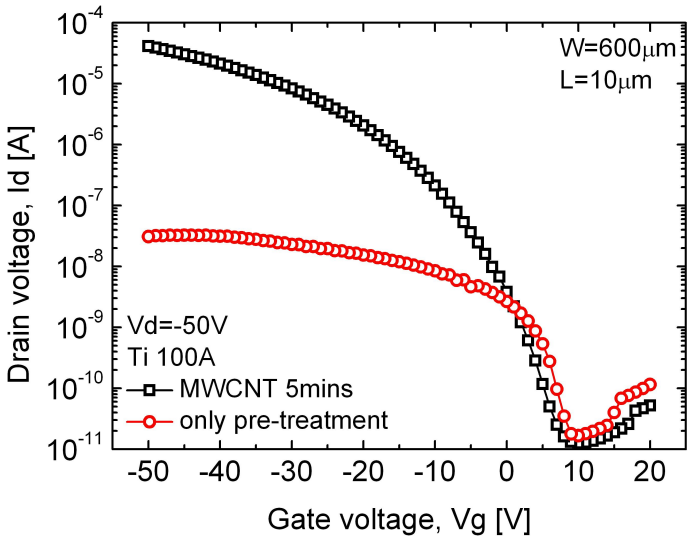


(b)

Figure 4.3.1-9 The Rtot-L diagram of pentacene TFTs with MWCNT S/D. The MWCNT growth times are (a) 3 minutes and (b) 5 minutes and thickness of Ti buffer layer is 10 nm.



(a)



(b)

Figure 4.3.2-1 The Id-Vg characteristics of the OTFTs prepared with and without MWCNTs coverage on the S/D region. The channel width/length are (a) 600/100 and (b) 600/10 μm/μm.

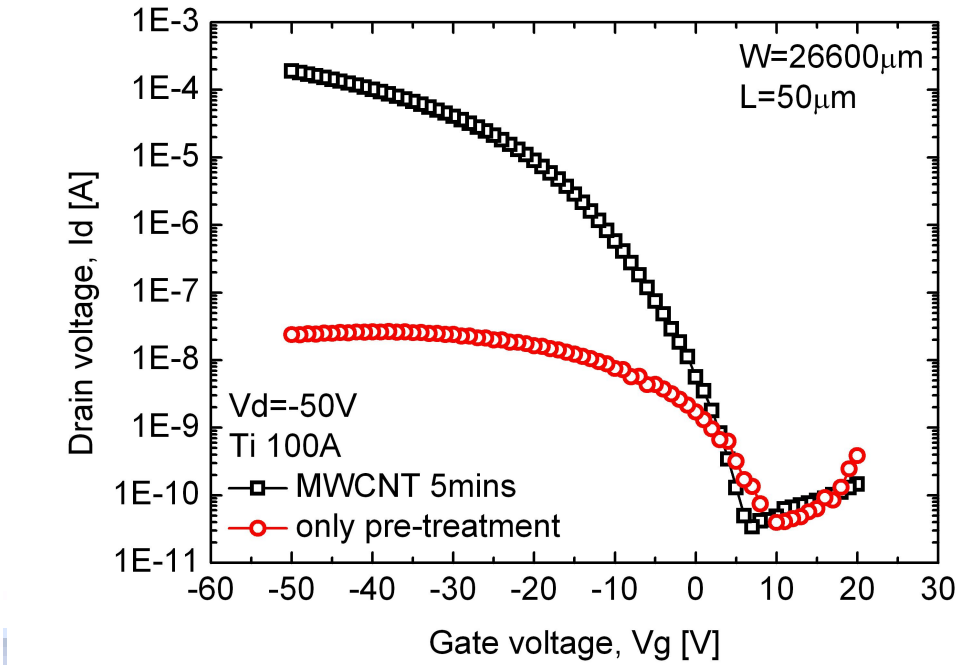
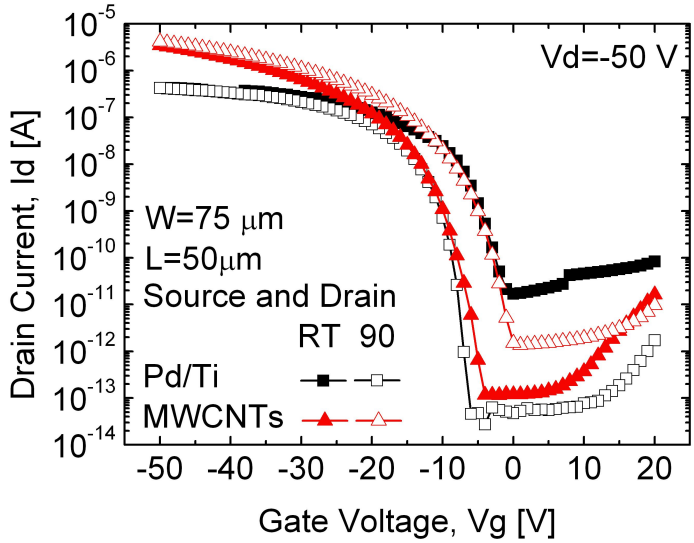
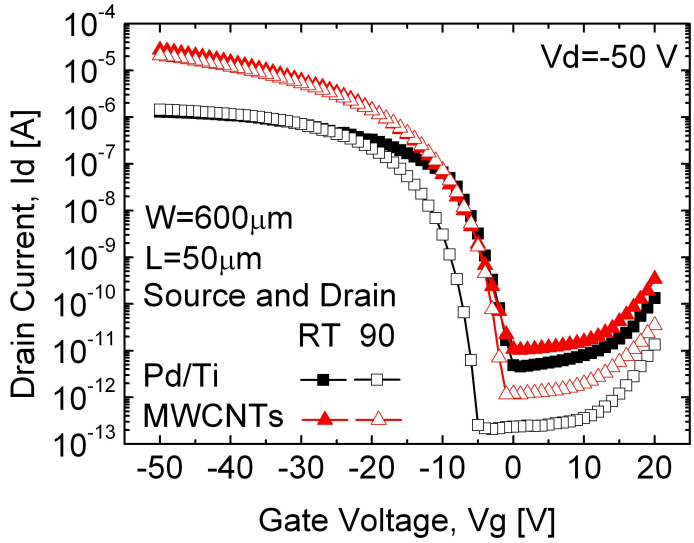


Figure 4.3.2-2 The Id-Vg characteristics of the OTFTs prepared with and without MWCNTs coverage on the S/D region. The channel width/length are 26600/50 μm/μm.

Figure 4.3.2-3 The AFM images to observe the morphologies of pentacene active layer on (a) S/D and (b) junction of S/D and gate dielectric.



(a)



(b)

Figure 4.3.3-1 The Id-Vg characteristics of the OTFTs with MWCNT and Pd/Ti S/D, and the channel width/length are (a) 75/50 and (b) 600/50 μm/μm.

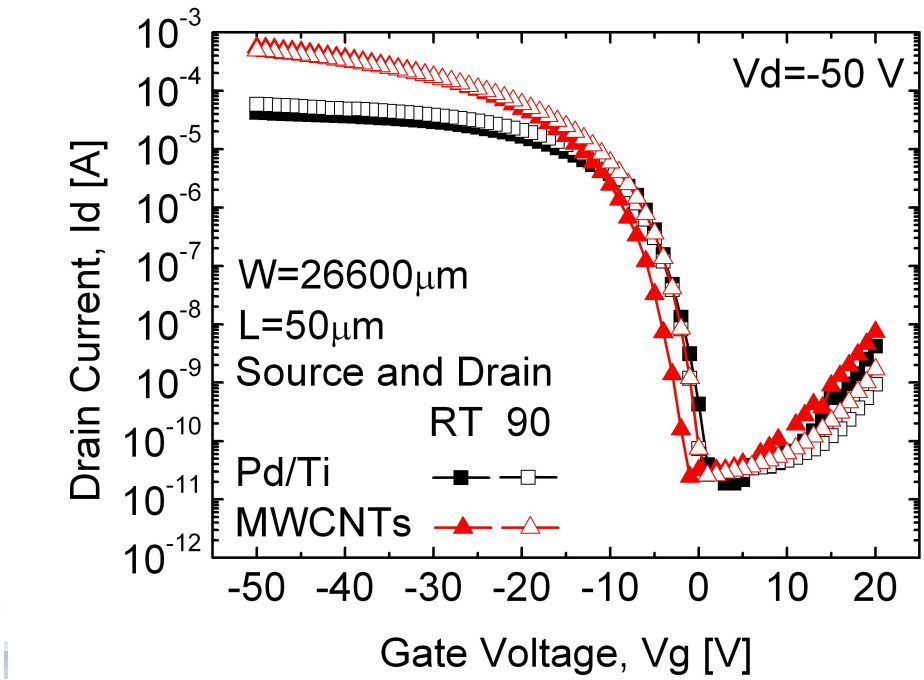
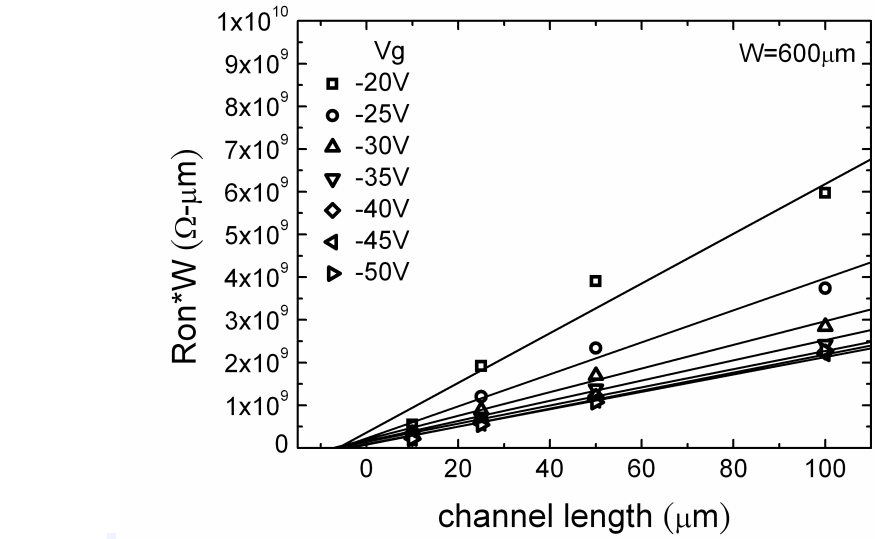
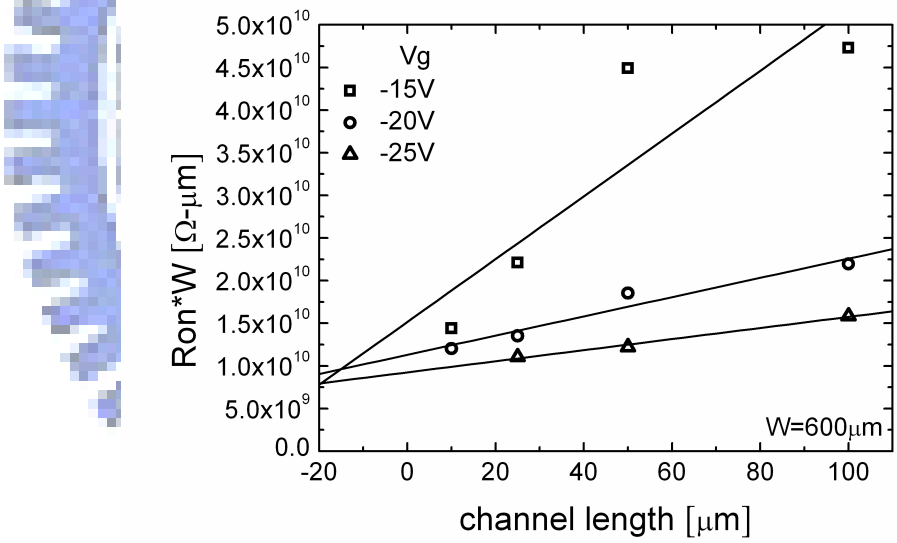


Figure 4.3.3-2 The Id-Vg characteristics of the OTFTs with MWCNT and Pd/Ti S/D, and the channel width/length are 26600/50 μm/μm.



(a)



(b)

Figure 4.3.3-3 The Rtot-L diagrams of pentacene TFTs with (a) MWCNT and (b) Pd/Ti S/D which pentacene deposition temperature is 90 ^{o}C.

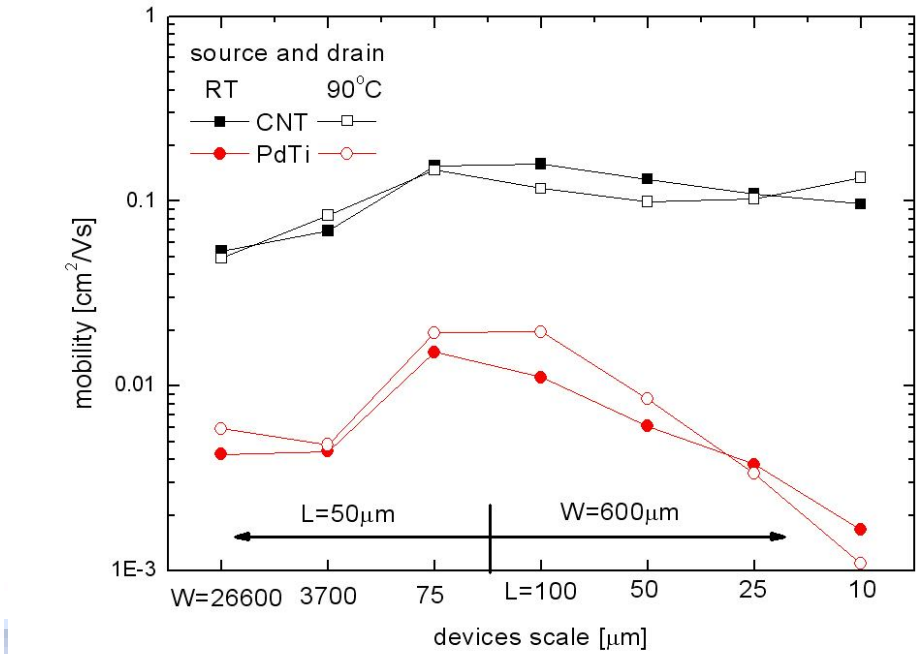


Figure 4.3.3-4 The extractions of mobility of pentacene TFTs with different device scales and pentacene deposition temperatures which are RT and 90 °C.