國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

一個 10GHz 快速鎖定之全數位式頻率合成器

A 10GHz, Fast-Locking All-Digital Frequency Synthesizer

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指導教授：陳巍仁

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碩士論文

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摘要

本論文提出一個具有動態迴路濾波器的 10GHz 快速鎖定之全數位式頻率合成器。其中，動態迴路濾波器主要由一個鎖定追蹤監測器(Locking Process Monitor, LPM)控制，可在追蹤相位時自動調整迴路濾波器的參數，使得整體迴路頻寬可自動調整直到頻率鎖定。利用此機制可使得整體鎖定時間低於 8μs，且當輸出頻率為 9.92GHz 時，其抖動(jitter)的均方根低於 1 ps。在此論文中，並提出一個具偏斜補償的相位累加器電路，使其不只能夠在高速下運作，亦可有低功率的優勢。此論文中的晶片是使用 90nm CMOS 技術實現，整體晶片面積為 0.902mm^2，核心電路的部份只佔 0.352mm^2，使用電壓為 1V，消耗功率約 7.1 mW，其中數位輸入/輸出單元的電壓為 3.3V，消耗功率為 2.7 mW

A 10GHz, Fast-Locking All-Digital Frequency Synthesizer

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Abstract

A 10 GHz all digital frequency synthesizer with dynamic digital loop filter is presented. Governed by a locking process monitor (LPM), the digital loop filter is automatically reconfigured during the frequency acquisition and phase tracking process. Also, the loop bandwidth is self-adjusted to a moderate bandwidth as the loop settles to phase and frequency lock. With less than 8 μsec locking time, the measured rms jitter from a 9.92 GHz carrier is less than 1 ps. A skew-compensated phase accumulator is proposed for high speed operation, which preserves the advantages of low power dissipation while eliminating the accumulated timing skew issue. Implemented in a 90 nm CMOS technology, the core area is only 0.352 mm^2, and the chip size including bonding pad is 0.902mm^2. The ADPLL core consumes 7.1 mW from a 1V supply, and the digital I/O cells drains 2.7 mW from a 3.3V supply for chip measurement.

Acknowledgement

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楊松諭 17, Nov, 2008

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Chapter 1 Introduction

1.1 Motivation

1.1.1 Introduction of Frequency Synthesizers

Frequency synthesizers are the key building blocks for most of the modern electronic and communication systems, including radio receivers, mobile telephones, and satellite receivers. The basic goal of a frequency synthesizer is to generate a periodic signal with a given frequency and phase relationship with respect to a reference signal. The generated clock signal can be served as clock source for processors, transmit clock in high speed data interfaces, sampling clock for analog to digital convertor, and local oscillator signal for wireless transceiver which mixes the signal of interest to a different frequency. Many approaches of frequency synthesizers have been devised over the years, such as phase-locked loops (PLLs), direct digital synthesis (DDS), and frequency mixing. Among different approaches of frequency synthesizer, most state of the art high-performance frequency synthesizers are based on the phase-locked loops technique.

A phase-locked loop is a frequency control system with negative feedback. By sensing the phase difference between the feedback path of a controlled oscillator and the input reference signal, a PLL generates a signal with the phase that has a fixed relation to the phase of a reference signal. It responds to both the frequency and the phase of the reference signal and automatically raises or lowers the frequency of a controlled oscillator until output signal is matched to the reference in both frequency and phase. A PLL can be used to generate a

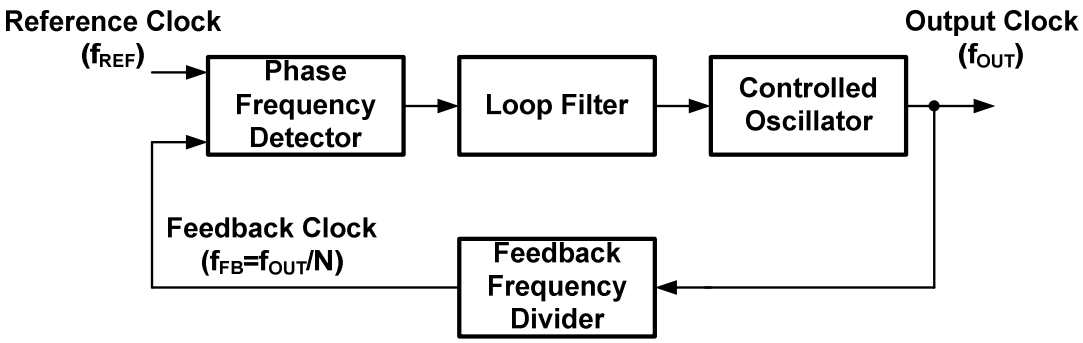


Fig. 1-1 Block diagram of a phase-locked loop

signal, modulate or demodulate a signal, reconstitute a signal with less noise, or multiply or divide a frequency.

The basic structure of a phase-locked loop is illustrated in Fig. 1-1 [1], which consists of a controlled oscillator, a phase frequency detector, a loop filter, and a feedback frequency divider. In this architecture a controlled oscillator generates a periodic signal with a frequency f_{OUT} determined by the value of controlled oscillator input. The output clock is divided by a feedback frequency divider having a frequency $f_{FB}=f_{OUT}/N$, where N is the divided ratio of the frequency divider. A phase frequency detector compares the phase or frequency difference between the feedback clock and a reference clock, having a frequency f_{REF}. The output signal of phase frequency detector which carries the frequency or phase error information is then processed by a loop filter. The abrupt changes in the error information generated by phase frequency detector are then smoothed out by loop filter. Finally, the output of the loop filter feeds to the controlled oscillator and adjusts the frequency f_{OUT} of the output clock. The loop reaches a steady state condition where $f_{OUT}=f_{REF}N$, and the given relationship between the output clock and reference clock is established if the loop is properly designed.

The design of the CMOS integrated PLL based RF synthesizers remains one of the most challenging tasks in communication systems because they must meet the strict requirements of low-cost, low-power, monotonic implementation while also meeting the noise and transient specifications. In general, a frequency synthesizer design can be evaluated by the following considerations: Phase noise or jitter performance, spurious noise performance, frequency hopping speed, tuning bandwidth, rejection of supply or substrate noise, chip area, power consumption and portability for the design to transfer to a different technology node. However, there exist complicated design trade-offs among these criteria mentioned above. Therefore the requirements that a synthesizer must fulfill depend heavily on the specific application.

The conventional PLL based RF synthesizer is usually made as an analog building block. As the feature size of the CMOS technology becomes smaller, the low-voltage deep-submicrometer digital CMOS process allows more and more digital circuits to be integrated in a single ship with higher operation frequency while consuming less power due to smaller parasitic capacitance and lower supply voltage. The analog circuits, however, does not benefit much from the scaling of the CMOS devices. Indeed, the small voltage headroom, high leakage current and the noisy environment on a SOC make the design of high-performance synthesizers more and more difficult. Thus, many research efforts recently focus on the digitally intensive or digitally assisted approach of the RF synthesizer [2]-[4]. Next, a description of the target application and its requirements on the synthesizer will be given.

1.1.2 Target Application and its Requirements

The rapidly growing volume of data transfer in telecommunication networks has motivated the widespread usage of the optical communication, which permits transmission over longer distances and at higher data rates than other forms of communication channels. Fig. 1-2 shows the block diagram of a generic optical communication system [5].

At the transmit side, the input parallel data is first converted to serial data by the serializer. Since the output of the serializer may suffer from nonidealities such as jitter and inter-symbol interference (ISI). The serial data is resampled by a flip-flop triggered by the clock multiplication unit (CMU) before the signal is sent to the laser driver. The output of retimer is then amplified to drive the laser diode. Finally, the optical signal is generated by the laser diode and guided by the optical fiber.

At the end of the fiber, a photodiode senses the light and produces electrical

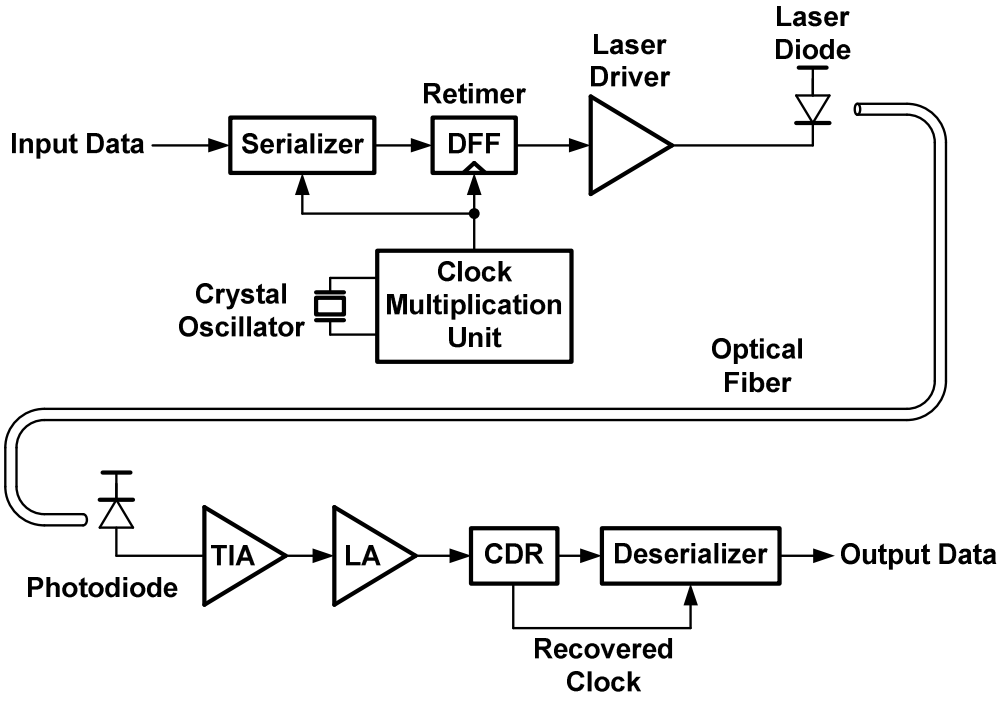


Fig. 1-2 Block diagram of optical transmitter and receiver.

current signal to the transimpedance amplifier (TIA). A high gain limiting amplifier (LA) follows the TIA and generates output signal with large voltage swing to provide logical levels. In order to perform synchronous operations such as retiming and deserializing on the random data, the receiver side must generate a clock. The task of generating such a clock from input data and retiming the data are performed by the clock and data recovery circuit (CDR). Finally, the original parallel data is reproduced by the deserializer.

The clock multiplication unit has been selected as our target in this thesis. In the synchronous optical network (SONET) standard, the data rate of the bitstream carried by the digital signal is defined by the optical carrier (OC) level. For example, the SONET OC-192 is a network line with transmission speeds of up to 9953.28 Mbit/s. Another major design consideration is the output jitter performance. The SONET specifications impose output peak-to-peak and rms jitter at the transmitter optical interface below 0.1UI and 0.01UI when integrated between 50 kHz and 80 MHz. These correspond to 10ps and 1ps for an OC-192 carrier. The goal of this work is to design a frequency synthesizer which generates a low jitter 10 GHz clock satisfying the SONET OC-192 specifications.

1.2 Overview of Thesis

The thesis is organized as follows. In chapter 2, the conventional analog PLL implementations and the state of the art digital frequency synthesizers will be shortly addressed with comments on systems and technology trend. The proposed all-digital phase locked loop (ADPLL) architecture and its operation principle will be presented.

In chapter 3, we make some investigations on the dynamic of the ADPLL. The conditions for stability and the expression of locking range will also be derived. To obtain the noise transfer function of the loop, a linear model for the ADPLL is introduced. The output phase and jitter will be analyzed with the help of the linear model.

Chapter 4 starts with the top level block diagram of the ADPLL. The implementation details of the most important building block, namely the phase detection circuits, the digitally controlled oscillator and the high speed frequency divider, will be described.

In chapter 5, the experiment setup and the measurement results of the implemented prototype will be presented. Finally, a brief conclusion of this work is given in chapter 6.

Chapter 2 ADPLL Architecture

2.1 Architecture of BBPLL

2.1.1 Analog PLL

A great majority of high performance analog PLL are based on the charge-pump PLL structure [5]. The structure of the charge-pump PLL is shown in Fig. 2-1. The phase frequency detector (PFD) estimates the phase difference between the reference clock f_{REF} and the divided-by-N voltage controlled oscillator (VCO) clock f_{FB} by measuring the time difference between their closest edges and generates either an Up or a Down pulse with width proportional to the time difference measured. The current pulse generated by the charge pump is converted into the control voltage of the VCO at the loop filter. The main task of the loop filter is to suppress the glitches introduced by the charge pump on every phase comparison instance. The loop automatic adjusts the VCO control voltage by the feedback mechanism, so that under locked conditions, the average output

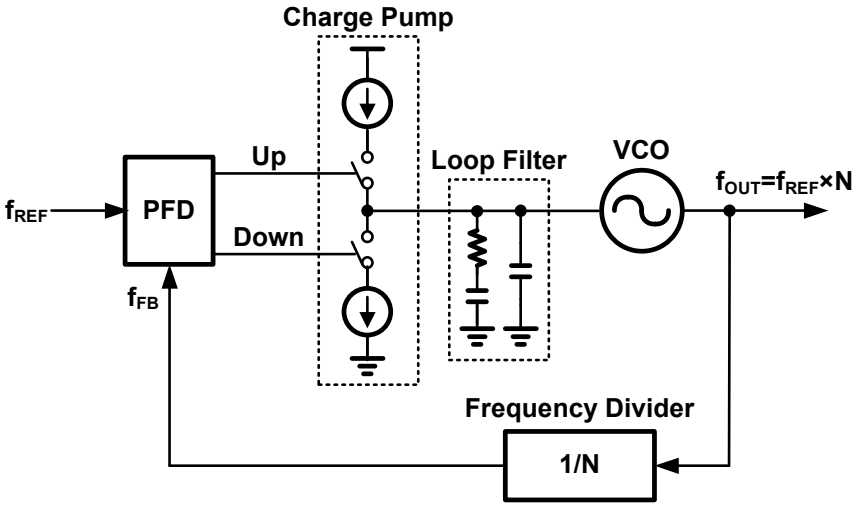


Fig. 2-1 Typical charge-pump-based PLL.

frequency establishes an exact relationship to the reference input frequency.

With proper design of the loop parameters, the performance of the charge-pump PLL can meet the requirements of different applications including Ethernet receivers, disk drive read/write channels, wireless transceivers, high-speed memory interfaces. Unfortunately, big challenges to the implementation of low-jitter analog synthesizers are coming from future system and technology trends.

The explosive growth of today's telecommunication market has brought an increasing demand for low cost, reduced power consumption and more functionality of the silicon chip. These requirements are driving an unprecedented degree of integration of digital and analog circuitry on the same die forming what is known as System-on-Chip (SoC).

As the technology paradigm shifts into the nano-meter CMOS arena, the advanced process presents the new integration opportunities but complicates the implementation of traditional RF and analog circuits. For example, charge-pump-based PLL implementations in the deep-submicron CMOS may encounter capacitor leakage, current mismatch, and limited dynamic range under low supply voltage, leading to higher noise floor and spurious tone emission. Moreover, the high degree of integration allows more digital switching noise to be coupled into the high-precision analog section through the power supply network and the low-resistance substrate. This degrades the noise signal to noise ratio of the analog circuit and the problem gets worse with the scaling down of the supply voltage.

On the other hand, migrating to the digitally intensive frequency synthesizer can benefit from the advantages of the digital design, including robustness against process-voltage-temperature (PVT) variation and substrate

noise, higher flexibility of the loop filter design, fast design turnaround cycles, ease of testability, smaller silicon area and less power dissipation, which can get better with each process node. Consequently, digital intensive or digital assistance approached of the frequency synthesizers have drawn tremendous research efforts recently [2]-[4]. In next section, some of the state of the art all digital synthesizer will be illustrated.

2.1.2 All-Digital PLL

Due to the lack of the low-jitter digitally controlled oscillator (DCO), all digital PLLs really took off in practical high-performance RF applications in the past decade. Recently, a digitally controlled oscillator, which deliberately avoids any analog tuning voltage controls, was first ever presented in [2] for RF wireless applications. The phase domain ADPLL which uses this DCO is also reported in [3]. Its block diagram is shown in Fig. 2-2. Excellent phase noise performance and fine frequency resolution is achieved through the LC-tank based DCO and high-speed ΣΔ dithering. The variable phase $R_V[i]$ is determined by counting the

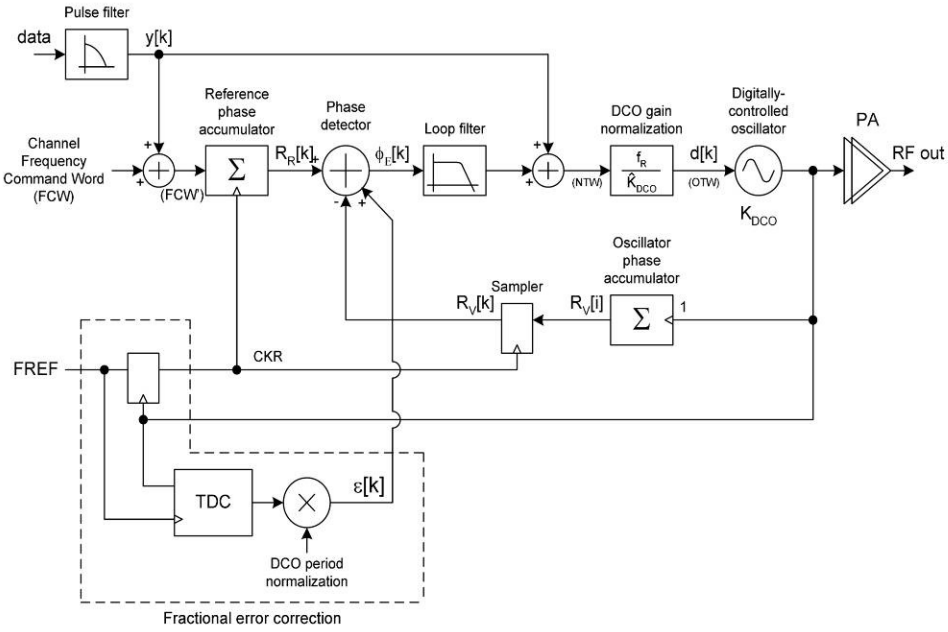


Fig. 2-2 Block diagram of the ADPLL architecture proposed in [3]

number of rising clock transitions of the DCO oscillator clock, while the reference phase $R_R[k]$ is obtained by accumulating the frequency command word (FCW) with every rising edge of the retimed reference clock CKR. The phase error is resolved by subtracting $R_V[i]$ from $R_R[k]$ and then filtered by a digital loop filter. Finally, the output of the filter is fed to the normalized DCO to adjust the output frequency.

Due to the edge counting nature, the quantization resolution is limited by the DCO clock period. For wireless applications, a finer resolution is required. This is achieved by using the time to digital converter (TDC), which measures the fractional time difference between the reference clock and the next rising edge of the DCO clock. It has a resolution of a single inverter delay, which is better than 40ps in the deep-submicrometer CMOS process. In order to accomplish good phase noise performance, great care must be taken with the TDC layout matching and the accuracy of the DCO period normalization factor for the output of TDC.

In [4] an all digital bang-bang PLL (BBPLL) with spread-spectrum capability is presented for the application of memory controller. The structure of the BBPLL is addressed in Fig. 2-3, where the phase information between the reference clock Fref and the feedback clock Fdiv is estimated by a simple binary phase detector (BPD). Its operation is equivalent to a one bit quantizer for the phase error. Since the BPD is sensitive only to the polarity of the phase information, it may suffer from long locking time with large initial frequency error.

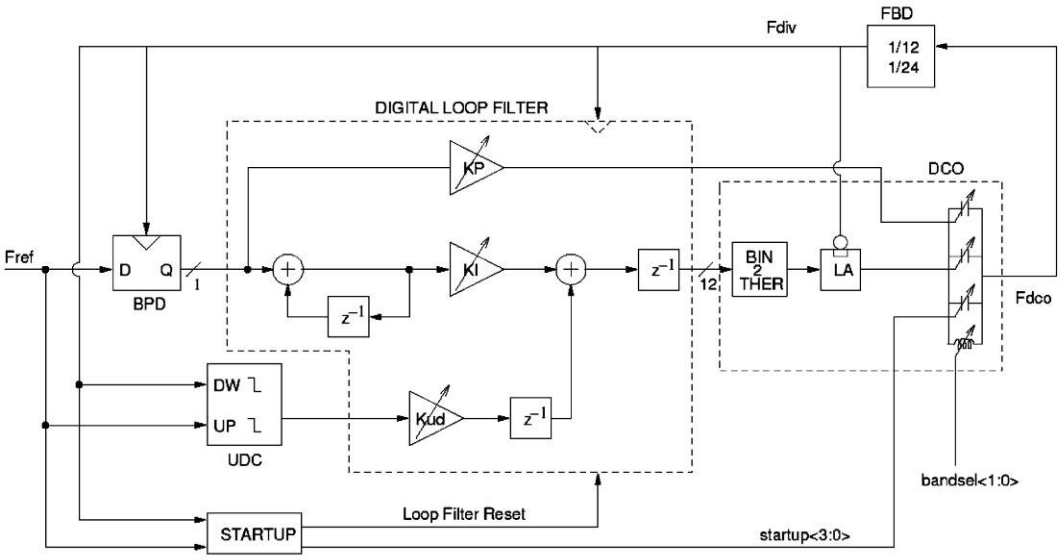


Fig. 2-3 Block diagram of the digital BBPLL architecture proposed in [4].

According to the method of the phase sensing, the ADPLL can be roughly classified into two major categories: linear phase detection and binary phase detection. [3] is belong to linear phase detection while [4] may represent the latter one. The ADPLL with linear phase detection may resort to the TDC or more complicated phase detector design compared to the one with binary phase detector. However, its counterpart that utilizes the binary phase detection suffers from larger output jitter, higher spur energy and longer settling time.

2.2 Proposed Solution

2.2.1 Proposed Dual Mode ADPLL Architecture

The architecture of the 10GHz ADPLL is illustrated in Fig. 2-4, which is composed of a dual-mode phase frequency detector (DPD), a PI digital loop filter composed of programmable integral (α) and proportional (β) path, a locking process monitor (LPM), an LC based digital controlled oscillator (DCO), a divide-by 4 prescaler, and two phase accumulators PAC1 and PAC2. The PAC1 accumulates quarter of the frequency multiplication factor (N/4), while

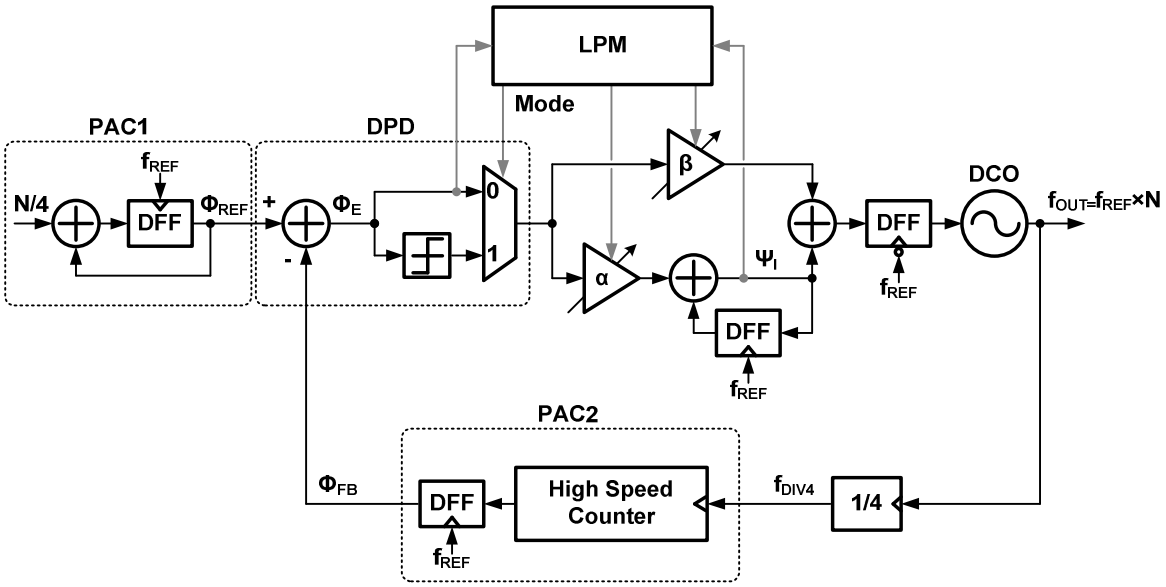


Fig. 2-4 Block diagram of the proposed ADPLL.

PAC2 accumulates the prescaler output phase. The phase difference (Φ_E) between f_{REF} and f_{OUT}/N is then resolved by a subtracter. In the locked state, the difference between the contents in PAC1 and PAC2 is constant. The DPD is operated in the linear mode during frequency acquisition (FA), and is turned into binary mode during the phase tracking (PT) process. In order to reduce the power consumption of PAC2, a divided-by 4 prescaler is introduced after the DCO. In the following section, the operation principle of the ADPLL will be discussed in detail.

2.2.2 Overview of the Operation

In the initial phase of the locking process, the loop starts with the FA mode. During this mode, the DPD is operated in linear mode (Mode=0) and the integral path of the digital loop filter is disabled (α=0), leading the PLL to become a second order frequency acquisition loop. To accelerate frequency acquisition, a larger forward path gain β_{FA1} is first applied and then switched to a smaller β_{FA2} after the loop is settled [15].

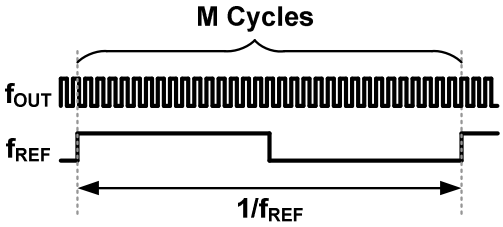


Fig. 2-5 Frequency detection by edge counting.

The principle of the frequency detection can be explained as following. Consider the case shown in Fig. 2-5. If M denotes the number of the rising edge appeared during a reference clock cycle, the relationship between the output frequency f_{OUT} and the reference frequency f_{REF} can be expressed as

$$M = \frac{f_{OUT}}{f_{REF}}. \tag{2-1}$$

The difference between M and the frequency multiplication factor N is

$$M - N = \frac{f_{OUT} - f_{TARGET}}{f_{REF}}, \tag{2-2}$$

where f_{TARGET} is the target output frequency Nf_{REF}. Thus the frequency error can be estimated by (M-N), which can lead to the frequency locked loop as shown in Fig. 2-6. It can be shown that this architecture is equivalent to the structure

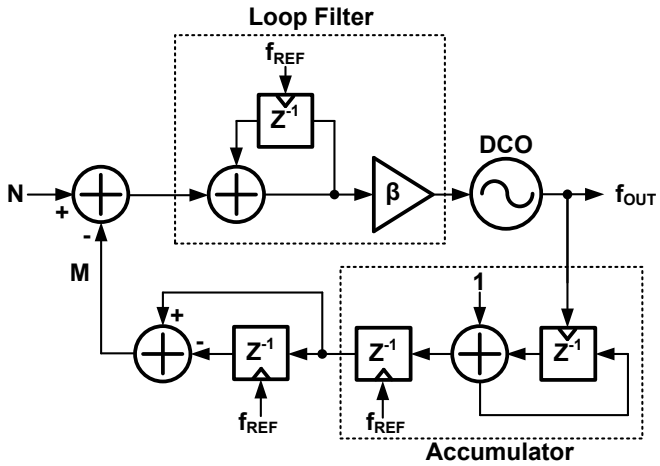


Fig. 2-6 Equivalent frequency locked loop during FA mode.

shown in Fig. 2-4, by moving the accumulator of the loop filter before the subtracter and noting that α=0.

After Φ_E variation is within 1 LSB, the LPM will launch the PT mode. The integral path is then activated, and the whole system is turned into a 2nd order phase-locked loop. In the meantime, PAC1 and PAC2 are reset, while the content of the integrator in the loop filter (Ψ_I) is preset to the current DCO control code. Afterwards, the DPD is switched to the binary phase detection mode by asserting the control signal Mode to 1 without resorting to sophisticated time to digital converter. In the mode, the DPD senses the phase difference Φ_E on every reference period and generates the output bit stream to the loop filter according to its polarity. For example, if Φ_E is less than zero, DPD outputs -1. If Φ_E is equal or larger than zero, DPD outputs 1. Therefore, the loop behavior can be simplified and described by the bang-bang PLL (BBPLL) as shown in Fig. 2-7. The term BBPLL will be used to represent the ADPLL during PT mode in this thesis.

2.2.3 Dynamic Loop-Gain Control

During PT mode, a larger β intends to broaden the loop bandwidth and speed up the locking process, but induces in larger steady state jitter. On the contrary, a

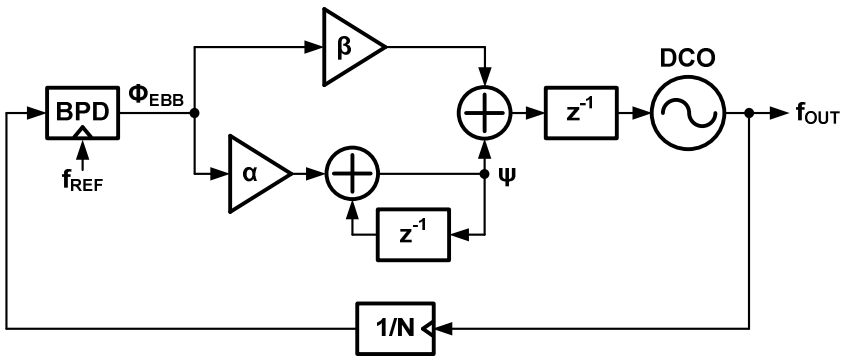


Fig. 2-7 Equivalent Block diagram of the ADPLL during PT mode.

smaller counterpart can suppress the spur and reduce peak to peak jitter, but may result in a lengthy locking time and a narrower lock-in range. To overcome this trade-off, a dynamic loop gain control scheme is proposed. The α and β are adjusted under the constraint of loop stability [7], while optimizing in locking speed, timing jitter, and reference spur prospects.

According to the ΣΔ analogy in the bang-bang PLL behavior [7], the mean value of Ψ_I ($\overline{\Psi_I}$) could represent the locking frequency of the PLL. Thus the proximity of frequency-locked can be detected by monitoring the ripple superimposed on $\overline{\Psi_I}$, which will diminish as the loop approaching the locked state.

Based on this principle, the LPM is realized as shown in Fig. 2-8. It is composed of an operation mode controller, peak/bottom hold detectors, a gradient polarity detector (GPD), registers, and a decision logic for adjusting α and β. The LPM rapidly captures $\overline{\Psi_I}$ by sensing the phase error Φ_E and Ψ_I, so as to adjust α, β and the operation mode (FA and PT mode) accordingly. The GPD generates pulse Φ_{sc} as the slope of Ψ_I changes its polarity. The local maximum (Ψ_p) and minimum (Ψ_b) of Ψ_I can then be updated by the peak/bottom hold detector, which is toggled by Φ_{sc}. Without resorting to time consuming filters, $\overline{\Psi_I}$ can be approximated as the average of successive peak and bottom values

$$\overline{\Psi_I} \approx \frac{\Psi_p + \Psi_b}{2}. \tag{2-3}$$

The criterion of approaching lock ($\overline{\Psi_I} \approx$ constant) can be expressed as:

$$\left|\overline{\Psi_I(n+m)} - \overline{\Psi_I(n)}\right| \le k, \tag{2-4}$$

where k is the locking window and m denotes the time interval between two adjacent peak/bottom values. Under this circumstance, α, β and k are decreased to resume LPM, making the loop bandwidth being dynamically adjusted from a wide-band mode to a narrow band mode. The loop parameters, α, β and k will remain unchanged until the loop reach the next locked state again. After 5 times of the switching gain operations, the loop will finally stay with the state where the loop parameters is optimizing for low output jitter. Fig. 2-9 shows the simulated locking behavior with and without LPM for the same steady state loop

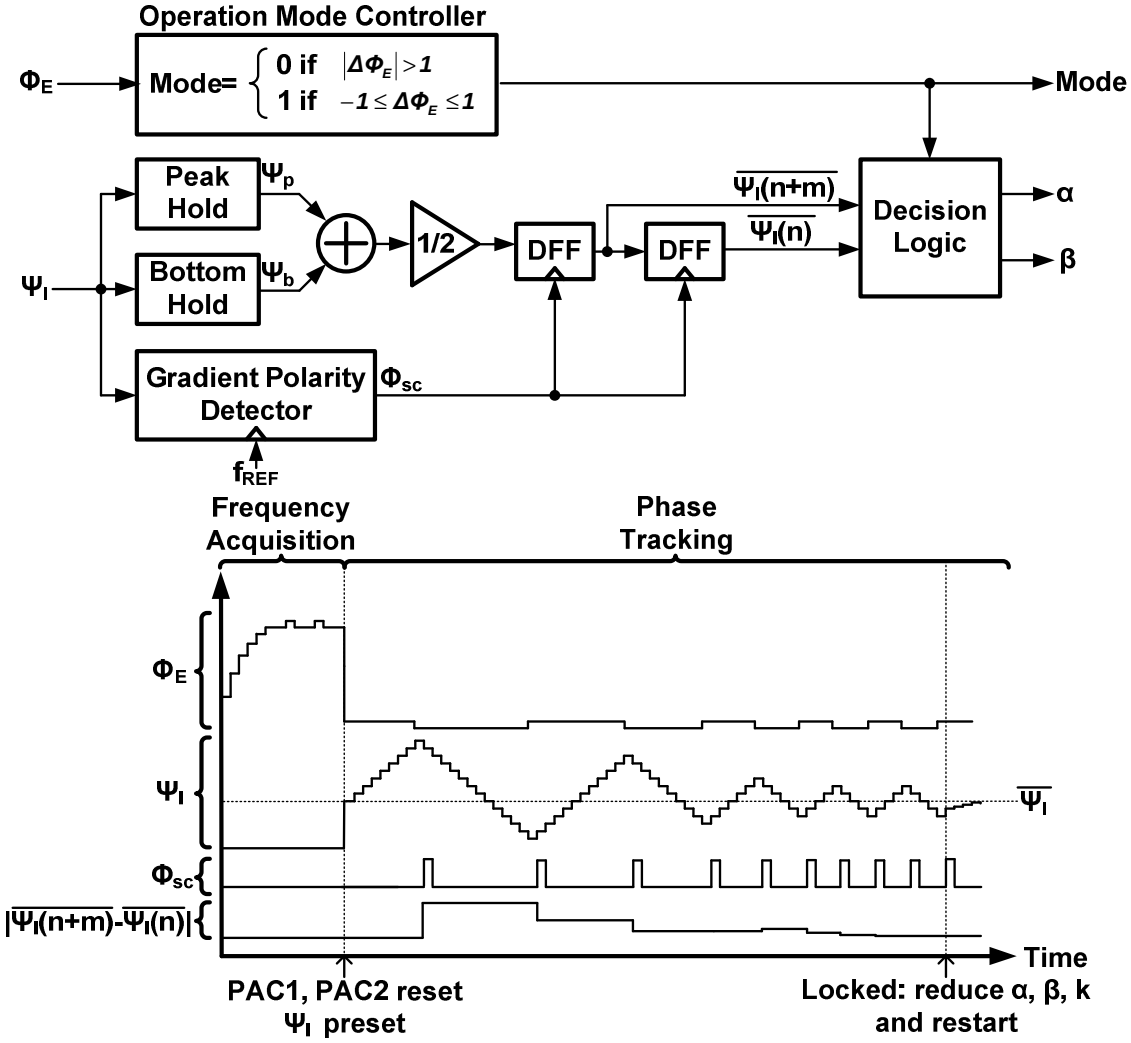


Fig. 2-8 The block diagram of LPM and its time diagram.

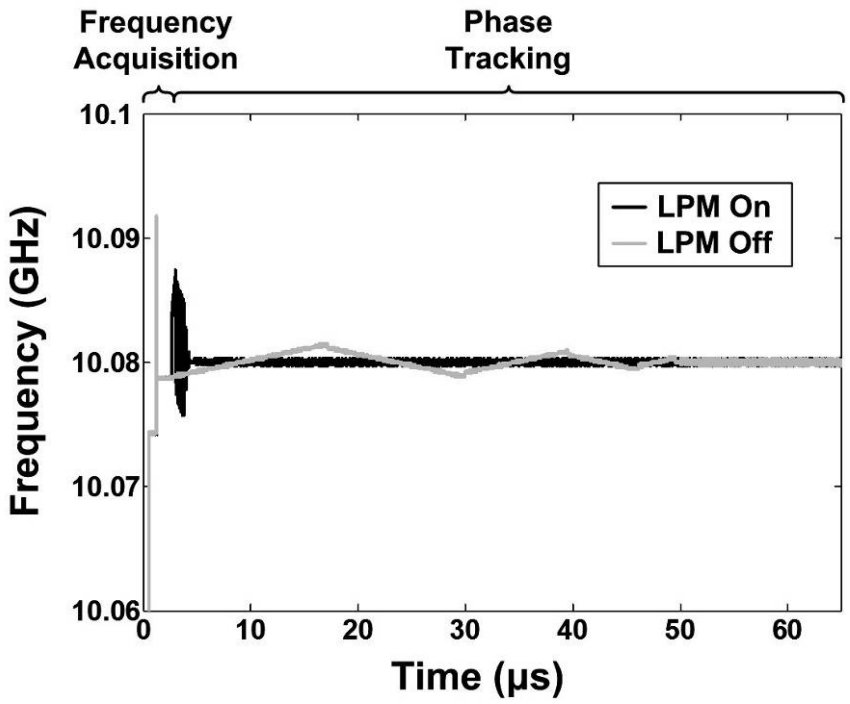


Fig. 2-9 Simulated locking behavior with and without LPM for the same steady state loop bandwidth (100 kHz).

bandwidth. The simulation result shows 10 times locking speed improvement (locking time reduced from 50μs to 5μs) with the aid of the proposed scheme.

In the next chapter, the loop dynamic, and the noise performance will be analyzed.

Chapter 3 Analysis of the ADPLL

3.1 ADPLL in Frequency Acquisition Mode

At the beginning of the locking process, the frequency acquisition mode is first activated and the DCO is locked roughly to the desired frequency. During this mode, the integral path of the digital loop filter is disabled (α=0), and the system block diagram can be simplified as shown in Fig. 3-1. The scaling factor β_{FA} introduced in the figure denotes the forward path gain during frequency acquisition mode. In the frequency domain it controls the gain of the frequency detected in response to the frequency changed at the DCO output. The gain factor β_{FA} also controls several key loop characteristics such as the loop stability, the transient response and the frequency error in the steady state.

In order to investigate in detail how β_{FA} affect the loop behavior, a discrete time z-domain model is build. As mentioned in chapter 2, the block diagram can be rearranged by moving the accumulation operation after the subtractor and places a differential operator on feedback path as illustrated in Fig. 3-2. Two

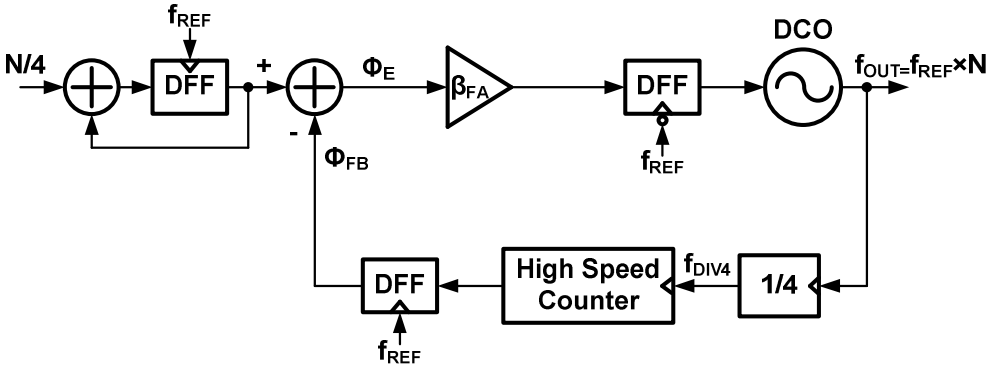


Fig. 3-1 System block diagram during frequency acquisition mode.

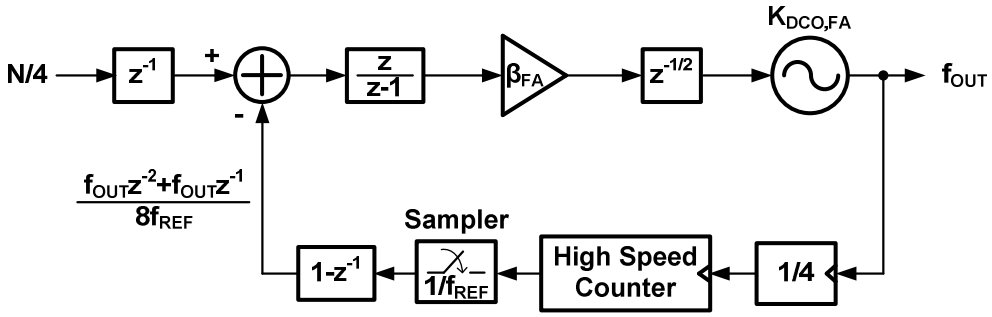


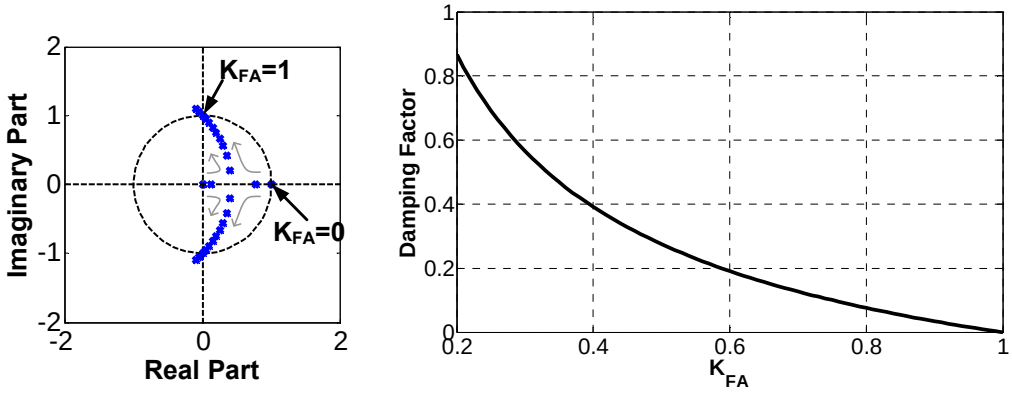
Fig. 3-2 Equivalent system block diagram during frequency acquisition mode.

approximations are used in order to simplify the model. The first is to force the uniform sampling or PLL update rate, despite the presence of a small amount of jitter in the reference clock. This approximation is very accurate since the period deviation due to jitter is several orders of magnitude smaller than the DCO period. The second approximation is the infinite resolution of the phase detection which neglects the fact that the phase information is quantized by the divided DCO clock f_{DIV4}. If the free running frequency of the DCO is ignored and is assumed to be 0, the closed loop transfer can be express as

$$H_{FA,C}(z)=\frac{f_{OUT}(z)}{N(z)}=\frac{2f_{REF}K_{FA}z^{-\frac{3}{2}}}{1+(K_{FA}-1)z^{-1}+K_{FA}z^{-2}} \text{ where } K_{FA}=\frac{K_{DCO,C}\beta_{FA}}{8f_{REF}}, \quad (3\text{-}1)$$

where $K_{DCO,C}$ denotes the frequency step per control code of the active varactor bank in the DCO during frequency acquisition mode.

According to the discrete time signal process theorem, the conditions for stability of a causal system can be derived by examining the position of its poles. For a given system function of a linear and time invariant system, if the outermost pole is included in the unit circle on the pole-zero plot, the system is stable. Considering the system function of the ADPLL in frequency acquisition mode $H_{FA,C}(z)$, the pole-zero plot is illustrated in Fig. 3-3(a) for different K_{FA}. It is clear that the loop stability requires K_{FA} to be less then 1.To gain more clear



(a) (b)

Fig. 3-3 (a) Pole-zero plot and (b) the damping factor as a function of K_{FA} of the ADPLL during frequency acquisition mode

insight into the time domain behavior, the damping factor which is derived from the equivalent continuous time poles by solving $z=e^{sT}$ is shown in Fig. 3-3(b). The result shows that for an over damping system, $K_{FA}<0.244$ for a critically damped system, $K_{FA}=0.244$; and for an under damped system, $K_{FA}>0.244$.

In order to validate the z-domain model of the ADPLL developed here, some simulations are performed by using MATLAB Simulink. Fig. 3-4 shows

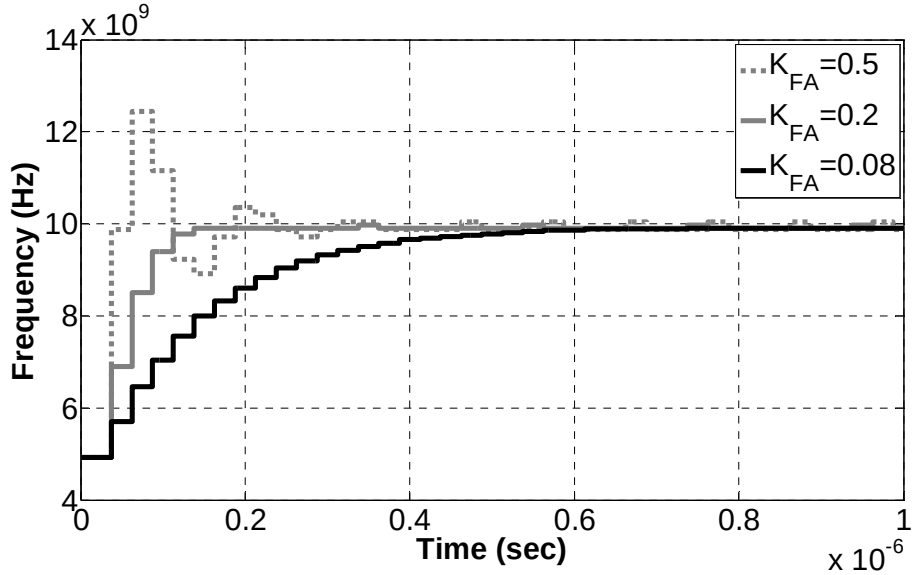


Fig. 3-4 Simulated time domain response of the ADPLL in frequency acquisition mode with 3 different K_{FA} value.

the simulation results of the time domain response with an initial frequency error of 5GHz. For K_{FA}=0.5 it shows a fast response with overshooting while a slow response with longer settling time is obtained for K_{FA}=0.08. The result shows a good agreement between simulation and the analytical model.

It should be noted by inspecting the result shown in Fig. 3-4 where some ripples appear on the output frequency in the steady state. This can be explained by taking the quantization effects into consideration. Due to the edge counting nature of the phase detection, the phase error between the reference clock and feedback is quantized with the resolution step determined by DCO clock rate. When the loop settles, the phase error will be located between two quantization steps, leading to constant output of the phase detection. The phase error will remain unchanged until the accumulated phase error exceeds one quantization step. Then the phase error is corrected by the feedback loop. Thus ripples are generated on the output of phase detector and the output frequency.

Due to the limitation of the capture range, the frequency error after the loop is settled must be taken into consideration before entering the bang-bang phase tracking mode. As mentioned before, the output of the phase detector iterates between two adjacent values when the loop reaches steady state. In other words, the average of the output frequency in steady state indicates the desired clock rate Nf_{REF}. Therefore, the frequency offset of the loop can be characterized by the frequency step

$$\Delta f_{RES,FA} = \beta_{FA} K_{DCO,C} . \qquad (3\text{-}2)$$

Equation 3-2 suggests that the forward gain β_{FA} should be kept lower to enhance the frequency resolution. Unfortunately, this suggestion is in conflict with the requirement for shortening the locking time. The frequency

quantization step could be mode finer at the cost of the slower loop response. Take the critical damping case as an example, substituting K_{FA}=0.244 and f_{REF}=40MHz in equation 3-1, we can obtain $\Delta f_{RES,FA}=\beta_{FA}K_{DCO,C}$=78.08MHz, which is too large for efficient phase tracking.

To speed up the locking process while keeps the frequency resolution high, two different β_{FA} is used during frequency acquisition mode. A larger value β_{FA}=8 is first applied to achieve high loop bandwidth and fast frequency tracking. As the loop settles, the second value β_{FA}=1 is then applied to improve frequency resolution. Since only the coarse tuning bank is active during this mode, $K_{DCO,C}$ is the frequency variation correspond to one LSB of the coarse tuning bank and is about 4MHz/LSB in this design. Thus form equation 3-1, K_{FA} for β_{FA}=1 and β_{FA}=8 is 0.1 and 0.0125, respectively. At the end of the frequency acquisition mode, the frequency resolution is 4MHz. From the simulation results, the time expended is less than 1μsec in frequency acquisition mode.

3.2 ADPLL in Phase Tracking Mode

3.2.1 Locking Transient of the ADPLL during Phase Tracking Mode

After the initial frequency is locked roughly using the frequency acquisition mode, the fine tuning varactor bank of the DCO and the integral path of the loop filter are activated. Then the bang-bang phase tracking (PT) mode is entered and the system block diagram during this mode is illustrated in Fig. 3-5.

As already mentioned in Chapter 2, the architecture can be further simplified as a digital bang-bang PLL (BBPLL) where a binary phase detector (BPD) and a divided-by-N frequency divider are used instead of the binary

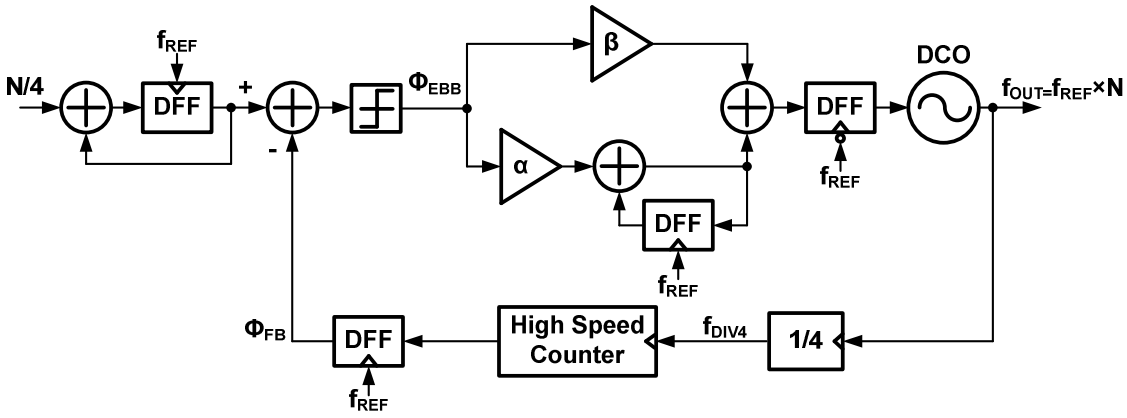


Fig. 3-5 System block diagram during bang-bang phase tracking mode.

quantizer, the accumulators and the subtracter as shown in Fig. 3-6. The binary phase detector output Φ_{EBB} is set to -1 when the rising edge of the feedback clock leads the reference clock edge. Otherwise, Φ_{EBB} is set to 1 to indicate that the feedback clock lags the reference clock. The variables D and Ψ_I introduced in Fig. 3-6 denotes the loop delay time normalized to one reference clock period $1/f_{REF}$ and the integral path output of the loop filter, respectively. In our design, the value of D is 0.5 which is introduced by the re-synchronizing operation before the digital loop filter output feds to the DCO.

The classical treatment of linear PLLs is done in the frequency domain by using of the Laplace transform or the Z-transform. Due to the presence of the

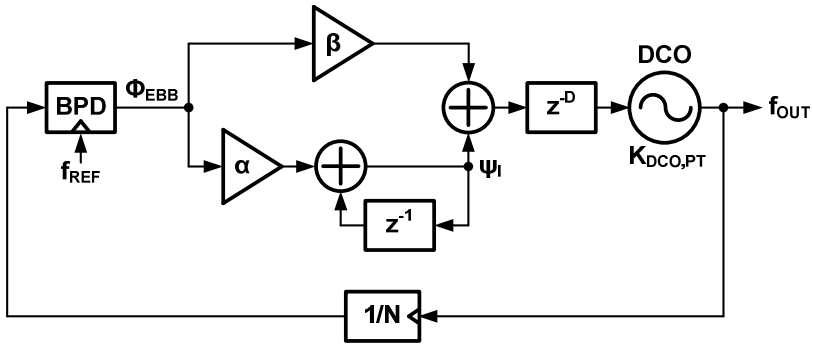
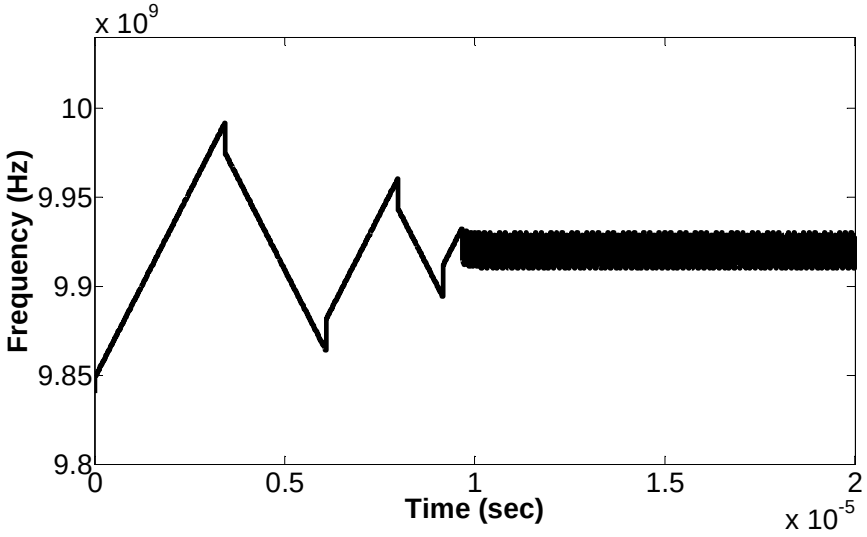


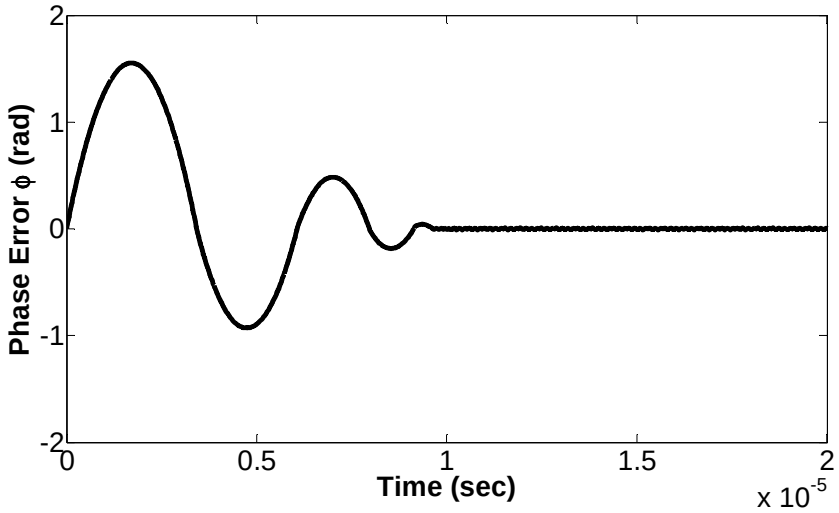
Fig. 3-6 Equivalent system block diagram during bang-bang phase tracking mode.

nonlinear binary phase detector block in the loop, this approach cannot be used for the ADPLL during PT mode. The fundamental aspect of BBPLL is the presence of limit cycles in the loop dynamics. In fact, a BBPLL cannot lock to the reference clock in a traditional sense, where the output of the phase detector and the loop filter voltages settle asymptotically around a fixed value, disturbed only by thermal noise.

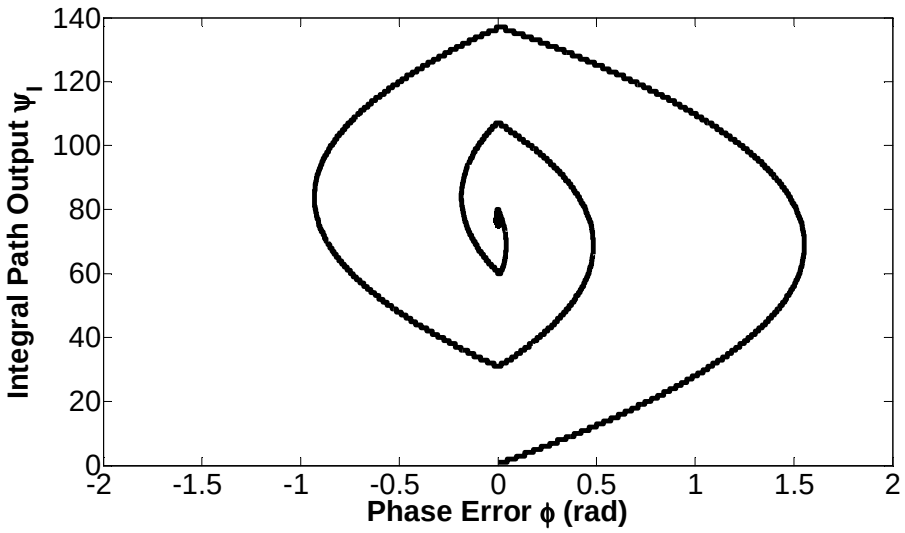
In order to achieve more insight into the BBPLL characteristics before the analytic equations of the loop property are given, some results of the behavior



(a)



(b)



(c)

Fig. 3-7 (a) Simulated output frequency, (b) phase error versus time and (c) the phase plane of the BBPLL.

simulations are shown. Fig. 3-7 shows the simulation results of the locking behavior and the phase plane of a BBPLL with D=0.5, where the phase error φ is the un-quantized phase difference between the reference clock and feedback signal.

It is clear from Fig. 3-7(a) that the BBPLL output frequency oscillates around a fixed value in locked state. The simulated phase plane is shown in Fig. 3-7(c), where the x-axis is the phase error and the y-axis is the integral path output Ψ_I of the loop filter. Since the loop dynamic tends to produce a phase detector output with duty cycle proportional to the loop frequency error when β is much lager the α, the integral path can be viewed as an inner frequency tracking loop [6]. Thus the dynamics of the integral path output Ψ_I can be treated as the behavior of the tracking frequency. When the stability conditions are met, the trajectory converges toward center and then enters a periodic orbit. In order to investigate the loop dynamics of the BBPLL, the time domain based approach proposed in [7] is used. Since only the loop dynamics in the presence of the hard

nonlinearity is interested in this approach, it is assumed that all the PLL building blocks are free from any kind of physical noise source.

By indicating with t_r and t_d the time instants of the rising edges of the reference and divided clocks, respectively, the logical output of the BPD can be express as:

$$\Phi_{EBB} = \mathrm{sgn}(\Delta t), \tag{3-3}$$

where $\Delta t=t_r-t_d$. The DCO can be modeled as a linear block with output clock period T_{OUT} depending linearly on the input control code C_{DCO}:

$$T_{OUT} = T_{DCO,free} - K_T C_{DCO}, \tag{3-4}$$

where $T_{DCO,free}$ is the DCO free running period and K_T is the period gain of the DCO which can be expressed in term of the frequency gain K_{DCO} of the DCO $K_T=-K_{DCO}(T_{DCO,free})^2$.

Fig. 3-8 reveals the time diagram of the BBPLL. By inspecting Fig. 3-6 and Fig. 3-8, the behavior of the BBPLL can be described by the following nonlinear

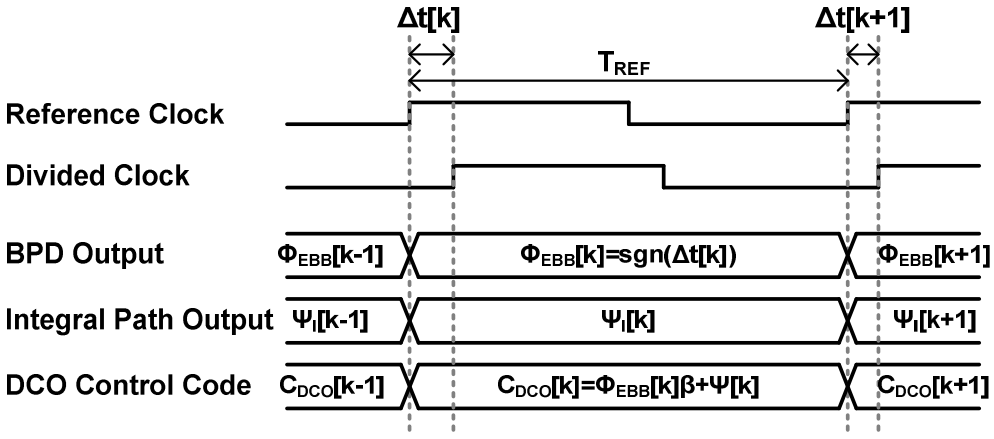


Fig. 3-8 Time diagrams of the signals in the BBPLL (Adapted from [7]).

map:

$$\begin{cases} \Delta t[k+1] = \Delta t[k] + T_{REF} - NT_{DCO,free} - NK_T \Psi_I[k-D] - N\beta K_T \operatorname{sgn}(\Delta t[k-D]) \\ \Psi_I[k+1] = \Psi_I[k] + \alpha \operatorname{sgn}(\Delta t[k+1]) \end{cases} \quad (3\text{-}5)$$

With the definition of the following quantities:

$$\Delta\tau = \frac{\Delta t}{N\beta K_T}$$
$$x_0 = \frac{T_{REF} - NT_{DCO,free}}{N\beta K_T}, \quad (3\text{-}6)$$
$$R = \frac{\alpha}{\beta}$$

equation 3-5 can be rewritten in the following simplified form:

$$\begin{cases} \tau[k+1] = \tau[k] + x_0 - \frac{R}{\alpha}\Psi_I[k-D] - \operatorname{sgn}(\tau[k-D]) \\ \Psi_I[k+1] = \Psi_I[k] + \alpha \operatorname{sgn}(\tau[k+1]) \end{cases}. \quad (3\text{-}7)$$

In equation 3-6, some words are defined. The symbol τ denotes the timing error normalized to the quantization step $N\beta K_T$ of the loop, and x_0 is the normalized difference between the period of the reference clock and the DCO free running period multiplied by N. The value of x_0 is zero only if the two periods are identical which can never be met in a practical BBPLL implementation. However, the assumption $x_0=0$ can be used as a starting point in order to simplify the analysis. It can be proved that a system with $x_0 \neq 0$ is described by the same nonlinear map as a system with $x_0=0$ with offset in Ψ_I-axis. For $x_0=0$, equation 3-7 can be reduced to

$$\begin{cases} \tau[k+1] = \tau[k] - \frac{R}{\alpha}\Psi_I[k-D] - \operatorname{sgn}(\tau[k-D]) \\ \Psi_I[k+1] = \Psi_I[k] + \alpha \operatorname{sgn}(\tau[k+1]) \end{cases}. \quad (3\text{-}8)$$

From this equation, the characteristics of the system can be described using only two state variables, namely τ and Ψ_I.

3.2.2 Stability Conditions of the ADPLL during PT Mode

Next the conditions for stability will be given for ADPLL during PT mode. Due to the presence of the nonlinear BPD, the conditions for stability of a BBPLL can not be derived directly form frequency domain analysis. Instead, the conditions for the BBPLL stability can be described by the existence of the orbit in the phase plane and can be expressed as [7]

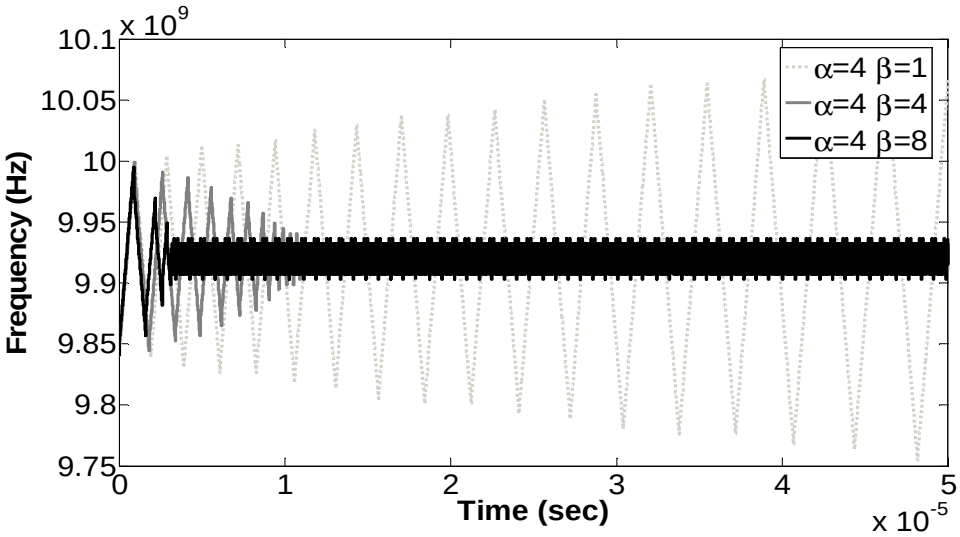
$$R < \frac{2}{2D+1}\ , \qquad (3\text{-}9)$$

which is independent of the multiplied ratio N and DCO frequency gain K_{DCO}. From this equation for a given α, the minimum β is limited to (2D+1)α/2. Thus reducing β or increasing the loop latency would drive the BBPLL toward the instability limit. The conditions and characteristic mentioned above could be confirmed by the simulation results as shown in Fig. 3-9, where the simulations are performed with different combinations of loop parameters.

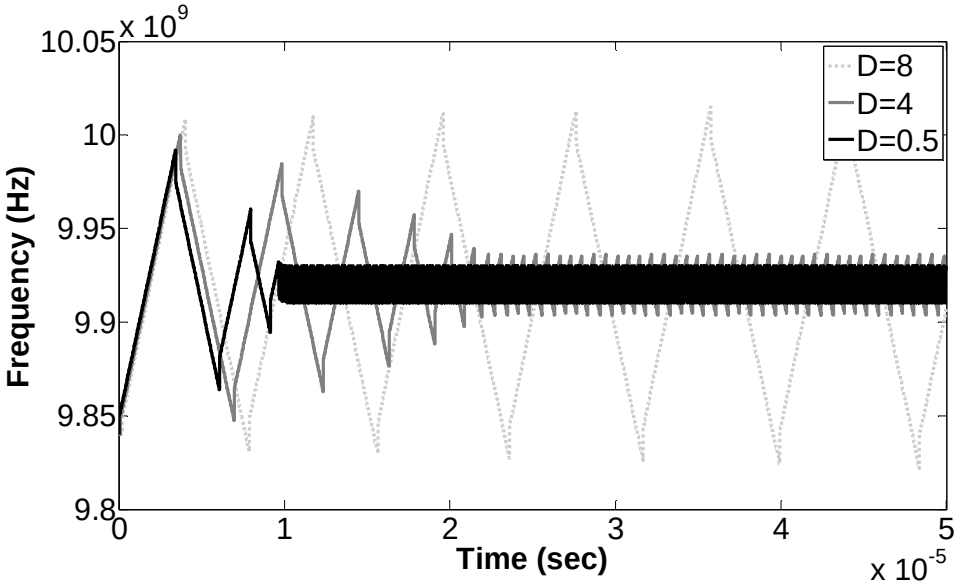
With constant loop delay, larger β tends to improve loop stability and locking speed. With the same loop filter parameters the longer the loop latency, the longer time the loop expends to achieve locked state. Further increasing of the delay will make the loop to diverge. It is worth noting that the BBPLL produces longer duration of the limit cycles with larger D which results in wider frequency variation in steady state.

3.2.3 Locking Range of the ADPLL during PT Mode

The time domain approach proposed in [7] seems to have an unbounded frequency capture range due to the introduced integral path of loop filter as an inner frequency tracking loop. However, the oscillator and phase detector suffers from the limited tuning range and detection range in practical implementations, leading to possibility of false-locking. In other words, the loop may reach



(a)



(b)

Fig. 3-9 Simulated locking behavior of BBPLL with (a) constant delay (D=0.5) and (b) constant α and β (α=1, β=8).

steady-state with the output frequency other than Nf_{REF} in presence of non-idealities of the circuit components.

In order to derive the analytical expressions of the BBPLL locking range, the dynamic range of the phase error is first investigated. Assume that the PAC1 ,PAC2 and the subtracter of the phase detector are all wordlength limited to υ-bits. This limitation carries over to the phase error signal Φ_E. Consequently,

the range of Φ_E signal is $[-2^{(\upsilon-1)}, 2^{(\upsilon-1)}-1]$ and limits the dynamic range of the un-quantized phase error to

$$\Delta\varphi_{range} = 2^{\upsilon} \times \frac{2\pi \times 4}{N} = \frac{2^{(\upsilon+3)}\pi}{N}(rad), \qquad (3\text{-}10)$$

where the phase error is normalized to reference period and the output frequency f_{OUT} is assumed to be Nf_{REF}. More detail of the implementation of the phase detector will be mentioned in section 4-2.

The limited range of the DCO tuning curve also sets another bound during the locking process of the BBPLL. With reference to Fig. 3-10, consider the locking behavior of the BBPLL starting with a initial frequency error Δf_0. The DCO must have a linear tuning characteristic covering the range from Nf_{REF}-Δf_1 to Nf_{REF}+Δf_0 for the loop to be able to successfully lock to the target frequency Nf_{REF}. It can be seen that under the conditions of the stability as expressed in equation 3-9, Δf_0 is larger than or equal toΔf_1. Thus, for a reasonable worst-case estimation, the following equation must be met:

$$Nf_{REF} - \Delta f_0 \le f_{OUT} \le Nf_{REF} + \Delta f_0 . \qquad (3\text{-}11)$$

The conditions expressed in equations 3-10 and 3-11 can be mapping to the

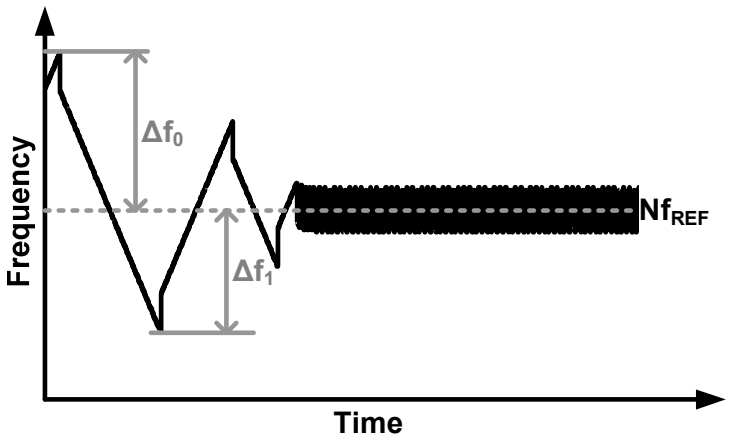


Fig. 3-10 The locking transient of the BBPLL.

boundary for the trajectory in the phase plane as shown in Fig. 3-11. To derive the frequency capture range of the BBPLL, we will select ($\varphi[0],\Psi_I[0]$) as starting condition the point immediately before the trajectory moves into the left half-plane. The trajectory starts from this point and it is assumed that the loop has a initial frequency error Δf_0 which implies $\Psi_I[0]=\Delta f_0/K_{DCO}$. It should be noted that when the trajectory lies on the φ axis ($\Psi_I[M]=0$) at M-th clock cycle, the phase error reaches it maximum negative value which is bounded by the phase detection range:

$$|\varphi[M]| \le \frac{2^{(\upsilon+2)}\pi}{N}. \qquad (3\text{-}12)$$

By inspecting the second equation of equation 3-8, the iteration index M can be expressed as

$$M = \frac{\Delta f_0}{K_{DCO}\alpha}. \qquad (3\text{-}13)$$

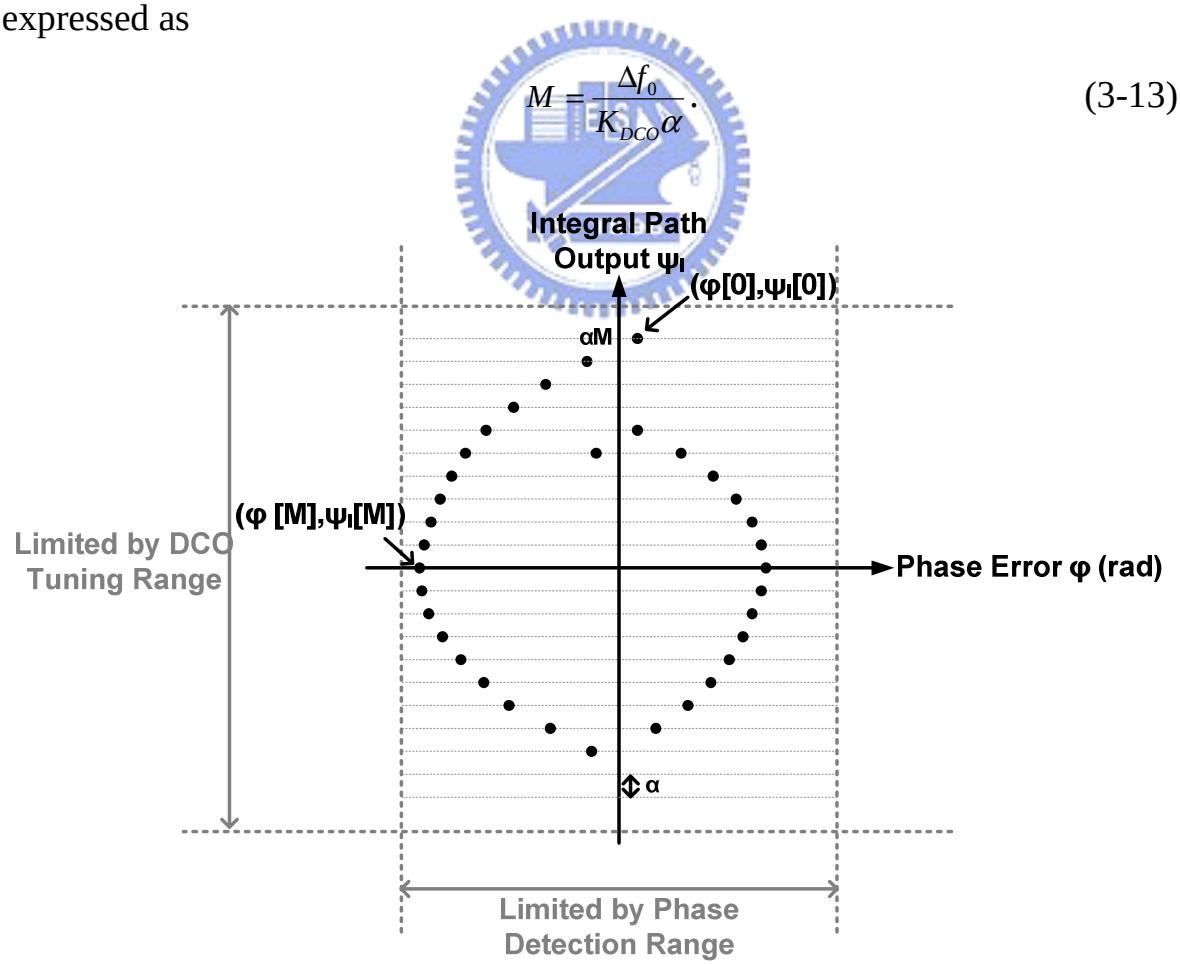


Fig. 3-11 Phase plane illustrating the boundary used to derive the locking range.

In order to calculate the value of φ[M], taking the sum for k=0…i-1 of both members of the first equation of equation 3-8, τ[i] can be written explicitly as [7].

$$\tau[i]=\begin{cases}\tau[0]-iR\left(M-D+\dfrac{1-i}{2\alpha}\right)-i, \text{for } i\le D+1\\ \tau[0]-R\left[iM-D(D+1)+iD+\dfrac{i(1-i)}{2}\right]-2D-2+i, \text{for } i\ge D+2\end{cases} \quad . \text{(3-14)}$$

For simplicity, we assume that the initial phase error is negligibly small which leads to τ[0]=0. By noting that M>D+2 for large initial frequency offset, the value of τ[M] can be rewritten as

$$\tau[M]=-\frac{\alpha}{\beta}\left[\frac{M^2}{2}+\frac{M}{2}-D(D+1)+MD\right]-2D-2+M\ . \qquad (3\text{-}15)$$

Substituting equation 3-12 and 3-13 into 3-15 and noting that $\varphi=2\pi f_{REF}N\beta K_T\tau$ gives

$$\frac{\alpha}{\beta}\left[\frac{1}{2}\left(\frac{\Delta f_0}{K_{DCO}\alpha}\right)^2+\frac{1}{2}\left(\frac{\Delta f_0}{K_{DCO}\alpha}\right)+D\left(\frac{\Delta f_0}{K_{DCO}\alpha}\right)-D(D+1)\right]+2D+2-\left(\frac{\Delta f_0}{K_{DCO}\alpha}\right)\le\frac{2^{(\upsilon+1)}}{N^2 f_{REF}\beta K_T}, \qquad (3\text{-}16)$$

which can be further simplified as

$$\left(\frac{1}{2K_{DCO}{}^2\alpha\beta}\right)\Delta f_0{}^2+\left(\frac{1+2D}{2K_{DCO}\beta}-\frac{1}{K_{DCO}\alpha}\right)\Delta f_0+\left[-\frac{\alpha(D^2+D)}{\beta}+2D+2-\frac{2^{(\upsilon+1)}f_{DCO,free}{}^2}{N^2K_{DCO}\beta f_{REF}}\right]\le 0\ . \qquad (3\text{-}17)$$

Assume that the condition of equation 3-11 is met. Using a MATLAB script, the relation between loop filter parameters and the allowed maximum initial frequency error $\Delta f_{0,max}$ can be solved for a BBPLL having the following parameters corresponding to our design: f_{REF}=40MHz, N=248, D=0.5, and υ=8. Fig. 3-12 shows the result and it can be seen that the locking range is proportional to the gain $K_{DCO}\alpha$ and $K_{DCO}\beta$ as expected.

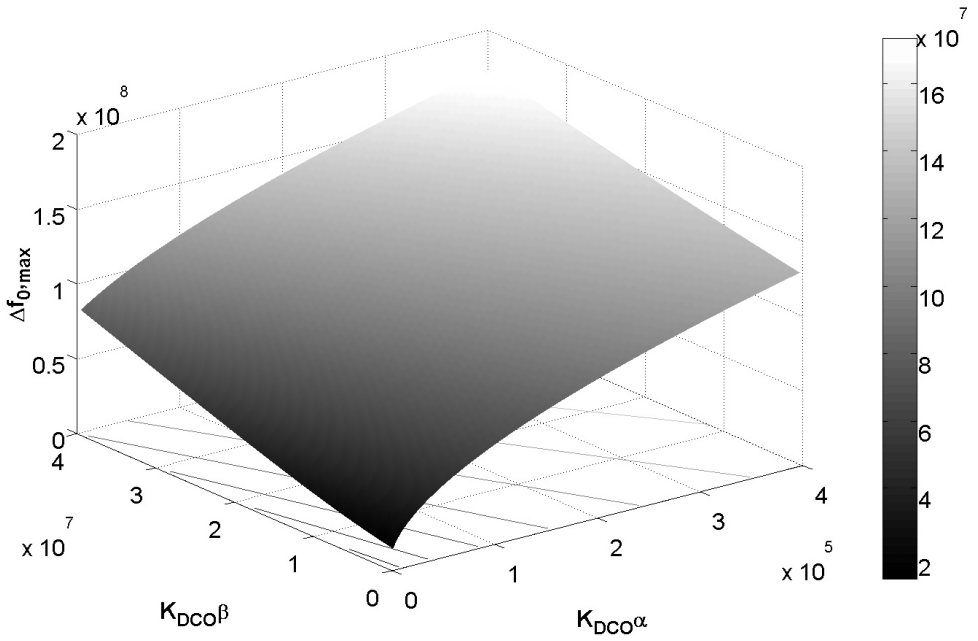


Fig. 3-12 Allowed maximum initial frequency error versus loop parameters $K_{DCO}\alpha$ and $K_{DCO}\beta$ for BBPLL. (f_{REF}=40MHz, N=248, D=0.5, and υ=8.)

3.2.4 Locking Time of the ADPLL during PT Mode

In the session, the locking time of the BBPLL will be calculated. A similar calculation has been already done in [10] for type II BBPLL where the delay introduced on proportional path is negligibly small compared to the period of reference signal. In our case, the locking time of the BBPLL can be calculated in a similar way. The locking time can be obtained from the number of iterations before the trajectory reaches the origin (BBPLL locked). As shown in Fig. 3-13, consider a trajectory starting from the point (0, M_0) and intercepting again the Ψ_I axis in (0, M_1) at the iteration index i. Since the trajectory can be described by the equation 3-14, for a given M_0, the time index i can be found by solving equation 3-14 with $M=M_0/\alpha$:

$$i=\left\lfloor\left(\frac{M_0}{\alpha}+D+\frac{1}{2}-\frac{1}{R}\right)+\sqrt{\left(\frac{M_0}{\alpha}+D+\frac{1}{2}-\frac{1}{R}\right)^2-2\left[D(D+1)-\frac{2D}{R}-\frac{2}{R}\right]}\right\rfloor . \quad (3\text{-}18)$$

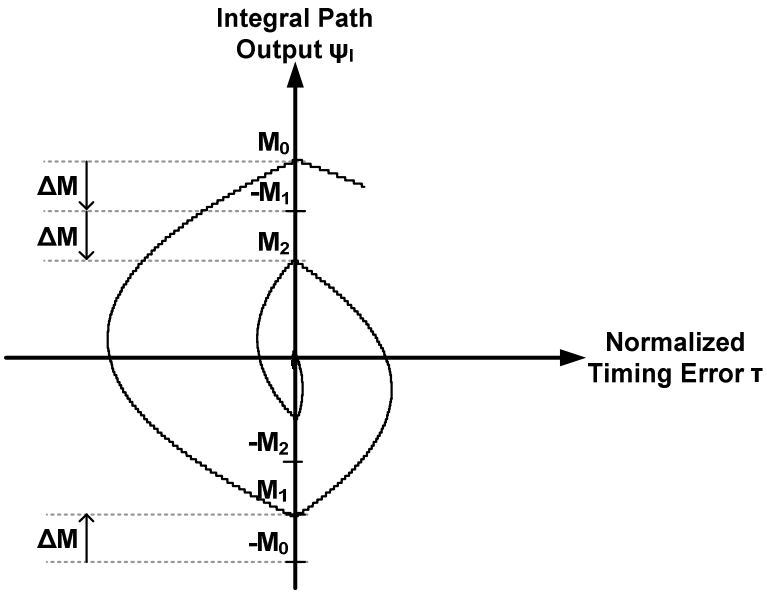


Fig. 3-13 Trajectory plot for the computation of the locking time. (Adapted from [7])

where the operator ⌊x⌋ indicates the biggest integer lower or equal to x. In practical cases

$$\left(\frac{M_0}{\alpha}+D+\frac{1}{2}-\frac{1}{R}\right)^2 >> 2\left[D(D+1)-\frac{2D}{R}-\frac{2}{R}\right], \tag{3-19}$$

so that i can be simplified to:

$$i \approx \left(\frac{2M_0}{\alpha}+2D+1-\left\lfloor\frac{2}{R}\right\rfloor\right). \tag{3-20}$$

The value of M_1 is then can be found by noting that $M_1=M_0-i\alpha$ and from that the reduction of the radius of the trajectory (ΔM) in one half turn around the origin can be obtained:

$$\Delta M = M_0-|M_1| = \left\lfloor\frac{2}{R}\right\rfloor\alpha-(2D+1)\alpha\,. \tag{3-21}$$

As ΔM does not depend on M_0, the decrease of the trajectory radius for every half turn is a constant. Thus, the number of half turns before the trajectory reaches the origin is $M_0/\Delta M$. By inspecting Fig. 3-13, the total number of iterations for the BBPLL to be locked is:

$$n_{tot} = M_0 + 2\sum_{k=1}^{M_0/\Delta M}|M_k| = M_0 + 2\sum_{k=1}^{M_0/\Delta M}|M_0 - k\Delta M| = \frac{M_0^2}{\Delta M}. \quad (3\text{-}22)$$

From above expression, it can be seen that for β>>α, the locking speed is proportional to β. To put this equation into practice, the value M_0 can be related to the initial DCO frequency error $\Delta f_0 = f_{OUT} - Nf_{REF}$ as

$$M_0 = \frac{\Delta f_0}{K_{DCO}}. \quad (3\text{-}23)$$

In order to evaluate the expression above, consider a BBPLL with the following parameters: Δf_0=6MHz, K_{DCO}=20kHz, α=1, β=32, D=0.5 and f_{REF}=40MHz. From equation 3-23 and 3-21, M_0=300 and ΔM=62. By substituting these values into equation 3-22, the total reference clock cycles needs to lock is n_{tot}=1452 cycles. This corresponds to a locking time of 36.3μs. From Fig. 3-14, it can be seen that the agreement between the estimation and the simulated locking time is quite satisfying.

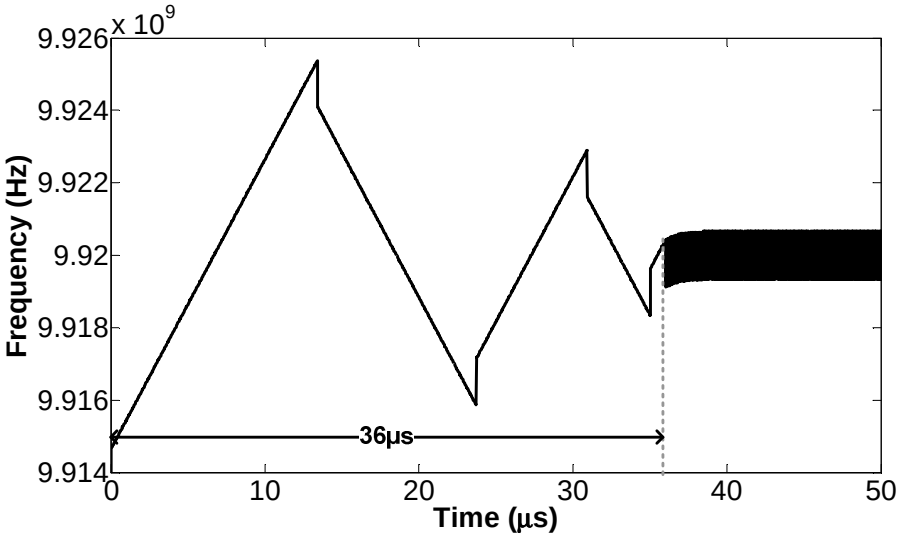


Fig. 3-14 Simulation result of DCO output frequency versus time during locking process of BBPLL. (Δf_0=6MHz, K_{DCO}=20kHz, α=1, β=32, D=0.5 and f_{REF}=40MHz.)

3.2.5 Input jitter tolerance of the ADPLL during PT Mode

Since the output of the phase detector during phase tracking can be either +1 or -1, the feedback clock period rate of change is limited to $NK_T\alpha$ per clock cycle. This indicates that the BBPLL has an intrinsic limited capability of tracking a reference clock whose period is changing with time. If the rate of the change of the reference frequency is larger than this limit, the loop will go into slew-rate limitation, losing its lock condition. Consider a reference clock f_R with a sinusoidal modulating signal.

$$f_R(t) = f_{R0} + A_{\text{mod}} \cos(\omega_{\text{mod}} t), \tag{3-24}$$

where A_{mod} and ω_{mod} are the modulation amplitude and the modulation angular frequency, respectively. The maximum frequency amplitude that the BBPLL can track can be expressed as [10]

$$A_{\text{mod}} < \max\left\{ \frac{\alpha K_{DCO} f_{R0}}{\omega_{\text{mod}} N}, \frac{\beta K_{DCO}}{N} \right\}. \tag{3-25}$$

From equation 3-24, the phase of the FM signal is

$$\theta(t) = 2\pi f_{R0} t + \frac{2\pi A_{\text{mod}}}{\omega_{\text{mod}}} \sin(\omega_{\text{mod}} t). \tag{3-26}$$

Thus, the resulting signal is

$$S_{FM}(t) = A\sin\left[2\pi f_{R0} t + \frac{2\pi A_{\text{mod}}}{\omega_{\text{mod}}} \sin(\omega_{\text{mod}} t) \right]. \tag{3-27}$$

Assume that $2\pi A_{\text{mod}} << \omega_{\text{mod}}$. Equation (14) could be rewritten after some trigonometric expansion as follows:

$$S_{FM}(t) \approx A\cos(2\pi f_{R0} t) - \frac{2\pi A_{\text{mod}}}{\omega_{\text{mod}}} A\sin(\omega_{\text{mod}} t)\sin(2\pi f_{R0} t). \tag{3-28}$$

Expanding the above expression into phasor form, we can get

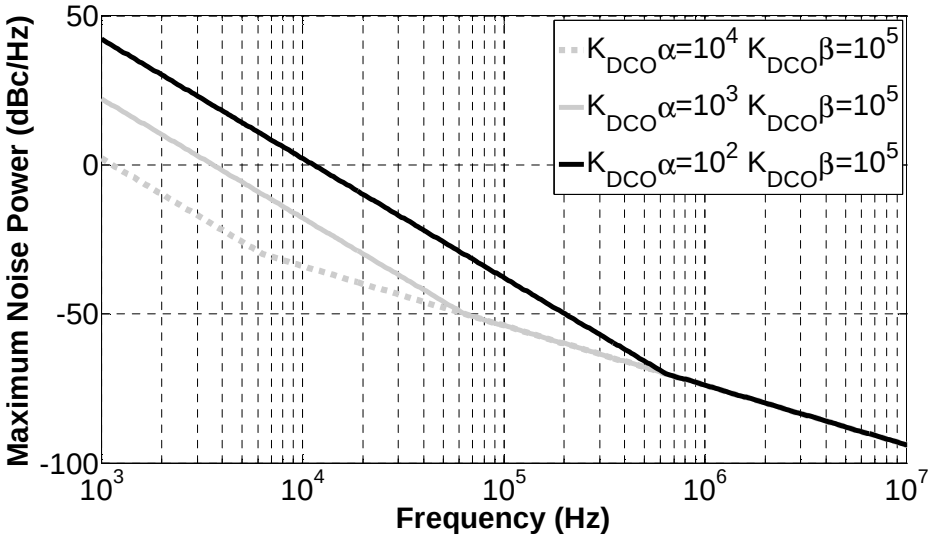


Fig. 3-15 Maximum input noise power sufficient to cause slew-limiting as a function frequency and with $K_{DCO}\alpha$ as a parameter.

$$S_{FM}(t) \approx \Re\left\{ Ae^{j2\pi f_{R0}t}\left(1+\frac{\pi A_{\text{mod}}}{\omega_{\text{mod}}}e^{j\omega_{\text{mod}}t}-\frac{\pi A_{\text{mod}}}{\omega_{\text{mod}}}e^{j\omega_{\text{mod}}t}\right)\right\}. \qquad (3\text{-}29)$$

From equation 3-29, it is clear that A_{mod} can be mapping to the sidebands with power $20\log(2\pi A_{mod}/\omega_{mod})$ dB below the main carrier tone. In this way, we can define the minimum value of $K_{DCO}\alpha$ and $K_{DCO}\beta$ for a given input phase noise. Fig. 3-12 illustrates the limit of the input noise power versus frequency with different $K_{DCO}\alpha$ value.

3.3 Output Noise Performance of the ADPLL

After the rapid frequency acquisition, the ADPLL will finally reach a steady-state condition in the bang-bang phase tracking mode. The output noise performance in locked state including the spurs, timing jitter and output phase will be investigated. In particular the spur emission will be derived using the

nonlinear model, while the output phase noise performance in the present of internal and external noise source will be analyzed with the help of the linear model.

3.3.1 Output Spur

Due to the presence of the limit cycles or orbit in the dynamics of the BBPLL, the output clock f_{OUT} is frequency modulated by a periodic control signal in locked state, leading to spurious tone emission.

To gain more insight into the loop dynamics, consider the BBPLL which is free from any internal or external noise source and has the following parameters: f_{REF}=40MHz, α=1, β=128, K_{DCO}=500, D=0.5 and N=248. Fig. 3-16(a) shows the simulation result of the output frequency versus time in the locked state of the BBPLL with above setting. The result shows that the modulating signal of the carrier is similar to a square wave with some ripples and the modulating rate is equal to $1/4f_{REF}$.

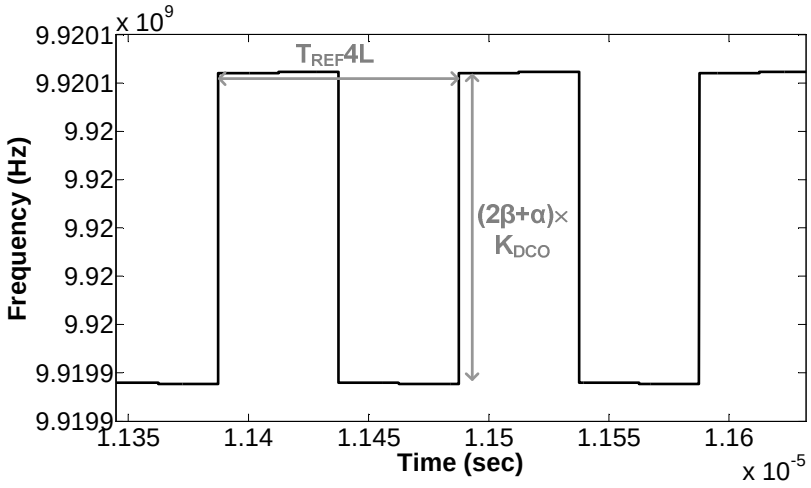
Under the assumption of narrow-band frequency modulation, the power level of the spurious tones compared to the carrier can be approximated as [4]:

$$P_{spur} = 20\log\left(\frac{1}{2}\beta\right)(\text{dBc}), \qquad (3\text{-}30)$$

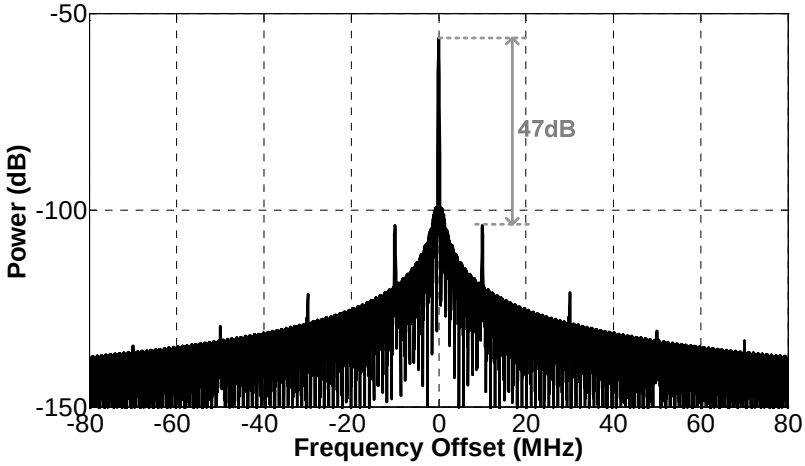
where β is modulation index defined as the ratio of the frequency deviation Δω to the frequency of the modulating wave ω_m in a frequency modulation system when using a sinusoidal modulating wave. However, for a symmetric square wave with frequency of ω_m as the modulating input, it can be expressed in the following Fourier series representation:

$$g_{square}(t) = \sum_{n=1.odd}^{\infty} \frac{2}{\pi}\frac{1}{n}\sin n\omega_m t\,. \qquad (3\text{-}31)$$

The modulation index of the nth harmonic for the Fourier series decomposition of a square modulating wave becomes:



(a)



(b)

Fig. 3-16 (a) The simulation results of the output frequency versus time and (b) the output spectrum in locked state of the ADPL with the following parameters: f_{REF}=40MHz, α=1, β=128, K_{DCO}=500, D=0.5 and N=248.

$$\beta_n = \frac{2}{\pi n}\frac{\Delta\omega_{pp}}{n\omega_m}. \tag{3-32}$$

It should be noted that in most cases, only the fundamental component (n=1) would really matter. Under the condition that β>>α, the BBPLL output can be approximated as a frequency modulation signal with a square wave as the

modulating input. By inspection of Fig. 3-6, the peak to peak frequency deviation is given as

$$\Delta\omega_{pp} = 2\pi(2\beta+\alpha)K_{DCO}\,. \tag{3-33}$$

From [7], the modulation rate of the BBPLL output is

$$\omega_m = 2\pi\frac{f_{REF}}{4L}, \tag{3-34}$$

where L is the integer value satisfying the following conditions:

$$\frac{D(2+R-RD)}{2+R-2RD} \le L \le \frac{(2-RD)(D+1)}{2-R-2RD}. \tag{3-35}$$

An inspection of equation 3-32, 3-33 and 3-34 reveals that larger βK_{DCO} and D will result in larger $\Delta\omega_{pp}$ and smaller ω_m, thus increasing the power level of the spurs.

As the example shown in Fig. 3-16, substituting α=1, β=128, K_{DCO}=500, and D=0.5 into equation 3-33 and 3-34, we obtain $\Delta\omega_{pp}=2\pi(1.28\times10^5)$ rad and $\omega_m=2\pi(1\times10^7)$ rad. If the first harmonic in the Fourier series decomposition is considered, substituting n=1 into equation 3-32 we can get $\beta_1=8.14\times10^{-3}$ This gives rise to spurs 10 MHz away on both sides from the oscillating frequency. Their power level is at

$$P_{spur} = 20\log\left(\frac{1}{2}\beta_1\right) = \text{-47.8 dB}, \tag{3-36}$$

relative to the main carrier tone. In Fig. 3-16(b), the simulated output spectrum is shown and the expression above is confirmed. It should be noted that the analysis is performed under the noise-free assumption. Obviously, this is not a practical case. In fact, the noise will randomize the spurious energy.

3.3.2 The Linear Model of the ADPLL during PT Mode

Although the nonlinear model has been helpful to find the stability criterion and general properties of the trajectories, this approach can not successfully describe

the output noise performance under the more realistic assumptions of the presence of internal and external noise sources. A different approach will be demonstrated in the following sections. A continue-time linear model will build for the ADPLL during bang-bang phase tracking mode. Then the system transfer function will be derived to estimate the performance of the loop.

From the system architecture shown in Fig. 3-6, the difficulty to build the linear model for this system is the hard nonlinearity introduce by the binary phase detector. An approach for modeling the binary phase detector is reported in [8] where the phase detector is modeled as a linear block with a gain K_{bpd} as illustrated in Fig. 3-17. The symbol $\Delta t=t_r-t_d$ is the difference between the rising edges instants of the reference (t_r) and feedback clock (t_d). It is clear that in the locked state, the average value of the BPD output $E[\Phi_{EBB}]$ converges to 0. Assume that for some reason the probability distribution of Δt is shifted away from its equilibrium point by a small amount η in the positive direction. In this case the average value of Φ_{EBB} will be slightly positive. Following this circumstances, the phase detector gain can be defined as the rate of change in $E[\Phi_{EBB}]$ due to a small shift η of the probability density function (pdf) around the locked condition:

$$K_{bpd} \equiv \frac{\partial}{\partial \eta}\left(E[\Phi_{EBB} \mid shift = \eta]\right)\Big|_{\eta \to 0^+} . \qquad (3\text{-}37)$$

Under this definition, the value of K_{bpd} can be approximated as:

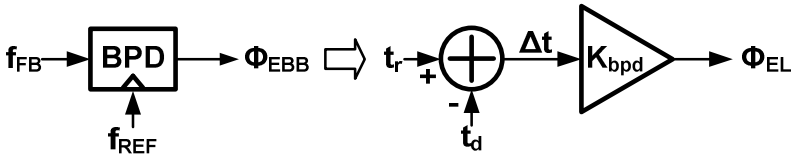


Fig. 3-17 BPD linearized model.

$$K_{bpd} = 2 f_{\Delta t}(0), \tag{3-38}$$

where $f_{\Delta t}$ denotes the pdf of Δt.

In this derivation we will assume $\alpha << \beta$. When the PLL is locked, the integral path will have centered the dynamics so that in equation 3-5 we can assume

$$T_{REF} - NT_{DCO,free} - NK_T \Psi[k-D] = 0. \tag{3-39}$$

Thus the nonlinear map in the presence of jitter on the reference and DCO clock can be written as:

$$\Delta t[k+1] = \Delta t[k] + t_j - N\beta K_T \operatorname{sgn}(\Delta t[k-D]), \tag{3-40}$$

where t_j is the timing jitter appeared on reference clock. To emphasize the fact that the loop has a non-integer loop delay of D=0.5, the above expression is rewritten as:

$$\Delta t[k+1] = \Delta t[k] + t_j - \frac{1}{2} N\beta K_T [\operatorname{sgn}(\Delta t[k]) + \operatorname{sgn}(\Delta t[k-1])]. \tag{3-41}$$

If it is assumed that $\Delta t[0]=0$ and the values of Δt in the case of unjittered reference and DCO clock is Δt^*,Δt^* can assume values only on discrete states:

$$\Delta t^* = nN\beta K_T, n \in Z \tag{3-42}$$

The probability occupancy of the state n ($\Delta t^* = nN\beta K_T$) is defined as:

$$q_n \equiv P[\Delta t^* = nN\beta K_T], \tag{3-43}$$

then the pdf of Δt, $f_{\Delta t}$, will be given by the superposition of the pdfs of t_j, shifted by an amount equal to each occupied state and weighted by the probability of that in steady-state

$$f_{\Delta t}(a) = \sum_{n=-\infty}^{n=+\infty} q_n f_{t_j}(a - nN\beta K_T). \tag{3-44}$$

In general, the f_{tj} can be modeled as a Gaussian process with variance σ_{tj}^2 where σ_{tj}^2 denotes the jitter variance of reference clock. In formulas

$$f_{t_j}(x) = \frac{1}{\sigma_{t_j}\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{x}{\sigma_{t_j}}\right)^2\right]. \quad (3\text{-}45)$$

In order to find $f_{\Delta t}$, a statistical approach is used as following to obtain the value of q_n. From a given state n, Δt^* might go to state n+1, state n-1 or state n itself, and the transition probabilities from state m to state n is defined as

$$P_{m,n} \equiv P\left[\Delta t_{k+1}^* \in n \mid \Delta t_k^* \in m\right]. \quad (3\text{-}46)$$

Under the assumption that σ_{tj} is much smaller than loop quantization step $N\beta K_T$, the states n with |n|>2 occur with a probability which is negligibly small. Then the state diagram of the system describe in equation 3-41 can be simplified to a three state chain as illustrated in Fig. 3-18.

If $f_{\Delta t}$ is symmetrical around 0 then $q_{-1}=q_1$, $P_{0,1}=P_{0,-1}=1/4$ and $P_{0,0}=1/2$. For the case that the loop stays in the same state at the next time index, there exist two possible situations. For example, it might go from state 0 to state 1 at time index k and stay in state 1 at the next time instance k+1 when $\Delta t_{k-1}<0$. Also, it might start from state 1 at the previous time instance k-1 and stay in state 1 at time index k. However, in this case it can never stay in state 1 at next clock cycle. Thus, by inspection of equation 3-41 and noted that $\sigma_{tj}<<N\beta K_T$,

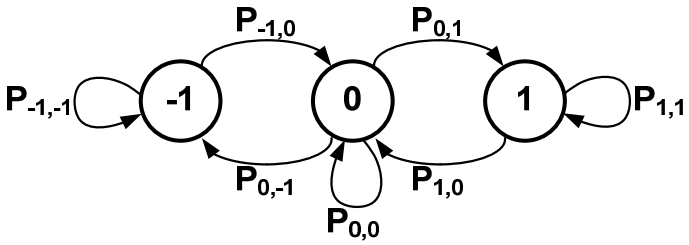


Fig. 3-18 State chain to approximating the BBPLL.

$$P_{1,1} = P_{-1,-1} = \frac{\frac{q_0}{2}}{q_0 + q_1}. \tag{3-47}$$

In the same way, we can find

$$P_{1,0} = \frac{\frac{q_0}{2} + q_1}{q_0 + q_1}. \tag{3-48}$$

To obtain the relationship between the state probability and transition probability, note that q_0 can be expressed as:

$$q_0 = q_{-1}P_{-1,0} + q_0P_{0,0} + q_1P_{1,0} = 2q_1P_{1,0} + q_0P_{0,0} \tag{3-49}$$

Since the states describe all possible events and they are disjoint, they must satisfy the normalization equation

$$q_{-1} + q_0 + q_1 = 1. \tag{3-50}$$

From equation 3-48, 3-49 and 3-50, we can obtain $q_{-1}=q_0=q_1=1/3$.Substituting these values into equation 3-44 and 3-45 and using the definition of equation 3-38, the equivalence gain of the binary phase detector is

$$K_{bpd} \approx \frac{1}{\sigma_{tj}\sqrt{2\pi}}\left[\frac{2}{3} + \frac{4}{3}e^{-\frac{1}{2}\left(\frac{N\beta K_T}{\sigma_{tj}}\right)^2}\right] \tag{3-51}$$

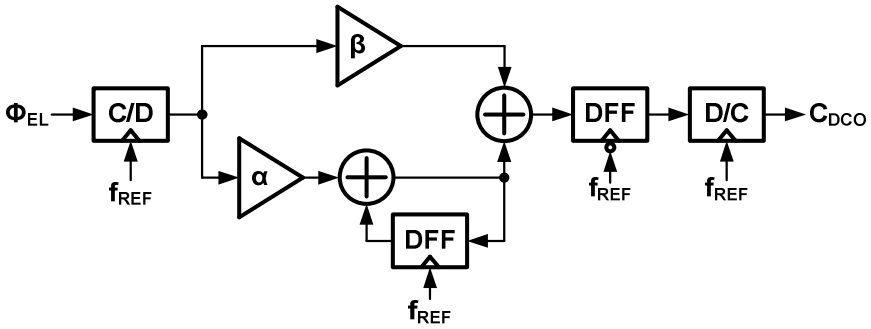
It should be noted that the above gain expression is defined in the unit of (sec)-1. It can be simply converted to the expression in the unit of $(rad)^{-1}$ by applying the relationship

$$K_{bpd,\varphi} = \frac{K_{bpd}}{2\pi f_{REF}}, \tag{3-52}$$

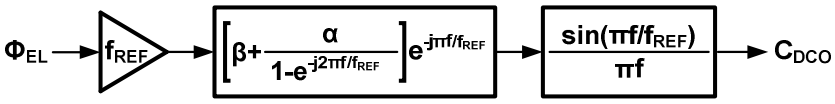
so that

$$K_{BPD,\varphi} \approx \frac{1}{\sigma_{tj}(2\pi)^{\frac{3}{2}} f_{REF}}\left[\frac{2}{3} + \frac{4}{3}e^{-\frac{1}{2}\left(\frac{N\beta K_T}{\sigma_{tj}}\right)^2}\right]. \tag{3-53}$$

Fig. 3-19(a) and Fig. 3-19(b) show the discrete time model and the corresponding continuous time approximation of the digital loop filter, respectively. Before the phase error output Φ_{EL} of the linearized phase detector is sent to the digital loop filter, the continuous-time signal Φ_{EL} is first sampling by the reference clock, which is indicated with the continuous-to-discrete-time (C/D) block. Assume that Φ_{EL} is a band-limited signal and the effect of aliasing is negligible. Then the sampling process can be replaced by a simple gain factor f_{REF}. In the discrete-time IIR filter, the delay in the loop is modeled by the z^{-1} operator defined as $z=\exp(j2\pi f/f_{REF})$. In Fig. 3-19(a), the signal reconstruction process is represented as a discrete-to-continuous-time (D/C) block. Obviously the DCO holds the frequency constant until the digital loop filter changes its output value. Consequently, the output sequence of the digital filter is reconstructed by the zero-order-hold operation which can be expressed as a sinc function in frequency domain. Finally, the approximated frequency response of



(a)



(b)

Fig. 3-19 (a) Discrete time model and (b) continuous time approximation of the digital loop filter.

the digital loop filter is

$$H_{LF}(f)=\frac{\sin\left(\frac{\pi f}{f_{REF}}\right)}{\left(\frac{\pi f}{f_{REF}}\right)}\left(\beta+\frac{\alpha}{1-e^{-j2\frac{\pi f}{f_{REF}}}}\right)e^{-j\frac{\pi f}{f_{REF}}}. \qquad (3\text{-}54)$$

Fig. 3-20 shows the complete model of the ADPLL during bang-bang phase tracking mode, which is obtained by substituting the different building blocks in Fig. 3-6 with their linear models. The DCO is modeled as integration operation with a gain $2\pi K_{DCO}$. The relationship between the phase of the output signal φ_{OUT} and feedback clock φ_{FB} is established by the division (1/N) block. The deviation of the loop transfer functions will be done according to the linear model and the phase noise performance will be analyzed later.

3.3.3 Generated Timing Jitter and Phase Noise

In general, the major noise sources of PLL are the external reference input noise and the internal oscillator natural noise. However, due to the presence of the bang-bang phase detector, the noise introduced by the quantization operation must be taken into consideration.

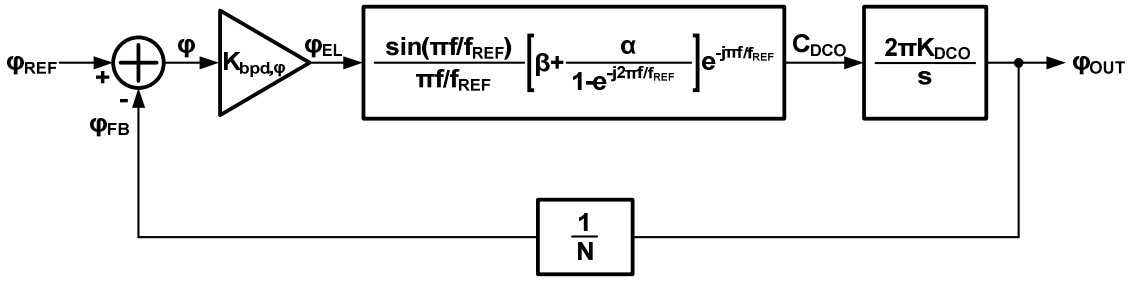


Fig. 3-20 Complete linearized model of the ADPLL during bang-bang phase tracking mode.

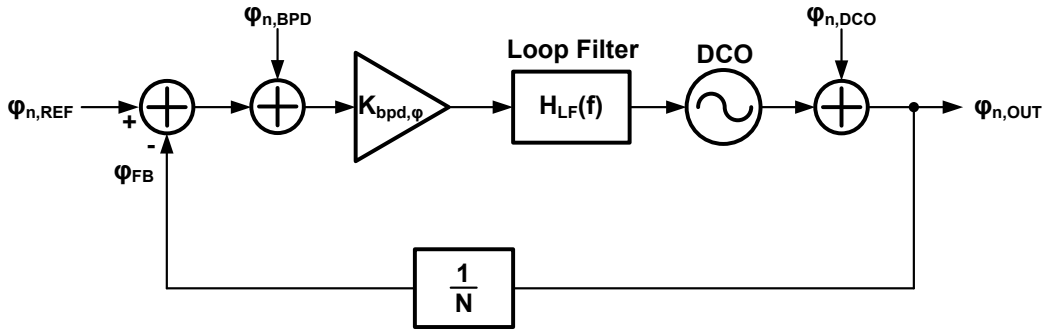


Fig. 3-21 Simplified linearized model of the ADPLL during bang-bang phase tracking mode with internal and external noise sources.

In Fig. 3-21 the linearized model of the ADPLL is illustrated again including the internal and external noise sources. In particular $\varphi_{n,REF}$ is the phase noise on the input reference clock, $\varphi_{n,BPD}$ is the input referred noise due to the quantization of the binary phase detector, and $\varphi_{n,DCO}$ is the phase noise on the DCO output produced by itself. It should be noted that only the deviation to their nominal value are considered for all the quantities in the analysis.

To find the total output noise of the ADPLL, the expression of the power spectral density (PSD) of each noise source is required. Since the signal generator is used for generating the reference clock in the practical implementation of the ADPLL, the phase noise PSD of the reference clock can be estimated as following expression according to the signal generator specifications [9]. The PSD of reference clock is estimate as:

$$S_{\varphi_{n,REF}}(\Delta f) = \text{-}132\ (\text{dBc/Hz}). \tag{3-55}$$

In our analysis, the BPD is modeled as a linear block with a gain $K_{bpd,\varphi}$. In order to emulate the quantization effect of the BPD, a input refer jitter is introduced and defined as

$$\varphi_{n,BPD} = \frac{\text{sgn}(\Delta\varphi) - K_{bpd,\varphi}\Delta\varphi}{K_{bpd,\varphi}} = \frac{\text{sgn}(\Delta\varphi)}{K_{bpd,\varphi}} - \Delta\varphi. \tag{3-56}$$

To find the total output phase noise, an approximation of the PSD of $\varphi_{n,BPD}$ is needed. In general, if the jitter of the reference clock is small compared to the BBPLL quantization step NBK_T, the BBPLL behaves like a first order ΔΣ modulator having a one bit quantizer with step $2N\beta K_T$. Thus, $\varphi_{n,BPD}$ can be approximated as a white process with uniform distribution and variance $(2N\beta K_T)^2/12$. However, if the jitter of the reference clock increases, the ΔΣ loop will be overload and result in slewing [10]. Therefore the variance of $\varphi_{n,BPD}$ will increase. To obtain the expression of its variance for larger input jitter, the approach proposed in [10] is resorted to simulation results. It shows that the jitter introduced by the BPD has a standard deviation which is roughly 3/4 of the standard deviation of the input jitter. From the above discussion, the PSD of the noise produce by the BPD can be defined as [10]

$$S_{\varphi_{n,BPD}}(\Delta f) = \max\left\{\frac{(2\pi)^2 f_{REF}(N\beta K_T)^2}{3}, \left(\frac{3}{4}\right)^2 S_{\varphi_{n,REF}}(\Delta f)\right\} \qquad (3\text{-}57)$$

Finally, the phase noise of the DCO $\varphi_{n,DCO}$ and its PSD will be derived. Although the profile of the DCO phase noise can be easily obtained from simulation results, the analytic approximation may give more insight about the generation of phase noise in the circuit design phase. Consider the differential LC tank cross-coupled pair oscillator. The generated phase noise can be express as [11]

$$S_{\varphi_{n,DCO}}(\Delta f) = \frac{\overline{i_n^2}/\Delta f}{q_{\max}^2}\frac{\Gamma_{rms}^2}{8\pi^2\Delta f^2}, \qquad (3\text{-}58)$$

where $\overline{i_n^2}/\Delta f$ is the PSD of the equivalent parallel current noise, Γ_{rms} is the rms value of the impulse sensitivity function (ISF) associated with that noise source, q_{max} is the maximum signal charge swing which is defined as the product of the

tank capacitance and maximum signal swing $C_{tank}V_{swing}$, and Δf is the the offset frequency from the carrier.

In a simplified stationary approach, the total noise power of the tank is mainly due to the cross-coupled transistor pair and the ohmic losses in the tank inductor:

$$\overline{i_n^2}/\Delta f \approx 2kT\gamma\mu_n C_{ox}\frac{W}{L}V_{ov} + \frac{4kT}{R_p}, \tag{3-59}$$

where $R_p \approx 2\pi f_{osc} L_{tank} Q$ is the equivalent parallel resistance at the frequency of oscillation f_{osc}, T is the temperature, k is Boltzmann constant, μ_n is the mobility of the carriers in the channel, C_{ox} is the oxide capacitance per unit area, W and L are the width and length of the MOS transistor, respectively, and V_{ov} is the gate drive of the MOS transistor. γ, however, may be between two and three in the short-channel devices. For simplicity, the output waveform can be assumed to be a sinusoidal waveform so that $(\Gamma_{rms})^2$ equals to 0.5 [11].

From the model shown in Fig. 3-21, it is straightforward to calculate the total output phase noise by summing the contributions of the different noise sources:

$$S_{\varphi_{n,OUT}}(\Delta f) = \left(S_{\varphi_{n,REF}}(\Delta f) + S_{\varphi_{n,BPD}}(\Delta f)\right)\cdot\left|H_{REF,OUT}(\Delta f)\right|^2 + S_{\varphi_{n,DCO}}(\Delta f)\cdot\left|H_{DCO,OUT}(\Delta f)\right|^2. \tag{3-60}$$

$H_{REF,OUT}(\Delta f)$ and $H_{DCO,OUT}(\Delta f)$ denote the transfer function from reference signal to PLL output and from DCO output to PLL output which can be found by inspecting Fig. 3-21. Thus the transfer functions are

$$H_{REF,OUT}(\Delta f) = \frac{H(\Delta f)}{1 + \frac{H(\Delta f)}{N}}, \tag{3-61}$$

and

$$H_{DCO,OUT}(\Delta f) = \frac{N}{N + H(\Delta f)}, \tag{3-62}$$

where

$$H(\Delta f)=\frac{K_{DCO}K_{BPD,\varphi}\sin\left(\frac{\pi\Delta f}{f_{REF}}\right)}{j\Delta f\left(\frac{\pi\Delta f}{f_{REF}}\right)}\left(\beta+\frac{\alpha}{1-e^{-j2\frac{\pi\Delta f}{f_{REF}}}}\right)e^{-j\frac{\pi\Delta f}{f_{REF}}}. \qquad (3\text{-}63)$$

As an example, Fig. 3-22 shows the transfer functions and the output phase noise for the case with following loop parameters: f_{REF}=40MHz, N=248, $K_{DCO}\beta$=19200, $K_{DCO}\alpha$=300, DCO free running frequency is 9.92 GHz. The DCO is assumed to have a LC oscillator with tank quality factor of 8, 1.2nH inductor, 0.8V output swing. To ensure oscillation, the cross-coupled pair transistors have their size of W=2μm and L=0.08μm. The result shows the loop bandwidth is about 150kHz. The result also reveals that the output phase noise at lower frequency is dominated by reference noise while it is affected by both DCO phase noise and reference noise at higher frequency.

In order to validate the expressions for the output phase noise obtained from the linearized theory, the results of the Simulink model are compared to the analytical expression. From Fig. 3-23 to Fig. 3-28 report the results of the simulations. It can be seen that the agreement between theory and simulation is good for most cases, excluding the one shown in Fig. 3-26. There is already a noticeable difference, meaning that in this case the dynamics of the BBPLL determines the output phase noise in a nonlinear way. By inspecting Fig. 3-23, Fig. 3-24 and Fig. 3-25, it can be noted that with constant $K_{DCO}\alpha$, larger $K_{DCO}\beta$ can result in boarder loop bandwidth. However, increasing $K_{DCO}\alpha$ and keeping $K_{DCO}\beta$ unchanged will drive the loop toward the instability border and generate peaking on the output PSD. Therefore, in order to achieve better jitter performance, $K_{DCO}\alpha$ should be minimized.

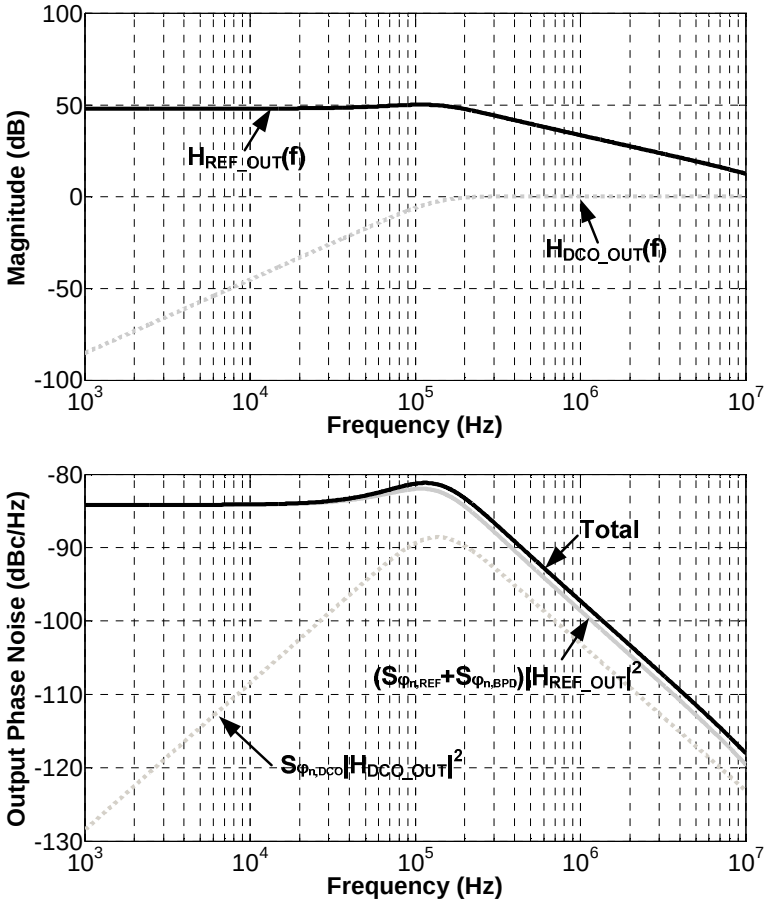


Fig. 3-22 Example computation of ADPLL transfer functions and contribution of each noise source.

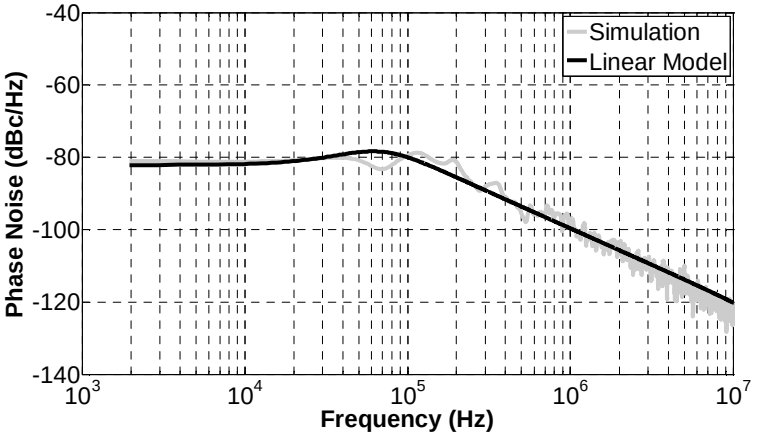


Fig. 3-23 Output phase noise with $K_{DCO}\alpha=3\times10^{2}$ and $K_{DCO}\beta=3.84\times10^{4}$.

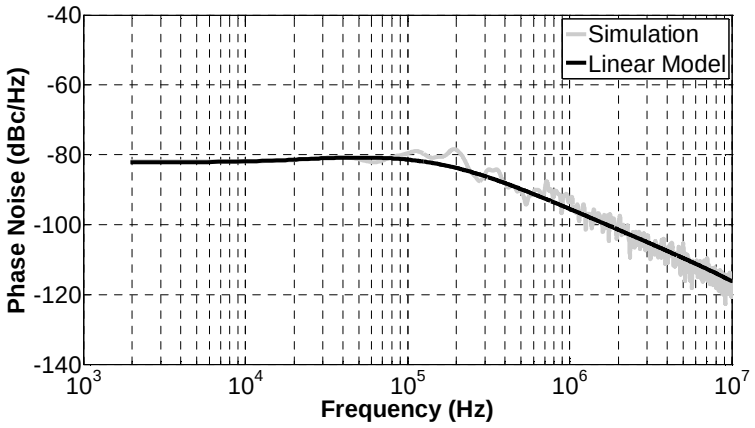


Fig. 3-24 Output phase noise with $K_{DCO}\alpha=3\times10^2$ and $K_{DCO}\beta=7.68\times10^4$.

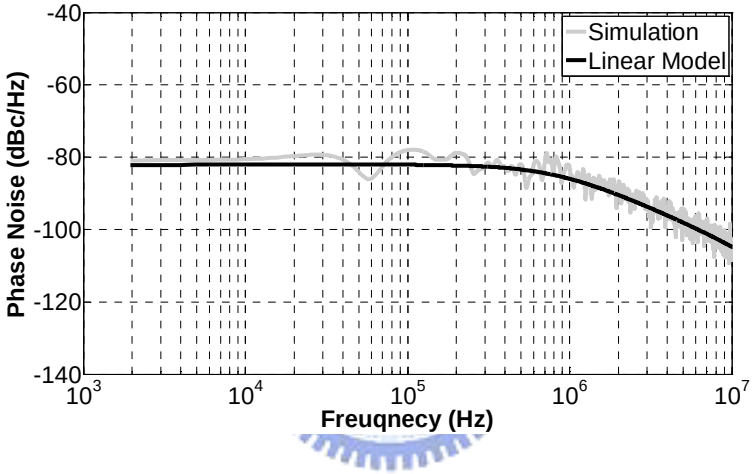


Fig. 3-25 Output phase noise with $K_{DCO}\alpha=3\times10^2$ and $K_{DCO}\beta=3.07\times10^5$.

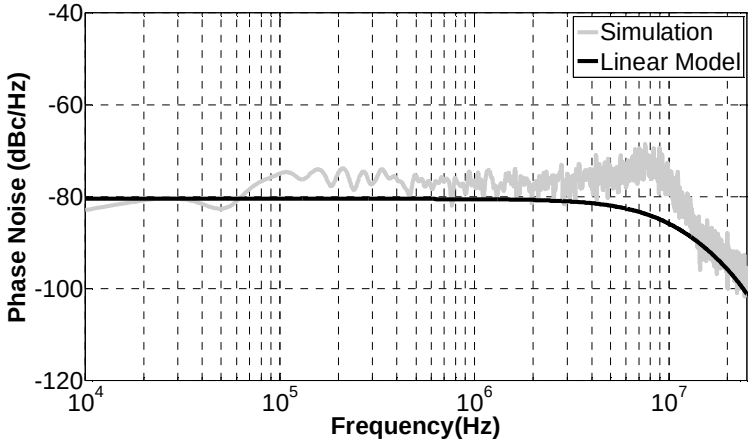


Fig. 3-26 Output phase noise with $K_{DCO}\alpha=3\times10^2$ and $K_{DCO}\beta=4.9\times10^6$.

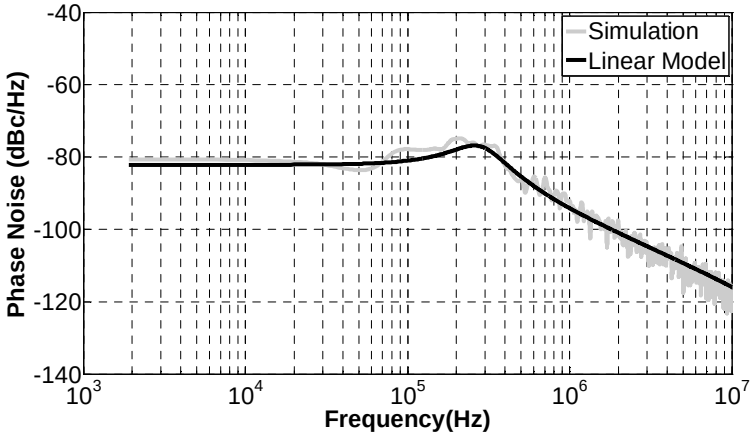


Fig. 3-27 Output phase noise with $K_{DCO}\alpha=4.8\times10^3$ and $K_{DCO}\beta=7.68\times10^4$.

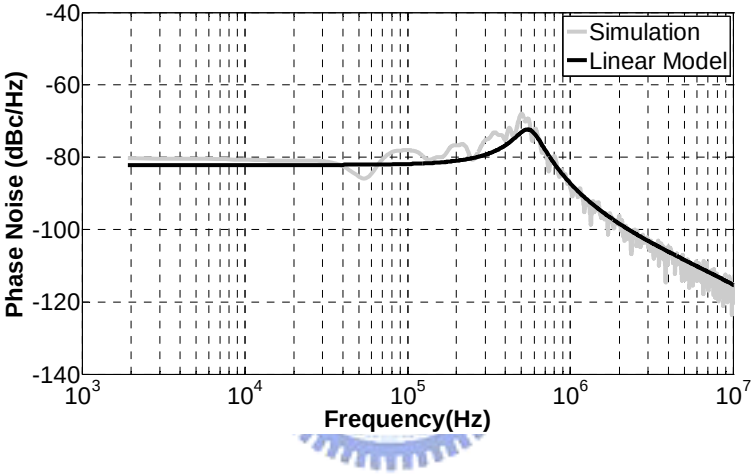


Fig. 3-28 Output phase noise with $K_{DCO}\alpha=1.92\times10^4$ and $K_{DCO}\beta=7.68\times10^4$.

For output jitter considerations, it is of great interest to determine the optimum value of $K_{DCO}\beta$ which minimizes the BBPLL output jitter for a given $K_{DCO}\alpha$. Fig. 3-29 reveals the simulation results of output rms jitter versus $K_{DCO}\beta$ and $K_{DCO}\alpha$. As expected, a smaller value of $K_{DCO}\beta$ causes the BBPLL to be close to the instability limit, where the peaking, and also the jitter, increases dramatically. Bigger values of $K_{DCO}\beta$ would stabilize the BBPLL on orbits with small radius. Nevertheless, increasing $K_{DCO}\beta$ further will cause the jitter to grow, due to the border loop bandwidth and bigger quantization step in the proportional path of the BBPLL. Thus there exists an optimum value of $K_{DCO}\beta$, which minimizes the output jitter.

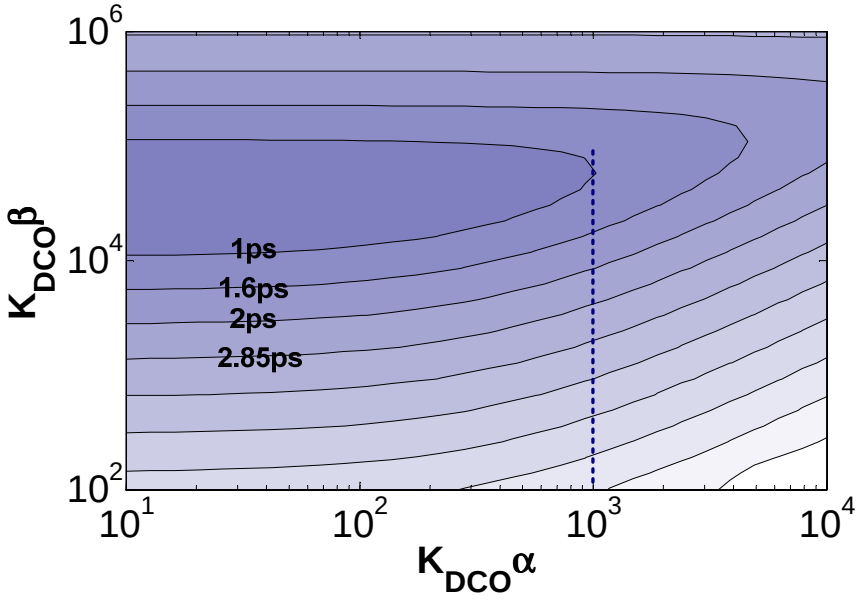


Fig. 3-29 Output jitter versus $K_{DCO}\beta$ and $K_{DCO}\alpha$.

Chapter 4 Design and Implementation of the ADPLL

4.1 Block Diagram of the ADPLL

A prototype of the ADPLL has been designed and fully integrated in UMC 90nm CMOS process with 9 metal layers. The detailed block diagram of the implemented ADPLL is shown in Fig. 4-1.

The dual mode phase detector (DPD) senses the phase difference between a reference signal (f_{REF}) and feedback signal from digitally controlled oscillator (DCO) by subtracting the output of phase accumulator 1 (PAC1) from phase accumulator 2 (PAC2). The phase information of reference signal is estimated by PAC1 which accumulating a frequency control word N/4 at every rising edge of the reference signal. At the same time, PAC2 measures the phase information of DCO output signal by counting the number of rising edge of the divided-by 4 DCO clock f_{DIV4}. The counted value is captured by a register at each reference cycle.

The loop filter which composed of programmable integral (α) and proportional (β) paths processes the phase error information and generates the control code for the DCO. The DCO adjusts the output frequency according to the control code and produces RF signal to output buffer. The frequency of high speed clock signal generated by DCO is then reduced by two stages of divided-by 2 frequency divider and the divided clock signal is fed back to PAC2.

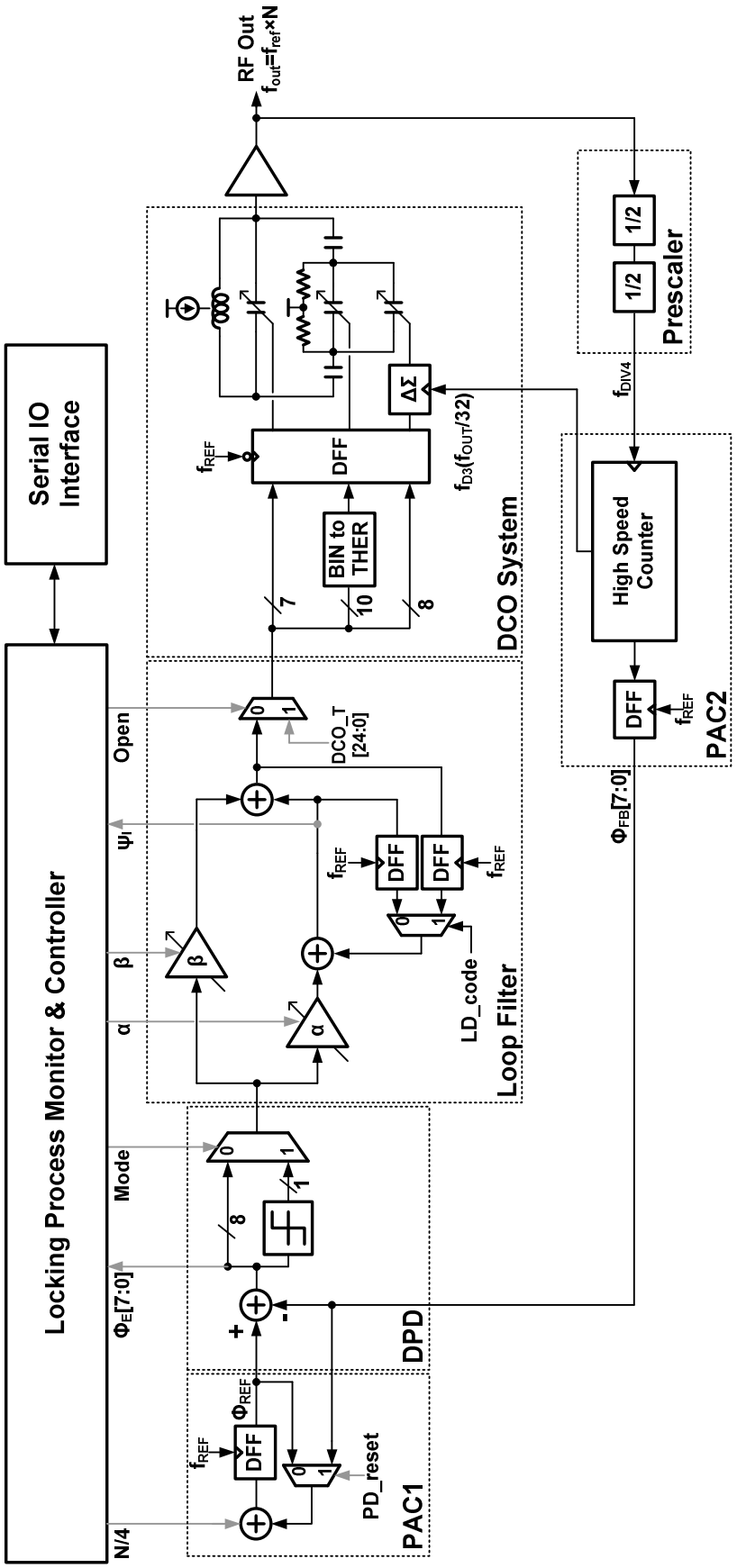


Fig. 4-1 Block diagram of the implemented ADPLL

In order to achieve dual mode operation and dynamically loop gain adjusting for fast locking, many multiplexer are inserted into the data path of the loop. The operation modes and loop gain parameters are controlled by the LPM.

In order to test the standalone DCO performance, a multiplexer has been introduced before the digital input of the DCO. In this way the DCO output frequency can be controlled externally and important properties such as the DCO tuning range and its tuning curves can be easily measured. For measurement considerations, the loop parameters and operation modes can be programmed by the control signals outside of the chip. Loop states and variables can also be read out by the instruments through output ports. In order to reduce the number of pins and occupied chip area, a simple serial interface is used to communicate with external testing instruments.

Owing to most of the building blocks, excluding the DCO, the prescaler and PAC2, are in digital manner, those circuits can be implemented straightforwardly with the conventional cell-based flow. By introducing the CAD tools in the design flow, design automation techniques including logic synthesis, automatic placement and routing can be utilized to accelerate design cycle of the chip. In the following sections, the most critical building blocks of the ADPLL will be investigated in more detail.

4.2 Phase Detection Circuits

The complete phase detection mechanism includes PAC1, PAC2 and DPD as shown in Fig. 4-3. Although the phase information of DCO output can be estimated by directly counting the number of the arrival rising edge of DCO output, it is difficult to design a counter which can work at such high frequency and the power consumption of the counter may become unacceptable. Thus, a

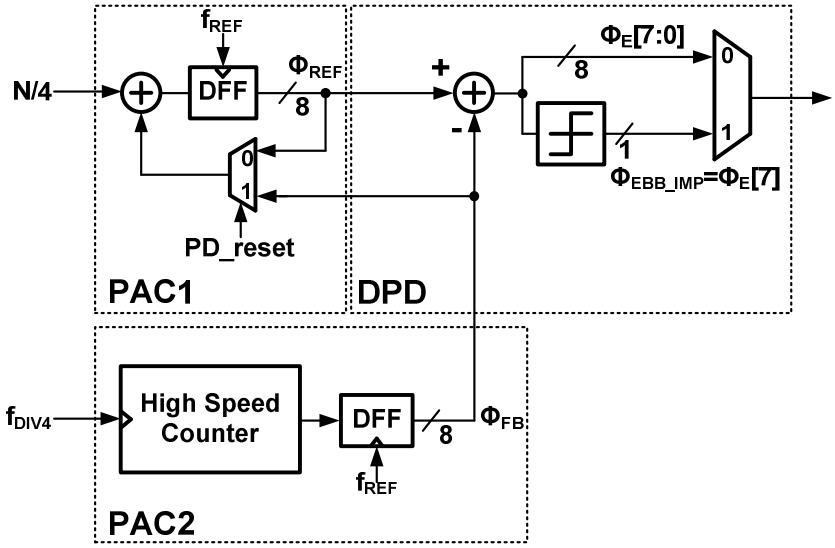


Fig. 4-2 Block diagram of the phase detector

prescaler which divides the DCO output frequency by 4 is inserted between the high speed counter and the DCO output.

The high speed counter counts the number of the arrival rising edge of the divided signal f_{DIV4} and produces the counter value Φ_{FB} when the rising edge of reference clock f_{REF} arrives. To calculate the phase difference information Φ_E, a subtracter which subtracts the feedback phase information Φ_{FB} from the reference phase information Φ_{REF} is introduced after PAC1 and PAC2.

As revealed in Fig. 4-2, the output of the subtracter is separated into two signal paths. The quantizer connected after the subtracter generates a single bit output Φ_{EBB_IMP} form the phase difference information Φ_E. The binary phase error signal Φ_{EBB_IMP} implemented as the sign bit of the phase difference signal Φ_E and the relation between them can be expressed as following equations:

$$\Phi_{EBB\_IMP} = \begin{cases} 0 \text{ if } \Phi_E \geq 0 \\ 1 \text{ if } \Phi_E < 0 \end{cases}. \qquad (4\text{-}1)$$

From this equation, it should be noted that the output of Φ_{EBB_IMP} is 0 or 1 rather then -1 or 1. The reason for it is to simplify the multiplication operations in loop filter and more detail descriptions will be given in section 4.3.

Due to the settling time during PT mode is largely determined by the initial phase error and frequency offset, the starting point of the bang-bang phase locking operation is important and the perturbation caused by the switching between different modes should be minimized. When the loop is in steady-state condition at the end of the fast frequency locking process, the DCO control code is stored to a register as the operation mode is changed from the FA mode to the PT mode. This saved value which is close to the DCO control code corresponding to the target oscillation frequency is loaded to the register of integral path in loop filter as loop entering the PT mode. Simultaneously, the output of phase detector is reset to 0 by equalizing the two input signals of the subtracter. This operation can be achieved by introducing a multiplexer before the register of reference phase accumulator and setting the control signal PD_reset to high.

4.2.1 Modulo arithmetic of the phase detection circuit

Due to the practical limitation of the word length of the arithmetic components, PAC1 and PAC2 are implemented in modulo arithmetic [12]. The reference and feedback phase information, Φ_{REF} and $\Phi_{FB,}$ respectively, are linear and grow without bound with the development of time. However, the registers

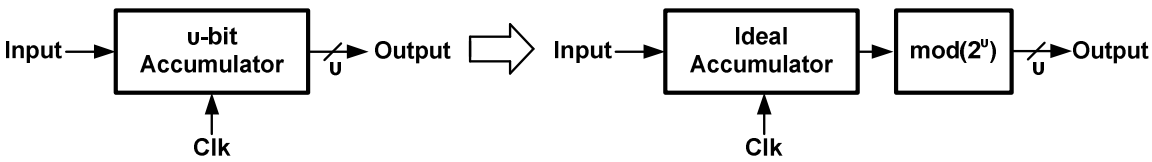


Fig. 4-3 Behavior model of υ-bit accumulator.

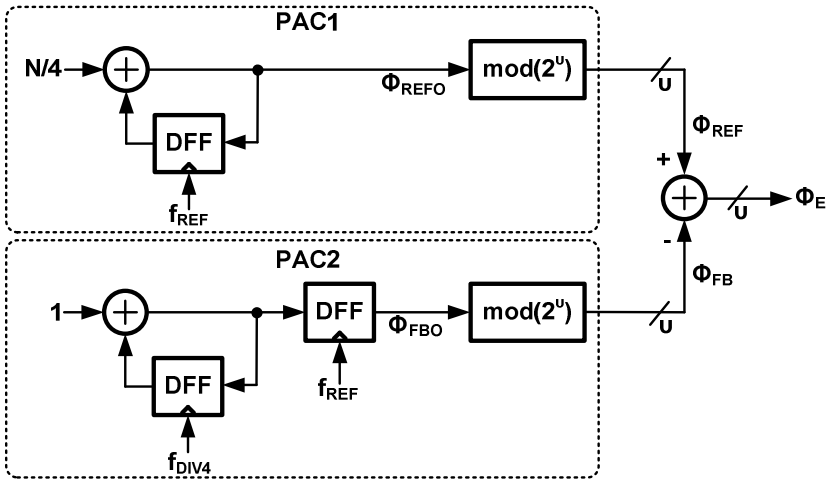


Fig. 4-4 Simplified block diagram of phase detector.

of accumulators can not hold unbound values and the stored values are restricted to the range of 0 to 2^{υ}-1, where υ represents the bit length of the accumulator. The accumulator overflows when the accumulated value reaches the upper bound. If the carry-out bits of the accumulator are simply disregarded, the behavior of the accumulator can be modeled as an ideal accumulator followed by a modulo-υ operator as illustrated in Fig. 4-3. After considering the effect of limited bit length of the accumulators, a block diagram representing the simplified phase detector is shown in Fig. 4-4.

In Fig. 4-4, the reference and feedback accumulators are replaced with two ideal accumulators and modulo-2^{υ} arithmetic units. The signals, Φ_{REFO} and Φ_{FBO}, represent the ideal reference and feedback phase information, respectively. To get a clear insight into the characteristics of the architecture, the modulo arithmetic on Φ_{REFO} and Φ_{FBO} could be visualized as two rotating vectors as shown in Fig. 4-5. In this figure, Φ_{REF} and Φ_{FB} are positive numbers which have a maximum possible value of (2^{υ}-1) without rollover. If the output of the subtracter is treated as a 2's compliment number, the phase detector output Φ_E has the same range but is symmetric around zero. It can be shown that the value

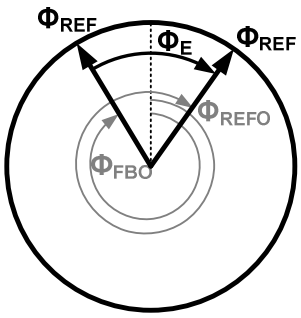


Fig. 4-5 Rotating vector interpretation of the reference and feedback phases.

of Φ_E lies within $[-2^{(\upsilon-1)}, 2^{(\upsilon-1)}-1]$ and invariably the phase detector output Φ_E indicates the smaller angle between the two vectors.

Due to the modulo arithmetic, the phase detector is not only the arithmetic subtracter of two numbers but also performs a cyclic adjustment as suggested by Fig. 4-5. For the phase detector output to be corresponding to the phase error in perspective, the difference between Φ_{REFO} and Φ_{FBO} should be restricted to the range of $[-2^{(\upsilon-1)}, 2^{(\upsilon-1)}-1]$. Under this limitation, the output of phase detector can be expressed as

$$\Phi_E = \Phi_{REFO} - \Phi_{FBO} \quad when \quad -2^{(\upsilon-1)} \le (\Phi_{REFO} - \Phi_{FBO}) \le 2^{(\upsilon-1)} - 1. \qquad (4\text{-}2)$$

From equation 4-2 it can be shown that under this condition, the output of phase detector Φ_E is simply an arithmetic subtraction of the two outputs of reference and feedback accumulators. From the design point of view, this condition sets the upper bound of the frequency offset between the target frequency and DCO output frequency (f_{OUT}-f_{REF}N). Assuming the initial phase error Φ_E is 0 and the DCO output frequency is f_{OUT}. At the next rising edge of reference clock (f_{REF}), the values of PAC2 and PAC1 increase by N/4 and $f_{OUT}/4f_{REF}$, respectively. To avoid aliasing, the following condition must be met:

$$\begin{aligned} &-2^{(\upsilon-1)} \le \left(\frac{N}{4} - \frac{f_{OUT}}{f_{REF}\,4} \right) \le 2^{(\upsilon-1)} - 1 \\ &\Rightarrow -f_{REF}\,2^{(\upsilon+1)} \le (f_{TARGET} - f_{OUT}) \le f_{REF}\,2^{(\upsilon+1)} - 1 \end{aligned} \quad , \qquad (4\text{-}3)$$

where $f_{TARGET}=Nf_{REF}$ is the target frequency. It should be noted that during fast frequency locking process, the absolute value of the phase error (Φ_{REFO}-Φ_{FBO}) might raise over the upper bound even if the condition mentioned in equation 4-3 is met. Neglecting the overshooting behavior during locking process, the phase detector output should be settled to some value within [$-2^{(\upsilon-1)}$, $2^{(\upsilon-1)}$-1]:

$$f_{OUT} = f_{DCO,free} + K_{DCO}\beta_{FA}\Phi_E$$
$$\Rightarrow -2^{(\upsilon-1)} \le \frac{Nf_{REF} - f_{DCO,free}}{\beta_{FA}K_{DCO}} \le 2^{(\upsilon-1)} - 1 \qquad (4\text{-}4)$$

In equation 4-4, β_{FA}, $K_{DCO,}$ f_{FREE} are forward path gain in fast frequency locking mode, DCO gain and DCO free running frequency respectively.

The possibility of aliasing due to the modulo arithmetic during PT process should be also taken into consideration. Assuming the DCO output frequency f_{OUT} equals to the target frequency Nf_{REF}, the range of the phase offset between reference and feedback phase normalized to reference clock period can be expressed as

$$\frac{-2^{(\upsilon-1)}}{N} \cdot 8\pi \le \varphi \le \frac{2^{(\upsilon-1)}-1}{N} \cdot 8\pi, \qquad (4\text{-}5)$$

which has been discussed in chapter 3.

In the implementation of the ADPLL, the bit length of the reference and feedback accumulators must be made sufficiently large to ensure that the conditions list in equations 4-3, 4-4 and 4-5 would be always met. In the design presented in this thesis, two 8-bit accumulators are utilized to construct the PAC1 and PAC2.

4.2.2 PAC2

As shown in Fig. 4-1, the PAC2 is implemented as a high speed counter with the rollover effect as described above. The counter can be implemented quite easily using register-type circuits such as the flip-flops, and a wide variety of design

exists. There are two major types of flip-flop based counter according to the clocking mechanism of the registers, namely asynchronous counter and synchronous counter.

The simplest asynchronous counter circuit is a D type flip-flop with input fed from its own inverted output. This counter increase once for every clock cycle and takes two clock cycles to overflow, so every cycle the output of the counter will alternate between 0 and 1. It should be noted that the counter creates an output clock at exactly half the frequency of the input clock and hence it also perform a divided-by 2 operation. The generated signal can clock the next counter stage if more than one stage is connected in series to extend the range of the counter.

An example of a 4-bit asynchronous down counter along with its time diagram is illustrated in Fig. 4-6. This down counter can be easily transformed to an up counter by simply inverting the output of each stage (Q_1~Q_4). Note that it can be shown from Fig. 4-6 that each counter stage working at half of the frequency of previous stage and the rising edge of each output (Q_1~Q_4) does not align to each other. The existence of the unavoidable propagation delay of the

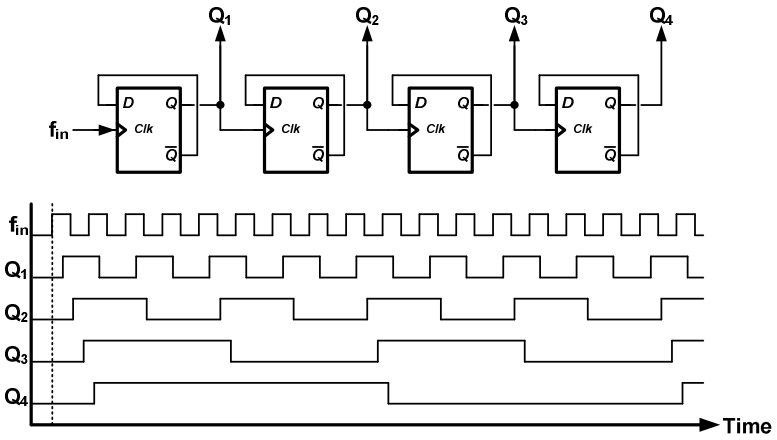


Fig. 4-6 Asynchronous counter.

flip-flop results in the unstable outputs as the overflows "ripple" from stage to stage. In the case where the instantaneous count is important, the timing skew between stages will cause incorrect counting results. Besides, the increasing of the input frequency and the counter length will worsen the situation. If each stage of the output of an asynchronous counter is sampled by the same clock phase, for an L bits asynchronous counter with the D flip-flop which have a clock to output delay of $t_{c\text{-}q}$ and a setup time of t_{setup}, the maximum operating frequency $f_{in,max}$ can be expressed as

$$f_{in,\max} = \left(Lt_{c-q} + t_{setup}\right)^{-1}. \qquad (4\text{-}6)$$

To solve this issue in the applications where a stable count value is important across several bits, the synchronous counters could be used. Rather then the asynchronous counters in which each flip-flop is triggered by the output of the preceding stage, the flip-flops of synchronous counters are all triggered by the same clock source. Fig. 4-7 shows a 4-bit synchronous counter composed of logic gates and flip-flops. The time diagram of the counter is also shown in Fig. 4-7 and it can be observed that the signal edge of each stage (Q_1~Q_4) is aligned to the input clock f_{in}. The synchronous output of this counter solves the issue of

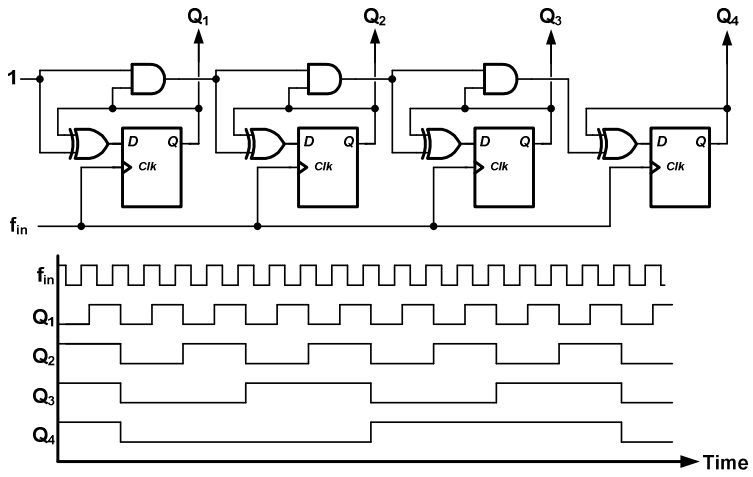


Fig. 4-7 Synchronous counter.

unsettled output while carrier signal propagates in asynchronous counter circuit at the expense of larger power consumption. Because all the flip-flops in the synchronous counter circuit operate at the frequency which is as high as input clock frequency, the synchronous counters consume much more dynamic power than asynchronous counters. In addition to the issue of power consumption, the synchronous also suffer the problem of slower operating speed. The maximum operation speed for an L bit synchronous counter can be determined by the time for the carrier signal to propagate from the first stage (LSB) to the last stage (MSB) and could be derived as:

$$f_{in,\max} = \left[t_{c-q} + (L-1)t_{AND} + t_{XOR} + t_{setup}\right]^{-1}, \qquad (4\text{-}7)$$

where $t_{c\text{-}q}$, $t_{setup,}$ t_{AND} and t_{XOR} are the clock to output delay of the flip-flops, the setup time of the flip-flops, the gate delay of the AND gate t_{AND}, and the gate delay of the XOR gate, respectively.

To solve the edge skewing issue and preserve the advantages of high speed operation and low power consumption of the asynchronous counter, a skew-insensitive high speed counter is proposed. Before presenting the complete architecture and operation of the high speed counter, a simple example of a 1-bit counter will be shown to give a clear insight into the operation principle of the high speed counter.

Fig. 4-8 shows a simple example of a 1-bit counter with proposed sample phase generator. The counter consists of a basic 1-bit flip-flop based asynchronous counter, a D type latch to perform sample phase generation and a D type flip-flop to fetch the output from the 1-bit asynchronous counter. The time diagram illustrated in Fig. 4-8 shows the relationship among the sample phase Φ_s, the input clock f_{in}, the asynchronous counter output D_1, the generated

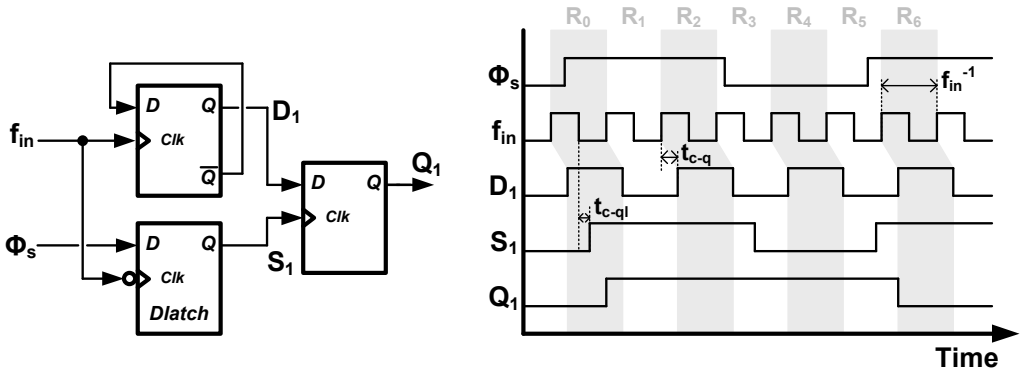


Fig. 4-8 Example of a 1-bit counter with sample phase generator.

sampling clock S_1 and the fetched output Q_1. The regions divided by the shadowed area indicate the connection between the time interval when the asynchronous output D_1 is valid and the time slots where the rising edge of the sample phase Φ_s appears. In other words, if the rising edge appears in R_0, the corresponding output should locate in the same region and thus Q_1 should be 1. The shadowed area would be a rectangular form without the skew edge, but in reality the existence of the clock to output delay $t_{c\text{-}q}$ of the flip-flop leads to the misalignment between the rising edges of f_{in} and D_1 which results in the distortion of the shape.

The introduced D type latch not only generates a delay version of the sample clock Φ_s, but also adjusts the sampling point so that the flip-flop can fetch the correct value from D_1. The sample phase Φ_s is postponed by the D latch controlled by f_{in} and a sampling clock S_1 which has a rising transition when the f_{in} is 0 is produced. It should be noted that when Φ_s goes to high, the output D_1 become valid after the most recently rising transition of f_{in} delaying by $t_{c\text{-}q}$. Similarly, the output D_1 remains valid until the f_{in} changes from low to high which results in the state transition on D_1.

To examine the design margin and the robustness of this topology, the operation condition and the propagation delay of each component must be taken into consideration. Due to the physical phenomenon of metastability, the input data for a flip-flop must have settled by a setup time t_{setup} for the data to be reliably sampled. In the case where Φ_s goes high before the D latch becomes transparent, the upper bound of input frequency $f_{in,max}$ can be determined according to the setup time requirement:

$$f_{in,\max} = \frac{1}{2\left(t_{c-q} + t_{setup} - t_{c-ql}\right)}. \qquad (4\text{-}8)$$

From equation 4-8, it can be seen that the maximum input frequency of this counter depends on the setup time t_{setup} of the D type flip-flop, the clock to output delay $t_{c\text{-}q}$ of the D type flip-flop, and the clock to output delay $t_{c\text{-}ql}$ of the D latch. In another case where Φ_s goes high after the D latch becomes transparent, the circuit may suffer from the metastability problem when the rising edge of Φ_s is close to the rising edge of f_{in}. To solve this issue, a D type flip-flop is introduced which makes the rising edge of the input signal of the latch always leads the rising edge of f_{in}, and the modified circuit is shown in Fig. 4-9.

After the detail description of the proposed 1-bit counter, it is

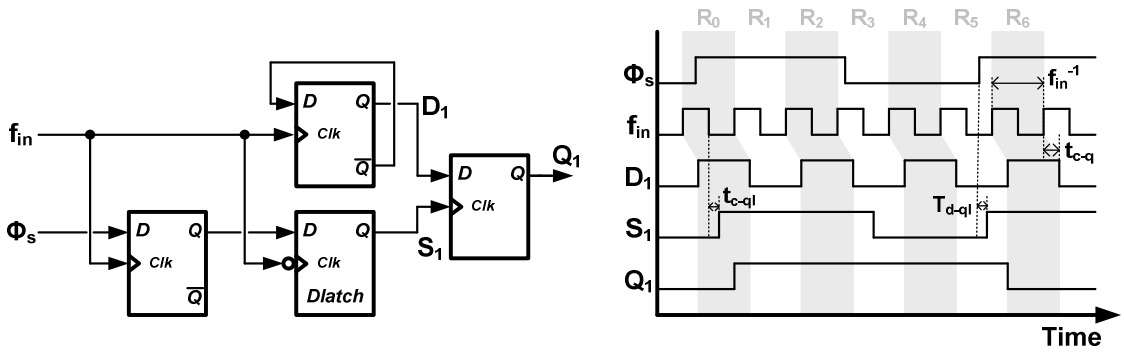


Fig. 4-9 Example of a 1-bit counter with an additional D type flip-flop.

straightforward to construct the counter with more bits by simply connecting the 1-bit counters in series. The complete block diagram and time diagram of the high speed counter is shown in Fig. 4-10. The operation principle of this architecture follows the one of the 1-bit counter as mentioned before.

Due to the non-bound relationship between f_{REF} and f_{DIV4}, it is quite likely that under certain condition, the flip flop may face the metastability problem. During metastability, the output of the flip flop could be undefined at a given clock cycle which is not acceptable for proper system operation. This problem can be solved by passing the lower frequency signal through a series of flip flops which are clocked by the higher frequency clock. The overall probability of metastability condition at output of the system decreases exponentially with the number of the flip flop. Furthermore, the probability of a metastable state of a single flip flop can be reduced by increasing the speed of the flip flop. In order

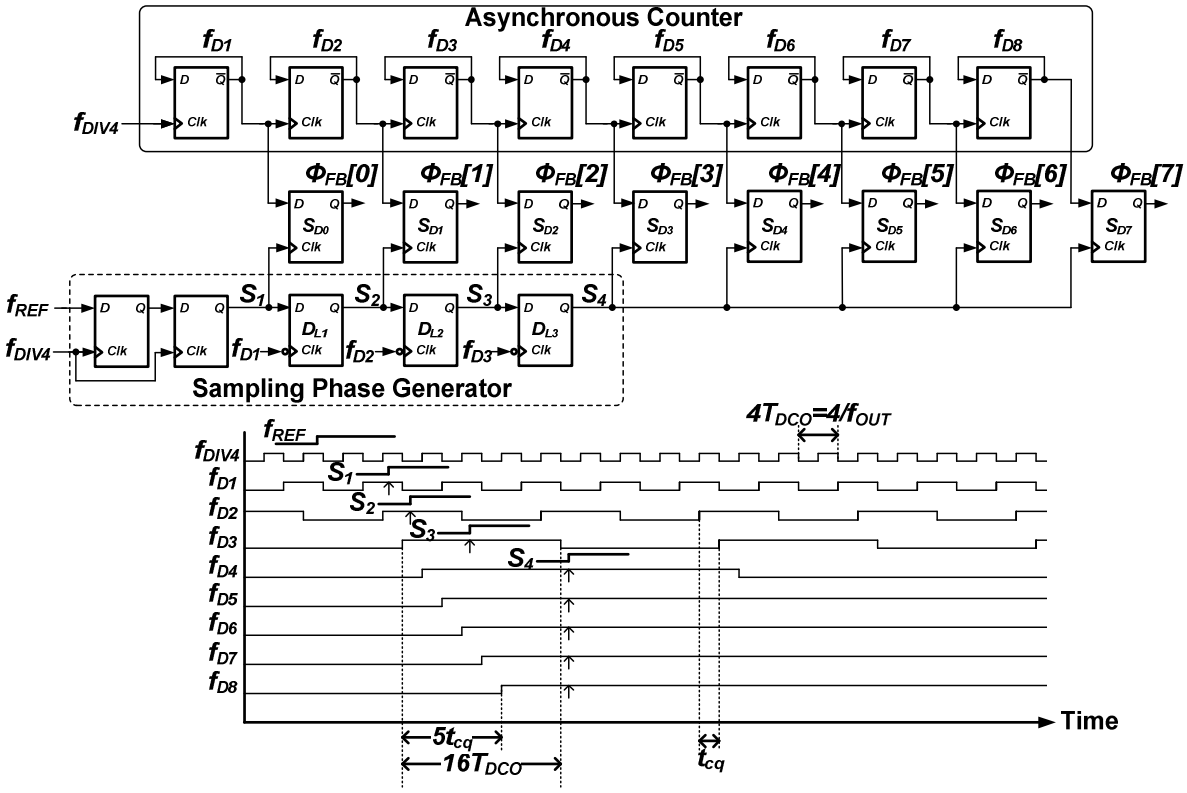


Fig. 4-10 Bock diagram and time diagram of the proposed high speed counter.

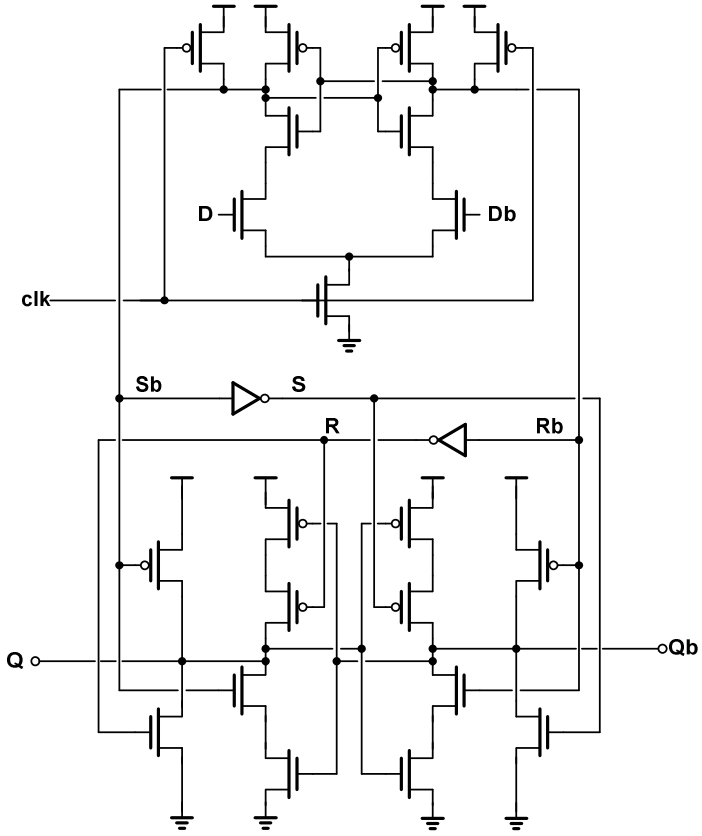


Fig. 4-11 Schematic of the tactical flip flop [13]

to reduce the probability of a metastable state, the sampling in the first stage of sampling phase generator is performed by a pair of sense amplifier based flip flops [13], and Fig. 4-11 shows the schematic of the sense amplifier based flip flop. The advantages of this topology are the fast response time and low power consumption.

When f_{REF} comes in to fetch the contents in PAC2, the sampling phase S_1 for the 1st stage of the asynchronous counter is generated by resampling f_{REF} through 2 D flip-flops to avoid metastability. S_1 is then postponed by D-latchs D_{L1}-D_{L3}, which are toggled by the falling edge of the 1st – 3rd stage divider outputs f_{D1}-f_{D3}, to generate the sampling phases S_2 – S_4. Thus, a minimum setup time of $4T_{DCO}$-t_{cq} can be guaranteed when retrieving the contents of the ripple counter.

The sampling scheme of the LSB $\Phi_{FB}[0]$ is slightly different form the topology illustrated in Fig. 4-8, where the sampling signal S_1 is generated by a D latch rather then a flip flop. By taking the advantage of short clock to output delay of the sense amplifier based flip flops, the asynchronous counter output f_{D1} can be sampled just before the transition occurs without violating the hold time condition of the output flip flop. In this way, the upper bound of input frequency as specified in equation 4-8 can be released and the additional flip flop shown in Fig. 4-11 can be removed.

From Fig. 4-10, it should be noted that the 5 MSBs asynchronous outputs f_{D4}-f_{D8} are sampled by the same signal S_4. From the simulation results, the delay time of the sampling signal S_4 satisfies the time requirement for the “carry” signal to propagate from the fourth stage to the last stage of the divider chain, so further generation of the sampling phase is unnecessary.

4.3 Digital Loop Filter and LPM

The digital loop filter consists of proportional path and integral path as shown in Fig. 4-1. The data path in the loop filter is 26 bits wide and represented in two’s complement arithmetic. Fig. 4-12 illustrates the block diagram of the detail implementation of the digital loop filter. It should be noted that the multiplied by α(β) and -α(-β) operation is replaced by selecting the positive or negative value from multiplexer inputs. In order to perform the dynamic loop parameters and modes switching, several multiplexers are introduced in the loop filter. The activity of the loop filter incorporated with these multiplexers during the locking process will be described as following.

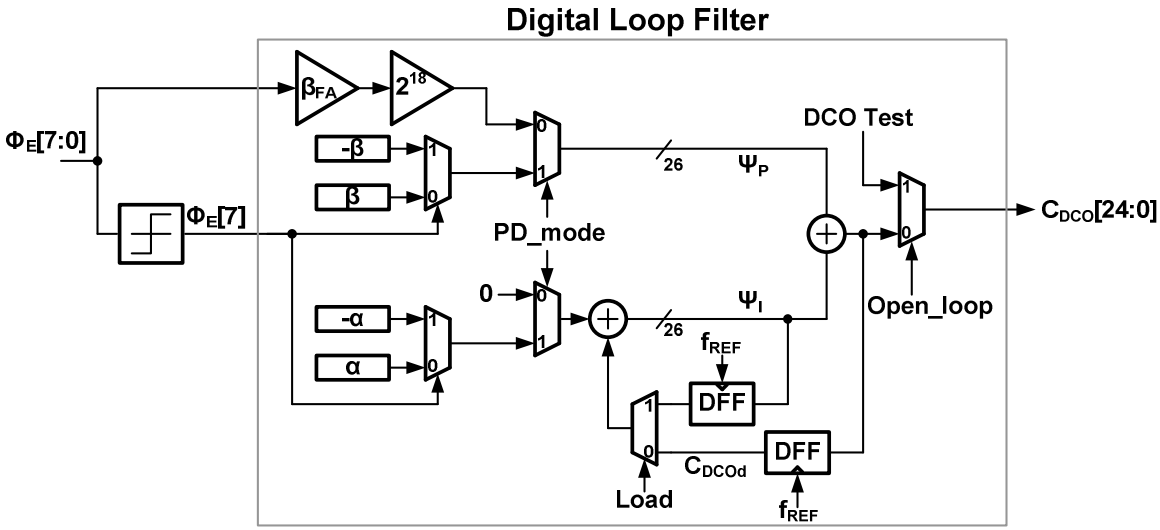


Fig. 4-12 Implementation of the digital loop filter.

At the beginning of the locking process, all memory elements are reset synchronous by asserting a control signal. At first, the fast frequency acquisition mode is activated where only the proportional path is used by set PD_mode to 0. During the FA mode, the output of the phase detector Φ_E is scaled by a value β_{FA}. The scaling operation is implemented in an efficient manner as programmable right-bit-shift operation and the variable value β_{FA} can assume to be a programmable integer value of power of two in the range from 2^0 to 2^3. To further enhance the locking performance, the FA mode is divided into two stages according to the proportional gain β_{FA}.

At the beginning of this mode, a large gain β_{FA} is used to allow the output frequency to lock quickly and roughly to the target frequency. Then the DCO control code C_{DCO} is stored to a temporary register as C_{DCOd} and control signal PD_reset shown in Fig. 4-1 is set to high to reset the phase detector. Finally, the stored control code C_{DCOd} is loaded to the register in integral path by asserting the control signal Load and the smallest allowed gain for β_{FA} is applied to resolve the frequency quantization error left from the proceeding stage.

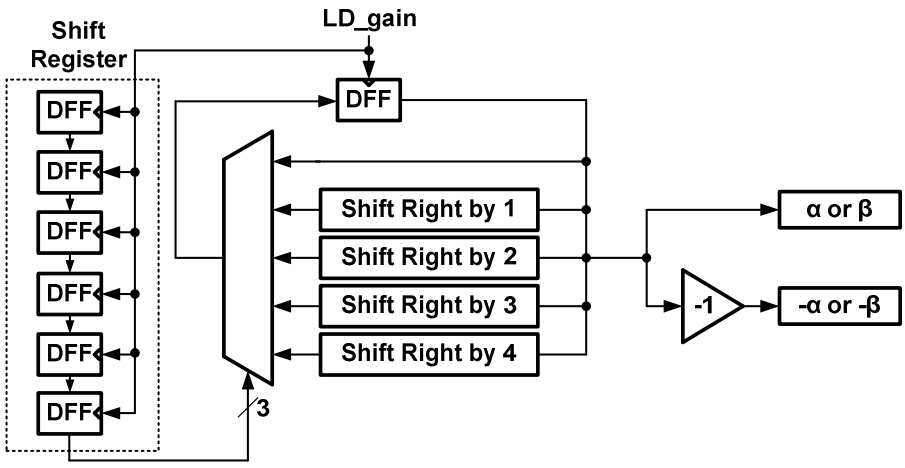


Fig. 4-13 Implementation of the gain controller

After the output frequency is settled, the PT mode is entered. The following events happen at almost the same time: First, the DCO control code C_{DCO} is sampled at the output of the loop filter and stored to a temporary register. The phase detector is then reset to clear the phase error residue and C_{DCOd} is loaded to the register in the integral path again. Finally the integral path is switched on by asserting the control signal PD_mode.

During the PT process, the loop parameters, α and β, are dynamically scaled to reduce the locking time. Fig. 4-13 reveals the hardware realization of α and β loop gain factors. At the beginning of the bang-bang phase locking process, both α and β are set to initial values. As LD_gain is asserted, α and β are scaled down by shift right operations and the scaling factors are based on the values stored in the programmable shift registers. It can be seen from Fig. 4-13 that the gain controller can generate 5 different pairs of α and β during locking operation. To reduce the computation complexity, the multiplications in the loop filter in phase locking mode are implemented as multiplexers controlled by $\Phi_E[7]$ with both positive and negative inputs of the gain factors α and β.

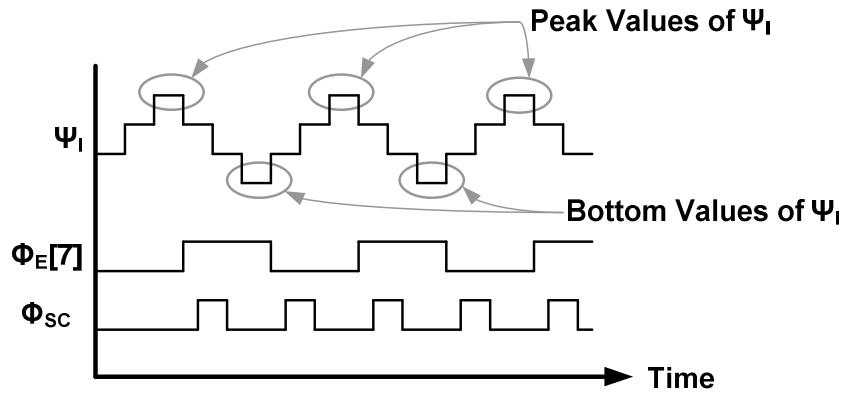


Fig. 4-14 Time diagram of the locking state in PT mode.

As mentioned in chapter 2, the time for the control circuit to perform gain scaling is determined by the existence of the locking state. The relationship between the output of the integral path Ψ_I and $\Phi_E[7]$ in the locking state can be shown in Fig. 4-14. It should be observed that the increment of the integral path when $\Phi_E[7]$ is 0 is equal to the decreasing amount while $\Phi_E[7]$ is 0. This implies that if the loop reaches steady-state condition, the peak or bottom values of Ψ_I will remain unchanged and thus the existence of the locking state can be detected.

Fig. 4-15 shows the implemented LPM. The signal Φ_{SC} indicates that there is a transition on the MSB of the phase detector output $\Phi_E[7]$ and also a local

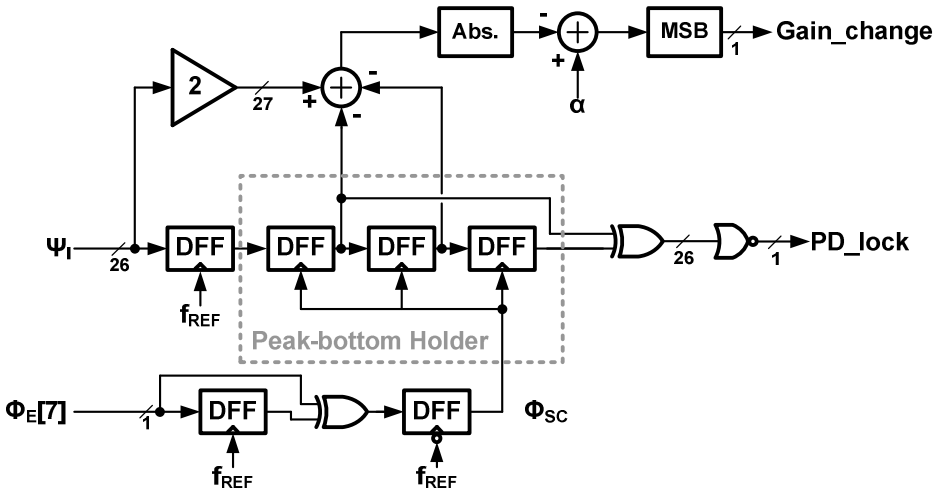


Fig. 4-15 Implementation of the LPM.

maximum or minimum value appears on Ψ_I. Thus, this operation can be treated as the gradient polarity detector (GPD) of Ψ_I. The peak-bottom holder stores the peak or bottom values by using the signal Φ_{SC} to clock a shift register. Note that the values stored in the peak-bottom holder should be either two peak values with one bottom value or one peak value with two bottom values. A XOR gate followed by a NOR gate is connected behind the peak-bottom holder which compares the first and third outputs of the flip-flops in the peak-bottom holder. Thus, the XOR produces an output that indicted the difference between the adjacent peak or bottom values. If the loop is in steady-state, the XOR produces an output with all digits in the bus equal to 0 and thus PD_lock is 1.

The PD_lock indicates that the locking state is reached and the loop gain factors can be scaled immediately. However, the time of switching the gain factors is significant as far as the locking speed is concerned. The time instance for the loop parameters to be adjusted is based on the state of the control signal

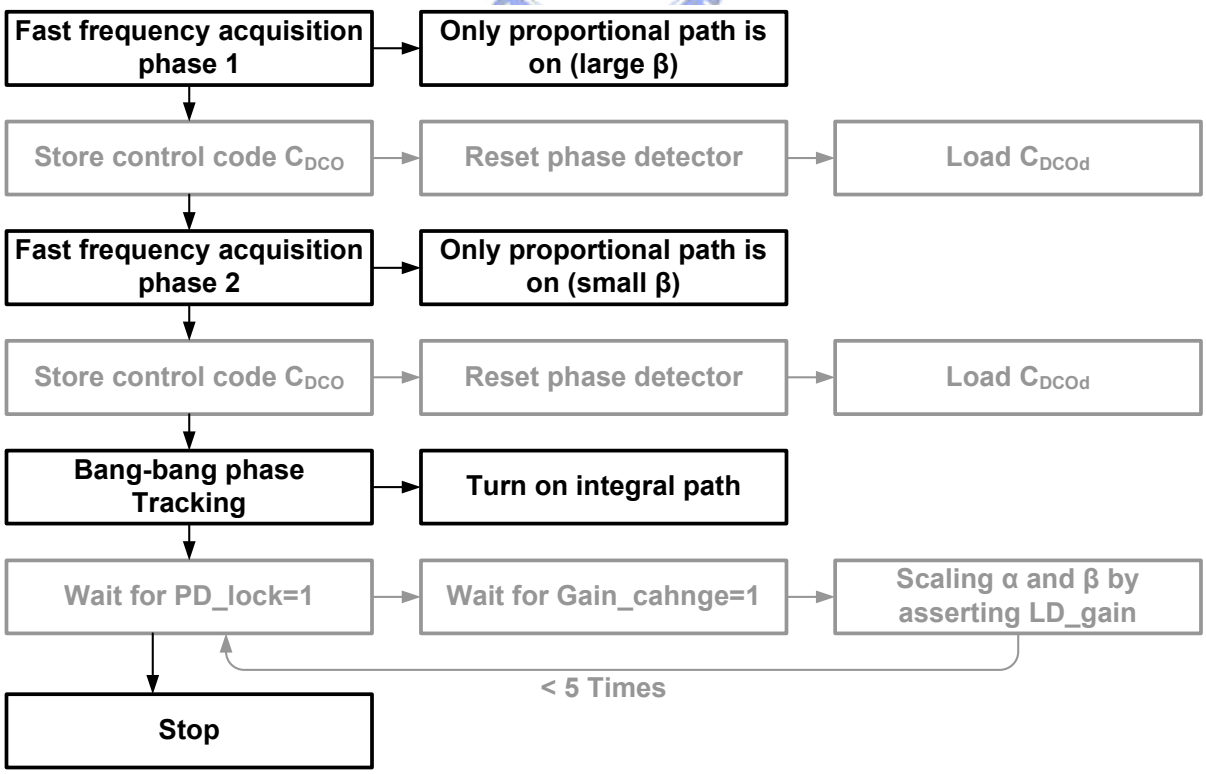


Fig. 4-16 Flowchart of the ADPLL locking process.

Gain_change. Since the nature of the bang-bang phase locking, the output value of the loop filter oscillates around a fixed value corresponding to target frequency as the loop is in steady-state. The average of the peak and bottom values of integral path output can be assumed as the control code corresponding to the frequency closed to the target frequency. This assumption leads to the using of the average of peak and bottom values as the starting point when the loop gain factor is scaled. The signal Gain_change is raised to high only if the difference between present integral path output and the average of its peak and bottom values is less then α/2. The loop controller will assert LD_gain to adjust the loop gain factors α and β when both transitions on PD_lock and Gain_change are received. Fig. 4-16 summarizes the locking process of the proposed ADPLL.

4.4 Digital Controlled Oscillator (DCO)

In this section, the design and implementation of the digitally controlled oscillator (DCO) will be illustrated. The implemented block diagram of the DCO system is shown in Fig. 4-17. The DCO receives a 25-bits wide control word C_{DCO}[24:0] from the loop filter without the sign bit and delivers a differential signal with frequency around 10GHz to the buffers.

Due to its relatively good phase noise, ease of implementation, and better rejection of common-mode additive noise, the cross-coupled inductance capacitance (LC) oscillator is chosen. The MOS implementation of the LC oscillator can be classified into two major categories: NMOS only structure and complementary structure which uses both NMOS and PMOS in a cross-coupled fashion to compensate the power loss in LC resonator.

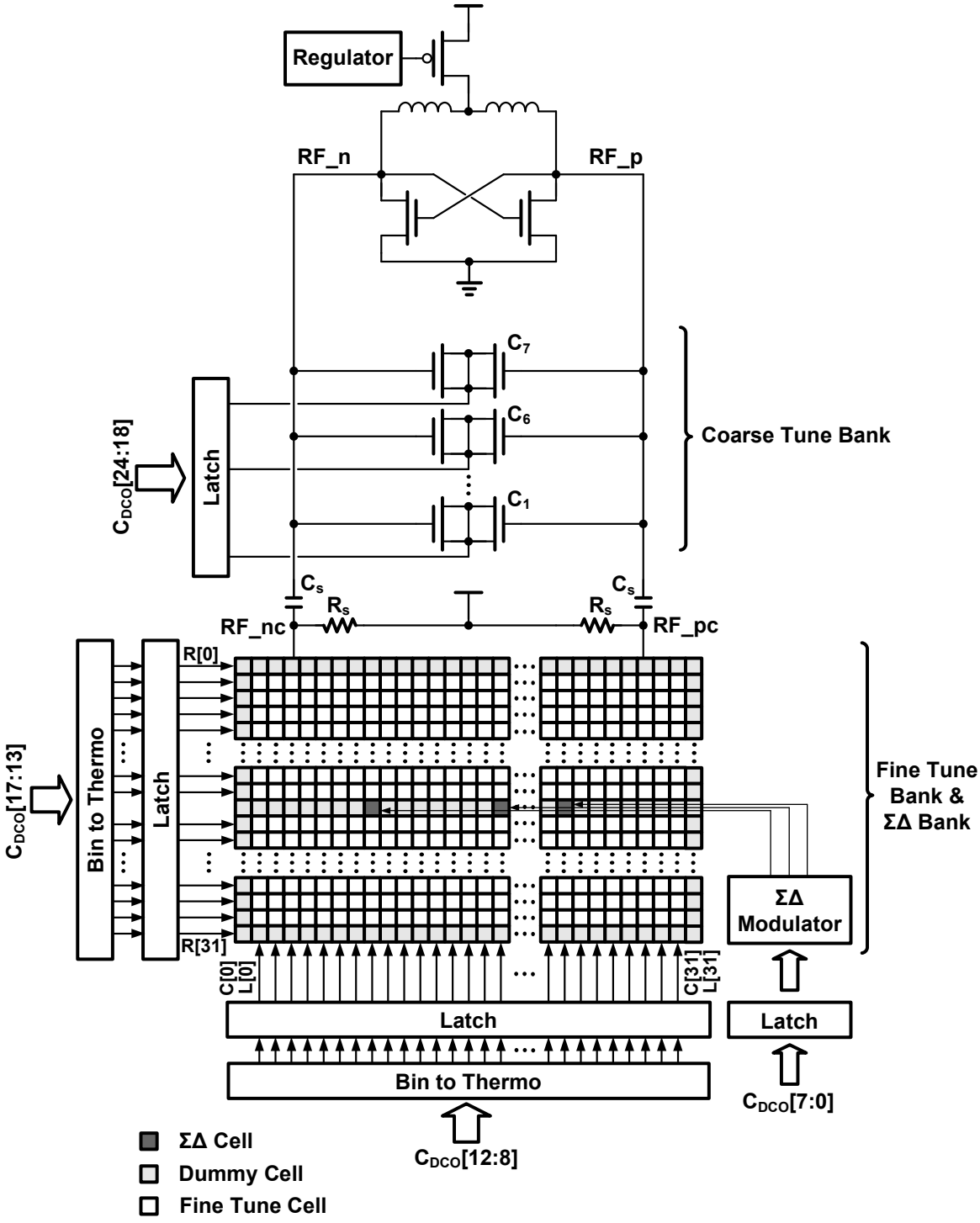


Fig. 4-17 Implemented block diagram of DCO system.

It has been reported that there are several reasons for the superiority of the complementary cross-coupled pair over the NMOS-only structure [11]. The complementary structure offers higher transconductance for a given current, which results in faster switching of the cross-coupled differential pair. It also

offers better symmetry of the waveform, which results in a smaller $1/f^3$ noise corner. Nevertheless, the single NMOS-only topology is chosen over the complementary one to enable the oscillators to operate in the current limited region for low voltage supply.

Since the tail current can contribute as much as 15% to the total phase noise [14] when the MOS of the current source is operated in saturation region, a PMOSs operated in linear region is used as biasing to reduce its noise contribution. The nominal bias current is 3mA and an on-chip regulator is introduced to stabilize the bias condition.

4.4.1 Varactor Banks

In an ideal LC oscillator the frequency f_{OSC} and the period T_{OSC} of the oscillation are a nonlinear function of the tank capacitance C_{tank}:

$$f_{OSC} = \frac{1}{T_{OSC}} = \frac{1}{2\pi\sqrt{LC_{tank}}}. \qquad (4\text{-}9)$$

In the traditional voltage controlled LC oscillator, frequency tuning is achieved by controlling the effective tank capacitance with an analog control signal. The variable capacitor is typically implemented by the diode or the MOS varactor which has a non-linear relationship between the capacitance and the tuning voltage.

In the concept of the digital tuning, the oscillation frequency is made to be proportional to the input digital control word C_{DCO}. To achieve digital tuning of the oscillation frequency, the varactor can be used but only two voltage levels are applied. In the implemented DCO system, NMOS with control signal short to drain and source is used as the inversion type varactor and each varactor operates in either high or low capacitance state. When the source voltage, drain voltage drop to zero and the gate potential V_G is 1V, an inversion layer exists

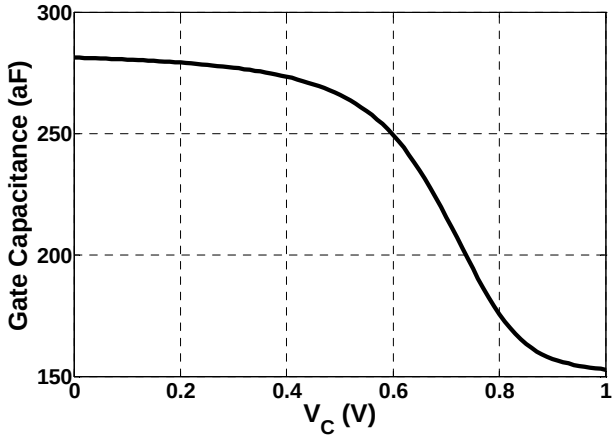


Fig. 4-18 Gate capacitance v.s. drain and source voltage, VC, of a simulated NMOS varactor with L=0.08μm, W=0.16μm.

below the gate oxide region. This structure behaves likes a parallel-plate capacitor with only a silicon oxide dielectric in between and the capacitance of the varactor is relatively high. As the control signal rise to 1V, the depletion region is formed under the gate oxide and a small overlap capacitance dominants the capacitance of the varactor. By this way, the digital tuning can be achieved by controlling the amount of the MOS varactors in high capacitance state. Today's advanced CMOS process makes it possible to create extremely small varactors which have controllable capacitance in the order of hundreds of attofarads and results in relatively fine frequency resolution in the digital tuning LC oscillator. Fig. 4-18 shows the simulation result of the C-V curve of a NMOS varactor with gate voltage tie to 1V.

Due to the finite DCO frequency resolution, the quantization error will introduce noise to the RF output signal. To gain insight into the quantization effects on the DCO phase noise, consider the quantization noise model, shown in Fig. 4-19 [15]. The quantization process can be modeled as an infinite-precision tuning signal added by an uniformly distributed random variable $\Delta f_{n,0}$ with white noise spectral characteristics. The quantization noise is

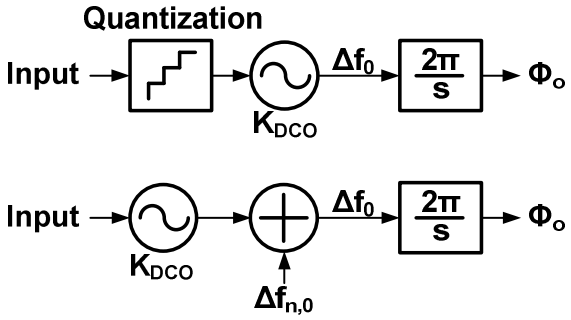


Fig. 4-19 DCO quantization noise model.

then converted to phase noise through the 2π/s integration. The output phase noise due to the finite quantization error can be expressed as [15]:

$$L_{Quantize}(\Delta f)=\frac{1}{12}\times\left(\frac{\Delta f_{res}}{\Delta f}\right)^2\times\frac{1}{f_{REF}}\times\left(2sinc\frac{\Delta f}{f_{REF}}\right)^2 \qquad (4\text{-}10)$$

In equation 4-10, Δf_{res} is the DCO quantization step which indicates the corresponding frequency deviation of one DCO control code. It can be seen that the output phase noise due to quantization process can be reduced by increasing the DCO frequency resolution. With careful design, the phase noise contributed from the quantization can be made below the natural DCO phase noise resulted from the finite quality factor of the LC tank and noise of active devices. As mentioned in section 3.3.3, the phase noise of the LC tank oscillator can be expressed as [11]

$$S_{\varphi_{n,DCO}}(\Delta f)=\frac{\overline{i_n^2}/\Delta f}{q_{\max}^2}\frac{\Gamma_{rms}^2}{8\pi^2\Delta f^2} \qquad (4\text{-}11)$$

where $\overline{i_n^2}/\Delta f$ is the PSD of the equivalent parallel current noise, Γ_{rms} is the rms value of the impulse sensitivity function (ISF) associated with that noise source, q_{max} is the maximum signal charge swing which is defined as the product of the tank capacitance and maximum signal swing $C_{tank}V_{swing}$, and Δf is the the offset frequency from the carrier. Consider the DCO with different frequency step Δf_{res} and assume that the quality factor of the inductor is 8. By substituting the

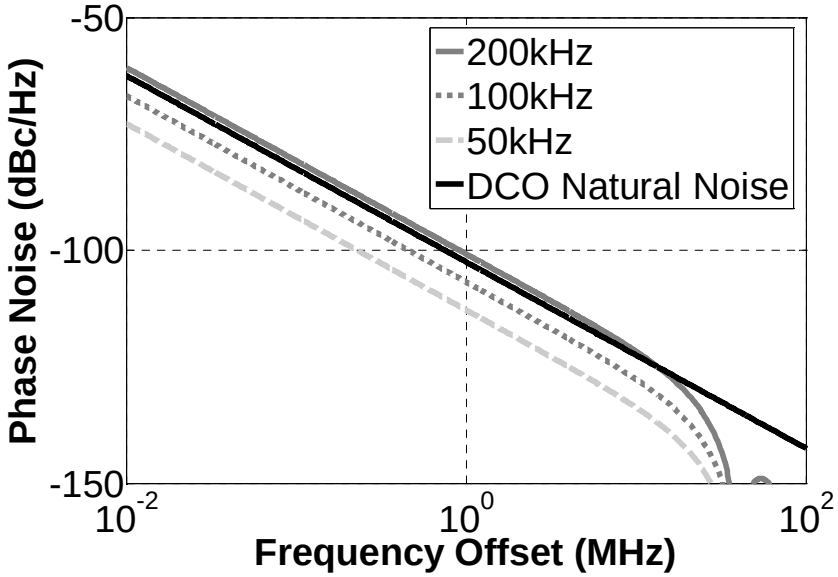


Fig. 4-20 Phase noise due to frequency quantization of different frequency resolution step.

parameters addressed in chapter 3, the phase noise spectrum due to frequency quantization is shown in Fig. 4-20. The spectrum shows that the quantization noise is below the DCO natural noise when Δf_{res} is less then 100kHz. This result suggests that the DCO frequency gain K_{DCO} should be below 100kHz/LSB. Besides, as also mentioned in chapter 3, smaller $K_{DCO}\alpha$ and thus K_{DCO} can reduce the peaking in the phase noise spectrum and thus improves the jitter performances. However, the finest frequency step achievable by switching a minimum size varactor is about 120kHz when tank inductance is 1.2nH. Finer resolution can be accomplish by means of high-speed ΣΔ dithering [15]. Due to the wordlength limitation of the digital dithering circuit, there will still be a phase noise contribution due to the finite resolution per equation 4-10, with $\Delta f_{res}=\Delta f_{res,I}/2^{WF}$. Where $\Delta f_{res,I}$ is the frequency step without utilizing ΣΔ dithering and WF is the wordlength of the dithering circuit.

Due to the noise shaping capability of the ΣΔ modulator, the quantization noise energy induced by the finite frequency step Δf_{res} is moved toward the high

frequency offset at the RF output. The phase noise spectrum due to the ΣΔ-shaped frequency deviation is [15]

$$L_{\Delta\Sigma}(\Delta f) = \frac{1}{12} \times \left(\frac{\Delta f_{res}}{\Delta f} \right)^2 \times \frac{1}{f_{dth}} \times \left(2 \sin \frac{\pi \Delta f}{f_{dth}} \right)^{2n}, \qquad (4\text{-}12)$$

where f_{dth} and n denote the sampling frequency and the order of the ΣΔ modulator, respectively. f_{dth} is normally much higher then f_{REF} and can be easily derived from the DCO by dividing the DCO output signal. Fig. 4-21 shows the phase noise spectrum due to ΣΔ-shaped frequency quantization with different dithering frequency f_{dth}. The 2nd ΣΔ modulator is assumed to plot this figure. It can be seen that the ΣΔ-shaped quantization noise is below the DCO natural noise with a margin of 5dB when f_{dth} is higher than 312MHz (divided-by-32 of the DCO output).

Fig. 4-22 shows the phase noise spectrum due to ΣΔ-shaped frequency quantization with 2nd and 3rd order ΣΔ modulator. Despite of the low in-band noise for 3rd order ΣΔ modulator, the noise energy appeared in high frequency

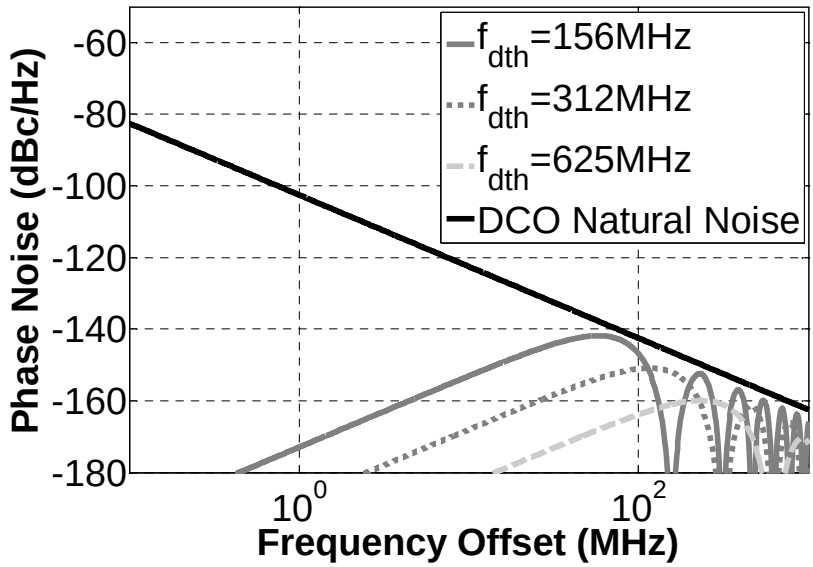


Fig. 4-21 Phase noise due to ΣΔ-shaped frequency quantization with different dithering frequency.

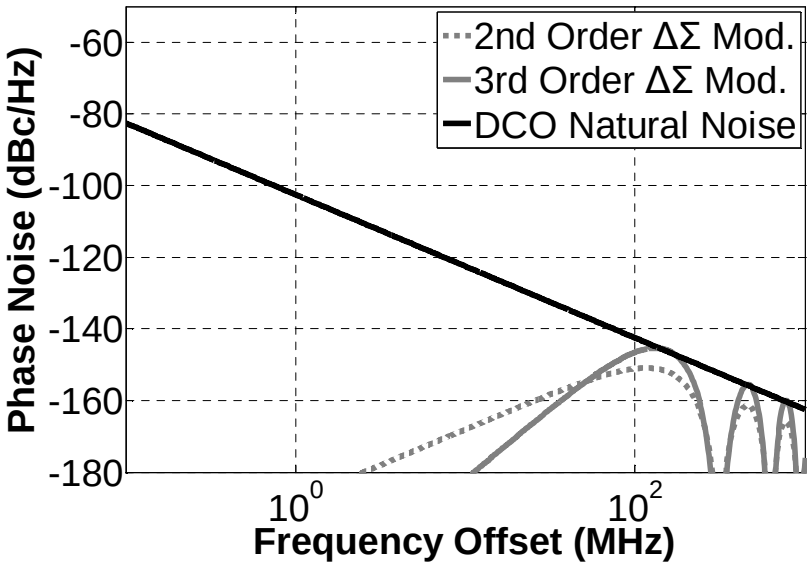


Fig. 4-22 Phase noise due to ΣΔ-shaped frequency quantization with different order of ΣΔ modulator.

offset rises over the DCO natural phase noise. Consequently, a 2nd order ΣΔ modulator triggered by the divided-by 32 of the DCO output is selected in this design.

In order to lower the area and the parasitic capacitance of the varactor bank, the whole bank is divided into 3 different weighted sub-banks. As shown in Fig. 4-17, the varactor bank incorporating 7-bits binary-weighted coarse tuning to cover the required tuning range and a 10-bits unity weighted fine tuning to ensure linearity. The layout of the coarse tuning bank is constructed with 128 identical NMOS varactors and each control signal drives different number of the varactors. For instance, $C_{DCO}[17]$ drives a single varactor while $C_{DCO}[18]$ controls a pair of the varactors.

In order to optimize the area usage, the 10-bit fine tuning bank is organized in the matrix of the elementary cells. As shown in Fig. 4-25, each cell includes a local decoder and two varactors with shorted drain and source terminals. The gate terminals of the 1024 cells are shorted together and AC coupled to the tank

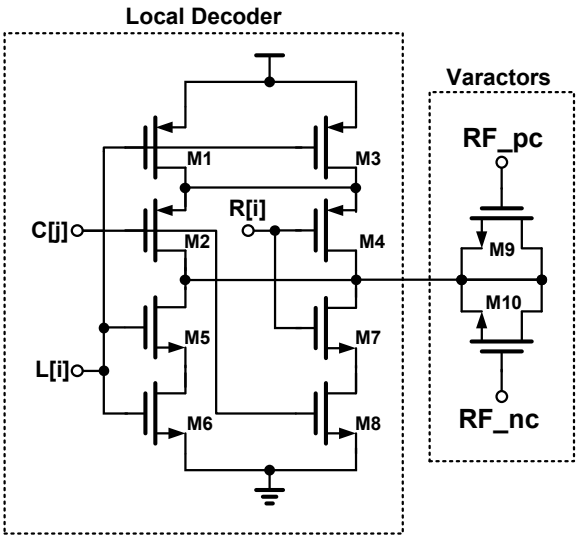


Fig. 4-23 Schematic of the fine tune cell shown in Fig. 4-17.

through a series capacitor Cs, which reduces the equivalent capacitance and enhanced the frequency resolution. Depending on the control signals R, L and C, each cell can be turned either into high capacitance mode or low capacitance mode. The condition for the cell to behaves as a large capacitance is

$$L[\mathrm{i}] + (R[\mathrm{i}] \cdot C[\mathrm{j}]) = 1. \qquad (4\text{-}13)$$

The binary weighted control code C_{DCO}[17:8] is first converted to thermometer code and then the tuning information R[31:0], L[31:0] and C[31:0] are latched to avoid glitches. The local logic implemented in the cells decode the row and column information in such a way that each odd row is filled up from column 1 to column 32, while each even row is filled up from column 32 back to column 1 of the matrix. The serpentine topology [4] and the dummy cells on the boundary of the matrix ensure the good matching between the elements in adjoining rows.

The structure of the ΣΔ modulator is illustrated in Fig. 4-24. It is implemented as digital second-order MASH-type architecture [15] which can be conveniently realized in digital domain by cell based design flow. Its output is

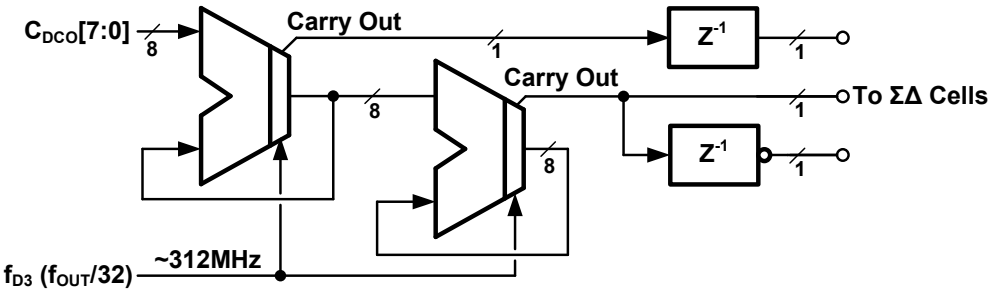
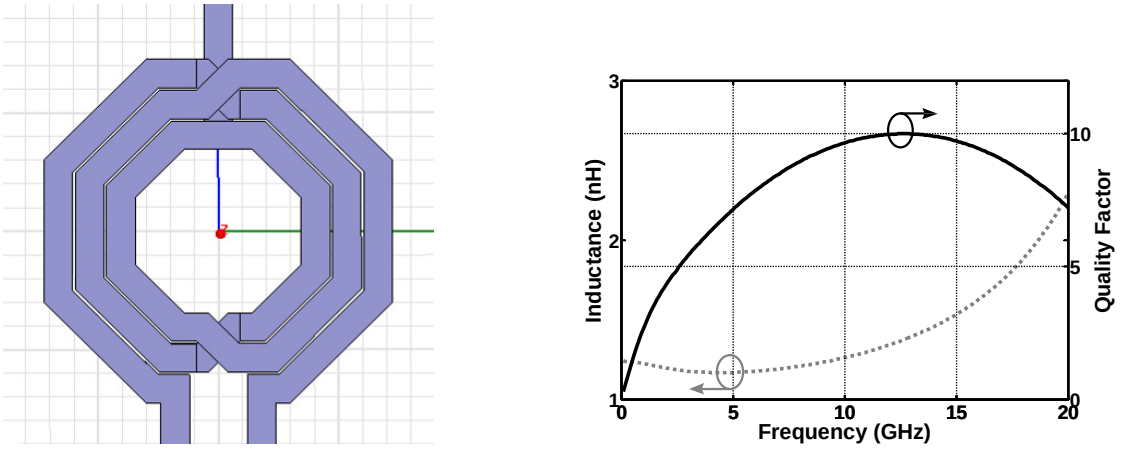


Fig. 4-24 Block diagram of the 2nd MASH-II order ΣΔ modulator.

fed to three ΣΔ cells which have the same structure as the fine tuning cell with R[i] and L[i] tie to 1 and 0, respectively. Table 4-1 reports the tuning characteristics of the DCO.

4.4.2 Inductor Coil

Due to the lack of the inductor models in the process development kit (PDK) of this 90nm mixed-mode CMOS process, a symmetric inductor coil with center tap is drawn and an EM simulation is taken to extract the characteristic of the inductor. In order to improve the quality factor, the top copper metal layer with 810nm thickness is used to construct the inductor. Also, the inductor layout is covered by some dummy-block layers to prevent automatic metal pattern filling procedure which is now standard in advance sub-micron process. Fig.



(a) (b)

Fig. 4-25 The layout view (a) and the EM simulation results (b) of the inductor.

4-25 shows the layout view, the inductance and the quality factor of the symmetric inductor. It can be seen from simulation results that the inductor has a quality factor of about 9 around 10GHz.

4.4.3 Simulation results of DCO

The time domain and frequency domain simulations are performed by

Table 4-1 Tuning characteristics of the DCO.

Varactor Bank	Weighting	Frequency Step
Coarse Tuning Bank	7-bit Binary	5MHz
Fine Tuning Bank	10-bit Unity	60kHz
ΣΔ Bank	3-bit Unity	235Hz

Hspice-RF. To accelerate the verification process, the varactor bank is substituted with a lamped model during simulations.

Fig. 4-26 shows the phase noise simulation result of the DCO, which reports -103dBc/Hz at 1MHz offset from a 10GHz carrier. The power

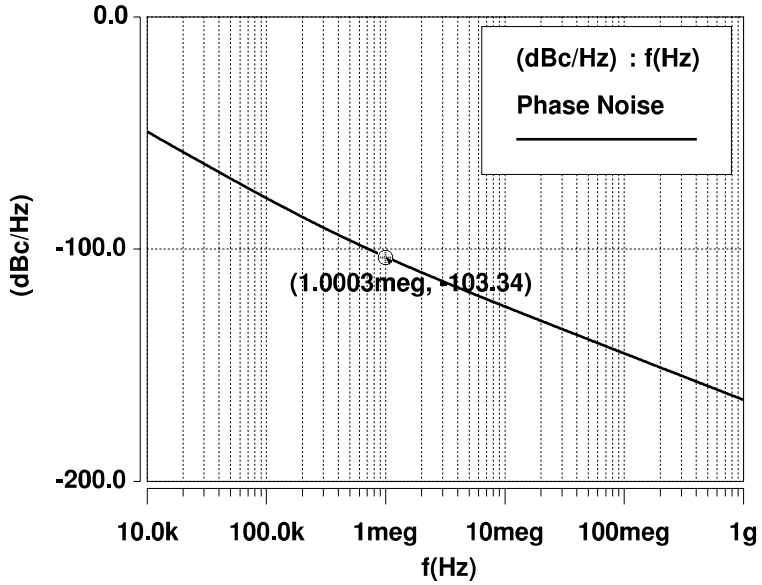


Fig. 4-26 Simulated phase noise performance of the DCO.

consumption is about 3.6mW in TT corner while delivering 900mV$_{pp}$ single-ended output swing.

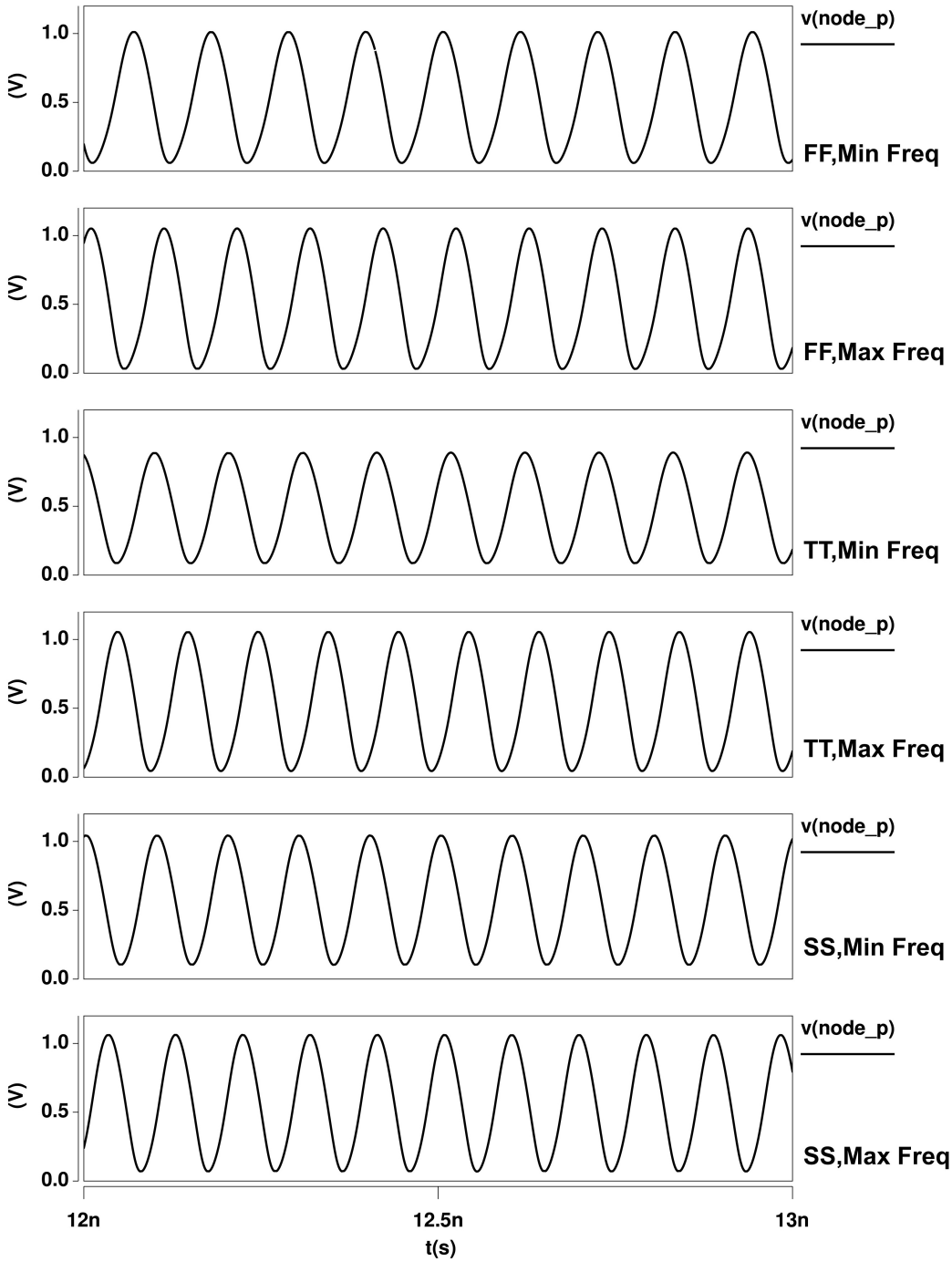


Fig. 4-27 Simulated time domain waveform of the DCO.

Table 4-2 summarized the tuning range and power consumption simulation results with different corner Table 4-2 reports the simulation results of the DCO

Table 4-2 Tuning characteristics of the DCO.

Case	$f_{OUT,max}$(GHz)	$f_{OUT,min}$(GHz)	Power (mW)
SS	10.877	10.274	3.50
TT	10.327	9.779	3.64
FF	9.9385	9.368	4.6

time domain waveform at its maximum and minimum operation frequency of SS, TT and FF corner.

4.5 Divided-by-4 Prescaler

The divided-by-4 prescaler is implemented as two cascade divided-by-2 frequency dividers. Each stage employs two D-latches in a master-slave configuration with negative feedback, as shown in Fig. 4-28 [13]. The top PMOS devices act as variable resistance loads, controlled by fin_p and fin_n.

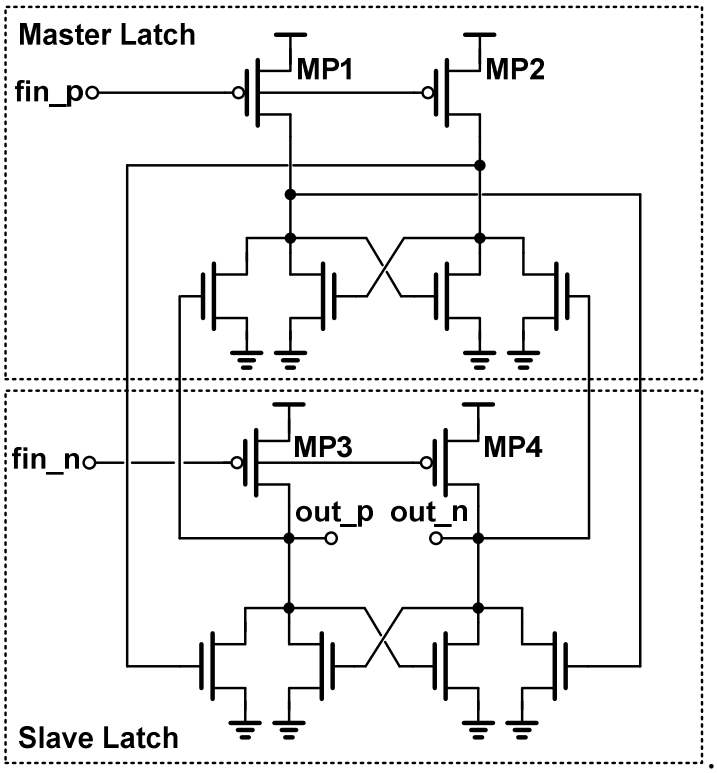


Fig. 4-28 Schematic of the divided-by-2 frequency divider [13].

Input and cross-coupled differential pairs are placed in parallel to accomplish sensing and regeneration action. It can be noted that there has no stacked devices and pass gates, which makes it to be suitable in low voltage operation.

The last divider stage is followed by a differential to single ended converter and inverter-based buffers. The simulation results of the prescaler are address in

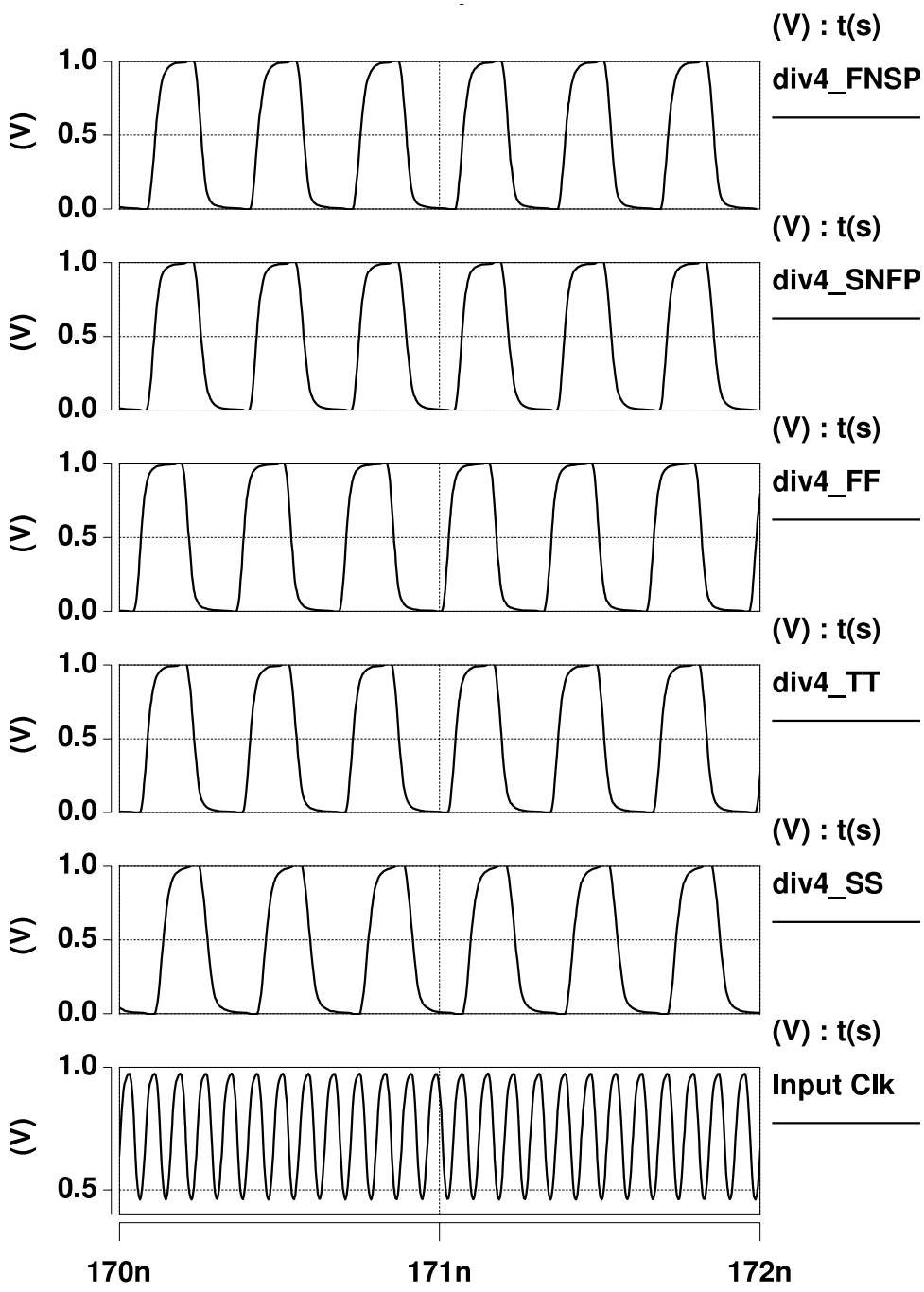


Fig. 4-29 Simulated time domain waveform of the divided-by-4 prescaler.

Fig. 4-29. The power consumption of the prescaler is 1.33mW in typical case when inputs a 2.5GHz sinusoidal signal.

Chapter 5 Experimental Results

5.1 IC Chip

Fig. 5-1 shows the die photograph of the ADPLL. The total silicon dimensions are about 0.9mm^2 (969μm × 93μm) including the bonding pads and digital I/O cells. The active area is about 0.352mm^2. Due to the automatic metal filling procedure which is now standard in the advanced CMOS process, there is not much to be seen from the chip photograph. Only some sensitive analog circuits such as inductor coil, MIM capacitors and the varactor bank have been excluded from the filling pattern to diminish the parasitic effects.

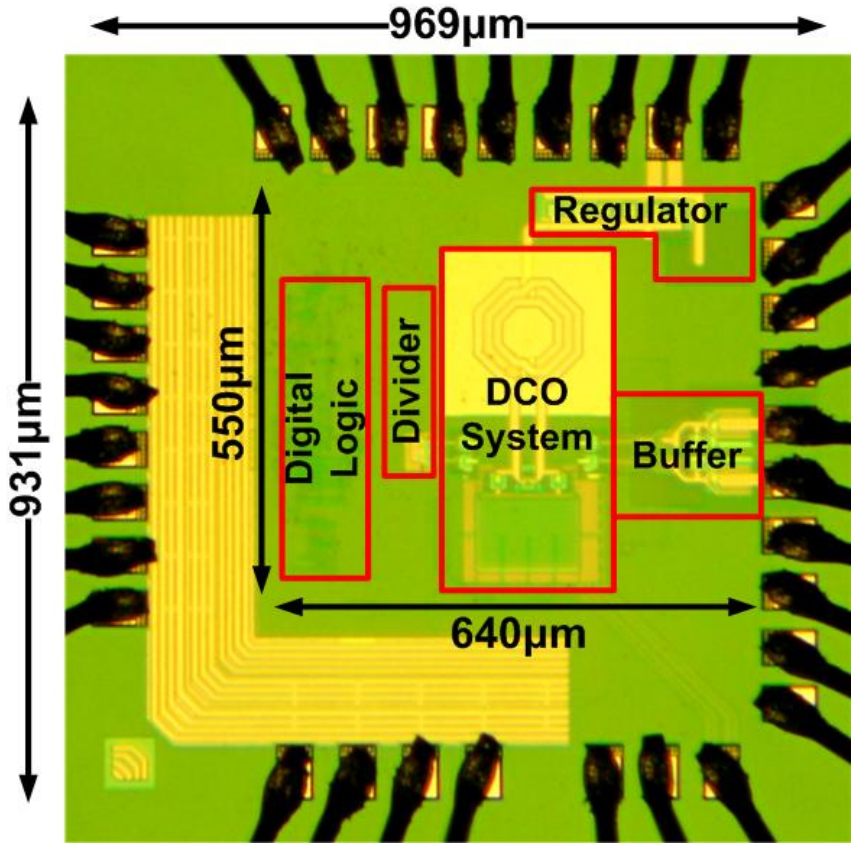
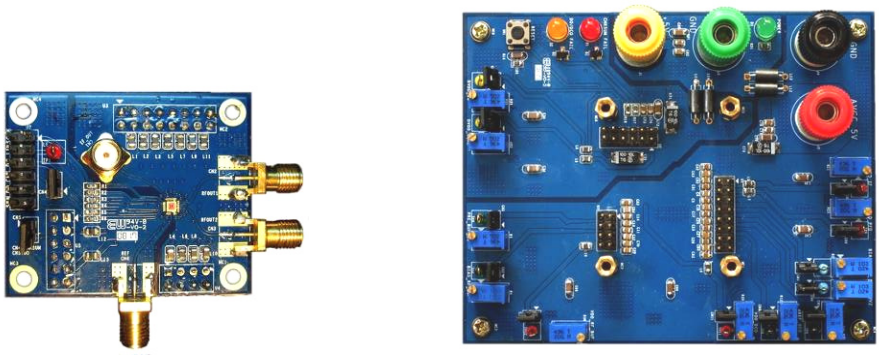


Fig. 5-1 Chip photograph of the implemented ADPLL.

5.2 Evaluation Board

To evaluate the performance of the implemented ADPLL, two printed circuit boards (PCBs) constructed of four layers have been built as shown in Fig. 5-2. Although placing the chip in package enables protection from stress and contamination while eases the connection between chip and printed circuit board (PCB), the package may degrade the chip performance especially in radio frequency applications. Thus, the chip is directly attached to the AC PCB (Fig. 5-2 (a)) and the I/O pads are connected to the signal traces on AC PCB through the bonding wires. The AC PCB is then mounted to the DC PCB (Fig. 5-2 (b)) which provides DC supplies and biases current for the test chip. As the result of the partition, it is facile to replace the test chip by simply substituting the AC PCB without re-soldering the regulator ICs and other passive components.

As shown in Fig. 5-2 (a), the die is located at the center-right of the AC PCB. The differential 10 GHz RF output, 40 MHz reference clock and the 1.25 GHz divided-by-8 clock are connected using subminiature version A (SMA) connectors, which provide DC to 18 GHz broadband performance with low



(a) (b)

Fig. 5-2 (a)AC PCB and (b)DC PCB for evaluating the chip

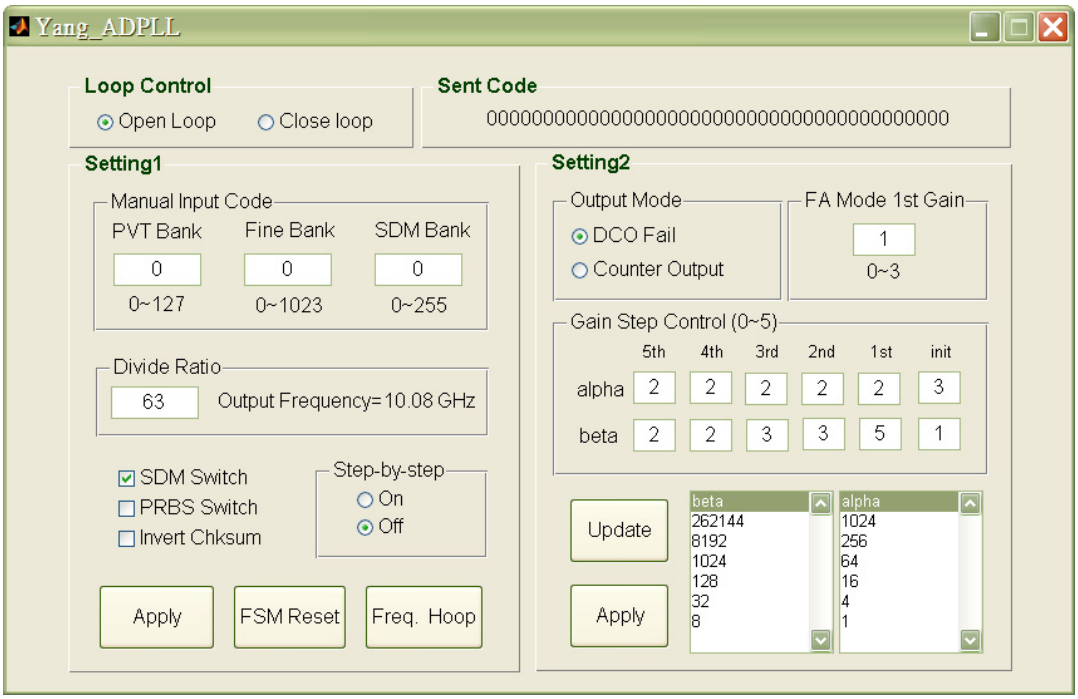


Fig. 5-3 GUI program for controlling the chip

reflections and constant 50-Ω impedance. The connector on the left-hand side attaches the AC PCB to an interface board (not shown), whose purpose is to control the chip by reading and writing its registers by means of a graphic user interface (GUI) program (Fig. 5-3) through the parallel port of the PC. The operation mode, the serial output mode, the initial DCO control code and the loop filter parameters of the synthesizer can be remotely controlled by the GUI program.

Three light-emitting diodes (LEDs) are used to indicate the power state, the output pin of the chip serial interface and the result of parity check which provides simple error detection of the input serial data. A push bottom is used as the reset bottom and its output is filtered by a low pass filter to solve key bouncing problem.

5.3 Measurement Setup

Fig. 5-4 shows the measurement environment setup and the equipments. The RF output and reference input clock are connected by SMA connectors with 50-Ω characteristic impedance. The 40 MHz reference clock is provided by an Agilent 8257D signal generator which has a phase noise of about -134 dBc/Hz at a 20 KHz offset. The 10 GHz differential RF outputs are first connected to the bias tees to provide current bias to the chip open drain buffer. The ac-coupled single-ended signal is then fed to the spectrum analyzer or the oscilloscope. The phase noise and spectrum of the closed loop PLL is measured using the Agilent E4448A with the option 226 phase noise measurement utility. The Tektronix DPO71254 real time oscilloscope with 12.5 GHz input bandwidth and up to 50 G sampling rate provides precise timing waveform and jitter measurement.

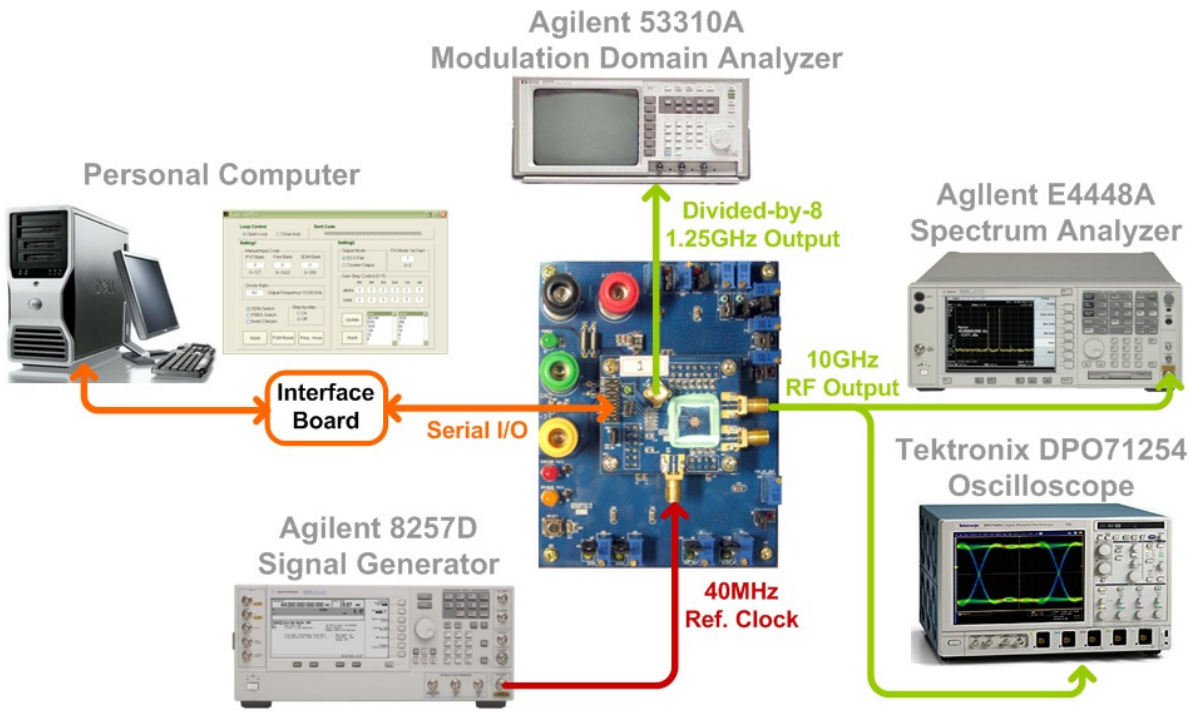


Fig. 5-4 Measurement setup of the test chip.

The frequency hopping time and modulation domain behavior are provided using Agilent 53310A modulation domain analyzer (MDA). Due to the input bandwidth limitation of the MDA, instead of the 10 GHz RF output, the 1.25 GHz divided-by-8 signal is used for measurement. The chip serial interface is connected to the PC parallel port for remote control through an interface board, which converts TTL signals of the parallel port to open collector signals while provides noise isolation between PC and the test chip.

5.4 DCO Measurement Results

5.4.1 DCO Tuning Curve

The DCO tuning curves have been characterized in open loop configuration by externally setting a 25 bits digital input code via the multiplexer in front of the DCO. The output frequency measurement is performed by the Agilent E4448A spectrum analyzer with internal frequency counter function. Since measuring the whole tuning curve of the DCO entails the programming of 2^{25}=33554432 different DCO control codes which consumes extremely long time to complete the measurement, the tuning curve of each varactor bank was characterized individually while kept other control code of other banks unchanged. The measurement process has been automatized using a PC with a GPIB IEEE488.1 interface card and a MATLAB program. The MATLAB routine generates sequentially all the input codes and provides the serial control data to the chip via the parallel port. After each code has been sent, the output frequency of the synthesizer is measured by the Agilent E4448A, and the result is communicated back through the GPIB interface to the PC. The results are automatically stores to the memory of the PC and can be post-processed by MATLAB. Higher

accuracy of the measurement is obtained by averaging up to 100 measurement results with the same DCO control code.

Linearity is important to have a value of K_{DCO} which is independent from the operating point of the BBPLL on the tuning curve. Nevertheless, more important is the uniformity of the minimum frequency step, or, in other terms, the differential nonlinearity (DNL) of the tuning curve. Too large nonlinearity may cause unstable condition in locking process and would worsen the output jitter and spurious tone performance.

Under nominal conditions, the maximum (C_{DCO}=33554432) and minimum (C_{DCO}=0) output frequency measured are 10.2GHz and 9.78GHz, respectively. Fig. 1 5 shows the measured tuning characteristics of the DCO versus different control codes of coarse tuning bank C_{DCO}[24:18] while the control code of fine tuning bank C_{DCO}[17:8] and ΣΔ bank CDCO[7:0] is set to 2'b1000000000 and 2'b10000000. Due to the digital tuning scheme which does not suffer from the highly nonlinear frequency versus voltage characteristics and low voltage headroom, it can be seen that the tuning curves are much more linear than the

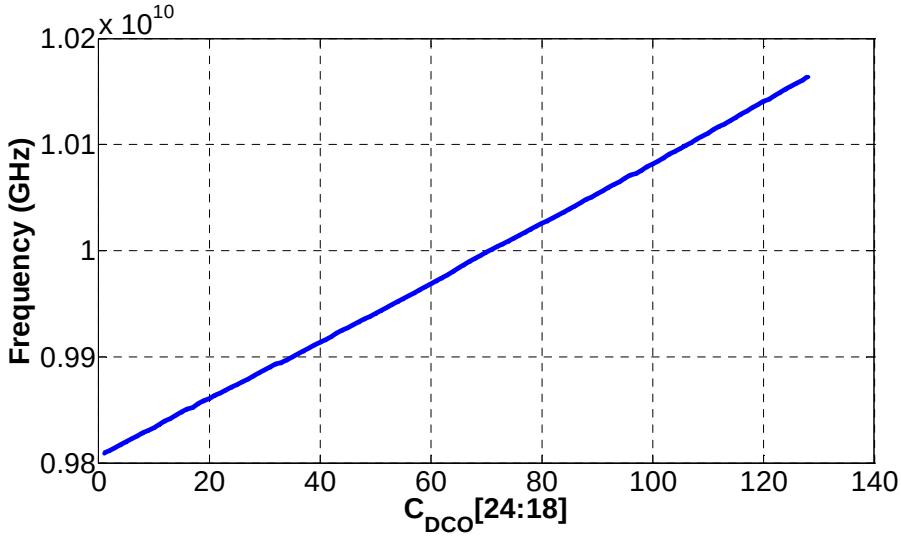


Fig. 5-5 Measured DCO frequency versus control code of coarse tuning bank C_{DCO}[24:18].

typical tuning curves of a conventional LC VCO. The measured average frequency step is 2.8MHz per LSB of coarse tuning bank and the DNL is less then 0.42LSB.

Fig. 5-6 and Fig. 5-7 report the DCO output frequency and the frequency step as functions of control code of the unity-weighted fine tuning bank

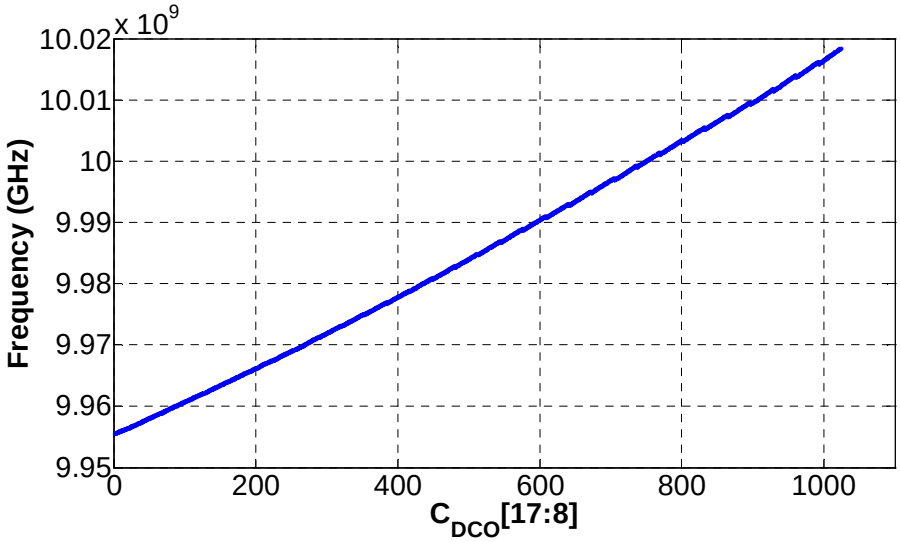


Fig. 5-6 Measured DCO frequency versus control code of fine tuning bank $C_{DCO}[17:8]$.

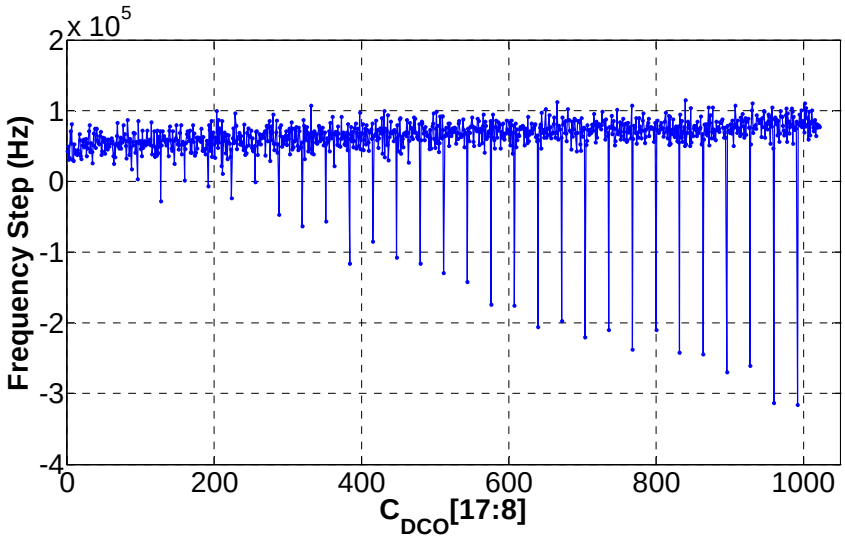


Fig. 5-7 Measured DCO frequency step versus control code of ΣΔ bank $C_{DCO}[17:8]$.

C_{DCO}[24:18]. As expected, the higher the carrier frequency, the larger the fine-tuning step. The average frequency step measured is about 75kHz per LSB of fine tuning bank. Several big jumps can be noticed for tuning words related to multiples of 32 (32-64-96…) because of the fact that each row in the varactor bank is built up of 32 elements. This behavior can be explained by noting that for those values, the active varactors are always at the border of the matrix and matching problems arise. When the varactor is switching from the last cell of one row to the first of the next row, the control lines r and l change their status at the same time, leading to small change of the parasitic capacitance of the next row. It also shows that the use of dummy cells and turning on the cells of the array in a meander way are not sufficient to improve this side effect. To solve the problem, special care must be taken in the layout matching and the design of the decoder.

Fig. 5-8 shows the tuning characteristics of the ΣΔ bank. The tuning curve is nonlinear and non-monotonic, which mainly arise from the mismatch of the varactor cells and the timing misalignment of the driving clocks. More effort

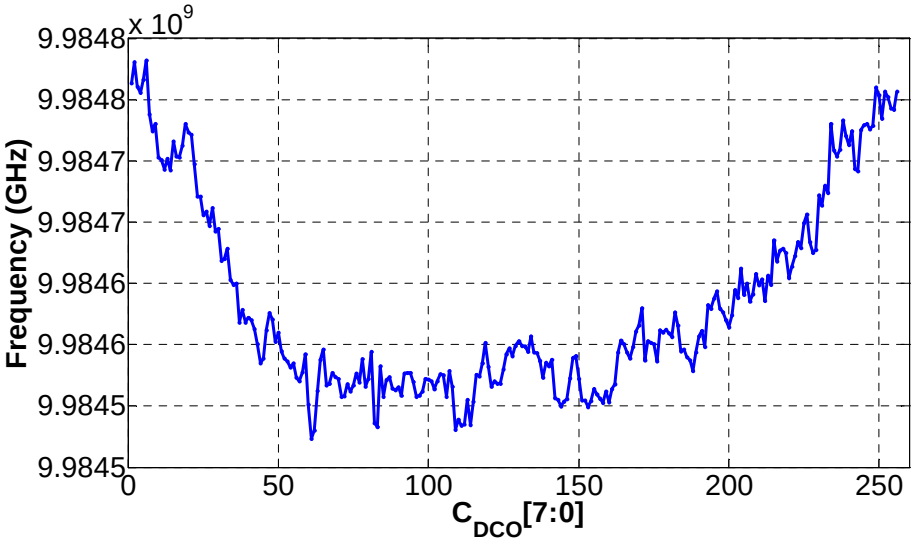


Fig. 5-8 Measured DCO frequency versus control code of ΣΔ bank C_{DCO}[7:0].

must be taken in the layout technique to improve the matching of the cells. The use of dynamic element matching (DEM) may be helpful to solve this issue.

5.4.2 Open loop DCO phase noise

Fig. 5-9 shows the phase noise plot of the free running DCO at 9.98GHz, measured with Agilent E4448A spectrum analyzer with phase noise personality. The measurement results are (-102dBc/Hz at 1MHz offset) agreed with the simulation counterpart where the phase noise at 1MHz offset is about -103 dBc/Hz. Better phase noise value is obtained for higher output frequency where the varactor banks are in low capacitance mode. When the MOS in the varactor bank enters inversion mode, the energy loss due to the effective resistance of channel and metal connections would increase. Thus, the quality factor of the LC tank reaches its minimum value at high capacitance state when the output frequency is lowest.

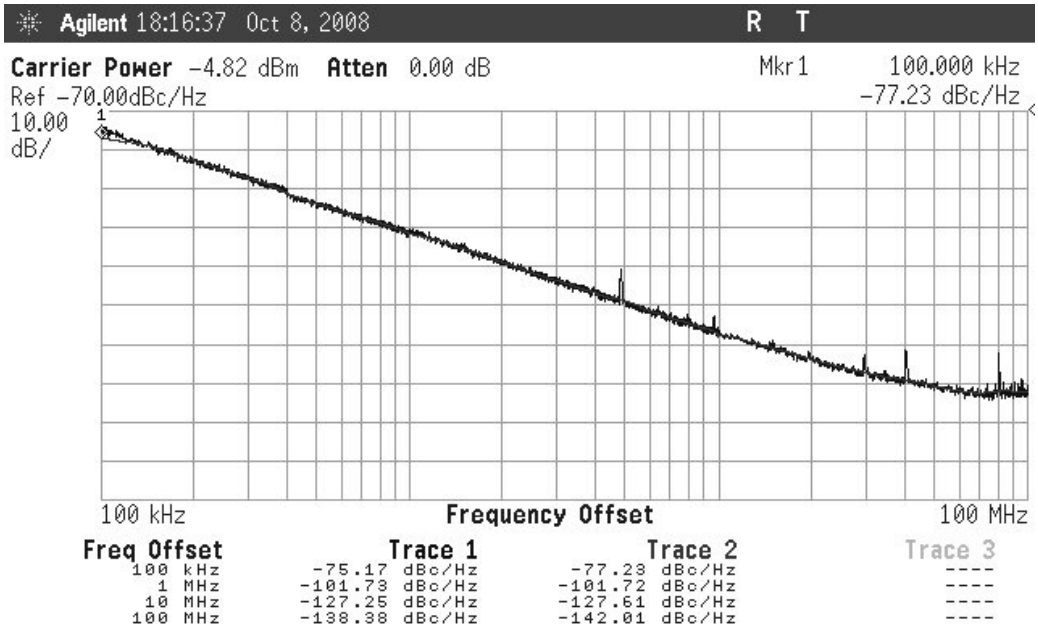


Fig. 5-9 Measure open loop phase noise from 9.98GHz carrier.

5.5 Closed-Loop Performance

5.5.1 Output Spectrum

In order to measure the output spectrum of the closed-loop ADPLL, the system has been reconfigured to a close-loop scheme and the multiplication factor N has been set to 248 and 252 via the on-chip serial interface. Since the reference clock is 40 MHz, the output frequency is 9.92GHz and 10.08GHz.

The measured closed-loop output spectrum of the ADPLL is shown in Fig. 5-10 for 9.92GHz carrier and in Fig. 5-11 for 10.08GHz carrier. The frequency span is 100MHz and the resolution bandwidth is set to 10 kHz. The measured RF output power from 9.92GHz and 10.08GHz carrier are -5dbm and -7dbm. The reference spurs (at 40MHz offset) with mark 3 are below -72dBc in the

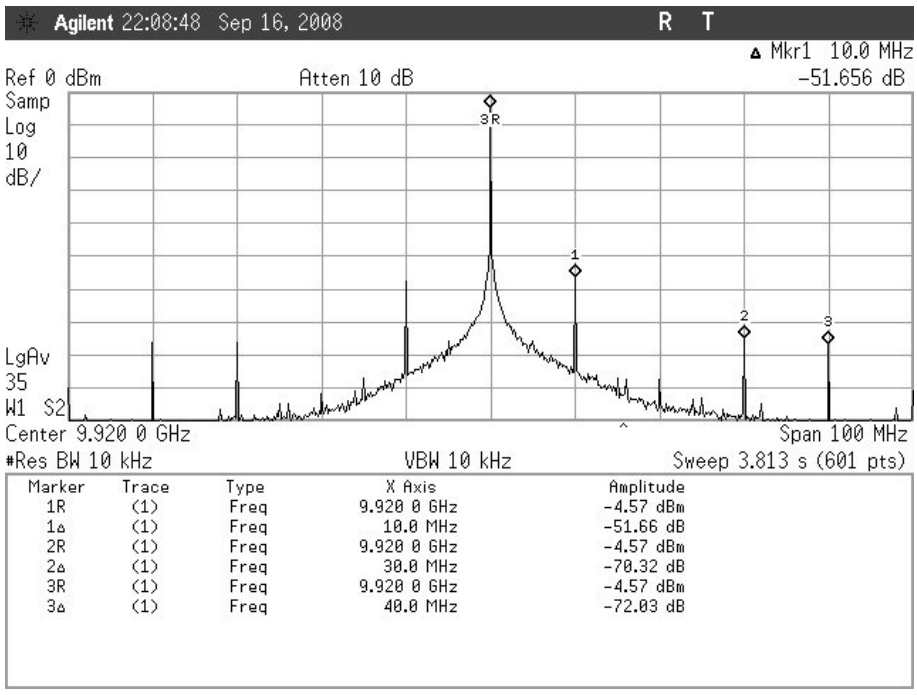


Fig. 5-10 Measured synthesizer output spectrum of 9.92GHz carrier with α=1 and β=256.

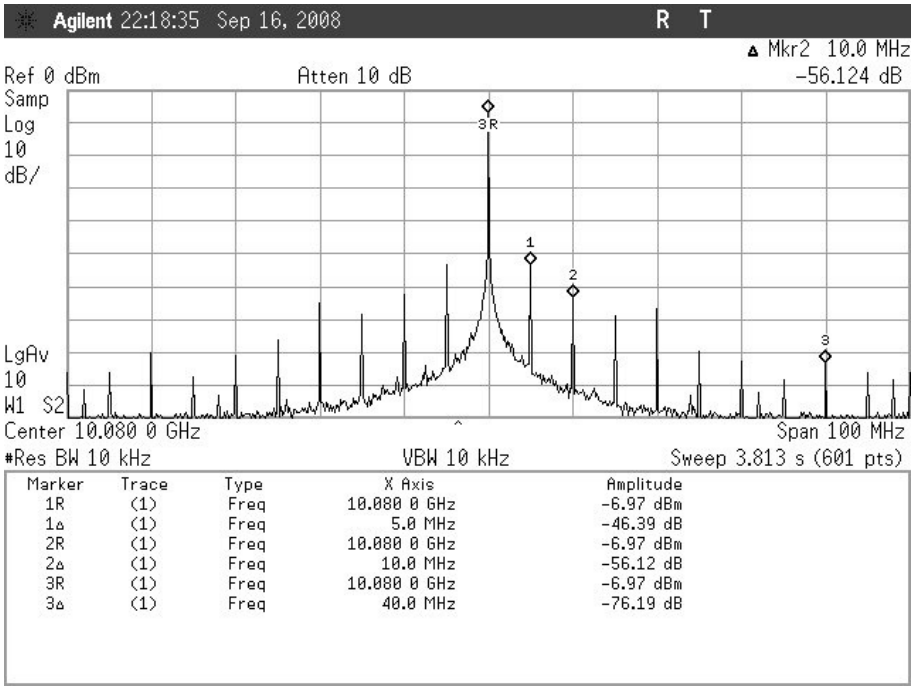


Fig. 5-11 Measured synthesizer output spectrum of 10.08GHz carrier with α=1 and β=256.

cases of both 9.92GHz and 10.08GHz output. The close-in spurious tones with mark 1 and mark 2 are due to the bang-bang cyclic oscillation in the steady-state resulted from hard nonlinearity of the binary phase detection. Due to the presence of the nonlinear characteristics of the DCO tuning curve, there are some differences in the position of the spurious tones between Fig. 5-10 and Fig. 5-11.

The magnitude and the position of these cyclic tones are mainly determined by the forward path gain β and the loop latency. As mentioned in chapter 3, the loop delay impacts the period and amplitude of the tracking trajectory of the loop and thus influences the spurious tone generation. Larger β makes the wider frequency variation every time the polarity of the phase detector output reverses and increases the magnitude of the spurs. With different β values and constant α value, the measured spectrums of the ADPLL from the 9.92GHz carrier are

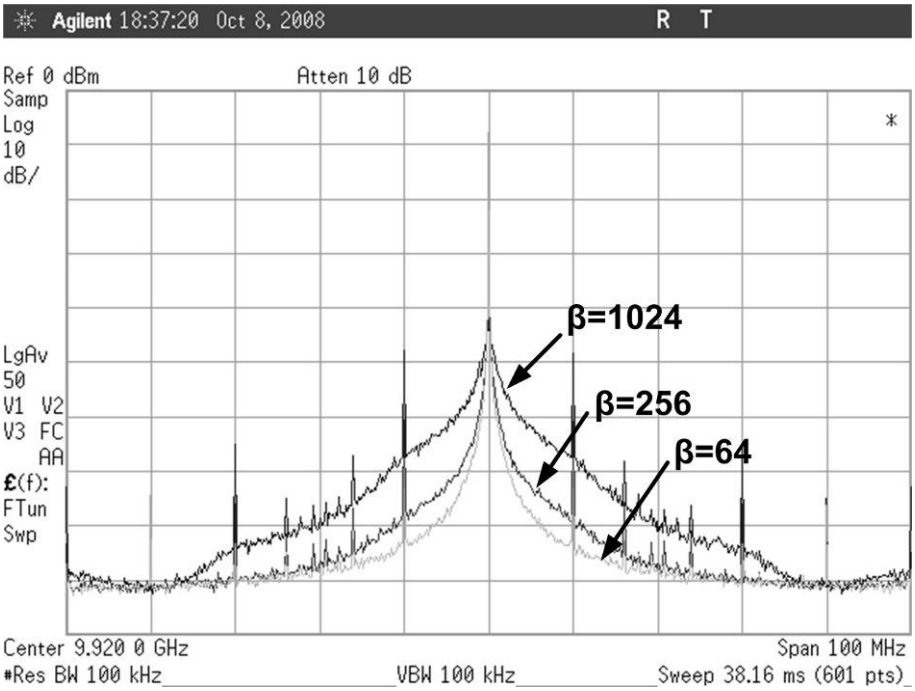


Fig. 5-12 Output spectrum of β=64,256 and 1024.

shown in Fig. 5-12. It can be seen that the larger the β value, the higher the spurious tones power. However, the power of the reference spur is almost constant with different β. The emitted power spurious tones are below -60dBc when β is reduced to 64.

5.5.2 Output Phase Noise

Fig. 5-14 and Fig. 5-13 report the measured phase noise of the PLL from the 9.92GHz and 10.0 GHz carrier respectively. With α=1 and β=256, the loop bandwidth is about 200kHz. The output phase noise at 1MHz and 10MHz offset is about -100dBc/Hz and -120dBc/Hz. It could be seen that the frequency components within loop bandwidth undergo 20 dB/decade attenuation such that the up-converted thermal noise is flat.

In Fig. 5-15, the phase noise measured from 9.92GHz carrier is reported for 4 different α and β combinations. It should be note that increasing β with constant α leads to a broader spectrum or a wider loop bandwidth while

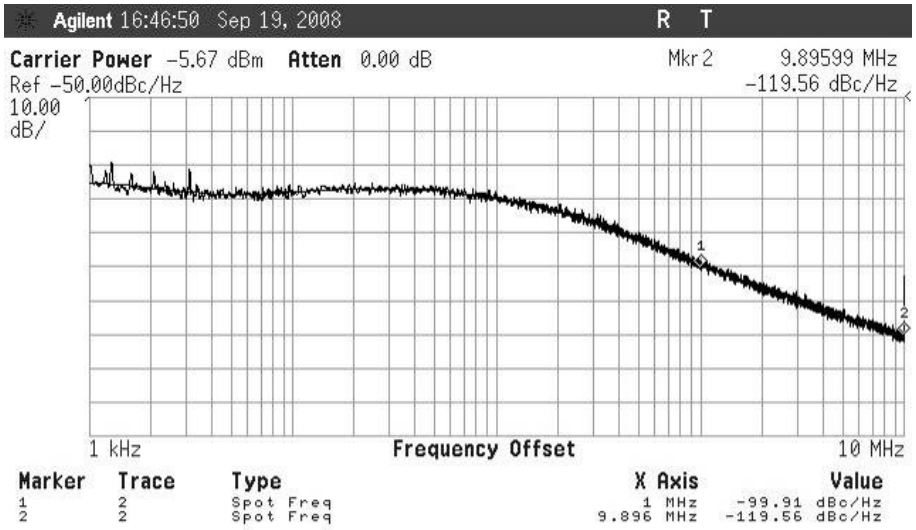


Fig. 5-14 Measured phase noise for 9.92GHz output with α=1 and β=256.

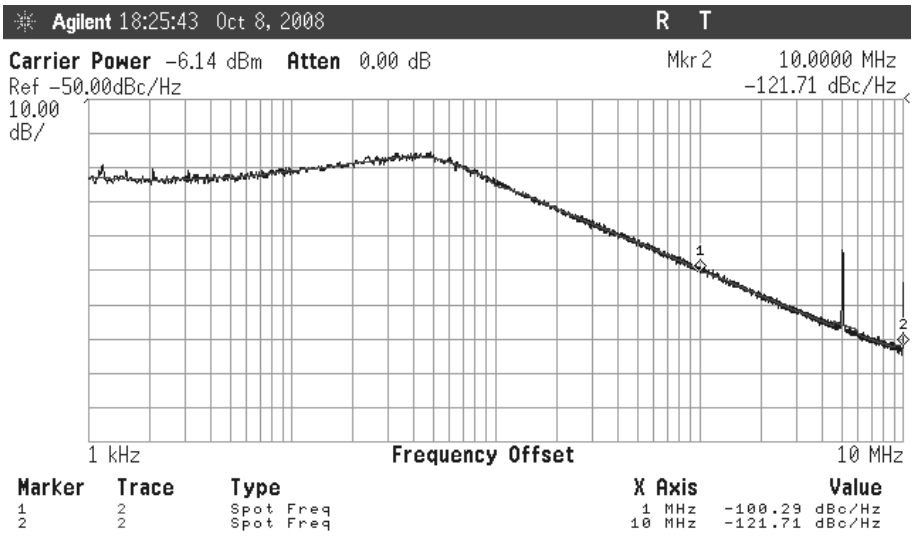


Fig. 5-13 Measured phase noise for 10.08GHz output with α=1 and β=256.

increasing α with β constant drives the BBPLL closer to the instability limit, thus introducing the peaking in the phase noise plot and degrading the output jitter performance.

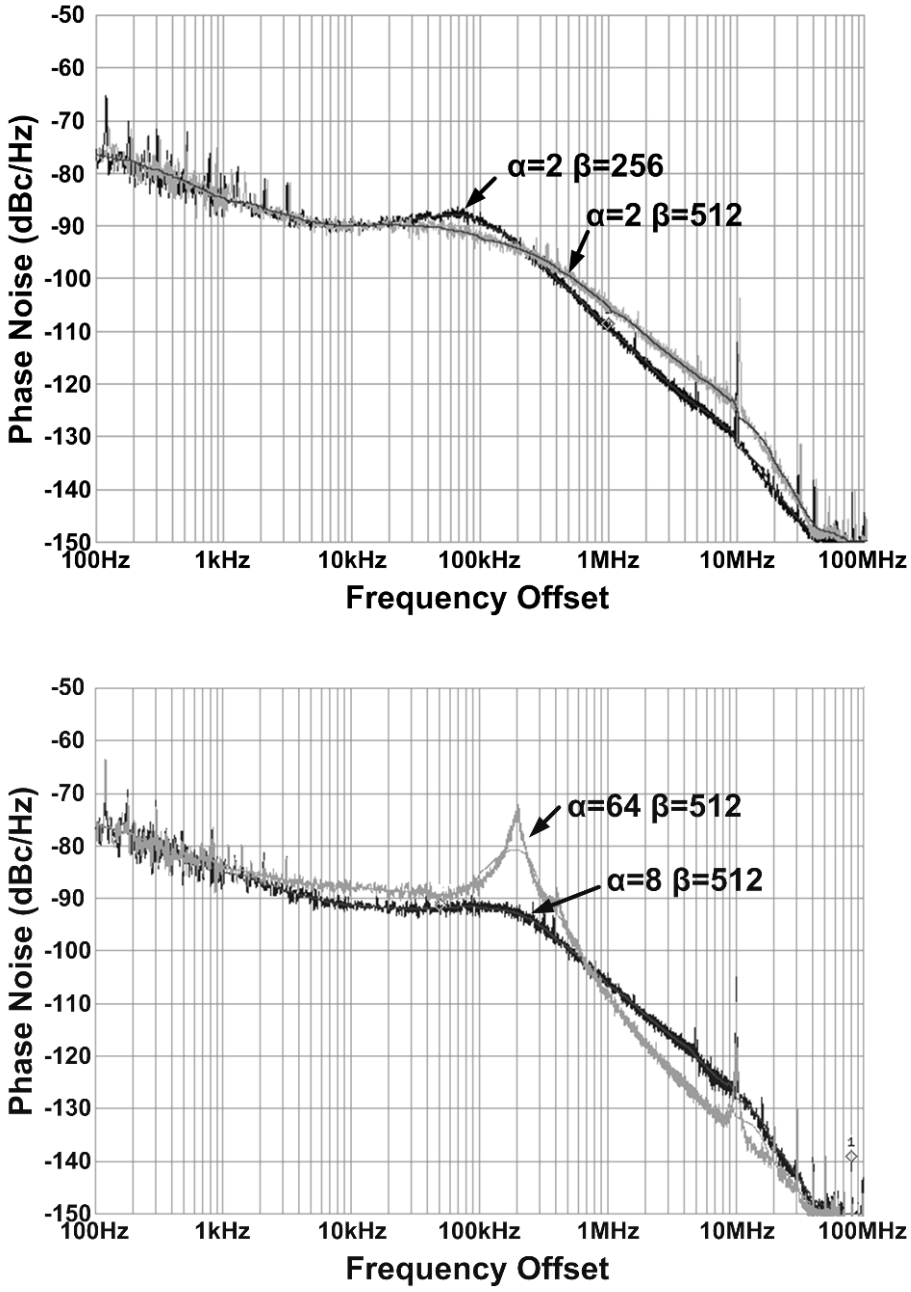


Fig. 5-15 Measured phase noise for 4 different loop filter setting.

5.5.3 Jitter Performance

Fig. 5-16 to Fig. 5-19 report the time domain waveforms of 9.92GHz and 10.08GHz, measured by Tektronix DPO71254 real-time oscilloscope with 12.5GHz input bandwidth. The best rms jitter achieved is about 0.9ps from the 9.92GHz carrier, including the trigger jitter of the instrument for about 100fs (rms). Due to the higher multiplication number and the nonlinearity of DCO

tuning curve, the phase noise for 10.08GHz output at low frequency components is higher then that of 9.92GHz output, which leads to degrading of jitter performance. For this reason, larger rms jitter is observed from the 10.08GHz output which is about 1ps.

Fig. 5-20 reports the measured rms jitter from 9.92GHz clock as the function of different β values while keeping α=1. The result shows that for β>512, the smaller β causes the loop to be close to the boundary of instability and narrower the loop bandwidth which make the rms jitter increases exponentially. However, further increasing the β value makes the loop dynamics to be dominated by quantization step in the proportional path, leading to linear increasing of the output jitter.

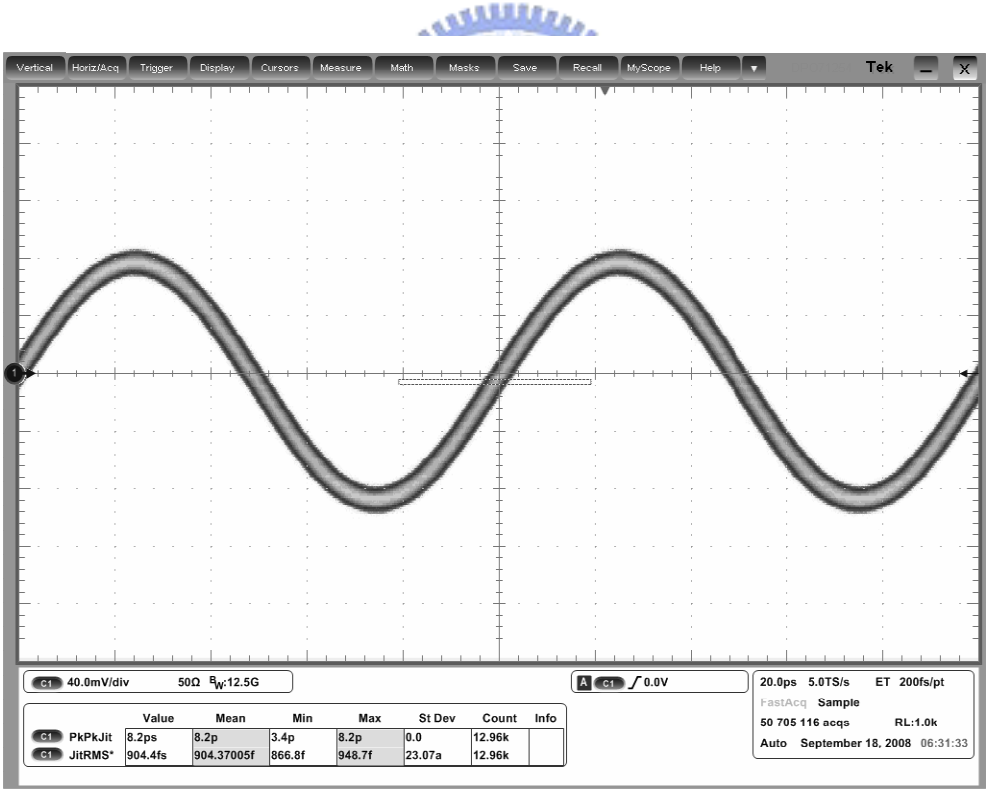


Fig. 5-16 Measured output waveform from 9.92GHz carrier with α=1 and β=256. The rms jitter is 904fs.

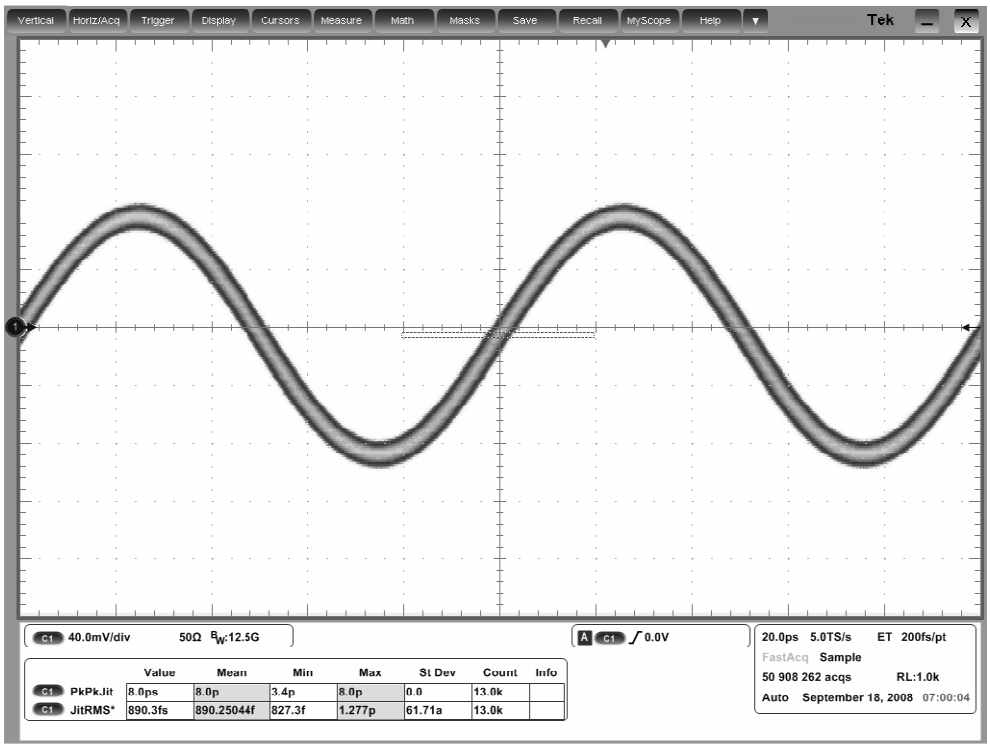


Fig. 5-17 Measured output waveform from 9.92GHz carrier with α=1 and β=512. The rms jitter is 890fs.

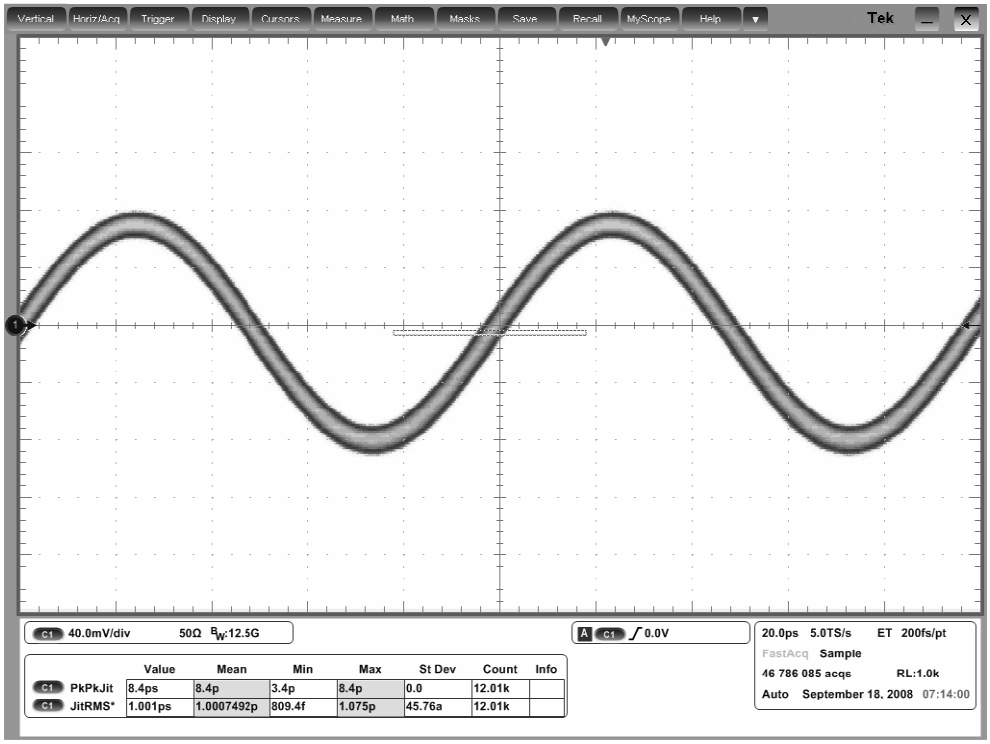


Fig. 5-18 Measured output waveform from 10.08GHz carrier with α=1 and β=256. The rms jitter is 1001fs.

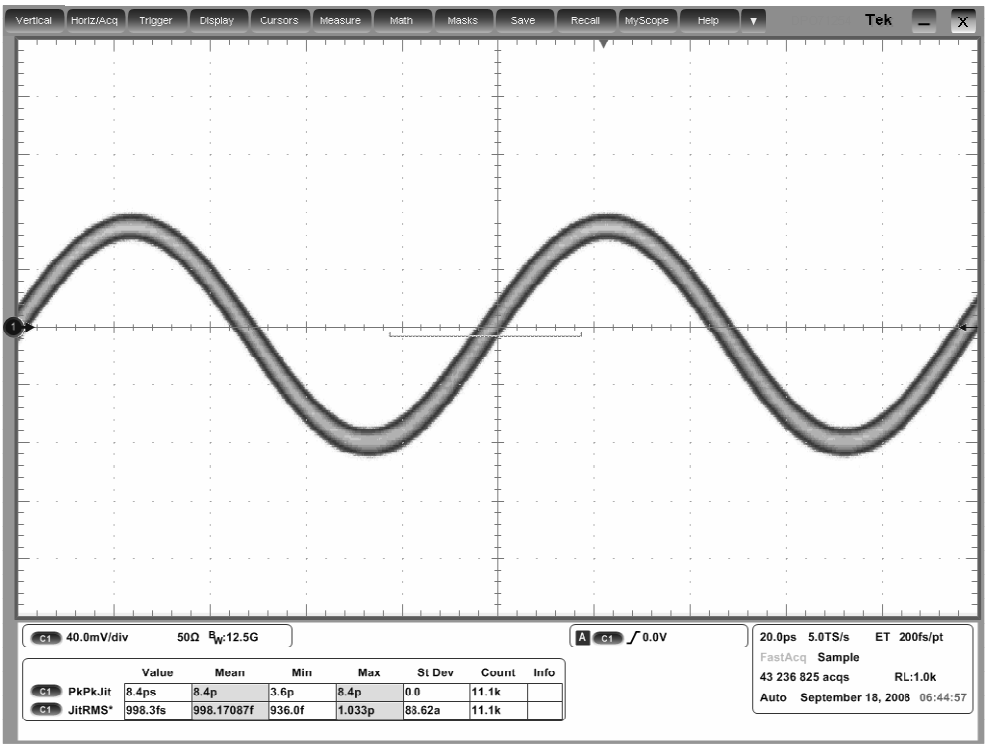


Fig. 5-19 Measured output waveform from 10.08GHz carrier with α=1 and β=512. The rms jitter is 998fs.

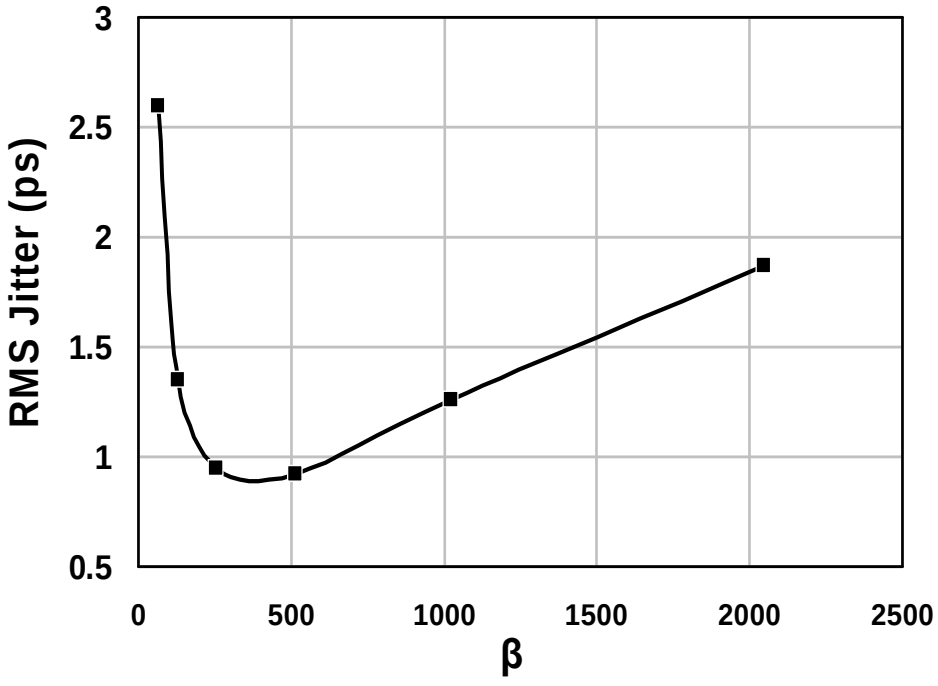


Fig. 5-20 Measured rms jitter from 9.92GHz carrier with constant α and different β values.

5.6 Locking Behavior

For locking behavior characterization, the divide-by-8 output is measured to meet the bandwidth of the modulation domain analyzer (Agilent 53310A). The multiplication ratio N is first reconfigured from 62 to 63 via the serial interface. After a reset signal of the finite state machine is received, the new N value is loaded and the locking procedure is resumed. The modulation domain analyzer demodulates the input clock as a FM signal and displays the result when a user defined frequency value is presented.

When the output frequency hops form 9.92GHz to 10.08GHz, the measured settling time within 20ppm accuracy is about 6.89μs, as is shown in Fig. 5-21. A zoomed in version of the settling behavior is also shown in Fig. 5-22. Fig. 5-23 reports the measured tuning behavior of the DCO control code during the frequency hoping from 9.92GHz to 10.08GHz. After 5μs of the locking process,

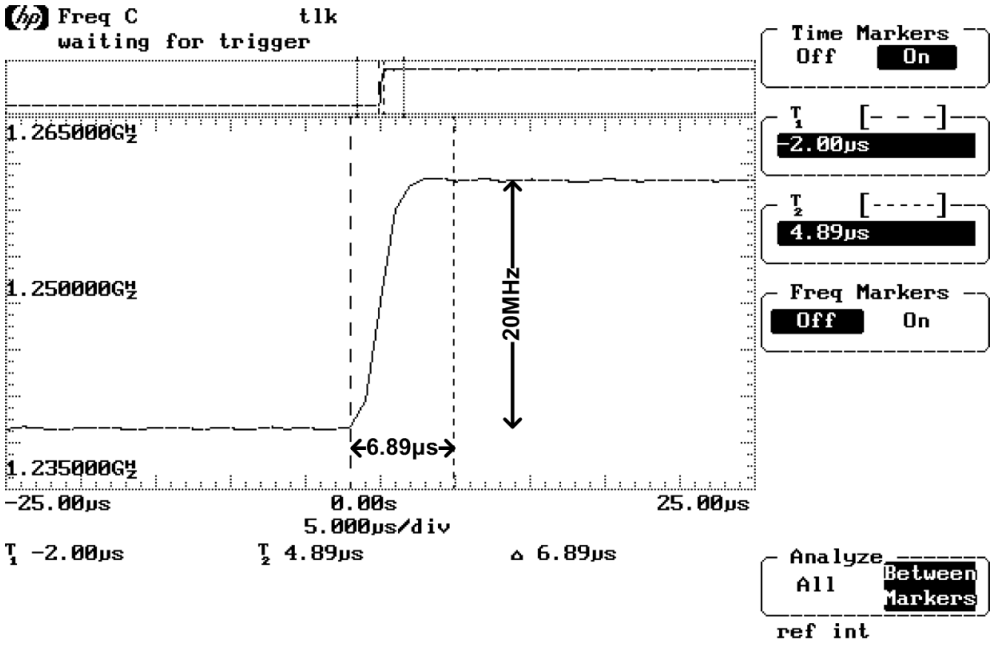


Fig. 5-21 The measured settling time for the output frequency changes from 9.92GHz to10.08GHz (divided-by-8 clock changes from 1.24GHz to 1.26GHz).

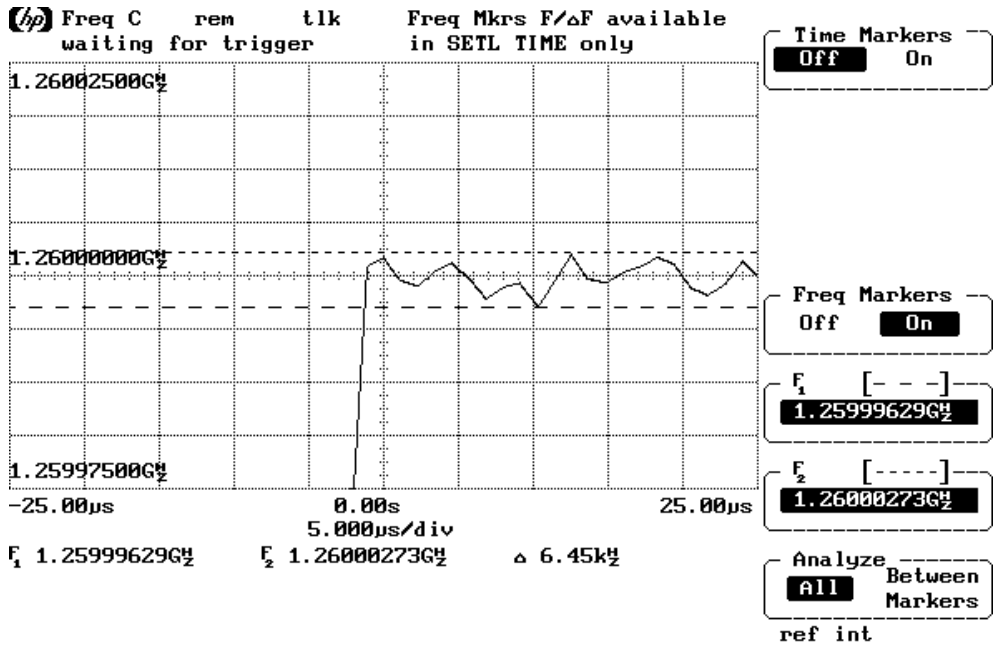


Fig. 5-22 Zoomed in version of the measured settling behavior.

the measured peak to peak control code difference is corresponding to 331 kHz frequency variation, which is within 20ppm accuracy of the target frequency.

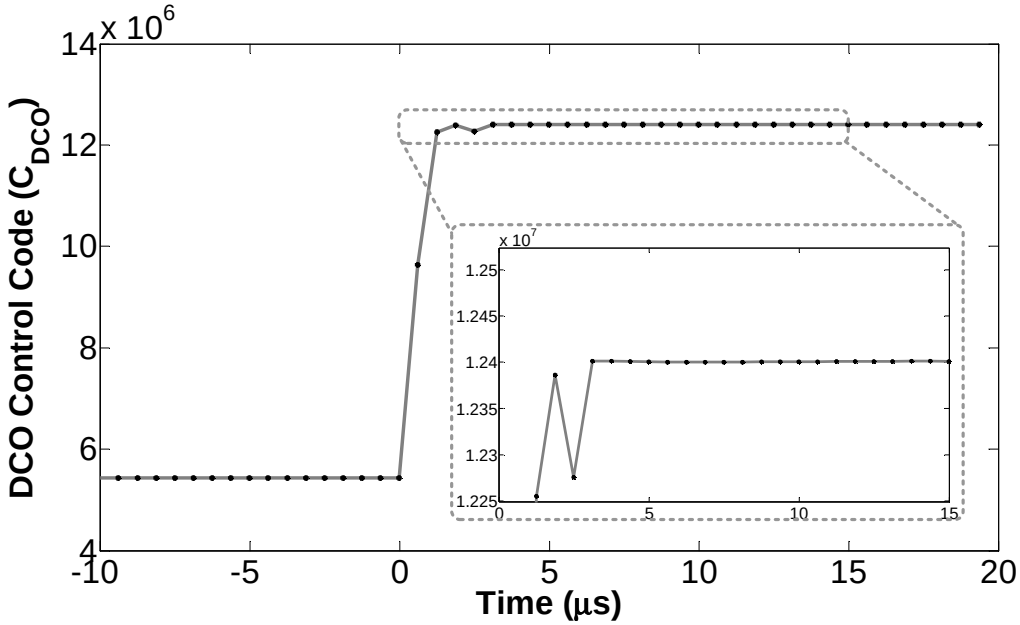


Fig. 5-23 The measured DCO control code during frequency hopping.

5.7 Performance Summary

The power consumption of the implemented chip is summarized in Table 5-1 and Fig. 5-24. It is clear from the results that the 10 GHz output buffer composed of 4 cascade CML stages and the 1.25 GHz divided-by-8 clock buffer dominant the total power dissipation. The ADPLL core circuits consume 7.1 mW from a 1V supply, and the digital IO cells drain 2.7 mW from a 3.3V supply for chip measurement. The measurement results are summarized and compared with the state-of-the art ADPLLs reported in recently year, as shown in Table 5-2. The proposed architecture manifests the highest output frequency, fastest locking time, and highest power efficiency.

Table 5-1 Summary of the power consumption

Circuit Items	Power Consumption (mW)
Digital IO Cells (3.3V supply)	2.7
Digital Logic	0.9
DCO System	3.9
1/4 Prescaler & High Speed Counter	2.3
RF Output Buffer & Divided-by-8 Clock Buffer	41.4

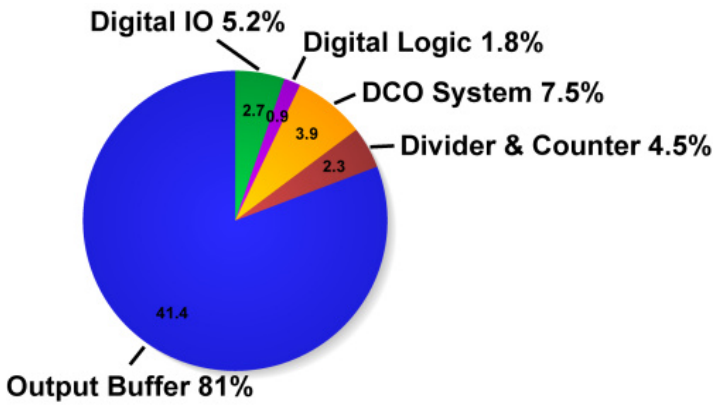


Fig. 5-24 Pie chart of the chip power distribution

Table 5-2: ADPLL performance benchmark

Reference	Tech.	Supply	Power	Frequency range	Phase Noise	Locking Time	Reference Frequency/ Multiplication Factor
[16] 05' JSSC	90nm	1.2V	19.6mW(1) (4.9 mW/GHz)	3.2GHz~4.0GHz	-165dBc/Hz @ 20MHz(2)	10μs	26MHz (N=31.7)
[4] 05' JSSC	130nm	1.5V	19.5mW (4.02 mW/GHz)	2.08GHz~2.25GHz 3.16GHz~3.66GHz 4.1GHz~4.85GHz	-118dBc/Hz @1MHz	N/A	200MHz (N=24)
[17] 08' JSSC	65nm	0.9V	17.2mW (3.37 mW/GHz)	0.5GHz~5.1GHz	-112dBc/Hz @1MHz(3)	N/A	500MHz (N=8)
[18] 08' ISSCC	130nm	1.5V	39mW (NA)	N/A	-132dBc/Hz @3MHz	20μs	50MHz (N=74)
[19] 08' ISSCC	130nm	N/A	40mA (10mA/GHz)	3.2GHz~4.0GHz	-126dBc/Hz @1MHz	N/A	26MHz (N=138.98)
This Work	90nm	1.0V	7.1mW (0.71 mW/GHz)	9.75GHz~10.17GHz	-100dBc/Hz @1MHz	6.9μs	40MHz (N=248)

(1)Power dissipation for DCO and time-to-digital converter only
(2)Measured from 900 MHz carrier
(3)Measured from 4 GHz carrier

Chapter 6 Conclusions

This work demonstrates a 10GHz all digital frequency synthesizer for the high speed serial data communication systems. With the dual mode phase detector, the loop rapidly locks to the target frequency and then reconstructs to a bang-bang PLL without resorting to the time to digital converter.

Governed by the proposed locking process monitor, the digital loop filter is automatically reconfigured and the loop bandwidth is self-adjusted during the frequency acquisition and phase tracking process. Less than 7μsec locking time and 0.9ps rms jitter including the trigger jitter of the oscilloscope have been measured.

A novel skew-compensated asynchronous phase accumulator is proposed, which preserves the advantage of low power dissipation of asynchronous counter while eliminating the accumulated timing skew issue.

A LC-DCO with a varactor bank incorporating 8-bits binary-weighted coarse tuning and 10-bits unity-weighted fine tuning to ensure linearity is presented. The frequency resolution is further enhanced by employing high speed dithering though an 8-bit MASH-11 ΔΣ modulator.

Using the UMC 90nm CMOS technology, the implemented prototype occupies only 0.352mm2 active area and manifests with power efficient of 0.71mW/GHz which is comparable with the state of the art frequency synthesizers.

Finally, because of the digital nature, the ADPLL can be further scaled down for future CMOS process and suitable in SOC designs.

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修習科目	類比積體電路(一)(二) 數位積體電路 有線傳輸通信積體電路設計 適應性訊號處理 數位通訊			
專業能力	類比電路設計 鎖相迴路設計	Full-Custom Design Flow Cell-Based Design Flow		
熟悉軟體	MATLAB/Simulink HSPICE Spectre RF Virtuoso Calibre	Verilog Design Vision SOC Encounter Office: Word, Excel, Power Point		
特殊表現	CIC 下線審查評鑑:B 斐陶斐榮譽會員 大三書券獎兩學期 大二書券獎兩學期			