國　立　交　通　大　學

電子工程學系　電子研究所碩士班

碩　士　論　文

60-GHz 互補式金氧半導體前端接收器之設計與分析

The Design and Analysis of 60-GHz CMOS Receiver Front-end

研 究 生：陳柏宏

指導教授：吳重雨 博士

中 華 民 國 九 十 六 年 七 月

60-GHz 互補式金氧半導體前端接收器

之設計與分析

The Design and Analysis of 60-GHz CMOS

Receiver Front-end

研究生：陳柏宏　　Student: Po-Hung Chen

指導教授：吳重雨 博士　　Advisor: Dr. Chung-Yu Wu

國立交通大學

電子工程學系

碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master

In

Electronics Engineering

July 2007

HsinChu, Taiwan, Republic of China

中華民國九十六年七月

60-GHz 互補式金氧半導體前端接收器之設計與分析

研究生：陳柏宏　　指導教授：吳重雨 博士

國立交通大學
電子工程學系 電子研究所碩士班

摘要

具有高操作頻率且高傳輸速率的通訊系統已被視為次世代通訊系統的主軸。在近幾年，60-GHz 附近的頻帶中，已有 7-GHz 的頻寬被釋出做為高速短距離通訊系統使用。此頻帶具有可應用在高達十億位元高傳輸速率的無線個人網路(WPAN)以及點對點傳輸上的潛力。

此論文中介紹了一個與三倍頻器整合的 60-GHz CMOS 直接降頻式接收器。此接收器包含了低雜訊放大器、降頻混頻器以及三倍頻器等電路，並且使用了 0.13-um CMOS 技術來設計並製造。藉由使用三倍頻器，所需要的頻率合成器之操作頻率可以由 60 GHz 降至 20 GHz，並使得頻率合成器的實現變得較為容易。根據量測結果顯示，此電路由於佈局時發生的錯誤，使得增益降至 13.9 dB。量測結果證實此電路具有 50.5 GHz 到 58.5 GHz 的頻寬，以及在中心頻率 54.5 GHz 具有-12 dBm 的輸入 1-dB 增益壓縮點與 -5 dB 的 S11 特性。並且，從修改後的模擬結果可知，雜訊大小約在 9.2 dB 左右。此電路操作在 1.2 V 的供應電壓下，並且消耗 11.4 mW 的直流功率。除此之外，此論文中也討論了造成頻率漂移以及增益降低的原因。從討論可知，若小心佈局電路，此架構的接收器可達到比量測結果更優異的特性，並且非常適合用在低功率，高傳輸速率的無線通訊系統中。

除了 60-GHz 接收器之外，此論文也提出一個 70-GHz 的低雜訊放大器電路。在此低雜訊放大器中，我們使用了三級串接的共源級架構來取代高頻常見的疊接架構以提升雜訊特性。並且可將電路的供應電壓降至 0.8 V 來達到低電壓以及低功率的設計。量測結果顯示此低雜訊放大器在中心頻率具有 10.9 dB 增益，以及小於-12 dB 的 S11 以及 S22 特性。由模擬結果可知在 67.8 GHz 的雜訊大小可達到 5.1 dB。 除此之外，此電路涵蓋了 65 至 72 GHz 的頻寬，非常適合用在寬頻的應用上。最後，這個操作在 0.8-V 低電壓的電路所消耗的功率只有 5.4 mW，並被實現在 0.38 mm^2 的晶片面積中。此結果證實了此電路非常適合用在 50 GHz 以上高頻的接收器中。

The Design and Analysis of 60-GHz CMOS Receiver Front-End

Student: Po-Hung Chen Advisor: Dr. Chung-Yu Wu

Department of Electronic Engineering &
Institute of Electronics
National Chiao Tung University

Abstract

In the next-generation wireless communication, high data rate transmission with a high operating frequency is expected. Over the past few years, the 7-GHz unlicensed band around 60 GHz has been released for high-speed and short-range communication systems. It has great potential in application of high data-rate wireless personal–area network (WPAN), high speed WLAN and point-to-point link, with possible data rate of gigabits per second.

In this thesis, a 60-GHz CMOS direct-conversion receiver integrated with a frequency tripler is presented. The proposed receiver which consists of a low-noise amplifier (LNA), a down-conversion mixer, output buffers, and a frequency tripler are designed using 0.13-um CMOS technology. By using a frequency tripler, the operating frequency of the frequency synthesizer can be reduced from 60 GHz to 20 GHz. This makes the implementation of the frequency synthesize much easier. Based on measurement results, as a result of the layout error, the receiver power gain is decreased to 13.9 dB. The measurement result presents the main circuit characteristics: covering 3dB-bandwidth from 50.5 GHz to 58.5 GHz,

input-referred 1-dB compression point of -12 dBm, input return loss of -5 dB at center frequency of 54.5 GHz and consumes 11.4 mW from 1.2-V power supply. Moreover, the re-simulated noise figure (NF) considering the undesired effects is about 9.2 dB. Afterwards, the reasons of malfunction which cause the frequency shift and gain reduction are discussed here. From the discussion, with the carefully layout, the proposed receiver can achieve much better performance than measurement and is confirmed to be suitable for low-power and high data-rate wireless communication systems.

Besides the 60-GHz receiver, a 70-GHz LNA is also presented. In the proposed LNA, three-stage common-source topology is used instead of cascode configuration to improve the noise performance. As a direct consequence of the use of common source structure in the proposed LNA, the voltage can be reduced to 0.8 V, which is much lower than that for the cascode structure. Therefore, the level of power consumption can be reduced greatly. The measured LNA gain is about 10.9 dB and the input and output return losses are lower than -12 dB at center frequency with the simulated noise figure of 5.1 dB. Furthermore, the 3-dB bandwidth covers from 65 GHz to 72 GHz which is suitable for wideband applications. Finally, this circuit can be operated on a low supply voltage of 0.8-V and only consumes 5.4 mW with a 0.38 mm^2 chip area. It is proved that the proposed LNA is feasible to use it in building fully integrated receiver at frequency of above 50 GHz.

誌謝

首先我要對吳重雨老師多年來的細心栽培與指導致上最誠摯的感謝。在老師的諄諄教誨下，不僅學會了積體電路設計方面的技巧及專業知識，在面對人、事、物的態度以及解決問題的方法也是受益良多。尤其在實驗室豐富的硬體及軟體資源的支援下，提供了我一個最佳的學習環境。此外要感謝老師在我研究方向最迷惘的時候，給予我適時的指導與啟發，以及對於我想法的支持與鼓勵，師恩浩蕩，銘記於心。再來要感謝論文口試的評審委員郭建男教授、蕭碩源博士以及高宏鑫博士對我的建議與指導。

在實驗室的夥伴中，首先感謝陳旻珓以及羅怡凱兩位學長，在這兩年來總是全力給予學習上的支持與指導。謝謝王文傑、虞繼堯、蘇烜毅、黃祖德、Fadi、詹豪傑學長們在這一段時間給予了我許多幫助還有指點。也要感謝與我一路奮鬥的夥伴們，晏維、順維、資閔、國忠、維德、必超、廷偉、雨軒、人文、旭佑、世豪、松諭、宗裕、巧伶、萬諶、國軒、國權等一群好朋友及同學，共同渡過富有挑戰性的研究生階段。除了這兩年一起在實驗室打拼之外，也在緊繃的生活中增添不少輕鬆的氣氛，使我的碩士生活增添了很多美好的回憶。

最後，我要對我的家人致上最深最誠摯的感謝，感謝父母的養育之恩以及長久以來無怨無悔的付出與栽培，在我面臨許許多多挑戰的時候，始終給予最堅強的後盾，讓我無後顧之憂。也謝謝他們能支持我的想法，讓我自由的追逐自己的夢想，逐步邁進。

陳柏宏

于 風城交大

96 年 夏

Contents

List of Tables

List of Figures

Chapter 1
Introduction

1.1 Background

Over the past few decades, wireless communication systems have been under significant development and are more closely related to our daily life than ever before. The most active RF/microwave bands are called industrial, scientific and medical (ISM) bands at 2.4 GHz, 5.2 GHz and 5.8 GHz for wireless LAN, which were allowed by the FCC for unlicensed transmissions [1]. However, due to the relative lower bandwidth, these systems can only access several Mbps and remain bottleneck for wireless broadband communications. Nowadays, the wireless system is still surging under increasing demands of high data rate and lower power consumption. Therefore, these issues have motivated the system designer to explore the higher frequency bands such as 60-GHz ISM band.

Recently, a 7-GHz band covering the range from 57 to 64 GHz has been released for unlicensed use in high-speed and short-range communication systems. The attraction of this band is its large bandwidth of 7 GHz and the lack of restrictions. There is only a maximum power restriction, on the order of +40dBm depending on the continent. It has great potential in the application of high speed WLAN and point-to-point links, and offers a possible data rate of gigabits per second.

In general, building high frequency circuits usually use special semiconductor materials, such as InP or GaAs. These processes have much higher electron mobility comparing to silicon substrate and allow for much faster devices. Moreover, SiGe process is also widely

applied in recent years due to its high performance characteristics. So far, existing millimeter wave receivers which use SiGe or HEMT have the great potential to implement wireless components for 60-GHz applications due to its high unit current gain frequency (f_T) [2]-[3]. However, as the f_T reaches 80 GHz in 0.13-um bulk CMOS technology, the advanced bulk CMOS technology becomes the potential choice for implementation of high speed wireless components. The bulk CMOS technology has the great advantages of low cost and high level integration. Recently aggressive downscaling of CMOS device sizes have resulted in significant improvements of their RF performances at a faster rate than SiGe bipolar and GaAs. Based on these features of CMOS process compounded with innovations in circuit design, it makes considerable improvements in wireless systems.

In the next generation wireless communication system, low cost, low power and high-performance 60-GHz transceivers are expected to entail high level of complexity. Even though there are still some restrictions to design the high-performance integrated receiver front-end using CMOS technology, we can use some circuit techniques or system architectures to overcome these limitations. So far, several 60 GHz band receivers and receiver building blocks like LNA and mixer using CMOS technology have been reported [4]-[8]. We would like to roughly describe these circuit techniques and find out a better solution for the proposed receiver architecture. Moreover, some frequency multipliers using HEMT or SiGe process have been reported [9]-[12]. From the authors' knowledge, there is still not any frequency tripler circuit proposed using CMOS technology. We would also like to introduce the frequency multiplier circuits and their operation principle in the following subsections.

1.2 Reviews on CMOS RF Front-end Receivers

The transceiver is quite a major component in the wireless communication equipment that commonly includes a receiver, a transmitter and a frequency synthesizer. The RF front-end receiver is a major component in the wireless communication equipments which generally consists of several main circuit blocks: a low-noise amplifier (*LNA*), down-converters, low pass filters and some baseband processing circuits. Conventionally, LNA amplifiers the RF signal received from the antenna with low noise contribution. Down-converters mix the output of *LNA* and local oscillator (*LO*) signal generated by frequency synthesizer to the desired intermediate frequency. Filters suppress the unwanted signals or interferences to provide a moderate signal quality for the baseband processing circuits to reach a reasonable performance. Figure 1.1 shows one of the receiver architectures for example.

Since the 60-GHz system has wide operating bandwidth, it is somehow different from narrow band receivers. As a result, some circuit blocks are supposed to have a wideband characteristic or multiple switched circuits used to work at various frequencies, and more than one single carrier frequency is required in the receiver chain for frequency down-conversion.

The architecture of the receiver must be selected appropriately to satisfy different system issues, for example complexity, cost and power dissipation. The characteristics of different receiver architectures are discussed in the following subsections.

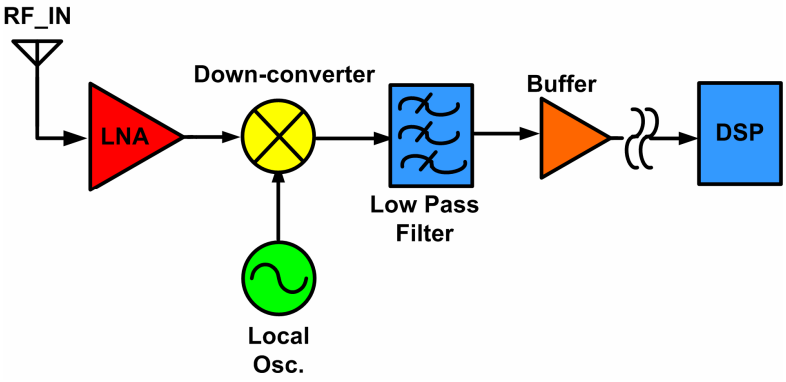


Figure 1.1 The architecture of the zero-IF receiver

1.2.1 Receiver Architectures

As RF receiver is evolving continuously, several main architectures have been generalized. The well-know architectures that widely used in recent years are super-heterodyne receiver, homodyne receiver and low-IF receiver [13].

- Super-heterodyne receiver

This architecture has been most widely used to gain the better selectivity and extreme sensitivity [14]. The block diagram of a typical double conversion super-heterodyne receiver is shown in Figure 1.2.

The received RF signal from the antenna is filtered first by a RF pre-scale filter and amplified by a LNA. The amplified signal is further discriminated from the image signal by an image rejection filter and applied to the first RF mixer. This down-conversion mixer translated the RF signal to lower intermediate frequency (IF) by mixing with the LO signal, where $\omega_{IF}=\omega_{RF}-\omega_{LO}$. At the output of the mixer, the desired signal is discriminated from the other channels by channel select filter and feed to the IF mixer. Through the IF mixer, the signal is down-convert to the more low IF frequency with additional filtering. The same as the RF mixer, the frequency of the IF signal is depended on the LO frequency that supplied to the IF mixer. The main selectivity of desired channel is provided at the same IF independent of the carrier frequency. Since the adjacent channels are filtered, the desired channel is discriminated from them.

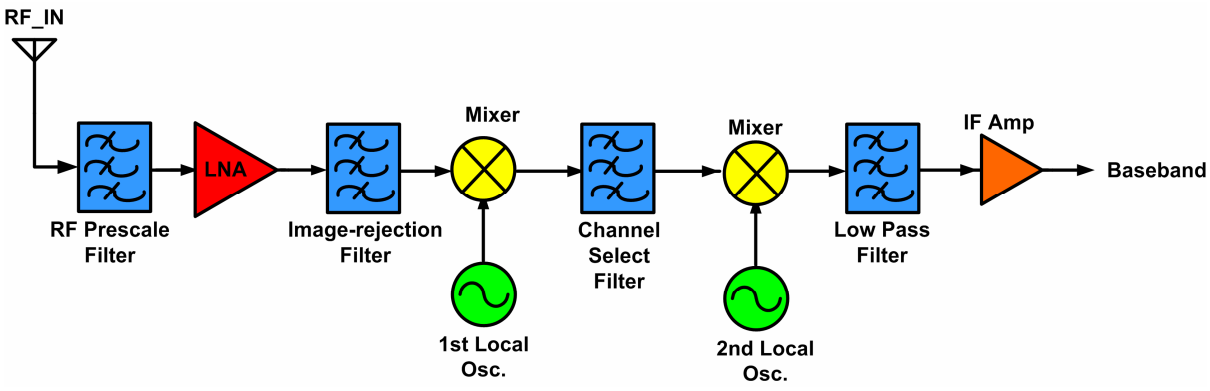


Figure 1.2 The block diagram of super-heterodyne receiver

The first IF (IF_1) frequency must be designed carefully. A high IF_1 increase the difference frequency between image and desired signal and gets better image-rejection performance. However, it requires a channel-selection filter with high Q-factor in this case and is difficult to implement on chip. On the other hand, a low IF_1 is difficult to obtain high image rejection but allows great suppression of nearby interferers. Furthermore, due to the lower frequency, a channel-selection filter only requires lower Q-factors and is much easier to implement.

This super-heterodyne receiver can easily overcome the DC-offset problem and has the better performance. The main drawback is its complexity and inadequacy of full integrating a receiver because the high-Q low loss filters are hard to implement using standard CMOS technology.

- Homodyne receiver

The homodyne receiver also called direct-conversion receiver or zero-IF receiver which eliminates many off-chip components and promising for single chip receiver, as shown in Figure 1.3. Since the RF signal is directly down-converted to the baseband, the image problem is eliminated because image is one of the sideband about the carrier of the desired signal. However, the lower part of the input spectrum itself is overlapped with the upper part of the spectrum. To avoid loss of information, two sides of input spectrum must be separated into in (I) and quadrature (Q) phase in translate to zero frequency [15]

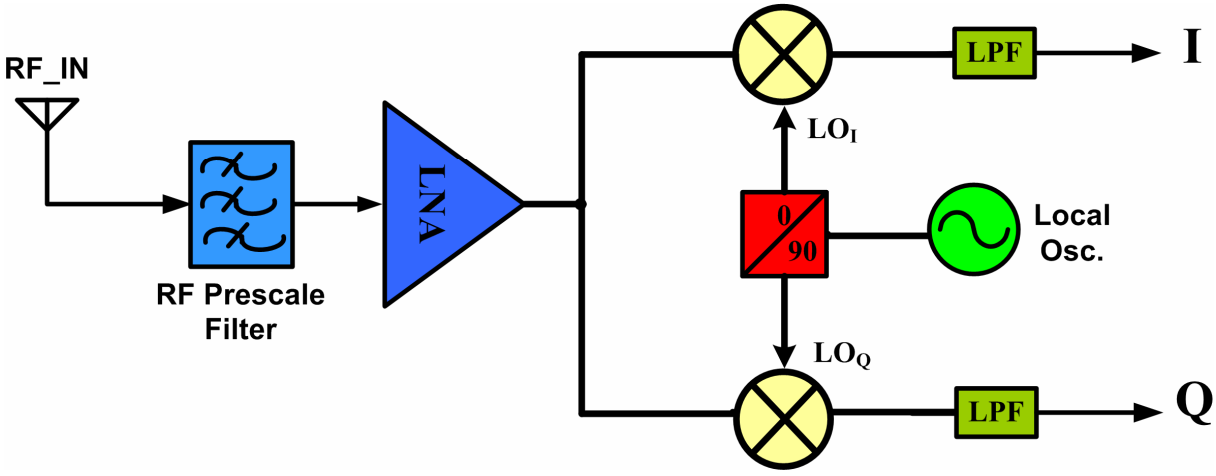


Figure 1.3 The block diagram of super-heterodyne receiver

Besides the image reduction, this architecture shows several advantages: high integration, simplicity of the structure, low cost and low power consumption. Moreover, the possibility of changing the bandwidth of the integrated low-pass filters is another advantage if multi-mode or multi-band applications are of concern [16].

However, the homodyne receiver suffers some drawbacks. The most serious problem is the DC offset impairment due to the LO leakage, which arise from capacitive and substrate coupling [17]-[18]. Due to the limited reverse isolation of mixers and LNAs, especially at high frequency, some of the LO signals may leak to the mixer, LNA, or even antenna. They will reflect to nearby objects and be mixed with the LO signal itself. This could saturate the consequent stages and affect the signal detection process. This problem may become more aggressive if self-mixing varies with time. This effect may be serious in CMOS process utilizing conductive substrate. In additional to DC offset, flicker noise, I/Q mismatch and even order distortions are other issues. I/Q mismatches may corrupt the down-converted signal and the bit error rates rise. Furthermore, since the down-converted signal is a baseband signal, it suffers the more serious flicker noise. These effects may become much more serious especially in CMOS technology [19].

- Low-IF receiver

In a low-IF receiver, the RF signal is mixed down to a non-zero low or moderate intermediate frequency, typically a few megahertz. Low-IF receiver has many of the desirable properties which the homodyne receiver has. Moreover, the architecture can avoid the DC offset and flicker noise problems which concerns seriously in homodyne receiver.

The use of a non-zero IF suffers from the image issue again. This image signal can be rejected by quadrature downconversion (complex mixing) and poly-phase filter [20]. However, double-quadrature architecture requires a quadrature generator on RF path and additional two mixers to implement which indicate the more power consumption is required.

Furthermore, the signal bandwidth in low-IF conversion is twice that in homodyne receiver. This requires doubling the analog-to-digital conversion sampling rate and results in more power consumption. The main disadvantage is the large mirror signal suppression requirement. In a zero-IF receiver, the mirror signal is the wanted signal itself. While in the low-IF case, it may be larger than the wanted signal. In addition, the double signal bandwidth in low-IF conversion mandates to double the baseband filter bandwidth, which further increase design complexity and power consumption [21].

1.2.2 Review on 60-GHz CMOS Receivers

As the 60-GHz band system is evolving continuously, several receivers have been published and analyzed. These receivers use different architectures to approach the better performance and high integration [4]-[6]. The followings are representative reviews of the state-of-the-art 60-GHz receivers.

- A 60-GHz CMOS Receiver Front-end [4]

The direct-conversion receiver is illustrated in this paper which is implemented using CMOS 0.13-um technology and operates under 1.2-V supply voltage. Figure 1.4 shows the block diagram of the receiver. The circuit consists of a LNA, quadrature mixers, and baseband amplifiers. For testing considerations, the balun is included here to convert the LO input signal from single-ended to differential. The low power consumption and high performance receiver characteristics offer the possibility of using the CMOS technology to implement the 60-GHz system instead of many III-V circuits. However, this type of architecture requires a 60-GHz frequency synthesizer to generate the LO signal, but such a high-frequency frequency synthesizer is difficult to implement and has the poor performance with high power consumption due to high frequency pre-scalar.

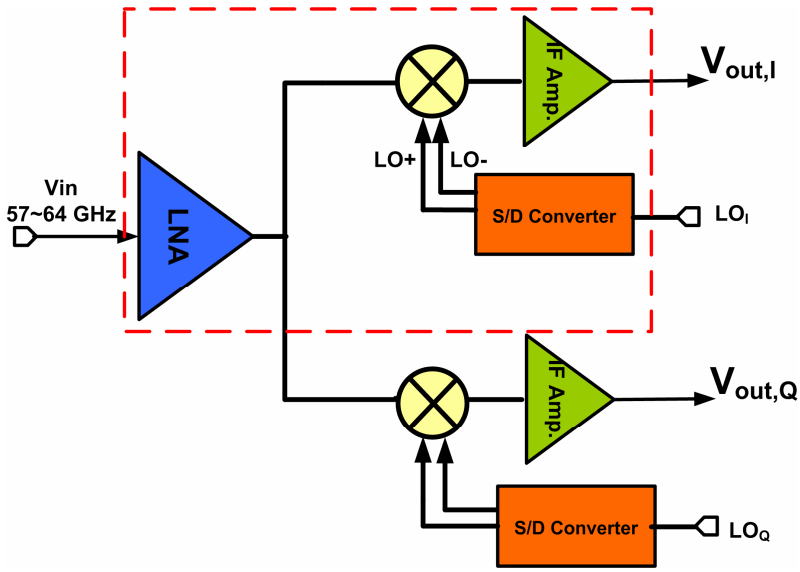


Figure 1.4 The block diagram of [4]

■ A mm-Wave CMOS Heterodyne Receiver with on-Chip LO and Divider [5]

This paper describes a heterodyne receiver using 90-nm CMOS technology and operates under 1.8-V supply voltage. This structure avoids quadrature turn separation and eases the management of interconnect which allows to be integrated with other high-frequency building blocks. Figure 1.5 shows the receiver architecture, where the RF mixer is directly driven by the LO and the IF mixers is driven through a divided by 2 circuit (with f_{LO}=40 GHz). However, the divide-by-2 circuit must operate at a nominal frequency of 40 GHz and consumes large power consumption with requiring the 40-GHz PLL.

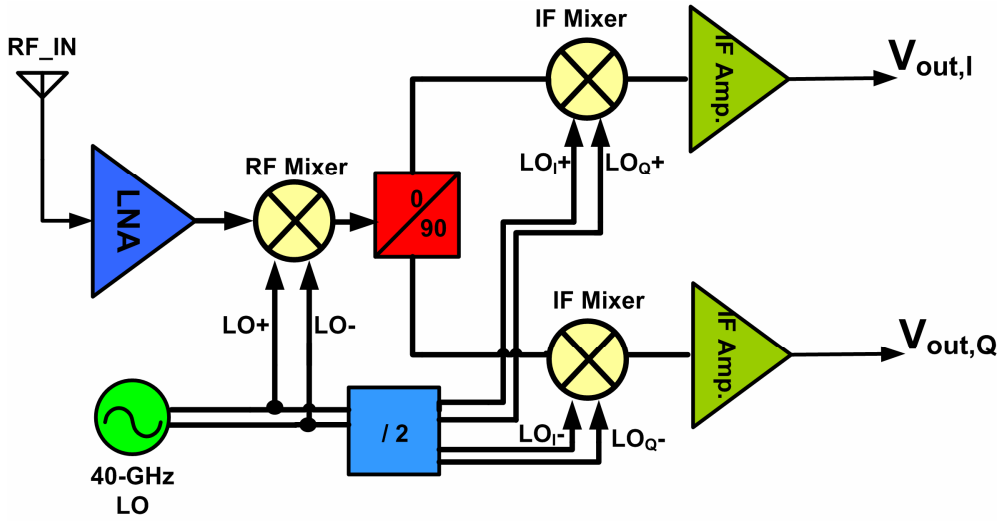


Figure 1.5 The block diagram of [5]

■ A High Integrated 60-GHz CMOS Front-End Receiver [6]

This paper describes a highly integrated 60-GHz CMOS receiver front-end which is fabricated in a 1P6M 0.13-um standard digital CMOS process and operates under 1.2-V power supply. The circuit consists of a LNA, a quadrature balanced down-conversion mixer, a 30GHz VCO, and a frequency doubler, as shown in Figure 1.6. By using the frequency doubler, only the 29-GHz PLL is required to down convert the 60-GHz signal to 2-GHz IF frequency. This is much easier to implement 29-GHz frequency synthesizer comparing to 60-GHz one when integrating with the receiver. However, the doubler can not provide the differential output signal associated with a mixer and such a circuit still consumes a large amount of power. Moreover, the 60-GHz mixer is down-converted to 2-GHz IF frequency and uses the inductor to peak the signal. This may reduce the noise contribution from the load of the mixer but more inductors are required which occupies large chip area. This architecture requires two PLLs to down-convert the RF signal to baseband and is much more complex with large power consumption.

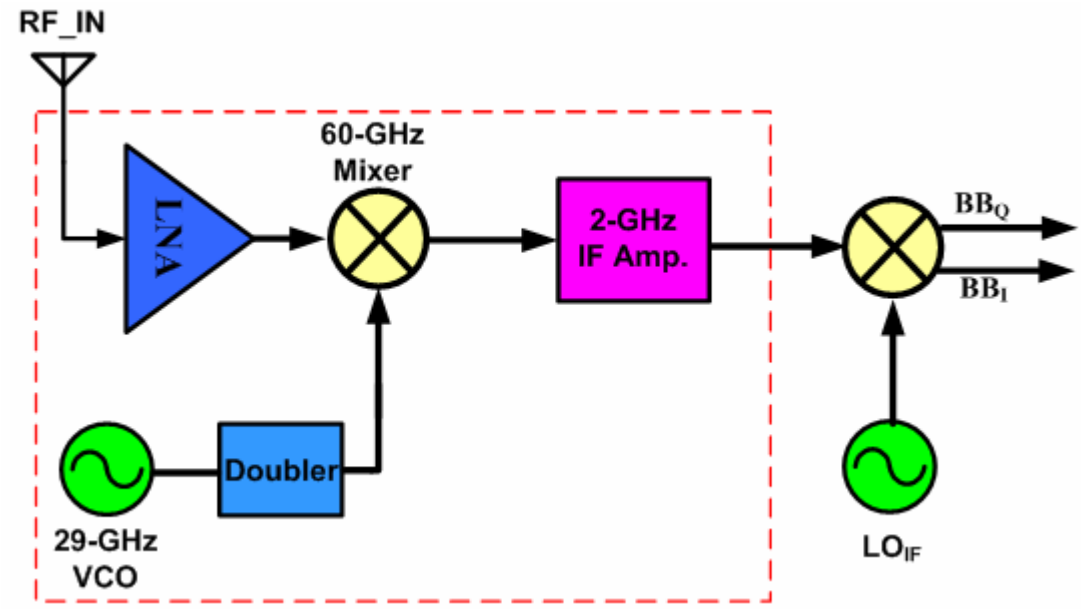


Figure 1.6 The block diagram of [6]

1.2.3 Review on Building Blocks of CMOS Receiver

Besides the receivers, several building blocks of receiver front-end at frequency of V-band (50~75 GHz) using CMOS technology have been published in recent years. These circuits provide some solutions and techniques to overcome the limitation of the device f_T which is around 80 GHz in 0.13-um CMOS technology. Here, we review these published V-band CMOS circuits to obtain the issues which must be pay more attention when designing the V-band circuits.

- A Miniature V-band 3-stage Cascode LNA in 0.13-um CMOS [8]

In this design, the three stages cascaded LNA using 0.13-um CMOS technology with operating under 2.4-V supply voltage is presented. The circuit schematic diagram is shown in Figure 1.7. This architecture uses the cascode device configuration to achieve high gain performance. All of the input, output and inter-stage matching networks are conjugated matched for maximum power transition. However, this structure requires a higher supply voltage and consumes much more power. Moreover, the parasitic capacitance at input stage of a cascode structure causes the signal loss and also increases the noise figure. As a result, the entire noise figure is much larger than conventional common-source architecture.

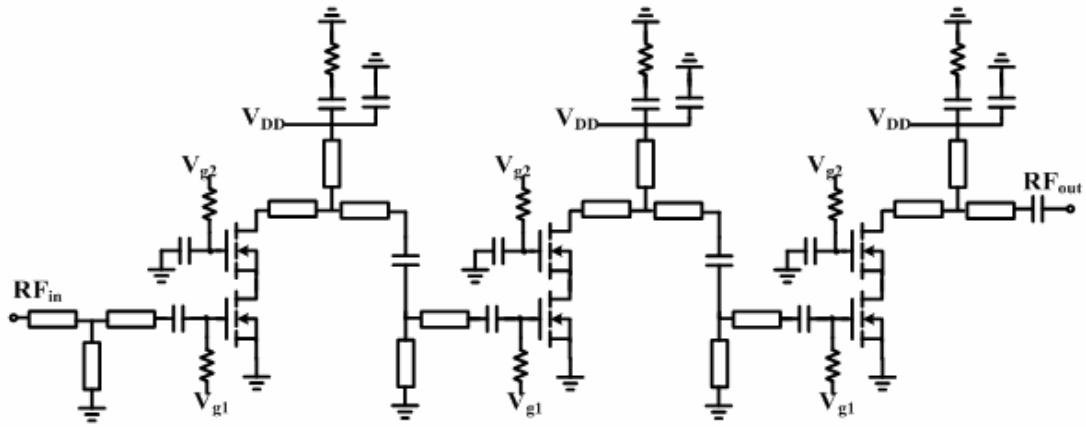


Figure 1.7 Circuit schematic of the V-band CMOS LNA in [8]

■ Single-gate quadrature balanced mixer [6]

This paper presents a quadrature balanced down-converting mixer consisting of two unit single-gate mixers with a 90° branch-line hybrid, as shown in Figure 1.8. The single-gate mixer down converts the RF frequency to 2-GHz IF signal. By taking advantage of the intrinsic device capacitances, the 90° phase shift can be realized by using CPW (coplanar waveguide) transmission lines shorter than λ/8. To reduce the length of the transmission lines, the LO and RF matching networks are co-designed with the 90° branch-line hybrid and gate-bias network. In addition, the insertion loss of the passive component can also be reduced. The on-chip LC components at the drain of CS stage complete the IF matching at 2-GHz. It also filters the LO and RF signal which is not desired at the output. By using the inductor for matching network, the noise contribution from the load can be reduced, but the larger chip area is required. This architecture provides good linearity but the conversion gain is negative which may lead the reduction of the entire receiver gain. Moreover, large amount of transmission lines require large chip area to implement on chip.

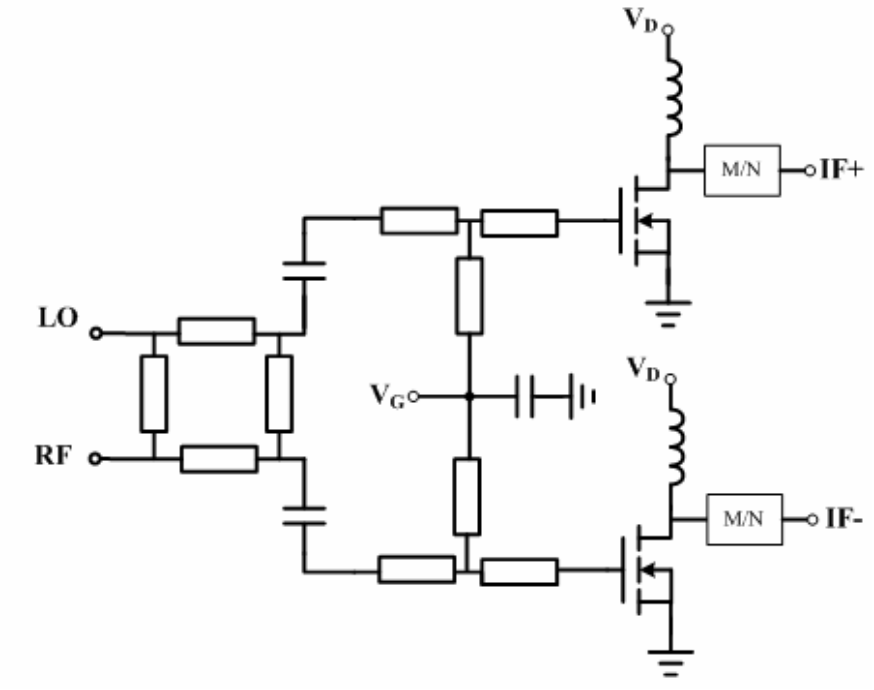


Figure 1.8 Simplified circuit diagram of the single-gate quadrature balance mixer in [6]

■ Gilbert-cell based mixer [5]

As operating at 60-GHz, the conventional Gilbert-cell mixer which is illustrated in Figure 1.9(a) has the poor performance due to several reasons: the total capacitance at the drain of M_1 gives rise to a pole on the order of $f_T/2$, the switching pair M_1, M_2 must carry the entire bias current of M_3 and the noise contribution from the switching stage may increase. Moreover, only the small voltage drop across the load resistors is allowed because of supply voltage limitation. These make the diminution of the conversion gain.

To improve these issues, the modified down-conversion mixer using inductive peaking and current injection techniques are implemented, which is shown in Figure 1.9(b). The inductor L_1 resonates with the total capacitance seen at the drain of M_3 and carries part of the drain current of M_3. This could lead the load resistance to be doubled. Moreover, since M_1 and M_2 carry smaller current, they can switch more abruptly. These improvements can abruptly improve the gain and the noise performance of the mixer.

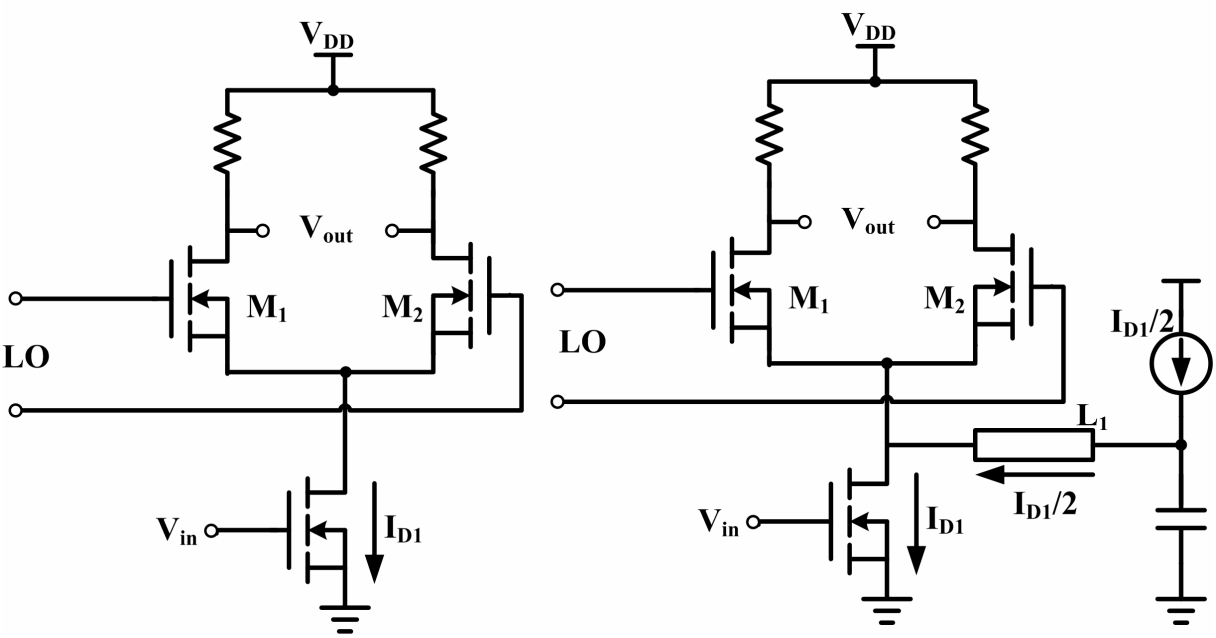


Figure 1.9 (a) Conventional and (b) proposed mixer in [5]

1.2.4 Review on Frequency Multiplier

In general, active multipliers are configured as doublers which have been demonstrated with good performance [23]. So far, several frequency multipliers using HEMT or SiGe processes have been published and analyzed [9]-[12]. The following reviews some of the techniques of the frequency multipliers.

- Frequency doubler using 0.13-um CMOS technology [6]

The schematic of the three-stage frequency doubler is shown in Figure 1.10. It consists of a 30-GHz input driver, a frequency doubler core, and a 60-GHz LO buffer. The Cascode devices form the input and output stages. The inter-stage matching is also applied using reactive components. The frequency doubler is made up by CS amplifier which is biased close to its threshold voltage to efficiently generate the desired second order harmonic signal. A passive network at the drain of the transistor can reject the 30 GHz fundamental while maximizing the second order harmonic at 60 GHz. In additional, it can optimize the power transfer to the output buffer. The input and output of the doubler core circuit are matched to 50 ohm at 30 GHz and 60 GHz separately.

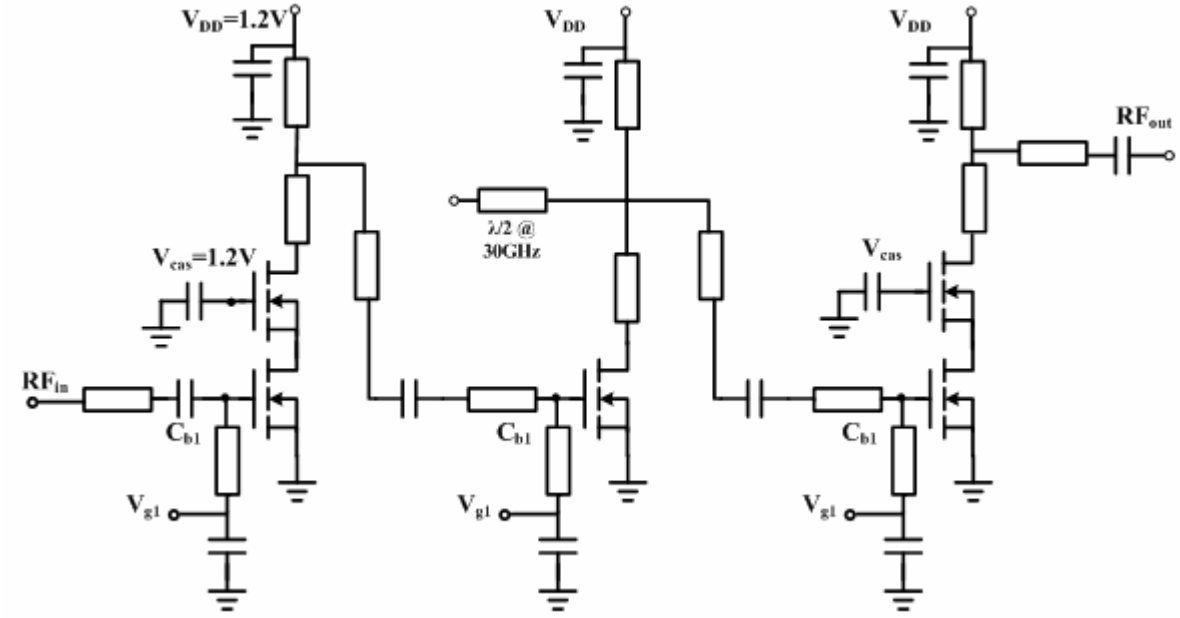


Figure 1.10 Simplified circuit diagram of the frequency doubler in [5]

However, this structure has some drawbacks: it requires large power consumption, applying with many transmission lines, and more importantly, the circuit can not generate the differential LO signals to supply to the mixer. These issues may require to be considered when integrating with other building blocks of the receiver circuit.

- An optimized 25.5–76.5 GHz pHEMT-based coplanar frequency tripler [12]

This tripler schematic diagram is shown in Figure 1.11, which presents a single-stage MMIC tripler with W-band output frequency. This circuit is based on a double δ-doped 0.15-um gate-length AlGaAs/InGaAs/GaAs PHEMT process. The HEMT device is operated under class AB bias point to efficiently generate the third order harmonic of the input.

This circuit is emphasized on selecting the optimum input and output terminations to get the maximum power transfer at fundamental and third-order harmonic of the input respectively. The terminating impedances are chosen to avoid signal losses and enhance the power at the desired harmonic. A shorter stub with a shunt capacitor is also applied here to eliminate the fundamental signal which is not expected at the output. From many aspects, this approach provides excellent performance but still can not generate the differential signal. Moreover, the circuit is fabricated using pHEMT process and large power consumption is a great concerned. In additional, the integration with other circuits is another issue.

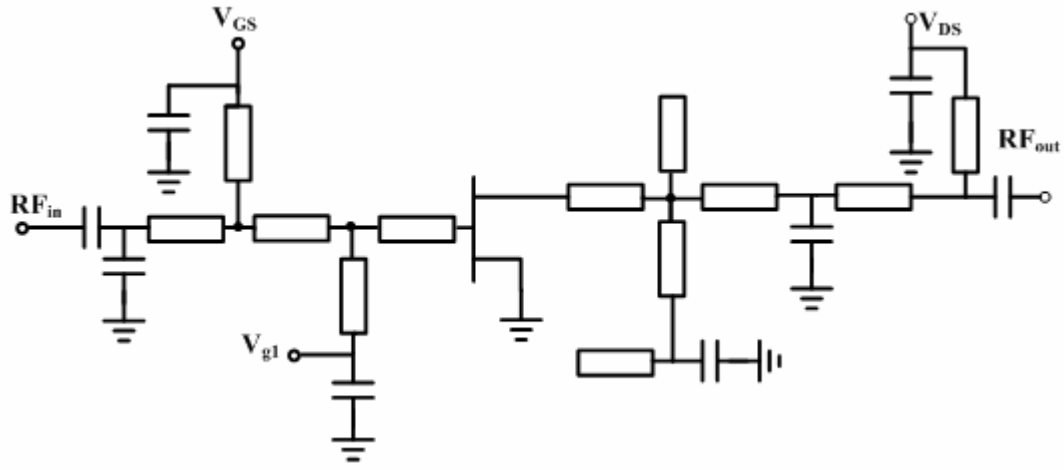


Figure 1.11 Schematic circuit diagram of the 25.5-76.5 GHz single-ended frequency tripler

1.3 Motivation

As mentioned above, some published receivers for 60-GHz applications have been developed and surveyed. These receivers require high-frequency frequency synthesizers to generate appropriate LO signal to down-convert the RF frequency to baseband. This may lead the receiver performance become poor because the frequency synthesizer performance degrades violently when operating at higher frequency. Moreover, the tuning range of the VCO also degrades due to smaller inductor values. This tuning range may not sufficient to cover the entire 57~64 GHz band and requires more than one PLL to cover the whole frequency band. Based on the drawbacks and design considerations of receiver architecture mentioned above, a wideband direct-conversion topology integrated with a frequency tripler has been proposed in this thesis. The design is realized by using TSMC 0.13-um CMOS technology under the standard supply voltage of 1.2 V. It attempts to design a low cost, low power and wide bandwidth circuit for 60-GHz system applications. This circuit also has great potential to be integrated with frequency synthesizer and baseband circuits.

1.4 Thesis Organization

Chapter 2 presents a novel frequency tripler circuit which can be applied in 60-GHz receiver front-end. The detail design considerations are also introduced here with its simulation results. In Chapter 3, the receiver architecture and its building blocks are presented. It includes a LNA, a down-conversion mixer and output buffers. The basic theory and simulation results of each building block are also illustrated here. Chapter 4 contains experimental results and discussions. Finally, conclusions and future work are presented in Chapter 5.

Chapter 2

A High-Frequency Frequency Multiplier

A novel configuration of balanced frequency tripler using standard 0.13-um CMOS technology is proposed. In this chapter, the circuit design consideration and theoretical analysis of frequency tripler are introduced together with the simulation results. The simulation results show that the circuit has great potential to apply in the high-frequency system such as 60-GHz receiver front-end.

2.1 Design of the Frequency Tripler

A frequency tripler based on FET type is very attractive for being integrated with other elements of a monolithic transceiver. In this design, by importing only 20-GHz input signal, the frequency tripler can successfully generate sufficient amplitude of the differential 60-GHz signal to be as LO signal of the mixer.

2.1.1 Operational Principle

The analysis of the frequency multiplier is usually a combination of gate bias and fundamental RF input levels for optimum generation of a desired harmonic signal [24]. To decide the bias point of the FET device, the drain current dependence model illustrated by Fudem and Niehenke is introduced here [25].

The optimal bias point is opted midway between pinch-off and the onset of forward condition which is consistent with a Class-A amplifier. When operating on this bias point, a large amplitude AC signal is required to over-drive the device both into pinch-off and forward conduction every cycle. The resulting drain current waveform is then severally clipped at both

ends. This clipped waveform successfully results the harmonics. If the ac signal becomes larger, the output waveform can be approximately considered as square-wave results. The Fourier transformation associated with a perfect square-wave is given by:

$$I_n = \frac{2I_{peak}(-1)^n}{n\pi} \quad , n\ odd$$
$$I_n = 0 \quad , n\ even$$

As can be seen, for the perfect square-wave, only the odd order harmonic is generated and even order term which we do not desired can be eliminated. For a square wave, if n=3 for the tripler design, the output amplitude of I_3 can be generated approximately $0.212I_{peak}$. This mode of operation obtains superior third-order conversion than biasing the device near the pinch-off which is more commonly used.

Besides biasing between pinch-off and the onset of forward condition, there is still another bias point that can obtain the same optimal value of I_3. This solution can be obtained by generating rectangular output waveform with a duty cycle of 1/6 rather than square one. Unlike the square-wave considered previously, although rectangular-wave does obtain the same conversion of the odd order harmonic, it also contains significant even order harmonics, especially second order harmonic which we do not desire.

The most significant benefit of choosing a 1/6 duty cycle in bias point design is the DC power reduction. In this mode, the device always operating in the cut-off region and rarely consumes DC power until AC signal is supplied. Furthermore, the fundamental content under this operation is less than that of square-wave, thus the fundamental rejection can be improved. Nevertheless, there are several serious drawbacks in this approach: poor even order harmonic rejection, high AC drive level of the fundamental input, and the breakdown issue due to large drive power.

2.1.2 Design Considerations

There are several limitations that need to be considered when implementing the frequency tripler which applies in 60-GHz receiver front-end. Especially, the design is implemented by using 0.13-um CMOS technology with 1.2-V supply voltage.

From the analysis that mentioned above, two optimal bias conditions are proposed. One is biasing in the middle between cut-off and forward conduction region, which generate square wave in the output. The other operation point is biasing at well below the cut-off region and generate 1/6 duty cycle rectangular wave with large AC signal. If we want to generate a 60-GHz LO signal, we must implement a 20-GHz frequency synthesizer or VCO to provide the sufficient input AC signal level for the tripler circuit. However, in 0.13-um CMOS technology, it is hard to generate such a large output swing signal due to low supply voltage. Beside, the FET device model of the CMOS process is not quite accurate when biasing well below cut-off region and the performance of the circuit can not be guaranteed. Hence, in the CMOS technology, the bias point of the device is better to be opted midway between pinch-off and onset of forward condition which is consistent with a Class-A amplifier.

Nevertheless, in practical case, the output waveform can not produce the perfect square-wave. Therefore, the undesired even order harmonics are no longer be zero, especially the second order harmonic is the extreme one. In the design of the frequency multiplier, harmonic rejection is also an import demand. The most popular method to filter out these undesired outputs is using the inductor peaking approach. By choosing appropriate value of LC tank, the band pass filter characteristic can be obtained. Another popular way is using the transmission lines with length of particular wavelength ratio to filter out the undesired signal. However, this method requires large chip area to implement the transmission lines.

2.1.3 Circuit Realization

The circuit scheme of the proposed two-stage CMOS frequency tripler is shown in Figure 2.1. It consists of a tripler core circuit and an output buffer stage with a fully differential configuration. The tripler function is made by MOS M_1 and M_2. As the fundamental signal (20 GHz) is applied to the gate terminals of M_1 and M_2, the third order harmonic signal (60 GHz) can be generated due to the output waveform distortion that mentioned in previous subsection. The inductors L_1 and L_2 are used to resonant with the parasitic capacitance at the third harmonic frequency of the input signal and the desired output signal can be extracted. Moreover, due to the band pass characteristic of the LC tank, the undesired harmonic signals will be filtered to some extent.

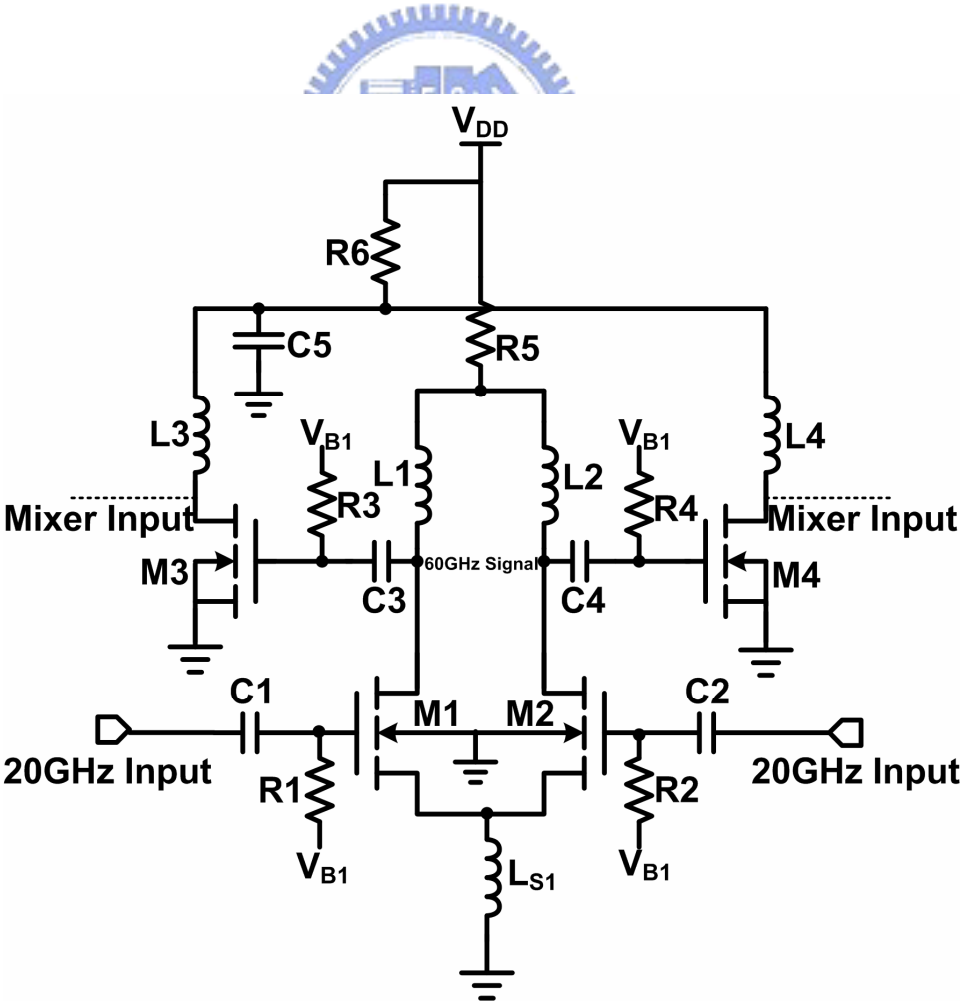


Figure 2.1 The circuit scheme of the proposed CMOS frequency tripler

The M_3 and M_4 perform as CS amplifiers and the load inductors L_3 and L_4 are also resonated at the third harmonic frequency. By using additional gain stage, not only can the desired signal be enhanced further but also the other undesired harmonics can be suppressed. A resistance R_2 is used to select the dc operation point of the mixer LO-port and can save a dc bias pin. In additional, to provide the stable dc bias, a bypass capacitance C_5 is also added.

Because the even harmonic signals at the output nodes are common-mode characteristic, appropriate value of R_5 can be designed to eliminate the undesired even order harmonic signals. The simulation result of the 2^{nd} and 4^{th} harmonic rejection improvement due to R_5 is shown in Figure 2.2

To further improve the performances, the source inductor L_S is applied to enhance the even order harmonics at the source terminal of $M_{1,2}$ to mix with the input fundamental signal. Thus, the third harmonic signals at the output nodes can be enhanced, as shown in Figure 2.3. When even-order harmonics are involved, the L_S can be seen as source degeneration inductor and a cause of even order signal gain reduction, as illustrated in Figure 2.4. Further improvement of the harmonic rejection ratio (HRR) is expected which shows in Figure 2.5. Although larger inductance value gets better performance, but it is not easy to implement such a large inductor and it requires large area. So we choose the appropriate value of source inductor here. The detail device parameters of proposed frequency tripler are list in Table 2.1.

Table 2.1 Detail parameters of proposed frequency tripler

$M_{1,2}$	**18 um / 0.13 um**	**$R_{1,2}$**	**5 kohm**
$M_{3,4}$	**9.6 um / 0.13 um**	**$R_{3,4}$**	**5 kohm**
$L_{1,2}$	**w=3 r=37 nr=1, CENT-Tap**	**R_5**	**8 ohm**
$L_{3,4}$	**Tline 230 pH**	**R_6**	**200 ohm**
L_{S1}	**Tline 200 pH**	**$C_{1,2}$**	**MIM 30um x 30um**
V_{B1}	**0.65 V**	**$C_{3,4}$**	**MIM 20um x 20um**
V_{DD}	**1.2 V**	**C_5**	**MIM 10um x 10um**

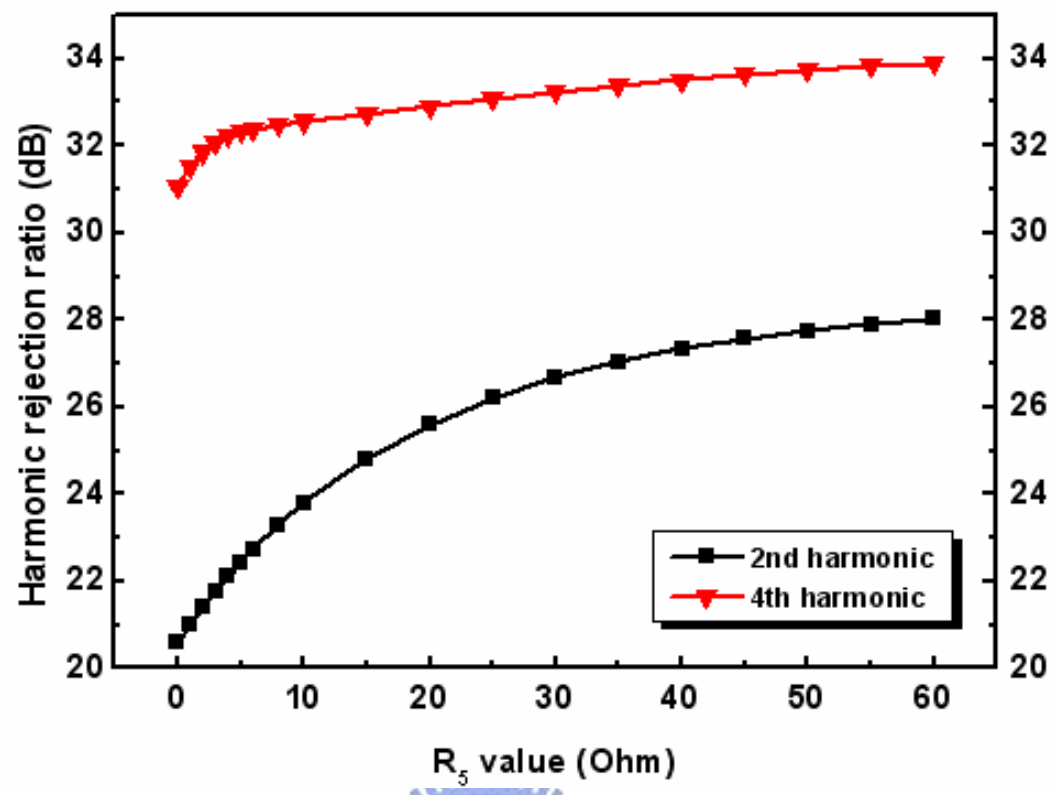


Figure 2.2 Simulation results of even-order HRR due to R_5

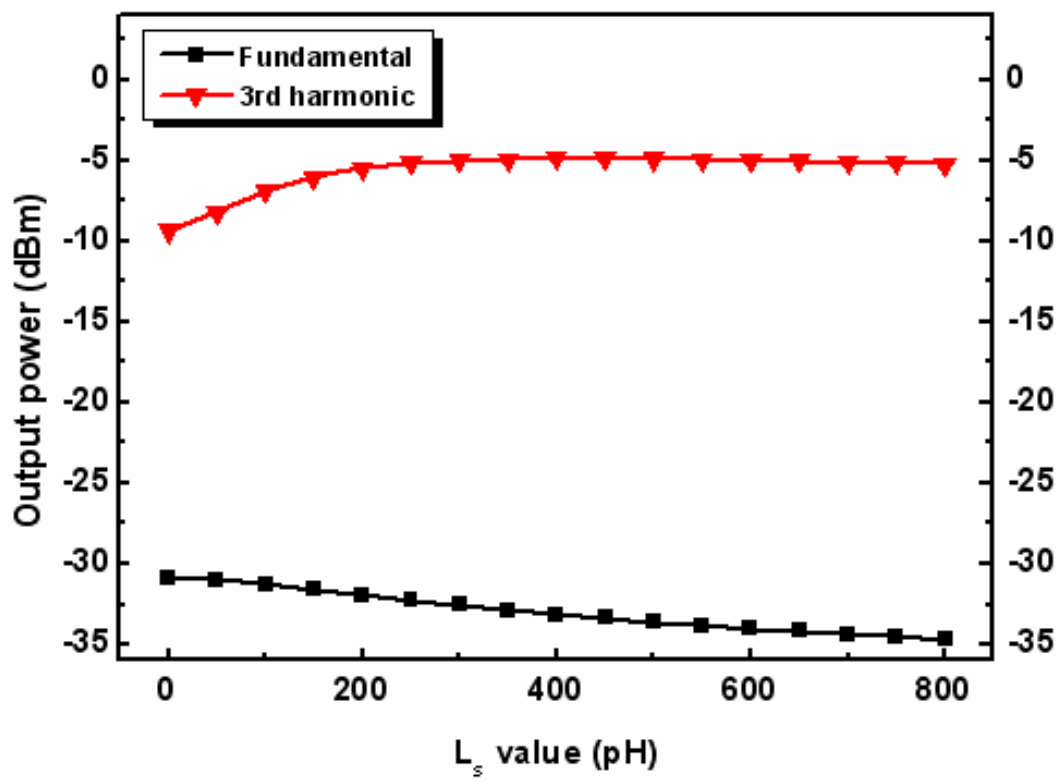


Figure 2.3 The simulation results of odd-order harmonic output powers versus L_s

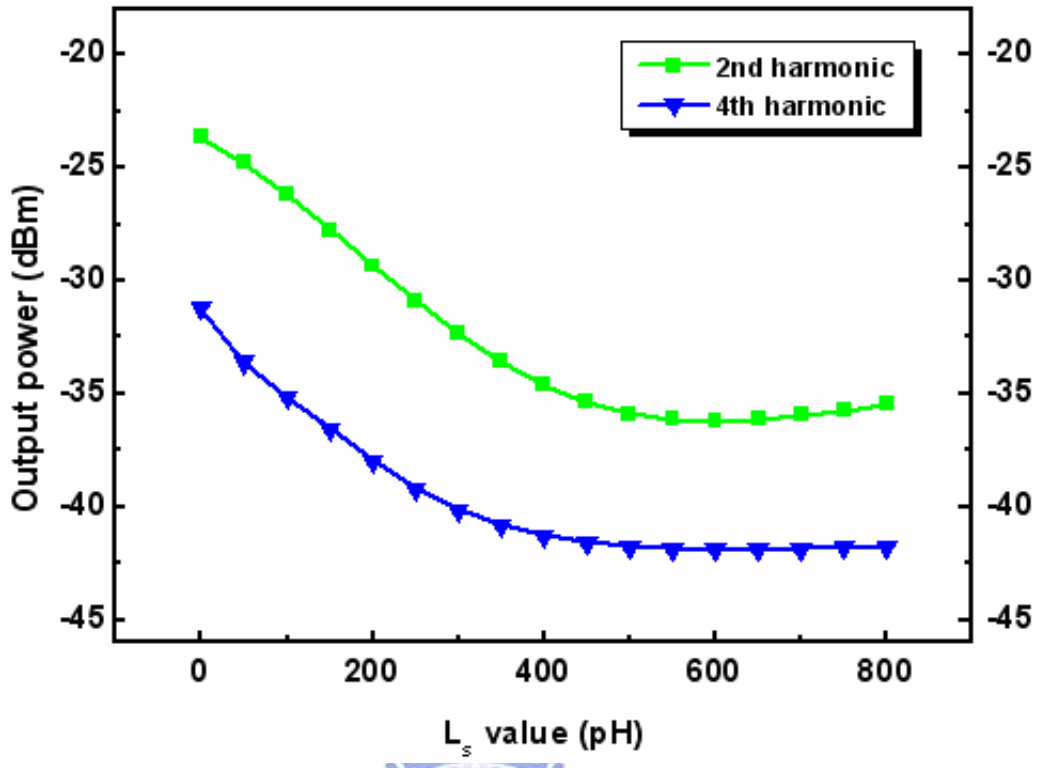


Figure 2.4 The simulation results of even-order harmonic output powers versus L_s

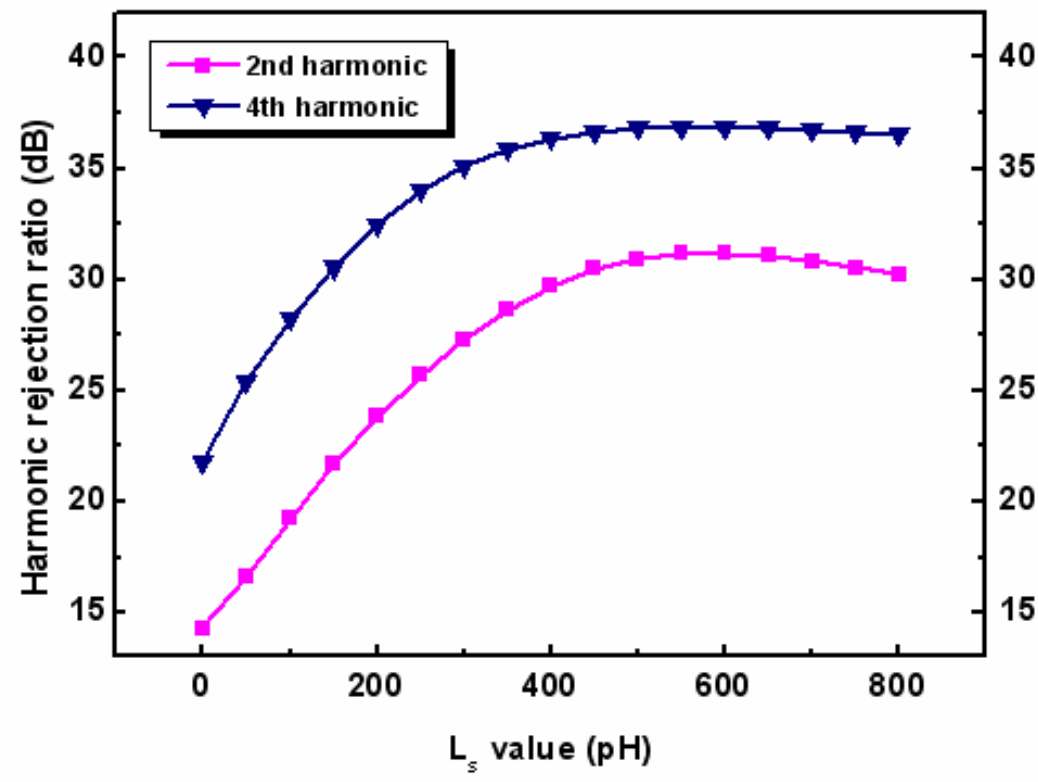


Figure 2.5 The simulation results of even-order HRR due to L_s

2.1.4 Simulation Results of Frequency Tripler

The performance of the proposed frequency tripler is simulated under the input power of 4 dBm. To count the loading effect of the mixer, the circuit is integrated with the mixer and obtains the inter-stage performances. Figure 2.6 shows the simulated relative output power of the frequency tripler between 56~65 GHz. In Figure 2.7, the HRR over the 57~64 GHz are calculated. It shows that the HRR can achieve better than 24 dB in each case. Since the output impedance is not 50-ohm, the simulation results taken as affirming the relative harmonic amplitude. The accurate output swing waveform at 60-GHz can be obtain by using transient analysis, as shown in Figure 2.8 to Figure 2.10. As can be shown, the output swing of the frequency tripler is between 125 mV and 270 mV. At last, the third-harmonic output power versus input power of the fundamental signal is illustrated in Figure 2.11. Obviously, the third-harmonic output power achieves saturate when input power is larger than 4 dB. Hence, we choose the 20-GHz input signal as 4 dBm here which is available to be generated by using 20-GHz PLL or VCO under 0.13-um CMOS process.

To obtain the phase noise contribution due to the proposed circuit, an additional 20-GHz VCO has been designed and connected to the proposed frequency tripler. Figure 2.12 shows the simulated phase noise performance of the 20-GHz VCO and the output signal of the frequency tripler circuit when VCO is connected as the fundamental input signal. As can be seen, the phase noise increases 11.8 dBc/Hz at 1 MHz offset before and after the frequency tripler circuit. Ideally, tripling the signal will cause the 9.54 dBc/Hz phase noise enhancement due to frequency transition. Hence, the phase noise contribution due to the proposed circuit itself is about 11.8 – 9.54 = 2.26 dBc/Hz.

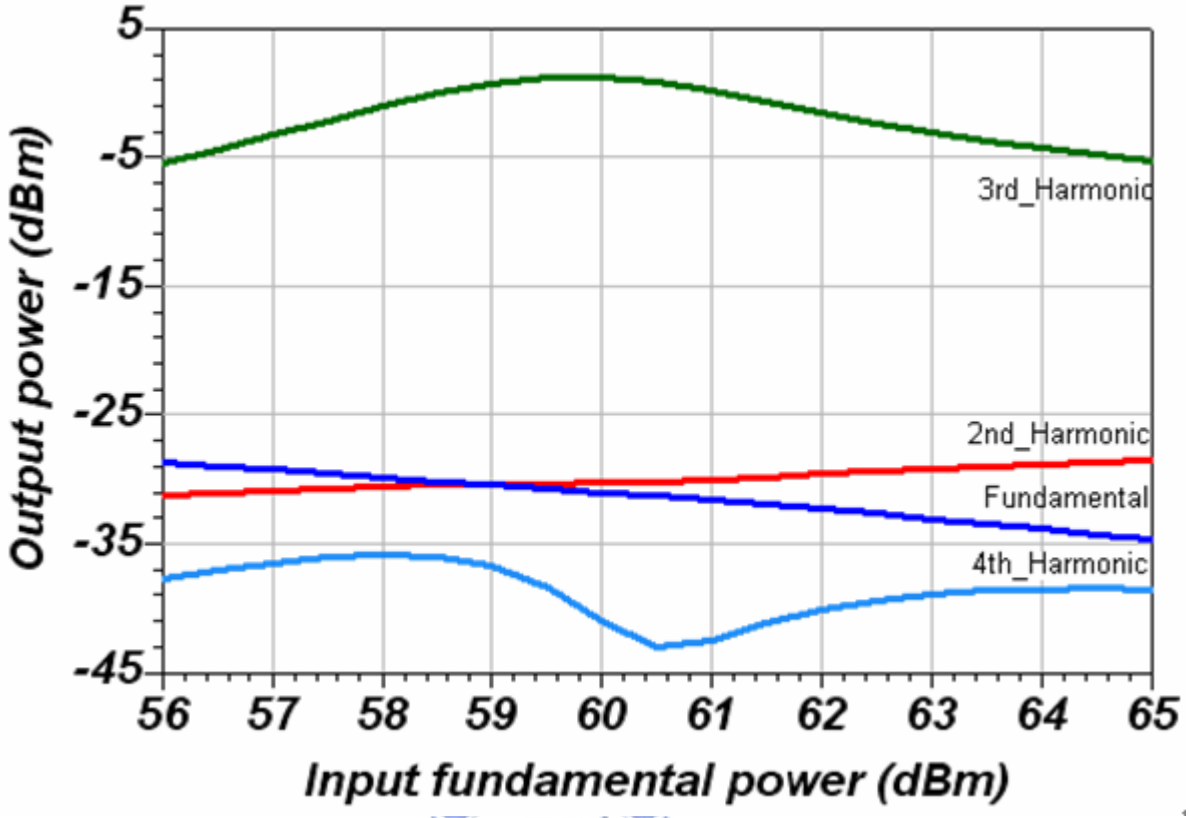


Figure 2.6 The simulation results of the relative output power

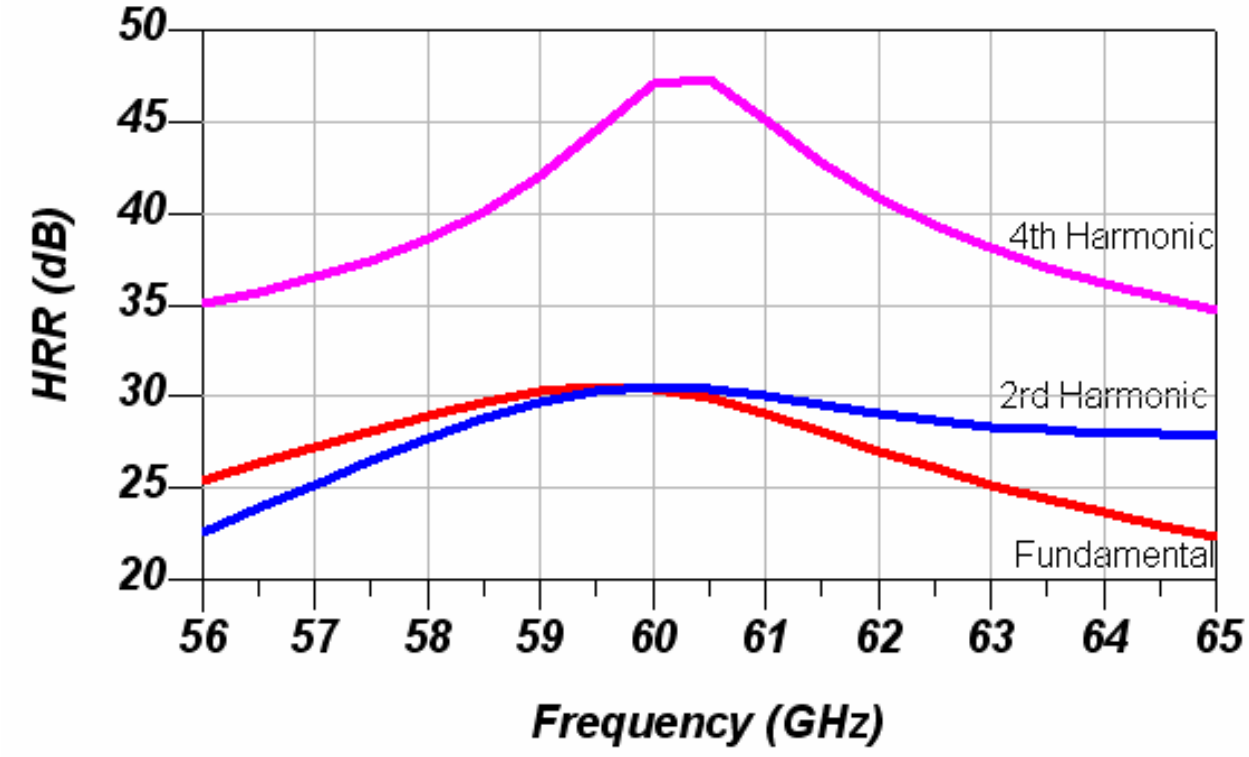


Figure 2.7 The harmonic rejection ratio to different harmonic

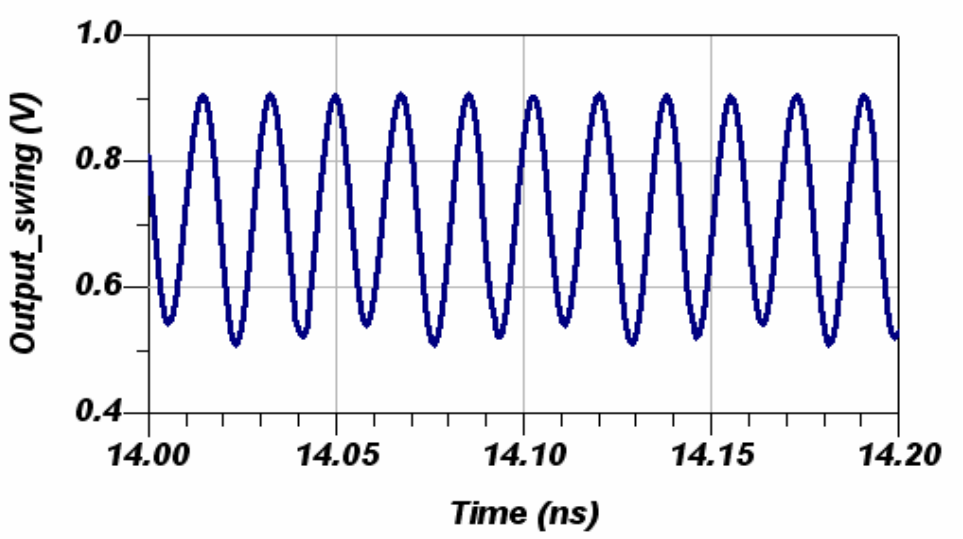


Figure 2.8 The simulation results of the output waveform at 57 GHz

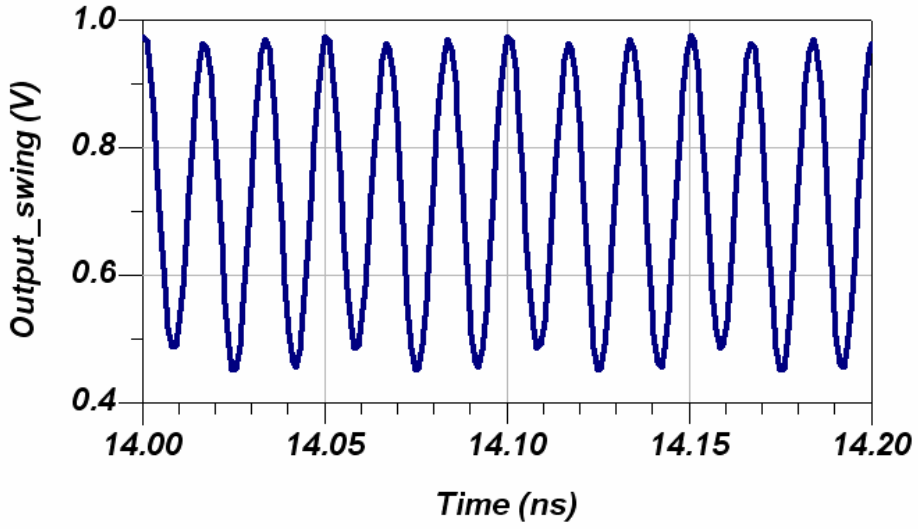


Figure 2.9 The simulation results of the output waveform at 60 GHz

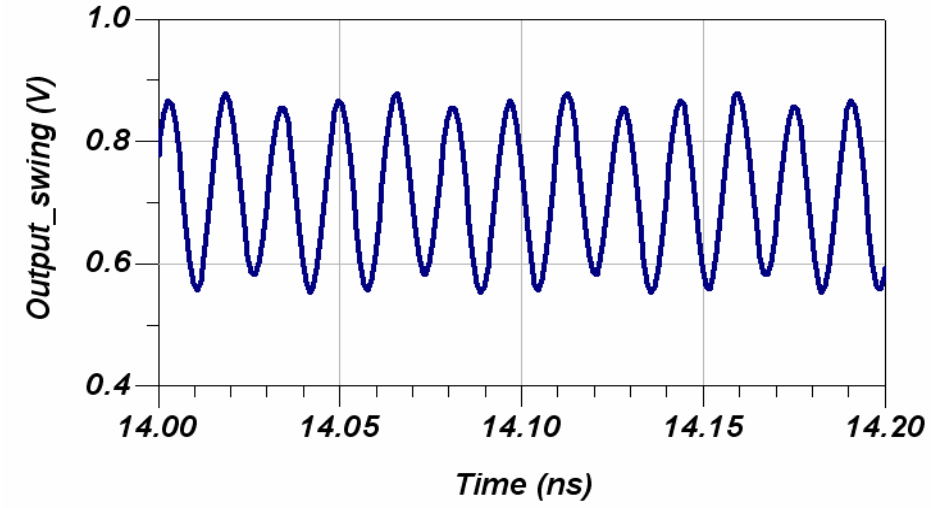


Figure 2.10 The simulation results of the output waveform at 64 GHz

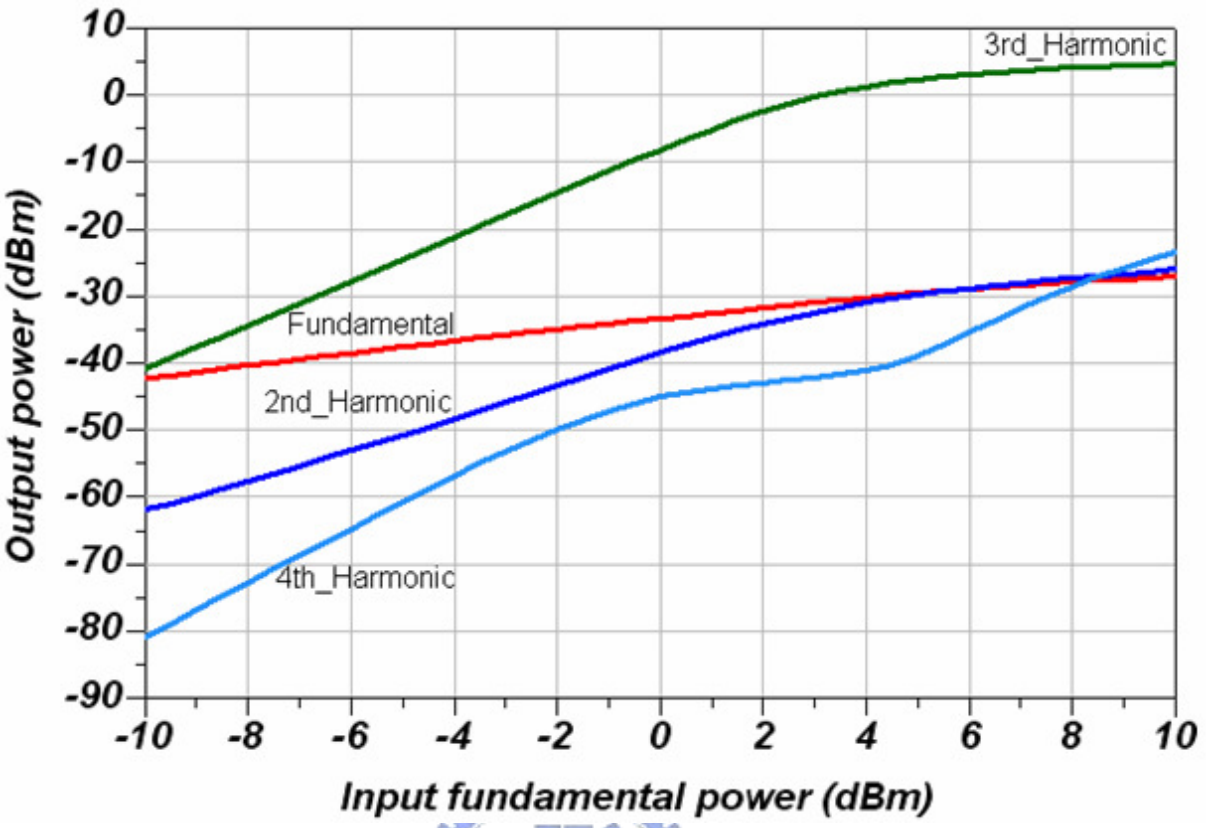


Figure 2.11 The output power versus fundament frequency input power at 20-GHz input

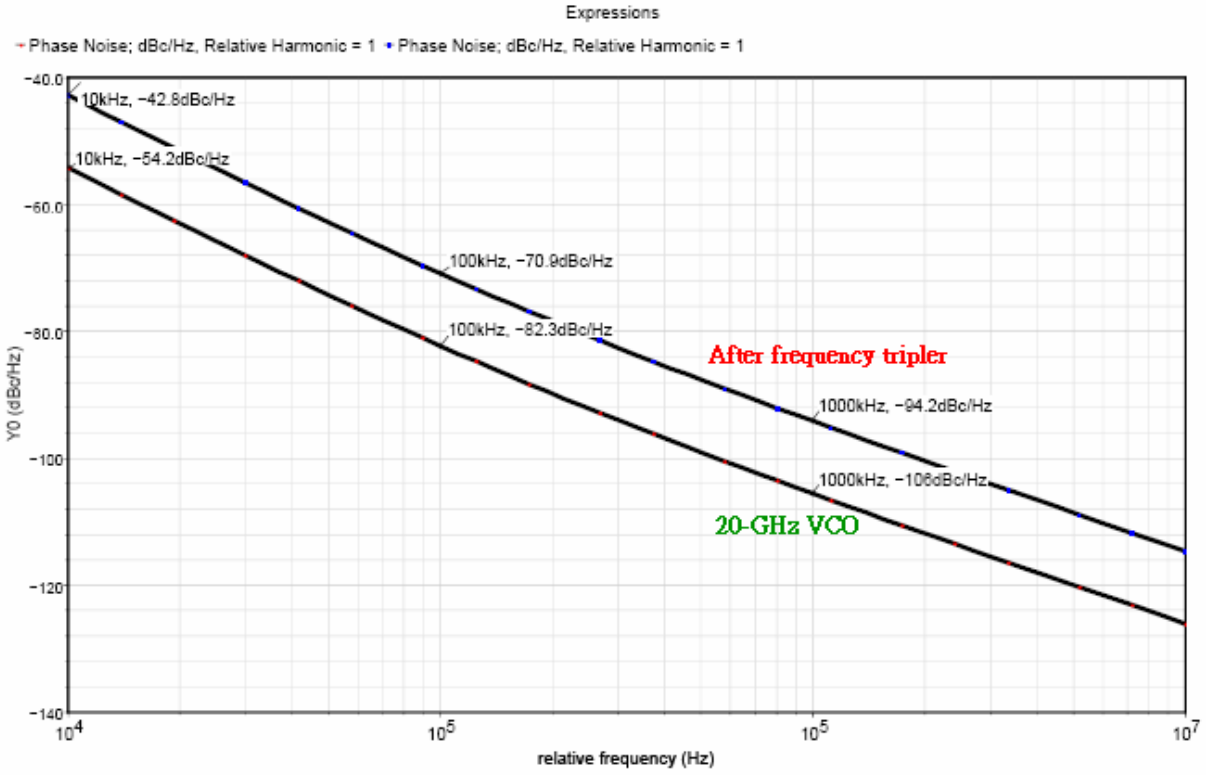


Figure 2.12 The phase noise contribution due to the frequency tripler

2.2 Comparison with Previous Works

In the following, the simulation results are compared with the previous works. The main results of the frequency multiplier are including input power level, output swing, HRR and power consumption. So far, from the author's knowledge, there is still not any frequency tripler circuit implemented using CMOS technology. We can only compare with the published works which are fabricated using pHEMT or SiGe technology. The simulation results summary of the proposed CMOS frequency tripler and the comparison with previous works are shown in Table 2.2 and Table 2.3, respectively.

As can be see, although we use the CMOS technology, the proposed frequency tripler performs the high output swing and the excellent harmonic rejection ability. A larger HRR can diminish the harmonic effects that influence the mixer performance. Since the 20-GHz VCO is available to reach the 4-dBm output power with 1.2-V power supply, this input power is quite make sense while simulating. From simulation results, the output voltage swing of the frequency tripler is larger than 125 mV and is enough to turn on and turn off the MOS device in the mixer stage. To deserve to be mentioned, the power consumption is much smaller than others and has great potential to implement the low power front-end circuits.

Table 2.2 Post simulation summary of the proposed frequency tripler

Technology	0.13-um CMOS 1P8M
Center Frequency	60 GHz
Input Power (20 GHz)	4 dBm
Output Swing (60 GHz)	270 mV
HRR 1st	31 dB
HRR 2nd	31 dB
HRR 4th	47 dB
DC Power Dissipation	8.5 mW
Supply Voltage	1.2 V

Table 2.3 Comparison with published frequency multiplier

	This work	[9]	[11]	[26]
Technology (um)	0.13 CMOS	0.15 pHEMT	0.15 pHEMT	0.25 pHEMT*
Sub-harmonic Number	3	3	3	3
Center Frequency (GHz)	60	36	76.5	76.5
Input Power (dBm)	4	9	8.5	17
Output Power (dBm)	**270 mV	-0.4	4.2	0
Conversion Loss (dB)	4.8	9.4	4.3	17
HRR 1st (dB)	31	22	16	24
HRR 2nd (dB)	31	22.1	32	19
HRR 4th (dB)	47	N/A	13	N/A
Power Consumption (mW)	8.5	39.2	N/A	50
Supply Voltage	1.2 V	1.5 V	2.5 V	2 V

* Dual recess process

** only output swing can be obtained

Chapter 3
RF Front-End Circuits

First of all, proposed receiver architecture is introduced together with its building blocks. In addition to the frequency tripler, the receiver requires a low noise amplifier and a down-conversion mixer. The frequency tripler is implemented by that mentioned in Chapter 2 and the other building blocks will be designed and simulated in the following subsections. Subsequently, a complete 60 GHz direct-conversion receiver which is integrated by these building blocks is simulated and the simulation results are presented.

3.1 Receiver Architecture and Design Considerations

Receiver Architecture

Figure 3.1 shows the block diagram of the proposed receiver. The circuit consists of a LNA, down-conversion mixers, output buffers and a frequency tripler. First of all, the RF input signal is amplified by a LNA which has low noise and sufficient gain to enhance the signal to noise ratio (SNR). The down-conversion mixer following LNA provides extra gain and down convert the RF signal to IF by mixing with proper LO signals. To obtain the desired LO signal, the 20-GHz differential input signal is supplied and through a frequency tripler on chip, the signal is multiplied to 60 GHz. Because of the poor properties of active and passive device characteristics at high frequency, this approach can design the high performance frequency synthesizer at relative low frequency. In other words, by supplying LO signals using low frequency PLL can promote the circuit to have better phase noise performance and reduce the power consumption of high frequency pre-scalar. To obtain the output performance of the receiver, the output buffer is exploited here for measurement consideration.

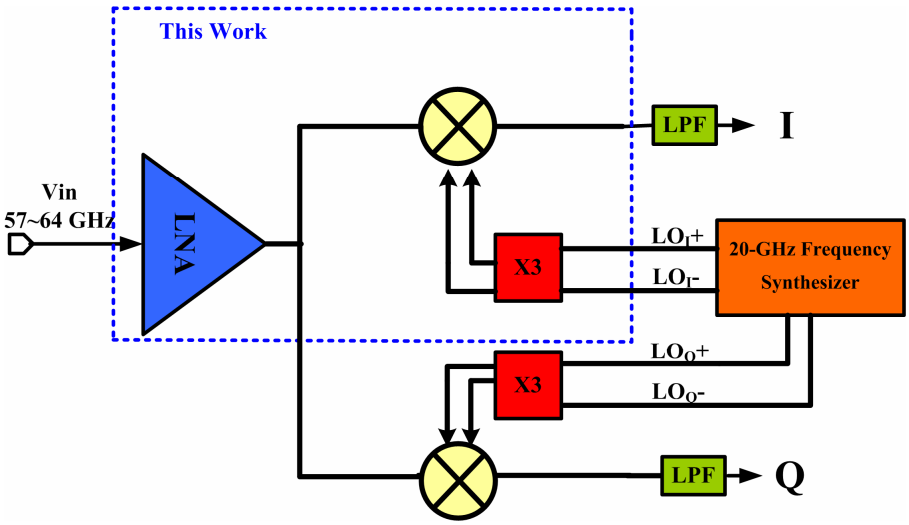


Figure 3.1 The proposed 60-GHz direct-conversion receiver architecture

Receiver Specifications

So far, there is still not a standard specification for 60 GHz band wireless communication system. From the system requirement, we could specify the receiver issues as follows:

The FCC made the 59~64 GHz unlicensed band available for use at first and extended it to 57~64 GHz subsequently. Both of the bands are widely designed and well applied in different countries. The 3-dB bandwidth covers from 57 to 64 GHz band are a better solution to conform each specification. For the sensitivity which can be calculated from IEEE 802.16 [6], the noise figure requirement of the receiver could be obtained. We note that the sensitivity is about -65 dBm and the channel bandwidth of 2 GHz drives to a noise figure of 12 dB.

Design Consideration of Transmission Lines

Since the f_T of nMOS is about 80 GHz in 0.13-um CMOS technology, the circuits would suffer from poor performances unless passive resonant devices are utilized in the design. Even though spiral inductors have better quality factors over tens of gigahertz, the large device occupied area will cause circuit integration even more difficult. In addition, the substrate eddy current at millimeter-wave will degrade the overall performance of the receiver. The receiver at the 60 GHz band usually claims for wide bandwidth in virtue of system requirement. Although high Q inductors get up to high gain performance, the bandwidth requirement may

not be achieved at the same time. More significantly, since silicon substrate is neither a perfect conductor nor good insulator, it would cause some current flow through the substrate. Magnetic coupling to the substrate significantly influences the inductance value at these frequencies and requires detailed knowledge of the substrate profile to develop an accuracy simulation models.

In contrast to spiral inductors, transmission lines (Tlines) substantially confine the electric/magnetic fields and hence better lend themselves to model. Coplanar lines in CMOS technology have already been characterized for frequency up to 50 GHz [5]. However, this structure still occupies large area and is not easy to integration a system. In this work, incorporates microstrip structures as they interact negligibly with the substrate and can be modeled more accurately. Meander configuration is applied to the circuit in order to mitigate the integration perplexity and exorbitant area usage, shown in Figure 3.2. The signal line is implemented by metal 8 while metal 1 under the signal line is used for being as ground plane. The ground plane can fully confine the electric and magnetic fields and eliminate the substrate induced losses. Comparing to coplanar architecture, this configuration saves the Tlines area even more and could alleviate routing difficulties when integrate the circuits.

By using the electromagnetic field simulator HFSS, the s-parameter around 60GHz could be simulated to compute the equivalent inductance value L_S and interior resistance R_S. The meander space S may be decided by layout and magnetic coupling considerations. Although small S can reduce the geometrical length, the mutual coupling between lines will become larger. In order to make sure how spacing S effect the performance, a simple structure is established as shown in Figure 3.3. Figure 3.4 plots the line characteristics as S varies from 5 um to 35 um. As expected, L_S and Q increase to some extent when S becomes larger. As this value increase to about treble the line width (about 15 um), the Quality factor reach to relatively constant and would not strongly influence the performance. This value is also acceptable for space consideration with other Tlines.

For a given meander length S=15 um, there are two parameters that may affect the inductance value (L_S) and quality factor (Q): total Tline length L and the width W. Figure 3.5 plots the equivalent inductance and quality factor as W varies from 3 um to 12 um while maintaining fixed total length at 400 um. It can clearly be seen that L_S decreases and Q increases as the width becomes larger. This is due to the fact that inductance is mainly determined by the outer magnetic flux generating from the conductor. Consequently, the self inductance increases when the width diminishes. Moreover, the resistance is inverse proportional to the width and quality factor can be improved as width become larger. Even though wider width can obtain better quality factor, it requires longer length to get the desired inductance and cause more parasitic capacitance. From the simulation results, the characteristic diminishing returns as W exceeds 5 um. Thus this value of W is chosen in this work. We can obtain the desired inductance by selecting the appropriate value of length.

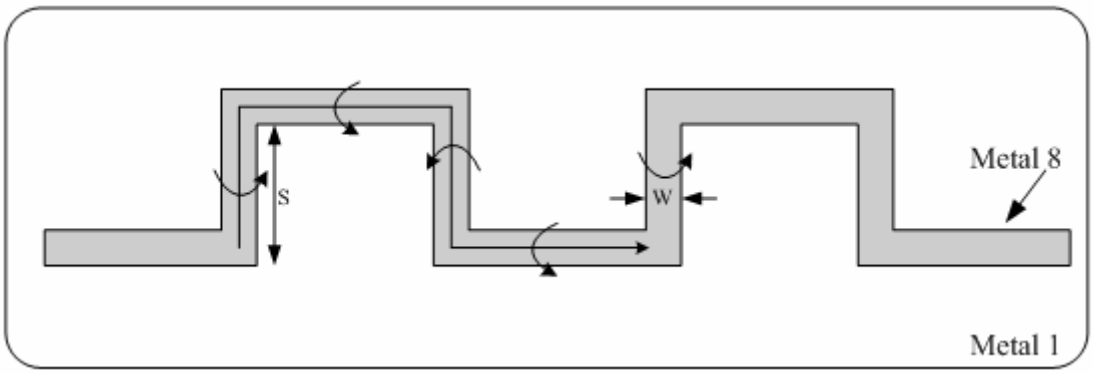


Figure 3.2 Geometrical lengths shortening by using Meander configuration

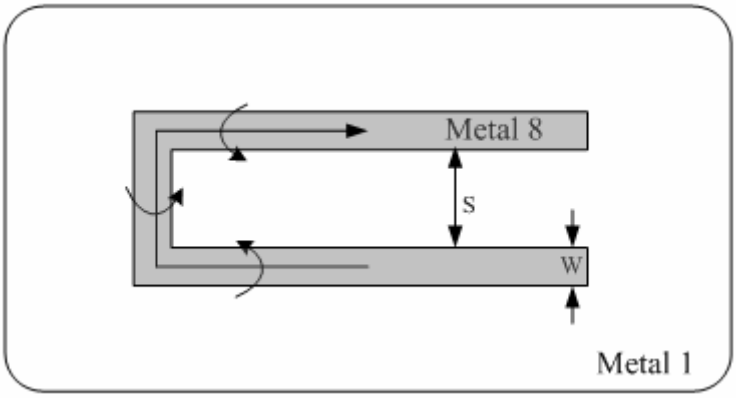


Figure 3.3 The test pattern of meander configuration

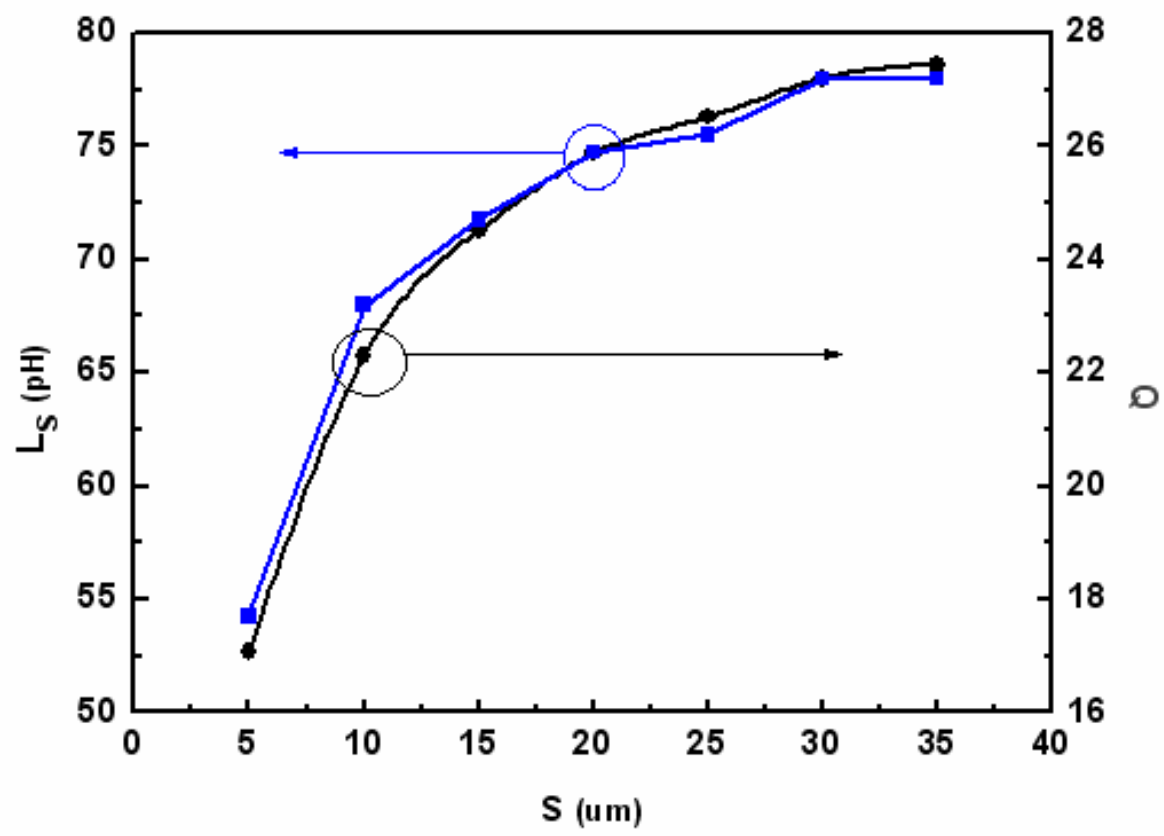


Figure 3.4 Inductance and quality factor variation as a function of S

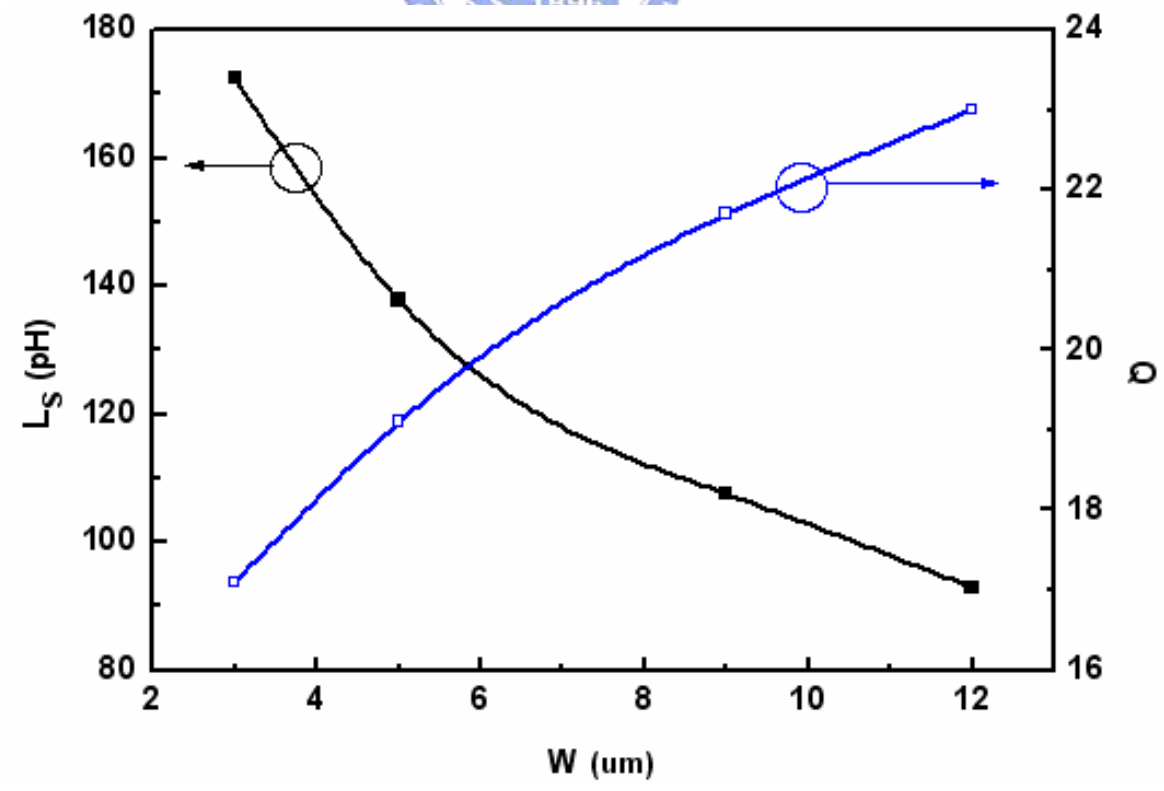


Figure 3.5 Inductance and quality factor variation as a function of S

3.2 Low Noise Amplifier Design

Low noise amplifier (LNA) is one of the key blocks in the RF transceiver because it is the first stage in the receiver chain. Thus, its performance would have great impact on the entire system. The main functions of LNA are amplifying RF signal receiving from the antenna, proving input impedance matching and contributing noise as few as possible. Additionally, to apply to 57 to 64 GHz wideband wireless communication, LNA faces some news challenges: the performances require broadband gain, wideband input matching and minimized noise figure must be satisfied simultaneously under acceptable linearity, power consumption and cost.

So far, most of the reported millimeter wave integrated circuit (MMIC) LNAs cover this band are implemented by using HEMT or SiGe process to achieve high ft, high gain and low noise performance [1]-[3]. Since CMOS technology has the function of low cost and high integration, several CMOS LNAs above 50 GHz were also reported [4]-[5]. So far, both of them use three-stage cascode amplifiers. However, the cascode structure requires higher supply voltage and consumes much more power. Moreover, since the input common-source device in the first cascode stage cannot provide enough gain, the noise from common-gate stage is referred to input without noise suppression. Hence the total noise contribution would be increased.

Here, we propose two kinds of LNAs to receive the V-band RF signal and perform low power and low noise issues. These methods can improve the noise and power performance while overcoming the defects of low isolation characteristic. The circuits are described and simulated as following.

3.2.1 Design Consideration

With an nMOS f_T of about 80 GHz in 0.13-μm CMOS technology, the receiver would suffer from several challenges implementing the 60 GHz wireless communication system. Besides the wideband gain requirement that covers entire unlicensed 7-GHz band, input matching, power, stability and noise figure are discussed in the following subsections.

Input Matching

Input matching is an important consideration for connection with external components. A 50-ohm-based approach is quite suitable and has become the conventional approach to well-matched with instruments. To simplify the input matching network, a common-source with source degeneration topology is used in both LNAs, as shown in Figure 3.6. C_{b1} is DC blocking capacitor and C_{pad1} is the equivalent pad capacitor at input terminal. The pad capacitance is designed as small as possible to avoid infirm of high frequency performance. The input impedance can be expressed as:

$$Z_{IN} \approx \frac{1}{sC_{pad}} // \left(\frac{1}{sC_{b1}} + s(L_s + L_g) + \frac{1}{sC_{gs}} + \frac{g_{m1}L_s}{C_{gs}} \right) \tag{3-1}$$

where C_{pad1} is always very small and C_{b1} is large enough to have less influence on the input impedance. Therefore, the equation 3-1 can be simplified to:

$$\begin{aligned} Z_{IN} &\approx s(L_s + L_g) + \frac{1}{sC_{gs}} + \frac{g_{m1}L_s}{C_{gs}} \\ &\approx \omega_T L_s \qquad (at\ resonance) \end{aligned} \tag{3-2}$$

At the series resonance of the input circuit, the impedance is purely real and proportional to L_s. By choosing L_s appropriately, this real term can be made equal to 50 ohm. If f_T is about 80 GHz, the 50-ohm impedance only requires 100 pH for L_s. This small inductance can easily be implemented by using micro-strip line. The gate inductance L_g is used to set the resonance frequency once L_s is chosen to satisfy the criterion with 50-ohm input impedance. Owing to the performance of L_g will critically influence the noise performance of LNA, we use the TSMC spiral inductor here which has better quality factor comparing to transmission line.

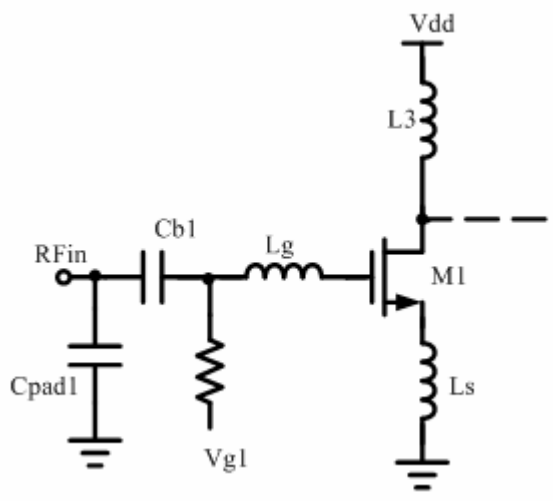


Figure 3.6 The input stage of proposed LNA

Noise Figure

In generally, the noise performance in the inductive degeneration configuration can obtain the minimal noise contribution comparing to the common-gate or cascode topology [28]. There are four main sources in inductor-degeneration configuration, thermal noise of channel current ($i_{n,o,d}$), gate induced current noise ($i_{n,o,g}$), thermal noise of source resistance ($i_{n,o,Rs}$) and thermal noise of output resistance ($i_{n,o,Rout}$). Figure 3.7 shows the equivalent noise model for the inductor-degeneration configuration. To simplify the analysis, the gate-drain capacitance (C_{gd}) is neglected here.

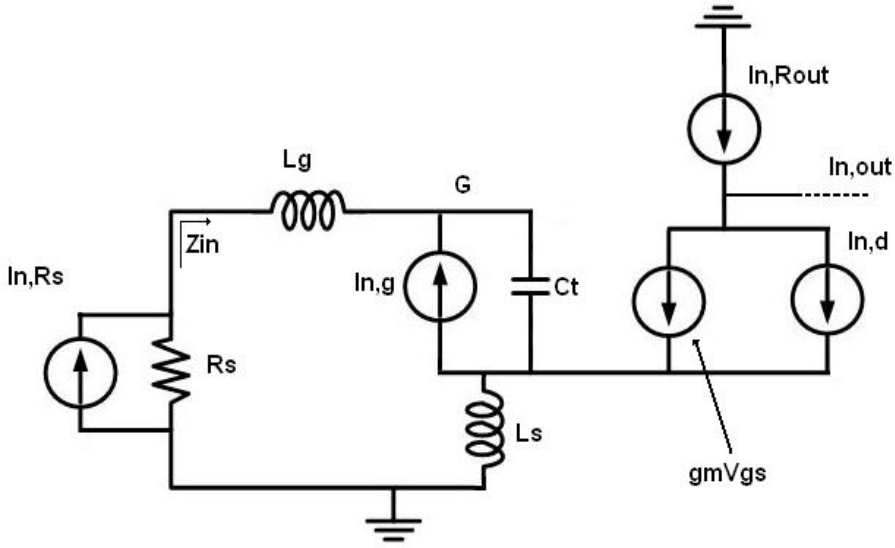


Figure 3.7 The equivalent noise model of the inductive degeneration configuration

From the noise analysis introduced in [29], we know that the four noise sources to the output noise current in/out at resonance can be written as:

$$i_{n,o,Rs} = \frac{g_m}{j2\omega_0 C_t} i_{n,R}, \quad i_{n,o,d} = \frac{1}{2} i_{n,d}, \quad i_{n,o,g} = \frac{g_m}{j\omega_0 C_t} \frac{jR_s\omega_0 C_t - 1}{j2R_s\omega_0 C_t}, \quad i_{n,g} \quad i_{n,o,Rout} = i_{n,Rout}$$

From the deviation, we can get the noise factor of the input stage and be written as:

$$F = \frac{\overline{i^2}_{n,o,R} + \overline{i^2}_{n,o,g} + \overline{i^2}_{n,o,d} + \overline{i^2}_{n,o,corr} + \overline{i^2}_{n,o,Rout}}{\overline{i^2}_{n,o,R}}$$

$$= 1 + \frac{\beta_1 (Q^2 + \frac{1}{4}) P^2 \frac{g_m^2}{g_{dn}} + \frac{\gamma_1}{4} g_{dn} + \sqrt{\frac{\gamma_1 \beta_1}{4}} cPg_m + \frac{1}{R_{out}}}{R_s Q^2 g_m^2}$$

Where Q is the quality factor of the input circuit and can be written as

$$Q = \frac{1}{(R_s + g_m \frac{L_s}{C_t})\omega_0 C_t} = \frac{1}{2R_s\omega_0 C_t}$$

and P is defined as:

$$P \equiv \frac{C_{gs}}{C_{gs} + C_{gs0}}$$

where C_{gs0} is non-negligible overlap capacitance between gate and source.

For the circuit designer, variable parameters are V_{DD}, W, L and V_{gs}. In general, the minimum value of L is chosen for higher unit current gain frequency and can achieve lower noise figure performance. By choosing the limited drain current of the MOSFET, the optimal value of the channel width and P is selected, since V_{DD} has been specified on 1.2 V.

Gain and Linearity

Normally, we require large gain and better linearity at the same time to satisfy the circuit requirements. However, on using the structure of common-source, gain and linearity are greatly depended on gate bias and would always be a tradeoff. In the V-band, the circuit is normally designed to promote the gain as large as possible while having appropriate linearity owing to low g_m consideration.

In order to achieve both of gain and bandwidth requirements, there are several ways to reach the goal: for example, the method generally used is to vary the capacitance or change the inductance by switching inductors in RF load. The former is realized by adding capacitance to change the resonant frequency as needed, which leads to decrease the load impedance and a wideband gain variation across the band of interests. The latter is generally considered infeasible due to the nonlinearity of most switches [8]. However, due to respective low quality factor (Q) characteristics of the transmission-line at desired frequency, the circuit could naturally reach the enough bandwidth without any additional components. The use of micro-strip line here can avoid the noise contribution from substrate and by applying ground plane under the transmission line, more accuracy Tline characteristics can be estimated when simulating by EM simulator.

Stability of the LNA

The stability of the LNA needs to be concern since common source structure may cause potential instability in the circuit. Various methods of analysis are available for the stability of the amplifier. The popular way to evaluate the stability is examined with Rollett stability factor [1] defined as

$$K = \frac{1+|\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{11}||S_{22}|}$$

$$\text{where } \Delta = S_{11}S_{22} - S_{12}S_{21}$$

And stability means, defined as

$$b = 1+|S_{11}|^2 - |S_{22}|^2 + |\Delta|^2$$

If K > 1 and b > 0, then the circuit is unconditionally stable, i.e. it does not oscillate with any combination of source and load impedance. These conditions must be satisfied over whole frequency range that signals may fall in.

3.2.2 A 0.8-V 70-GHz Three-stage Cascaded Common-source Topology with Inductive Feedback

Circuit Realization

A three-stage cascaded common-source topology is designed for the proposed LNA. The complete schematic is shown in Figure 3.8. The first stage is designed to provide a better noise figure performance and the second and third stages are designed to increase amplification. As a direct consequence of the use of common source structure in the proposed LNA, the voltage can be reduced to 0.8 V, which is much lower than for the cascode structure. Therefore, the level of power consumption can be reduced greatly in the proposed LNA.

The input stage is the most significant part of LNA performance because it dominates the input matching ability and overall noise performance. Moreover, any gain in the input stage can suppress noise levels in the subsequent stages. In order to simplify the input matching network, a common-source with a source degeneration topology is applied [6]. Another advantage of this technique is that the noise and input impedance matching at the desired frequency can be brought closer together by selecting appropriate values for the degeneration inductor L_S and gate inductor L_g. The capacitance C_{Pad1} is the input pad capacitance which is always designed as small as possible in order to limit its influence on a received signal. On the other hand, the C_{b1} is the input bypass capacitor that is usually designed with large value to block the dc level and to avoid attenuating the input signal amplitude.

The second stage is used to increase the overall gain performance of an LNA. To reduce the noise contribution caused by second stage, a conventional common-source topology is applied because of its high gain and low noise characteristics. In order to achieve a higher gain, the degeneration inductor is removed from the second stage

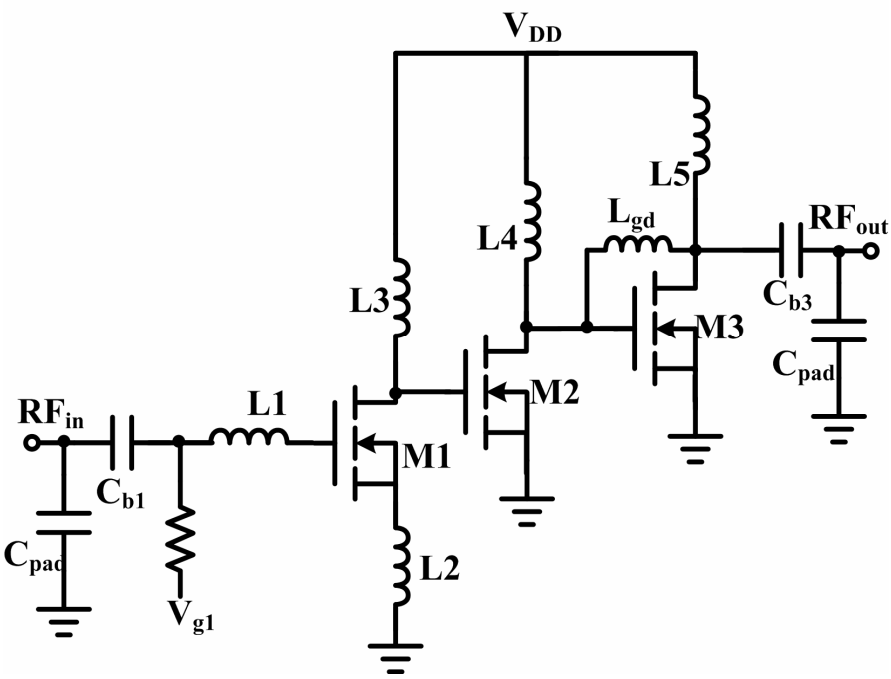


Figure 3.8 The circuit diagram of CMOS V-band *LNA*

Table 3.1 Detail parameters of 70GHz LNA

M_1	12 um / 0.13 um	L_5	Tline 155 pH
M_2	9.6 um / 0.13 um	L_{gd}	w=3 um r=19 um nr=2
M_3	13.8 um / 0.13 um	C_{pad}	20 fF
L_1	w=3 um r=15 um nr=0.5	C_{b1}	MIM 11um x 10um
L_2	Tline 55 pH	C_{b2}	MIM 6um x 5um
L_3	Tline 165 pH	R_1	5 kohm
L_4	Tline 135 pH	Vdd	0.8 V

The last stage is added not only to provide extra gain but also to match the output impedance for the measurement requirements. Owing to the fact that the measurement instruments are 50-ohm system, the output impedance must be transformed from high impedance to 50 ohm and the characteristics of the drain terminal of MOS M_3 must be changed significantly. Due to the low isolation characteristic of MOSFET at Millimeter Wave (MMW) frequency approaching f_T, the performance of the second stage will also be affected

by the output matching network thus making the circuit difficult to design. Therefore, a common-source with a gate-drain inductance feedback is proposed to oscillate the gate-drain parasitic capacitance of M_3 in order to increase the isolation. Hence we can only match the output impedance by using a dc blocking capacitance C_{b2} and equivalent pad capacitance C_{pad2} .Thus the output matching can be completed without the use of an additional output matching network. The inductors L_3, L_4 and L_5 are used to peak the amplified signal to the desired operating frequency of M_1, M_2 and M_3 respectively.

Most of the previously reported multi-stage cascaded LNAs involve a redesign of the bias voltage of each stage by using blocking capacitors to achieve low power consumption [7]. However, passive devices may also contribute noise and increase the overall noise figure. Hence, instead of biasing each stage again, a directly supply-voltage is used.

The capacitance coupling between the transmission line and the substrate is often the dominant source of high frequency loss [8]. In order to reduce substrate induced losses, a micro-strip structure is used as an inductive element due to its shielding effect of the ground plane. The structure can be realized with Metal 8 as the signal line and Metal 1 and Metal 2 forming the ground plane. In order to accommodate metal density, some space needs to be left on the ground plane. Therefore, a double-layer ground plane is adopted here instead of a single-layer ground plane in order to reduce the loss of signal caused by a substrate. The meandering configuration is used to shorten the geometrical length in order to reduce the overall chip size. Furthermore, the meandering configuration will increase the quality factor of the inductors due to its magnetic coupling [9]. The resulting chip size is 0.67x0.57 mm^2, Inclusive of all I/O pads and dummy metal.

3.2.3 A 60-GHz Two-stage Low Noise Amplifier

Circuit Realization

The proposed LNA is designed as a two-stage single-ended amplifier that is applied for 60-GHz receiver system. The complete schematic is shown in Figure 3.9. The first stage is designed not only for input matching consideration, but also make the noise as small as possible. The second stage is designed for enhance the gain performance and transform the signal to current to feed to the mixer. Considering the integration requirements, the supply voltages of each receiver building blocks are given as 1.2 V which is a standard voltage for 0.13-um CMOS technology. Comparing to the supply voltage of 0.8 V that mentioned above, this supply voltage leads the cascode structure available to use and could lead to improve the performance. Although the supply voltage is increased but there are only two stages used here and by limiting the gate bias, the power consumption could also be restricted.

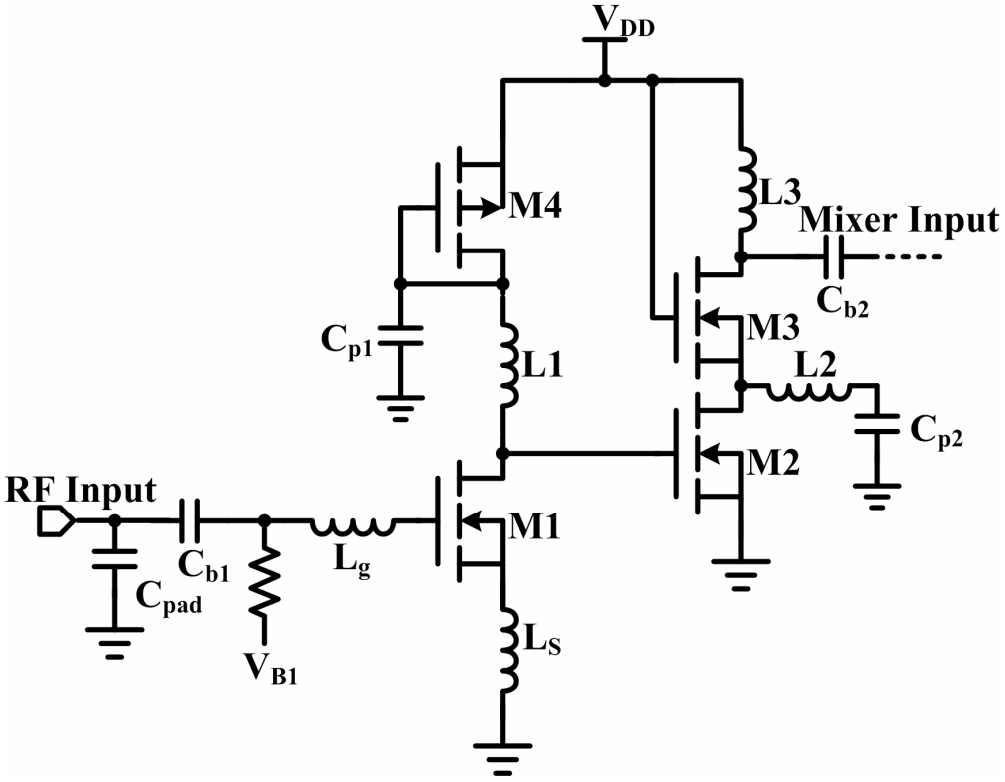


Figure 3.9 The circuit diagram of CMOS 60 GHz LNA

Table 3.2 Detail parameters of 60GHz LNA

M_1	16 um / 0.13 um	L_g	w=3 um r=15 um nr=0.5
M_2	16 um / 0.13 um	C_{pad}	20 fF
M_3	18 um / 0.13 um	C_{b1}	MIM 14um x 13um
M_4	200 um / 0.13 um	C_{b2}	MIM 4um x 4um
L_1	Tline L=155 pH	C_{p1}	> 8 pH
L_2	Tline L=240 pH	C_{p2}	> 5 pH
L_3	Tline L=230 pH	R_1	5 kohm
L_S	Tline L=70 pH	V_{DD}	1.2 V

The first stage dominates the input matching ability and overall noise performance because the gain of the first stage can suppress the noise contribution from the subsequent stages. In order to improve gain and noise performances, a common-source with source degeneration topology is applied. By selecting the appropriate values of the degeneration inductor L_S and the gate inductor L_g, noise and input impedance matching at the desired frequency can be achieved. The device size and bias point of the input MOS should be optimized for best noise performance, of which this stage dominant noise contribution of the entire receiver. Figure 3.10 shows the simulated NF_{min} for different NMOS width. Considering the bias point of second stage, the V_{DS} is setting to 0.7 V. The data show that for W=16 um, the device has best noise performance while achieving reasonable gain. Figure 3.11 is the simulation results of NF_{min} and maximum available gain (MaxGain) with variation of gate voltage. As can be seen, minimum NF_{min} happens at gate voltage around 0.55 V to 0.65 V and MaxGain achieves relative high when V_{GS}=0.65 V. Thus, this V_{GS} is chosen in this work.

So far, most of the previously reported multi-stage cascaded LNAs bias each stage separately by using blocking capacitors to reduce power consumption [5]. However, the non-ideal effect and parasitic capacitance of the passive components would also contribute

some noise referring to the input and increase the overall noise figure. Moreover, the dc blocking capacitances also cause a signal decrease due to the parasitic capacitance of the input MOSFET and therefore the small signal gain decreases. To solve this problem, the dc voltage of the second stage is appropriately designed by using a PMOS load M_4 as shown in Figure 3.9. The capacitance C_{b1} is a bypass capacitance which provides an ac ground path at the drain of M_4. This approach could be achieved without additional dc bias pins between first and second stage and makes the circuit more flexible to design.

The second stage is implemented by using a cascode structure as the other gain stage and this provides the output current to the next stage. The conventional cascode structure provides the advantages of a low noise figure, a high gain and a high reverse isolation at a frequency much lower than f_T as shown in Figure 3.12(a). However, at the frequency round 60 GHz, the pole at the drain of M_1 shunts the RF current to ground, hence degrading gain and raising the noise contributed by M_2; as a result, the performances of gain and noise are degraded. The inductive peaking technique could resonates the parasitic capacitance at drain of M_1 and overcome the signal loss problem, as shown in Figure 3.12(b). Therefore, the inductive peaking technique is applied in this study to resonate with the parasitic capacitance at the drain of M_2 and to improve the performance of this stage. This scheme not only provides better noise and gain performances but it also improves the degree of isolation. Comparing to the LNA introduced above, using this structure could replace the large feedback inductor (about 470 pH) to small peaking inductor (about 240 pH). This small inductor could be implemented by transmission line that could greatly reduce the chip area and is superior to integration. The capacitor C_1 is used to block the DC from ground here.

To reach the maximum gain around center frequency, the inductors L_1, L_2 and L_3 are used to resonate with the capacitance at the drain of M_1, M_2, M_3, respectively.

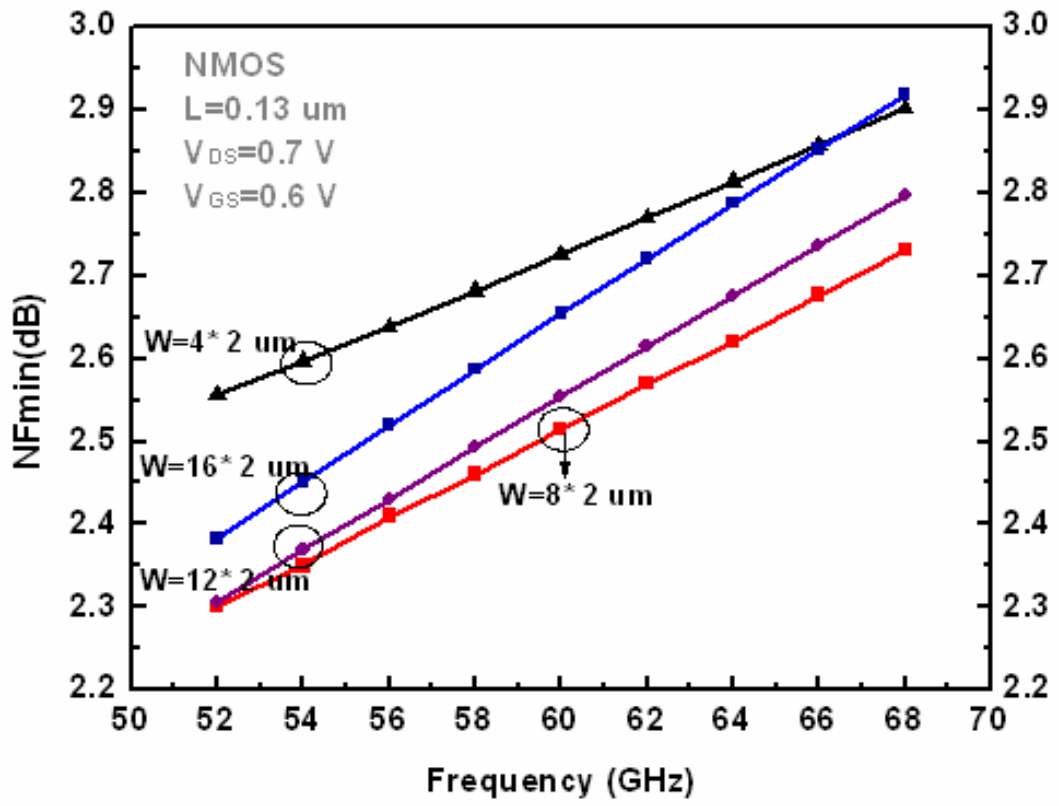


Figure 3.10 Comparison of simulated NF_{min} with different device width

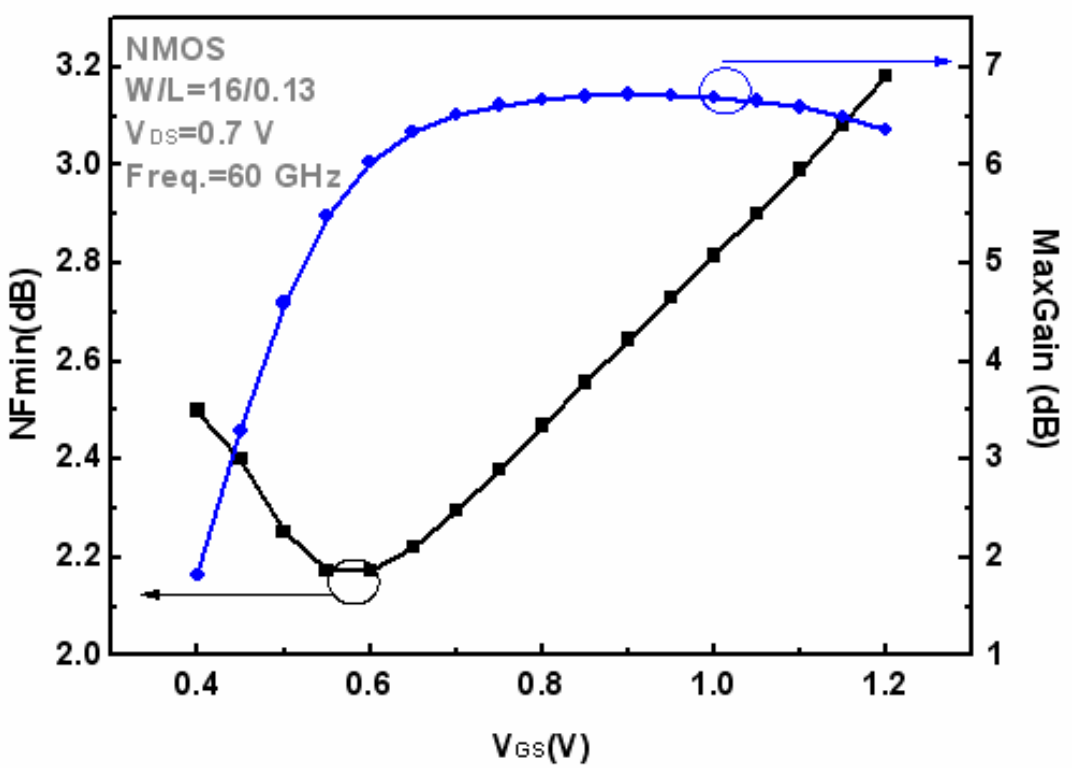


Figure 3.11 Comparison of simulated NF_{min} with different gate bias

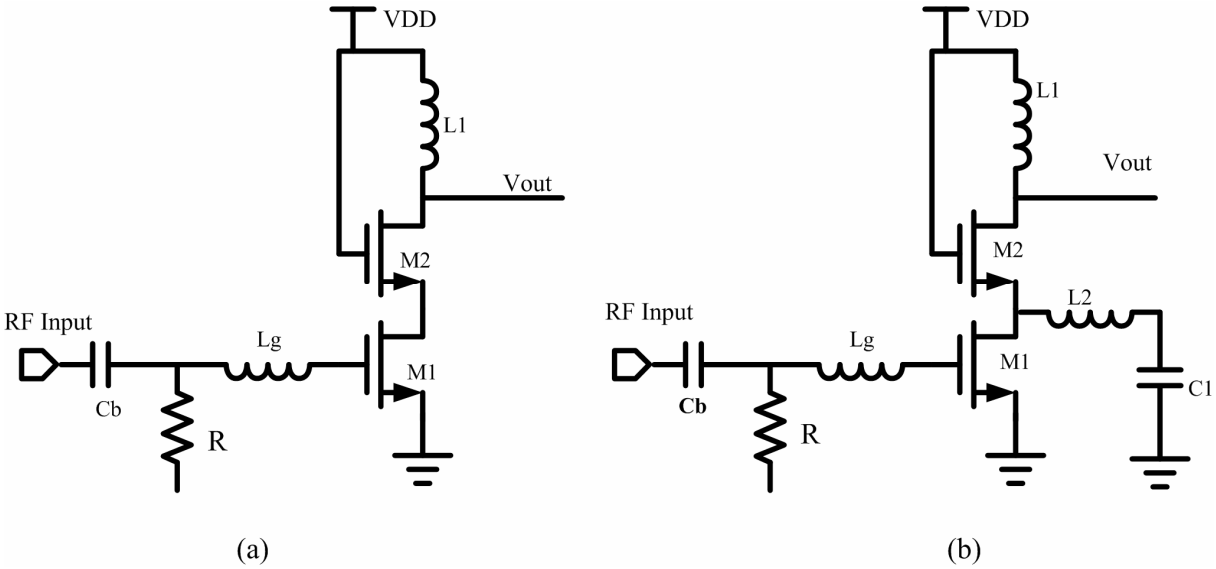


Figure 3.12 (a) Conventional and (b) Proposed circuit diagram of Cascode topology

3.2.4 Simulation Results of LNAs

Post-simulation is completed by ADS and EM simulator HFSS with process parameters of TSMC 0.13-um mixed signal 1P8M salicide 1.2 V/2.5 V RF SPICE models. LNA is the first stage of this receiver and provides 50-ohm input matching, voltage gain, low-noise contribution, and sufficient linearity for minimum distortion to the receiver in the frequency bands of interests.

☆ **A 70 GHz Three-stage Cascaded CS LNA**

Figure 3.13 shows simulated input/output (IO) return loss of proposed LNA under TT corner. It reveals that under the operating frequency, the simulated S11 and S22 are lower than -10 dB from 67.5 to 80 GHz and 67.5 to 72 GHz, respectively. Figure 3.14 plots the simulated small signal gain from 60 to 80 GHz at 0.8-V drain bias with total current of 7.5 mA. It shows that peak gain could achieve 13.2 dB at 69 GHz while covering 7 GHz 3-dB bandwidth from 66 GHz to 73 GHz. The noise figure performance at the same bias point is shown in Figure 3.15. and exhibits a noise figure lower than 5.3 dB from 66 to 74 GHz with a minimum of 4.9 dB at 69.5 GHz. Fig 3.15 exhibits the simulated input 1-dB compression point (P_{1dB}) to obtain

the input power when gain drops 1 dB and is about -17 dBm when V_{DD} is given to 0.8 V. In order to ensure the stability of the LNA, Rollet stability factor and stability measure parameters are reexamined. The simulated stability factor is greater than 1 and stability means is positive which means that the circuit is unconditionally stable as shown in Fig 3.16. The summary of the proposed 70-GHz LNA is listed in Table 3.3.

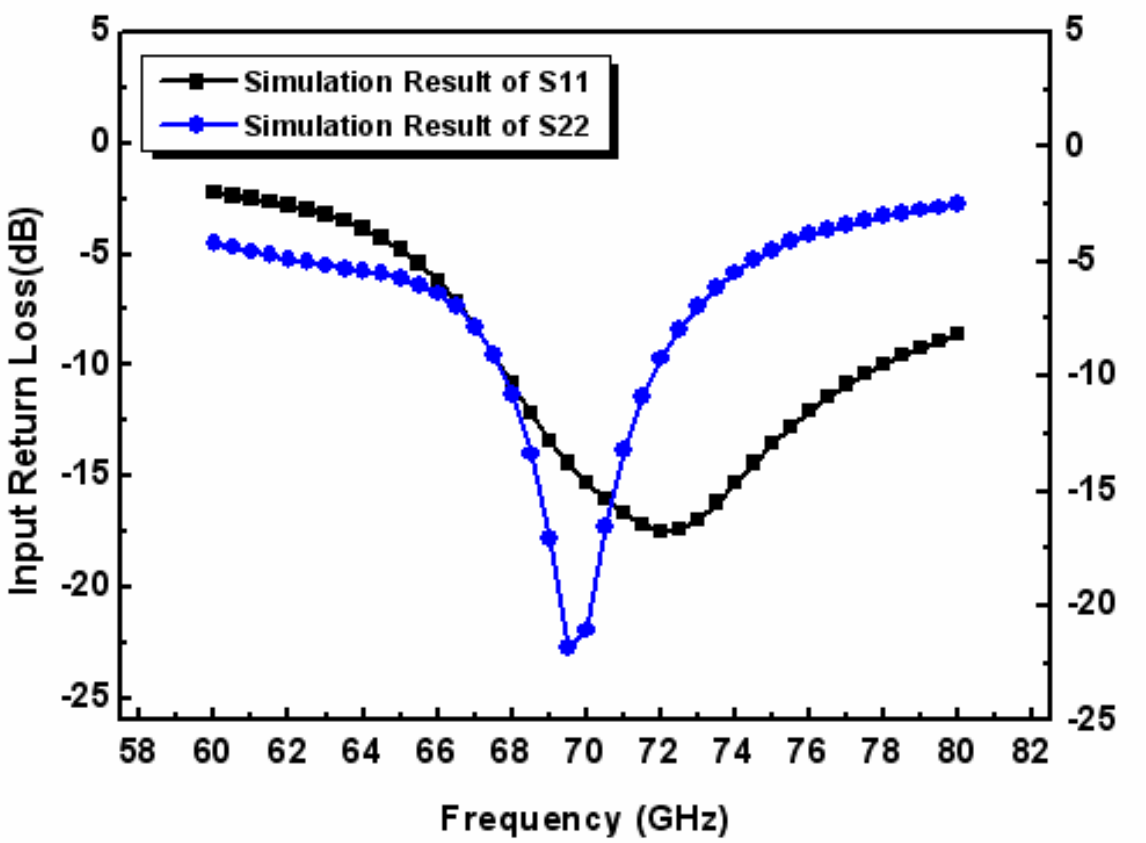


Figure 3.13 Simulated I/O return loss of the proposed 70-GHz LNA

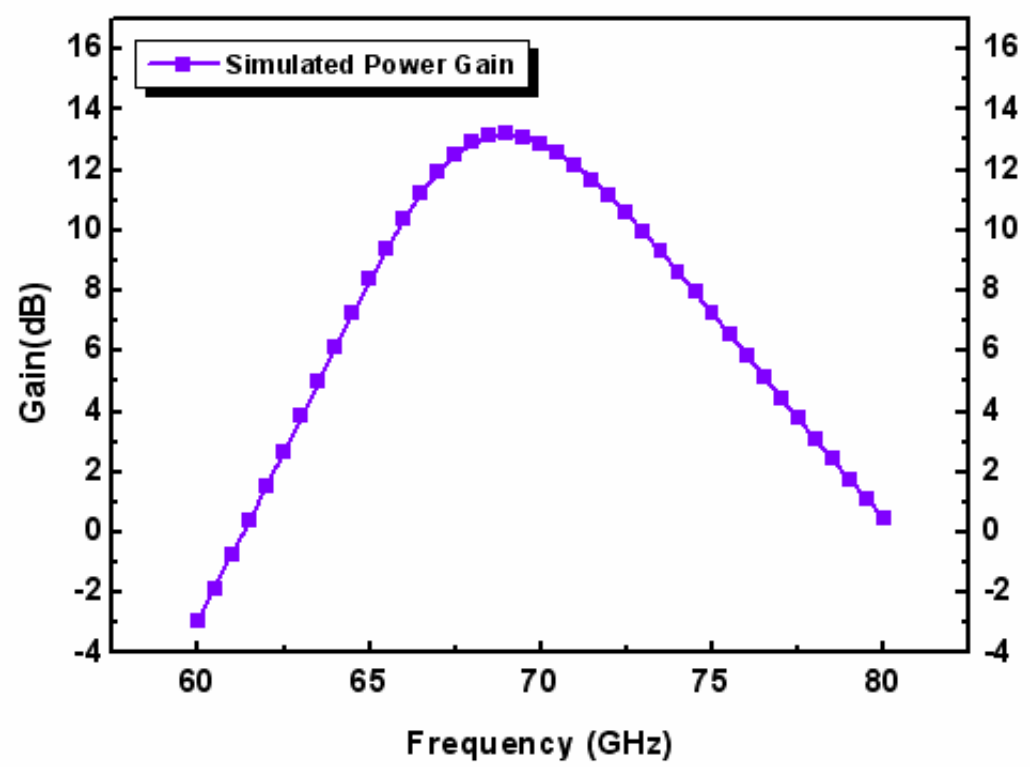


Figure 3.14 Simulated S21 of the proposed 70-GHz LNA

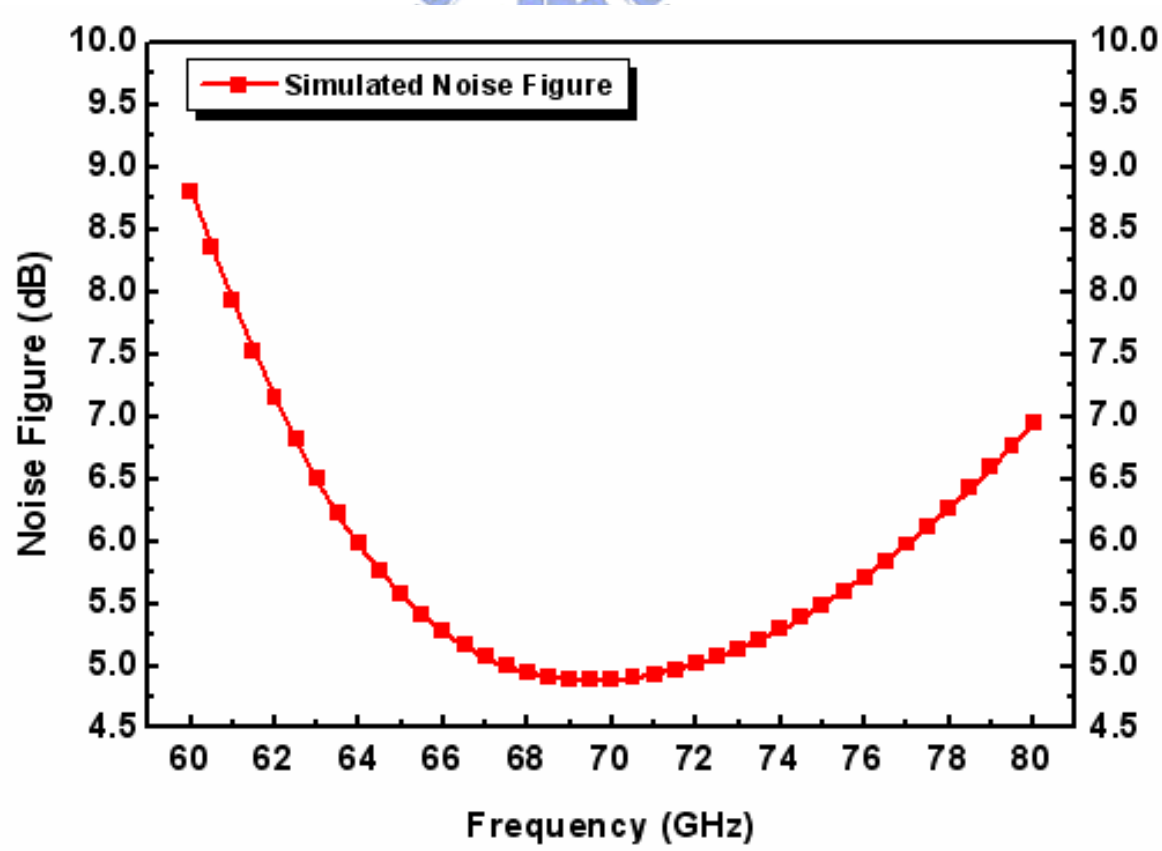


Figure 3.15 Simulated NF of the proposed 70-GHz LNA

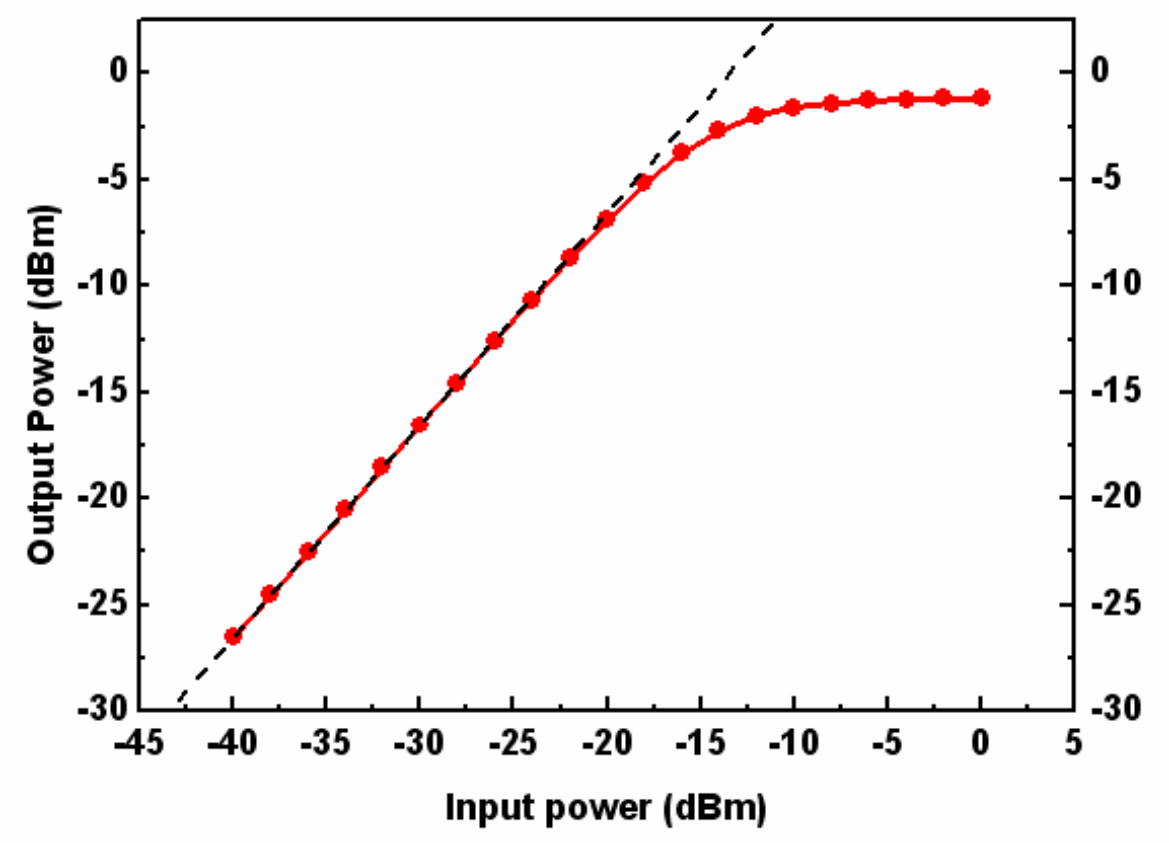


Figure 3.16 Simulated P_{1dB} of the proposed 70-GHz LNA

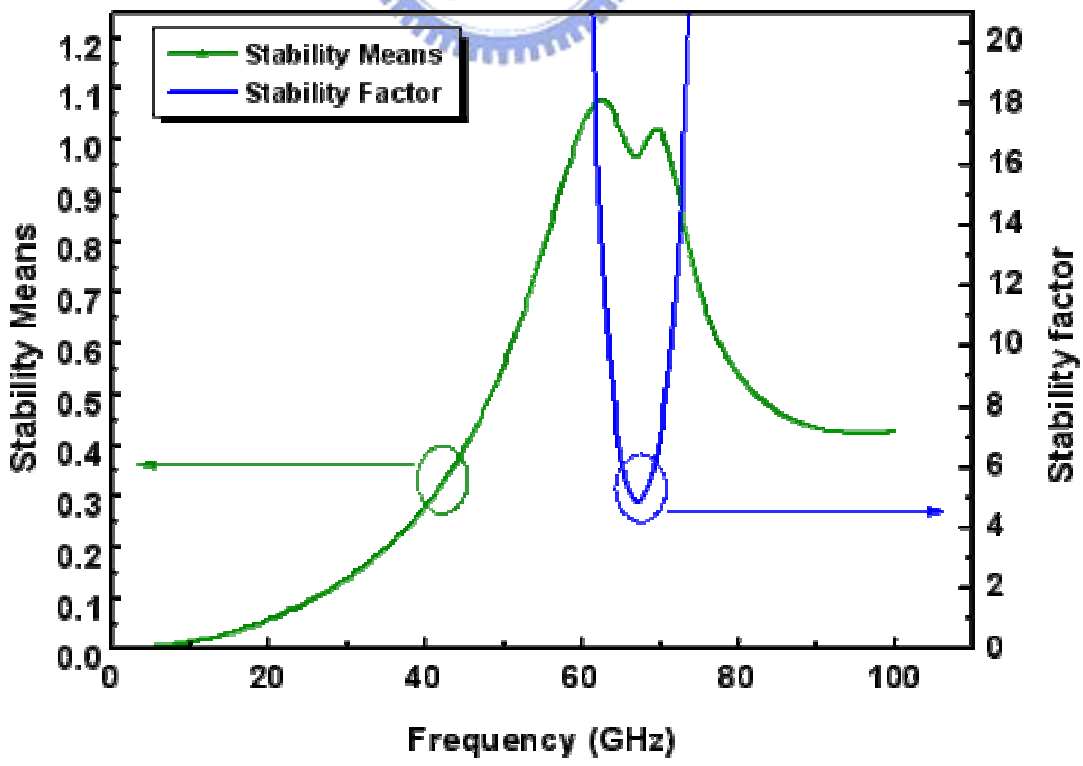


Figure 3.17 Simulated Rollet stability factor of the proposed 70-GHz LNA

Table 3.3 Post simulation summary of the 70GHz LNA

Technology	0.13-um CMOS 1P8M
Center Frequency	68.5 GHz
3dB Band-width	66~72.7 GHz
Gain	13.2 dB
NF	4.9 dB
P_{1dB}	-16.8 dBm
Power Dissipation	6 mW
S11 [dB]	<-13 dB
S22 [dB]	<-16 dB
Supply Voltage	0.8 V

☆ A 60 GHz Two-stage LNA circuits of Receiver

Resembling to the circuit mentioned above, we list the simulation results that LNA in entire receiver chain concerns about. Comparing to the previous work which matches the output impedance to measurement instruments (50 ohm), LNA in the receiver chain must matching output to mixer input. Moreover, the supply voltage in the circuit is chosen as 1.2-V to integrate with other building blocks of the receiver. Figure 3.18 and Figure 3.19 plots the simulated input return loss and small signal gain from 50 to 70 GHz while consuming 4.8 mW. The input return loss is better than -10 dB between 58 GHz and 71 GHz and voltage gain is higher than 9.5 dB from 56 to 65 GHz with a peak gain of 12.3 dB at 61 GHz. The NF performance of proposed LNA is shown in Figure 3.20. As can be seen, the NF is lower than 4.5 dB over desired frequency band (57 to 64 GHz) and may achieve minimum value of 4.3 dB at 61 GHz. Figure 3.21 shows the P_{1dB} is better than -13.5 dBm when using 1.2-V power supply and 0.63-V gate bias. At last, the stability factor and stability measure are shown in Fig 3.21 to ensure the circuit is unconditionally stable. The summary of the proposed 60-GHz LNA in entire receiver chain is listed in Table 3.3.

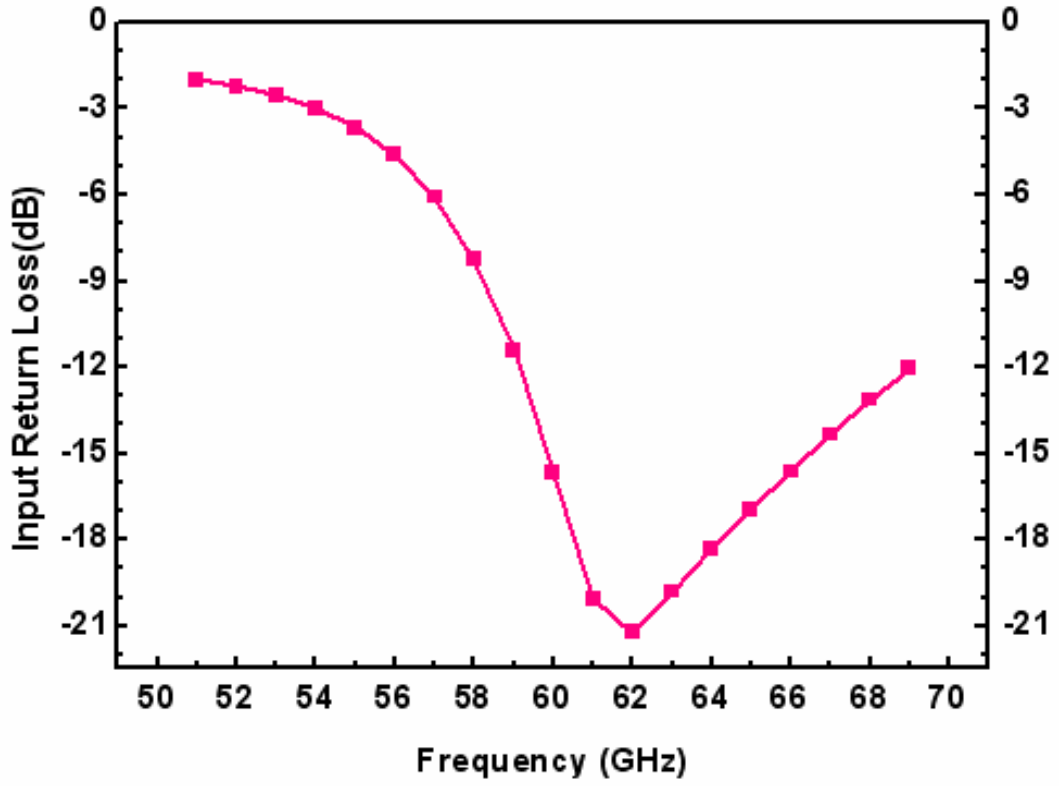


Figure 3.18 Simulated S11 of the proposed LNA of 60GHz receiver

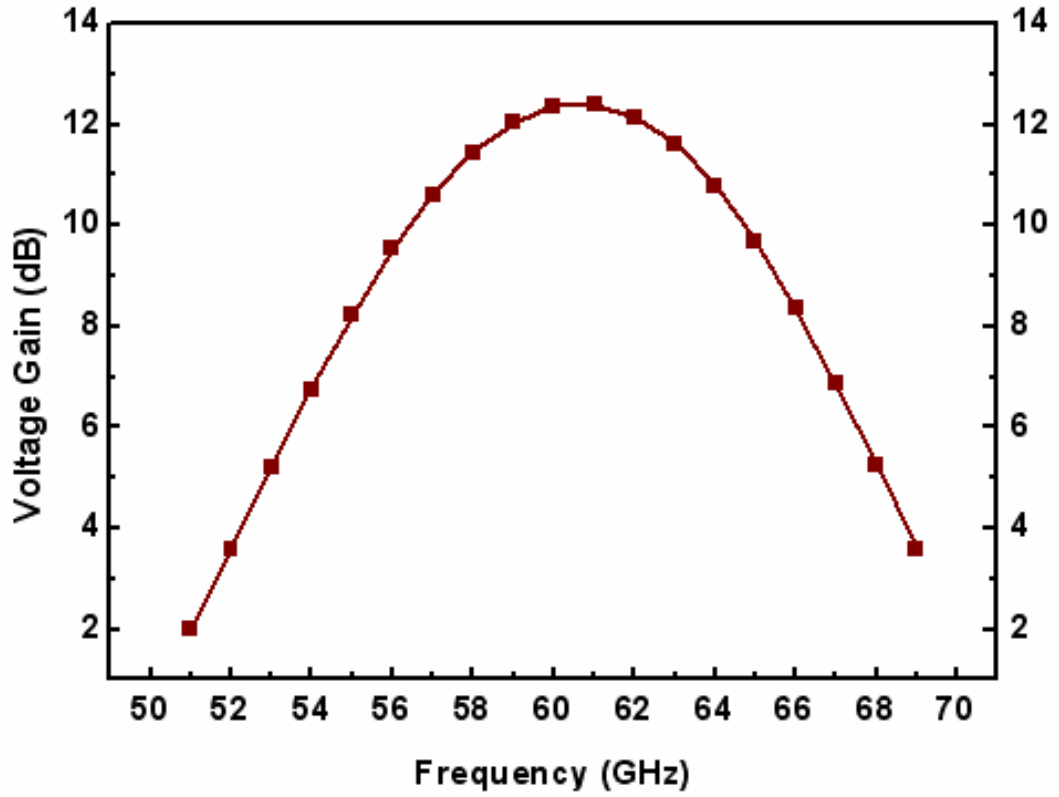


Figure 3.19 Simulated voltage gain of the proposed LNA of 60GHz receiver

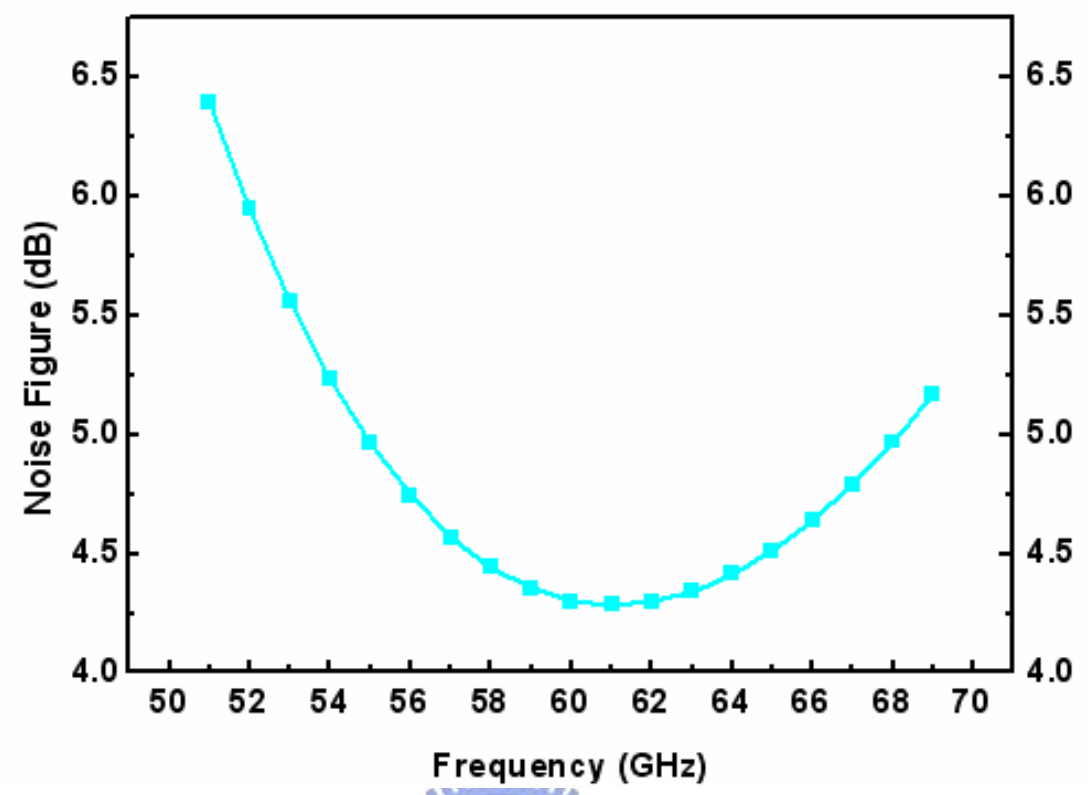


Figure 3.20 Simulated noise figure of the proposed LNA of 60GHz receiver

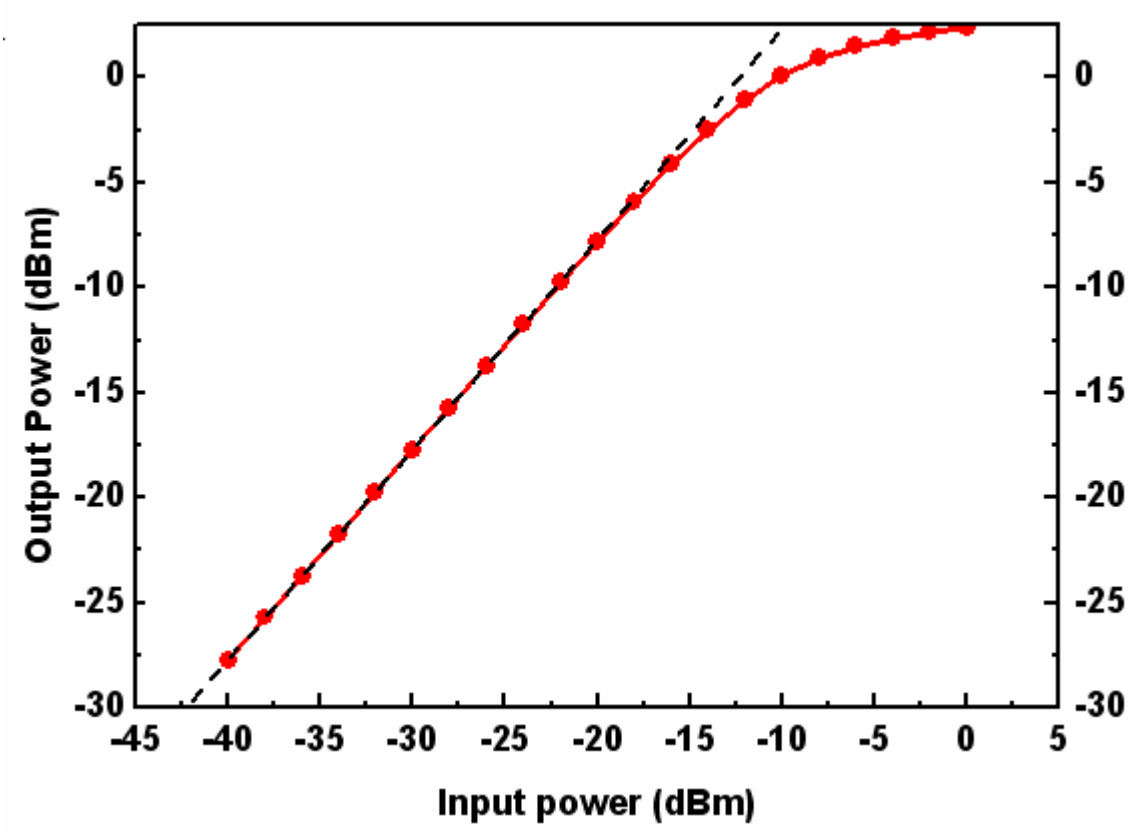


Figure 3.21 Simulated P_{1dB} of the proposed LNA of 60GHz receiver

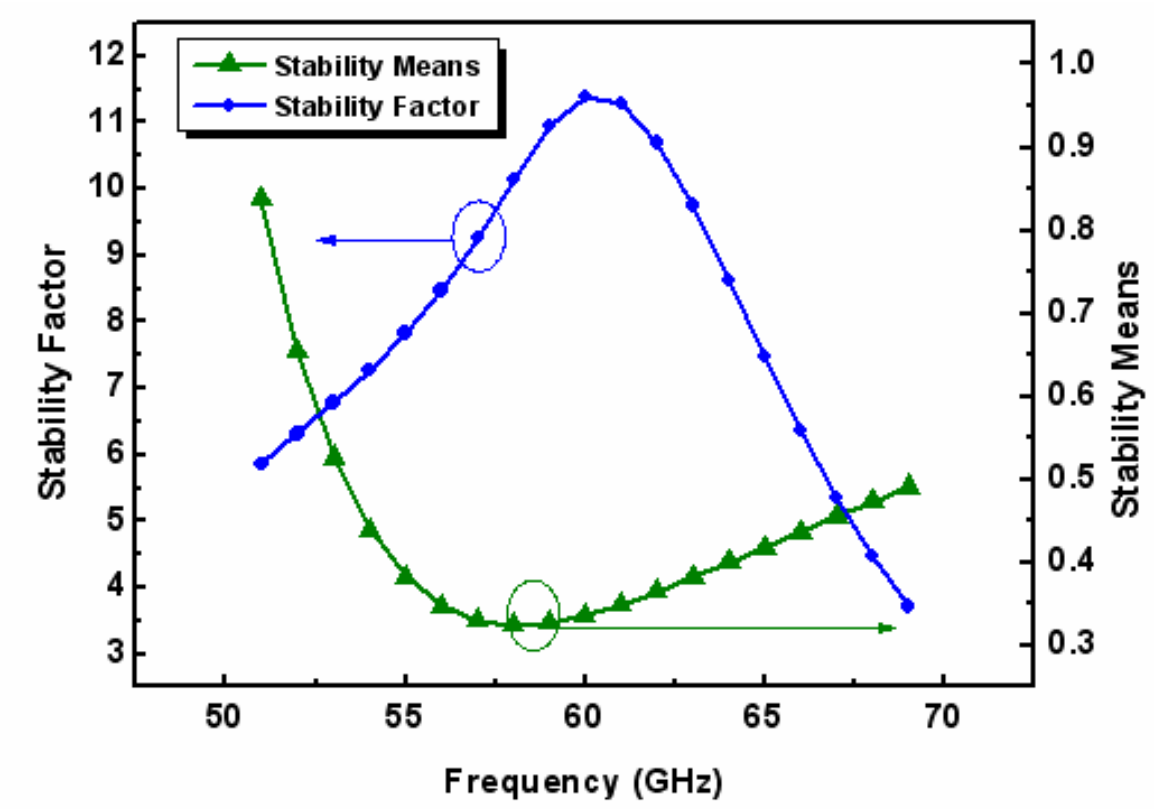


Figure 3.22 Simulated stability factor and meansure of the proposed LNA of 60GHz receiver

Table 3.4 Post simulation summary of the 70GHz LNA

Technology	**0.13-um CMOS 1P8M**
Center Frequency	**61 GHz**
3dB Band-width	**56 ~ 65 GHz**
Gain	**12.3 dB**
NF	**4.3 dB**
P_{1dB}	**-13.2 dBm**
Power Dissipation	**4.8 mW**
S11	**<-15 dB**
Supply Voltage	**1.2 V**

3.3 Down Conversion Mixer

Down-conversion mixer is the circuit block following the LNA in the receiver chain and converts the RF signal amplified by the LNA to the lower IF signal. With proper selection of the LO and the RF frequencies, the signal at frequency of interests can be obtained. Besides providing adequate conversion gain with acceptably low noise, linearity is also a critical consideration which dominates the entire receiver linearity greatly. According to Farris equation, the noise of mixer could be suppressed by the gain of LNA. But with an NMOS property in 0.13-um CMOS technology, it becomes somehow difficult to obtain the sufficient gain at desired frequency that we still desire the noise as small as possible to enhance the receiver performance. At last, common-source buffers follow by mixer output is designed for measurement requirement. Figure 3.23 is the simplified circuit diagram of the proposed mixer.

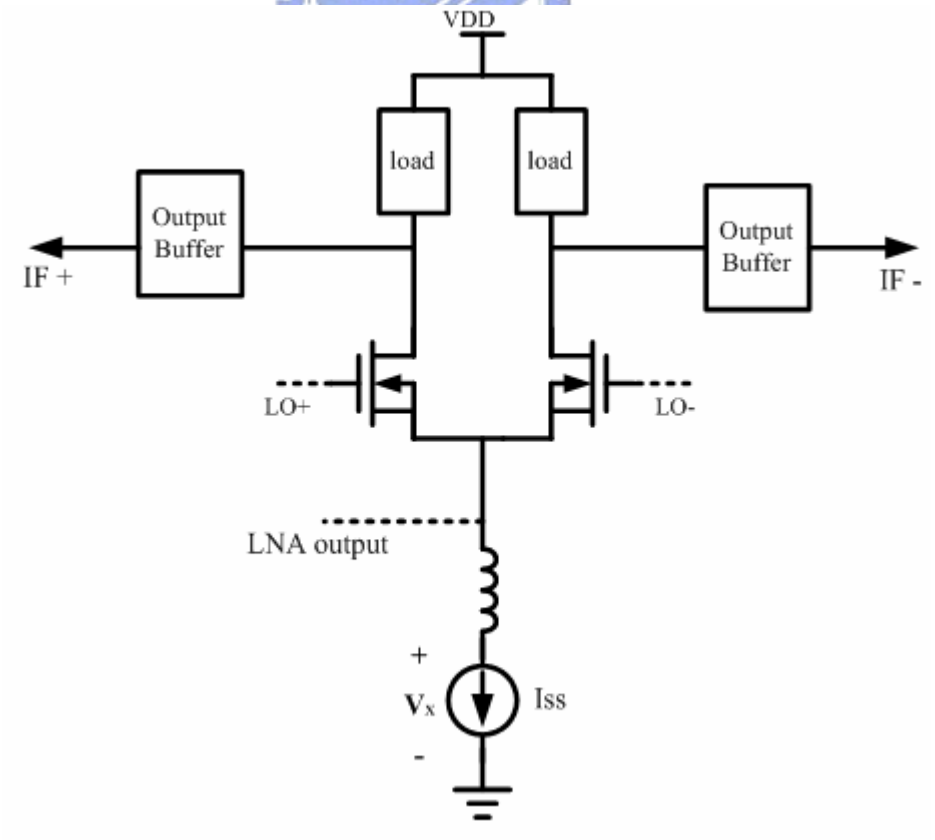


Figure 3.23 Circuit block of the proposed down-conversion mixer

3.3.1 Design Consideration of Mixer

The proposed mixer is realized by a single-balanced mixer here. Differential output is preferred for higher conversion gain which is twice of single end and more immunity to RF-IF feed-through. Otherwise, any strong interferers at RF port will undergo inter-modulation. For the same power consumption, the input referred noise of the single balanced mixer is less than that of double-balanced architecture. A main drawback is high LO to IF feed-through, which may desensitize the subsequent stage. To analysis the mixer performances, two of the most importance parameters, linearity and conversion gain is discussed here in the following subsections.

Linearity

As same as amplifiers, 1-dB compression point defines the upper limit of a mixer's dynamic range. The compression in a mixer can occur due to two reasons: the limitation of voltage headroom or due to odd order nonlinearity. Though the third order intercept point (IIP_3) measures only the third order nonlinearity, high order harmonic nonlinearity should be considered where higher input power is available. A balanced structure could normally suppresses even order distortion and enhance LO to RF isolation. However, the benefits of balanced structure would be degraded due to device mismatch in the RF path. For direct conversion application, even order distortions also need to be considered because even order harmonic of LO signal would also be translated to DC level due to even order of RF signal. Thus, we applied the circuit to translate the RF signal to very low IF signal such as 50 MHz to avoid this kind of distortion. Besides reducing the harmonic effect, the over-all linearity of the mixer can be improved by providing enough headroom.

The available headroom in most cases is limited by V_{DD}, especially in deep-submicron technology with low supply voltage which would greatly restrict the output voltage swing. The available voltage headroom is mainly depended on bias conditions and choice of load

resistance. Thus the available headroom can be expressed as $V_{headroom} = V_{DD} - V_{DSmin} - V_x$, where V_X is the voltage drop of current source and $V_{DSmin} = V_{GS} - V_{TH} \propto \sqrt{I_D}$ for a long channel and approaching to $V_{DSmin} = V_{GS} - V_{TH} \propto I_D$ for short channel due to velocity saturation. By appropriate selecting the DC bias condition, the entire linearity performance can be improved.

Taking away the gm stage in proposed mixer, the linearity limitation cause by g_m stage would no more need to be concerned. This approach can eliminate the trade off between linearity and noise figure and may have better linearity comparing to Gilbert cell mixer

Conversion Gain

To simplify the analysis, we could consider the differential pair in the mixer stage as ideal MOS switches which translate the signal to IF and degrade the amplitude to $\frac{2}{\pi}$. From the mixer architecture of Figure 3.23, the input signal amplified by LNA would see the input impedance of $\frac{1}{g_m} \| R_s$ which R_S means the equipment resistance that inductor resonates with parasitic capacitances of MOS. The small signal current that flows to the load impedance can be expressed as $i_d = v_{in} / \left(\frac{1}{g_m} \right)$ and the conversion gain of mixer could be written as

$$CG = 2 g_m R_L \frac{2}{\pi} = \sqrt{K_n I_s} R_L \frac{4}{\pi}$$

where g_m is the trans-conductance of differential pair and R_L is the output resistance of mixer load. Considering finite output resistance of the MOS in the switching core, the load resistance would change to $R_L = r_o \| R_{Load}$. Hence, we could increase the R_L and MOS size of differential pair to enhance the conversion gain. In contrast to the gain enhancement while increasing R_L, the linearity would be obviously reduced due to the headroom reduction caused by $I_S R_L$ and they would be trade-off. Hence we should determinate the appropriate value of R_L, g_m and bias current to achieve the required performance.

Since the differential pair is taken as ideal switch, the LO signal must be an ideal square

wave that could perfectly switch the MOS to turn-on and turn-off. However, the LO signal is a sine-wave not a perfect square wave, thus we need to increase the amplitude to make the MOS to perform better.

Noise Figure

Noise analysis of the mixer is much more complicated due to frequency translation. The noise in the mixer is generated due to the switching quad and load resistance. The noise in the proposed mixer is dominated due to the thermal noise of switching quad and load resistance. The high frequency noise contributed from the current source M_{b2} would be filtered out by the bypass capacitance C_{b1} and would not affect the mixer noise performance. Comparing to conventional Gilbert cell mixer, which is contributed from trans-conductance stage, switching quad and load resistance, this architecture eliminates the noise contribution from trans-conductance stage and greatly reduce the entire noise figure. While the mixing operation takes place, noise associated with the RF band is down converted to the IF band along with the signal, and flicker noise is up converted to the LO band. Since for 60GHz application, we expected to down convert to 50 MHz band, noise contribution due to flicker noise is neglected here.

The noise in the IF frequency at load of mixer would translate to RF frequency by mixing with LO signal. The load of mixer chooses to be resistance instead of PMOS load here to avoid the flicker noise contributed from MOSFET.

The MOSFET in the switching pair contribute noise only when they are in the “on” state. The output noise current produced by a single transistor in the switching core is given in [k-band 77] as:

$$\overline{i_o^2} = 4KT\gamma_n \frac{I_S}{\pi V_{LO}}$$

Where γ_n is channel noise factor for NMOS device and I_S means the bias current for switching

core and V_{LO} is the LO swing that supplies to gate. Though this simple expression is independent of the device width, in reality the noise due to this switching core increases with the increase of the device size [41]. As the LO generates several higher harmonics along with the fundamental frequency, those higher harmonics down-convert noise in the incoming input signal to IF band as shown in Figure 3.24. Thus the total output noise voltage of the mixer can be expressed as:

Total noise voltage $\overline{V_{o,total}^2} = V_{switching\ noise} + V_{Load} = 4KT\gamma_n \frac{Is}{\pi V_{LO}} R_L^2 + \overline{V_{n,L}^2}$

where noise due to the load resistance is:

$$\overline{V_{n,L}^2} = 8KTR_L$$

Since the total mixer output noise is obtained, he noise figure can further be acquired by

$$NF_{Mixer} = 10log\frac{\overline{V_o^2}}{CG^2 4KTR_s}$$
$$= 10log[\overline{V_o^2} / 4KTR_S (g_m R_L \frac{2}{\pi})^2]$$

Generally speaking, noise figure would be larger than this if flicker noise and substrate noise are considered.

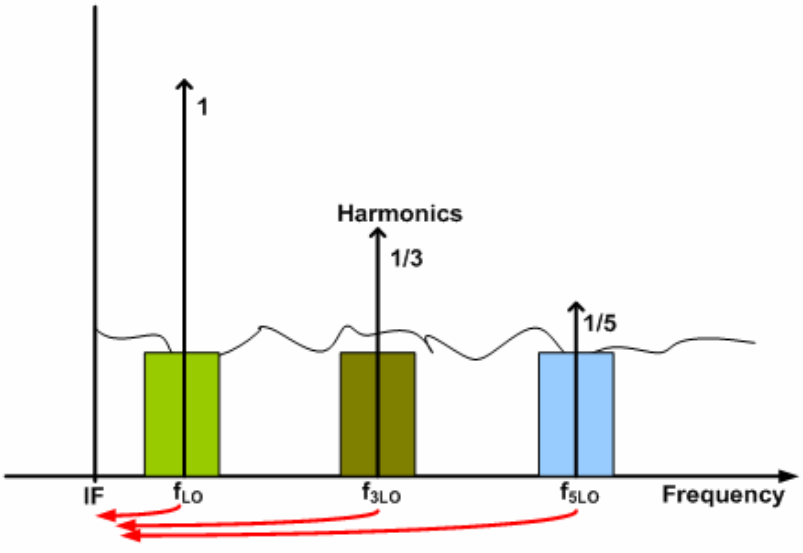


Figure 3.24 Frequency translation of white noise from mixer input MOS

3.3.2 Circuit Realization of Mixer

Figure 3.25 is the complete schematic of the proposed mixer composed of core circuit and output buffer pair. The CMOS active mixer is realized by differential pair with a current source that supply stable DC current to the core circuit of mixer. The LNA output current enters the source of the differential MOS pair $M_{1,2}$.

To increase the mixer linearity by alleviating the output signal headroom, the current mode interface between the LNA and mixer presented in [6] is used in this study. In a conventional architecture as shown in Figure 3.26, the LNA output voltage is fed to the g_m stage of the mixer and transfer to the current. This architecture leads to less degree of freedom when the noise performance and the dc biasing margins are to be optimized. To achieve better thermal noise performance and higher g_m value from the input transistor, a high biasing current may be required. However, the flicker noise of the mixing transistors is a dominant source of noise, which can be reduced by reducing the bias current of the mixer [4]. These are conflicting requirements. Moreover, the gate overdrive voltage of the input transistor needs to be large to get better input linearity. For low voltage designs, there is limited headroom to allow large enough voltage in this circuit.

The interface between LNA and mixer is shown in Figure 3.27, it avoids these limitations and the complete scheme of the proposed mixer is shown in Figure 3.25. The trans-conductance stage which converts the voltage signal to current signal in a conventional Gilbert cell mixer can be removed. The RF current is coupled from the output of the LNA through the dc blocking capacitance and fed into the source of the differential pair to mix with the LO signals. The separate bias currents are provides for the LNA and mixer that allows independent optimization for the noise in the two blocks. Because the proposed mixer operates on a switched current principle, the MOS M_1 and M_2 are turned on and off by the differential LO signal and each time the switches change position in tandem, the direction of

the small signal current through the load resistor reverse. The headroom requirements are also relaxed here because the tail current source in the mixer does not influence the linearity, and hence can have much smaller gate-overdrive.

A current mirror implemented by $M_{b1,b2}$ generates the desired dc current to the differential pair. To avoid the noise contribution from the current source, a large bypass capacitance C_{b1} is applied to filter out the flicker noise. The inductor L_S is used to resonate with parasitic capacitance at the source terminal of $M_{1,2}$ at the desired frequency. This inductor could reduce the signal loss caused by the parasitic capacitance The capacitance $C_{p1,p2}$ and $R_{L1,L2}$ function as a low pass filter to extract the undesired signal. Due to the low-pass characteristics of the filter, the LO to IF isolation can be markedly improved. To reduce the IF signal loss resulting from the low pass filter at the output of the mixer, the pole of the filter needs to be selected appropriately. For measurement considerations, MOS M_3 and M_4 are used as unit-gain buffers to drive the 50-ohm measurement system.

In comparison with a conventional mixer, the proposed mixer has the following advantages. First, the noise figure is better due to the absence of the noise resulting from the input stage in a conventional mixer. Second, the supply current only needs to provide the mixing stage $M_{1,2}$ in this case and the dc current can be reduced to improve the noise performance even more. Finally, an improvement in linearity is expected due to the enhancement of headroom and input stage that dominates the linearity of a conventional structure. The resistance $R_{L1,L2}$ enhancement results in an increase in conversion gain but a decrease in the DC voltage at the output nodes. In short, there is a trade-off between conversion gain and linearity.

To improve the linearity of entire receiver, we desire the circuit to have the linearity as large as possible while approaching acceptable value of gain. As mentioned above, the headroom is one of the most importance parameter that effecting the entire linearity. To

improve the headroom, considering the V_{DSsat} of M_{b2} is about 175 mV, we designed the V_{DS} to be 225 mV which is minimum value that ensure the MOS to operate in saturation region and provide fixed DC current. Because of dc drop causing by supply current and R_{Load} ($I_S R_{Load}$) is another issue may expense the headroom, we degrade the dc current to about 0.7 mA to enhance the linearity.

An increase in $R_{L1,L2}$ results in an increase in conversion gain but a decrease in the DC voltage at the output nodes. In short, there is a trade-off between conversion gain and linearity. The detail device parameters of proposed mixer are list in Table 3.3.

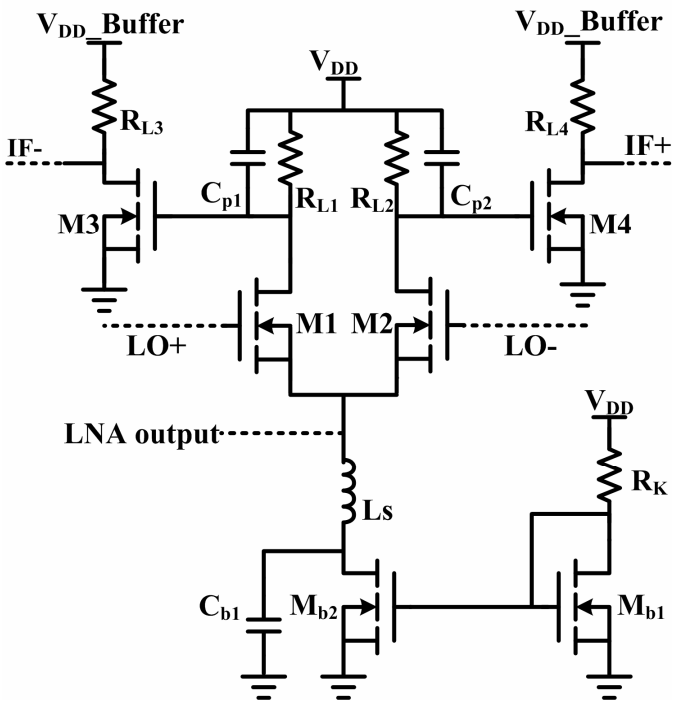


Figure 3.25 The circuit diagram of the proposed down-conversion mixer

Table 3.5 Device parameters of the down-conversion mixer circuit

$M_{1,2}$	16 um / 0.13 um	$R_{L1,2}$	1.1 kohm
$M_{3,4}$	36 um / 0.13 um	R_K	5 kohm
M_{b1}	4 um / 0.35 um	$C_{p1,2}$	MIM 8um x 8um
M_{b2}	24 um / 0.35 um	$C_{p3,4}$	MIM 20um x 20um
L_S	Tline L=200 pH	C_{b1}	> 5 pH
V_{DD}	1.2 V		

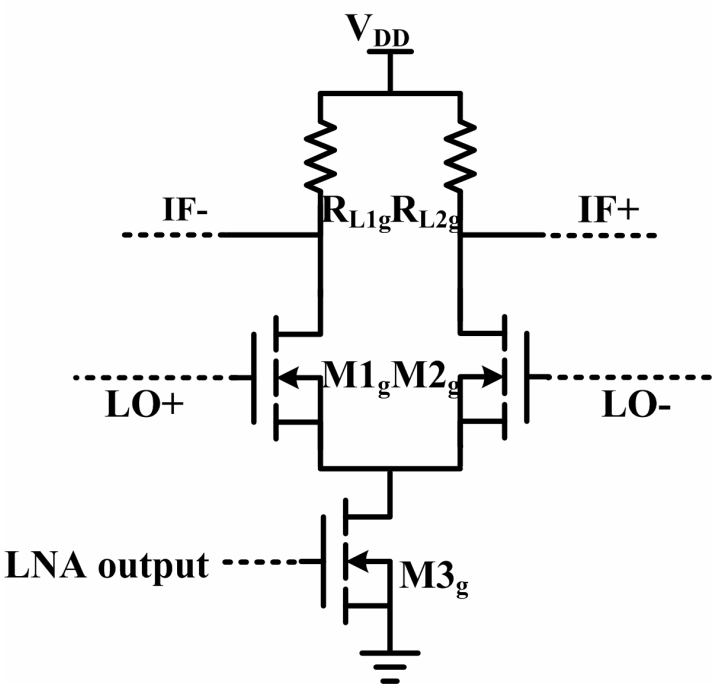


Figure 3.26 The circuit diagram of the conventional Gilbert cell mixer

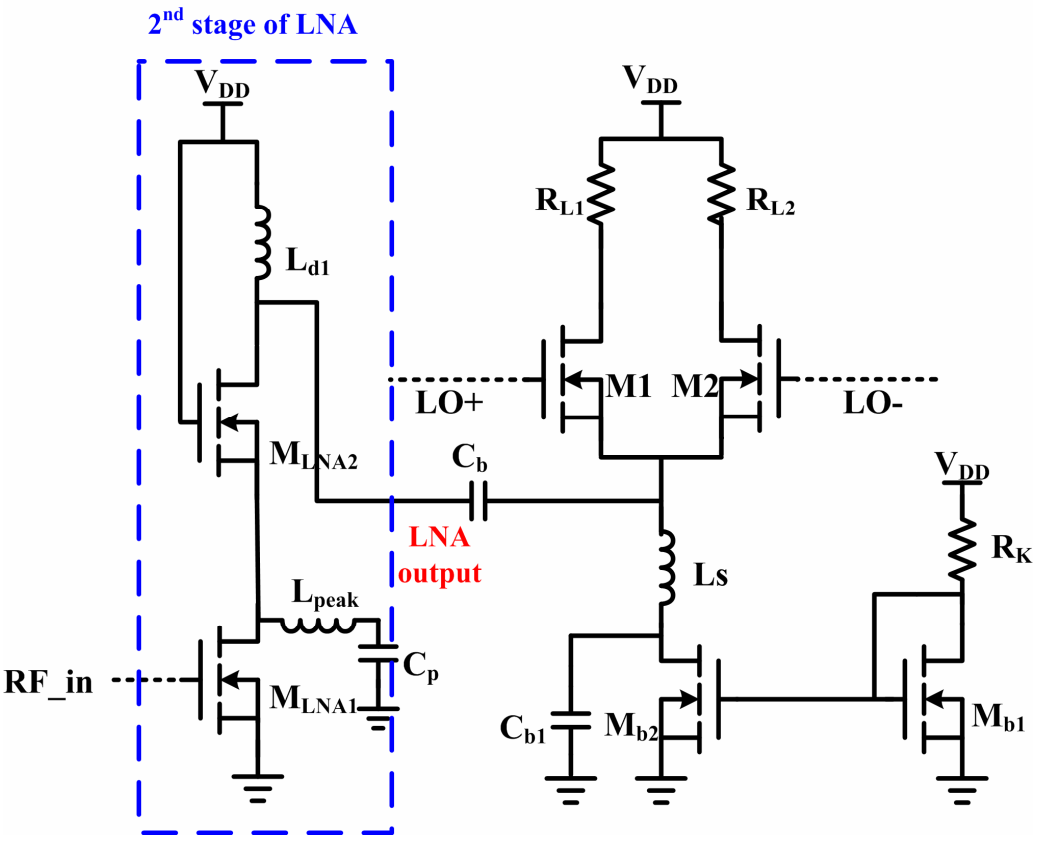


Figure 3.27 The circuit diagram of the proposed LNA/mixer interface

3.3.3 Simulation Results of Mixer

The performance of proposed mixer is simulated under the circumstance of 50-ohm input and output matching to compete with LNA output and measurement instrument. Figure 3.28 shows the simulated NF of the down-conversion mixer, the IF is selected to 50 mega hertz by varying input RF frequency from 50 GHz to 70 GHz. As can be shown, the simulated NF is lower than 9.5 dB across unlicensed band and the minimum NF could achieve lower than 8.5 dB. This noise performance is much better than conventional Gilbert cell mixer and be modified Gilbert cell mixer [4]. The circuit in the receiver chain exhibits conversion gain of 12.5 dB as shown in Figure 3.29 while the mixer core draws 0.9 mA. At last, in Figure 3.30, the simulated P_{1dB} is expressed which is about -11 dBm and a summary of the down-conversion mixer is listed in Table 3.4.

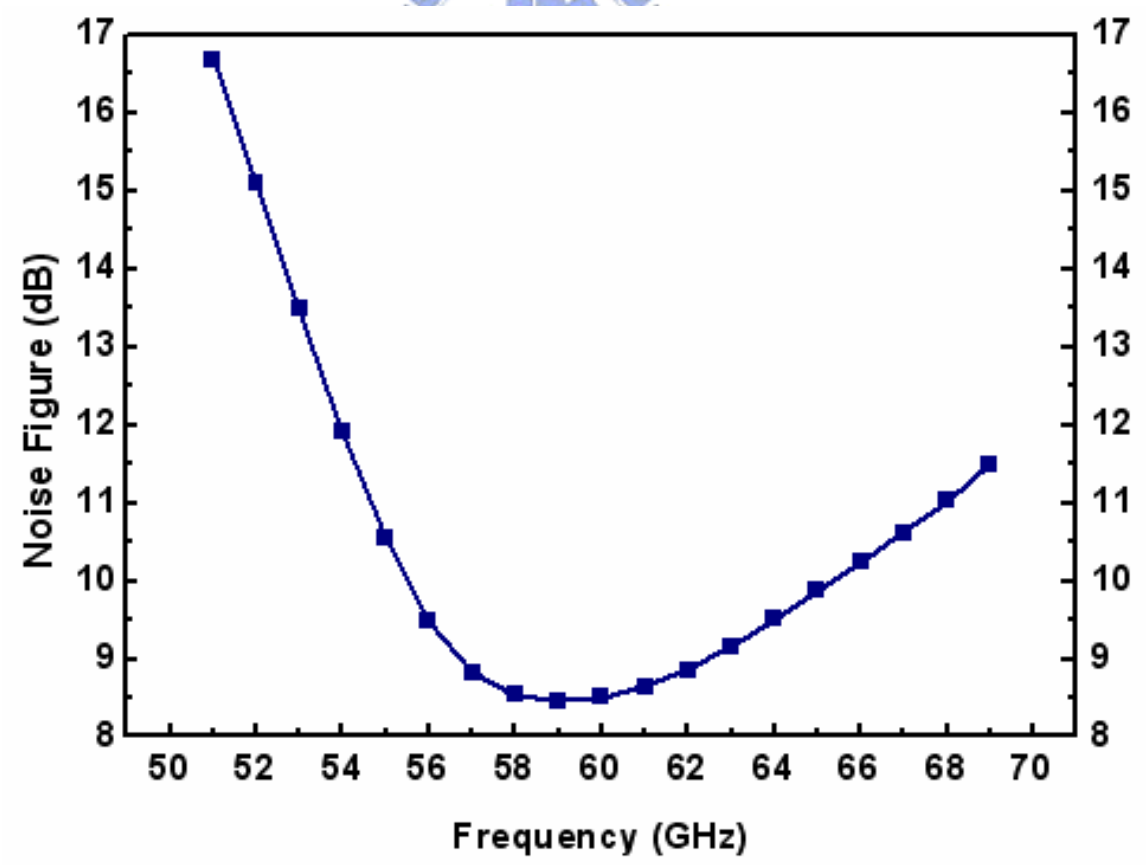


Figure 3.28 Simulated noise figure of the proposed mixer

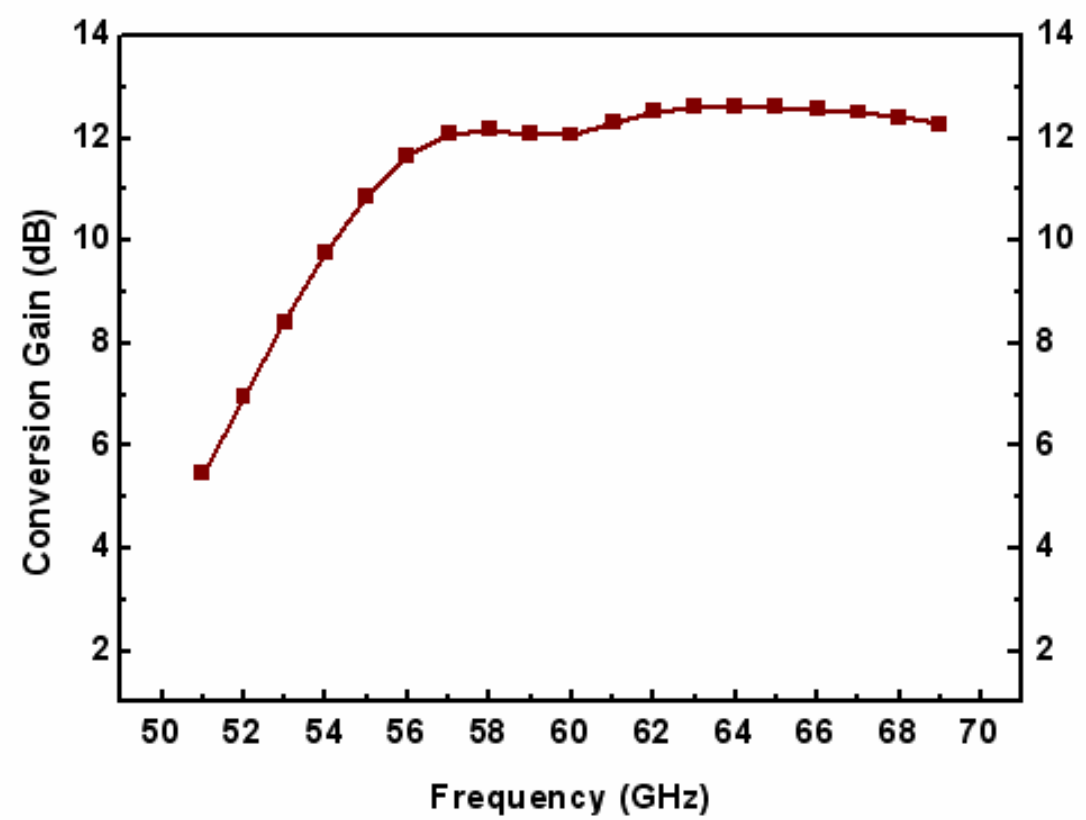


Figure 3.29 Simulated conversion gain of the proposed mixer

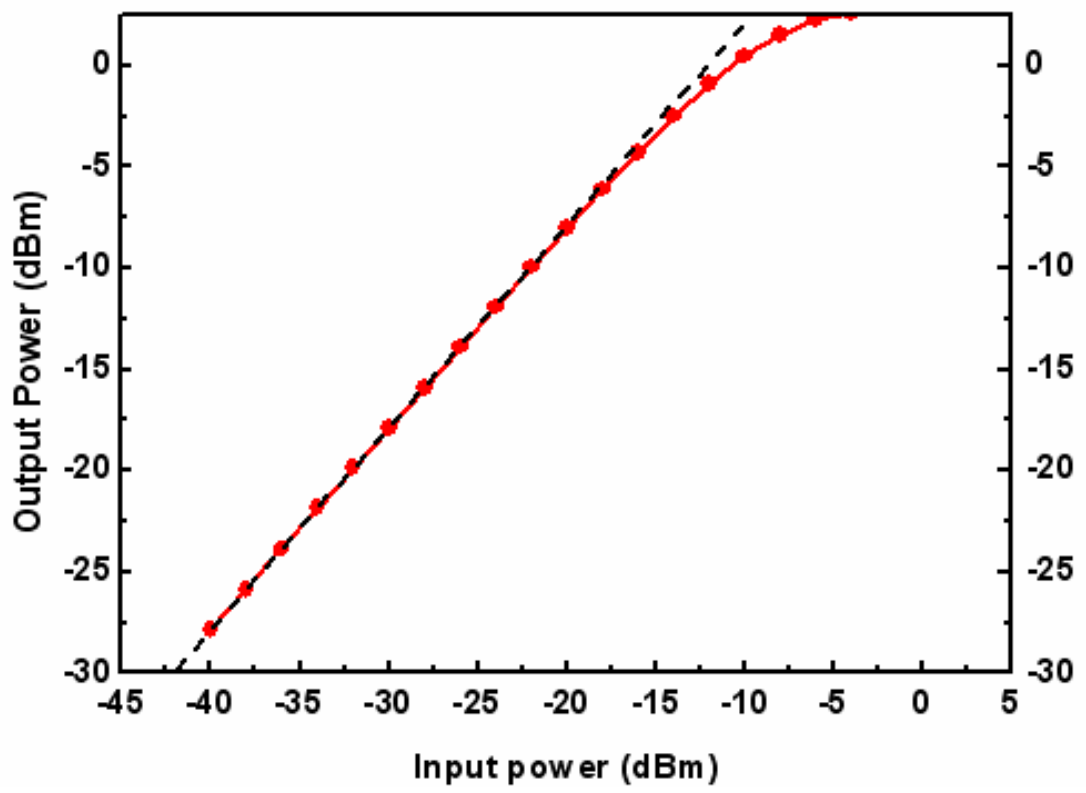


Figure 3.30 Simulated input 1dB compression point of the proposed mixer

Table 3.6 Post simulation summary of the proposed mixer

Technology	0.13-um CMOS 1P8M
Frequency	60 GHz
3dB Band-width	54 ~ 76 GHz
Gain	12.5 dB
NF	8.5 dB
P_{1dB}	-11 dBm
Power Dissipation	0.8 mW
Supply Voltage	1.2 V

3.4 Simulation Results of Receiver Front-end

The entire receiver consists of the foregoing circuit blocks: LNA, down-conversion mixer, frequency tripler and output buffers. Moreover, this design is aimed at on-wafer measurement; the bonding wire effects is out of concern and parasitic capacitance resulting form input GSG pad (60*60 um^2 with pitch of 100 um) is taken into concern that is simulated to be around 20 fF within the operating frequency; the input and output impedance is matched to 50 ohm for measurement consideration. To avoid the voltage signal division caused by blocking capacitance and for supply pins consideration, the gate bias of the differential pair in mixer is realized by dc current following through the preceding stage in tripler resistance instead of re-biasing which uses dc-blocking capacitance and additional bias pin.

The simulation results are expressed as IF signal at 50 MHz and frequency between 57 GHz to 64 GHz which we are interested in. Figure 3.31 plots the simulated power gain and Figure 3.32 plots simulated noise figure of entire receiver front-end. The power gain is higher than 22.5 dB with a peak gain of 24.4 dB at 61 GHz and the noise figure varies from 7.8 dB to 8.2 dB where the minimum noise could also be achieved at 61 GHz. The linearity P_{1dB} is illustrated in Figure 3.33 across the unlicensed band. The linearity performance of P_{1dB} is between -21.4 dBm to -22.8 dBm according to gain variation. The linearity of the entire

receiver is limited by mixer circuit because the LNA already provides some gain and enhances the input signal of the mixer.

The input LO power of frequency tripler would extremely influence the entire performance. As the input power level of fundamental LO signal increase, the frequency tripler could result to higher output power and lead the switching pair in mixer operates more resemble to ideal switch. Figure 3.34 and Figure 3.35 are plots of the simulated output power and noise figure versus fundamental LO input power from -10 dBm to 10 dBm at 60 GHz. The figure shows that from -10 to 2 dBm, the conversion gain increases with increasing of input power and tends to be saturated as the power level above 4 dBm. Finally, the output transition waveform is shown in Figure 3.36, and Table 3.7 and Table 3.8 list the summary of the post-simulation results with process and temperature variations. At last, performances are comparing with recently published papers which are listed in Table 3.9.

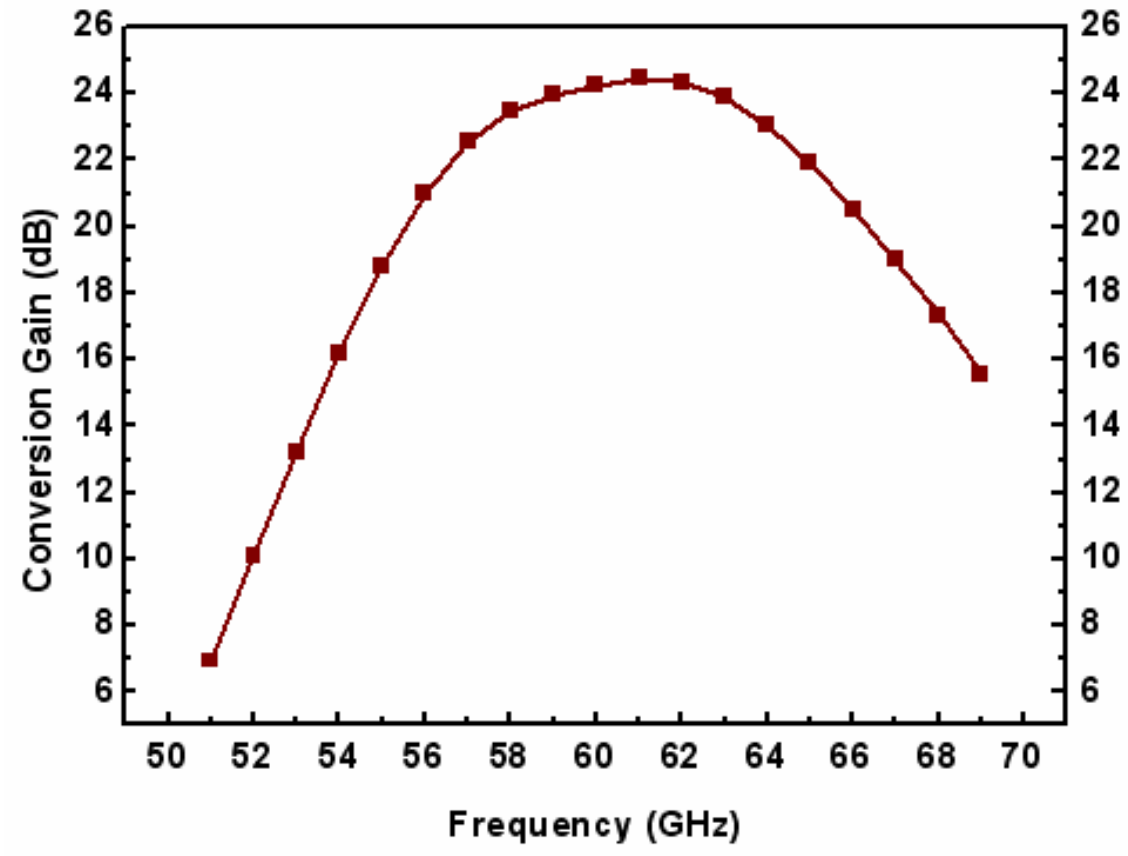


Figure 3.31 Simulated conversion gain of the direct-conversion receiver

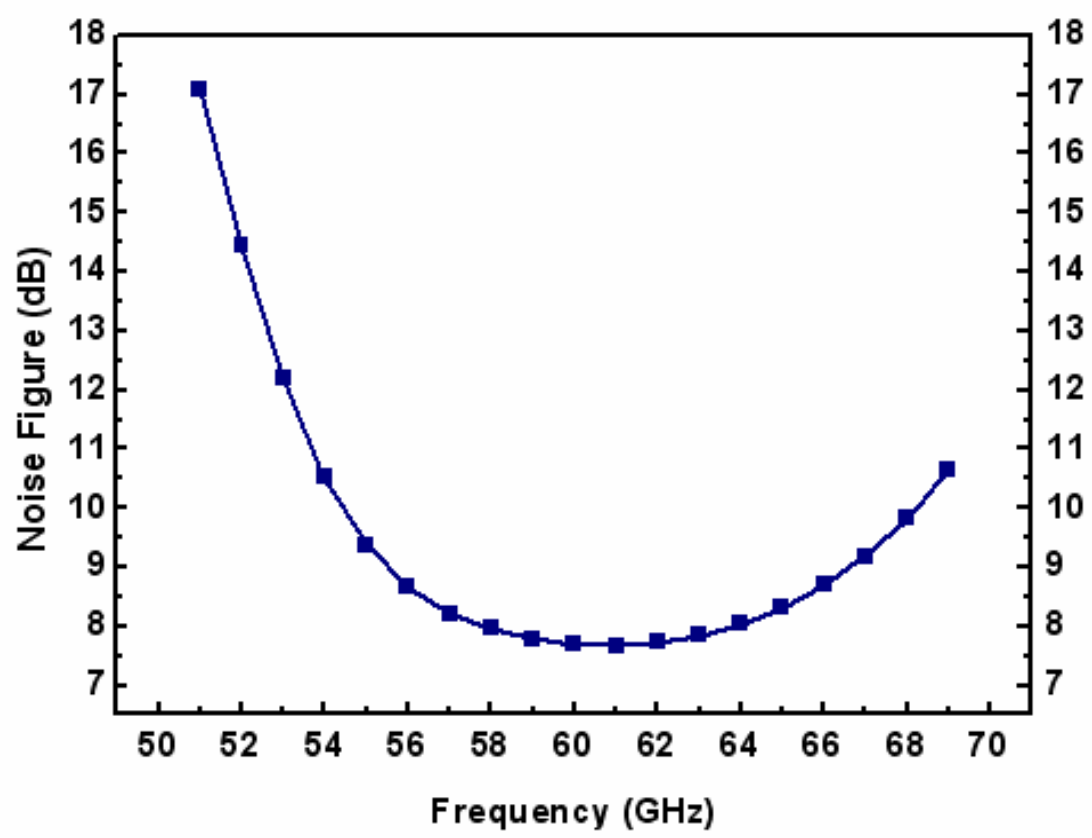


Figure 3.32 Simulated noise performance of the direct-conversion receiver

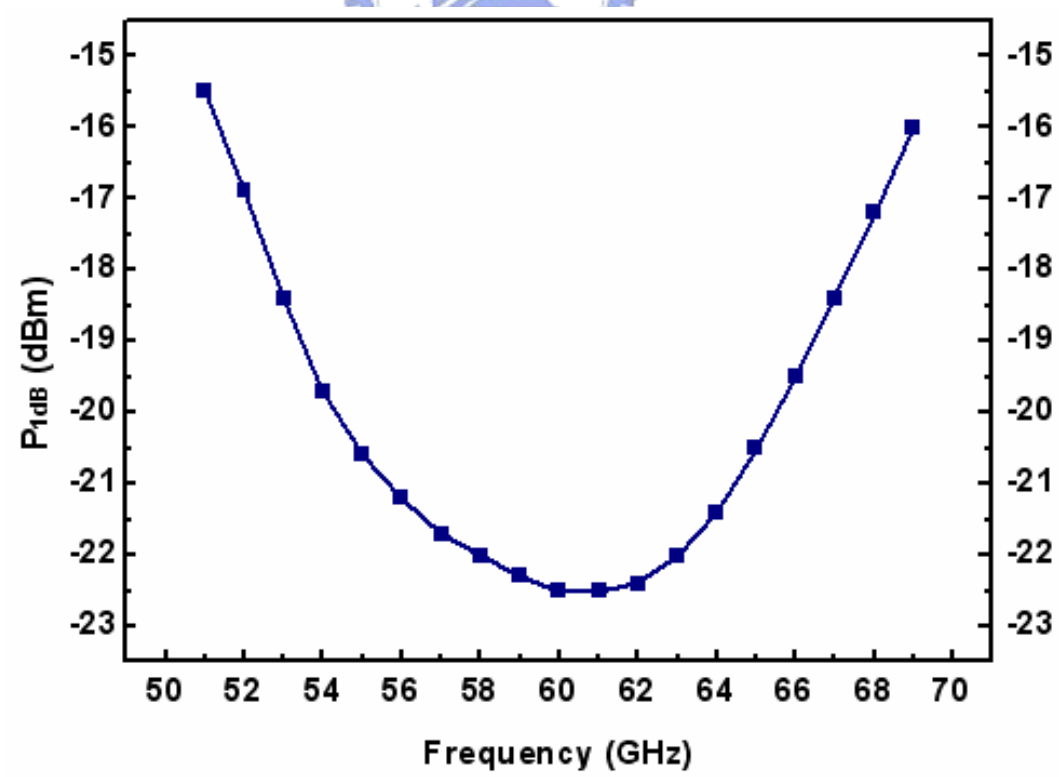


Figure 3.33 Simulated linearity and P_{1dB} of the direct-conversion receiver

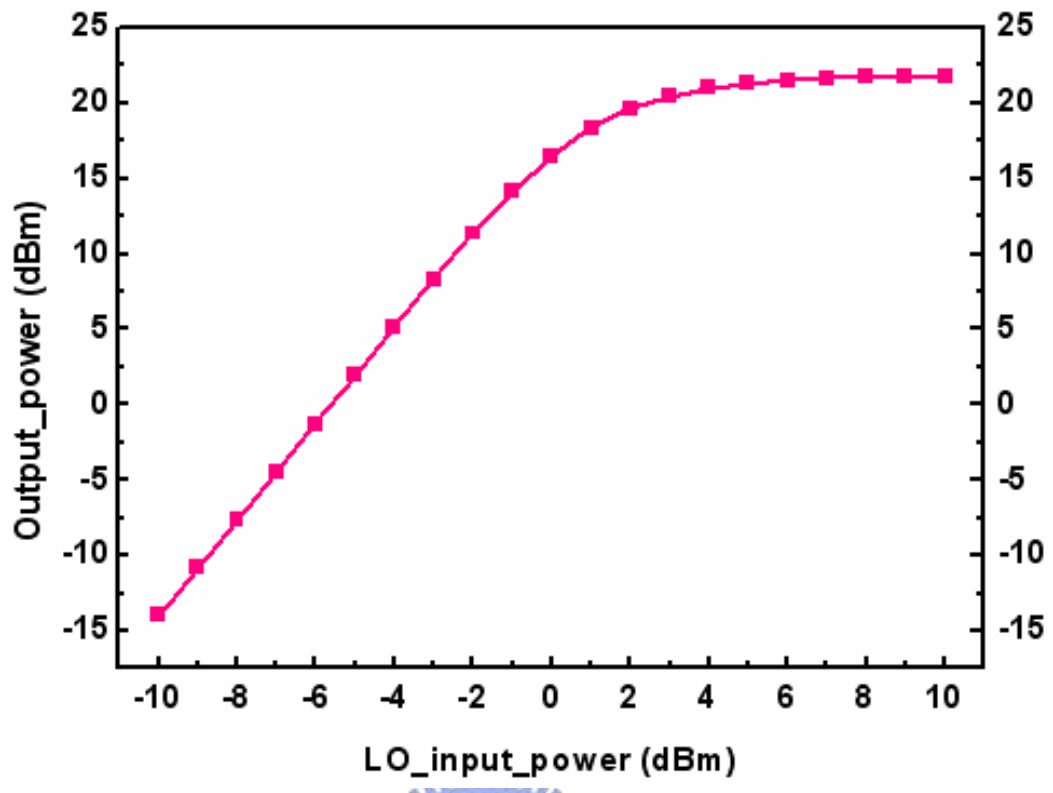


Figure 3.34 Simulated output power as a function of LO input power at 60GHz

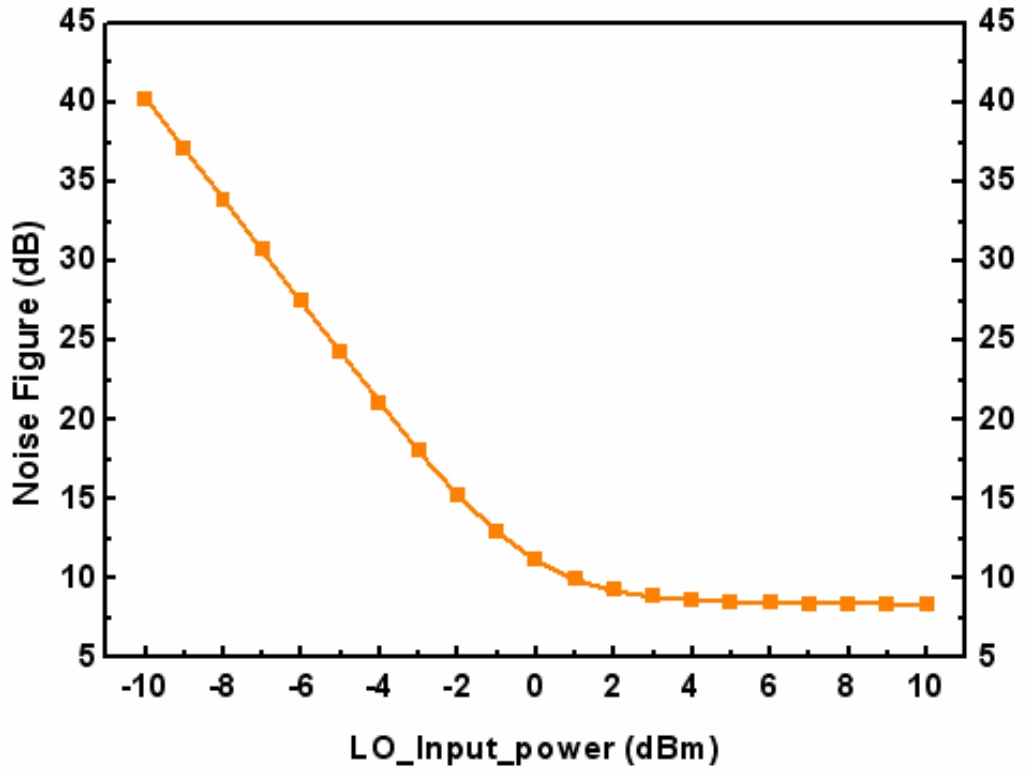


Figure 3.35 Simulated noise figure as a function of LO input power at 60GHz

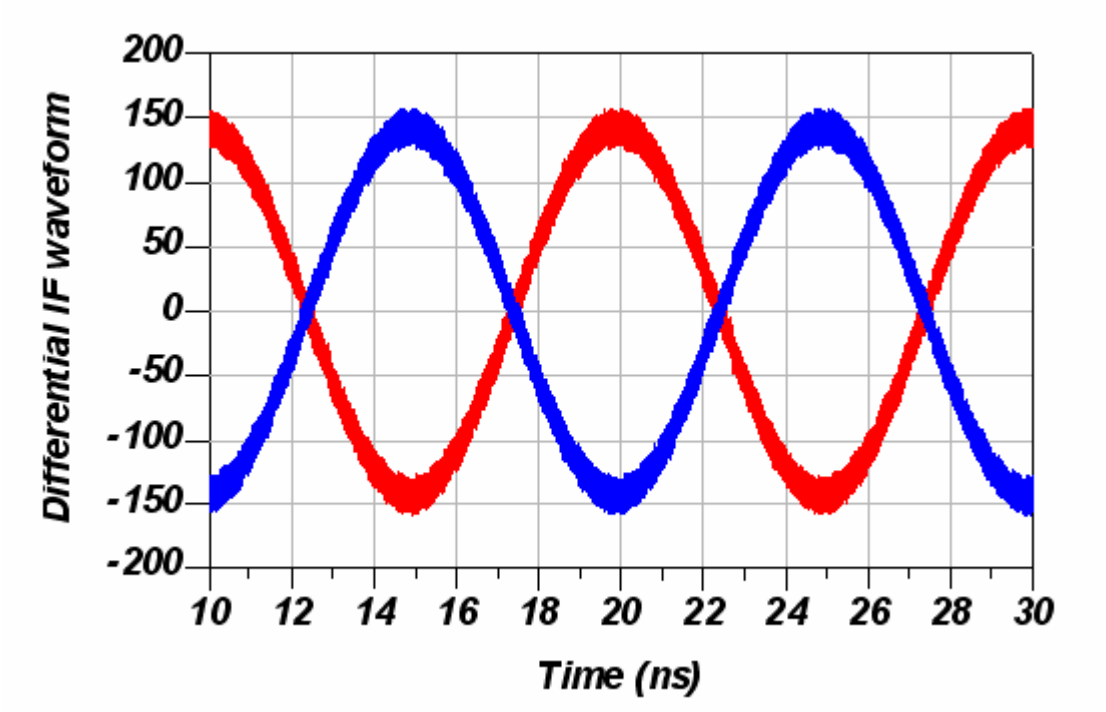


Figure 3.36 Differential IF output waveform

Table 3.7 Post simulation summary of the receiver front-end with corner

Post-Simulation	FF	TT	SS
Frequency [GHz]	56~65	56.3~65.5	56.9~65.3
Rx Gain [dB]	25.6	24.4	22.9
NF [dB]	7.5	7.7	8.3
P1dB [dBm]	-23.9	-22.8	-20.9
LNA Gain [dB]	12.5	12	10.1
LNA NF [dB]	4.1	4.4	5.3
LNA Power [mW]	7.2	4.8	3
Mixer Gain [dB]	10.8	12	12.6
Mixer NF [dB]	8.4	8.8	10.6
Mixer Power [mW]	1.2	0.95	0.8
Rx Power [mW]	20.6	14.4	10.3
S11 [dB]	< -15	< -15	<-15
Supply Voltage [V]	1.2	1.2	1.2

Table 3.8 Post simulation summary of the receiver front-end with temperature variation

Post-Simulation	0	25	100
Frequency [GHz]	56.1~65.6	56.3~65.5	57~64.3
Rx Gain [dB]	25.3	24.4	19.8
NF [dB]	7.4	7.7	9.2
P1dB [dBm]	-22.4	-22.8	-22.9
LNA Gain [dB]	12.5	12	10.1
LNA NF [dB]	4.1	4.4	5.3
LNA Power [mW]	4.6	4.8	5.4
Mixer Gain [dB]	12.8	12.4	9.7
Mixer NF [dB]	8.4	8.8	10.6
Mixer Power [mW]	0.94	0.95	1
Rx Power [mW]	12.8	14.4	15.1
S11 [dB]	< -15	< -15	<-15
Supply Voltage [V]	1.2	1.2	1.2

Table 3.9 Post simulation summary and compassion of the receiver front-end

Reference	[4]	[6]	This work
Frequency (GHz)	57.5~64	57~63	56-65.5
LNA Gain (dB)	13.2	12	12
LNA NF (dB)	4.6~5.4	8.8	4.3~4.7
LNA Power (mW)	4.8	43.2	4.8
Mixer Gain (dB)	12	-2	12.4
Mixer NF (dB)	18.5~19.5	13.8	8.8~9.5
Mixer Power (dB)	1.1	2.4	0.95
Receiver Gain(dB)	28*	11.8	24.5
Receiver NF(dB)	12.5	10.4	7.7
$P_{1dB\text{-}in}$(dBm)	-22.5	-15.8	-22.8
IF Amplifier	Yes	Yes	No
Technology	0.13-um CMOS	0.13-um CMOS	0.13-um CMOS

Chapter 4
Experiment Results

The proposed direct-conversion receiver for 60-GHz application and a 70-GHz LNA is designed and fabricated using TSMC 0.13-um CMOS process. This chapter presenting the chip layout, test environment, and experiment results. Measured performance is compared with post-simulation results and discussion which is made for further study.

4.1 Layout Description

This receiver chip is fabricated using TSMC 0.13-um CMOS 1P8M copper process with eight metal layers, in which ultra thick metals, seventh and eighth layers, are implemented for mixed signal / RF applications. By using this technology, an inductor with high quality factor and lower parasitic capacitance can be implemented. Besides, all NMOS devices are arranged with deep n-well device which allows the connection of source and body terminals to avoid body effect. Dummy gates and dummy resistors are equipped at the margin of every MOS device to cope with process variation. The MIM capacitor in this technology provides two kinds of arrangements: with or without under ground metal shielding. The former has high immunity to substrate noise and the latter presents less parasitic capacitance. Meanwhile, the spaces between the transmission lines are more than three times that of the line-width with other transmission lines to prevent mutual inductance. Moreover, we comprise ground plane metal to avoid the substrate induced loss.

The chip is designed for on-wafer probing measurements. Hence all the pad pitches must be designed to compete with the RF and DC probes. Moreover, the pad sizes are designed as small as possible to reduce the parasitic capacitance that may degrade the performance. The LNA and receiver layouts are shown in Figure 4.1 and Figure 4.2, respectively.

In LNA layout, due to the small core circuit of the LNA, the chip area is limited by the DC pads and RF I/O pads. This cause the signal line much longer than required and the performance may a little bit degrade. To realize the more accurate inductance model of the transmission lines in simulation, the EM simulation of the each micro-strip transmission lines and interconnections between stages are simulated by using EM simulator, Ansoft HFSS. Moreover, to stabilize the DC supply to the circuit, large amount of the bypass capacitances are also implemented by using the metal sandwich capacitance ($M_1M_3M_5M_7$ for ground and $M_2M_4M_6M_8$ for DC bias). By applying metal sandwich capacitance, we can implement the bypass capacitance large than 10 pF on chip. The resulting chip size is 0.67x0.57 mm^2, Inclusive of all I/O pads and dummy metal.

In receiver design, symmetric layout is important to keep balanced of differential mixer LO input and IF output signals to reduce the mismatch. Because this chip requires six power supplies to supply the LNA, mixer and frequency tripler circuits, the 6P DC probe with 150-um pitch must be applied here. This limits the chip length because large space between six pads must be required. Furthermore, since both of the LO input and IF output are the differential, the GSGSG probes is also applied here and it also requires 150-um pitch between each pads. The chip width is limited by GSGSG pads and the area is much larger than core circuit. In order to make the signal path as short as possible to reduce the parasitic capacitance and induced inductance, the RF GSG pad and LO GSGSG pad are placed inside the whole chip instead of its fringe. This makes the signal path length reduction of at least 400 um and can reduce the non-ideal interconnection effects. The entire chip area is 1.2 mm^2.

Besides the DC bypass capacitance, the receiver circuit also requires some bypass capacitance to provide the ac ground node to the circuit. However, this capacitance is much more critical than DC bypass capacitance because it will dominate the circuit performance. Hence, we draw the bypass capacitance as large as possible to more close to ac ground point. From simulation results, each of them can achieve larger than 5 pF.

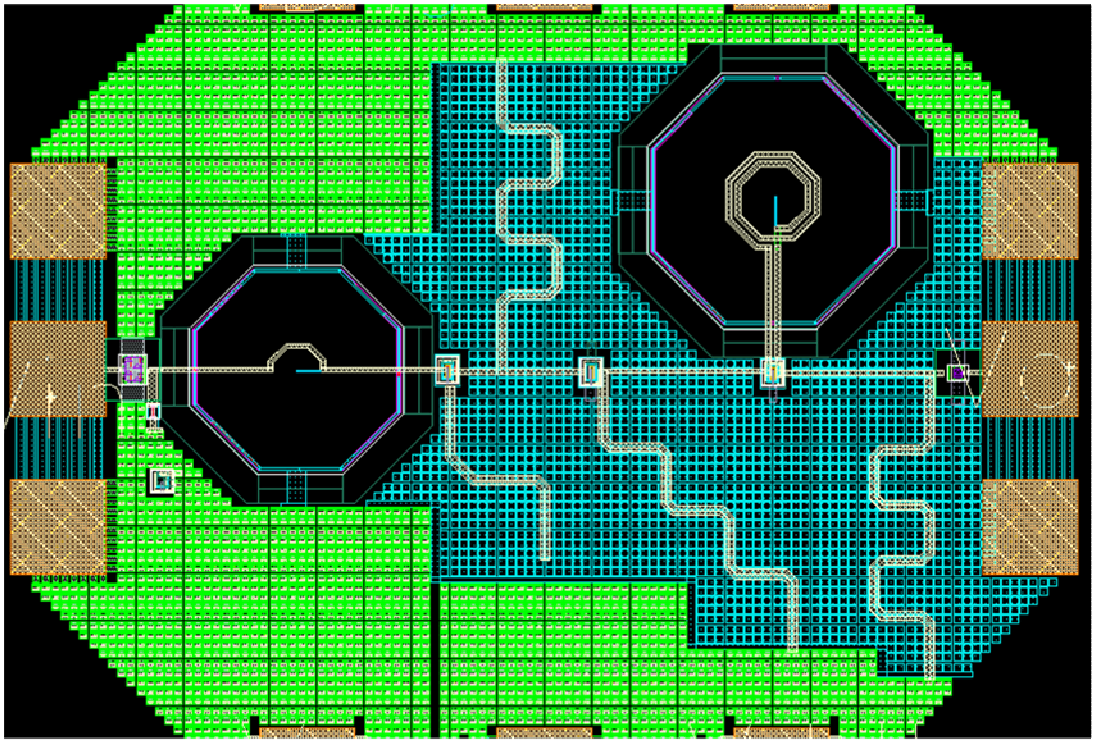


Figure 4.1 The 70-GHz LNA layout view.

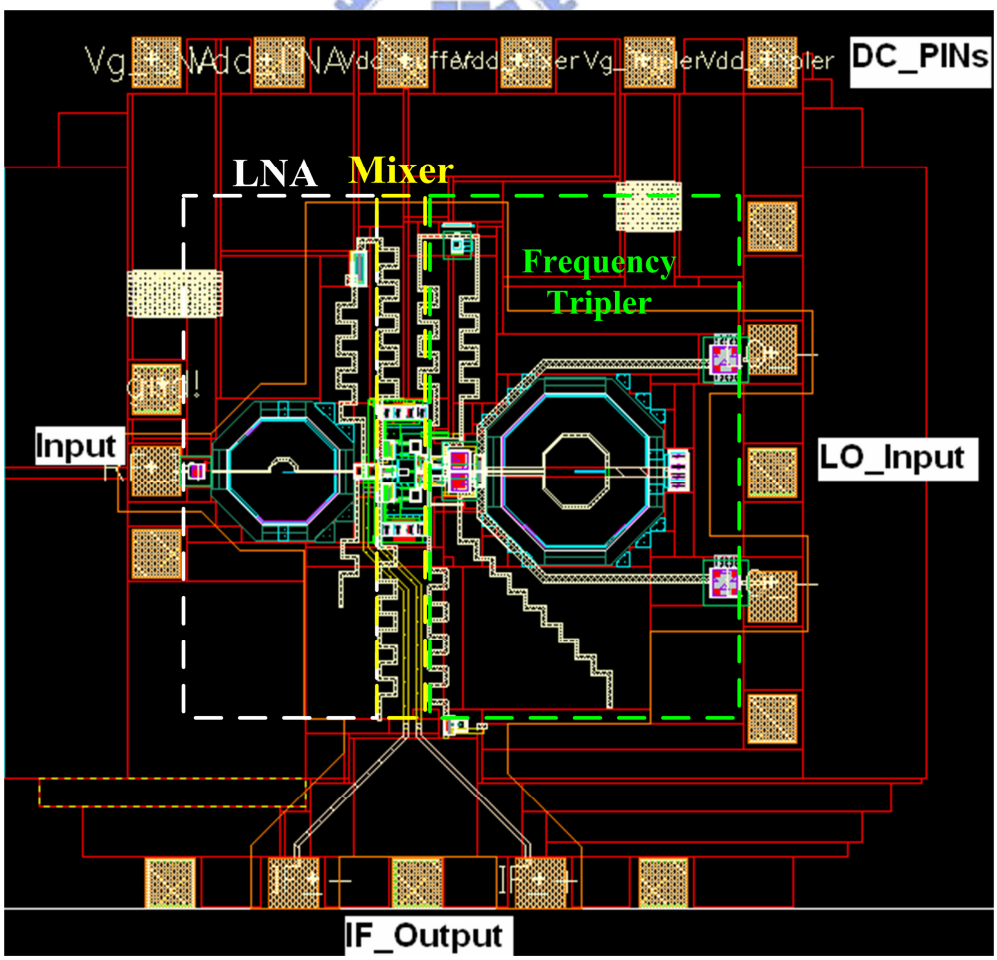


Figure 4.2 The 60-GHz receiver layout view.

4.2 Measurement Consideration and Setup

The proposed 70-GHz LNA and 60-GHz receiver chips have been fabricated and measured to verify the circuit performance. Some of the circuit parameters are measured at our laboratory and the others are measured at National Nano Device Laboratories (NDL) or National Chip Implement Center (CIC) due to instrument requirements. In the following, we introduce the measurement consideration and setup of the two chips respectively.

4.3.1 Measurement of 70-GHz Low Noise Amplifier

The LNA chip is bared die and measured directly on-wafer. The chip microphotograph is shown in Figure 4.3 and the measuring environments are shown in Figure 4.4 and Figure 4.5. The S-parameters of the circuit can be measured at NDL using HP 8510XF network analyzer to obtain the I/O return losses, power gain and reverse isolation characteristics. Since the minimum input power of the network analyzer is -15 dBm and excess the simulated 1-dB compression point of the LNA, the measured power gain may be underestimated. So, the power gain is re-measured to obtain the accurate value before gain compression.

The circuit power gain is re-measured by using the signal generator of HP E8257D cascading with V-band source module to up-convert the input signal to the desired frequency. The output signal is down-converted and observed the output spectrum by using HP 8563E spectrum analyzer. The RF I/O pads are directly probed with CASCADE ACP-50-GSG-100 probes. All of the DC supplies are implemented on chip and DC pads are probed using 150-pitch PGP DC probes. In addition, by using the attenuator, we can vary the power of input signal and observe the input 1dB compression point. To compensate the signal power loss in the input and output path in the frequency of interest must be measured firstly. After compensate the power loss caused by cables and probes, the actual power gain of the LNA can be calculated.

So far, there are two approaches to measure the noise figure and can give nearly the same noise figure results [4]. One is applying a noise source and obtaining by a noise analyzer. But a high frequency noise source and noise analyzer is required in this case. The second approach is obtaining the difference between the input and output SNRs (all in dB). Nevertheless, this method only can apply in a high gain circuit otherwise the output SNR will be affected by instrument. Moreover, the noise contribution due to V-band source module and down-conversion mixer is another concern. Since the power gain of the LNA is not high enough, the SNR ratio method may not a good choice.

So far, we do not have enough instruments to exact measure the noise figure and the IIP3 performance. Besides the noise figure instruments, the IIP3 measurement requires two V-band source modules and two attenuators to generate the desired input power. These instruments are under setup in our laboratory and can be measured in the future. All of instrument setup block diagrams are depicted in Figure 4.6 ~ Figure 4.8.

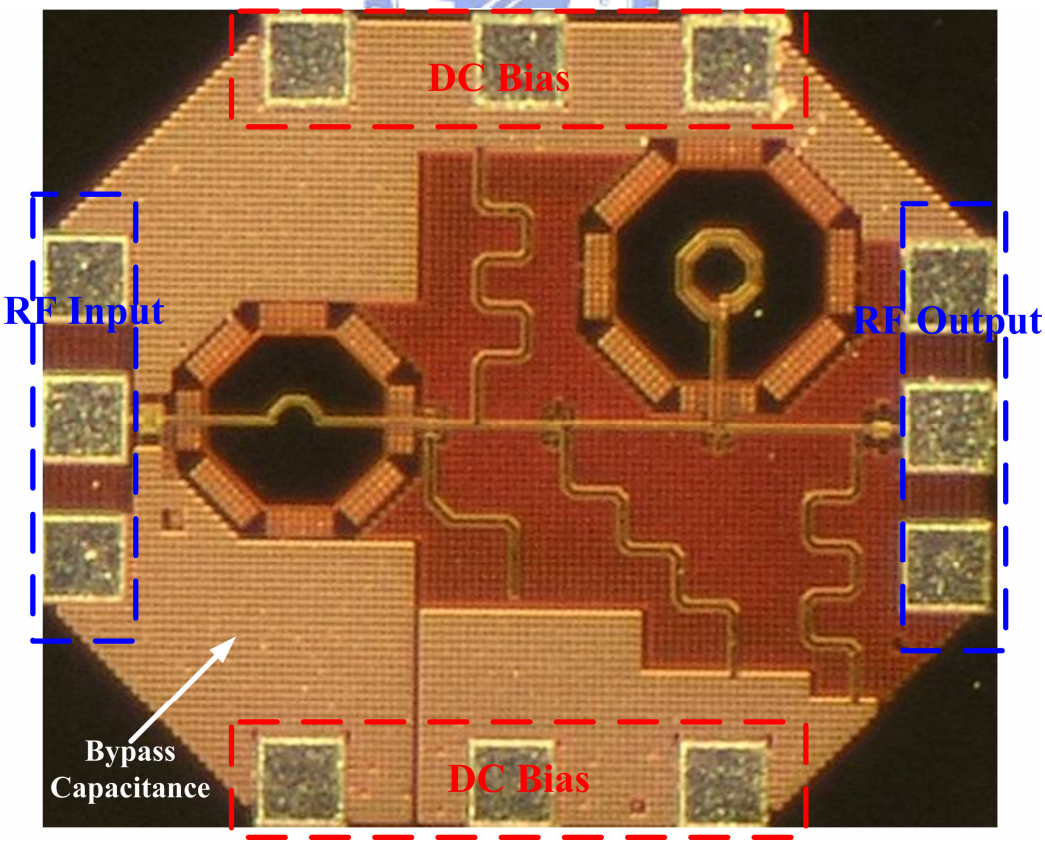


Figure 4.3 Chip microphotograph of the LNA

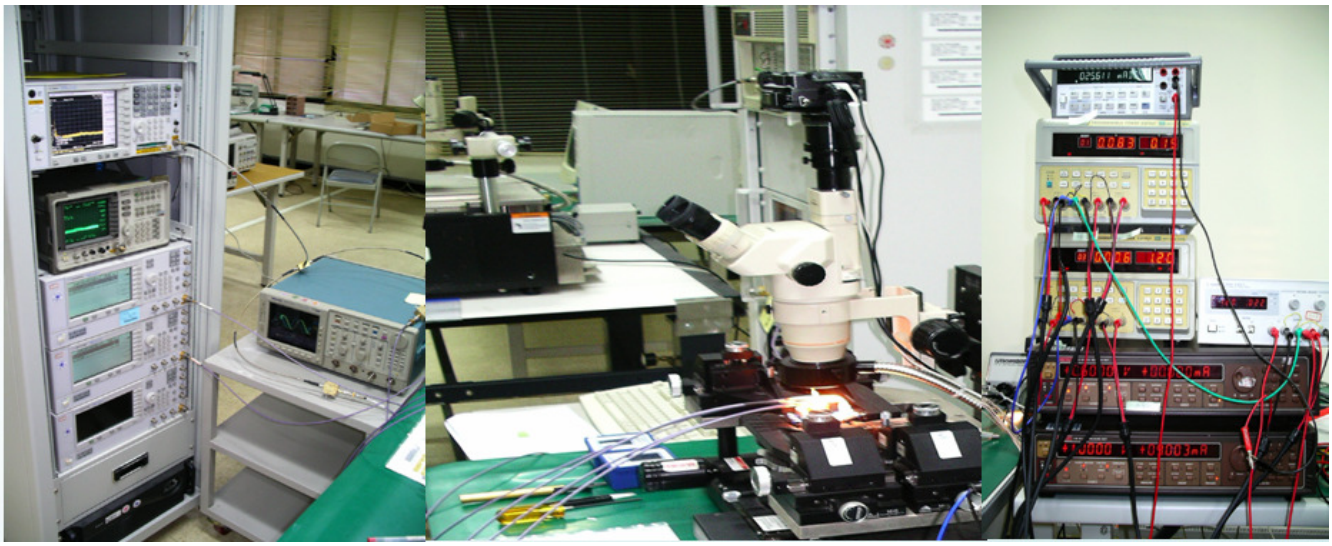


Figure 4.4 Measuring environment at laboratory

Figure 4.5 Measuring environment at NDL

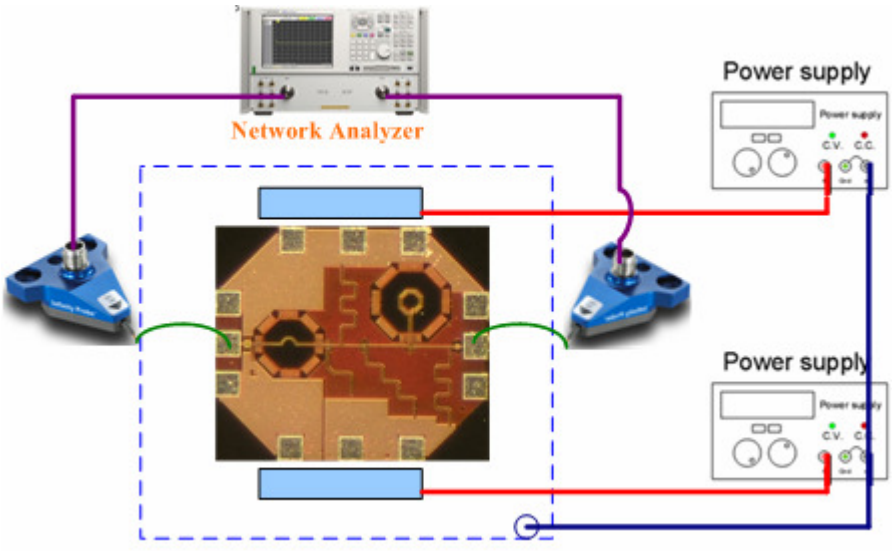


Figure 4.6 Instrument setup for LNA S-parameter analysis

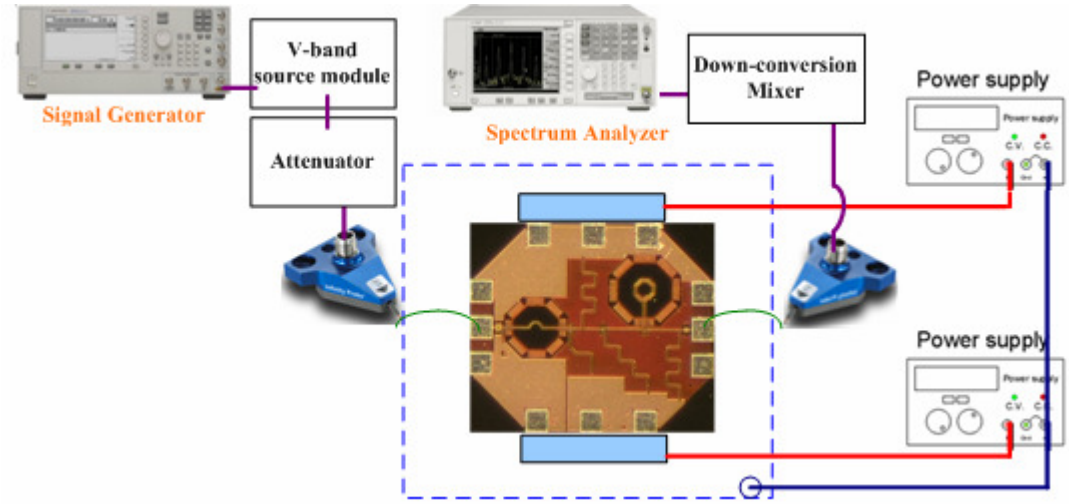


Figure 4.7 Instrument setup for LNA spectrum analysis

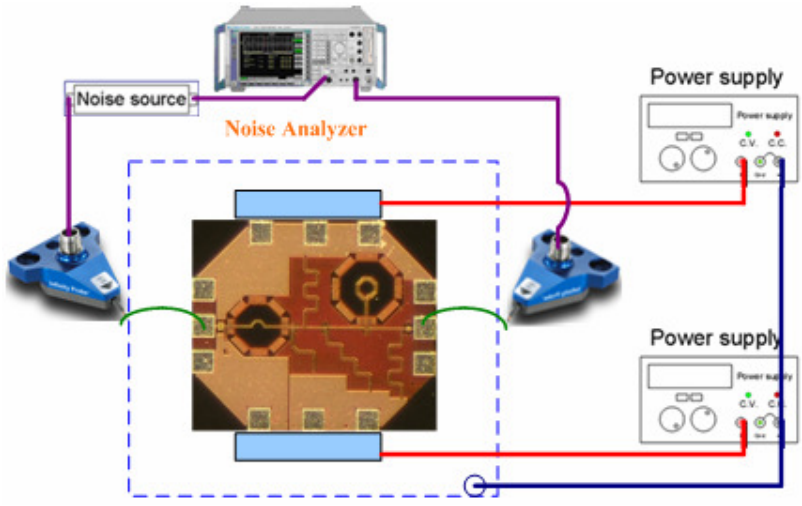


Figure 4.8 Instrument setup for LNA noise analysis

4.3.2 Measurement of 60-GHz Receiver

The fabricated chip is measured on-wafer using high frequency probes. The chip microphotograph is shown in Figure 4.9 and the measuring environment is the same as previous The S-parameters of receiver can be measured at NDL using HP 8510XF network analyzer. Due to the down-conversion mechanism of the receiver chip, the input and output signals frequency are not the same and we can only obtain the input return loss here.

To get the power gain of the receiver, we can observe the output power from the spectrum analyzer. The input is also generated by signal generator cascading with V-band source module to up-convert the input signal to the desired frequency. In the receiver circuit, the down-conversion mixer is implemented on chip and the output signal can be directly observed by spectrum analyzer without off-chip down converter. The input RF signal is directly conveyed with CASCADE ACP-50-GSG-100 probe to input GSG pad. Because the input LO and output IF are differential signals, these signals must be taken from two GSGSG pads which are conveyed with CASCADE -GSGSG-150 probes. The LO signals are generated by signal generator cascading with a transformer to translate the single-end LO signal to differential. Finally the differential output signal is connect to power combiner to combine the differential signal to single-end and observed by spectrum analyzer.

There are six DC powers that must be supplied to the receiver circuit which are probed using 150-pitch 6P DC probe and the additional off-chip dc bias is not required. To measure the linearity property of the receiver, we can vary the input power and observe the output spectrum. The power loss induced from the cable and probes must be compensated at desired frequency to acquire the practical gain of the circuit. Figure 4.10 to Figure 4.13 depict the measurement block diagrams.

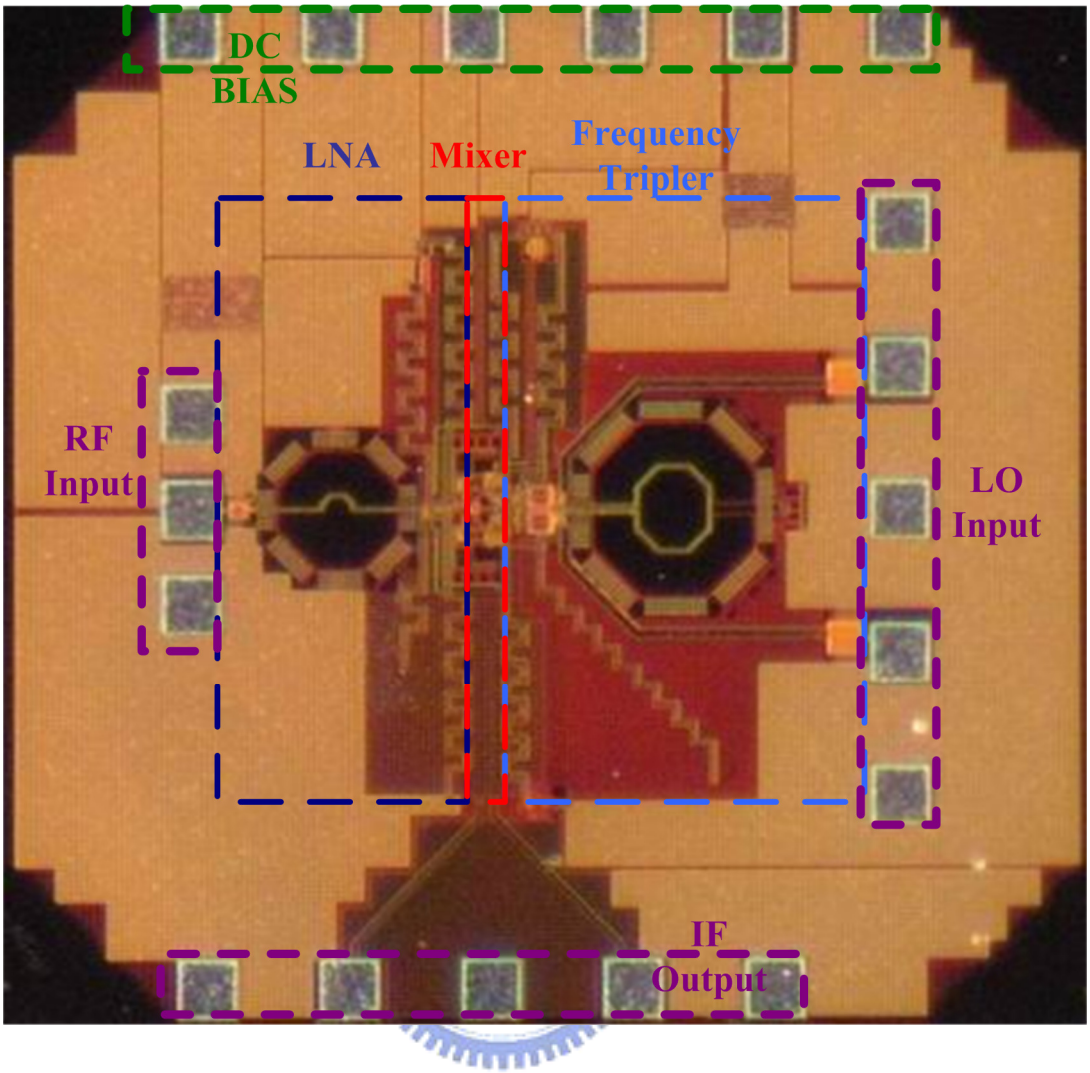


Figure 4.9 Chip microphotograph of the receiver

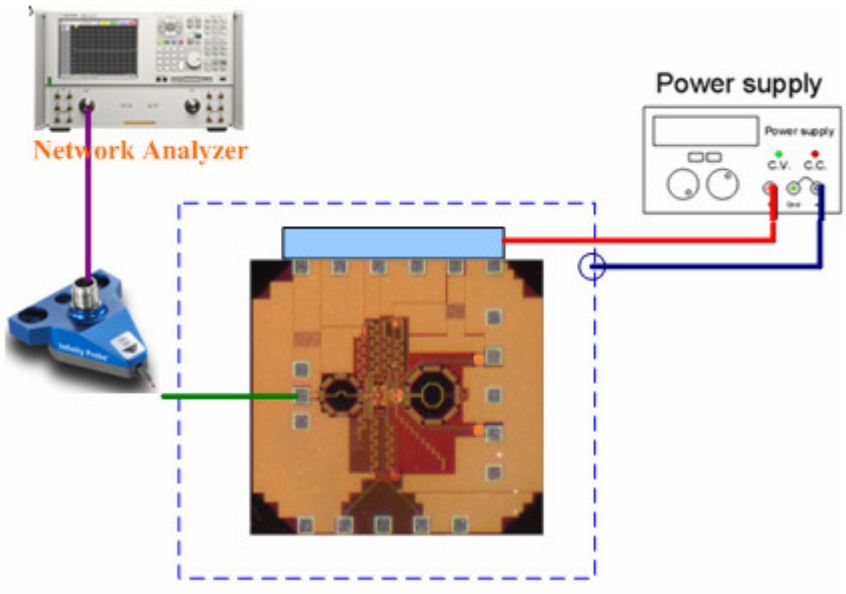


Figure 4.10 Instrument setup for Rx S-parameter analysis

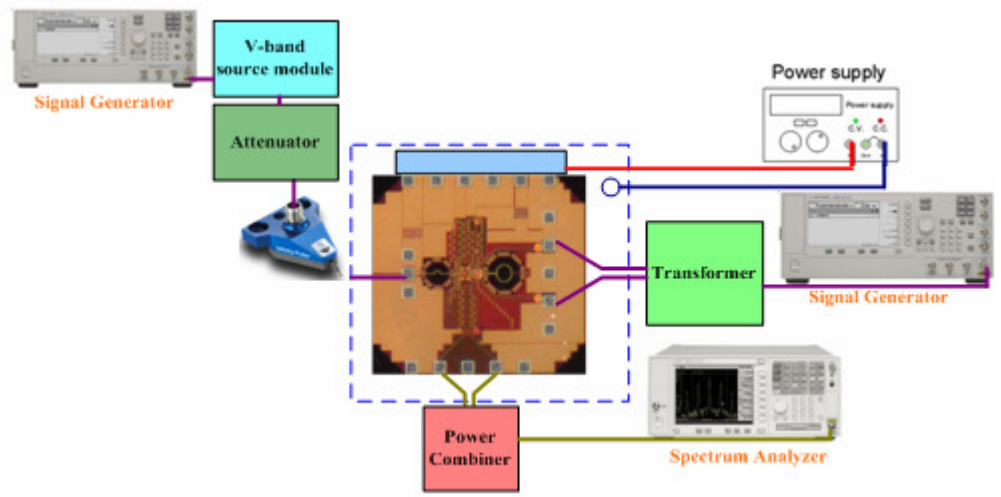


Figure 4.11 Instrument setup for Rx spectrum analysis

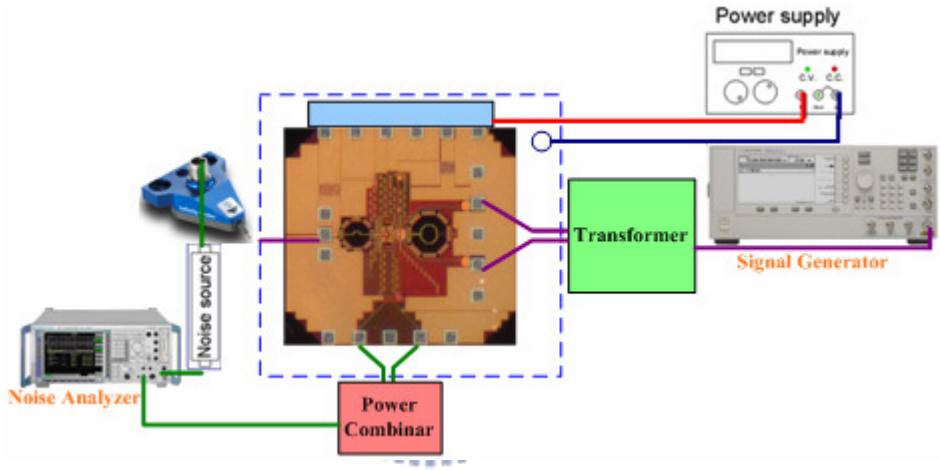


Figure 4.12 Instrument setup for Rx noise analysis

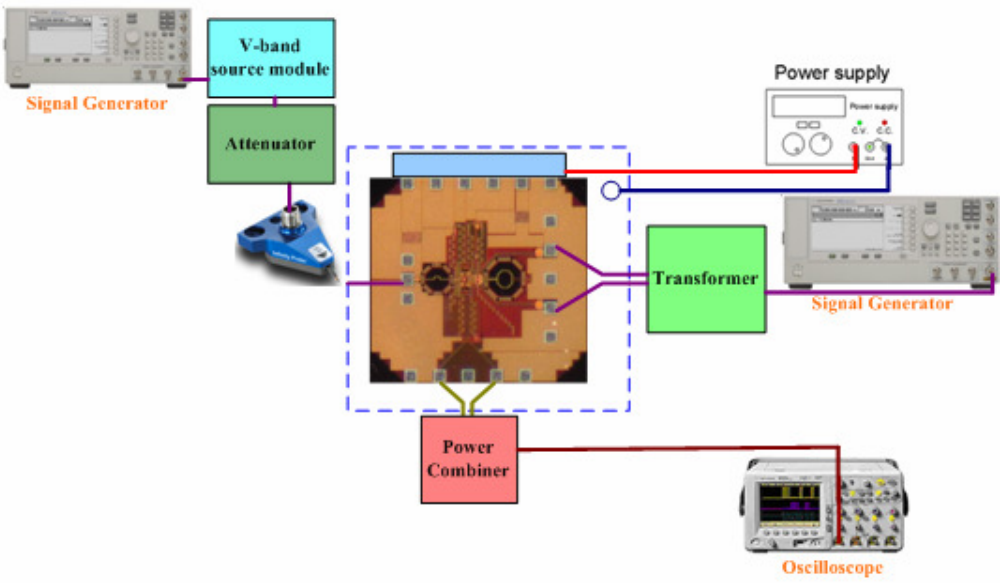


Figure 4.13 Instrument setup for Rx waveform analysis

4.3 Experiment Results

Circuits are fabricated using CMOS 0.13-um 1P8M CMOS technology with ultra thick metal measuring 3.3 um. The chip is measured using on-wafer probing. Here we show the measurement results of LNA and receiver circuit respectively.

4.3.1 Experiment Results of 70-GHz LNA

In the first, the s-parameters of the LNA are measured while the input power is set constant at -15 dBm. The gate voltage at the input stage of MOS is biased at 0.7 V due to optimal noise and gain considerations. The circuit is supplied at a 0.8-V supply voltage with the dc power consumption of 5.4 mW and the chip area is only 0.38 mm^2 including all the test pads and dummy metals. The measured gain is plotted against frequency are presented in Figure 4.14. The measurement shows that a maximum gain of 9.1 dB at 68.5 GHz and 3-dB bandwidth covers from 65.1 GHz to 72.3 GHz. The input and output return losses are shown in Figure 4.15 and Figure 4.16, respectively. Under the operating frequency, input and output return losses are 12 dB and 14 dB, respectively.

Figure 4.18 illustrates the linearity performance, P_{1dB}, of the proposed LNA. With a 0.8-V supply voltage, the input-referred 1 dB compression point ($P_{1dB\text{-}in}$) is -17 dBm at the center frequency. This result ensures that input power of S21 gain measurement is larger than P_{1dB} point and the power gain is limited by circuit linearity. Figure 4.19 shows the re-measurement results under input power of -40 dBm at out laboratory and comparison with simulation result. It performs that the circuit has a gain of 10.9 dB at 67.8 GHz with a 3-dB bandwidth of 7 GHz from 65 to 72 GHz. So far, we still cannot measure the noise figure performance and the measurement result of the noise figure is not shown here. The noise figure measurement is waiting for the instruments and will be measured in the future. Table 4.1 lists the summary of the LNA measurement and comparison with post-simulation results.

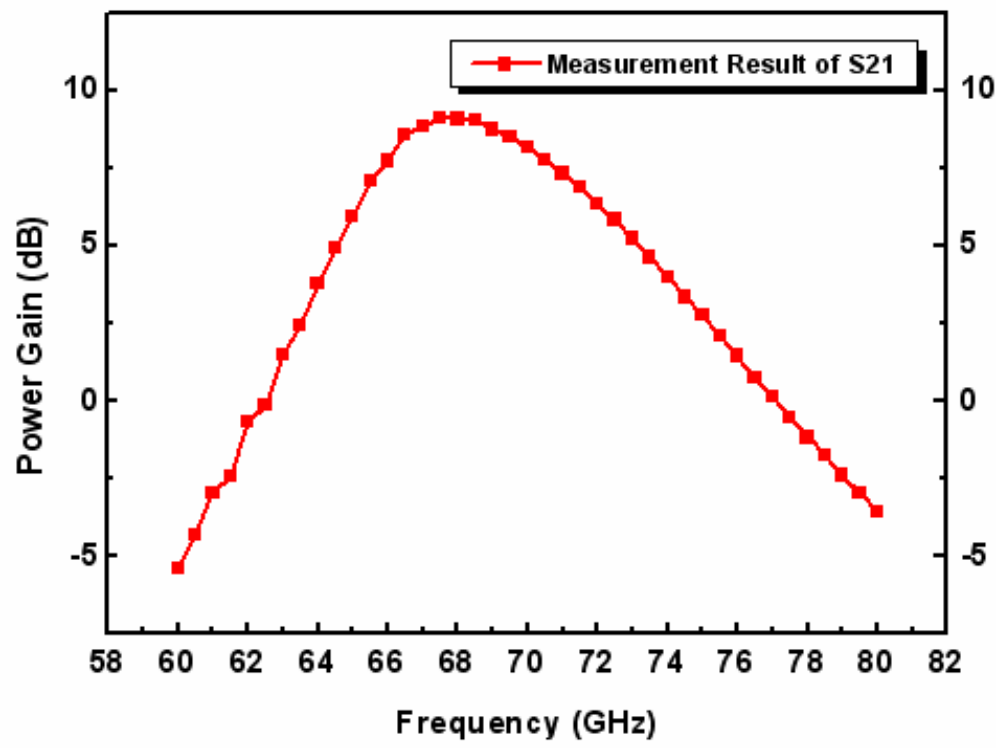


Figure 4.14 Measured S21 for the proposed LNA

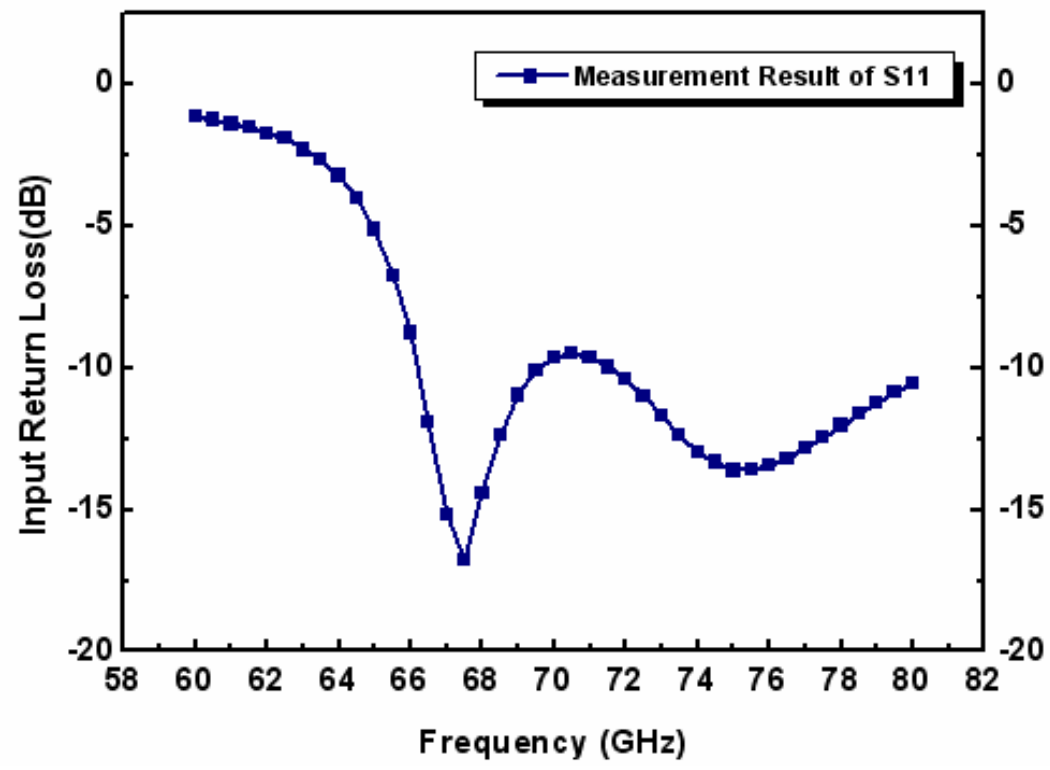


Figure 4.15 Measured S11 for the proposed LNA

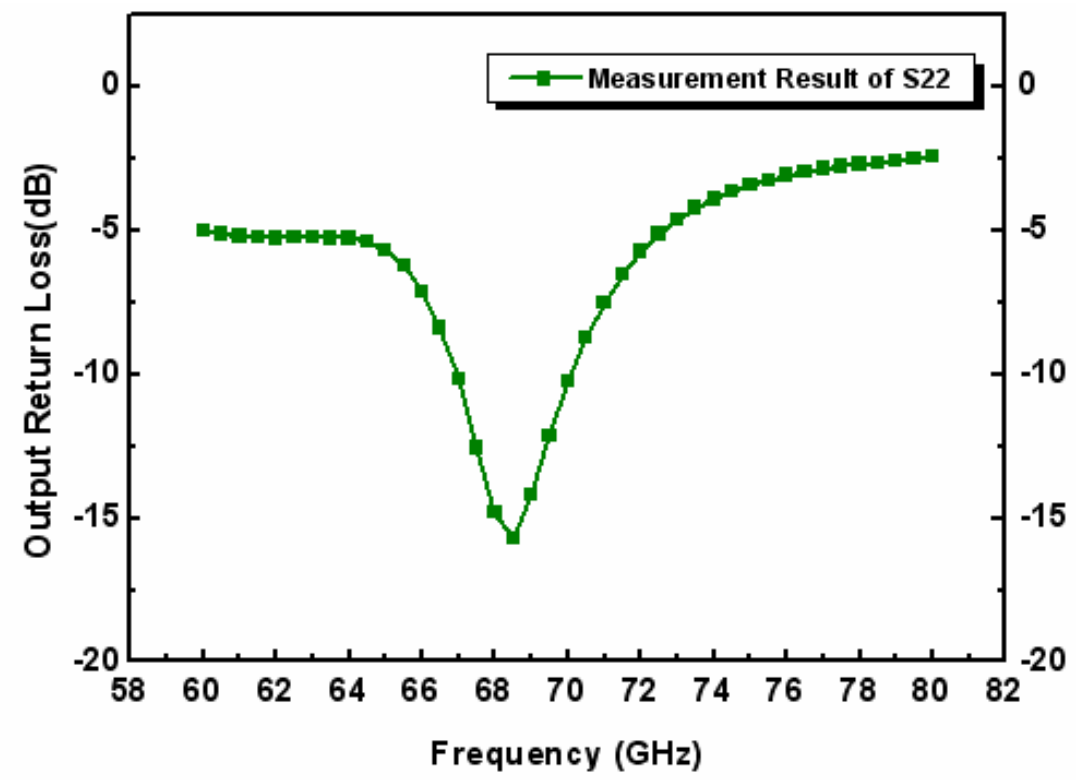


Figure 4.16 Measured S12 for the proposed LNA

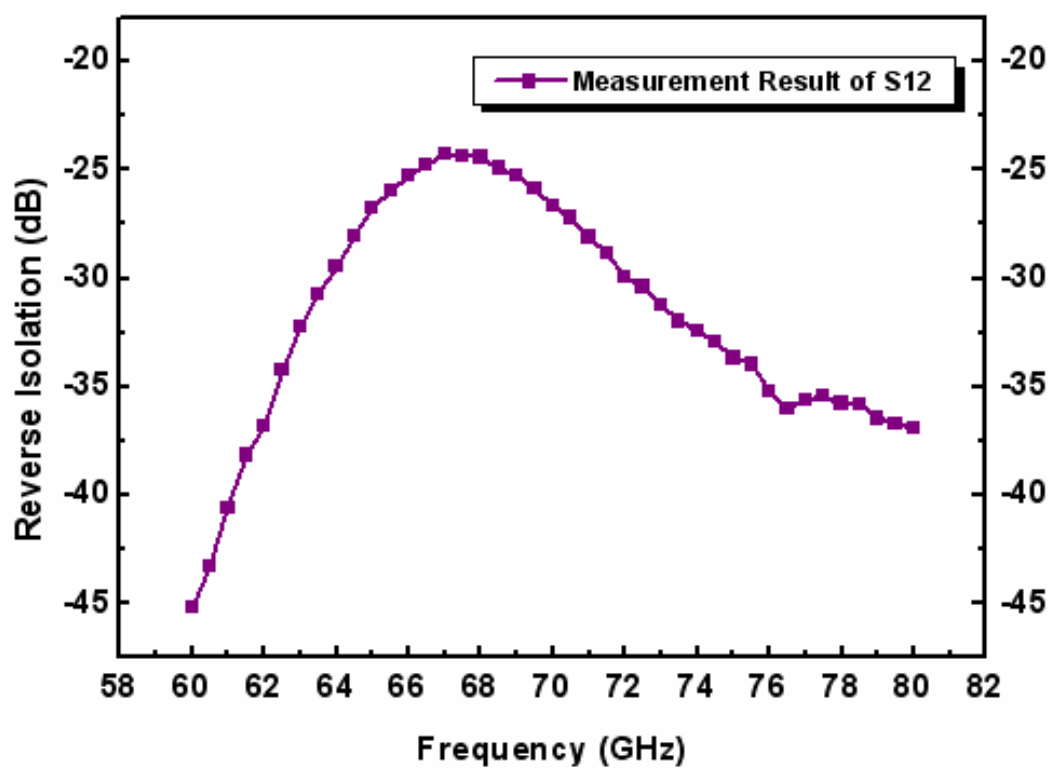


Figure 4.17 Measured S22 for the proposed LNA

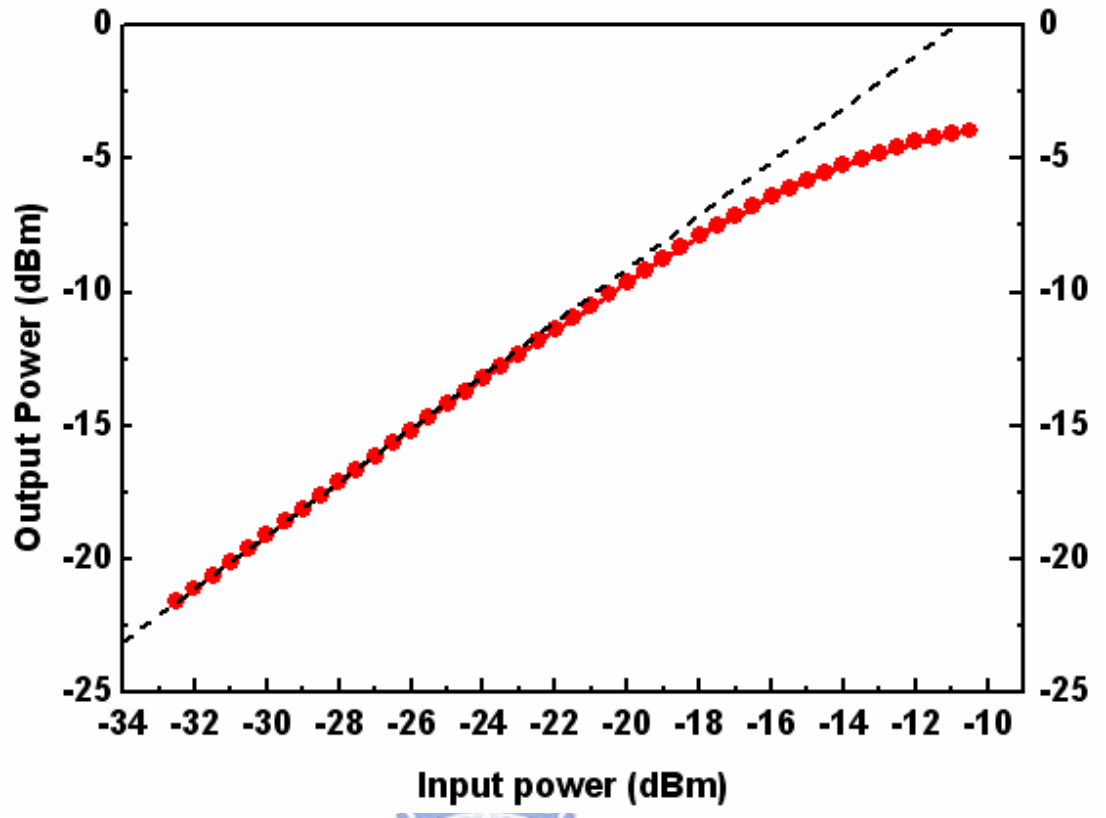


Figure 4.18 Measured 1-dB compression point for the proposed LNA

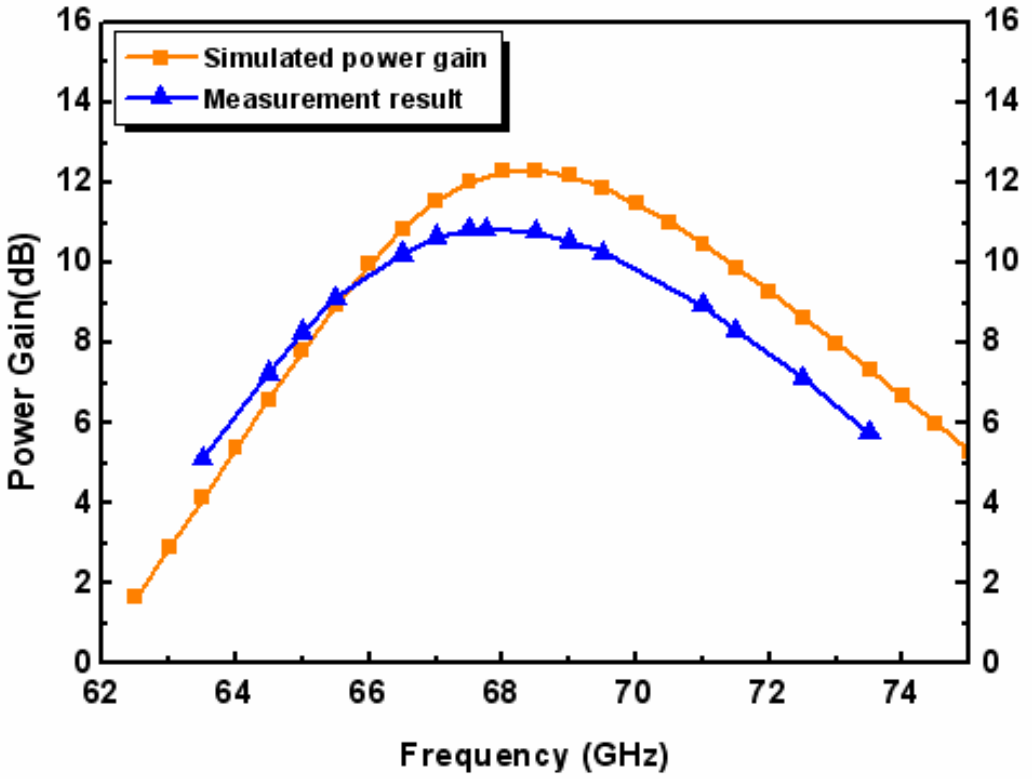


Figure 4.19 Measured simulated power gain for the proposed LNA

Table 4.1 Summary of the 70-GHz LNA

	Post-simulation			*Measurement*
Technology	**TSMC 0.13-um 1P8M**			
Frequency Band	**66.2 ~ 73.8 GHz**	**66 ~ 73 GHz**	**65.8 ~ 72.1 GHz**	**64.8 ~ 71.8 GHz**
Center Frequency	**69.7 GHz**	**69 GHz**	**68.4 GHz**	**67.8 GHz**
Corner	**FF**	**TT**	**SS**	**none**
VDD	**0.8 V**			
Gate Bias	**0.7 V**			
S11 (< -9.5 dB)	**67.7 ~ 79.7 GHz**	**67.5 ~ 78.6 GHz**	**67.1 ~ 77.8 GHz**	**66.1~ 80 GHz**
Gain (dB)	**13.1**	**12.8**	**11.9**	**10.9**
S22(<-9.5 dB)	**69.1 ~72.8 GHz**	**67.7 ~ 71.9 GHz**	**65.4 ~ 70.7 GHz**	**66.9 ~ 70.2 GHz**
P_{1dB} (dBm)	**-17.9**	**-17.3**	**-16.5**	**-17**
NF (dB)	**4.9**	**5**	**5.2**	*****
Power (mW)	**7.9**	**6**	**4.3**	**5.4**

Comparing with post-simulation results, the fabricated chip possibly fell on the corner between SS and TT corners. It is accordance with the DC power consumption under the same DC bias condition. The proposed circuit consumes 5.4 mW and is between TT and SS corners that are simulated. The frequency shift of the proposed circuit is around 1 GHz and is less than 1.5 % when normalized with center frequency. This may come from the process variation of the transmission line that may not be predicted under simulation. Although we are not measured the noise figure performance, owing to the input/output return loss and power gain performance of the measurement result is close to the simulation results, the noise figure performance around 5 dB can be expected. The actual value of the noise figure can be measured after the high-frequency measurement instruments arrive.

4.3.2 Experiment Results of 60-GHz Receiver

The chip is designed and fabricated using 0.13-um CMOS technology with a total die area of 1.2mm^2 including all test pads and dummy metal. The circuit is biased at a 1.2-V supply voltage with current consumption of 3, 0.5, and 6 mA for the LNA, mixer, and frequency tripler respectively. The circuit dc power consumption is about 11.4 mW excepting the buffer power consumption.

In the first, the input return loss (S11) of the receiver is shown in Figure 4.20. The measured S11 is below than -10 dB for frequency larger than 60 GHz. When measure the other parameter of receiver such as conversion gain and IF-bandwidth, the LO and RF power levels are set constant at 6 dBm and -40 dBm, respectively. Figure 4.21 shows the measured conversion gain of the receiver and the IF frequency is chosen as 50 MHz. To observe the conversion gain of the different RF frequency, the LO frequency is chosen as: $\mathrm{LO} = (RF - IF)/3$. The measurement shows that 11-dB maximum conversion gain with 3-dB bandwidth covering from 50.5 to 58.5 GHz.

To evaluate the large-signal behavior of the receiver, the P_{1dB_in} is measured as shown in Figure 4.22. The measured P_{1dB_in} is estimated as the receiver gain drops 1 dB and is occurred when input power reaches -12 dBm. Due to the measurement instrument limitations, the LO and IF port input return loss and the noise figure performance cannot be measured in this circuit. However, the LO signal is supplied by signal generator and the LO power can be enhanced by tuning the signal generator. Since IF output frequency is 50 MHz or 100 MHz, the output impedance matching can easily be achieved by using the resistance and is not critical at such a low frequency. Table 6.2 summaries the measured results of the overall receiver circuit.

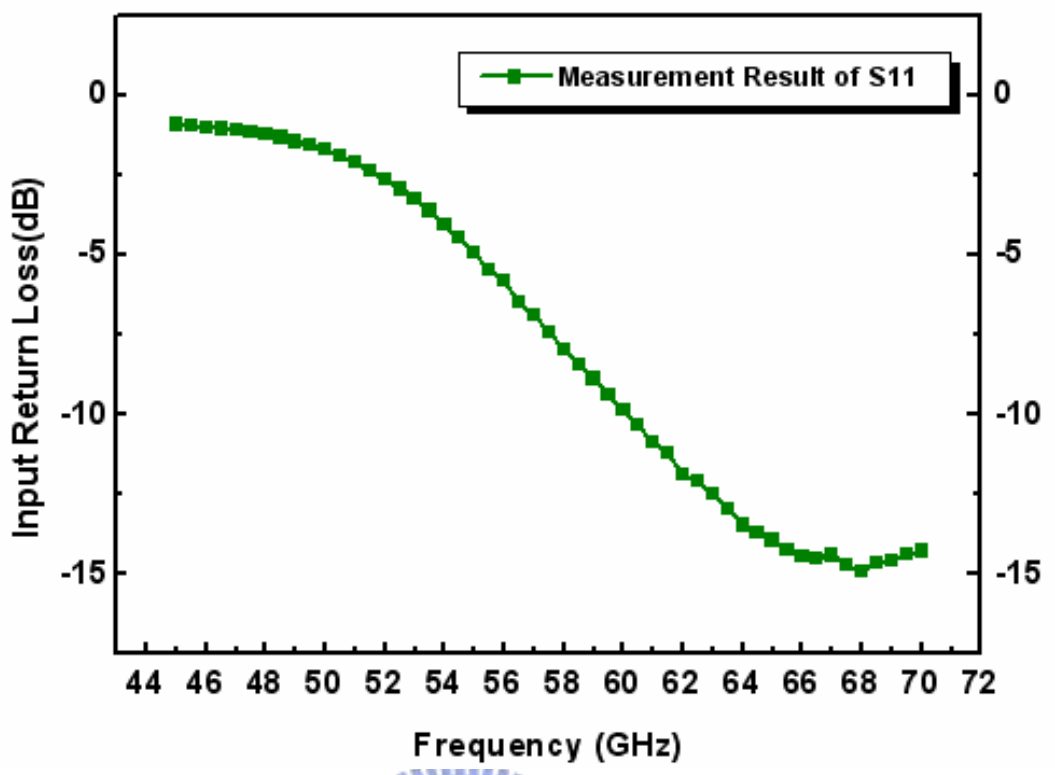


Figure 4.20 Measured S11 for the proposed receiver

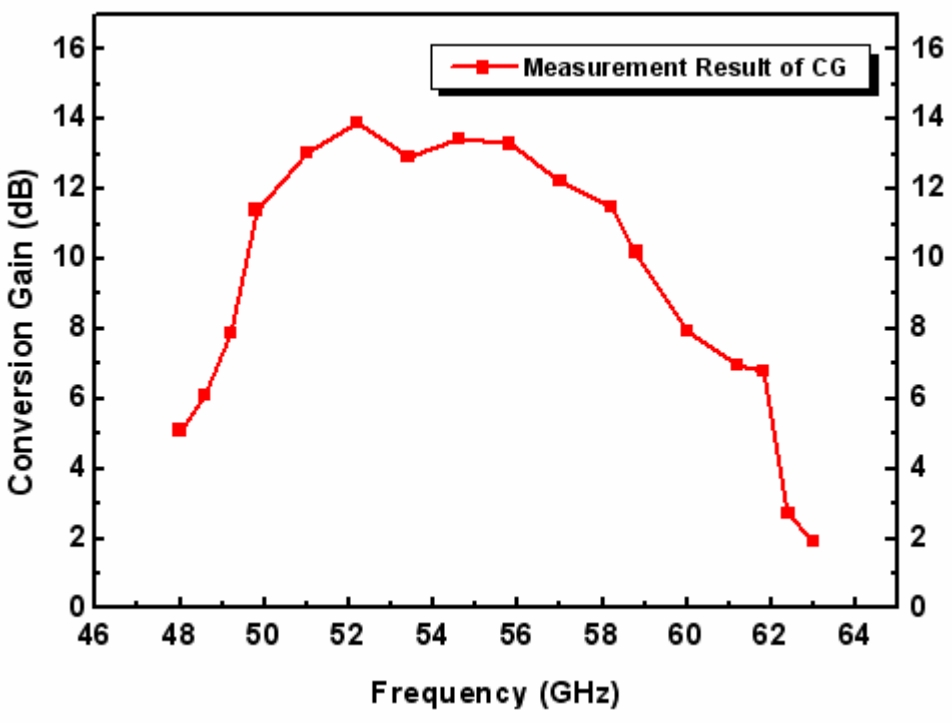


Figure 4.21 Measured conversion gain for the proposed receiver

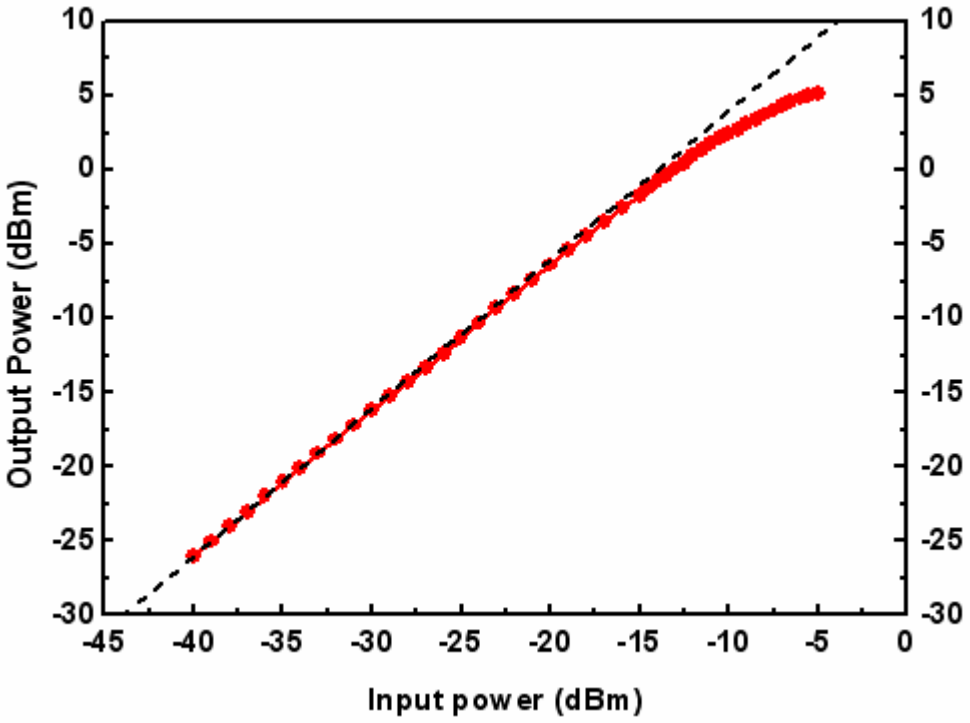


Figure 4.22 Measured P_{1dB} for the proposed receiver

Table 4.2 Summary of the RUT

	Post-simulation			*Measurement*
Technology	**TSMC 0.13-um 1P8M**			
Frequency band	**56 ~65 GHz**	**56.3 ~65.5 GHz**	**56.9 ~ 65.3 GHz**	**50.5 ~ 58.5 GHz**
Corner	**FF**	**TT**	**SS**	**none**
VDD	**1.2 V**			
Gate Bias	**0.65 V / 0.65 V (LNA/Tripler)**			
S11 (< -9.5 dB)	**> 58.5 GHz**	**> 58.6 GHz**	**> 58.7 GHz**	**> 60 GHz**
LO Power (dBm)	**4**	**4**	**4**	**6**
Gain (dB)	**25.6**	**24.4**	**21.8**	**13.9**
P_{1dB} (dBm)	**-23.9**	**-22.8**	**-20.9**	**-12**
NF (dB)	**7.5**	**7.7**	**8.3**	*****
Power (mW)	**20.6**	**14.4**	**10.3**	**11.4**

4.4 Discussions and Comparisons

From the comparison shown in Table 1, the peak gain frequency of 67.8 GHz is in good agreement with the design value of 69 GHz. The gain mismatch between simulation and measurement results may come from the EM simulation inaccuracy. In the other words, the quality factor of the micro-strip transmission line is not good enough as expected.

All of the T-lines characteristics are simulated using an EM simulator, Ansoft HFSS. Comparing with another EM simulator, Sonnet, the quality factor of the HFSS is much better than the sonnet. This may be caused from the dissimilar of mathematical calculation or the difference of simulation settings. Another factor that may effect the simulation is the inaccurate active device modeling at high frequency beyond 30 GHz. Since the circuit is operating under 70-GHz band, the active device performance may somehow different from the simulation. Table 4.3 summarizes the previously reported CMOS LNAs operated above 50 GHz and compared with the proposed LNA circuit. The proposed LNA exhibits lower NF and small power consumption as comparing with other works.

Table 4.3 Comparison of previously reported LNAs for frequency above 50 GHz

Reference	[7] JSSC 05'	[8] ISSCC 06'	This work
Frequency (GHz)	51-65	50-58	65-72
Gain (dB)	15	24.7	10.9
NF (dB)	6	7.1	*5.1
Power (mW)	54	72	5.4
P_{1dBin} (dBm)	-18	-22	-17
Chip Size(mm^2)	1.3	0.46	0.38
Supply Voltage	1.5	2.4	0.8
Technology	0.13um CMOS	0.13um CMOS	0.13um CMOS
Topology	3-stage Cascode	3-stage Cascode	3-stage CS

* Simulation Results

From the comparison between simulation and measurement results which is illustrated in Table 2, there are large amount differences between them. Main differences are the power gain mismatch and the frequency shift. Since the power consumption of each stage is reasonable as comparing with simulation, each building block can be taken as working normally. Moreover, when obtaining the output spectrum from baseband to RF frequency, there is not any unexpected signal tone and shows the circuit blocks are not oscillating. From the output signal spectrum, it also shows the tripler circuit exactly performs the right function to down convert the RF frequency to the baseband using LO frequency of only 1/3 RF frequency.

By carefully checking the layout of the circuit, we find out the most critically error is caused by the schematic wrong in the LNA, as shown in Figure 4.23. This cause the MOS M3 on the cascode stage becomes diode connect and hence, the second stage of the LNA almost provide 0-dB gain here and greatly reduce the entire gain. The modified simulation result of the power gain is shown in Figure 4.24.

Since the schematic error can be checked from the LVS (layout versus schematic), but this inductor is implemented using Tline. To LVS, the Tline is nothing more than a metal and cannot find if the layout is wrong. To overcome this problem, we can choose a given device model such as resistance to replace with the Tlines to check the LVS. After that, we can put the Tlines back to the circuit and remove the given device. Finally, check the LVS one more time. By using this method, we can ensure the circuit layout is completely match to the schematic when using the Tlines.

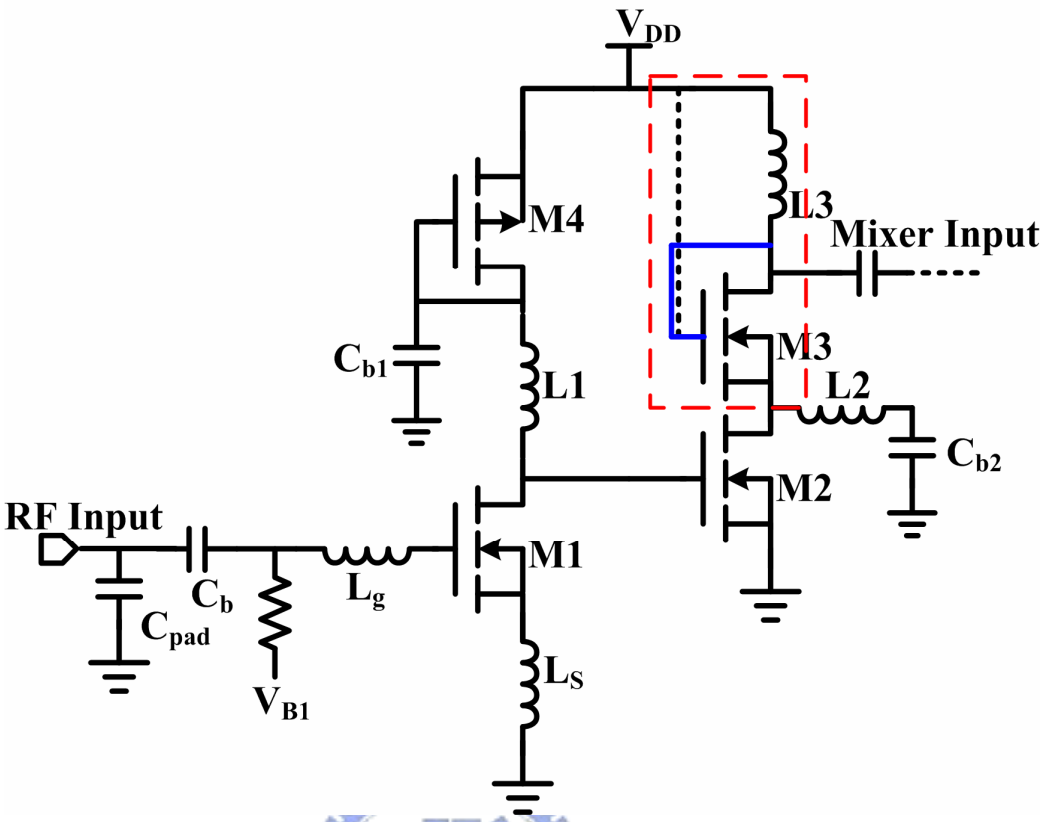


Figure 4.23 The schematic error of the LNA circuit in receiver

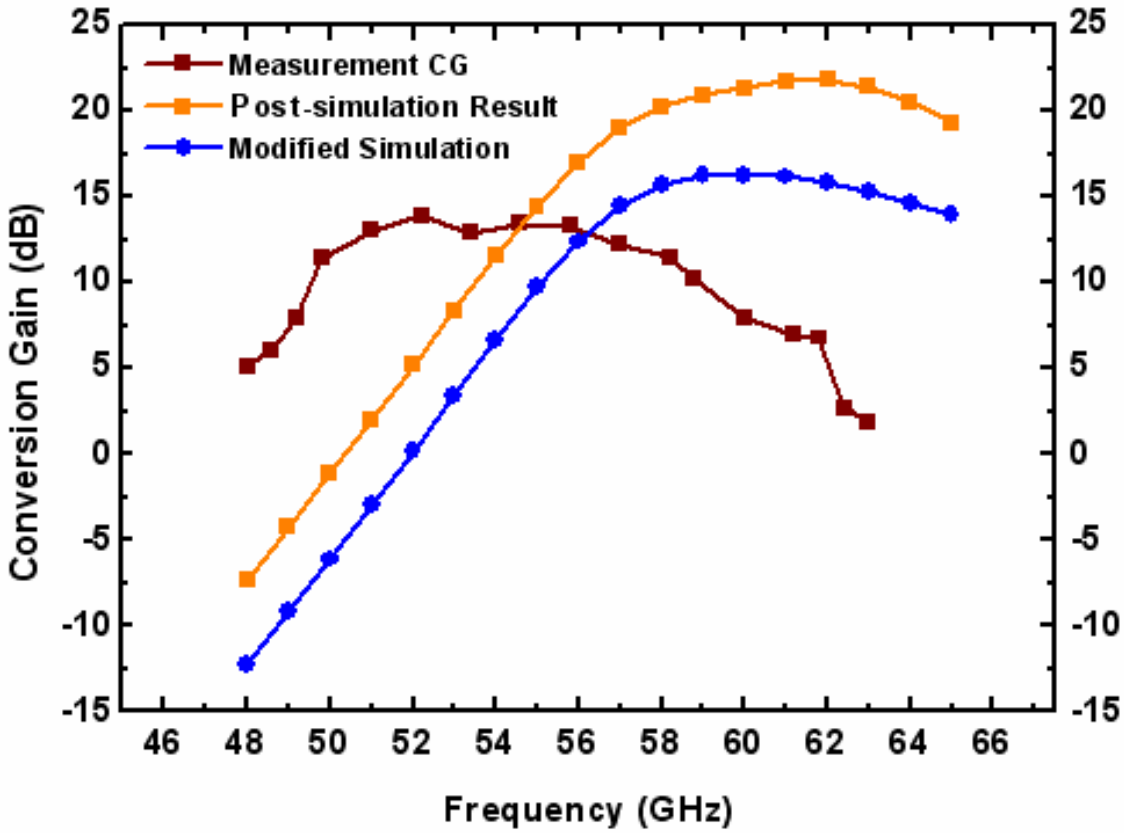


Figure 4.24 The modified simulation result and comparsion with measurement results

Second, the frequency shift of the conversion gain is discussed. The most probably reason is the inductance value mismatch with the layout. Observing the layout of the transmission line, we find that the short length of interconnect between two MOS is disregarded in simulation, as shown in Figure 4.25. Since the circuit is operating under high frequency and the resonating inductance is relatively small, a small amount of inductance will cause the large frequency shift. For example, the resonate inductances at 60-GHz is around 200 pH and if the interconnect has the inductance of 5 pH, the frequency shift will go to about 1.5 GHz. After compensate the interconnection inductance into the circuit, the receiver is re-simulated and comparing with measurement results. The modified simulation result of the power gain is shown in Figure 4.26. As can be seen, the center frequency of the receiver is down to 57 GHz and is closer to the measurement result. Table 4.4 shows the comparison summary of post-simulation, modified-simulation, and measurement results.

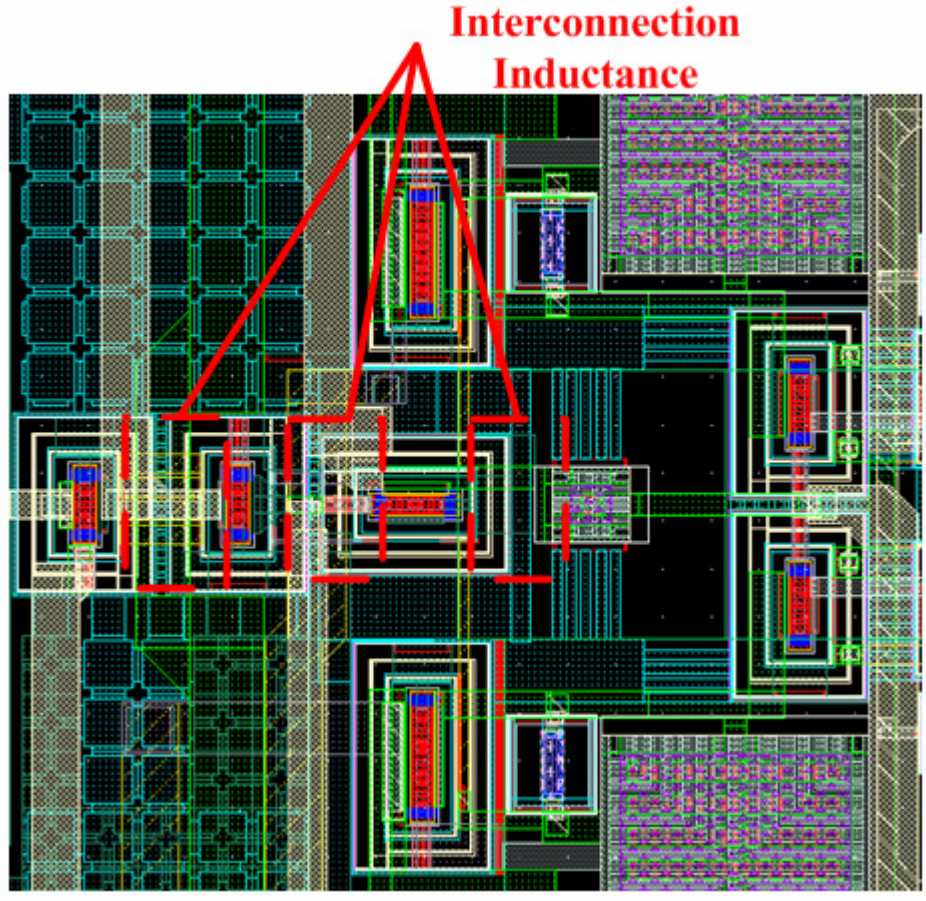


Figure 4.25 The transimission line layout of the receiver

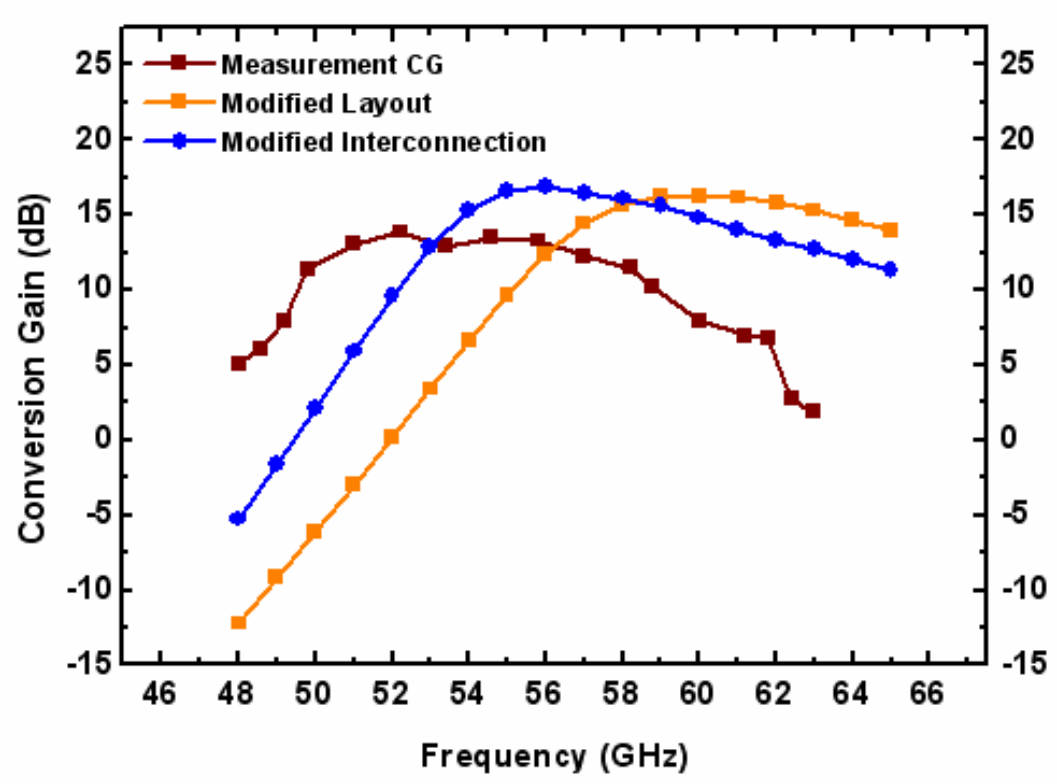


Figure 4.26 The modified post-simulation results of conversion gain

Table 4.4 Comparison of measurement and modified simulation results

	Post-simulation	*Modified-Simulation*	*Measurement*
Frequency band	56.9 ~ 65.3 GHz	53.3 ~ 61.2 GHz	50.5 ~ 58.5 GHz
Corner	SS	SS	none
VDD	1.2 V		
Gate Bias	0.65 V / 0.65 V (LNA/Tripler)		
S11 (< -9.5 dB)	> 58.7 GHz	> 55.6 GHz	> 60 GHz
LO Power (dBm)	4	4	6
Gain (dB)	21.8	16.8	13.9
P_{1dB} *(dBm)*	-20.9	-16.5	-12
NF (dB)	8.3	9.3	*
Power (mW)	10.3	10.3	11.4

The gain mismatch between the simulation and measurement may also come from the EM simulation inaccuracy. Moreover, the measurement input return loss at the center frequency is about -5 dB and the input power cannot perfectly transport to the circuit. This also causes some of the power gain loss. The other mismatch may come from the LO imbalance and the inaccurate active device modeling at such a high operating frequency. Since the receiver is operating under 60-GHz band, the active device performance may somehow different from the simulation. Consequently, if we have in mind of the above considerations and fine tune the circuit layout and EM simulation, the proposed receiver can work as well as expected.

Finally, Table 4.5 presents the comparison of this work and other published 60-GHz receivers. This work has superior advantage of low noise and low power consumption. More importantly, by applying the frequency tripler, only 20-GHz frequency synthesizer is required in this architecture and is suitable for 60-GHz applications.

Table 4.5 Performance comparison with other 60-GHz receiver

	This work (Measured)	This work (Post-sim)	[4] JSSC 06'	[5] ISSCC 07'	[6] ISSCC 07'
Architecture	**Homodyne**	**Homodyne**	**Homodyne**	**Heterodyne**	**Heterodyne**
Frequency (GHz)	**50.5 ~ 58.5**	**56.3 ~65.5**	**57.5~64**	**49.5~**	**57~63**
Supply Voltage (V)	**1.2**	**1.2**	**1.2**	**1.8**	**1.2**
Chip Area (mm^2)	**1.2**	**1.2**	**N/A**	**N/A**	**3.6**
DC Power (mW)	**11.4**	**5.9 + 8.5 †**	**9**	**56*****	**76.8****
Conversion Gain (dB)	**13.9**	**24.4**	**28***	**31.5***	**11.8**
Noise Figure (dB)	**9.2 ††**	**7.7**	**12.5**	**6.9**	**10.4**
P_{1dB} (dBm)	**-12**	**-22.8**	**-22.5**	**-25.5**	**-15.8**
IF Amplifier	**No**	**No**	**Yes**	**Yes**	**Yes**
Technology	**0.13 um CMOS**	**0.13 um CMOS**	**0.13 um CMOS**	**0.09 um CMOS**	**0.13 um CMOS**

†including tripler =receiver core + tripler (20GHz VCO can be implemented by 8mW)

†† simulation result *including IF amplifier ** including 40-GHz VCO and divider

***including 29 GHz VCO and doubler

Chapter 5
Conclusions and Future Work

5.1 Conclusions

Two V-band circuits: 70-GHz LNA and 60-GHz direct-conversion receiver which consists a LNA, a down-conversion mixer and frequency tripler have been designed, fabricated and tested in a 0.13-um CMOS technology.

In the proposed LNA, three-stage common-source topology is used instead of cascode configuration to improve the noise performance. Therefore, supply voltage can be reduced to 0.8 V for low voltage and low power design. The measured LNA gain is 10.9 dB and the simulated noise figure is 5.1 dB at 67.8 GHz while the input and output return losses are lower than -12 dB at center frequency. Furthermore, the 3-dB bandwidth covers from 65 GHz to 72 GHz which is suitable for wideband applications. Finally, this circuit can be operated on a low voltage of 0.8-V and only consumes 5.4 mW with a chip size of 0.38mm^2. According to the comparisons in Table 4.3, the proposed LNA shows low noise, low power and low supply voltage while achieving reasonable power gain and wideband input and output matching. It is proved that the proposed LNA is feasible to use it in building fully integrated receiver at frequency of above 50 GHz.

A 60-GHz CMOS direct-conversion receiver integrated with a frequency tripler is also proposed. The receiver consists of a two-stage LNA, a single-balanced active mixer, a frequency tripler, and output buffers. By using a frequency tripler, the operating frequency of the frequency synthesizer can be reduced from 60 GHz to 20 GHz, so the implementation of the frequency synthesizer also becomes much easier. According to the measurement results,

the receiver has power gain of 13.9 dB with 3-dB bandwidth covering from 50.5 to 58.5 GHz. The input-referred 1-dB compression point is about -12 dBm and the input return loss of -5dB at center frequency of 54.5 GHz. The simulated noise figure (NF) is about 9.2 dB. The entire circuit consumes 15.1 mW from 1.2-V power supply.

Finally, the main cause of the malfunction of the receiver has been found and verified lying in the schematic of LNA and interconnection between MOS to MOS. According to the comparisons in Table 4.5 Performance comparison with other 60-GHz receiver, the post-simulation of the receiver shows better performance on operating frequency of 57 ~64 GHz band, low noise figure and low power consumption as compared to other state-of-the-art works. It shows that the proposed receiver is very suitable to be applied in 60 GHz ISM band and has the great potential to be integrated with PLLs and baseband circuits. Furthermore, we believe the proposed method can also be applied to the other high frequency receiver circuit such as 77 GHz radar or even more high frequency systems.

5.2 Future work

The proposed direct-conversion receiver for 60-GHz ISM applications could be fabricated again with the modification of schematic error and taken the interconnection effects into account. To realize the complete homodyne receiver circuits, the I/O mixer and I/Q VCO can be implemented together with the LNA and frequency tripler circuits. Finally, the 20-GHz frequency synthesizer may also be included to provide a stable local frequency and form the more complete system.

References

[1] Federal Communications Commission, FCC 47 CFR, 10-1-93 Edition, pp. 581-582.

[2] B. A. Floyed, S. K. Reynolds, U. R. Preiffer, T. Zwick, T. Beukema and B. Gaucher, "SiGe Bipolar Transceiver Circuits Operating at 60GHz," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, January 2005.

[3] S. E. Gunnarsson, C. Karnfelt, H. Zirath, R. Kozhuharov, D. Kuylenstierna, C. Fager and A. Alping, "Single-Chip 60 GHz Transmitter and Receiver MMICs in a GaAs mHEMT Technology," *IEEE MTT-S International Microwave Symp. Dig.*, June 2006, pp. 801-804.

[4] B. Razavi, "A 60-GHz CMOS Receiver Front-End," *IEEE J. Solid-State Circuits*," vol. 41, pp. 17-22, January 2006.

[5] B. Razavi, "A mm-Wave CMOS Heterodyne Receiver with on-Chip LO and Divider," *IEEE Solid-State Circuits Conf .Dig. Tech. Papers*, pp. 188-189, February 2007.

[6] S. Emami, C. H. Doan, A. M. Niknejad and R. W. Brodersen, "A Highly integrated 60GHz CMOS Front-End Receiver," *IEEE Solid-State Circuits Conf .Dig. Tech. Papers*, pp. 190-191, February 2007.

[7] C. H. Doan, Sohrab Emami, Ali M. Niknejad and Robert W. Broderson, "Millimeter-Wave CMOS Design," *IEEE J. Solid-State Circuits*, vol40, no.1, pp.144-155, January 2005.

[8] Chieh-Min Lo, Chin-Shen Lin, Huei Wang "A Miniature V-band 3-stage Cascode LNA in 0.13um CMOS," *IEEE Solid-State Circuits Conf .Dig. Tech. Papers*, pp. 1254-1263, February 2006.

[9] J. C. Chiu, C. P. Chang, M. P. Houng, and Y. H. Wang, "A 12–36 GHz pHEMT MMIC balanced frequency tripler," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 1, pp. 19–21, January 2006.

[10] A. Boudiaf, D. Bachelet, and C. Rumelhard, "A high-efficiency and low-phase-noise 38-GHz pHEMT MMIC tripler," *IEEE Trans. Microwave Theory and Tech.*, vol. 48, no. 12, pp. 2546–2553, December 2000.

[11] Y. Campos-Roca, L. Verweyen, M. Fernández-Barciela, E. Sánchez, M. C.

Currás-Francos, W. Bronner, A. Hülsmann, and M. Schlechtweg, "An optimized 25.5–76.5 GHz pHEMT-based coplanar frequency tripler," *IEEE Microwave and Guided Wave Letters*, vol. 10, no. 6, pp. 242–244, June 2000.

[12] Scott K. Reynolds, Brain A. Floyd, Ullrich R. Pfeiffer, Troy Beukema, Janusz Grzyb, Chuck Haymes, Brain Gaucher, Mehmet Soyuer, "A Silicon 60-GHz Receiver and Transmitter Chipset for Broadband Communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2820-2831, December 2006.

[13] Behazad Razavi, *RF Microelectronics*. Prentice Hall.

[14] Edwin H. Armstrong, "The super-heterodyne – its origin, development, and some recent improvements," *Proceedings of the IRE*, vol. 12, October 1924, pp. 539-522.

[15] Chung-Yu Wu, Hong-King Kao, "A 2-V low power CMOS direct-conversion quadrature modulator with integrated quadrature voltage-controlled oscillator and RF amplifier for GHz RF transmitter applications," *IEEE Transactions on Circuits and System*, vol. 49, no. 2, pp. 123-134, February 2002.

[16] Andreas Springer, Linus Maurer, and Robert Weigel, "RF system concepts for highly integrated RFICs for W-CDMA mobile radio terminals," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 254-267, January 2002.

[17] J. Wenin," ICs for Digital Cellular Communications," *European Solid State Circuits Conf.*, Ulm, Germany, 1994, pp. 1-10.

[18] B. Razavi, "Design Considerations for Direct-Conversion Receivers," *IEEE Transactions on Circuit and Systems*, vol. 44, pp. 425-428, June 1997.

[19] H. Darabi and A. Abidi, "A 4.5mW 900-MHz CMOS Receiver for Wireless Paging," *IEEE J. Solid-State Circuits*, vol.35, Aug. 2000, pp. 1085-1096.

[20] J. Crols and M. Steyaert, "A single chip 900-MHz CMOS receiver front-end with a high-performance low-IF topology," *IEEE J. Solid State Circuits*, vol.30, no. 12, pp. 1483-1492, December 1995.

[21] Pengfei Zhang et al., "A 5-GHz direct-conversion CMOS transceiver," *IEEE J. Solid State Circuits*, vol.38, no. 12, pp. 2232-2238, December 2003.

[22] S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Brodersen, "A 60-GHz Down-Converting CMOS Single-Gate Mixer," *IEEE RFIC Symp. Dig. Papers*, pp. 163-166, June 2005.

[23] Y. Campos-Roca. L. Verweyen, M. Fernandez-Barciela. W. Bischof, M. C. Curras-Francos, E. Sanchez, A. Hulsmann, and M. Schlechtweg, "38/76 GHz PHEMT MMIC balance frequency doublers in coplanar technology," *IEEE Microwave and Guided Wave Letters*, vol. 10, no. 11, pp. 484-487, November 2000.

[24] Eoin Carey and Sverre Lidholm, "FET Frequency Multipliers," *Millimeter-Wave Integrated Circuits*, 2005, Chapter 7, Section2, pp. 169-186.

[25] H. Fudem, E.C. Niehenke, "Novel Millimeter Wave Active MMIC Triplers," *IEEE MTT-S International Microwave Symp. Dig.*, June 1998, pp. 387-390.

[26] Donald Allen, Danny Bryant, and Warren Gaiewski, "25.5 to 76.5 GHz Active Frequency Tripler for Automotive Radar Applications," *IEEE MTT-S International Microwave Symp. Dig.*, June 2003, pp. 2233-2236.

[27] C. H. Doan, Sohrab Emami, Ali M. Niknejad and Robert W. Broderson, "Millimeter-Wave CMOS Design," *IEEE J. Solid-State Circuits*, vol40, no.1, pp.144-155, January 2005.

[28] Derek K. Shaeffer and Thomas H. Lee, *The Design and Implementation of Low-Power CMOS Radio Receivers*, Kluwer Academic Publishers.

[29] Pietro Andreani and Henrik Sjoland, "Noise Optimization of an Inductively Degenerated CMOS Low Noise Amplifier," *IEEE Transaction on Circuit and Systems v*ol. 52, no. 5, May 2004.

Appendix

Re-designing the receiver circuit

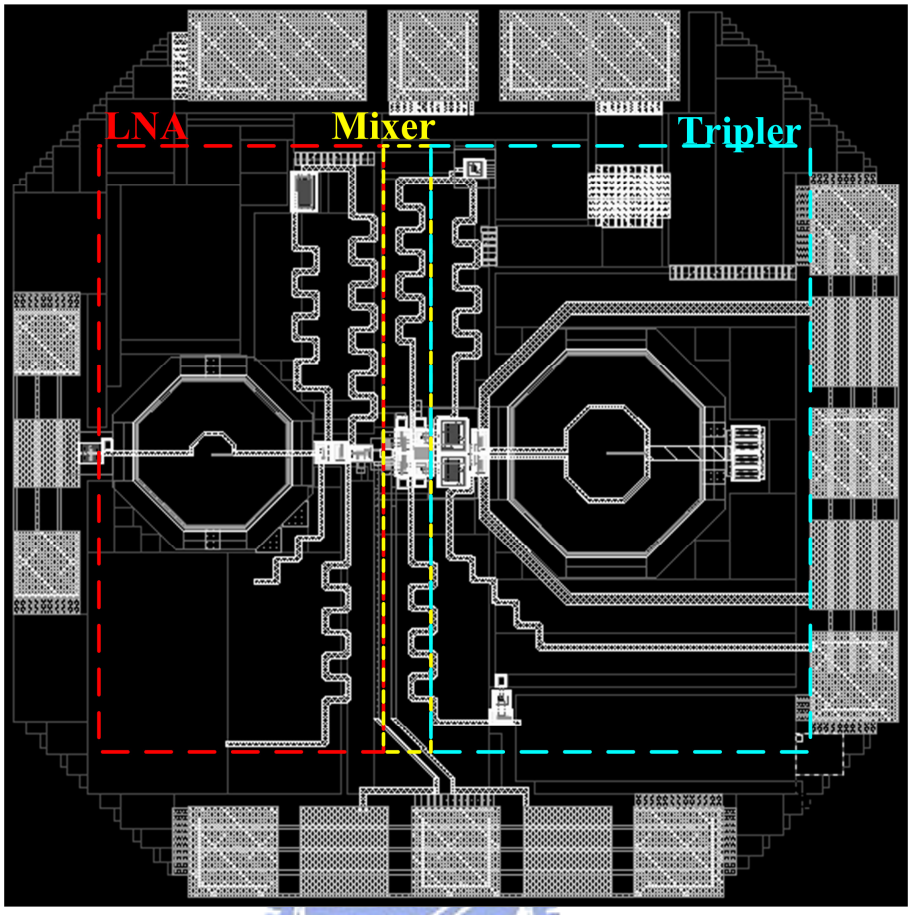
Besides compensating the layout error and take the parasitic capacitance of the interconnection lines into account, we also modified the circuit to improve the performances of the receiver.

At first, in order to reduce the DC bias pins, the scheme of the output buffer is modified to the open drain structure and the supply voltage can be provided off-chip. Moreover, we also make the supply voltage of the LNA, mixer and frequency tripler together which provide the same voltage level in the circuit. Hence, the DC pads can be reduced from 6-pin to 3-pin and can scale down the entire chip area greatly.

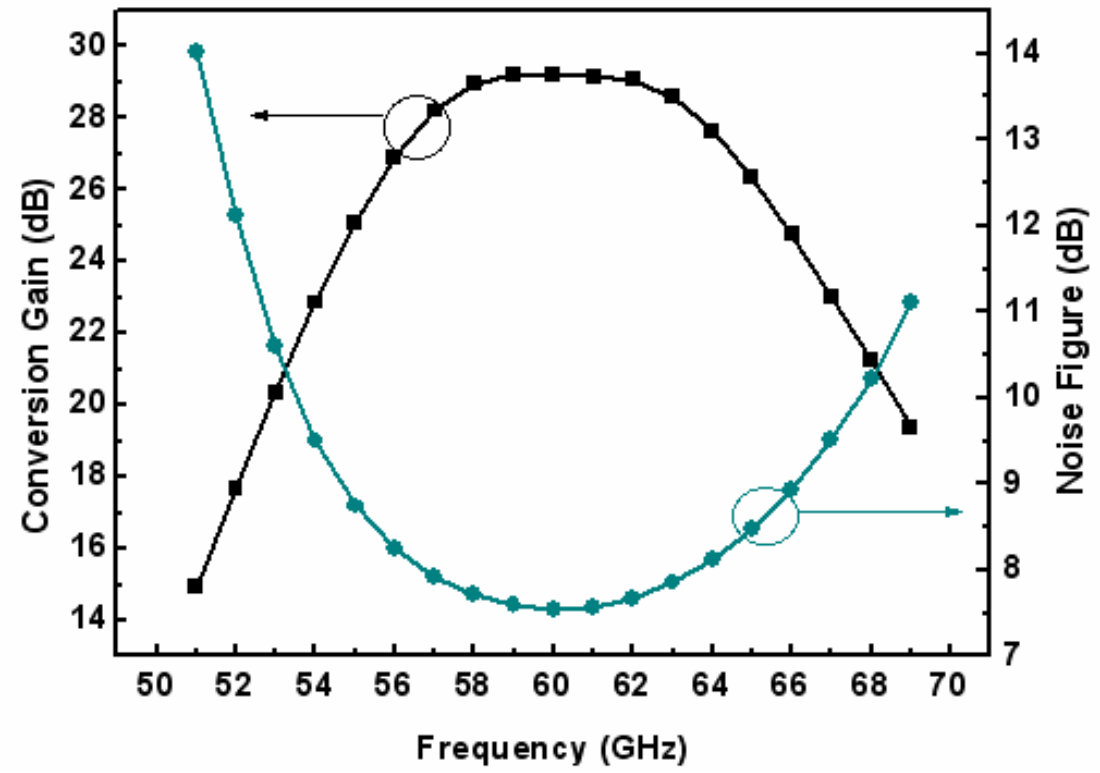
Second, the conversion gain of the mixer is designed as large as possible to improve the gain performance. Since the larger gain may limit the linearity performance, but from the experiment, the measurement gain will be larger than expected and we can pre-design the larger gain to compensate this mismatch.

In previous work, the gate bias of the frequency tripler core circuit and frequency tripler output buffer are co-designed to be 0.65 V, but we cannot just change the gate bias of the core circuit to observe the maximum frequency transition. Hence, in this case, the gate bias of the frequency tripler core circuit is also implemented off-chip and we can change the bias point individually to get the best receiver performance.

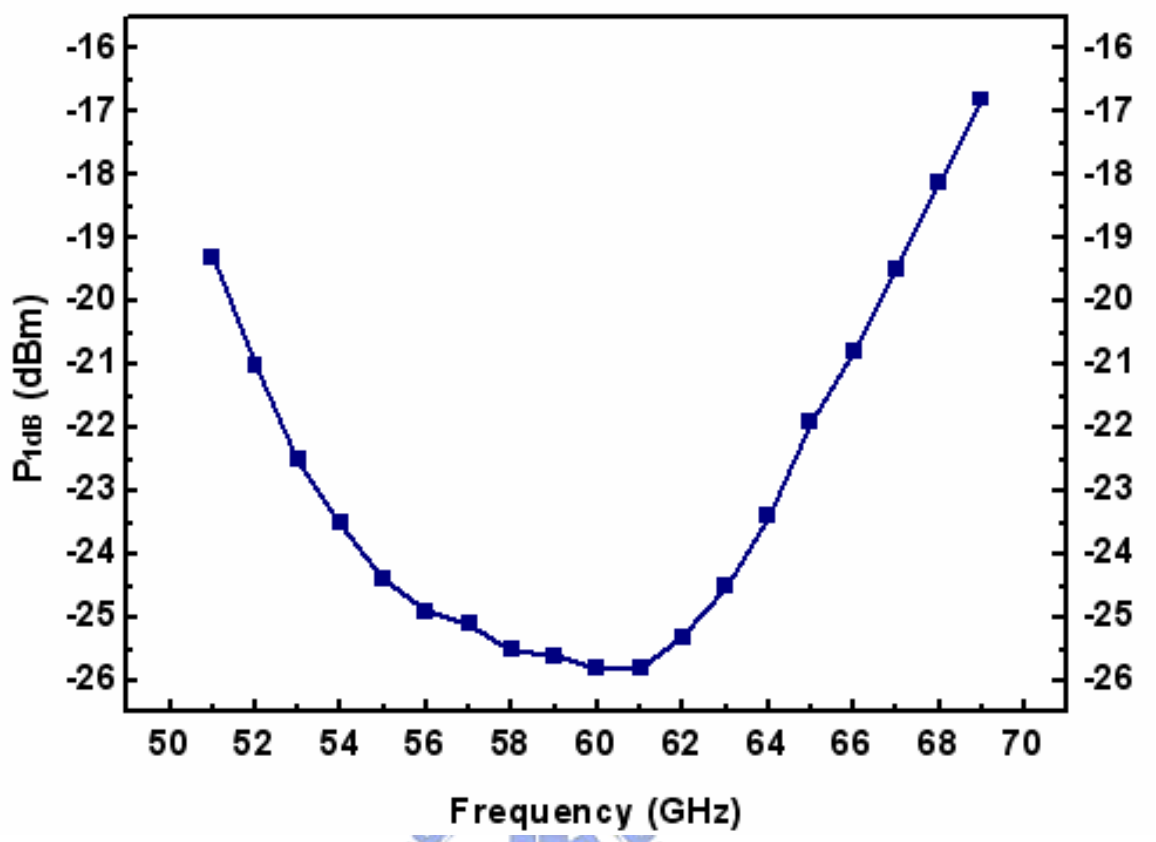
Moreover, ground planes of all the transmission lines are implemented by using only M1 as ground plane improve the quality factors. Comparing to use the M_1,M_2 or M_1,M_2,M_3 as the ground planes, the circuit can get the better noise performance and larger gain. The layout view of the re-designed receiver is shown in (a) and the re-designed receiver performances are shown in the (b) to (d). The total power consumption of the proposed receiver circuit is 14.2 mW. Finally, the comparison of the previous works are illustrated in Table a.



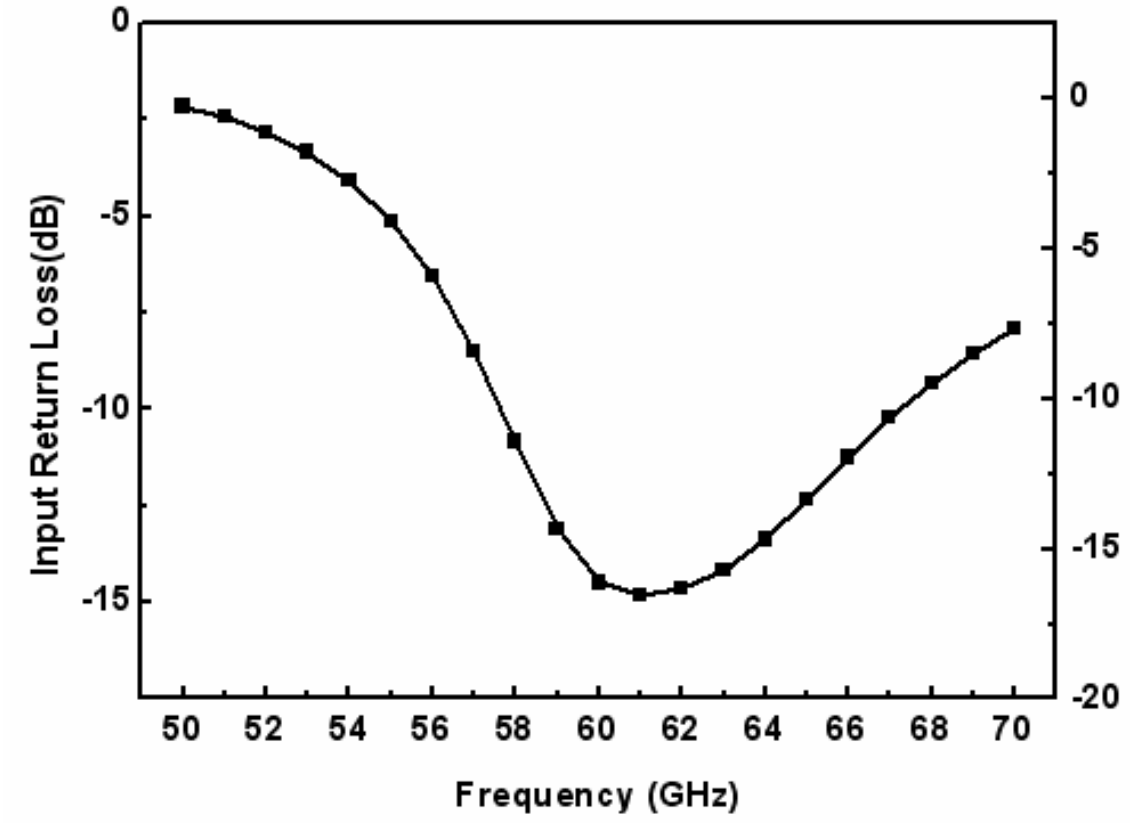
(a) The layout view of the re-designed receiver



(b) Simulated conversion gain and noise figure of the re-designed receiver



(c) Simulated P_{1dB} of the re-designed receiver



(d) Simulated R11 of the re-designed receiver

Table a Performance comparison with other 60-GHz receiver

	This work (Measured)	This work (Post-sim)	This work (re-design)	[4] JSSC 06'	[5] ISSCC 07'	[6] ISSCC 07'
Architecture	Homodyne	Homodyne	Homodyne	Homodyne	Heterodyne	Heterodyne
Frequency (GHz)	50.5 ~ 58.5	56.3 ~65.5	55.5 ~65	57.5~64	49.5~	57~63
Supply Voltage (V)	1.2	1.2	1.2	1.2	1.8	1.2
Chip Area (mm^2)	1.2	1.2	0.63	N/A	N/A	3.6
DC Power (mW)	11.4	5.9 + 8.5†	6.4+7.8†	9	56***	76.8**
CG (dB)	13.9	24.4	29.2	28*	31.5*	11.8
Noise Figure (dB)	9.2† †	7.7	7.6	12.5	6.9	10.4
P_{1dB} (dBm)	-12	-22.8	-25.8	-22.5	-25.5	-15.8
IF Amplifier	No	No	No	Yes	Yes	Yes
Technology	0.13 um CMOS	0.13 um CMOS	0.13 um CMOS	0.13 um CMOS	0.09 um CMOS	0.13 um CMOS

† Including tripler =receiver core + tripler (20 GHz VCO can be implemented by 8mW)

† † Modified simulation result

*Including IF amplifier

** Including 40-GHz VCO and divider

***Including 29-GHz VCO and doubler

By re-designing the circuit, the receiver can achieve the noise figure of 7.6 dB, a power gain of 29.2 dB and P_{1dB} of -25.8 dBm. It only consumes 14.2-mW power and the total chip area can be reduced to 0.63 mm^2. This is suitable for low-power and low noise 60-GHz system applications.

簡歷

姓名 ： 陳柏宏

生日 ： 1982 年 9 月 21 日

出生地 ： 台北市

E-mail ： hakko.ee94g@nctu.edu.tw

學歷 ：

國立新竹科學園區高級中學國小部	1989/9 ~ 1992/6
日本神奈川縣広畑小學	1992/6 ~ 1995/3
日本神奈川縣大根中學	1995/4 ~ 1996/6
新竹市立建華國中	1996/6 ~ 1998/6
國立新竹科學園區實驗高級中學	1998/9 ~ 2001/6
國立中山大學 電機工程學系	2001/9 ~ 2005/6
國立交通大學 電子研究所	2005/9 ~ 2007/7

論文名稱: 60 GHz 互補式金氧半導體射頻前端接收器之設計與分析

The Design and Analysis of 60-GHz CMOS Receiver Front-End