國　立　交　通　大　學

電子工程學系　電子研究所碩士班

碩　士　論　文

沉積後電漿處理對鉿類高介電常數材料熱穩定性之影響

The effects of plasma treatment on the thermal stability of Hf-based dielectrics

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中華民國 九十六年 七 月

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摘要

隨著金氧半場效電晶體的微縮，二氧化矽當作閘極介電層將面臨到物理限制。當互補式金氧半場效電晶體的閘極通道長度微縮到 100 奈米以下時，閘極介電層的有效電性厚度將縮小至 1.2 奈米以下，以二氧化矽當作氧化層將會面臨到很多的挑戰，影響最嚴重的就是超薄厚度之二氧化矽絕緣膜其直接穿遂電流將大到無可忍受的程度，因此需要高介電係數材料來取代二氧化矽作為閘極氧化層。高介電係數氧化層可以擁有較厚的物理厚度而維持相同的等效氧化層厚度來抑制穿遂電流的形成。其中鉿類為主的材料被認為是目前最有可能來取代二氧化矽。本實驗以鋁-HfO_2,$HfAlO_x$-矽之MIS結構為分析元件。首先，我們利用原子層沉積方法分別在矽晶片上沉積HfO_2和$HfAlO_x$，然後進行不同溫度的沉積後退火步驟，找出最適當的退火溫度。接著再分別進行表面電漿處理以及電漿後的退火步驟。最後，我們再進行 900 度 30 秒的高溫快速熱退火。我們利用量測C-V和I-V曲線去探討薄膜的基本特性。另外藉由磁滯效應、SILC特性、CVS測試和不同的sintering時間來討論經過電漿處理和沒有經過電漿處理元件的可靠度分析。我們可以發現經過電漿處理的試片可以承受較高的溫度卻不會降低原本的電容

值。這是因為電漿源中的氮原子可以抑制介電層和矽之間的氧化層成長。最後我們也可以發現$HfAlO_x$比HfO_2的熱穩定性較高，但是其電容值是比較低的。

The effects of plasma treatment on the thermal stability of Hf-based dielectrics

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ABSTRACT

The aggressive scaling of MOS devices is quickly reaching the fundamental limits of SiO_2 as the gate insulator. When the gate oxide thickness scales down below 1.2 nm for 100 nm-node CMOS technology and beyond and the SiO_2 will face severe challenges such as the direct-tunneling current. Therefore, high dielectric constant gate oxides with large physical thickness while identical equivalent oxide thickness (EOT) have been used to replace SiO_2 in order to reduce gate leakage current. Hf-based dielectric is a most suitable material for future MOSFET gate oxide applications. In this study, we analysis the Al/HfO_2 or $HfAlO_x$/Si MOS structure. First, we deposited HfO2 and $HfAlO_x$ on Si wafers individually by atomic-layer-deposition (ALD) system. Then, the films received different post-deposition-annealing temperature. After PDA, we had additional plasma treatment and post-nitridation annealing (PNA). Next, we treated the films with high temperature 900℃ 30 sec.

The electrical characteristics of the film were discussed by C-V and I-V curves. The reliability of the film with nitridation or not were discussed by hystersis effect, SILC(Stress Induce Leakage Current), CVS(Constant Voltage Stress) test, and

different sintering time. We could find that that the film with nitridation could sustain high thermal stress, and its capacitance did not decrease. It might be that nitrogen could suppress the formation of interfacial layer between the high-k/Si interface. Finally, we compare HfO_2 and $HfAlO_x$ films, we found that $HfAlO_x$ had better thermal stability for high crystallization temperature. But, its capacitance was smaller than HfO_2.

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Chapter 1

Introduction

1.1 Background

According to the recent prediction which was made by the Semiconductor Industry Association (SIA) in International Technology Roadmap for Semiconductors (ITRS) [1-3], the IC technology will continue its historical rate of advancement with Moore's law for at least a couple of decades. "Moore's Law", proposed by Gordon Moore in 1965, which states that " The number of transistors and resistors on a chip doubles every 18 months ", so it is needed to pursue better performance with lower cost. In order to achieve the goal, the scaling down of the device dimension is an inevitable tendency. The IC industry has been rapidly and consistently scaling down the design rule, increasing the chip and wafer size, and cleverly improving the design of devices and circuits for over 35 years [1-3]. In terms of the first order current-voltage relation, the driving current of a MOSFET can be given as

$$I_{dsat} = \frac{1}{2} C_g \mu_n \frac{W}{L_{eff}} (V_{GS} - V_t)^2 \qquad (1.1)$$

$$C_g = \kappa \varepsilon_0 \frac{A}{t_{inv}} \qquad (1.2)$$

Where V_{GS} is the applied gate to source, L_{eff} is the effective channel length, W is the

channel width, V_t is the threshold voltage, μn is the mobility for electrons, C_g is the gate capacitance, κ is the dielectric constant, ε_0 is the permittivity of free space and t_{inv} is the electrical film thickness. From the formula, to reach better current driving ability , we can reduce effective channel length, threshold voltage, or we can increase mobility, gate capacitance . However , some approaches will bring about serious shortcomings. For example, too large V_g will cause an undesirable high electric field across the gate oxide , which reduces the device reliability . Furthermore , the reduction of V_t about 200 mV is limited because of the induced statistical fluctuations in thermal energy at a typical operation circumstance of up to 100℃. Therefore, the reduction of gate oxide thickness and the shrinkage of the channel length are the simple ways to improve the device performance in the former two decades. Reducing the lateral L_{eff} and vertical t_{inv} dimensions of the device increases the current flow between the drain and source. This is because reducing t_{inv} increases C_g and the amount of channel charge; reducing L_{eff} decreases the distance from source to drain and let the channel charge travel fast. Reducing the gate oxide thickness t_{inv} along with the channel length L_{eff} also helps to improve short channel effects. Increased gate capacitance allows the gate potential to modulate more channel charge and is especially important as the supply voltage scales down. Much of the progress in silicon microelectronics has been driven by the ability to continually shrink these and other critical dimensions of the MOSFET to increase performance and decrease die area, a process referred to as scaling [4].

1.2 Scaling down of Oxide Thickness

According to the SIA (Semiconductor Industry Association) roadmap, CMOS with gate length below 70 nm will need an oxide thickness of less than 1.5 nm, which

corresponds to two or three layers of silicon dioxide atoms. Reducing the thickness of silicon dioxide to these dimensions would result in an exponential increase of direct tunneling current [5]. The resulting gate leakage current will increase the power dissipation and decrease the device performance and circuit stability for VLSI circuits. There are several kinds of conduction mechanisms of the leakage current passing through the oxide layer, which contain hot carrier injection、Fowler-Nordheim tunneling and direct tunneling. When the oxide thickness is less than 2 nm, the dominant leakage mechanism is direct tunneling. This results that the leakage current increase rapidly with the decrease of the oxide thickness. We can see the machine from (1.3)

$$I_{DT} \propto \exp -\left(\sqrt{\frac{2mq\phi}{\left(h/2\pi\right)^2}} T_{phys} \right) \qquad (1.3)$$

From Fig.1-2, when the equivalent oxide thickness (EOT) is 2 nm, the leakage current density of SiO_2 is 10^{-2} A/cm^2, which is lower than logic limit but higher than wireless limit. We could use SiON to replace SiO_2 and reduce the leakage current density about one order to make it lower than wireless limit. However, when the EOT is less than 2 nm, SiON also couldn't be used for wireless application. In addition, the leakage of SiO_2 even is larger than logic limit when the EOT is down to 1.5 nm. SiON also couldn't be used for logic application when the EOT is less than 1.3 nm. Therefore, we must use high-k materials instead of SiO_2 to be the gate dielectric. High-k dielectrics could effectively reduce the leakage current density about 4 orders. We also can see the gate leakage current of scaling down of SiO_2 from Fig.1-3.

In addition, we can compare the Roadmap of gate dielectric. Fig. 1-4 shows the

high-performance logic scaling-up of gate leakage current density limit and of simulated gate leakage due to direct tunneling. In 2007, the EOT (Effective Oxide Thickness) is about 1.1 nm and the leakage current density of the oxynitride is below the leakage limit line. However, after 2008, the EOT is below 1.0 nm and the oxynitride is incompetent to meet the limit on the gate leakage current density.

Fig.1-5 shows the low operating power (LOP) scaling-up of gate leakage current density limit and simulated gate leakage due to direct tunneling. In 2007, the EOT is only 1.2nm but the leakage current density of the oxynitride is still below the limit line because the application of high-performance logic could tolerate larger gate leakage current. However, after 2010, the oxynitride couldn't be used for high-performance logic anymore.

Fig. 1-6 shows the Low Standby Power scaling-up of gate leakage current density limit and simulated gate leakage due to direct tunneling. About this case we can notice that the oxynitride couldn't be used for Low Standby Power device anymore after 2007.

Table 1-1 is the roadmap of 2005 (update) ITRS (International Technology Roadmap for Semiconductor) for the high performance logic technology. According to the projection of the International Technology Roadmap for Semiconductors, an equivalent oxide thickness of less than 1.0 nm is required for sub-65-nm metal–oxide–semiconductor field-effect transistor (MOSFET) devices [11]. Due to a high tunneling leakage current, the scaling of SiO_2 below 1.0 nm with an acceptable leakage current level is very difficult. Recently, high-dielectric constant (high-k) oxide thin films have attracted great interest as a replacement for nitrided SiO_2 gate oxide films [7~10].

(1.2) can be rewritten as follows:

$$t_{high-k} = \frac{k_{high-k}}{k_{ox}} t_{eq} = \frac{k_{high-k}}{3.9} t_{eq} \quad (1.4)$$

From (1.4) we can see that if we increase the gate dielectric thickness and as usual retain the same Cg value, the leakage current problem could be solved.

1.3 High-k Materials

1.3.1 The advantages of High-k dielectric

High-k gate materials can maintain the same EOT with thicker physical thickness, and is therefore expected drastically reduced direct-tunneling current. From Fig1-7, the increased physical thickness significant reduces the probability of tunneling across the insulator, and hence, reduces the amount of off-state leakage current density. [12]

The relationship between dielectrics constant and thickness is followed:

$$EOT = \frac{k_{ox} \times t_{high-k}}{k_{high-k}} \quad (1.5)$$

A suitable replacement gate dielectric with a high permittivity (k) must exhibit low leakage current, have the ability to be integrated into a CMOS process flow, and exhibit at least the same equivalent capacitance, performance, and reliability of SiO_2.

1.3.2 Challenges of High-k Material

Although high-k material is expected to replace SiO_2 ideally, there are many problems to use high-k material practically. The issues for choosing a high-k material

may include：

(1) Low dielectric constant interfacial layer between substrate and high-k material

(2) Degradation of carrier mobility

(3) Shift of threshold voltage

(4) Thermal stability

(5) Boron penetration prevention

(6) Poly interface and poly gate electrode

(7) Compatibility with traditional CMOS process.

1.3.3 The choice of High-K materials

It is important to discuss the general requirements and challenges associated with different High-k materials as possible gate dielectrics. Issues to be discussed include processing, dielectric constant, capacitance, bandgap, tunnel current, and reliability. In the past three decades, SiO_2 has served as an ideal gate dielectric, its several advantages, such as being amorphous phase through the whole integration processing, high quality interface and good thermal stability, can indeed serve as a good guide of choosing high-k material. So, an ideal gate dielectric should meet the following requirements below:

Physical Properties

a. Suitable high k value (12~60)

A suitable k value is indispensable. Those with not enough high k value could not satisfy (1.3) to lower the leakage by increasing physical thickness.

While those with too high k value, in general, would suffer from thermal stability issues and larger fringing field.

b. Wide bandgap with conduction band offset > 1eV

It is found that most of the high-k materials do not have wide enough bandgap. In contact with silicon and gate electrode, the bandgap is closely related to the barrier height for carrier transport. Low bandgap will lead to intolerably high gate leakage (leakage current ~exp(-△Ec)) [13].

c. Thermodynamic stability in direct contact with silicon

Preserve capacitance of gate stack after processing.

d. Film morphology (amorphous) and stable process compatibility

In the VLSI process, the thermal budget is an important issue since high temperature changes dielectric phase. Once the gate dielectric material has transformed to polycrystalline from amorphous phase, the large grain boundaries would serve as leakage path, and induce large leakage current.

e. Gate material compatibility

Materials such as metal gate, and metals have been considered for better controllability and better performance.

Electrical Properties

(a)Low interface state density (Dit< $5x10^{10}/cm^2$-eV^{-1}), and SiO2-like mobility, The interface would affect the carrier mobility in the channel, and from (1.2), mobility degradation is related to poor current drivability. In high-k, there are so many sources that would reduce mobility, such as fixed charge, remote phonon, interfacial dipoles, remote surface roughness, surface roughness and phase separation crystallization. And most of them can be

avoided by improving process technology.

(b) T_{inv}<1nm,

(c) J<10^{-3}A/cm^2@ VDD,

(d) V_{FB} and hysteresis < 20mV,

(e) No C-V dispersion,

(f) Reliability issue.

To serve as a new gate dielectric, we must also take into consideration electrical reliabilities, such as stress-induced leakage current (SILC), time dependent dielectric breakdown (TDDB), hot carrier aging, bias temperature instability and charge trapping issues [15].

1.3.4 Why choose HfO_2-base

There are many kinds of high-k materials, including Al_2O_3, Y_2O_3, Ta_2O_5, TiO_2, ZrO_2 and HfO_2 etc. Table 1-2 lists basic characteristics of several high-k dielectrics. Unfortunately, many high-k materials such as Ta_2O_5, TiO_2, $SrTiO_3$, and $BaSrTiO_3$ are thermally unstable when directly contacted with silicon [16] and need an additional barrier layer which may add process complexity and impose thickness scaling limit. Also, materials with too low or too high dielectric constant may not be adequate choice for alternative gate dielectric application. Ultra high-k materials such as STO or BST may cause fringing field induced barrier lowering effect [17]. Materials with relatively low dielectric constant such as $A1_2O_3$ and Y_2O_3 do not provide sufficient advantages over SiO_2 or Si_3N_4 [18]. Among the medium-k materials compatible with silicon, oxides of Zr and Hf are attracting much attention recently. Especially, Hf forms the most stable oxide with the highest heat of formation (ΔHf = 27l Kcal/mol)

among the elements in IVA group of the periodic table (i.e. Ti, Zr, Hf). Unlike other silicides, the silicide of Hf can be easily oxidized [19]. HfO_2 possesses a dielectric constant of up to 25 [20], a large bandgap of 5.7 eV with sufficient band offset of larger than 1.5 eV [21], and well thermal stability in contact with silicon [22]. HfO_2 is very resistive to impurity diffusion and intermixing at the interface because of it's high density (9.68 g/cm^3) [23]. In addition, HfO_2 is the first high-k material showing compatibility with polysilicon gate process [24]. These properties make HfO_2 to be one of the most promising candidates for alternative gate dielectric application. Although inadequate mobility of HfO_2 MOSFETs is among the biggest concerns, various techniques have been explored to enhance the mobility. Introduction of strained silicon substrate [25], for example, drastically improved the mobility by changing the band structure of the substrate rather than changing the dielectric itself. However, the characteristics and mechanism of HfO_2 are not totally understood.

1.4 Plasma Nitridation

According to traditional view of improving SiO_2 device performance, we could find that nitridation is a common method to improve the interface. [26] Property with the result that there is often N_{it} or D_{it} in the interface, imperfect bonding of interface usually makes the characteristic of the device deteriorate. Such as charge will be trapped by the defects of the interface, it produce flat band voltage shift and also reduce mobility. Another shortcoming is that these dangling bonds will easily bond with oxygen atom in the following high temperature environment. The extra chemical reaction will let the interfacial oxide growth, and it will reduce the C value because of the lower dielectric constant. In addition, the quality of interfacial layer formed by oxidation is worse, and it would cause the problem of charge trapping. In order to solve these problems, nitridation treatment could let the atom of nitrogen bond with

these dangling bonds and fix it while entering the interface layer, and then improve the stability and reliability of interface. Consequently, nitridation treatment is a workable solution to improve interface quality. As we note before, the question about using high-k materials to replace SiO_2 is that there are too many defects in the interface to cause reliability degradation. Therefore, when we use high-k materials, it is consider that nitridation treatment is a more suitable way to improve reliability and thermal stability of device. These kind of treatment have already used in some relevant references. [27] [28] Among them, someone take nitridation treatment at high temperature, others take so-called plasma nitridation . According to [29], we could understand that the effect of plasma nitridation is better than thermal nitridation. The reason is that high-k materials could not sustain high thermal stress. As long as the temperature reaches certain degree, we would see the phenomenon of crystallization. The crystallization of dielectric would increase leakage current substantially, because it offers the path of leakage current. On the other hand, the meaning of plasma nitridation is to activate the source gas first. The high activation energy of radical will provide better mend which is better than nitridation at high temperature. For all these reasons, we adopt plasma nitridation in present experience.

1.5 Thesis Organization

Following chapters in the thesis are primarily organized as follow：

In chapter 2, we make a description of experimental details. Atomic Layer Deposition system is used to deposit hafnium-based materials on silicon surface.

In chapter 3, we discuss the characteristics of HfO_2 or $HfAlO_x$ insulator by Metal-Insulator-Semiconductor (MIS) capacitors.

In chapter 4, we discuss the reliability of HfO_2 or $HfAlO_x$ insulator by

Metal-Insulator-Semiconductor (MIS) capacitors and the effects of Post-Metallization-Annealing.

In chapter 5, we make the conclusions for this thesis and provide some suggestions for future work.

Chapter 2

Experiments of Al/HfO_2 and $HfAlO_x$ /Si MIS Capacitor

2.1 The way to prepare High-K thin film

There are several methods to prepare high-k thin films, such as chemical vapor deposition (i.e. ALCVD, MOCVD, PECVD etc.) [30]-[32] and physical vapor deposition (i.e. Sputtering, PLD etc.) [33][34]. ALCVD, MOCVD and Sputtering are the usual methods for preparing HfO_2 films. We will compare the ALD and sputter methods below.

2.1.1 ALCVD

The major difference between conventional chemical vapor deposition (CVD) and ALCVD (atomic layer CVD) arises from how precursors are introduced to the substrate and how the substrate surface is applied to control growth. In ALCVD, precursors are introduced alternatively to the substrate surface with an inert gas purge. The precursors are not allowed to be in contact with each other in the gas phase. This results in a surface controlled, layer-by-layer process for the deposition of thin films with atomic layer accuracy. Each atomic layer formed in the sequential process is a result of saturated surface controlled reaction. It provides well controlled growth of thin film and excellent step coverage. Fig. 2-1 shows how ALCVD Al_2O_3 and HfO_2

were deposited by ligand exchange reaction. Trimethyl aluminum Al(CH3)3 (TMA) and H2O were used for Al_2O_3 deposition and hafnium tetrachloride $HfCl_4$ and H_2O were used for HfO_2 deposition. Much more detail on the surface chemistry is presented elsewhere [35].

ALCVD Hf-based high-k materials have demonstrated the feasibility of EOT scaling down to 1 nm by using $HfAl_xO_y$ on nitrided surfaces [36]. HfO_2 with Al_2O_3 in it, such as $HfAl_xO_y$ or $HfO2/Al_2O_3/HfO_2$, shows much better scaling capability than only HfO_2. The physical defects observed in the thin HfO_2 will limit the physical thickness scaling. However, the charge trapping is worsened by the presence of Al_2O_3. It has been found that the interfacial layers and high-k bulk materials will increase the trap density. Some initial physical analysis data suggests the chemical oxide of SC1 might be a very promising way for EOT scaling of ALCVD high-k stacks because chemical oxide has been demonstrated as a good starting surface for ALCVD growth. The rapid thermal SiO_2 or SiON grown at the reduced partial pressure of reaction gases also is considered a possible solution for further reducing interfacial layer thickness. In the future, the project will focus on solving the charge trapping, mobility degradation of HfO_2 with Al_2O_3 in it. Furthermore, the flat band voltage shift after thermal process will be a problem. The uniformity and repeatability of HfO_2 is quite reasonable [36]. Currently, ALCVD is a very slow process. The deposition time for a 3 nm HfO_2 film is over 4 min without counting time for stabilization, pumping down and up, and wafer transfer. This would result in a total of 10–15 min for 2–4 nm HfO_2 deposition. The very slow throughput might be the major problem to use ALCVD tool for mass production.

2.1.2 DC Magnetron Sputtering

The usual HfO_2 film with DC magnetron sputtering method is reactively sputtered from an Hf target in an Ar + O_2 ambient onto Si substrate, then annealing in the furnace system. The advantages of the DC magnetron sputtering are simple and cheap. In addition, the HfO_2 film prepared by CVD system easily contains organic impurities and/or oxygen vacancies inside. This will cause leakage current through Frenkel-Pool effect or trap assisted tunneling [37]. Less contaminants are produced by the process of the sputtering because there is no other unnecessary chemicals. However, the uniformity of the DC sputtering is worse than that of the ALCVD in 12 inch diameter Si wafer. Furthermore, sputtering in an O_2 ambient easily produces SiO_2 interfacial layer. Therefore, we decide to use ALD to prepare our thin film.

2.2 Rapid Thermal Annealing system

METAL RTA-AG 610 was a single-wafer lamp-heated and computer-controlled rapid thermal processing (RTP) system. Water and compressed dry air (CDA) cooling system were used to cool down the quartz chamber. High intensity visible radiation heating and cold-heating chamber walls allow fast wafer heating and cooling rate. The tungsten halogen lamps were distinguished into five groups, and the relative percentage of lamp intensity can be adjusted individually for each group to achieve uniform temperature distribution. Temperature was obtained from pyrometer and precise controlled by computer. Two gas lines were used in the system which can be switched between Ar and N_2. Before RTA process started, one minute N2 gas purge was performed to minimize the water vapor introduced during wafer loading and also swept unwanted particles induced during process. A fast heating rate of 100℃/s was chosen in this work. When anneal was complete, chamber temperature was quickly cooled down from 900℃ to 500℃ by N_2 purge 30 seconds.

Then, the chamber was slowly cooled down to 280℃ without N2 purge to avoid creaking of films. After five minutes later, wafers can be taken out from the chamber. Films' creak can be avoided by two-steps-cooling method.

2.3 Plasma treatment system

When the PDA (Post-Deposition-Annealing) was finished, some samples were subjected to an additional plasma treatment in order to improve the electrical properties of gate dielectric. There were various source gas (N_2, N_2O) and process time (30 sec, 60 sec, 90 sec) as the experiment conditions. Parallel plate high-density plasma reactor employing an ICP source was a single-wafer treated and computer-controlled system.

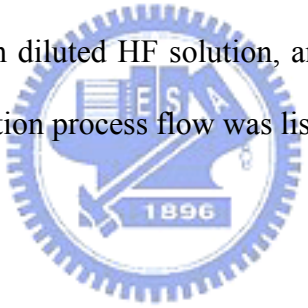
Fig. 2.2 illustrates ICP system that was used in this experiment. 13.56 MHz RF power was coupled to the top electrode through a matching network. After the sample load to reactor, the system was pumped down to keep the chamber clean enough. Subsequently, the source gas was become radical by the plasma system, as the chamber pressure was 100 mTorr and the substrate temperature was 300℃ so that to achieve the goal of low temperature process. The power of working plasma was kept constant at 200W and the flow rate of source gas was 100 sccm. While the process of plasma treatment was finished, these samples were brought to thermal treatment to reduce plasma damage.

2.4 MIS Capacitors Fabrication Process

In this thesis, Al/HfO_2/Si and Al/$HfAlO_x$/Si MIS capacitor were fabricated to study ultra thin HfO_2 and $HfAlO_x$ gate dielectrics. Figure 2-3 shows the fabrication flow of this experiment. The starting wafer was four inch (100) orientated p-type or

n-type wafer. It was one side polished and its resistivity was 5~10 ohm-cm.

After standard initial RCA cleaning, wafers were put into chamber and grew HfO_2 and $HfAlO_x$ layer with atomic layer deposition system. After the thin films were prepared, some samples were annealed after deposition (post-deposition anneal) and then subjected to an additional plasma treatment at the substrate temperature of 300℃ while the pressure was 100 mTorr and the plasma power was 200W. The plasma treatment conditions were in pure N_2 and N_2O for 30 sec, 60 sec, and 90 sec respectively and the flow rate were 100 sccm. After nitridation, we also annealed these samples to reduce the plasma damage. Finally, pure aluminum films were thermally evaporated on the top side of wafers. Mask defined the top electrode. Then, we used wet etching to etch undefined Al and HfO_2 films. After patterning, backside native oxide was stripped with diluted HF solution, and Al was deposited as bottom electrode. The detailed fabrication process flow was listed as follows.



1. Initial RCA cleaning.

2. Atomic layer deposition HfO_2 and $HfAlO_x$.

3. Post-deposition anneal with 600℃ for HfO_2 and 800℃ for $HfAlO_x$.

4. Plasma treatment with N_2 ，N_2O plasma for 30 sec, 60 sec, 90 sec respectively.

5. Post-nitridation annealing with 600℃-30sec.

6. Thermally evaporate 4000 Å aluminum as the top electrode.

7. Mask: define top electrode and then wet etch undefined Al and HfO_2 films.

8. Strip backside native oxide and coat 4000 Å aluminum as bottom electrode.

After the Al/HfO_2 or $HfAlO_x$ /Si MIS capacitors were prepared, we used semiconductor parameter analyzer (HP4156A) and C-V measurement (HP4284) to analysis electric characteristics (i.e. I-V, C-V, EOT, leakage current density etc.). Then we tested their reliability, including stress induced leakage current (SILC), constant current stress(CCS), constant voltage stress (CVS), Hysteresis effect.

Chapter 3

Electrical Characteristics of Al/HfO_2 or $HfAlO_x$/Si MIS Capacitors

3.1 Electrical Characteristics with different post-deposition annealing temperature

3.1.1 Capacitance-Voltage Characteristics FOR HfO_2

In order to measure the C-V characteristics of our MIS capacitors, we used HP 4284A precision LCR meter in our experiments. We swept the gate bias from accumulation region to inversion region to obtain the curve at the frequency of 50 kHz from -2V to 0V. First, the effects of different PDA (post deposition annealing) will be discussed.

Fig. 3-1 shows the capacitance-voltage (C-V) characteristics of HfO_2 gate dielectric anneal with different temperature for 30 sec. The capacitors of PDA (400℃, 500℃, 600℃) show higher capacitance than the original sample. In addition, the capacitor of PDA (850℃) shows the worse C-V curve, because HfO_2 could not sustain the high temperature anneal over 600℃. The best PDA temperature range is about 400℃~600℃.

3.1.2 Current-Voltage Characteristics FOR HfO_2

The leakage current of our MIS capacitors were analyzed from the current -voltage (I-V) characteristics measured by an HP4156A semiconductor parameter analyzer.

Fig. 3-2 shows the J-V characteristics of HfO_2 gate dielectrics anneal with different temperature for 30 sec from 0V to -2V. We observed that with suitable temperature annealing, the leakage current density can be decreased, because PDA could make the thin film dense. The leakage current density of the sample (PDA-850℃) is larger owing to the crystallization-induced leakage current.

3.1.3 Capacitance-Voltage Characteristics FOR $HfAlO_x$

Fig. 3-3 shows the capacitance-voltage (C-V) characteristics of $HfAlO_x$ gate dielectrics anneal with different temperature for different process time. PDA could reduce the flat-band voltage and make the thin film dense. From Fig 3-3 we think that the suitable annealing temperature is about 600℃~800℃. The C-V curves of those samples over 900 ℃ are a little distorted.

3.1.4 Current-Voltage Characteristics FOR $HfAlO_x$

Fig. 3-4 shows the J-V characteristics of $HfAlO_x$ gate dielectrics anneal with different temperature for different process time from 0V to -2V. The gate leakage current density of these samples (600℃, 800℃) could be decreased, because the film became dense after PDA. The leakage current of those samples (PDA over 900℃) are large, it might be caused by crystallization.

For reasons mentioned above, we would use the 600℃ to be as the PDA temperature for HfO_2 and the 800℃ for $HfAlO_x$.

3.2 Electrical Characteristics with different plasma

treatment for different process time

There are two kinds of plasma treatment with different source gas (i.e. N_2, N_2O) and they were treated for different process time (i.e. 30 sec, 60 sec and 90 sec). First, the relationship of difference process time in one kind of plasma treatment will be discussed. Then we compare the effect of different source gas.

3.2.1 Capacitance-Voltage Characteristics FOR HfO_2

Fig 3-5 shows the capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics treated with N_2 plasma treatment for different process time. The capacitor treated for 90 sec shows the maximum capacitance among these conditions of process time. Furthermore, the capacitor treated for 30 sec and 60 sec both show the good capacitance values which are larger than the capacitor which was not treated by N_2 plasma.

Fig. 3-6 shows the capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics treated with N_2O plasma treatment for different process time. Just like the samples of N_2 plasma treatment. The improvement of capacitance could be seen. At this condition, the capacitance treated with N_2O plasma for 90 sec shows the largest value. By the way, all the samples which use N_2O plasma have larger capacitance than the sample without treatment. It is indicated that N_2O plasma treatment is also a practicable method to improve the capacitance-voltage characteristics of HfO_2 gate dielectrics.

3.2.2 Current-Voltage Characteristics FOR HfO_2

Fig. 3-7 shows the J-V characteristics of p-type HfO_2 capacitors treated by N_2 plasma with different process time from 0 V to -2 V. We observed that the gate

leakage current density is suppressed while treatment conditions are 60 sec and 90 sec. It is indicated that N_2 plasma treatment supply an effective barrier against the leakage current. The film after N_2 plasma treatment became dense and strong, so the leakage current could be effectively decreased, especially for capacitor which treated with N_2 plasma 90 sec and it also has the lowest leakage and largest capacitance value from Fig. 3.5. Gate leakage current density of no treatment insulator at VG = -1 V is about 1×10^{-7} A/cm^2. From Fig.3-5, however, gate leakage current density of the capacitor treated for 90 sec N_2 plasma at VG = -1 V is about 1×10^{-8} A/cm^2. It has less gate leakage than no treatment insulator about 1 order. Furthermore, we notices that the capacitor treated with N_2 plasma for 30 sec has high leakage current, it is might be that the N_2 plasma is too little time to react with the film and caused by plasma damage.

Fig. 3-8 shows the J-V characteristics of p-type HfO_2 capacitors treated by N_2O plasma with different process time from 0V to -2V. After N_2O plasma treatment, we could see the reduction of leakage current in contrast of no treatment samples. However, the sample of plasma treated for 90 sec got the small gate leakage current and a good C-V curve from Fig 3-6. Relative to the case of N_2 plasma, we could see that the level of leakage current increasing obviously mitigate. It is possibly due to the additional oxidation layer formed by oxygen radical. The interfacial oxidation layer will let the dielectric thicker to prevent from gate leakage.

Fig. 3-9 and Fig.3-10 shows the capacitance-voltage (C-V) and J-V characteristics of HfO_2 gate dielectrics treated with N_2 plasma treatment for 90 sec and N_2O plasma treatment for 90 sec. It is indicated that the capacitance treated with N_2 plasma for 90 sec shows the most excellent value (i.e. 50% increasing about capacitance). Among these samples, the reason why the sample treated with N_2O plasma has lower capacitance than N_2 plasma treatment is complex. It is may be the

growing of interfacial oxide made the C value smaller and this interfacial layer also made the gate leakage current smaller.

3.2.3 Capacitance-Voltage Characteristics FOR $HfAlO_x$

Fig. 3-11, Fig. 3-12 shows the C-V curves for MOS capacitors with nitridation by N_2 and N_2O plasma of 200 W at different time. The capacitance density of $HfAlO_x$ nitrided by N_2 plasma 30 sec and N_2O plasma 30 sec are largest. Plasma nitridation (N_2, N_2O) at 30 sec could more effectively increase the dielectric constant of $HfAlO_x$. The passivation effect of plasma nitridation could decrease the flatband voltage of C-V curve. From Fig. 3-11, when the N_2 plasma process time over 60 sec, the C value will become smaller, we think that it is may be caused by the growing of interfacial oxide in the plasma process time. The same phenomenon is also found on N_2O plasma from Fig 3-12.

3.2.4 Current-Voltage Characteristics FOR $HfAlO_x$

Fig. 3-13 shows the J-V characteristics of p-type $HfAlO_x$ capacitors treated by N_2 plasma of 200W with different process time from 0V to -2V.We observed that the gate leakage current density is suppressed while treatment conditions are 30 sec and 60 sec. The film after nitridation with N_2 plasma became dense and strong, so the leakage current could be effectively decreased, gate leakage current density of no treatment sample at VG = -1 V is about 1×10^{-5} A/cm^2, gate leakage current density of the capacitor treated for 30 sec N_2 plasma at V_G = -1 V is about 1×10^{-7}~1×10^{-8} A/cm^2. It has less gate leakage than no treatment insulator about 2~3 order. Furthermore, we found that the 90 sec nitrided sample has high leakage current, it is maybe caused by plasma damage.

Fig. 3-14 shows the J-V characteristics of p-type $HfAlO_x$ capacitors treated by

N_2O plasma with different process time from 0 V to -2V. After N_2O plasma treatment, we can see the reduction of leakage current in contrast of no treatment samples. It is worthy to be noticed that all the capacitors treated by N_2O plasma have a low leakage current about 1×10^{-8} A/cm^2 at Vg = -1V. Relative to the case of N_2 plasma, we can see that the level of leakage current decreased obviously. It is maybe due to the additional oxidation layer formed by oxygen radical. The interfacial oxidation layer will let the dielectric thicker to prevent from gate leakage.

Fig. 3-15 and Fig. 3-16 shows the capacitance-voltage (C-V) and J-V characteristics of $HfAlO_x$ gate dielectrics treated with N_2 plasma treatment for 30 sec and N_2O plasma treatment for 30 sec. It is indicated that the capacitance treated with N_2 plasma treatment for 30 sec shows the better C-V curve.

As a consequence, the N_2 and N_2O plasma treatment all shows better electrical properties than no treatment sample. Furthermore, the N element and O element all could fix the interface and improve the electrical properties include of C-V curve and J-V curve. But for the reason of oxidation caused by oxygen radical, the N_2O plasma treatment samples show the lower C value.

3.3 Electrical Characteristics with different steps for PDA and post-plasma treatment anneal

3.3.1 Capacitance-Voltage and Current-Voltage Characteristics FOR HfO_2

Fig 3-17, Fig 3-18 shows the the C-V and J-V characteristics of HfO_2 gate dielectrics treated with different steps of post-plasma treatment anneal and PDA. As

show in Fig. 3-17, the sample without nitridation can not sustain the high temperature annealing, so nitridation can improve the thermal stability of high-k film. In addition, we observe that the C-V curve of the sample without PDA and treated by N_2 plasma directly is distorted at high negative bias voltages owing to the crystallization, we could see that after post deposition anneal, nitridation could effectively improve the thermal stability of the thin film. From Fig. 3-18, we can find the same result, the sample with nitridation after PDA can effectively decrease gate leakage current. It is good evidence to show that the thin film treated by N_2 plasma after post-deposition anneal can make the thin film sustain high thermal stress.

Fig 19, Fig 20 shows the capacitance-voltage (C-V) and J-V characteristics of HfO_2 gate dielectrics after different PDA temperature and different PNA temperature. The sample with PDA 600℃ and PNA 600℃ has the better C-V curve and lower leakage current.

Fig 21, Fig 22 shows the capacitance-voltage (C-V) and J-V characteristics of HfO_2 gate dielectrics after nitridation and 900℃ 30 sec thermal treatment. The capacitor with PDA 600℃ and after plasma treatment annealing 600℃ certainly has the better C-V curve and lower leakage current. But, the capacitance value decreased at negative bias, this was caused by the additional interfacial layer during the thermal process. However, it is particularly noteworthy that nitridatuon can let the HfO_2 gate dielectric sustain high temperature (900℃) thermal treatment. Compare to Fig 3-1, the film without nitridation will breakdown after high temperature (over 800℃) thermal treatment.

3.3.2 Capacitance-Voltage and Current-Voltage Characteristics FOR $HfAlO_x$

Fig. 3-23 shows the capacitance-voltage (C-V) characteristics of $HfAlO_X$ gate dielectrics after post-deposition annealing and plasma treatment annealing. First, we can find that the sample without PDA and treated with N_2 plasma directly, its C-V curve is distorted. It might be cause by plasma damage, therefore we must add the post-nitridation anneal step to restore the plasma damage. In addition, the C-V curve of the sample with PDA and PNA is better than others. Fig 3-24 shows the J-V characteristics of $HfAlO_x$ gate dielectrics after post-deposition annealing and plasma treatment annealing. The sample with nitridation, whose gate leakage current is lower than original one. The phenomenon is similar with HfO_2.

Fig. 3-25 shows the capacitance-voltage (C-V) characteristics of $HfAlO_x$ gate dielectrics treated with different PNA. In Fig. 3-25, the C-V curve of the sample with PNA 400℃ is distorted, it might be the PNA temperature is too lower to restore the plasma damage. Fig. 3-26 shows the J-Vcharacteristics of $HfAlO_x$ gate dielectrics treated with different PNA. The gate leakage current of all the samples with nitridation is smaller than the original sample.

Fig. 3-27 shows the capacitance-voltage (C-V) characteristics of $HfAlO_x$ gate dielectrics after nitridation and 900℃-30 sec thermal treatment. The C-V curve of the sample with PDA 800℃ and PNA 600℃ is the best. Furthermore, the C–V distortion of the $HfAlO_x$ films with only RTA was observed at a high gate bias owing to the crystallization-induced leakage current. Fig 3-28 shows the J-V characteristics of $HfAlO_x$ gate dielectrics after nitridation and 900℃-30 sec thermal treatment. It shows that the sample without nitridation could not sustain high thermal stress and the gate leakage current would become large after high temperature process. Therefore, nitridation could effectively improve the thermal stability of high-k thin film.

Chapter 4

Reliability of Al/HfO_2 or $HfAlO_x$/Si MIS Capacitors

4.1 Hysteresis

When a ferromagnetic material is magnetized in one direction, it will not relax back to zero magnetization when the applied magnetizing field is removed. It must be driven back to zero by the additional opposite direction magnetic field. If an alternating magnetic field is applied to the material, its magnetization will trace out a loop called a hysteresis loop. The lack of retrace ability of the magnetization curve is the property called hysteresis and it is related to the existence of magnetic domains in the material. Once the magnetic domains are reoriented, it takes some energy to turn them back again [38]. The hysteresis phenomenon is similar in the C-V curve of the MIS capacitor device. When we apply a voltage in opposite direction, it will not fit the original C-V curve measured previously. It is due to the traps of interface which would trap charges to influence the flat band voltage and C-V curve. [39]

Fig. 4-1 shows the hysteresis of p-type HfO_2 gate dielectric which was deposited by sputter system without plasma treatment. Fig. 4-2 shows the hysteresis of p-type HfO_2 gate dielectric which was deposited by atomic layer deposition system without plasma treatment. We see that, the hysteresis of the thin film deposited by ALD is smaller than the thin film deposited by sputter system. It is a good way to use ALD to deposit Hf-base dielectric, because its interfacial trap density is smaller than the sample deposited by sputter system.

Fig. 4-3 shows the hysteresis of p-type HfO_2 gate dielectrics (ALD) with PDA 600℃-30 sec、nitridation、PNA 600℃-30 sec and 900℃-30 sec. The hysteresis is also small after 900℃ annealing, so nitridation could decrease the trap density and let the thin film sustain high thermal stress.

Fig. 4-4 shows the hysteresis of n-type $HfAlO_X$ gate dielectrics (ALD) without plasma treatment and Fig. 4-5 shows the hysteresis of n-type $HfAlO_X$ gate dielectrics (ALD) with PDA 600℃-30 sec、nitridation、PNA 600℃-30 sec and 900℃-30 sec. The tendency of hysteresis is similar with the case of HfO_2. As a consequence, the plasma treatment can improve the reliability of gate oxide. The limit of hysteresis for transistor in the future generation is less than 10 mV under high frequency C-V measurement. It seems we could use atomic layer deposition to deposit the Hf-base thin film to decrease hysteresis of Hf-base device.

4.2 Stress Induced Leakage Current (SILC)

In order to investigate the reliability of MIS capacitor device, the stress induced leakage current (SILC) is a common and simple experiment. The additional stress would induced trap density in the bulk or interfacial layer. The trap density would introduce another leakage path. Fig. 4-6 shows the SILC curve of p-type HfO_2 gate dielectrics treated with N_2 plasma for different PDA and PNA temperature. First, we used constant voltage (2V) for 60 sec, but SILC did not increase. Therefore, we use constant voltage (3V) for 60 sec to stress the thin film. After the stress of constant voltage (3V) for 60 sec, the gate leakage current become larger then before. The degree of leakage current degradation can be judged for the reliability of MIS capacitor. From Fig. 4-6, it shows the film after high temperature treatment, the quality would become worse, but it was better than the sample without nitridation.

Second, it is considered that the SILC of sample (800 ℃-30 sec + N_2 plasma treatment + 600℃-30 sec + 900℃-30 sec) which has the best C-V curve and the lowest leakage shows a small degradation. On the other hand, it is also can be noticed that the SILC of other samples is large.

Fig. 4-7 display the SILC curve of n-type $HfAlO_x$ gate dielectrics treated with N_2 plasma treatment for different PDA and PNA temperature. First，we use constant voltage (3V) for 60 sec to stress the thin film, but we found that the thin film could not sustain the gate voltage stress, the SILC of all the samples were very large, so we use (2V) for 60 sec to replace the original ones. In Fig. 4-7, it was indicated that the SILC of the sample (800 ℃- 30 sec + N_2 plasma treatment + 600℃-30 sec + 900℃-30 sec) was the smallest. The leakage current of other samples after stress were larger than original ones. So, nitridation can decrease the SILC degradation effectively.

4.3 Constant Voltage Stress (CVS)

To study the reliability of thin films, we can stress the samples with a constant voltage or a constant current, which are useful methods. The mechanism of CVS is the charge trapped by the interfacial trap density which is caused by stress for a long time. In addition, the increasing interface trap density would cause new leakage path to add leakage current. In our experiments, we use constant voltage stress (CVS) to test the reliability of the thin film. Fig. 4-8 shows gate current shift of p-type HfO_2 gate dielectrics treated with N_2 plasma treatment for different annealing process during CVS with V_g = 2 V. It indicated that the thin film with N_2 plasma treatment which current shift was smaller than the original one. The sample with N_2 plasma treatment after the 900℃annealing also had smaller current shift. Fig. 4-9 shows gate current shift of n-type $HfAlO_x$ gate dielectrics treated with N_2 plasma treatment for

different process annealing during Vg = -2 V CVS. It had similar behavior like the previous experiment. The gate leakage shift level of the samples with or not nitridation differed about 4 orders, so nitridation process could decrease the trap density effectively. It might be a good way to incorporate N atoms in the thin film to improve the reliability of the gate dielectrics.

4.4 Sintering

The purpose of sintering is to reduce the contact resistant, but we found that long sintering time would reduce the reliability of Hf-base thin film. Fig. 4-10, Fig. 4-11 shows the capacitance-voltage (C-V) and J-V characteristics of p-type HfO_2 gate dielectrics with different sintering time. As shown in Fig.4-10 and Fig.4-11, the capacitance of the sample with sintering 10 minute would decrease and its gate leakage current was almost the same with the original sample. However, when the sintering time was over 10 minute, the C-V curve would distort and its leakage current was very large, so the HfO_2 thin film could not sustain high thermal budget.

Fig. 4-12 the capacitance-voltage (C-V) characteristics of p-type HfO_2 gate dielectrics with different sintering time after PDA and Fig. 4-13 shows the J-V characteristics of p-type HfO_2 gate dielectrics with different sintering. We could also find that as the sintering time increased, the capacitance would become smaller and the gate leakage current would become large. In addition, when the sintering time over 10 minute, the gate oxide would be breakdown and the gate leakage current was very large.

Fig. 4-14 shows the capacitance-voltage (C-V) characteristics of n-type $HfAlO_X$ gate dielectrics with different sintering time and Fig. 4-15 shows the J-V characteristics of p-type $HfAlO_x$ gate dielectrics with different sintering time. As

shown in Fig.4-14 and Fig. 4-15, the samples with sintering over 20 min would get worse performance. So, we could find that the thermal stability of $HfAlO_x$ is better than HfO_2. Furthermore, as the sintering time increased, the capacitance would become low, it could be cause by additional interfacial layer during sintering.

Fig. 4-16 shows the capacitance-voltage (C-V) characteristics of n-type $HfAlO_x$ gate dielectrics with different sintering time after PDA and Fig. 4-17 shows the J-V characteristics of p-type $HfAlO_x$ gate dielectrics with different sintering time after PDA. We could find that the capacitance of the samples after PDA would not change greatly. It might be that the PDA could make the thin film dense and improve thermal stability.

Compare to the HfO_2 and $HfAlO_x$, we could find that $HfAlO_x$ had better thermal stability, but it had small capacitance.

Chapter 5

Conclusions and Future work

5.1 Conclusions

In this thesis, we performed that the quality of Hf-base thin film could be improved by the post-deposition annealing (PDA) and the post plasma treatment (PNA). The plasma treatment conditions are N_2, N_2O plasma for 30 sec, 60 sec, 90 sec individually. We find several important phenomena and they would be summarized as follows.

First, improvement in the electrical characteristics of Al/HfO_2 or $HfAlO_X$/Si MIS capacitors after post-deposition-annealing has been demonstrated in this work. The Hf-base thin film after PDA would become dense and we could find their capacitance would increase and gate leakage current would decrease.

Second, all of the samples after plasma treatment can promote the electrical characteristics and reliability until the plasma damage happened. Among these treatments, the sample treated by N_2 plasma 90 sec for HfO_2 and N_2 plasma 30 sec for $HfAlO_x$ represented a fairly great improvement, such as good capacitance (40% increasing for HfO_2 and 10% increasing for $HfAlO_x$), reduced leakage current (about 2 order reduction for all samples). It was showed that the interfacial layer could be suppressed and the weak structure of interface has been repaired by N_2 plasma respectively. The sample treated by N_2 plasma also showed excellence promotion about reliability issues, such as smaller hysteresis (< 10 mV), smaller SILC, better

CVS curve, and larger V_{BD}. However, N_2O plasma treatment also can provide good effects on electrical characteristics. The samples treated N_2O plasma treatment would introduce oxygen bonding to form additional interfacial layer, so the capacitance would be decreased. However, the thicker interfacial layer became a good resistance against leakage current. Furthermore, we could find that the $HfAlO_X$ had better thermal stability than HfO_2 from different sintering time. In addition, we compare the HfO_2 thin films, one was deposited by sputter and the other was deposited by ALD. The sample deposited by ALD had better C-V curve.

Finally, in this thesis, it has been indicated that the post-deposition annealing and the treatment of N_2 plasma could improve thermal stability of Hf-based thin film. Simultaneously, the reliability of the film after nitridation also represented better electronic characteristics. The most suitable way for post-deposition treatment by plasma to improve electrical characteristics on MIS structure has been observed.

5.2 Future work

The interfacial layer between high-k/Si would be increased by increasing post-deposition-annealing temperature. In order to suppress the growth of the interfacial layer, we could use some pre-treatment methods to introduce a thin oxide or nitride layer by HDP-PECVD or chemical deposition. Furthermore, we might have to understand the mechanism of leakage current of thin film and thick film individually. Finally, the mechanism of the generation of the defects in the high-k bulk or interface still needs to be solved.

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Table

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
L_g: Physical L_{gate} for High Performance logic (nm) [1]	32	28	25	22	20	18	16	14	13
EOT: Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	12	11	11	9	7.5	6.5	5	5	
UTB FD (Å)				9	8	7	6	5	5
DG (Å)							8	7	6
Gate Poly Depletion and Inversion-Layer Thickness [3]									
Extended Planar Bulk (Å)	7.3	7.4	7.4	2.9	2.8	2.7	2.5	2.5	
UTB FD (Å)				4	4	4	4	4	4
DG (Å)							4	4	4
EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
Extended Planar Bulk (Å)	19.3	18.4	18.4	11.9	10.3	9.2	7.5	7.5	
UTB FD (Å)				13	12	11	10	9	9
DG (Å)							12	11	10
$J_{g,limit}$: Maximum gate leakage current density [5]									
Extended Planar Bulk (A/cm^2)	1.88E+02	5.36E+02	8.00E+02	9.09E+02	1.10E+03	1.56E+03	2.00E+03	2.43E+03	
FDSOI (A/cm^2)				7.73E+02	9.50E+02	1.22E+03	1.38E+03	2.07E+03	2.23E+03
DG (A/cm^2)							6.25E+02	7.86E+02	8.46E+02
V_{dd}: Power Supply Voltage (V) [6]	1.1	1.1	1.1	1	1	1	1	0.9	0.9
$V_{t,sat}$: Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	195	168	165	160	159	151	146	148	
UTB FD (mV)				169	168	167	170	166	167
DG (mV)							181	184	185
$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]									
Extended Planar Bulk (µA/µm)	0.06	0.15	0.2	0.2	0.22	0.28	0.32	0.34	
UTB FD (µA/µm)				0.17	0.19	0.22	0.22	0.29	0.29
DG (µA/µm)							0.1	0.11	0.11
$I_{d,sat}$: effective NMOS Drive Current [9]									
Extended Planar Bulk (µA/µm)	1020	1130	1200	1570	1810	2050	2490	2300	
UTB FD (µA/µm)				1486	1625	1815	2015	2037	2198
DG (µA/µm)							1899	1932	2220
Mobility Enhancement Factor for $I_{d,sat}$ [10]									
Extended Planar Bulk	1.09	1.09	1.08	1.09	1.10	1.10	1.12	1.11	
UTB FD				1.06	1.06	1.06	1.06	1.05	1.05
DG							1.05	1.04	1.05
Effective Ballistic Enhancement Factor [11]									
Extended Planar Bulk	1	1	1	1	1	1	1	1	
UTB FD				1	1	1	1	1	1.1
DG							1.17	1.25	1.31

Table 1-1 High-performance Logic Technology Requirements Roadmap.

(ITRS：2005 updae)

Material	SiO_2	Si_3N_4	Al_2O_3	HfO_2	ZrO_2	La_2O_3	Ta_2O_5	TiO_2	Pr_2O_3	$SrTiO_3$
K value	3.9	7.1	9	25	29	30	26	95	31	200
Bandgap (eV)	9	5.3	8.8	6	5.8	6	4.4	3.1	4.2	3.3
E_{bd} (MV/cm)	10	15	13.8	6.7	5.7	5.6	3.7	2.5	3.4	2.2

Table 1-2 Characteristics of various high-k materials.

Figure-chapter 1

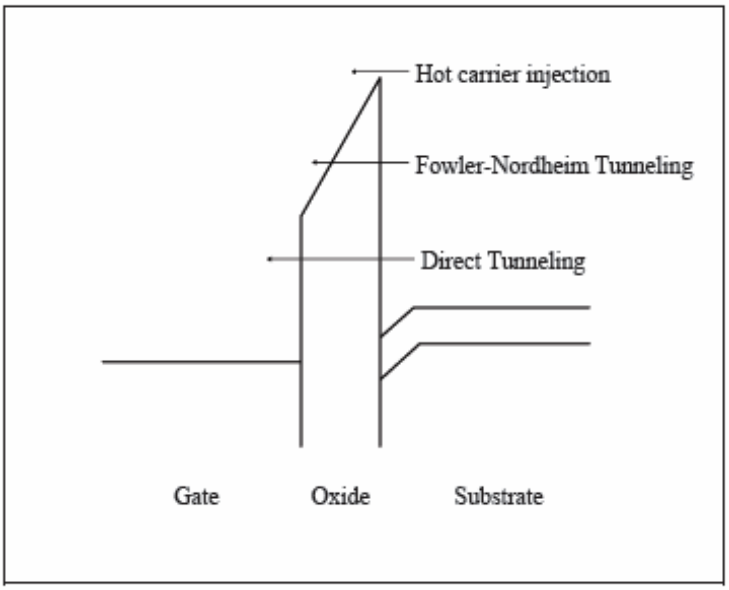


Fig. 1-1 Conduction mechanism in oxide for the MOS structure.

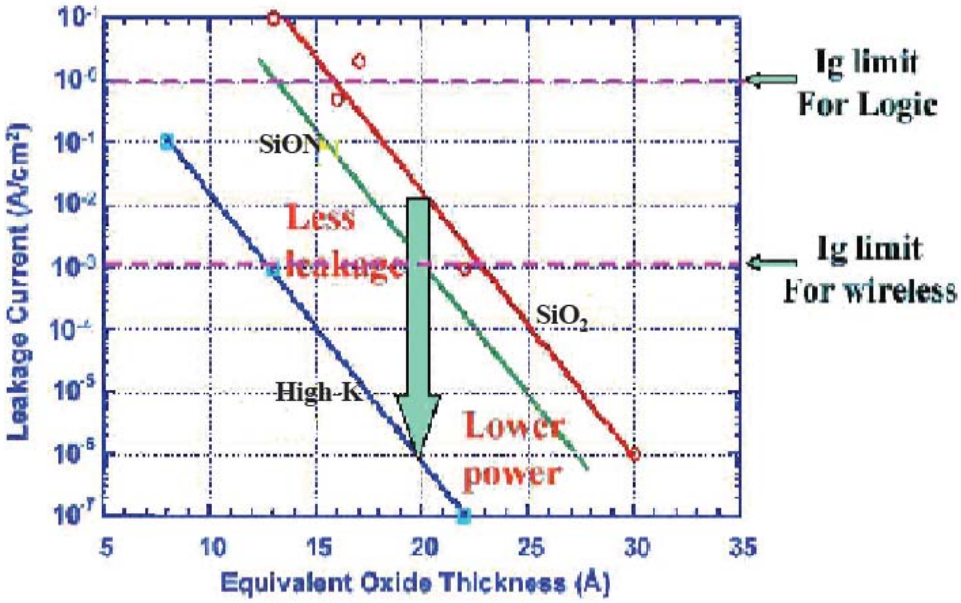


Fig. 1-2 Gate leakage reduction by high-k dielectric.

(B-Y Nguyen, 6th TRC October 27-28, 2003 *Motorola*)

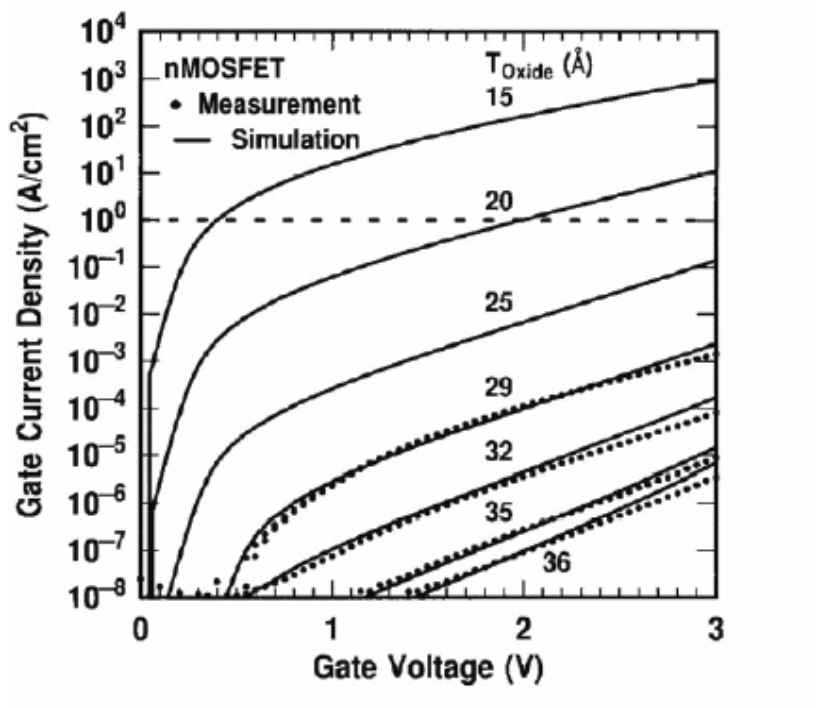


Fig. 1-3 Measured and simulated Ig-Vg characteristics under inversion condition form MOSFETs. The dotted line indicates the 1A/cm^2 limit for the leakage current. [6]

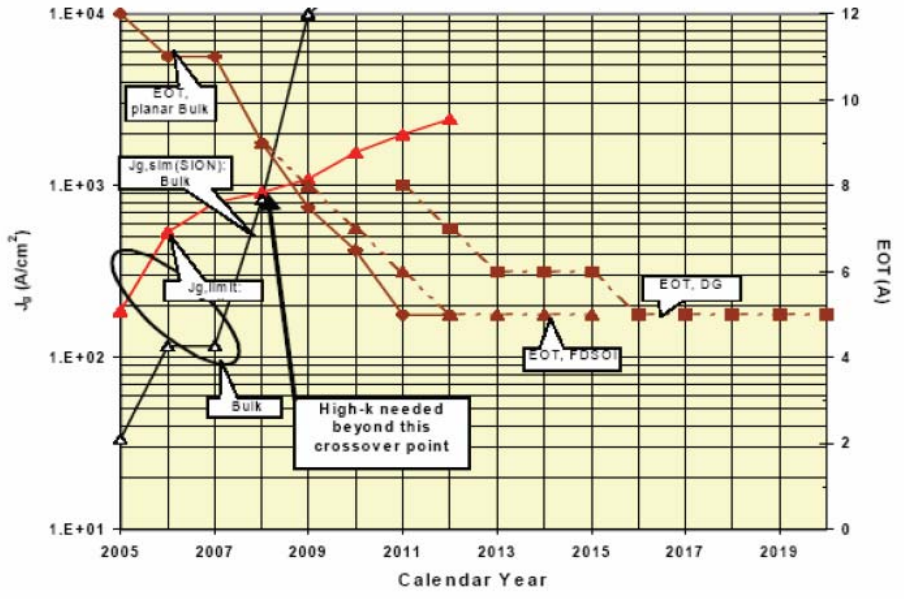


Fig. 1-4 Jg, limit versus Jg, simulated for High-Performance Logic (ITRS: 2005 update)

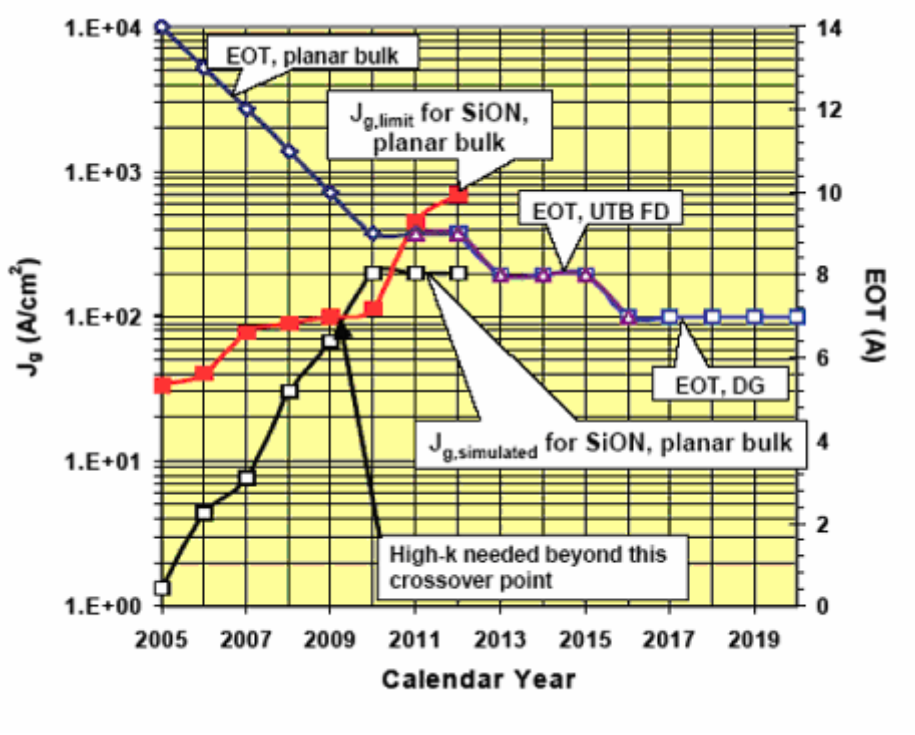


Fig. 1-5 Jg,limit versus Jg,simulated for Low Operating Power

(ITRS: 2005 update)

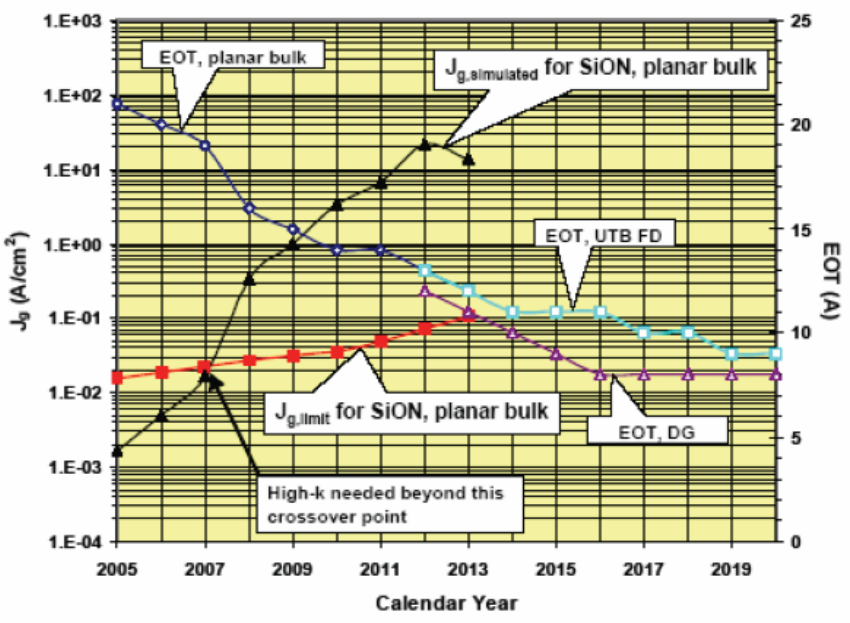


Fig. 1-6 Jg,limit versus Jg,simulated for Low Standby Power

(ITRS: 2005 update)

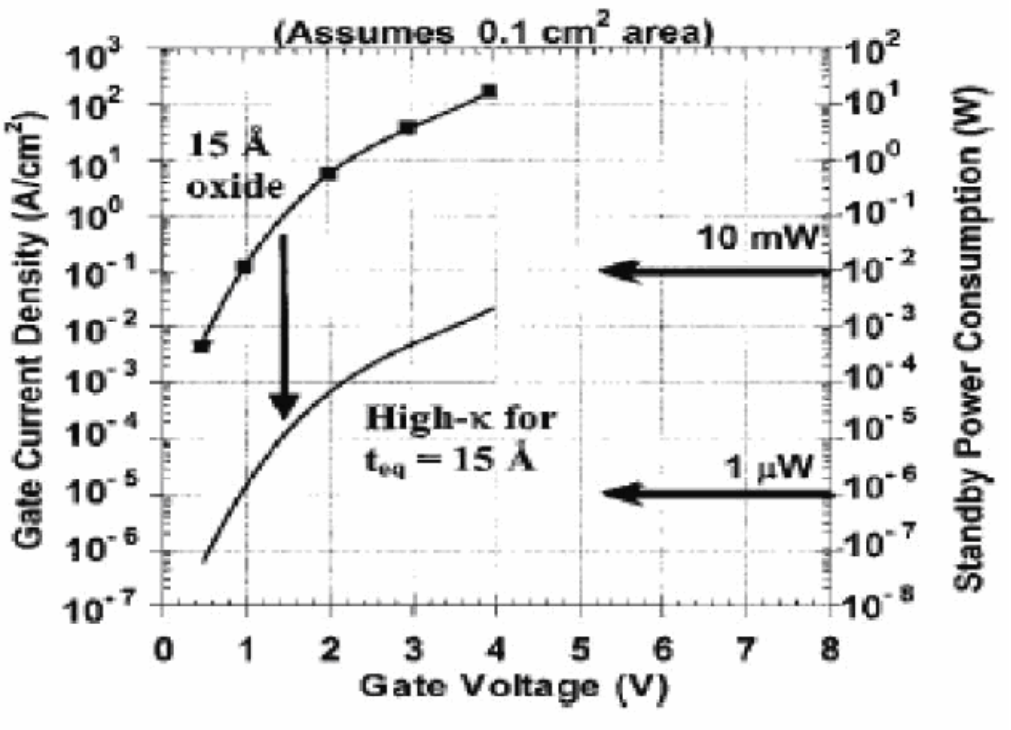


Fig. 1-7 Power consumption and gate leakage current density comparing to the potential reduction in leakage current by an alternative dielectric exhibiting the same equivalent oxide thickness [12].

Figure-chapter 2

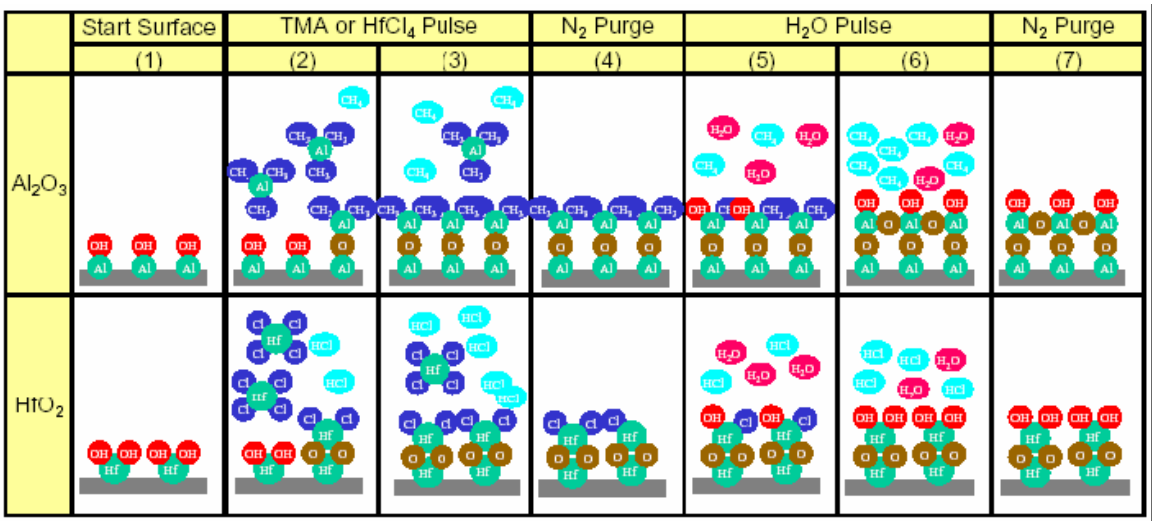


Fig 2-1 ALCVD growth mechanism of AL2O3 and HfO2.

(International SEMATECH Confidential and Supplier Sensitive, 2002)

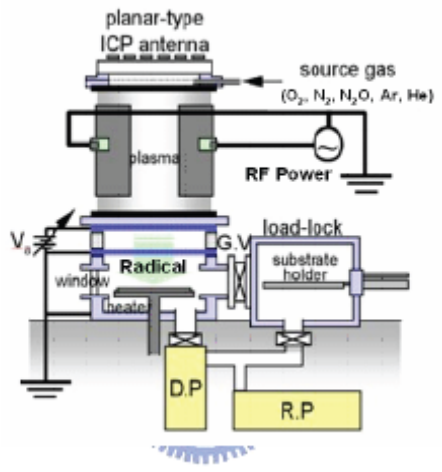


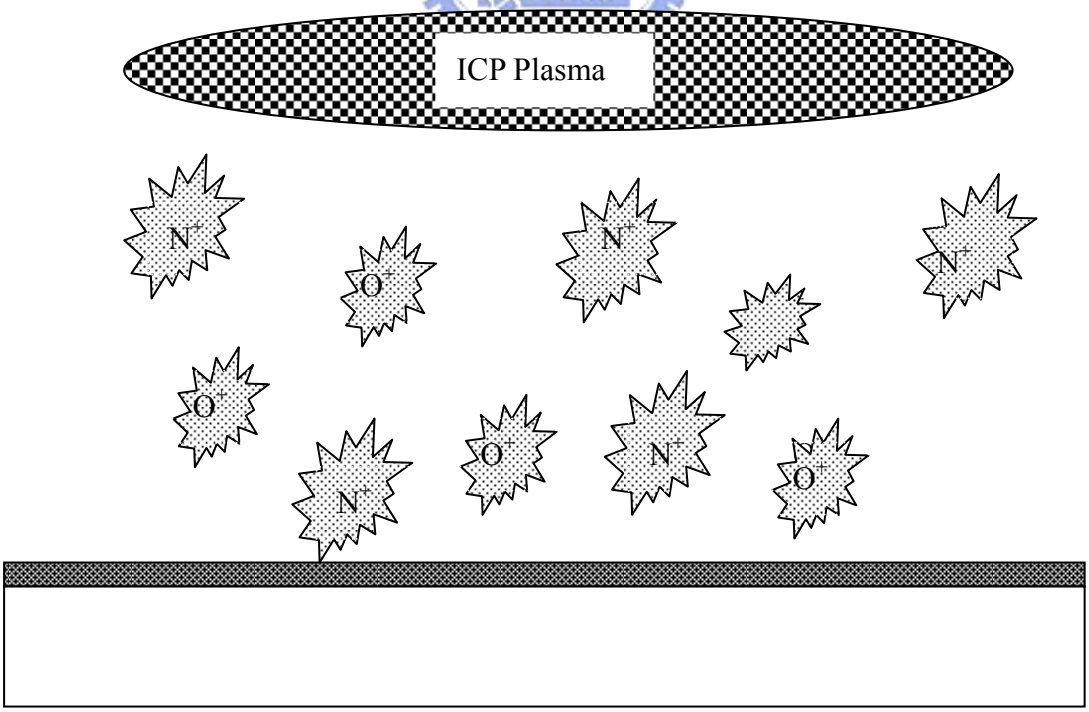
Fig 2-2 The ICP plasma system that was used in this experiment.

1. Standard RCA cleaning.

2. ALD HfO_2 and $HfAlO_x$.

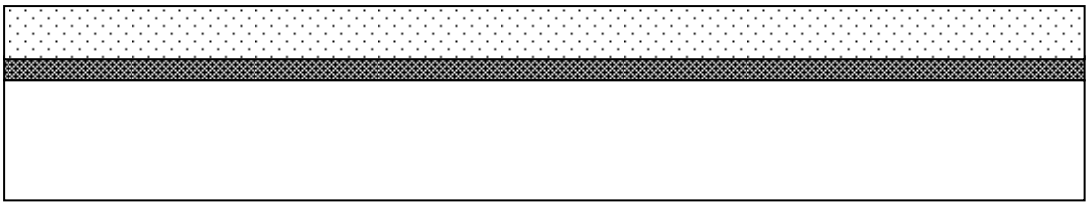
3. Post-Deposition-Annealing (600℃-30 sec for HfO_2 and 800℃-30 sec for $HfAlO_x$).

4. Plasma treatment with N_2 or N_2O (30sec, 60 sec, 90 sec)

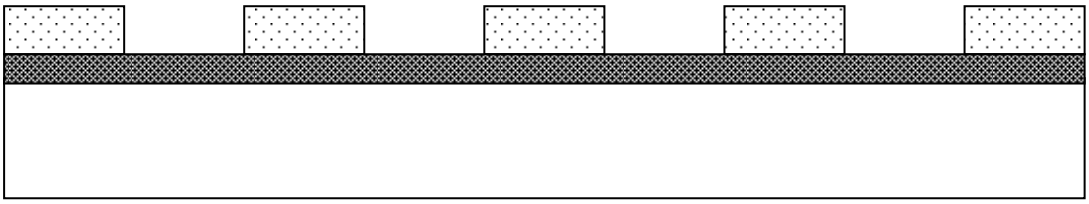


5. Post-Nitridation-Annealing (600℃-30sec)

6. Thermally evaporate 400 nm aluminum as top electrode.



7. Lithography：Define top electrode → Wet etch undefined Al.



8. Thermally evaporate 400 nm aluminum as bottom electrode

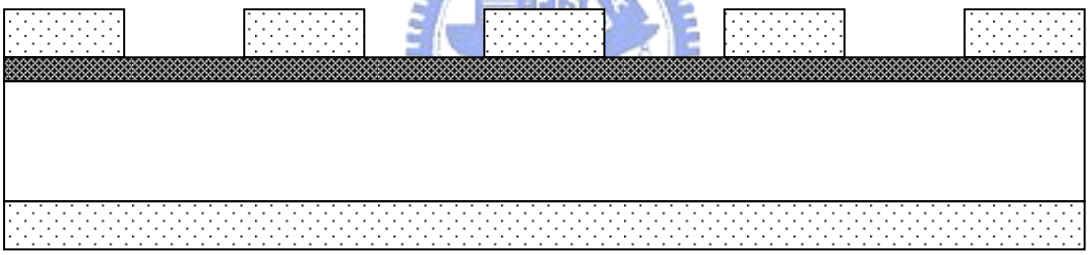


Fig. 2-3 The fabrication flow of the experiment.

Figure-chapter 3

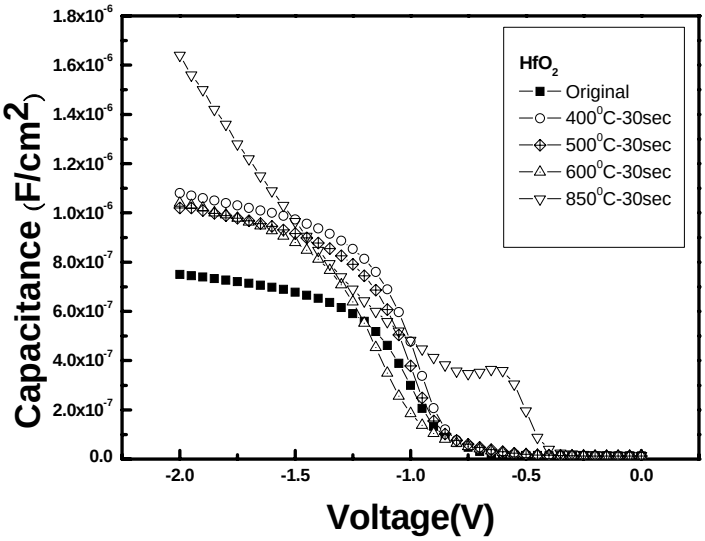


Fig. 3-1 The capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics anneal with different temperature for 30 sec

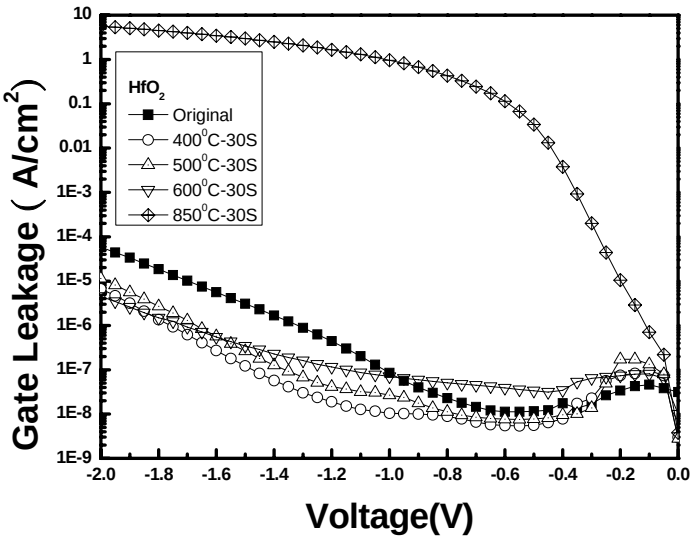


Fig. 3-2 The J-V characteristics of HfO_2 gate dielectrics anneal with different temperature for 30 sec from 0 V to -2 V

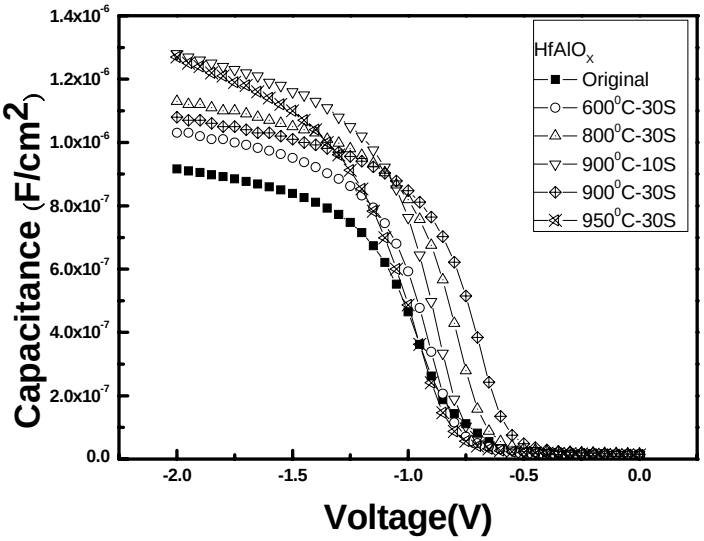


Fig. 3-3 The capacitance-voltage (C-V) characteristics of $HfAlO_x$ gate dielectrics anneal with different temperature for different process time.

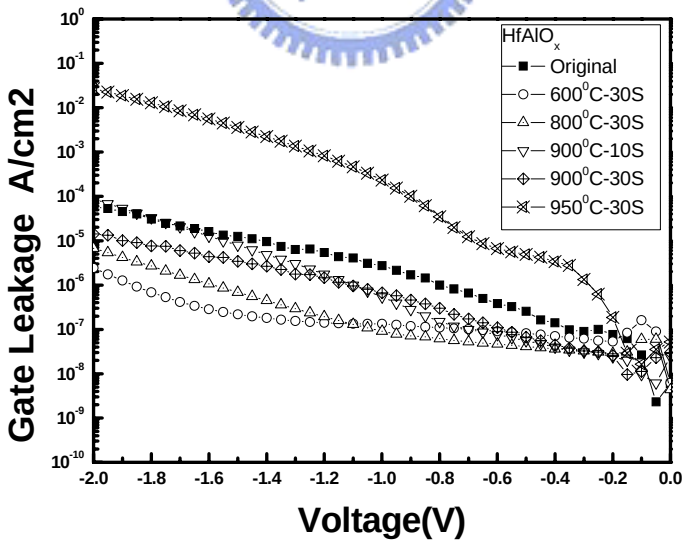


Fig 3-4 The J-V characteristics of $HfAlO_x$ gate dielectrics anneal with different temperature for different process time from 0V to -2V.

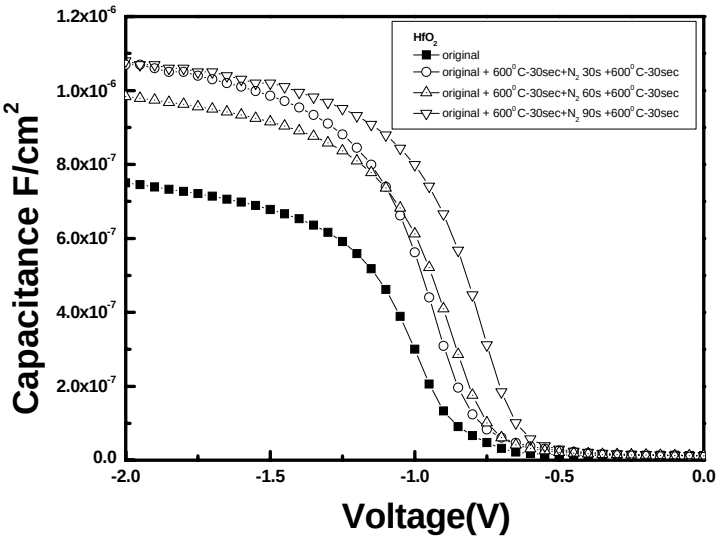


Fig. 3-5 The capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics treated with N_2 plasma treatment for different process time.

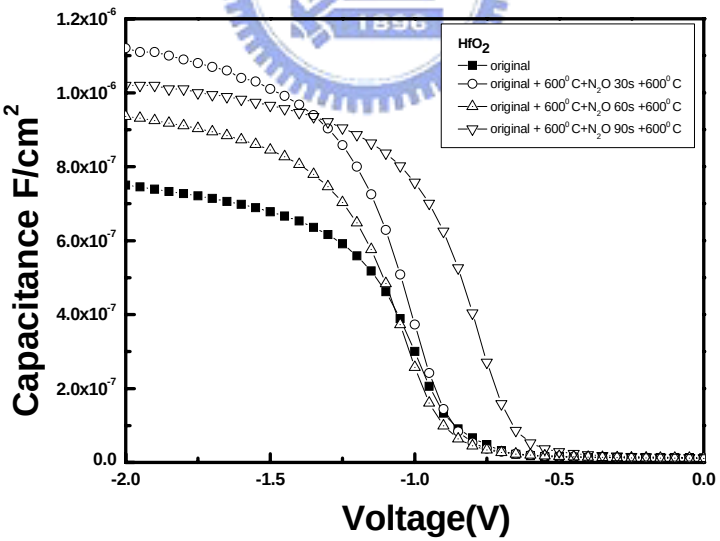


Fig. 3-6 The capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics treated with N_2O plasma treatment for different process time.

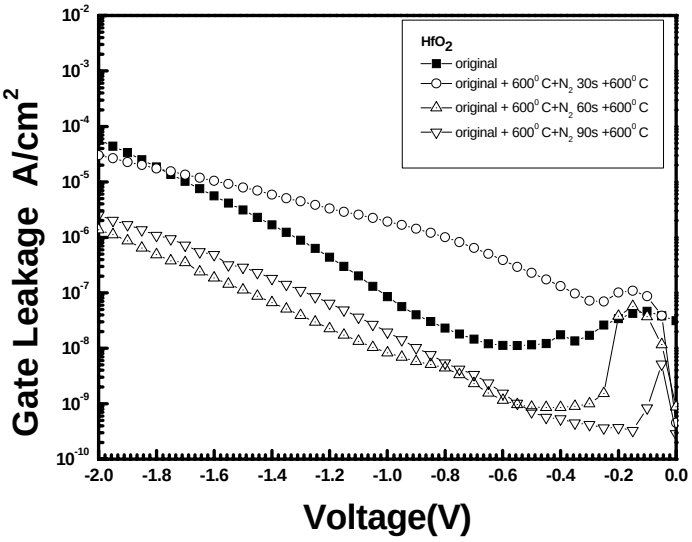


Fig. 3-7 The J-V characteristics of p-type HfO_2 capacitors treated by N_2 plasma with different process time from 0V to -2V.

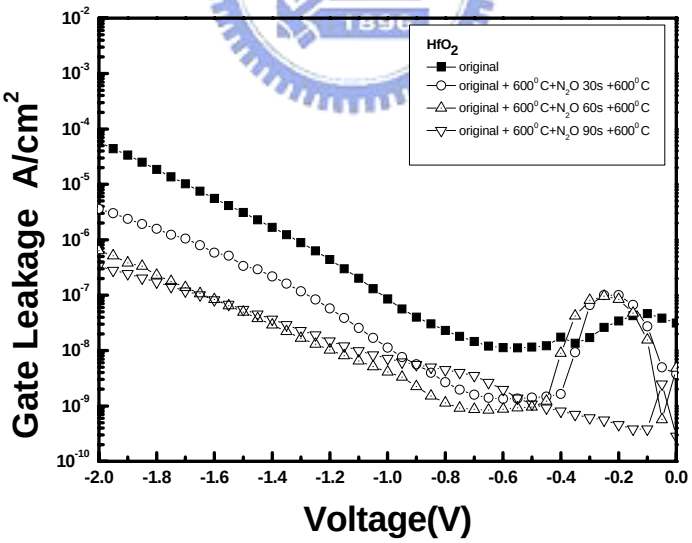


Fig. 3-8 The J-V characteristics of p-type HfO_2 capacitors treated by N_2O plasma with different process time from 0 V to -2 V.

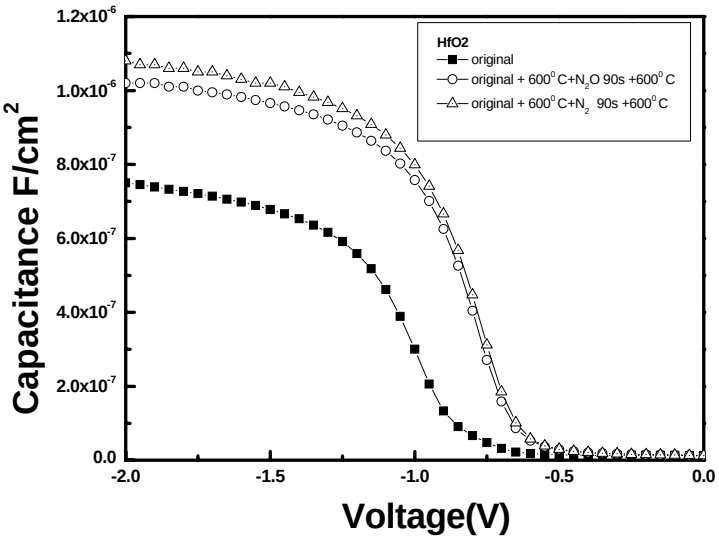


Fig. 3-9 The capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics treated with N_2 plasma treatment for 90sec and N_2O plasma treatment for 90 sec.

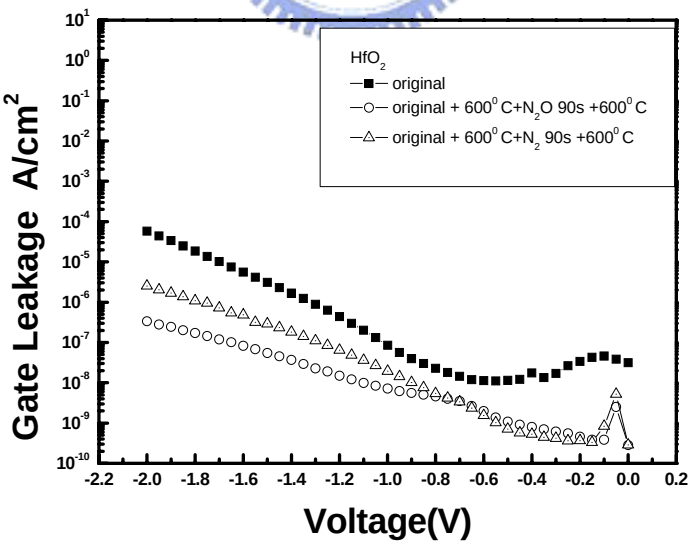


Fig. 3-10 The J-V characteristics of HfO_2 gate dielectrics treated with N_2 plasma treatment for 90 sec and N_2O plasma treatment for 90 sec.

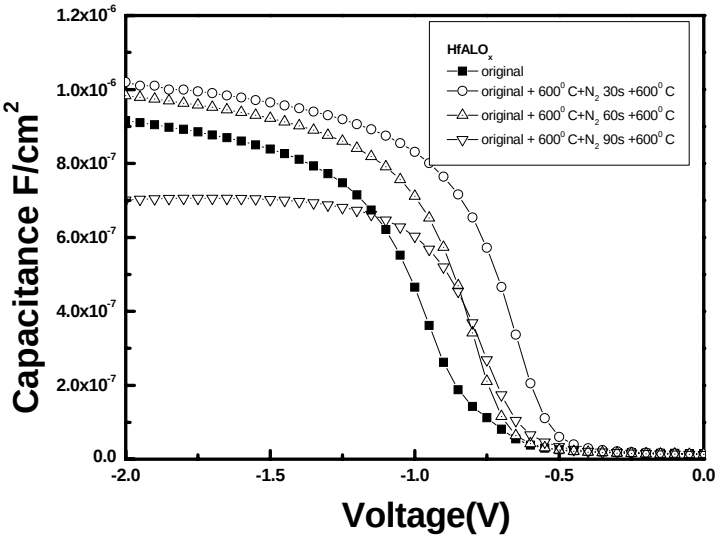


Fig 3-11 The capacitance-voltage (C-V) characteristics of $HfAlO_x$ gate dielectrics treated with N_2 plasma treatment for different process time.

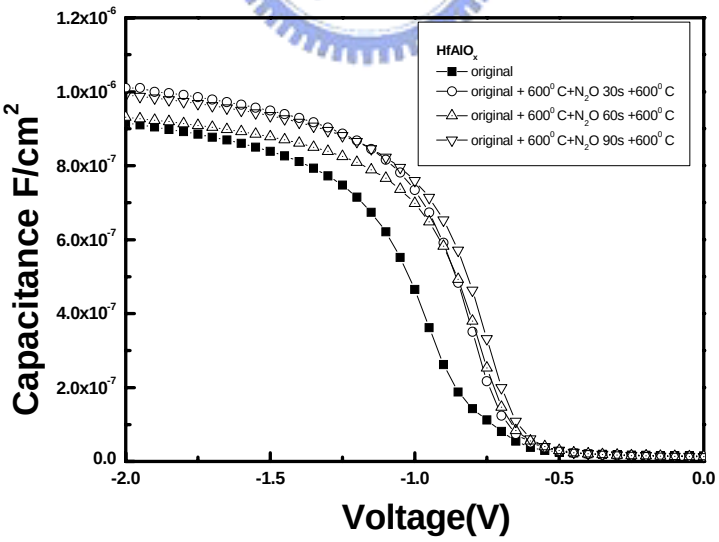


Fig 3-12 The capacitance-voltage (C-V) characteristics of $HfAlO_x$ gate dielectrics treated with N_2O plasma treatment for different process time.

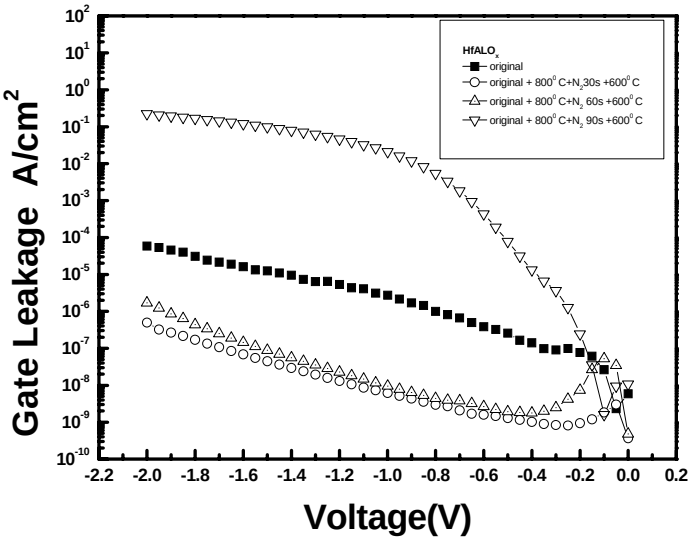


Fig 3-13 The J-V characteristics of p-type $HfAlO_x$ capacitors treated by N_2 plasma with different process time from 0 V to -2 V.

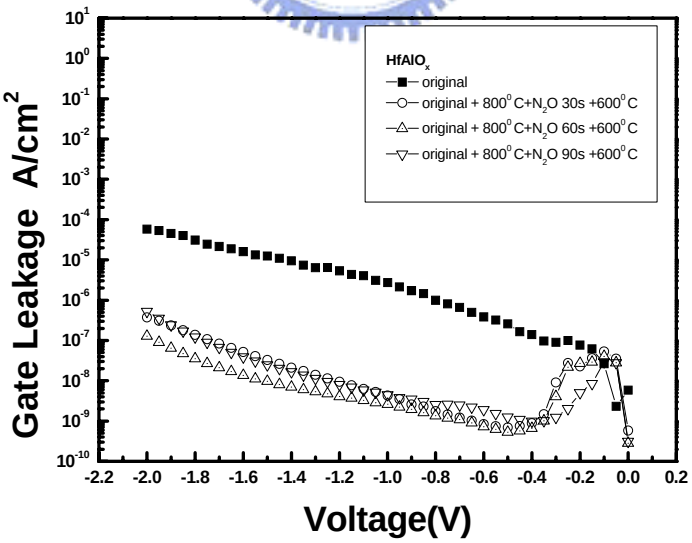


Fig 3-14 The J-V characteristics of p-type $HfAlO_x$ capacitors treated by N_2O plasma with different process time from 0 V to -2 V.

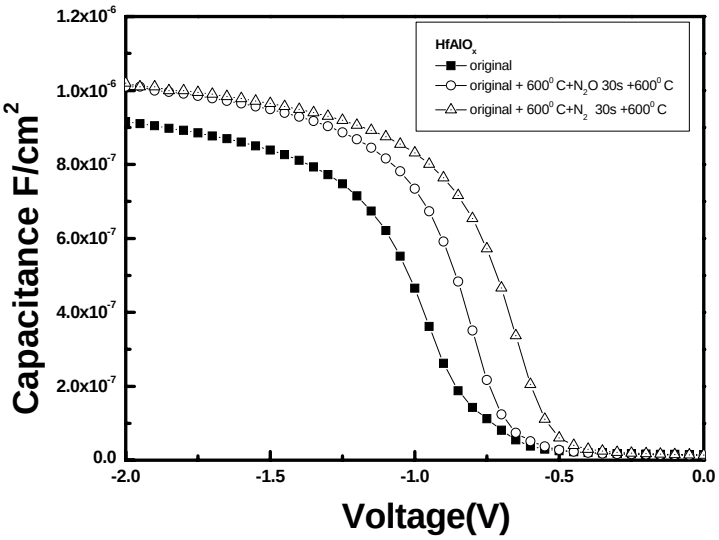


Fig 3-15 The capacitance-voltage (C-V) characteristics of $HfAlO_x$ gate dielectrics treated with N_2 plasma treatment for 30sec and N_2O plasma treatment for 30 sec.

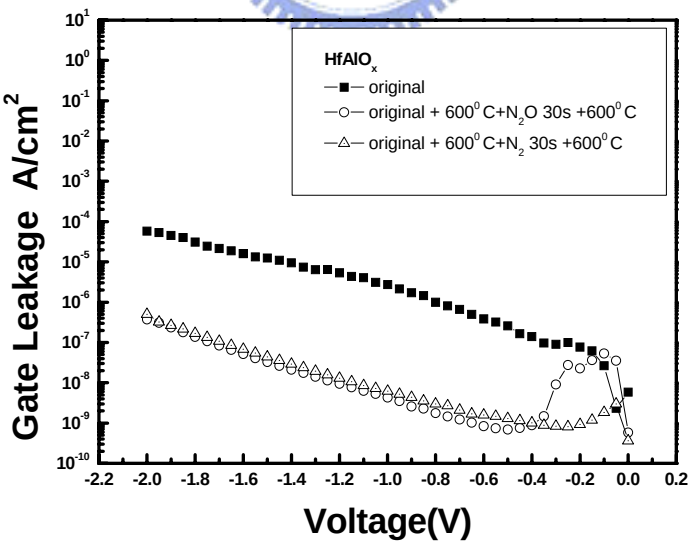


Fig 3-16 The J-V characteristics of $HfAlO_x$ gate dielectrics treated with N_2 plasma treatment for 30 sec and N_2O plasma treatment for 30 sec.

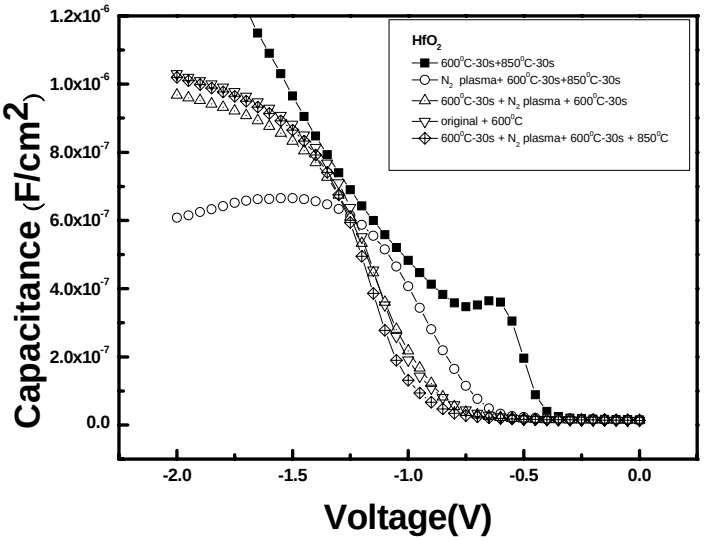


Fig. 3-17 The capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics treated with different steps of after plasma treatment annealing and post-deposition annealing.

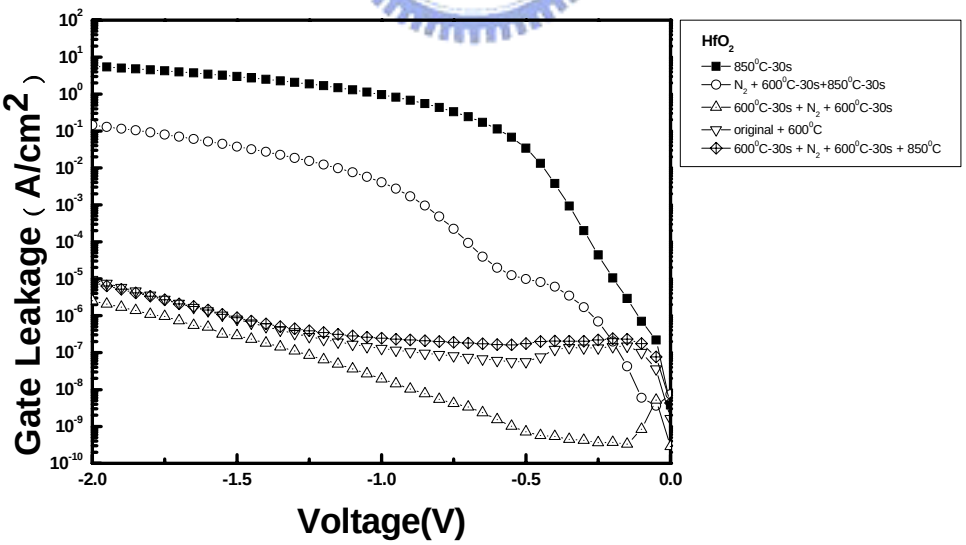


Fig. 3-18 The J-V characteristics of HfO_2 gate dielectrics treated with different steps of after plasma treatment annealing and post-deposition annealing.

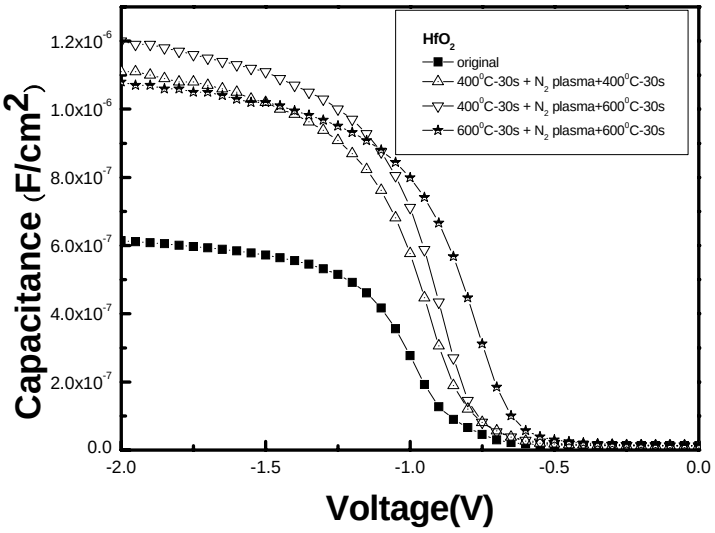


Fig. 3-19 The capacitance-voltage (C-V) of HfO_2 gate dielectrics after different PDA temperature and different PNA temperature.

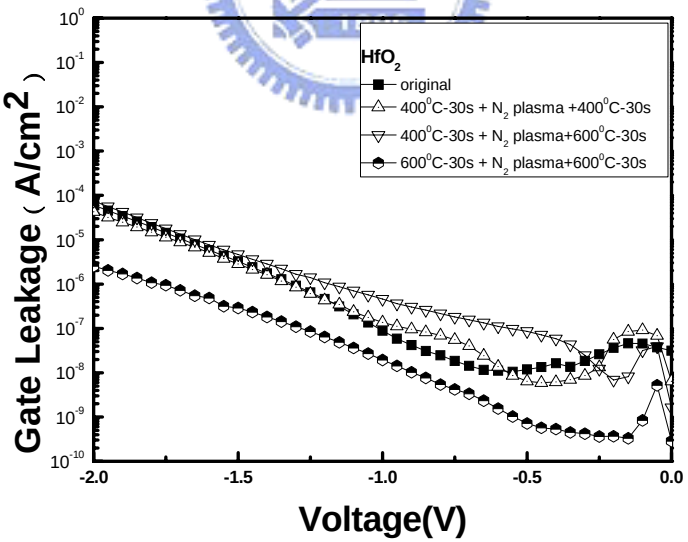


Fig. 3-20 The J-V characteristics of HfO_2 gate dielectrics after different PDA temperature and different PNA temperature.

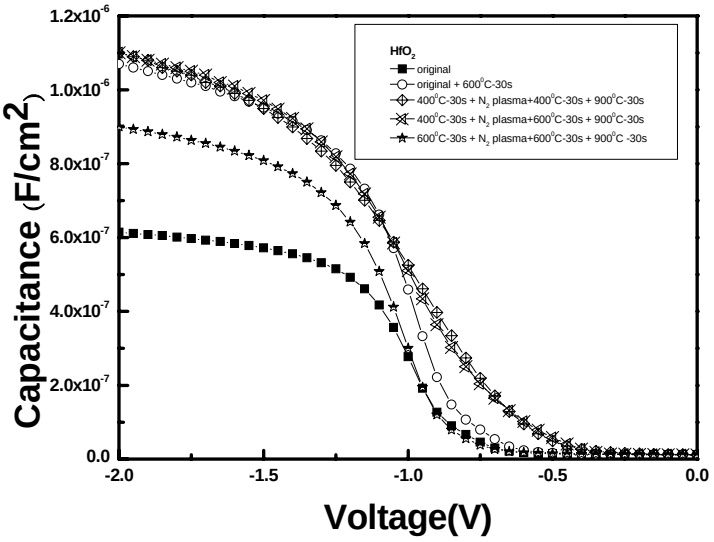


Fig. 3-21 The capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics after nitridation and 900 ℃ 30 sec thermal treatment.

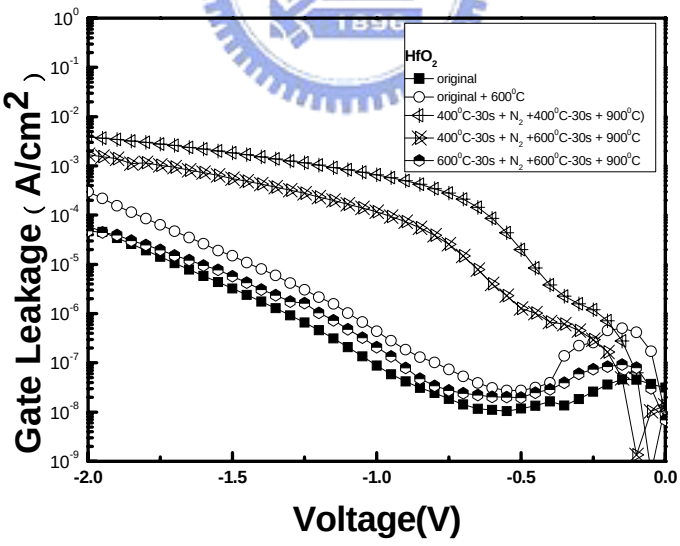


Fig. 3-22 The J-V characteristics of HfO_2 gate dielectrics after nitridation and 900 ℃ 30 sec thermal treatment.

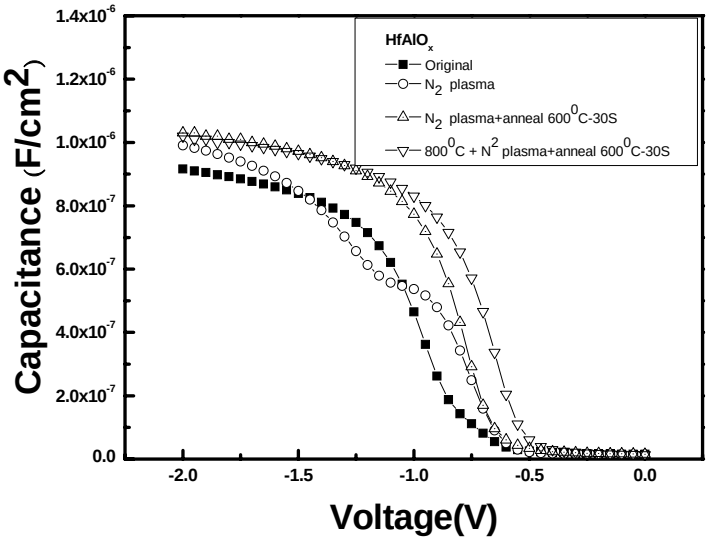


Fig. 3-23 The capacitance-voltage (C-V) characteristics of $HfAlO_x$ gate dielectrics after post-deposition annealing and plasma treatment annealing.

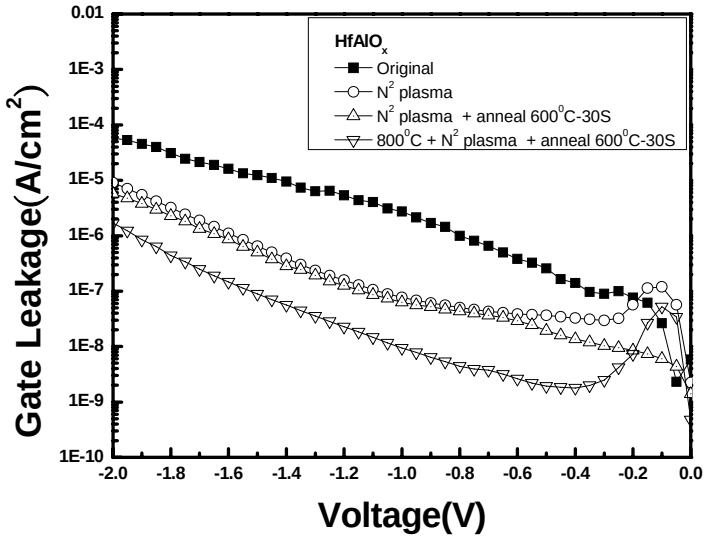


Fig. 3-24 The J-V characteristics of $HfAlO_X$ gate dielectrics after post-deposition annealing and plasma treatment annealing

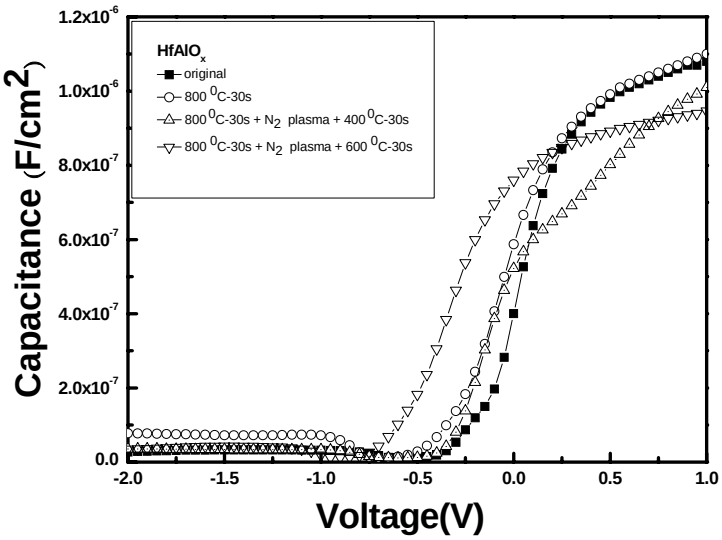


Fig. 3-25 The capacitance-voltage (C-V) characteristics of $HfAlO_x$ gate dielectrics treated with different PNA.

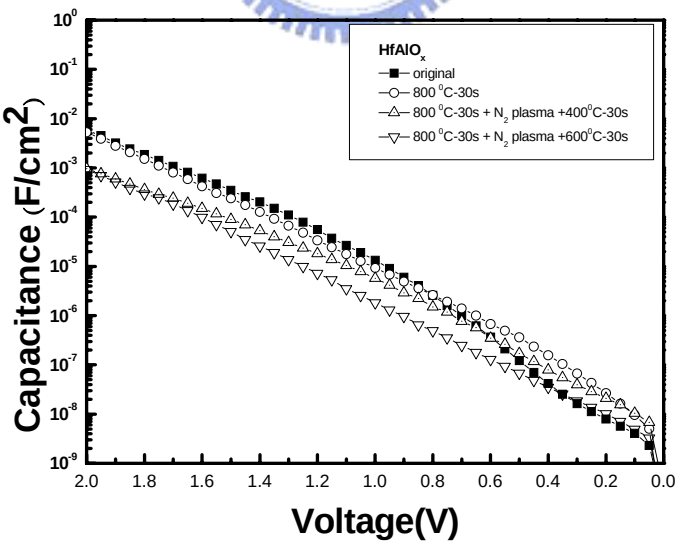


Fig. 3-26 The J-V characteristics of $HfAlO_x$ gate dielectrics treated with different PNA.

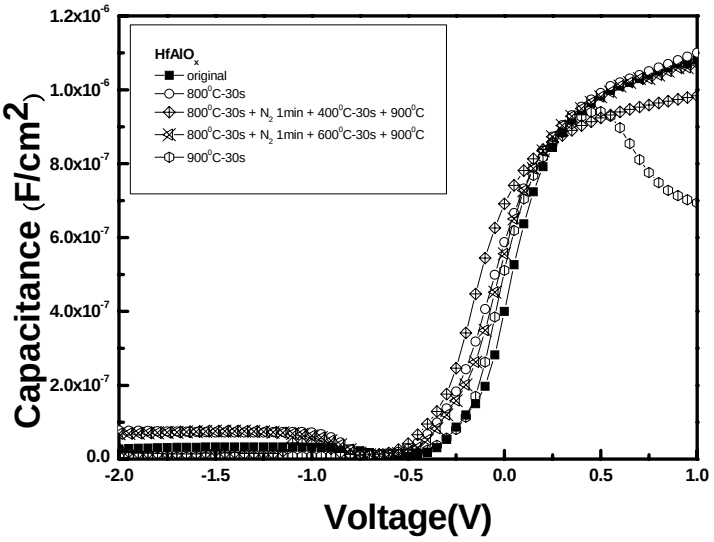


Fig. 3-27 The capacitance-voltage (C-V) characteristics of $HfAlO_x$ gate dielectrics after nitridation and 900℃-30 sec thermal treatment.

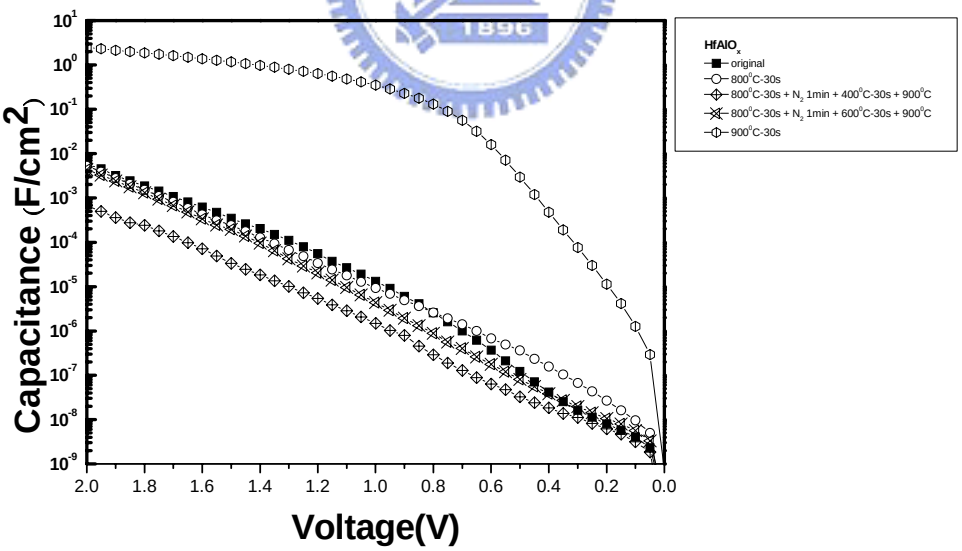


Fig. 3-28 The J-V characteristics of $HfAlO_X$ gate dielectrics after nitridation and 900℃-30 sec thermal treatment.

Figure-chapter 4

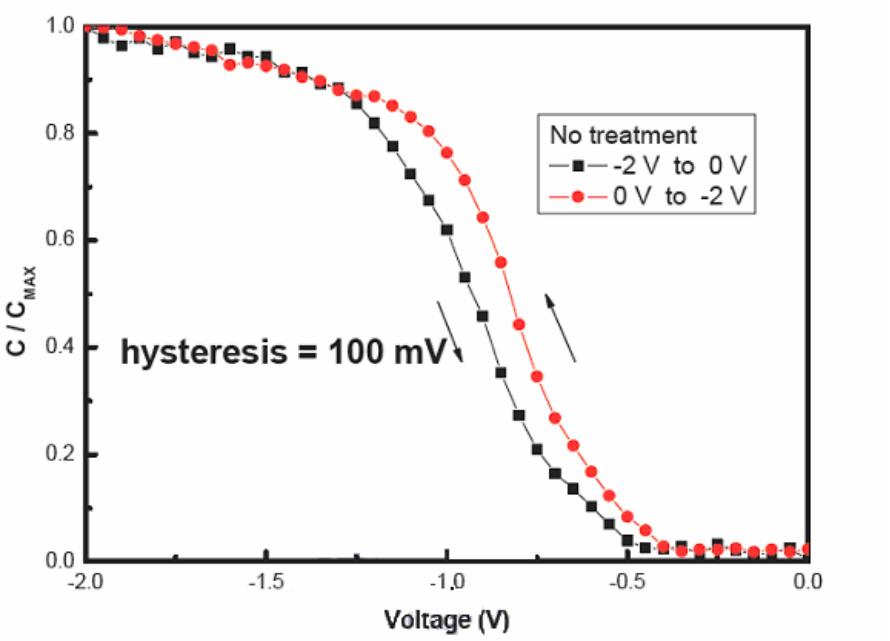


Fig. 4-1 The hysteresis of p-type HfO_2 gate dielectrics (sputter) without plasma treatment.

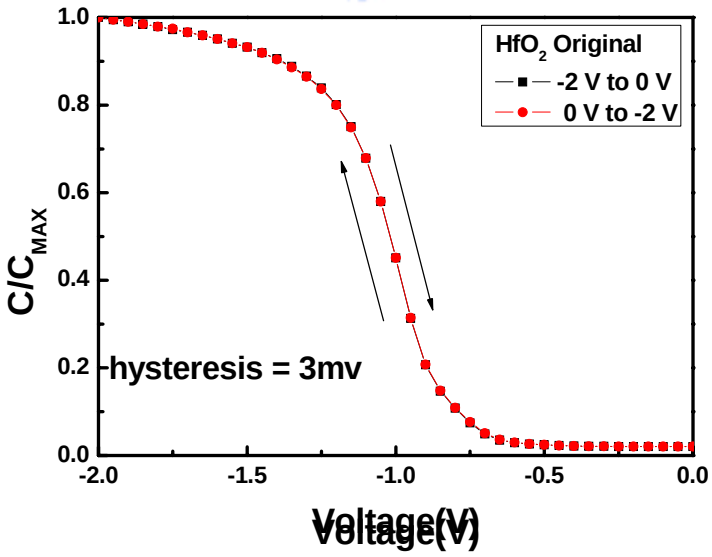


Fig. 4-2 The hysteresis of p-type HfO_2 gate dielectrics (ALD) without plasma treatment.

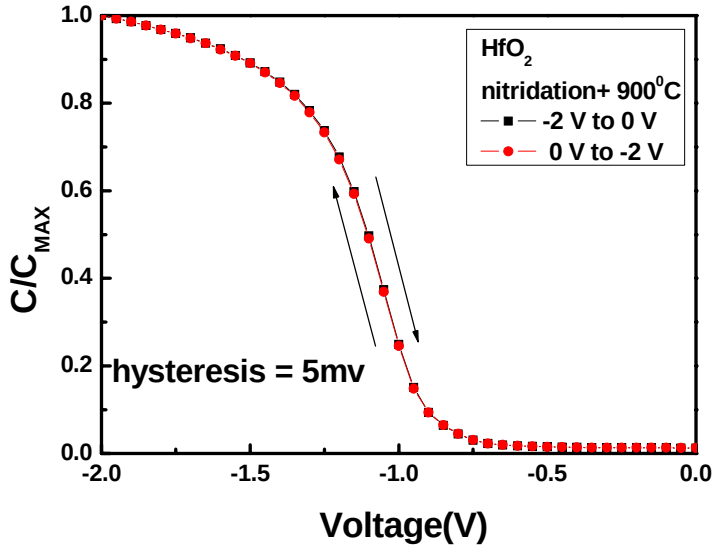


Fig. 4-3 The hysteresis of p-type HfO_2 gate dielectrics (ALD) with PDA 600℃-30 sec, nitridation, PNA 600℃-30 sec and 900℃-30 sec.

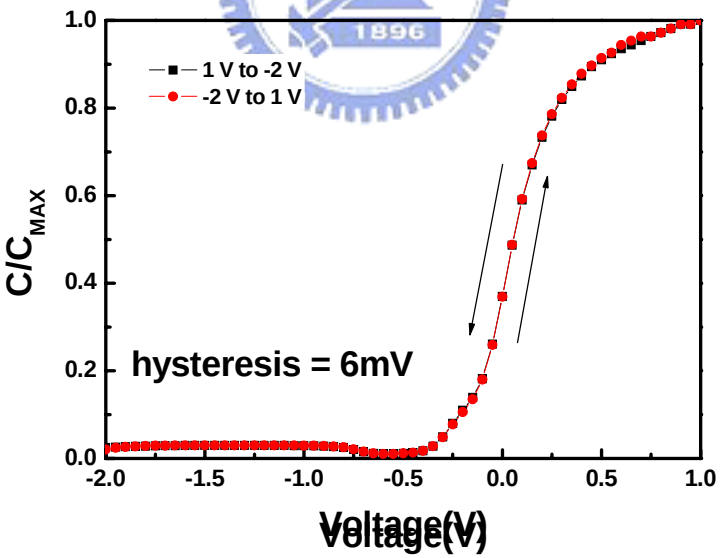


Fig. 4-4 The hysteresis of n-type $HfAlO_x$ gate dielectrics (ALD) without plasma treatment.

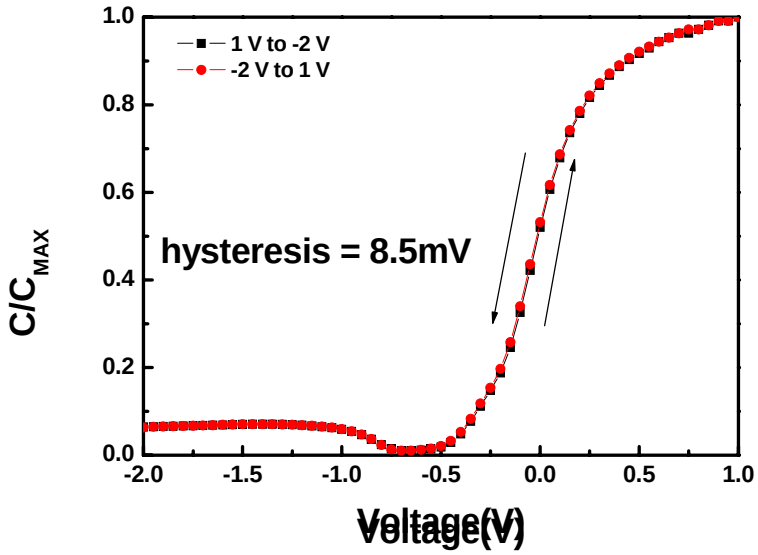


Fig. 4-5 The hysteresis of n-type $HfAlO_x$ gate dielectrics (ALD) with PDA 600℃-30 sec, nitridation, PNA 600℃-30 sec and 900℃-30 sec.

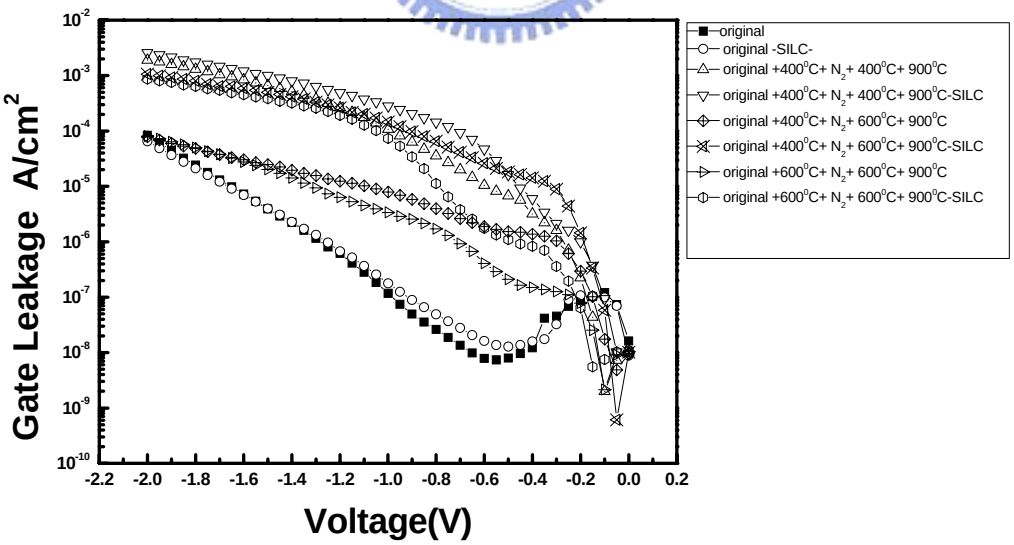


Fig. 4-6 The SILC curve of p-type HfO_2 gate dielectrics treated with N_2 plasma for different PDA and PNA temperature

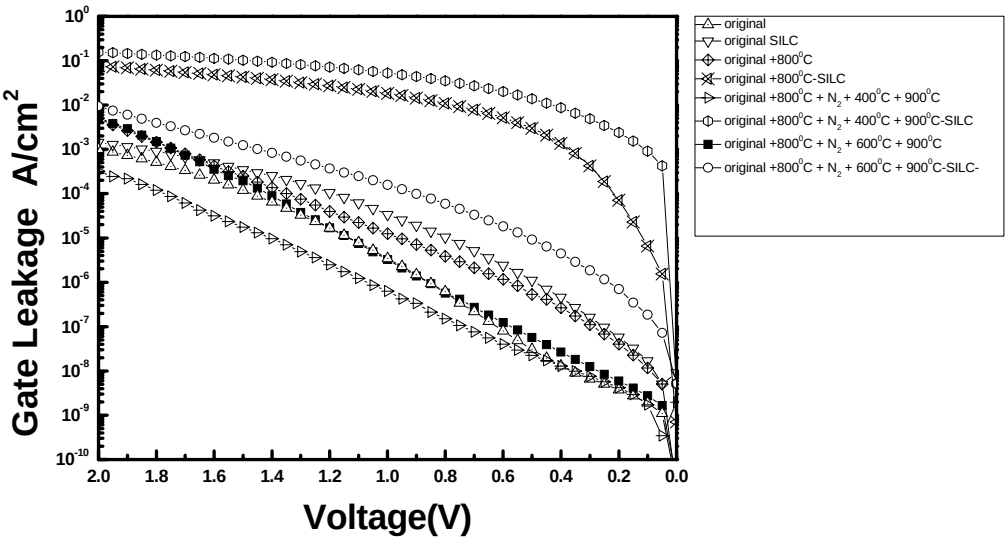


Fig. 4-7 The SILC curve of n-type $HfAlO_x$ gate dielectrics treated with N_2 plasma for different PDA and PNA temperature

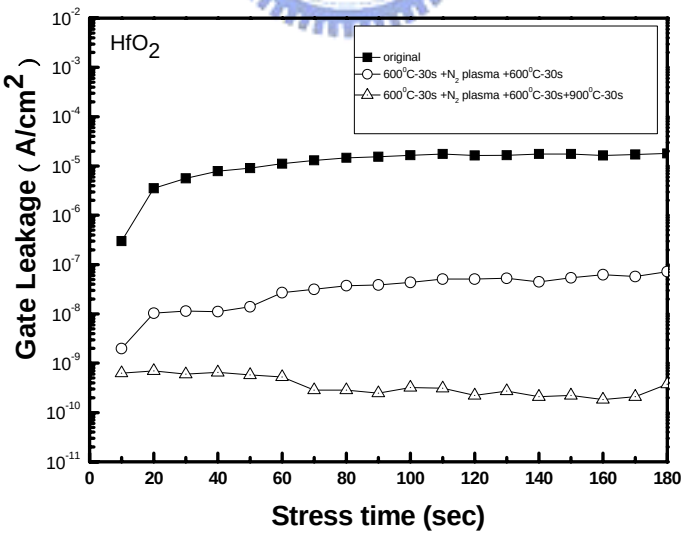


Fig. 4-8 Gate current shift of p-type HfO_2 gate dielectrics treated with N_2 plasma treatment for different annealing process during Vg = 2V CVS.

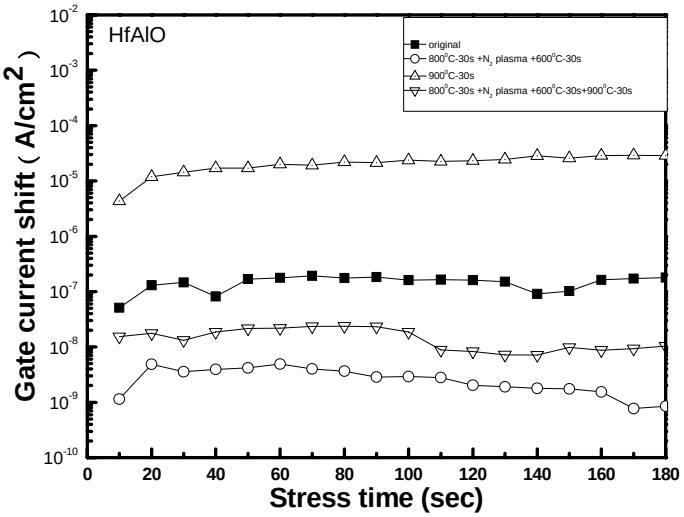


Fig. 4-9 Gate current shift of n-type $HfAlO_x$ gate dielectrics treated with N_2 plasma treatment for different process annealing as a function of stress time during Vg = -2V CVS stress.

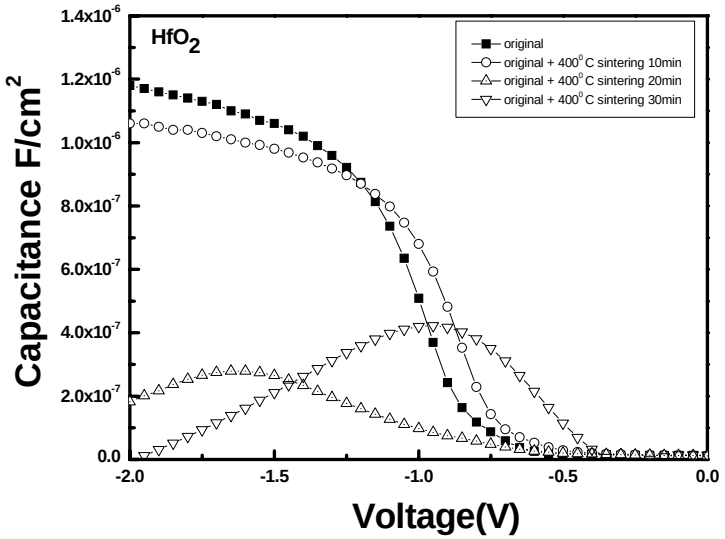


Fig. 4-10 The capacitance-voltage (C-V) characteristics of p-type HfO_2 gate dielectrics with different sintering time.

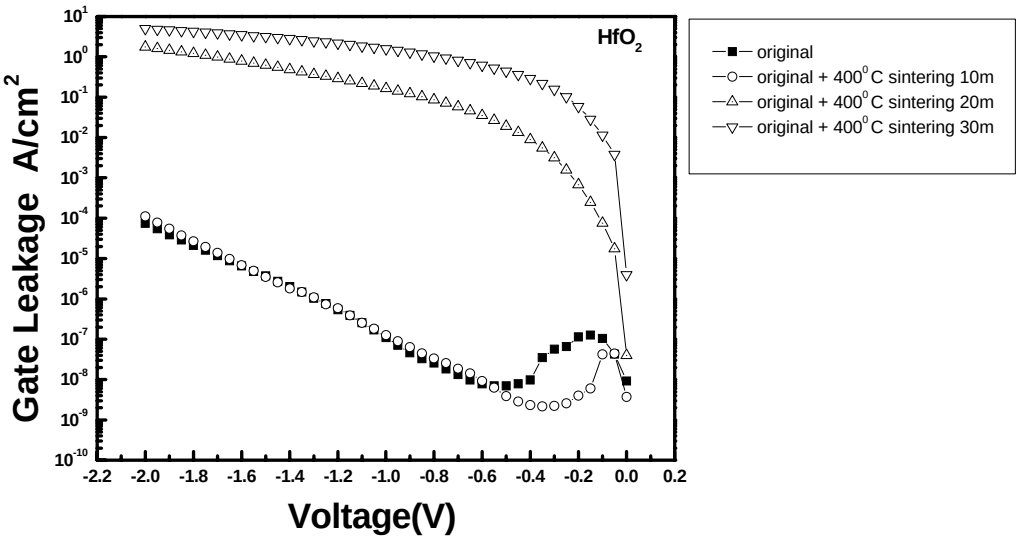


Fig. 4-11 The J-V characteristics of p-type HfO_2 gate dielectrics with different sintering time.

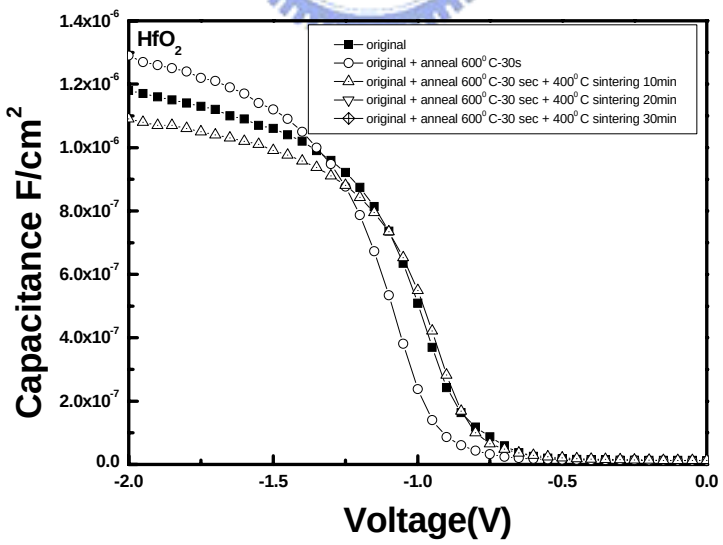


Fig. 4-12 The capacitance-voltage (C-V) characteristics of p-type HfO_2 gate dielectrics with different sintering time after PDA.

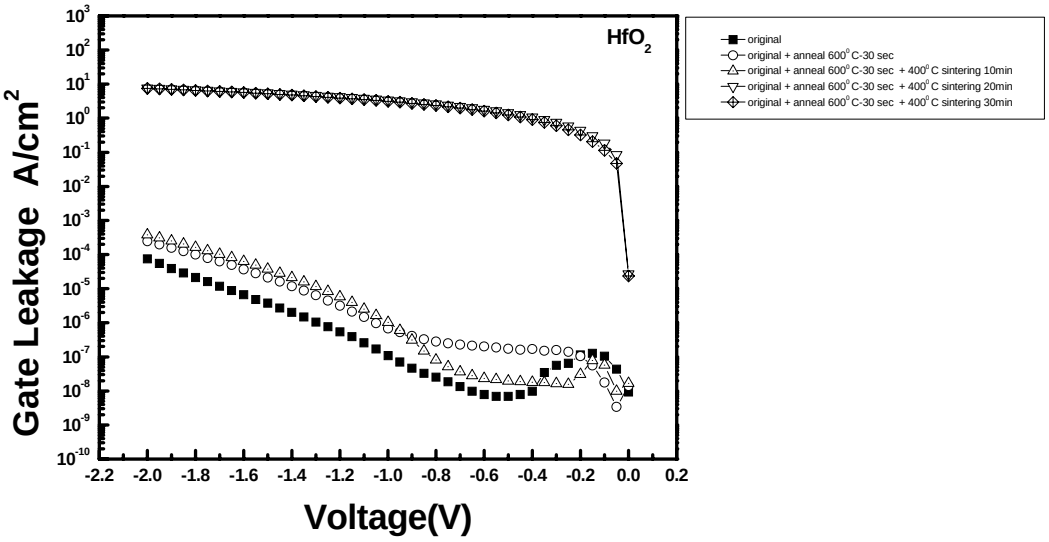


Fig. 4-13 The J-V characteristics of p-type HfO_2 gate dielectrics with different sintering time after PDA.

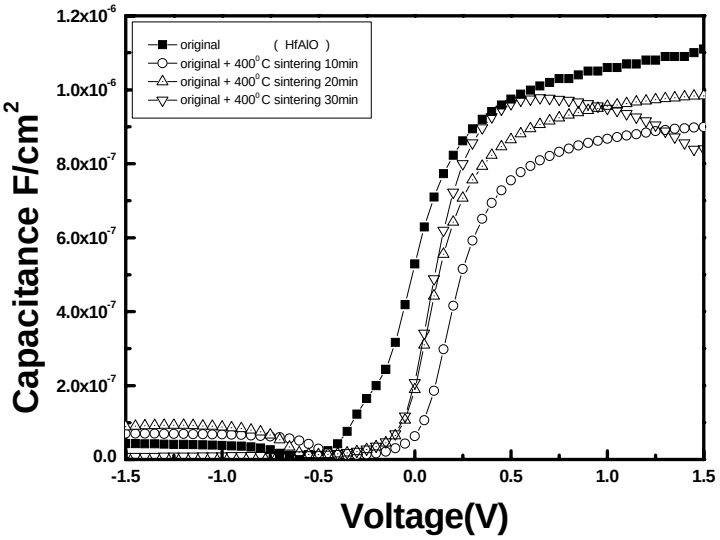


Fig. 4-14 The capacitance-voltage (C-V) characteristics of n-type $HfAlO_x$ gate dielectrics with different sintering time.

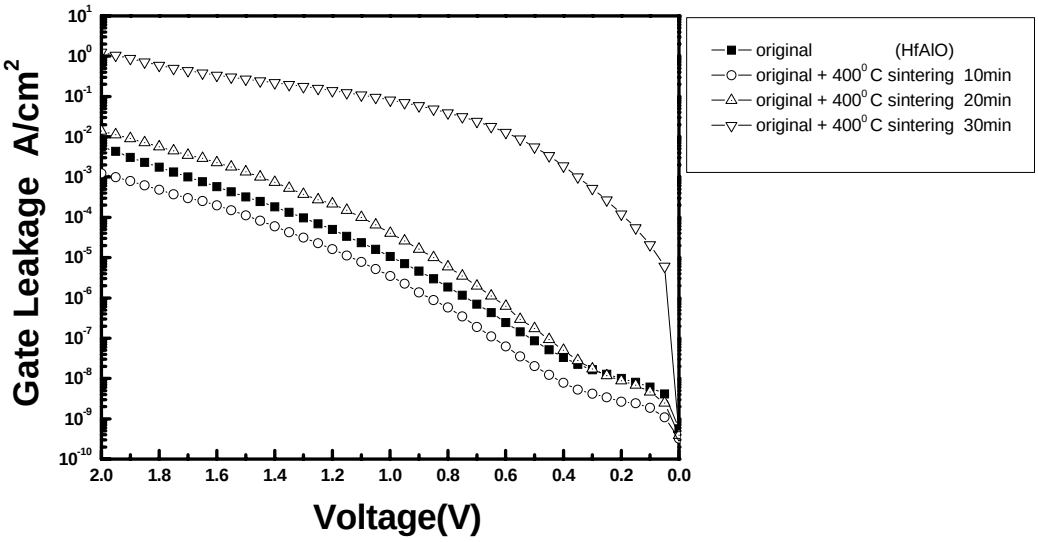


Fig. 4-15 The J-V characteristics of p-type $HfAlO_x$ gate dielectrics with different sintering time.

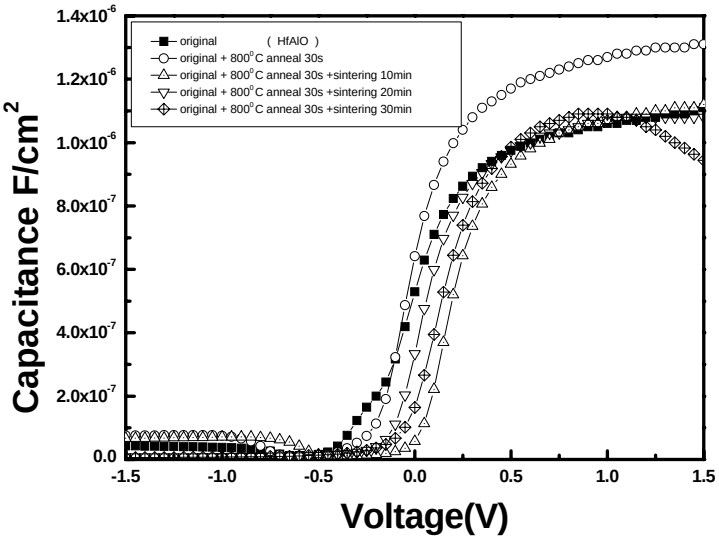


Fig. 4-16 The capacitance-voltage (C-V) characteristics of n-type $HfAlO_x$ gate dielectrics with different sintering time after PDA.

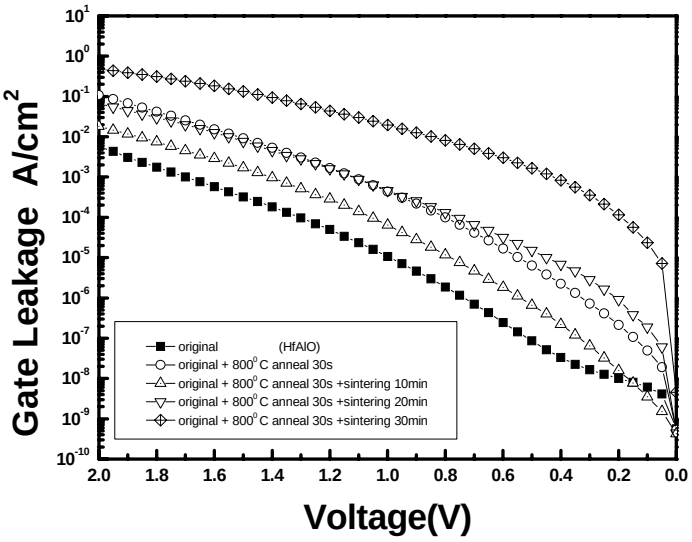


Fig. 4-17 The J-V characteristics of p-type $HfAlO_x$ gate dielectrics with different sintering time after PDA.