國　立　交　通　大　學
電機與控制工程研究所

碩士論文

整合機械式開關之微電容式振動-電能轉換器

Micro Capacitive Vibration-to-Electric Energy Converter with Integrated Mechanical Switches

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中華民國九十六年十月

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中文摘要

微機電系統是一個微系統與電子電路整合的科技平台。在無線感測網路等應用中，這些高度整合的可攜式元件都具有獨立電源的需求。拜先進的超大型積體電路技術所賜，這些微系統節點的電能需求已降至數十 μW 的程度。利用環境中的能源轉換成電能來供給這些可攜式元件使用已經成為一個可行的方法。

此論文呈現一個電容式振動-電能轉換器的設計、製作以及量測。在 1 cm^2 的元件面積以及 3.6 V 輔助電池電源的限制下，此元件的輸出功率可達 31 μW (輸出電壓約 40 V)。我們使用一個 4 克的外加質量塊來調整元件特性，使其在輸入振動下共振。元件整合了機械式開關，以提供準確的充電-放電能量轉換控制。元件是利用 SOI 晶圓並且搭配深蝕刻技術來製作，現階段已克服了所有的製程問題。此能量轉換器已經過量測。元件在有無承載外加質量塊的不同情形下，其共振頻率都符合設計值。元件的電容變化量比預期的還要小。利用背後基底部份掏空的技術，元件的寄生電容已被最小化。元件在無外加質量塊、5 MΩ負載以及 1880 Hz 振動頻率的情形下，量測到的交流輸出功率為 1.2 μW。此情形的最大輸出功率預計為 16 μW。有承載外加質量塊的元件之輸出功率量測仍在進行中。

Abstract

Micro-Electro-Mechanical System (MEMS) is the technology platform that promotes the integration of various microsystems with circuit electronics on the same chip. When applied in fields such as wireless sensor networks, each one of these highly integrated portable devices needs an independent power supply. Due to recent advances in low power VLSI design technology, the power consumption is reduced to about a few tens of microwatts. Therefore, it becomes feasible to power the portable devices by scavenging the ambient energy.

The design, fabrication and measurement of a capacitive vibration-to-electric energy converter are presented in this thesis. With a device area constraint of 1 cm^2 and an auxiliary battery supply of 3.6 V, the device was designed to generate an output power of 31 μW with an output saturation voltage of 40 V. An external mass of 4 grams was needed to adjust the device resonance to match the input vibration. Mechanical switches are integrated onto the device transducer unit to provide accurate charge-discharge energy conversion timing. The device was fabricated in SOI (silicon-on-insulator) wafers by deep silicon etching technology. By overcoming all processing issues, the device can be successfully fabricated by a modified fabrication process. Measurements on the energy converter were also conducted. Resonant frequencies of the device with and without the external mass agreed with the designed values. Capacitance change was smaller than expected. Parasitic capacitance was minimized by partial back side substrate removal. Without the external mass, the measured AC output power was 1.2 μW with a load of 5 MΩ at 1880 Hz. The maximum output power in this condition is expected to be 16 μW. AC output power measurement of the devices with external mass attached is still in progress.

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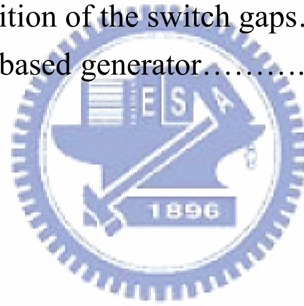

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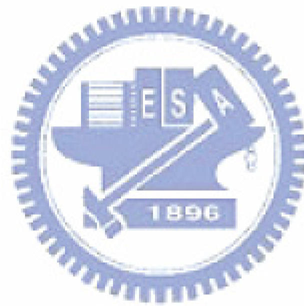


Chapter 1 Introduction

1.1 Motivation

Micro-Electro-Mechanical System (MEMS) is the integration of mechanical elements, sensors, actuators, and electronics on a common substrate through micromachining processes compatible with conventional integrated circuit (IC) fabrication. By combining silicon based micro-machines with microelectronics, MEMS technology has revolutionary impact on all categories of applications, making possible the realization of the complete system on chip (SOC) concept. Current MEMS research and development has already been applied in fields such as micro optical systems, sensors and actuators, micro fluidic elements, and even biomedical applications, all with fruitful results.

Such continuous improvement of microsystem technology promotes the development of smart micro transducer networks, such as RFID (Radio Frequency Identification) and wireless sensor network [1]. These highly integrated portable devices have received increasing interest in recent years. Nevertheless, power consumption has become a severe limitation on the development due to the limited energy capacity of the small volume energy storage devices [2]. Traditional storage devices include batteries [3], micro batteries [4], micro fuel cells [5], ultra capacitors [6], micro heat engines [7], and radioactive materials [8]. Researchers attempt to increase the energy density in these storage devices, but the solutions still have finite lifetime and high maintenance costs.

Fortunately, the advance in low power VLSI (Very Large Scale Integrated circuit) technology, along with the low duty cycles of the wireless sensor networks, have reduced power requirements to tens to hundreds of microwatts [9]. It becomes

possible to power these portable devices by scavenging ambient energy from the environment, thus providing a self renewable or even self sustainable energy source which can replenish part or all of the consumed power. This concept has received attention along with the development of wireless sensor networks, and research on various ambient energy scavenging technologies are being conducted.

1.2 Literature survey

State-of-art ambient energy scavenging devices can extract energy from a range of ambient energy sources, such as light exposure, thermal gradients, human power, air flow, acoustic noise, and vibration [10]. Methods to harvest energy from various ambient energy forms are studied and compared in this section in order to decide the main energy conversion technology of concern in this thesis. Due to the inexhaustible energy providence from the environment, the performance of such harvesting devices is characterized by their power density, instead of energy density used for traditional storage devices.

1.2.1 Photovoltaic light exposure

Light exposure is converted into electrical power by photovoltaic cells, more popularly known as solar cells. Photovoltaic cells function by the photovoltaic effect [11], originated by the photo-generation of charge carriers in specially treated light absorbing semi-conductor material under light exposure. The charge carriers are then transmitted out by conductive contacts to form electricity. The operation schematic is shown in Fig. 1.1. Single crystal silicon photovoltaic cells possess conversion efficiency ranging from 12% to 25%. Thin film polycrystalline and amorphous silicon photovoltaic cells are also commercially available. They cost less but provide lower

conversion efficiency [12]. Overall, photovoltaic energy conversion offers sufficient output power for electronics. The fabrication is also compatible with conventional IC technology. Nevertheless, the output power of photovoltaic cells is dominated by environmental conditions. For instance, if the device is installed outdoors and operated primarily during daytime, the photovoltaic cell offers a sufficient power density up to 15 mW/cm^2. However, under normal indoor office light exposure, the photovoltaic cell can only supply a power density below 5 μW/cm^2. Due to this characteristic, the photovoltaic cell device is limited to specific applications.

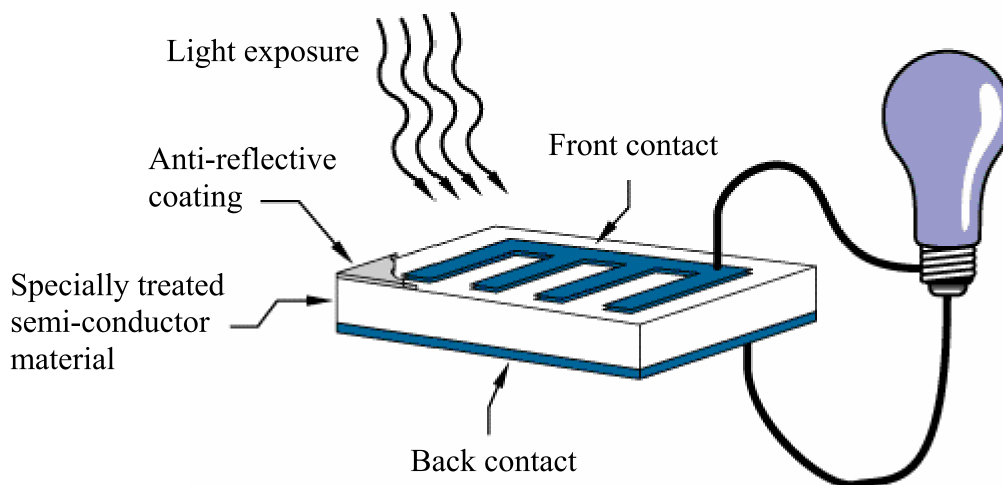


Fig. 1.1 Typical operation schematic of photovoltaic energy conversion [11]

1.2.2 Thermal gradient potential

The thermal gradients in the environment can also serve as power sources through the Peltier–Seebeck effect, or the thermoelectric effect [13]. In this effect, a voltage difference, probably several microvolts per degree, will build up between two different metals or semiconductors in the presence of a temperature difference. If the two materials are connected in a closed loop, a continuous current will flow.

Materials with large Seebeck coefficients and high electrical conductivity can improve conversion efficiency and minimize power loss. However, typical materials

used for thermoelectric energy conversion, such as Sb_2Te_3, Bi_2Te_3, Bi-Sb, PbTe, Si-Ge, BiSbTeSe compounds, and InSbTe, are not completely compatible with the IC process. Furthermore, although an output power density of 40 μW/cm^3 under a 5 ˚C temperature gradient has been demonstrated [14], temperature differences of this level (5 ˚C) are not common in typical micro system environment [15]. Without large thermal gradients, the output power is limited. Connecting several thermocouple elements in series can be used to generate larger output power, as shown in Fig. 1.2. However, the increased series resistance increases the ohmic power loss and thus reduces the overall power conversion efficiency.

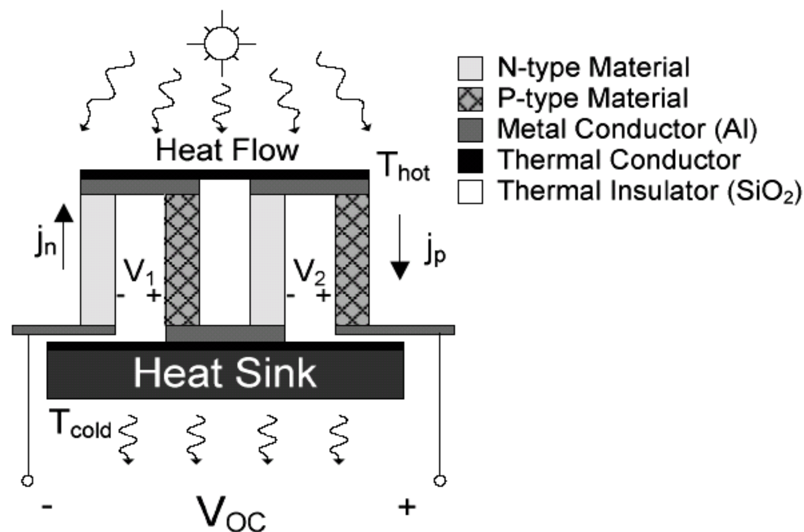


Fig. 1.2 Thermoelectric energy converter composed of two series thermocouples [16]

1.2.3 Human kinetic energy

Another energy source with significant potential is the human body movement. Typical research on this subject use piezoelectric conversion to scavenge the kinetic energy produced by the human body, which has a pulse-like percussive energy form. Significant amount of work has been conducted to harvest energy off the human body by wearable devices [17, 18]. The studies by Massachusetts Institute of Technology

suggests that the human foot has the greatest potential as an energy source due to its high energy production rate at the heel and ball of the foot during walking. This research has led to the development of the piezoelectric shoe inserts, as shown in Fig. 1.3, with a power density of 330 μW/cm^3. The application is however limited by the piezoelectric and IC integration issues as well as the power delivery issues. For specific requirements such as RFID tags and other wireless devices worn on the foot, the piezoelectric shoe inserts serves as a good solution.

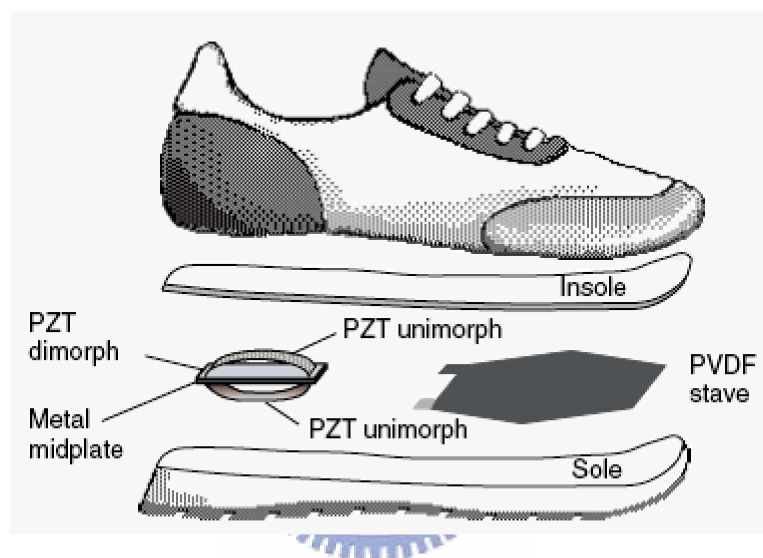


Fig. 1.3 Exploded view of the piezoelectric shoe inserts located underneath the heel and ball of the foot [18]

1.2.4 Aerodynamic air flow

Traditional wind powered generators, such as wind mills, have existed for a long time. Current interest is to proceed into the centimeter scale. With the output power related to the air velocity, a 5 mW/cm^3 power density can be achieved under an air velocity of 8 m/s [10]. Without sufficient air velocity, the output power significantly decreases (e. g. 380 μW/cm^2 at 5 m/s air velocity) [10]. This eventually limits the application of such technology. Up to current date, no effort on converting air flow to electric power at centimeter scale has been reported.

1.2.5 Acoustic noise power

Another extraordinary power source is the acoustic noise power, which is usually considered as pollution. This perspective method should be especially useful in the urban environment or industrial environment, which is constantly contaminated by noise. Unfortunately, current research and development of this method has only been able to scavenge limited power from noise with extremely high decibel levels [1]. Therefore, it is not a feasible power source for common applications.

1.2.6 Ambient vibration

Similar but unlike human or acoustic vibration, the ambient vibration is another widely existing energy source. Typical ambient vibration sources are classified into two major categories. One is the steady low amplitude vibration with constant or small deviation of frequency. It is mainly observed in large commercial and office buildings, industrial environments, and residential household appliances. The other is the more randomly distributed vibration with varying frequency and intensive amplitude. It is often observed in automobiles, aircrafts, ships, trains and other machinery that produces intensive forces. Different conversion technologies are utilized for different types of vibration sources. Theory and experiments show that more than 300 $\mu W/cm^3$ can be generated [10]. The potential of this method is greatly amplified when targeted on specific vibration sources. More discussion and detail will follow.

1.2.7 Summary on energy sources

Summary of the different ambient energy sources and energy storage devices is shown in Table 1.1 [10]. The upper portion shows the comparison of the ambient energy sources; the lower portion shows the comparison of the energy storage devices.

Based on the above survey, ambient vibration is chosen as the energy source for conversion due to its ubiquity and sufficient power density.

Table 1.1 Comparison of energy scavenging and power sources [10]

Power sources	**Power density ($\mu W/cm^3$ or $\mu W/cm^2$)**	**Commercially available?**
Solar (outdoors)	15, 000 $\mu W/cm^2$	Yes
Solar (indoors)	10 $\mu W/cm^2$	Yes
Temperature gradient	40 $\mu W/cm^3$ at 5°C gradient	Soon
Human power	330 $\mu W/cm^3$	No
Air flow	380 $\mu W/cm^3$ at 5 m/s velocity	No
Acoustic noise	0.96 $\mu W/cm^2$ at 100 dB	No
Vibration	375 $\mu W/cm^3$	No

Storage devices	**Energy density ($\mu Wyear/cm^3$)**	**Commercially available?**
Batteries (Lithium)	90 $\mu Wyear/cm^3$	Yes
Batteries (Lithium-ion)	34 $\mu Wyear/cm^3$	Yes
Fuel cells	110 $\mu Wyear/cm^3$	No
Ultra capacitors	1.6~3.2 $\mu Wyear/cm^3$	Yes
Heat engine	105 $\mu Wyear/cm^3$	No
Radioactive (^{63}Ni)	52 $\mu Wyear/cm^3$	No

1.3 Ambient vibration energy conversion

Based on the previous discussion, more details on the conversion of ambient vibration source energy into electrical power are discussed in this section. Typical

vibration-to-electric energy conversion technology is based on three methods. They are respectively electromagnetic inductive conversion, the electrostatic capacitive conversion, and the piezoelectric conversion.

1.3.1 Electromagnetic energy conversion

Electromagnetic energy conversion is based on the Faraday's law of induction, which states that any change of the magnetic flux linkage in a coil will induce a voltage or electromotive force (EMF). This induced voltage is equal to the negative rate of change of magnetic flux times the number of turns in the coils. The operation of the electromagnetic energy converter is shown in Fig. 1.4 [16, 19]. The coil is attached to a vibration-driven oscillating mass and moves through a magnetic field established by a permanent magnet. The output AC power depends on the number of turns in the coil, the magnetic field intensity, and the vibration amplitude and frequency.

Shearwood and Yates [20] developed a device to produce a 0.3 μW output power (power density of 10~15 $\mu W/cm^3$) from a vibration source with amplitude of 500 nm and frequency of 4.4 kHz. The output AC voltage was 8 mV, which was too small to be rectified by a bridge configuration that requires a turn-on voltage of about 0.5 V.

More recently, Chandrakasa et al. have developed an electromagnetic converter targeting the vibration with amplitude of 2 cm and frequency of 2 Hz of a walking person [21-23]. Their simulations showed that a maximum output power of 400 μW could be achieved with the output voltage of 180 mV. The device had a large size of 4 cm$\times$4 cm$\times$10 cm, and the corresponding power density was 2.5 $\mu W/cm^3$.

The most common drawback of electromagnetic energy conversion is the relatively low induced voltage, which can be foreseen from the scaling law on electromagnetic effect. Transformers or other solutions are inadequate due to the

limited device volume. Difficulty in fabricating high quality coils with large number of turns in the thin film process is also encountered. These drawbacks result in a large device volume, and thus a lower power density.

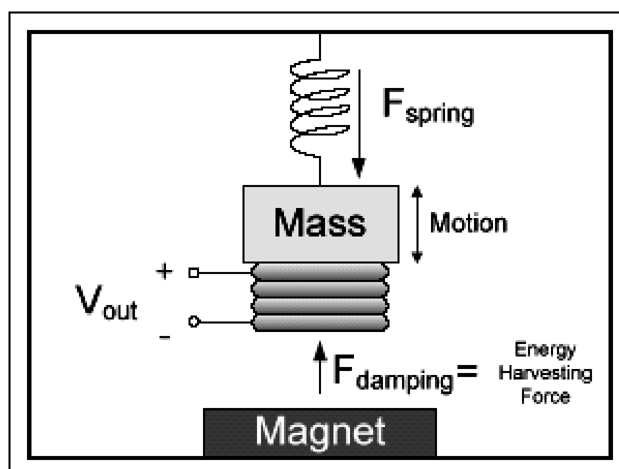


Fig. 1.4 Electromagnetic energy converter [16]

1.3.2 Piezoelectric energy conversion

Piezoelectric energy conversion relies on the piezoelectric effect of specific materials in the presence of an applied mechanical stress. When the electrical charge in the crystal lattice is separated by the stress, a voltage drop will be induced across the piezoelectric material. Typical piezoelectric conversion device consists of a bimorph piezoelectric cantilever beam with mass attached to the free end, as shown in Fig. 1.5. Piezoelectric energy conversion is more suitable for the frequency varying intensive amplitude vibration source mentioned before.

The output power due to vibration stimulation is in AC form, and further power management circuitry is needed to extract stable and thus usable output power. Optimal power circuitry for piezoelectric generators has been studied [24, 25]. The maximum reported output power was 18 mW with a power density of 1.86 mW/cm^3 for a vibration frequency of 53.8 Hz. Other works on piezoelectric converters were

also conducted [10, 15, 26]. Power density of 200 μW/cm^3 was achieved for the input vibration of 2.25m/s^2 at 120 Hz.

In piezoelectric converters, high-piezoelectric-constant materials such as PZT are not compatible with conventional IC process. Most research so far use bulk fabricated materials to form the cantilever beam, which is not suitable for the integration with microsystem technology.

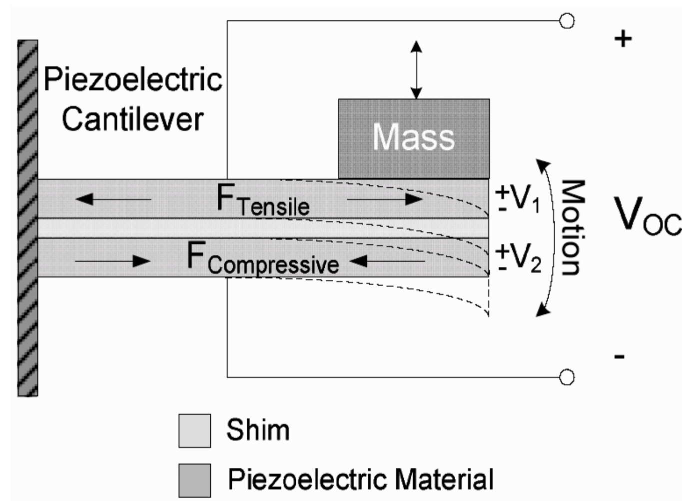


Fig. 1.5 Bimorph cantilever beam piezoelectric energy converter

1.3.3 Electrostatic capacitive energy conversion

Electrostatic capacitive energy conversion utilizes a variable capacitor to convert vibration energy into electric energy. The electrical energy W stored in a capacitor with capacitance C and voltage V is $W = \frac{1}{2}CV^2 = \frac{1}{2}\frac{Q^2}{C}$. If the capacitance of a pre-charged capacitor with constant charge Q is decreased due to vibration, the stored electrical energy in the capacitor will increase, thus converting the kinetic energy into electrical energy. The main concern of the capacitive energy conversion is how to extract the stored electrical energy in a properly controlled timing scheme. Capacitive energy conversion is more suitable for the steady frequency moderate amplitude

vibration source mentioned before. More detail on such charge-discharge conversion cycle operation is given in Chapter 2.

Design of the capacitive energy converter was carried out by Meninger et al. [23]. Comb structured variable capacitors were fabricated on silicon on insulator (SOI) wafers by MEMS technology. Simulation showed an output power of 8.6 μW with a device size of 1.5 cm × 0.5 cm × 1 mm from a 2.52 kHz vibration source. Another design was proposed by Roundy [15], which can achieve an output power density of 110 $\mu W/cm^3$ from a vibration with amplitude of 2.25 m/s^2 and frequency of 120 Hz.

MEMS variable capacitors can be fabricated through mature silicon-based micromachining process. Therefore, the capacitive energy converter is compatible with conventional IC process. It can also provide high output voltage and adequate power density. The drawback of the converter is that it needs an external voltage source V_{in} to charge the variable capacitor. Thus the life time of the external voltage source must be considered. This issue can be alleviated by employing inductive flyback circuitry proposed by Bernard et al. [27], which constantly feeds back the temporary stored energy to the external voltage supply for further usage.

The extraction of the energy in capacitive energy conversion must be accurately timed in order to optimize the conversion efficiency. A prototype circuitry for capacitive energy conversion was proposed by Roundy [15], in which the two switches were realized by diodes. However, this model results in an excessive output power reduction due to the far from ideal operation of the diodes. Other researches [27-29] utilized gate clocked MOSFET switches or other circuit configuration. Problems such as power consumption by the electronics or parasitic capacitive and resistive coupling still exist in these designs, not to mention the non-synchronous operation of the circuitry with the input vibration. Therefore, improved switch design is critical for better energy conversion efficiency.

1.3.4 Summary on vibration energy conversion technologies

According to the above literature survey, electrostatic capacitive vibration-to-electric energy conversion is used to scavenge ambient vibration energy due to its compatibility to IC processes, ubiquity in the environment and sufficient output power density. A novel mechanical switch is proposed to address the timing switch issues in current technology as the focus of this thesis.

1.3.5 Progress in previous generation devices

Capacitive energy conversion by our team has been conducted in the past [30]. The achievements of the earlier generations of devices prior to this thesis include the preliminary modeling and optimization of the device, the fabrication process development (including backside substrate removal), and the measurement system setup. However, electrical power output has not been measured due to limited number of devices after final assembly. Therefore, this thesis will continue on the basis of the previous effort to improve the device in all aspects of interest, especially the power output measurement.

1.4 Thesis objectives and organization

Most of the works on capacitive vibration-to-electric energy conversion were focused on the backend power electronics. Literature survey and our previous effort [30] show that design optimization and fabrication processes of the MEMS variable capacitor itself can still be improved. New switches for charge-discharge control are also needed in order to eliminate the defects mentioned above. Therefore, the objectives of this thesis are:

(a) Improve the design of the MEMS variable capacitor in order to maintain

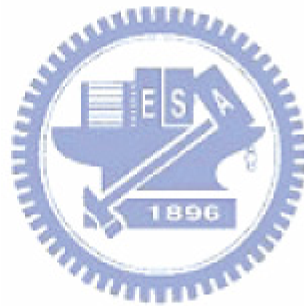
steady operation and eliminate unwanted parasitic effects,

(b) Propose novel mechanical switches for charge-discharge conversion timing control,

(c) Construct the dynamic model of the converter including the capacitor unit and the mechanical switches,

(d) Fabricate and conduct preliminary measurement on the devices

The organization of this thesis is as the following. Design and analysis of the converter is given in Chapter 2. The fabrication process and technology are discussed in Chapter 3. Preliminary measurement results of the fabricated converter are presented in Chapter 4. Finally, conclusion and future work are discussed in Chapter 5.



Chapter 2 Principle and Design

The basic concept of the capacitive energy converter is the conversion of kinetic energy into electrical energy when a pre-charged variable capacitor is displaced by external vibration. Furthermore, the extraction of the electrical energy relies on a switching mechanism which is realized mechanically in this thesis. In order to achieve greater conversion efficiency, the variable capacitor, charge-discharge switches and output storage component must all be designed with care, as discussed in this chapter.

2.1 Operation principle

The converter is composed of an auxiliary battery supply V_{in}, a vibration driven variable capacitor C_v and an output storage capacitor C_{stor}, which is connected to the load R_L, as shown in Fig. 2.1. Two switches, SW1 and SW2, are used to connect these components and control the charge-discharge conversion timing [30]. The variable capacitor serves as the conversion transducer and the auxiliary battery supply is used to pre-charge the capacitor.

A basic operation cycle begins when the variable capacitor C_v is charged by the auxiliary voltage supply V_{in} through SW1 at its maximum C_{max}. After C_v is charged to V_{in}, SW1 is opened and the capacitance changes from C_{max} to C_{min} due to vibration

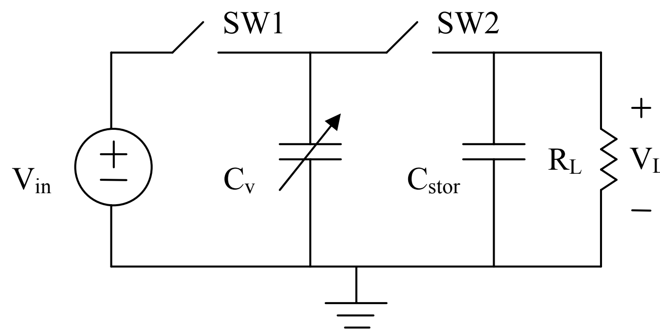


Fig. 2.1 Operation of the electrostatic energy converter

driven displacement. In this process, the charge Q on the capacitor remains constant (SW1 and SW2 both open). Therefore, the terminal voltage on the capacitor is increased, converting the kinetic energy of vibration into electrical energy stored in C_v. When the capacitance reaches C_{min} and terminal voltage reaches V_{max}, SW2 closes and allows C_{stor} to be charged by C_v through charge redistribution, transfering the energy to the output port. SW2 is then opened and C_v varies back to C_{max}, preparing for the next conversion cycle. During this period, the charge on C_{stor} is dissapated through the load resistance R_L with a time constant $\tau = R_L C_{stor}$ before it is charged again by C_v, as shown in Fig. 2.2. The DC level of the output will increase with each charging process. The output voltage V_L will eventually reach the steady state when the initial and final voltages of the charge-discharge process become equal.

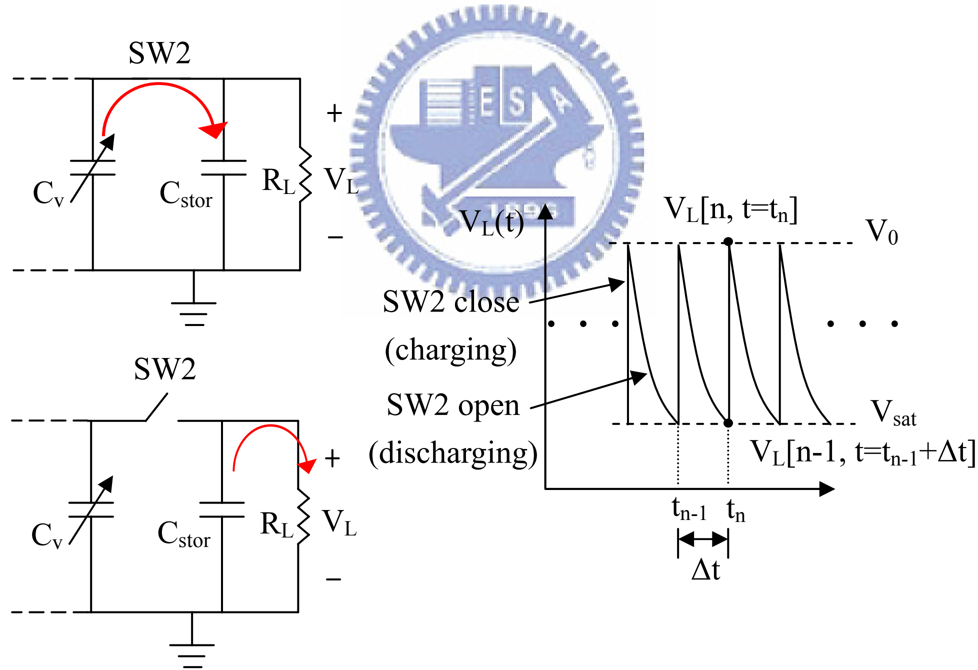


Fig. 2.2 Charge transfer process from C_v to output port

Let the conversion cycle time be Δt, the output voltage variation of the n-th cycle before and after the charge transfer can be expressed as

$$V_L[n, t = t_n] = \frac{V_L[n\text{-}1, t = t_{n\text{-}1} + \Delta t] C_{stor} + V_{max} C_{min}}{C_{stor} + C_{min}}, \tag{2.1}$$

where V_{max} is equal to $V_{in}C_{max}/C_{min}$, $V_L[n\text{-}1,\ t = t_{n-1}+\Delta t]$ is the voltage before the charge transfer, and $V_L[n,\ t = t_n]$ is the voltage after the charge transfer. After SW2 is opened, the output voltage in this charge dissiaption period is

$$V_L[n, t = t_n + \Delta t] = \frac{V_L[n\text{-}1, t = t_n + \Delta t]C_{stor} + V_{max}C_{min}}{C_{stor} + C_{min}} \times \exp(-\Delta t / R_L C_{stor}). \qquad (2.2)$$

With relatively large time constant $\tau = R_L C_{stor}$, the net charge transfer to C_{stor} is positive, resulting in a rise of V_L cycle by cycle. In the steady state, the net increment of charge transfer to C_{stor} becomes zero and the initial and final values of V_L become the same ($V_L[n,\ t = t_{n-1}+\Delta t] = V_L[n\text{-}1,\ t = t_{n-1}+\Delta t]$). Defined as V_{sat}, the final saturation voltage of the output terminal can be derived as

$$V_{sat} = \frac{\frac{C_{max}}{C_{stor}} V_{in}}{(1+\frac{C_{min}}{C_{stor}}) \times \exp(\Delta t / R_L C_{stor}) - 1}, \qquad (2.3)$$

where Δt = conversion cycle time = 1/2f and f is the vibration frequency. The average output power can be calculated as,

$$P(t) = \frac{V_L^2(t)}{R_L} = \frac{(V_0 e^{-t/R_L C_{stor}})^2}{R_L}, \qquad (2.4)$$

$$P_{out} = \frac{1}{\Delta t}\int_0^{\Delta t} P(t)dt = \frac{C_{stor}V_0^2}{2\Delta t}[1-\exp(\frac{-2\Delta t}{R_L C_{stor}})] \approx \frac{V_{sat}^2}{R_L}, \qquad (2.5)$$

where $V_0 = V_{sat} \times e^{\Delta t / R_L C_{stor}}$, as in Fig. 2.2. The approximation takes place when $\Delta t \ll R_L C_{stor}$, which also results in a small output voltage ripple.

2.2 Preliminary study

Before the design and analysis of the device and its components, the characteristics of various ambient vibration sources and battery supplies are studied to determine the targeted vibration source and the auxiliary battery supply.

2.2.1 Characteristics of vibration sources

In order to determine the achievable output power, the acceleration amplitude and frequency of the vibration source must be known beforehand. Measurement of different vibration sources was conducted by Roundy [10], as shown in Fig. 2.3. From the spectra of these low-level vibrations, a few points can be observed. First, a common low frequency fundamental peak (usually near 120 Hz) exists in a wide range of ambient vibration sources. Second, the acceleration amplitude is either constant or decreasing with frequency, in which no amplitude peaks appear in higher frequencies. This type of steady moderate vibration source is a suitable input for capacitive energy conversion. Designing the device dynamics to resonate with the input vibration will also greatly improve the conversion efficiency.

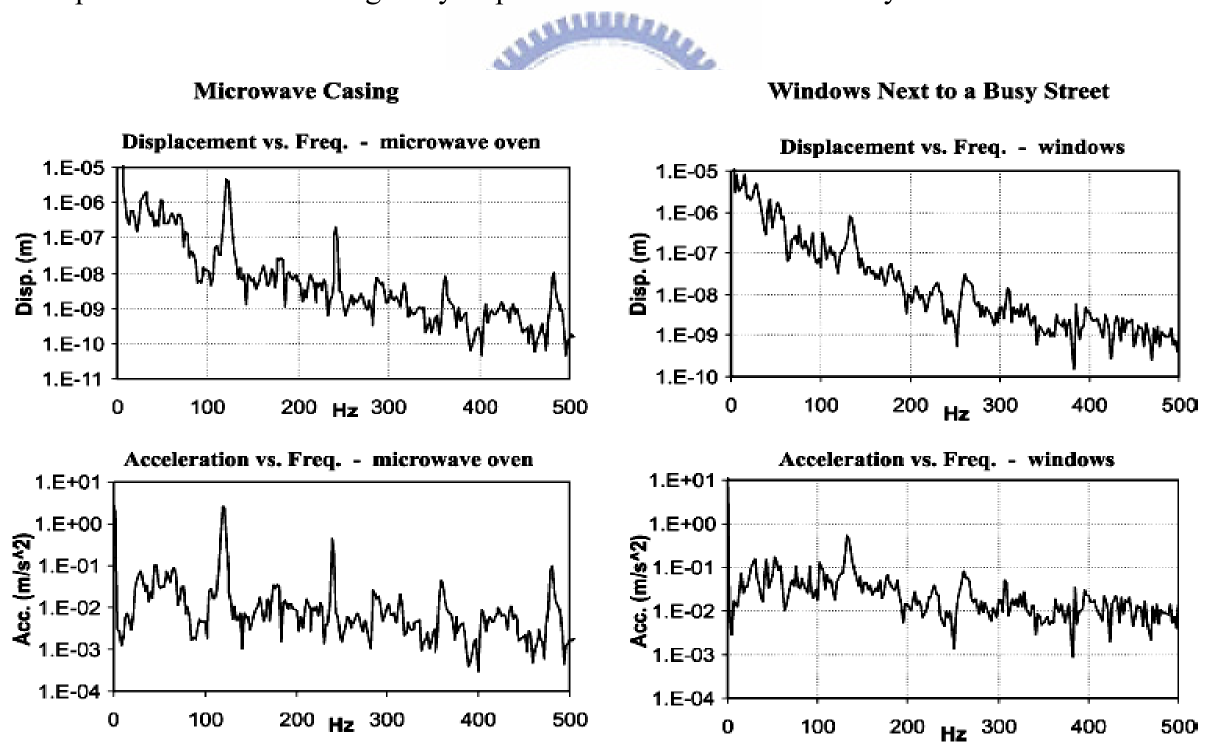


Fig. 2.3 Vibration spectra by Roundy [10]

Our own measurement of the vibration of an air conditioner is shown in Fig. 2.4. A fundamental vibration frequency similar to those acquired by Roundy can be

observed with an acceleration amplitude of about 2.25 m/s^2. Therefore, the vibration source with a peak acceleration of 2.25 m/s^2 and frequency of 120 Hz is chosen as our targeted input vibration source due to its common existence. It should be noticed that operating at such low frequency is not common for typical MEMS device, thus an external mass attachment is required.

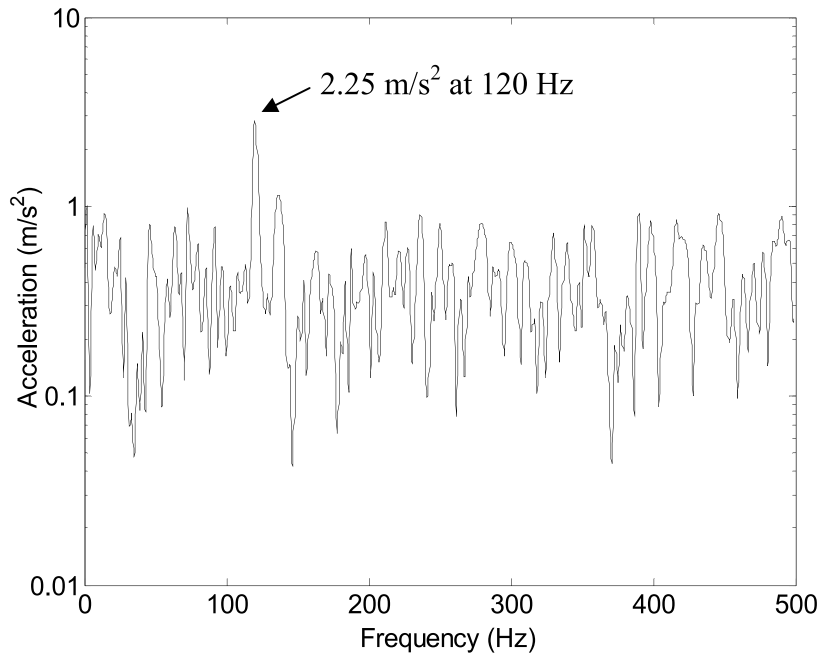


Fig. 2.4 Vibration spectrum of an air conditioner

2.2.2 Auxiliary battery supply

The auxiliary battery supply is used to pre-charge the variable capacitor through SW1, similar to the charge pumping technique. When the ambient does not have vibration for the converter to provide enough power, the battery can also serve as the main voltage supply. The converted energy can also be restored back into the battery supply through an additional inductive flyback circuitry [27]. In this case, it functions as a general storage device and provides power more smoothly.

Typical storage devices include capacitors, inductors and batteries. Capacitors and inductors have lower energy density. They often serve as short-term energy

storage cells. Batteries, such as NiZn, NiMH, NiCd, and Lithium-ion (Li-ion), store energy chemically and are rechargeable. Among these types, Li-ion batteries (Fig. 2.5) offer the best performance with high energy density, high discharge rate, high cell voltage, long life span, and no “memory” effects. The disadvantage is the higher sensitivity to over charging and discharging, which will damage the battery permanently [31]. In this study, LIR1620 (3.6 V, Φ 16 mm, H 2.2 mm, 1.2 g) and LIR2016 (3.6 V, Φ 20 mm, H 1.8 mm, 1.6 g) Li-ion cells can be used as the auxiliary battery supply. Moreover, the battery can act as part of the external mass if it is well bonded on the device.

Fig. 2.5 Lithium-ion rechargeable battery

2.3 Device design

The analysis of the device operation, structural design of the variable capacitor and, and simulation of the device dynamic behavior is discussed in this section. The design is focused on the modeling and optimization of the capacitive energy converter with two ideal switches. The mechanical design of the two switches is discussed in the next section. In the design flow, MEMS fabrication capability is considered in order to obtain feasible parameters.

The design is iterated between the static and dynamic analyses due to the influence of the maximum capacitance C_{max} on the mechanical spring constant k,

known as the electrostatic spring softening effect. Design constraints on k and m sets a limit on C_{max} (approximately below 2000 pF), and thus influencing the static design on the variable capacitor. Under these limitations, the device is optimized to achieve maximum output power.

2.3.1 Static analysis

The static analysis is conducted to obtain mathematical guidelines for deciding overall parameters and output specifications. With the discharge time constant $\tau = C_{stor}R_L$ designed much larger than the conversion cycle time Δt to minimize the output ripple, Eq. (2.3) can be simplified as

$$V_{sat} \approx \frac{C_{max}V_{in}}{C_{min}\left(1+\frac{\Delta t}{R_L C_{min}}+\frac{\Delta t}{R_L C_{stor}}\right)}. \tag{2.6}$$

C_{min} is usually relatively small (about 100 pF). The other circuit components can be chosen such that $C_{stor} >> C_{min}$ and $R_L C_{min} << \Delta t$. Therefore, Eq. (2.6) can be further simplified as

$$V_{sat} \approx \frac{C_{max}V_{in}}{C_{min}\frac{\Delta t}{R_L C_{min}}} = \frac{C_{max}V_{in}}{\Delta t}R_L. \tag{2.7}$$

The output power now becomes

$$P_{out} \approx \frac{V_{sat}^{\ 2}}{R_L} \approx \left(\frac{C_{max}V_{in}}{\Delta t}\right)^2 R_L. \tag{2.8}$$

From Eq. (2.7) and Eq. (2.8), it can be seen that the output power is basically proportional to $C_{max}^{\ 2}$ and R_L.

A maximum device area of 1 cm^2 was set as the device size constraint. The output should have a voltage below 40 V for further integration with power management circuits. With V_{sat} equal to 40 V for maximum output power, it is seen

from Eq. (2.7) that the load R_L must increase due to limited C_{max}. This increase of R_L will result in a decreased output power (Eq. (2.8)). With a limited value of C_{max} = 1570 pF, R_L is chosen as 50 MΩ, resulting in a corresponding output power of 31 μW. C_{stor} generally does not influence the output power but has a tradeoff between the output voltage ripple and the saturation time. For a output voltage ripple lower than 1 V, C_{stor} was chosen to be 5 nF.

2.3.2 Variable capacitor design

Deep silicon etching technology and SOI wafers with highly doped thick device layers were used to fabricate the devices. From [30], an in-plane gap-closing comb structure is used for the variable capacitor, as shown in Fig. 2.6. Compared with the in-plane overlap type comb structures, this topology has the advantage of larger capacitance change for smaller displacement. Compared with the out-of-plane capacitors, this topology has the advantage of lower mechanical damping loss and possibility to incorporate minimum gap control designs.

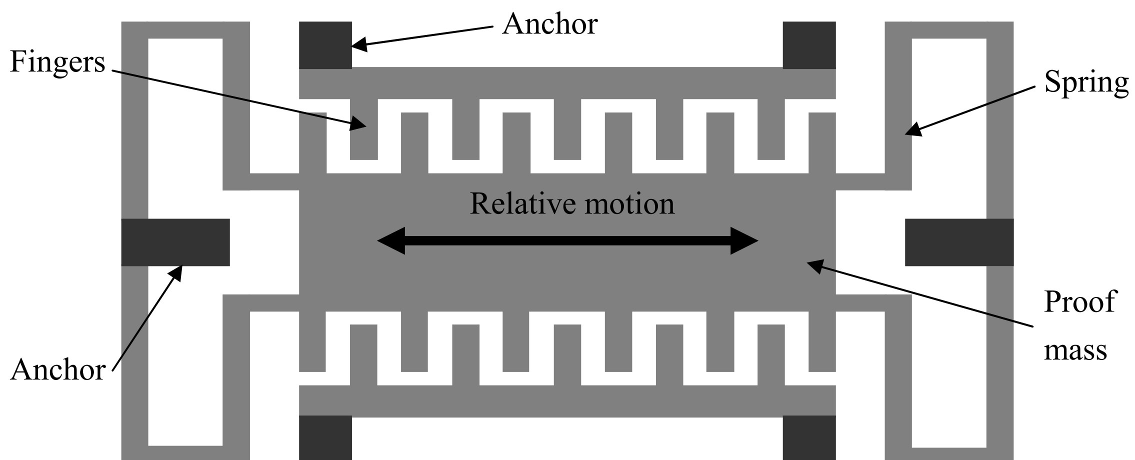


Fig. 2.6 Top view of the in-plane gap closing variable capacitor topology

The symbols used in the following discussion are listed below:

d: gap between comb fingers

d_{air}: minimum air gap between fingers

W_f: comb finger width

L_f: overlap length of comb fingers

h: thickness of device layer

N_g: number of variable capacitor cells

x_r: relative displacement between movable and still electrodes

t: thickness of silicon nitride sidewall dielectric coating

ε_0: permittivity of free space ($\varepsilon_0 = 8.842 \times 10^{-12}$ F/m)

ε_r: relative permittivity of silicon nitride ($\varepsilon_r = 7$)

μ: viscosity of air at 1 atm ($\mu = 1.82 \times 10^{-5}$ Pa-sec)

α: damping coefficient depending on effective region ($\alpha \approx 1.74$)

Q: charge on the variable capacitor

Figure 2.7 (a) shows the comb finger design where silicon nitride is applied to the device sidewall for electrical insulation. Another purpose of the silicon nitride coating is to significantly increase C_{max} without altering C_{min}. As shown in the series capacitance model in Fig. 2.7 (b), the equivalent air gap of the capacitor is $d_{eq} = d - 2t + \frac{2t}{\varepsilon_r}$ with dielectric thickness t and relative permittivity ε_r. The equivalent capacitance is increased only when d is relatively small at the C_{max} position.

The finger width W_f is designed as 10 μm due to deep silicon etching limits on high aspect ratio structures. The comb finger length must be limited to 425 μm with a overlap length L_f of 400 μm. The minimum air gap d_{air} between the fingers is 0.5 μm.

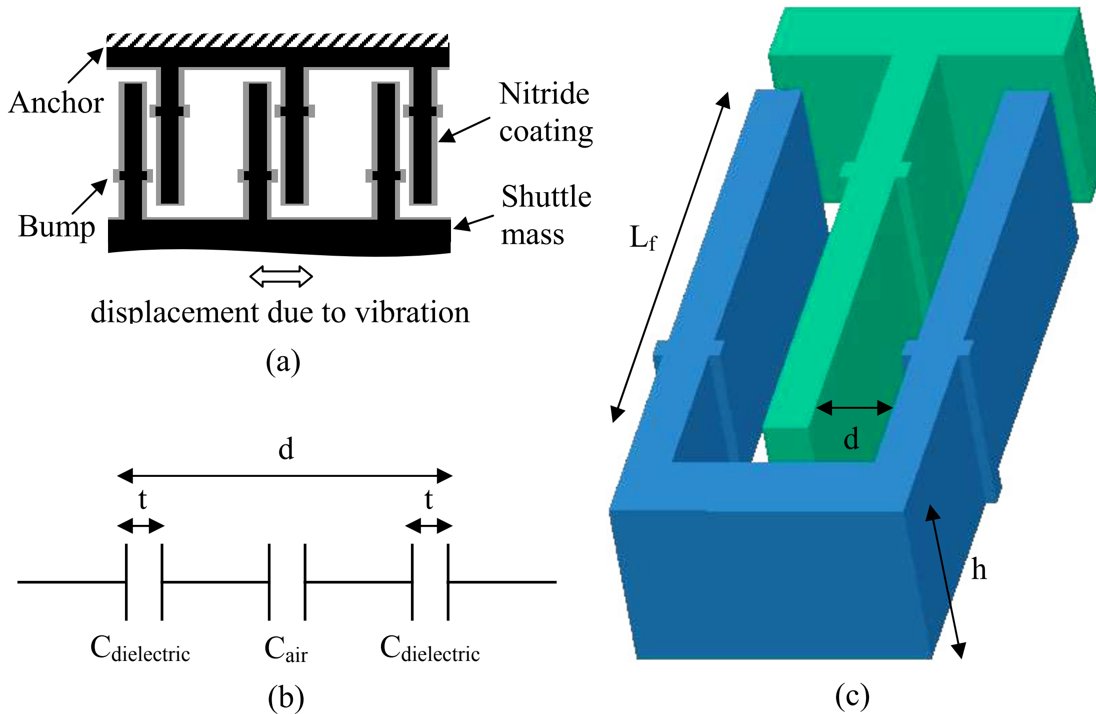


Fig. 2.7 (a) Close up view of fingers with silicon nitride sidewall coating, (b) equivalent capacitance model between fingers, (c) schematic view of one finger cell with the bump design

There are two reasons to set these restrictions on the finger design. First, they are used to properly limit the maximum capacitance C_{max} mentioned in p. 21. Second, it is used to prevent the electrostatic pull-in between the fingers during the charging process at the C_{max} position. The fingers are designed with special "bumps" on the sidewalls (Fig. 2.7 (a), (c)) to provide a more compliant minimum air gap control between electrodes. These bumps do not alter the capacitance due to their relatively small size.

With the sidewall dielectric coating and the removal of the substrate beneath the movable plate to eliminate parasitic capacitance, the total variable capacitance between comb fingers is [32]

$$C_v(x_r)=N_g\varepsilon_o L_f h\left(\frac{2(\frac{2t}{\varepsilon_r}+d-2t)}{(\frac{2t}{\varepsilon_r}+d-2t)^2-x_r^{\ 2}}\right). \qquad (2.9)$$

The mechanical damping force for large displacement is [33, 34]

$$F_m = b_m(x_r)\dot{x}_r = \left(\alpha \frac{\mu N_g L_f h^3}{(d-2t)^3 \left[1-(\frac{x_r}{d-2t})^2 \right]^{1.5}} \right) \dot{x}_r, \tag{2.10}$$

with $b_m(x_r)$ as the equivalent mechanical damping constant. Only squeeze film damping between fingers is considered due to the backside substrate removal. Notice that $b_m(x_r)$ is a nonlinear function of x_r. It behaves as a normal damper for small displacements, but causes a large damping force when device approaches the maximum displacement. The electrostatic force induced by the charge Q on C_v is [32]

$$F_e = b_e x_r = \left[\frac{-Q^2}{2N_g \varepsilon_o L_f h(\frac{2t}{\varepsilon_r} + d-2t)} \right] x_r. \tag{2.11}$$

This force acts as a negative spring force with b_e as the electrostatic spring constant. The electrostatic spring constant is determined by the charge Q on the variable capacitor, which varies in the charge-discharge process. The maximum value depends on $Q_{max} = C_{max}V_{in}$. This maximum electrostatic spring constant b_{e_max} will reduce the mechanical spring constant of the device. Therefore it needs to be limited as low as possible. This addresses the need to limit the value of C_{max} of the variable capacitor mentioned before.

The output power versus variable capacitor parameters is calculated according to Eq. (2.5) and Eq. (2.9). Device thickness h is 200 μm to have large capacitance and robust structure. It is also a reasonable depth for fabrication. Output power increases with decreasing sidewall nitride thickness t. Therefore, a rather thin but reasonable thickness of 500 Å is used. With the above design parameters, the relationship of the output power P_{out} and maximum electrostatic spring constant b_{e_max} to the initial finger gap d is shown in Fig. 2.8. The output power of 31 μW can be achieved with

the initial finger gap of 26 μm, and the corresponding value of b_{e_max} is 774 μN/μm. With a maximum achievable number of variable capacitor finger cells N_g = 1126 by compact layout design, the capacitance change is from 62 pF to 1570 pF. Design parameters of the variable capacitor are arranged in Table 2.1.

Table 2.1 List of variable capacitor design parameters

Variable	**Description of variables**	**Designed value**
h	Device thickness	200 μm
N_g	Number of variable capacitor cells	1126
W_f	Finger width	10 μm
L_f	Finger overlap length	400 μm
L_{f_total}	Finger total length	425 μm
d	Finger initial gap	26 μm
d_{air}	Minimum air gap	0.5 μm
t	Silicon nitride sidewall thickness	500 Å
C_{max}	Maximum value of capacitance	1570 pF
C_{min}	Minimum value of capacitance	62 pF
b_{e_max}	Maximum electrostatic spring const.	774 μN/μm
R_L	Driven load resistance	50 MΩ
C_{stor}	Output temporary storage capacitor	5 nF
V_{out}	**Output voltage (steady state)**	**40 V**
P_{out}	**Output power (steady state)**	**31 μW**

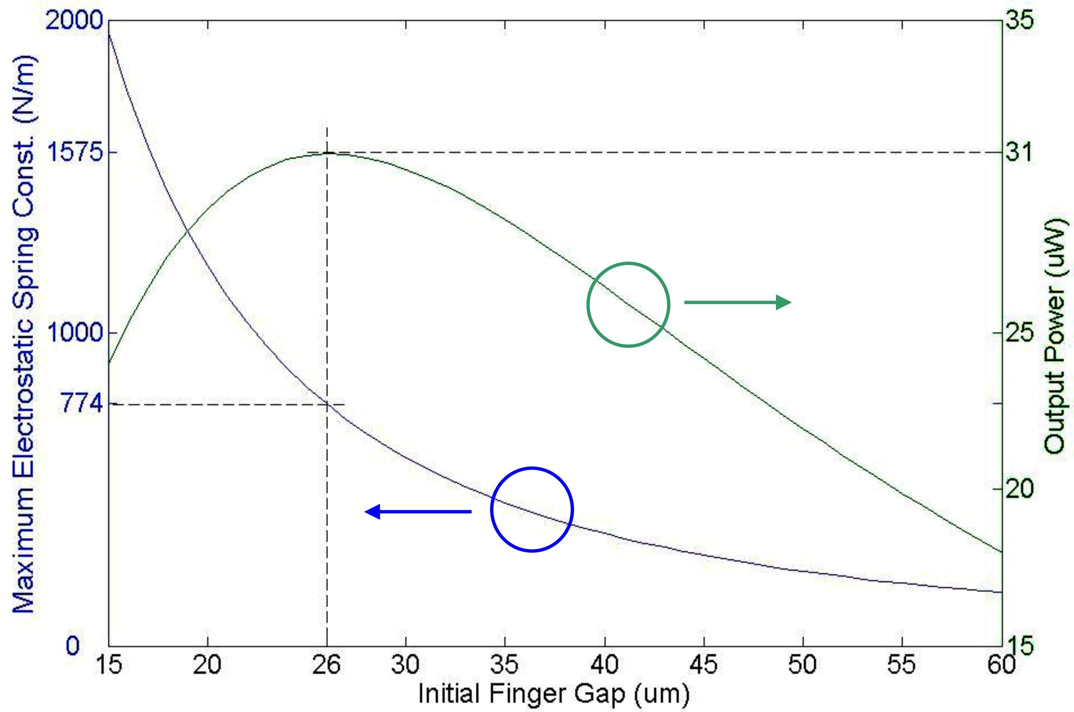


Fig. 2.8 Output power and maximum b_e versus initial finger gap

2.3.3 Dynamic analysis

The dynamic analysis is performed to decide the mechanical spring constant k and proof mass m in order to achieve the desired maximum displacement under the targeted input vibration. The electro-mechanical dynamics of the variable capacitor can be modeled as a spring–damper-mass system, as shown in Fig. 2.9.

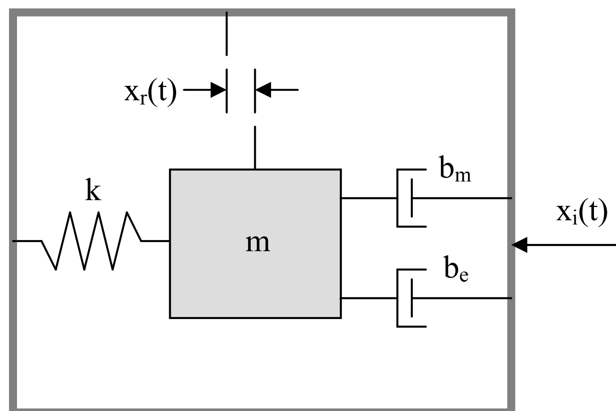


Fig. 2.9 Schematic of the conversion dynamic model

The dynamic equation is

$$m\ddot{x}_r + b_e x_r + b_m(x_r)\dot{x}_r + kx_r = -m\ddot{x}_i, \tag{2.12}$$

where x_i is the displacement of the device frame caused by the ambient vibration, x_r is the relative displacement between movable and still electrodes, $b_m(x_r)\dot{x}_r$ is the mechanical damping force caused by the squeezed film damping effect (Eq. 2.10), and $b_e x_r$ is the electrostatic force caused by the charge on the capacitor (Eq. 2.11).

Equation (2.12) indicates a nonlinear system caused by the mechanical damping constant $b_m(x_r)$. In order to simplify the design, constant damping constant determined from the range of $b_m(x_r)$ is used to approximate the original system. For a sinusoidal vibration source with complex amplitude $\tilde{X}_i$ and frequency ω, and relative displacement with complex amplitude $\tilde{X}_r$, Fourier transform is applied to solve the equation and yield

$$-m\omega^2\tilde{X}_r + j\omega b_m\tilde{X}_r + (k+b_e)\tilde{X}_r = -m\omega^2\tilde{X}_i, \tag{2.13}$$

$$\left|\tilde{X}_r\right| = \frac{m\omega^2}{\sqrt{(k+b_e-m\omega^2)^2 + b_m{}^2\omega^2}}\left|\tilde{X}_i\right|. \tag{2.14}$$

The solution shows that the equivalent spring constant of the system is k' = k + b_e, which is "softened" by the negative electrostatic spring b_e. Thus, the resonant frequency of the system is now

$$\omega_n = \sqrt{\frac{k+b_e}{m}}, \tag{2.15}$$

which indicates unsteady resonance due to the time varying electrostatic spring constant b_e. In order to maintain steady resonance, the mechanical spring constant k should be relatively larger than the maximum value of b_e (b_{e_max}). Shown in Fig. 2.10 is the relationship of the needed k/b_{e_max} ratio in order to achieve the desired maximum displacement of 25.4 μm at resonance.

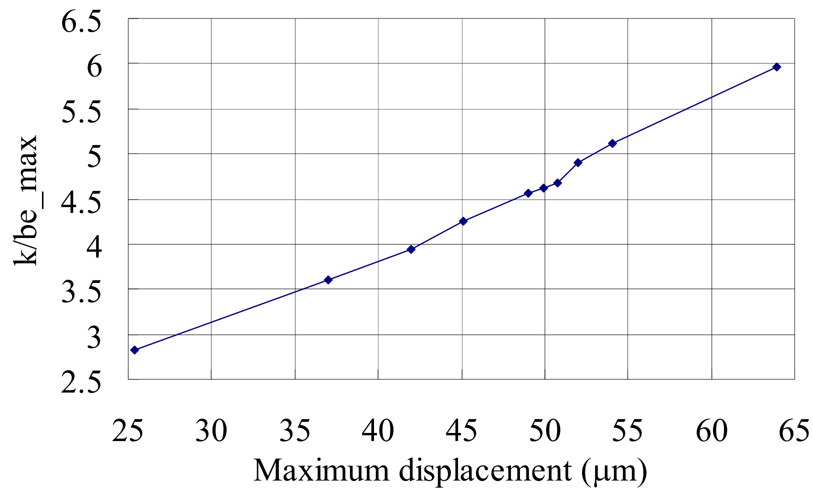


Fig. 2.10 The needed k/b_{e_max} ratio versus maximum displacement

The k/b_{e_max} ratio increases proportionally with the needed maximum displacement in the displacement range of concern. This is due to the larger restoring force the spring has to offer in order to reach the larger maximum displacement. Therefore, the mechanical spring constant k can be decided directly from the knowledge of b_{e_max} and maximum displacement of x_r. The proof mass of the system can then be obtained from

$$\omega_n = \sqrt{\frac{k + b_e}{m}} \approx \sqrt{\frac{k}{m}} \tag{2.16}$$

when the mechanical spring constant k is determined. The proof mass must be limited due to the device size constraints and the weight carrying ability of the device itself. For a conservative design, a spring constant k of 2425 N/m with a proof mass m of 4 grams is chosen to ensure maximum displacement during device resonance.

Dynamic response of the device was simulated by Simulink. The block diagram is shown in Fig. 2.11. The “MEMS_structure” block simulates the dynamics of the variable capacitor with constant charge, while the “Qcontrol” block decides the value of the charge during the charge-discharge process. The “SW1_Q_{max}” block determines

the operation of SW1 from the displacement, and the maximum value of charge on the capacitor. Similarly, the "SW2_Q_{min}_Output" block serves as the SW2 operation control and generates the output power together with the output charge redistribution information. The operation of SW1 and SW2 is considered ideal. SW1 closes when maximum displacement is reached; SW2 closes when maximum voltage on capacitor is reached. A more realistic model considering switch timing will be constructed and discussed in next section. Detailed information on the model and function blocks can be seen in the appendix.

Fig. 2.11 Simulink model of device with ideal switch operation

Figure 2.12 shows the time response of the relative displacement x_r of the variable capacitor. Maximum displacement is reached after approximately 0.02 s, and

then the device undergoes steady vibration between -25.4 μm to 25.4 μm. When the maximum displacement is reached, charging to C_v begins. The time response of the charge on C_v is shown in Fig. 2.13. The maximum charge is 5660 pC, while the lower charge level increases by each cycle and saturates to a value of 2410 pC. Closer view of the displacement z and charge Q in steady state is shown in Fig. 2.14, which shows that the charge-discharge process operates at twice the frequency of the vibration.

The simulated time response of the output voltage is shown in Fig. 2.15. The saturation voltage is close to the expected 40 V. The saturation time is about 0.4 seconds. The close up view of the steady state response shows that output voltage ripple is indeed below 1 V.

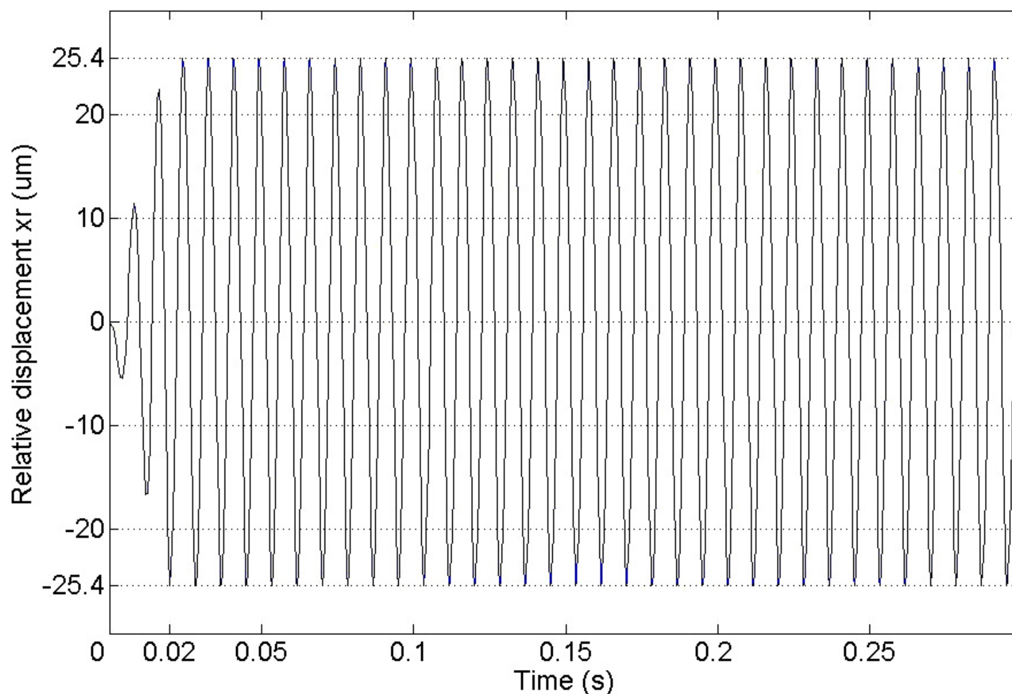


Fig. 2.12 Time response of the relative displacement x_r

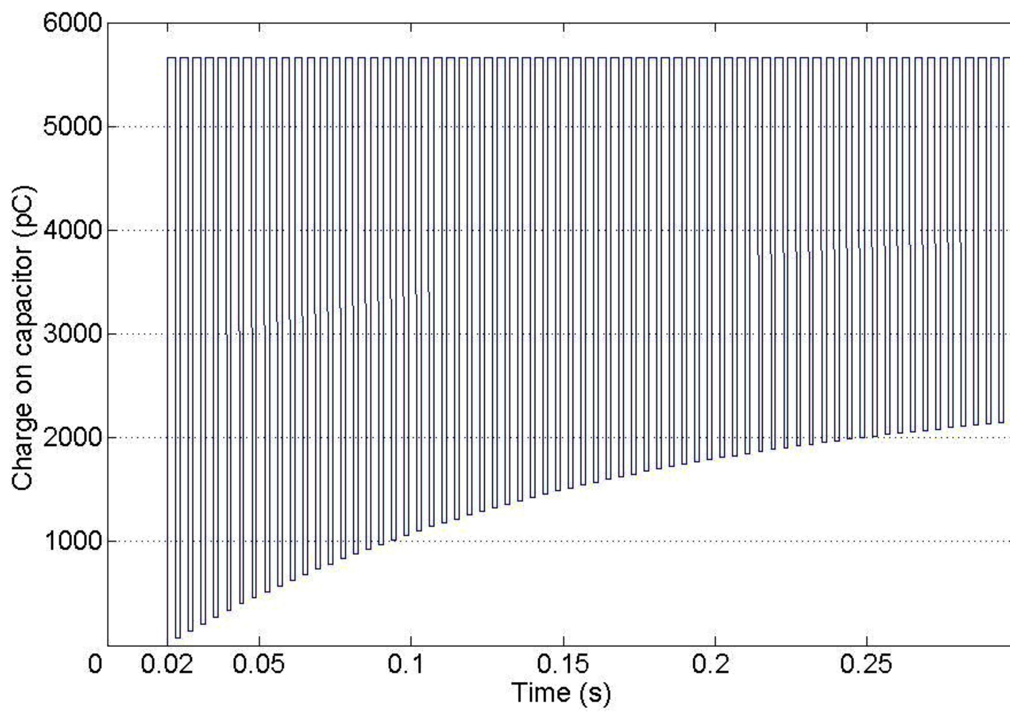
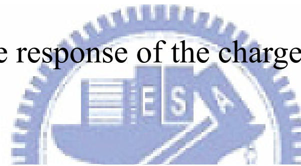


Fig. 2.13 Time response of the charge Q on capacitor



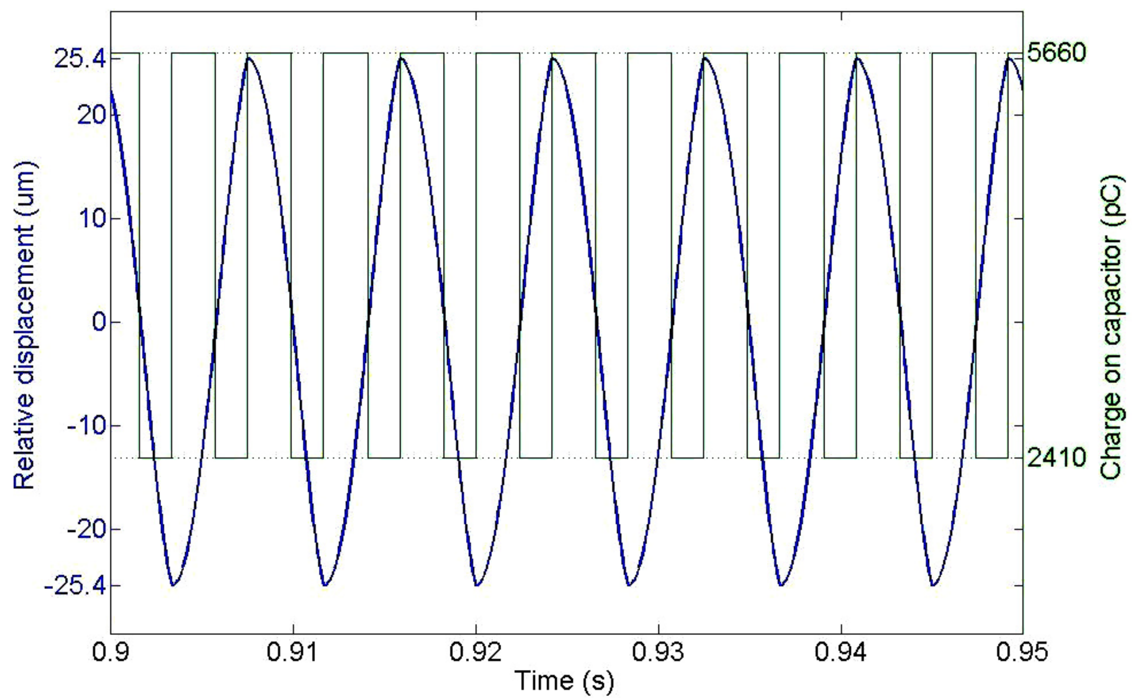


Fig. 2.14 Steady state displacement and charge operation

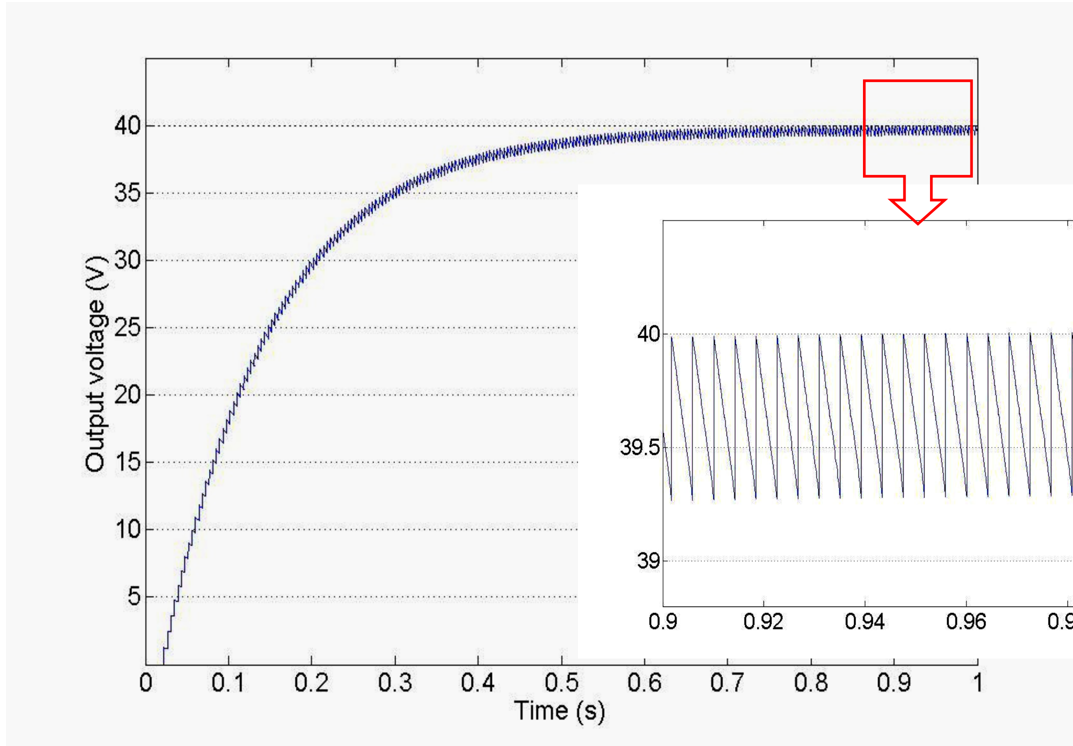


Fig. 2.15 Output voltage time response

2.3.4 Spring design

In the variable capacitor design, the mechanical springs are arranged on the two sides of the shuttle mass. The primary deformation is along the direction of the relative displacement x_r. The springs have conventional folded serpentine structures, as shown in Fig. 2.16. Each spring consists of two beams connected by a truss. If the truss is assumed rigid, the spring constants in different directions are [35],

$$k_z = N\frac{Eh^3W_k}{2L_k^3}, \tag{2.17}$$

$$k_x = N\frac{EhW_k^3}{2L_k^3}, \tag{2.18}$$

$$k_y = N\frac{EhW_k}{2L_k}. \tag{2.19}$$

The number of springs N is 20 in the concentrated layout floor-planning. h is the thickness of the springs. E is the Young's modulus of single crystal silicon. L_k and W_k are the length and width of the beams. As seen in Fig. 2.16, k_x in the x direction is the

main spring constant used for device design.

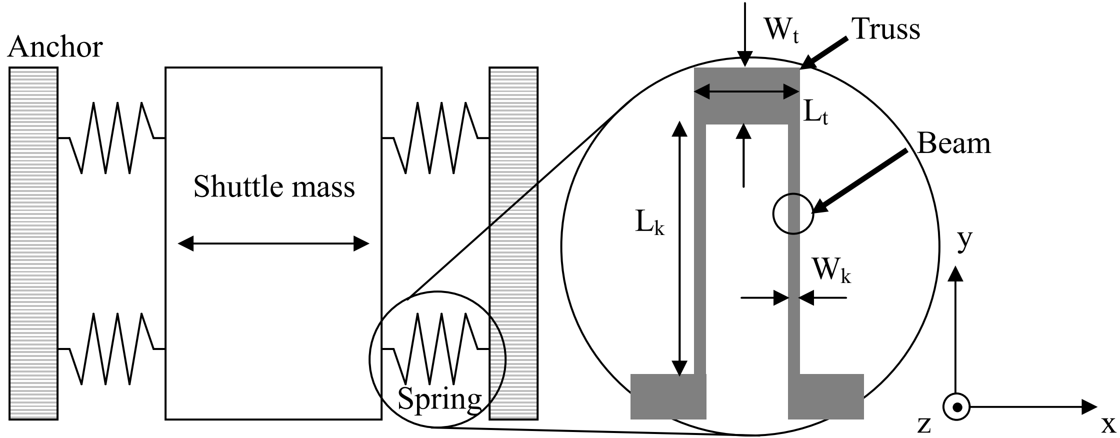


Fig. 2.16 Spring structure schematic view

Typical Young's modulus of single crystal silicon is 169 GPa in the <110>-type direction, 130 GPa in the <100>-type direction, and 190 GPa in the <111>-type direction. The SOI wafers in which the devices are fabricated have a heavily doped p-type device layer with <100> orientation. The device will be fabricated in the direction parallel to the flats of the wafer. Therefore, the <110>-type Young's modulus will be utilized. Influence of heavy doping on the Young's modulus is ignored.

If the effect of non-rigid truss is considered, the above spring constants should be multiplied by a coefficient λ [36],

$$\lambda=\frac{a^2+16as^3+44s^6}{4a^2+34as^3+44s^6}, \tag{2.20}$$

where a is the truss length to beam length ratio (L_t/L_k) and s is the truss width to beam width ratio (W_t/W_k). In our spring design, L_t = 53 μm, L_k = 574 μm, W_t = 40 μm and W_k = 11 μm. The calculated λ is equal to 0.998, which implies that the effect of non-rigid trusses is small.

Several issues must be considered when designing the spring structure. The z-axis stiffness k_z and y-axis stiffness k_y should be relatively larger than the lateral x-axis stiffness k_x to reduce the out-of-axis motion. Static displacement due to weight mg of the external mass should be maintained small. The stress in the spring should be much smaller than the yield stress of single crystal silicon (7 GPa). The safety factor, defined as the yield stress divided by the maximum stress during deformation, is used to check the spring robustness. The maximum stress in the x and z directions for maximum displacement x_{max} and static weight loading mg are

$$\sigma_x = \frac{3EW_k x_{max}}{2L_k^2}, \tag{2.21}$$

$$\sigma_z = \frac{3mgL_k}{NW_k h^2}, \tag{2.22}$$

respectively.

For the device thickness of 200 μm, the vertical static load of 4 grams, the lateral maximum displacement of 25.4 μm, and the total number of 20 serpentine springs connected to the mass, Table 2.2 lists the spring dimensions, spring constants, the lateral and vertical stiffness ratio, and the safety factors. Fig. 2.17 shows the finite element method (FEM) simulation of a single spring element by CoventorWare. The total spring constant is designed to be 2425 N/m; thus a single spring element has a spring constant of 121.25 N/m. The simulation results agree well with the design value.

Fig. 2.18 shows the CoventorWare modal simulation of the device without the fingers. Simulation is performed with and without the external mass which is approximated by a cylinder with identical radius and mass to a 4 gram tungsten ball. Without the external mass, the first three modes are respectively the lateral mode, the vertical mode, and the torsional mode. With external mass attached, the second and third mode exchange orders due to the levitation of the center of mass. The first mode

Table 2.2 List of spring design parameters

Variable	Description of variables	Designed value
W_k	Spring Width	11 μm
L_k	Spring Length	574 μm
k_z	Vertical spring constant	8.01×10^5 μN/μm
k_x	X-axis spring constant	2425 μN/μm
k_y	Y-axis spring constant	6.6×10^6 μN/μm
k_z / k_x	Vertical stiffness ratio	331
k_y / k_x	Lateral stiffness ratio	2723
Sf_x	Lateral safety factor	32.5
Sf_z	Vertical safety factor	912.5

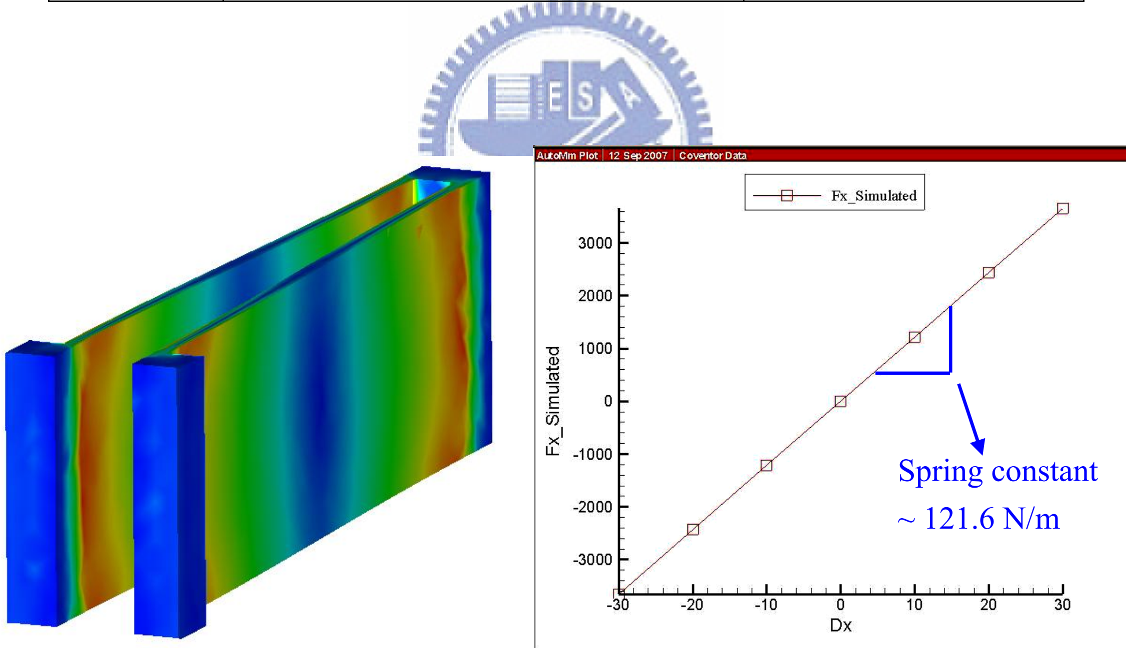
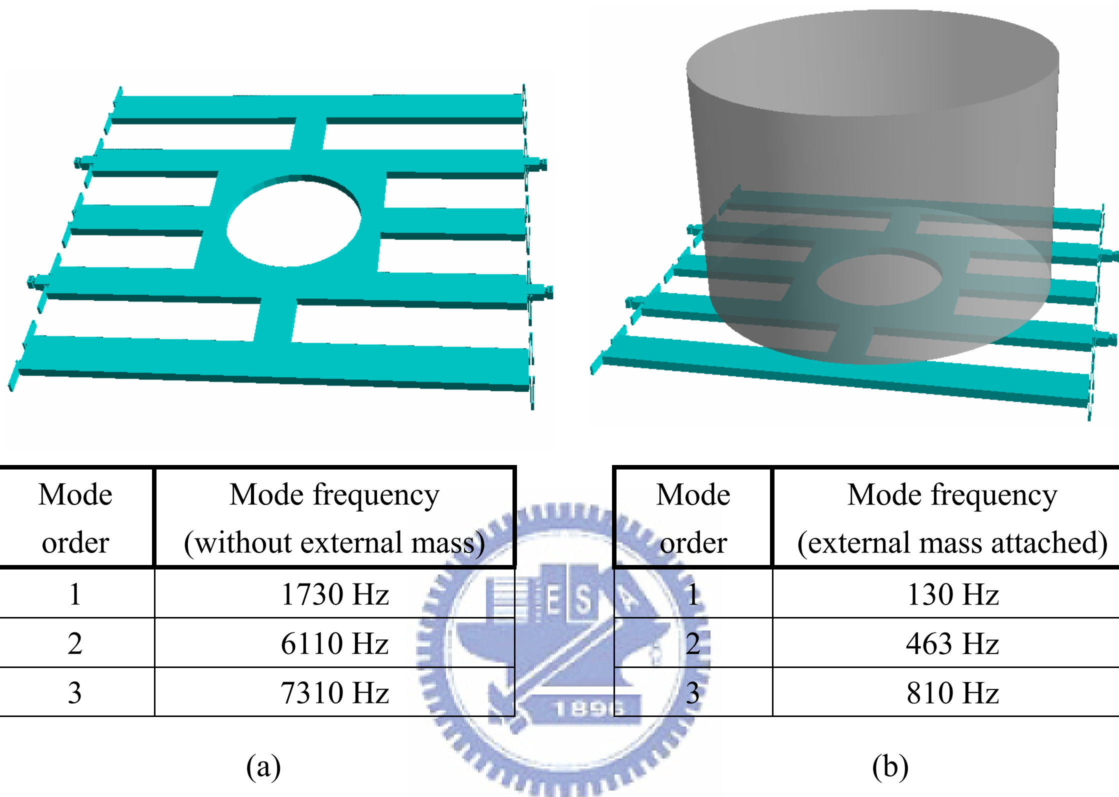


Fig. 2.17 CoventorWare simulation of the spring constant of a single spring element

frequency is 1.73 kHz without the external mass and 130 Hz with the external mass attached. The first mode frequency with the external mass differs from the desired value of 120 Hz. This is possibly due to the approximation of a ball by a cylinder

structure. Other mode frequencies are at least 3.5 times higher than the primary mode in both situations. The separation is large enough to avoid stimulation of these unwanted modes by the input vibration.



Mode order	Mode frequency (without external mass)
1	1730 Hz
2	6110 Hz
3	7310 Hz

(a)

Mode order	Mode frequency (external mass attached)
1	130 Hz
2	463 Hz
3	810 Hz

(b)

Fig. 2.18 CoventorWare modal analysis, (a) without external mass, (b) with external mass attached

2.3.5 Conversion efficiency

Figure 2.19 (a) shows the Q-V plane plot of the operation, which can be used to estimate the output power of such conversion process. The slopes of the lines are the capacitance in respective positions. The charge-discharge cycle starts from point A with no charge on C_v. The cycle proceeds to point B where C_v is charged to Q_{max} at the C_{max} position by V_{in}, and continues to point C where C_v changes to C_{min} and the voltage increases to V_{max}. At last, the operation assumes total discharging of C_v at the C_{min} position and returns to point A. The converted energy of this ideal cycle is the

area of the triangle ABC. Multiplying the area with the operation frequency yields ideal output power. The conversion efficiency is defined as the expected output power of the designed converter, which is 31 μW, divided by the ideal output power derived from Fig. 2.19 (a), which is 58.5 μW. The conversion efficiency is approximately 53 % in this case. Conversion efficiency is reduced by the incomplete discharging in the charge redistribution between C_v and C_{stor}. If this effect is considered, the Q-V plane is modified into Fig. 2.18 (b). The discharging process stops at Q_{min} (point D), and proceeds to point A' for another charging process. In the steady state situation, where Q_{max} is 5660 pC and Q_{min} is 2410 pC, the output power derived from the Q-V plane is 47.7 μW. Conversion efficiency is now 65 %. The reason why the conversion efficiency is not close to 100 % in this case is probably due to the energy loss during charge transfer from C_v to C_{stor}. A more accurate modeling of the conversion efficiency should be derived.

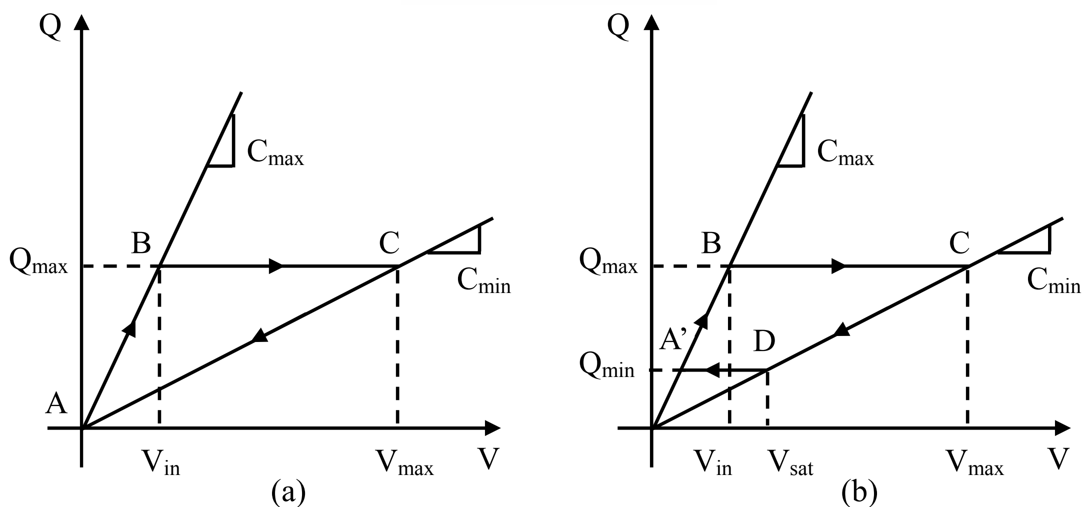


Fig. 2.19 Q-V plane (a) ideal operation, (b) operation with charge redistribution between C_v and C_{stor}

2.4 Mechanical switch

The switches SW1 and SW2 are realized as lateral contact mechanical switches. Conventional design of the charge-discharge timing control switches utilize diodes or clocked active switches [29-31]. In order to prevent charge leakage out of C_v and C_{stor}, the switches must have a reverse leakage current lower than a few nA. This is not common in commercially available diodes and other switching circuitry. Capacitive coupling is another problem, in which the capacitance of the switch contributes to parasitic capacitance. Our design of SW1 and SW2 has barely zero charge leakage and very low capacitance coupling effect. Other advantages are the low energy consumption, the synchronous operation to the variable capacitor, and the monolithic integration with the whole device structure.

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2.4.1 SW1 design

SW1 should ideally be closed when the variable capacitor is near the maximum displacement, and be opened immediately after charging is finished at the C_{max} position. In our design, SW1 is realized as a mechanical switch by a contact mechanism between nodes N1 and N2, as shown in Fig. 2.20. With one end connected to the movable proof mass of C_v and one end connected to the still charging electrode, SW1 laterally contacts at the C_{max} position when the comb fingers of the variable capacitor touch.

Layout of SW1 is also shown in Fig. 2.20. Considering the extra displacement the elastic finger configuration can allow, SW1 is designed to contact simultaneously when or merely after the fingers have touched. The finger bump design mentioned before is used to maintain a constant C_{max} during the SW1 charging process. SW1 is also designed with a restoring spring structure which deforms upon contact and

provides enough contact force to reduce contact resistance during charging. In a previous research [37], a sputtered gold contact should have a contact force over several hundred μN to assure a reliable metallic contact resistance under about 100 mΩ. The restoring spring is designed to provide a 500 μN restoring force at an extra displacement of 0.2 μm to maintain small contact resistance during charging.

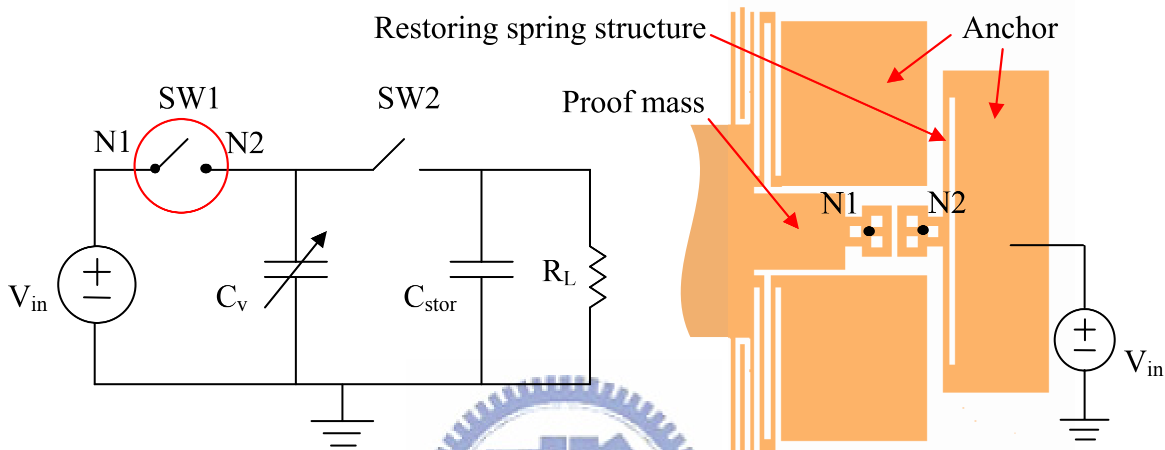

Fig. 2.20 SW1 as a contact mechanical switch

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2.4.2 SW2 design

SW2 should ideally be closed when the variable capacitor moves to the middle position. At this position, the terminal voltage of C_v has a maximum value V_{max}. This high voltage is used to induce electrostatic pull-in between nodes N3 and N4 to actuate the switch, as shown in Fig. 2.21. When SW2 is about to close, the voltage on node N3 approaches to $V_{max,}$ and node N4 remains at an adjustable voltage V_{adj}. This adjustable voltage is used to tune the pull-in timing of the switch to match the dynamics of the variable capacitor under fabrication uncertainties. When pull-in occurs, the movable node N3 is attracted by the electrostatic force to contact with node N5 before touching node N4. The layout of SW2 in Fig. 2.21 shows the suspended mass, springs, actuation electrodes, and output node N5.

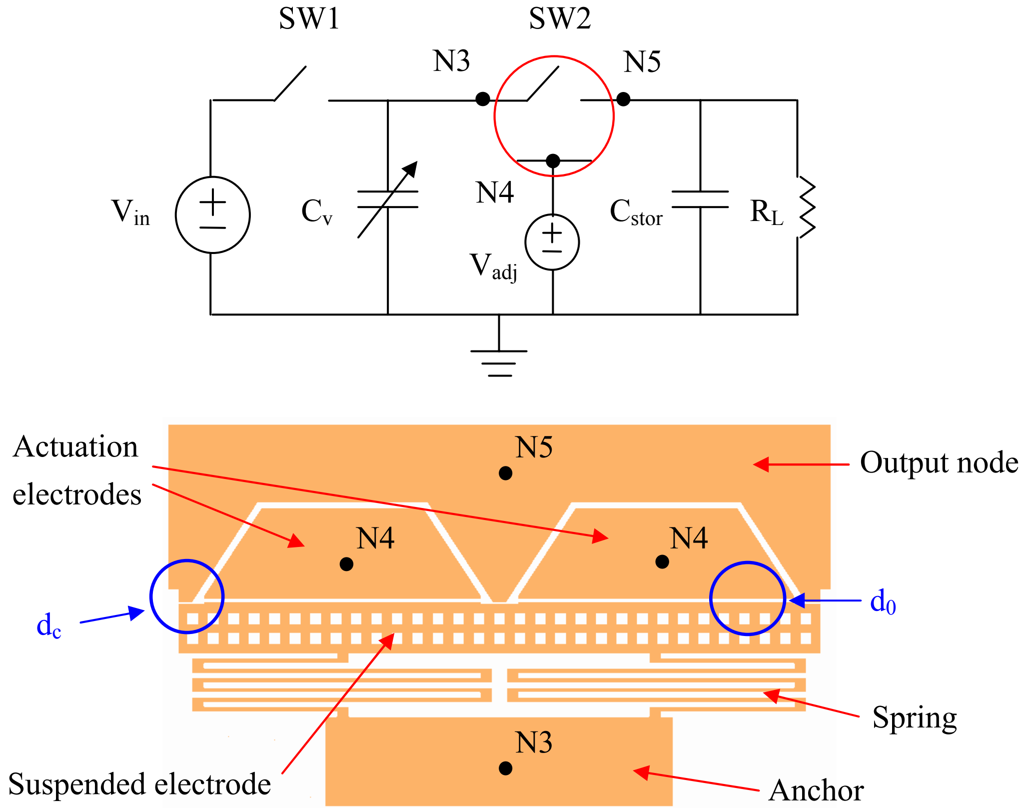


Fig. 2.21 SW2 as a lateral pull-in contact switch

The pull-in voltage of a spring suspended parallel plate capacitor can be determined by the following equation

$$V_{PI} = \frac{2}{3}\sqrt{\frac{2}{3}\frac{k_{SW2}d_0^{\ 3}}{\varepsilon h L_{SW2}}}, \tag{2.23}$$

where k_{SW2} is the spring constant, d_0 is the initial gap between nodes N3 and N4, and L_{SW2} is the total overlap length of nodes N3 and N4. The device thickness h is identical to the variable capacitor. The maximum voltage V_{max} of the variable capacitor on N3 is

$$V_{max} = \frac{C_{max} + C_p}{C_{min} + C_p} V_{in}, \tag{2.24}$$

where C_p is the parasitic capacitance due to anchors. With C_p = 60 pF, V_{max} drops from the ideal 90 V to approximately 50 V. SW2 must be timed precisely to V_{max}-V_{adj}

to ensure maximum conversion efficiency. Therefore the pull-in voltage should be lower than 90 V and tuned to match V_{max} by V_{adj} after C_p is determined by measurement.

Another parameter is the release voltage in the hysteresis of the pull-in effect. Conventional pull-in systems have different in pull-in and release voltages. When the charge on C_v is transferred to C_{stor} and the voltage between node N3 and N4 drops below the release voltage, SW2 will release and automatically open. In the current design, the output saturation voltage Vsat is about 40 V; therefore the release voltage V_R should be higher than V_{sat}-V_{adj}. The release voltage is determined by

$$V_R = \sqrt{\frac{2k_{SW2}d_c(d_0 - d_c)^2}{\varepsilon h L_{SW2}}}, \tag{2.25}$$

where d_c is the initial gap between nodes N3 and N5. Due to design constraints, the release voltage cannot be designed too high. The target of choice is about 50 V.

For a parasitic capacitance of 60 pF as the worst case, V_{max} and V_{sat} will drop to 50 V and 30 V, respectively, due to reduced capacitance variation in device operation. With V_{PI} targeted at 70 V and V_R targeted at 50 V, SW2 can still function with a V_{adj} = -20 V under worst condition and a V_{adj} = 20 V under ideal condition.

SW2 can be modeled as a second order system considering the spring force, the squeeze film damping between nodes N3 and N4, the electrostatic force due to voltage V_c, and the inertial force of the proof mass. A Simulink model is constructed to simulate the pull-in and release performance of SW2. Detailed information on the SW2 model is given in the appendix. Integrated Simulink model of the switch and the device is shown in Fig. 2.22. The "SW2" block determines the operation of SW2 by the voltage on the variable capacitor terminals. All device parameters were tuned until system response was identical to the case with ideal switches. The finely tuned parameters of SW2 are listed in Table 2.3, with the targeted voltages referred to the

static operation of the switch.

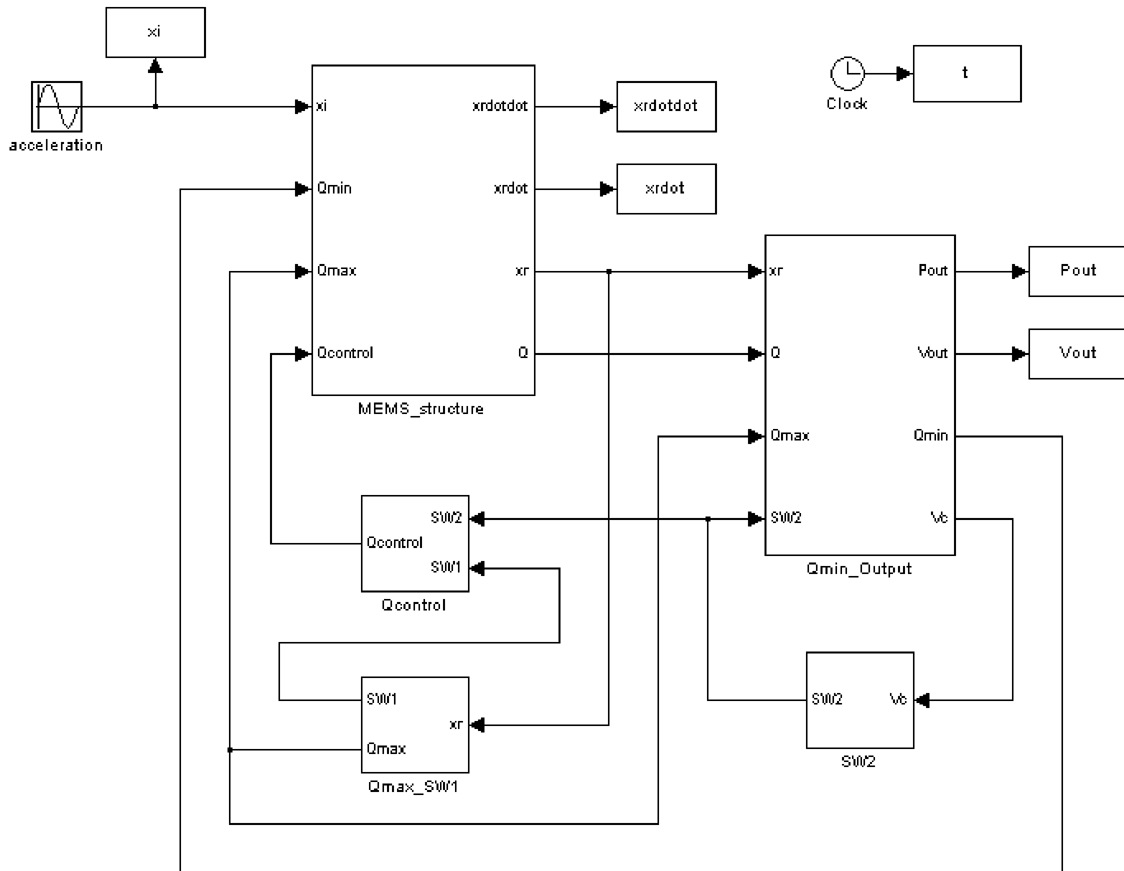


Fig. 2.22 Simulink model of the device with switch operation

Table 2.3 SW2 parameters

Variable	**Description**	**Value**
k_{SW2}	SW2 spring constant	11.24 μN/μm
d_0	Initial gap between N3 and N4	19 μm
d_c	Initial gap between N3 and N5	11 μm
h	Device thickness	200 μm
L_{SW2}	Overlap length between N3 and N4	2154 μm
V_{PI}	Pull-in voltage of SW2	74 V
V_R	Release voltage of SW2	50 V

Shown in Fig. 2.23 is the time response of V_c on the capacitor and SW2. The distance between N3 and N4 is also shown in the figure. It can be seen that SW2 contacts at nearly the maximum value of V_c, and releases immediately after charge is transferred and V_c decreases to 40 V. The ringing effect of SW2 due to mechanical damping is also shown in the figure. SW2 is designed with a resonant frequency of approximately 1.5 kHz, which is high enough to neglect the coupling of the input vibration to the switch response. Also worth noticing is the V_c variation in the conversion process. It increases from 3.6 V to 90 V, then drops instantly to 40 V due to charge transfer, and decreases to a lower value of 1.5 V due to remaining charge, and at last charged to 3.6 V again. This completely agrees with the expected operation cycles.

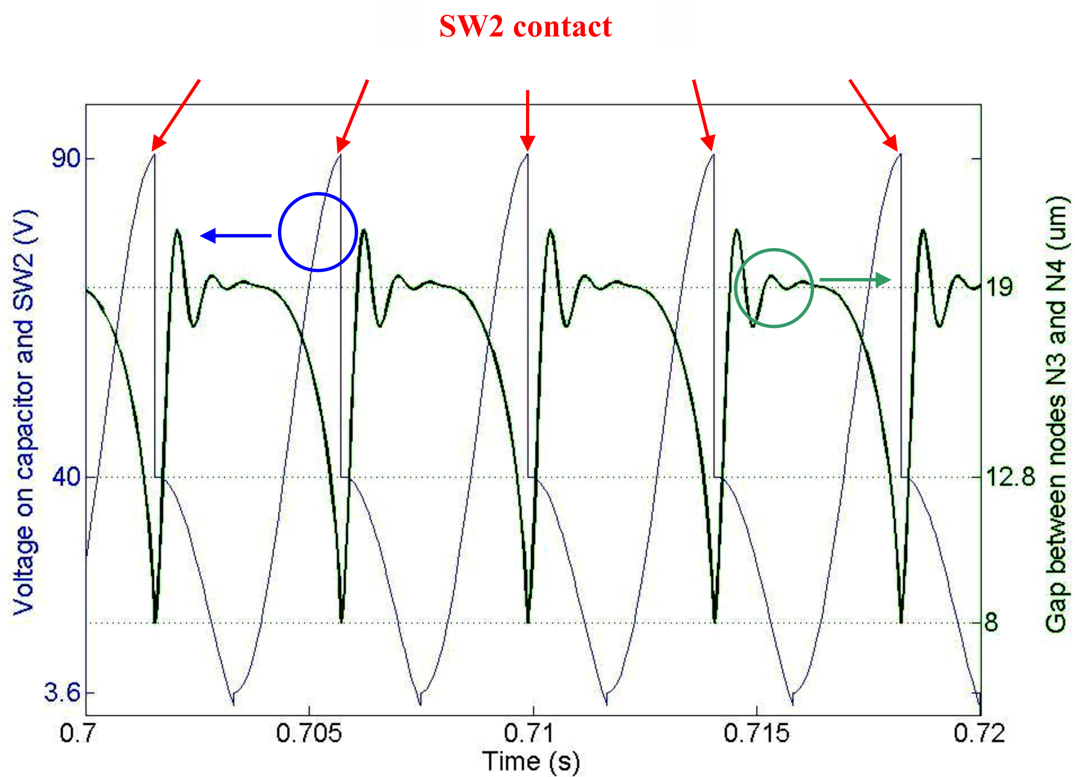
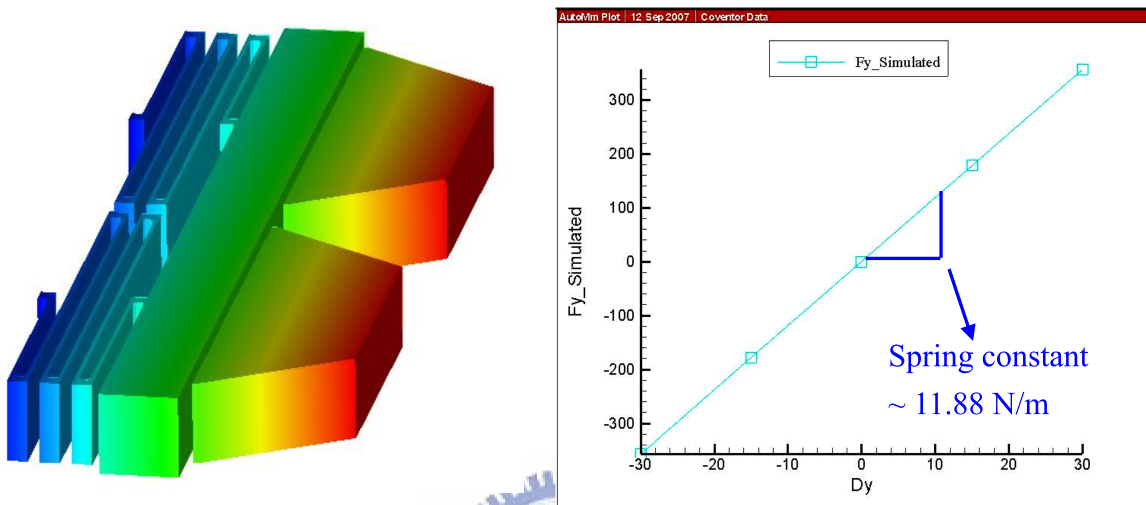


Fig. 2.23 Time response of SW2 gap and V_c

CoventorWare simulation of SW2 spring constant and pull-in voltage is shown in Fig. 2.24. The simulated spring constant is close to desired value. The pull-in voltage

simulation has a upper limit of 81.25 V and a lower limit of 80.93 V. Simulated pull-in voltage differs from the design value by about 7 V, probably due to simulation inaccuracy.



Spring constant	Pull-in voltage (upper)	Pull-in voltage (lower)
11.88 N/m	81.25 V	80.93 V

Fig. 2.24 CoventorWare simulation of SW2 spring constant and pull-in voltage

2.5 Layout schematic

This section discusses the floor-planning of the device layout. In the variable capacitor design, floor-planning must be done beforehand in order to determine maximum achievable number of finger cells without resulting in a fragile mechanical structure. As shown in Fig. 2.25, in order to maximize the number of finger cells, the proof mass is divided into several rows. The minimum width of the proof mass structure is larger than 800 μm to maintain a high rigidness. This highly concentrated layout design is required to achieve the output specifications under device dimension constraints. It greatly improves the area power density of the in-plane gap-closing

variable capacitor topology. The center hole in Fig. 2.25 serves as a self alignment mechanism for the external tungsten ball in the final assembly. 20 springs are connected to the proof mass and the anchored areas of the springs are minimized in order to reduce parasitic capacitance. The outer frame is also used to connect the fixed electrodes to ground, whereas the voltage on the movable electrode is connected to the anchors. The layout of the two mechanical switches is shown in Fig. 2.26. SW2 will be electrically connected to the anchor pad with wire bonding. Other contact pads will be wire bonded to a printed circuit board (PCB) for further measurement use.

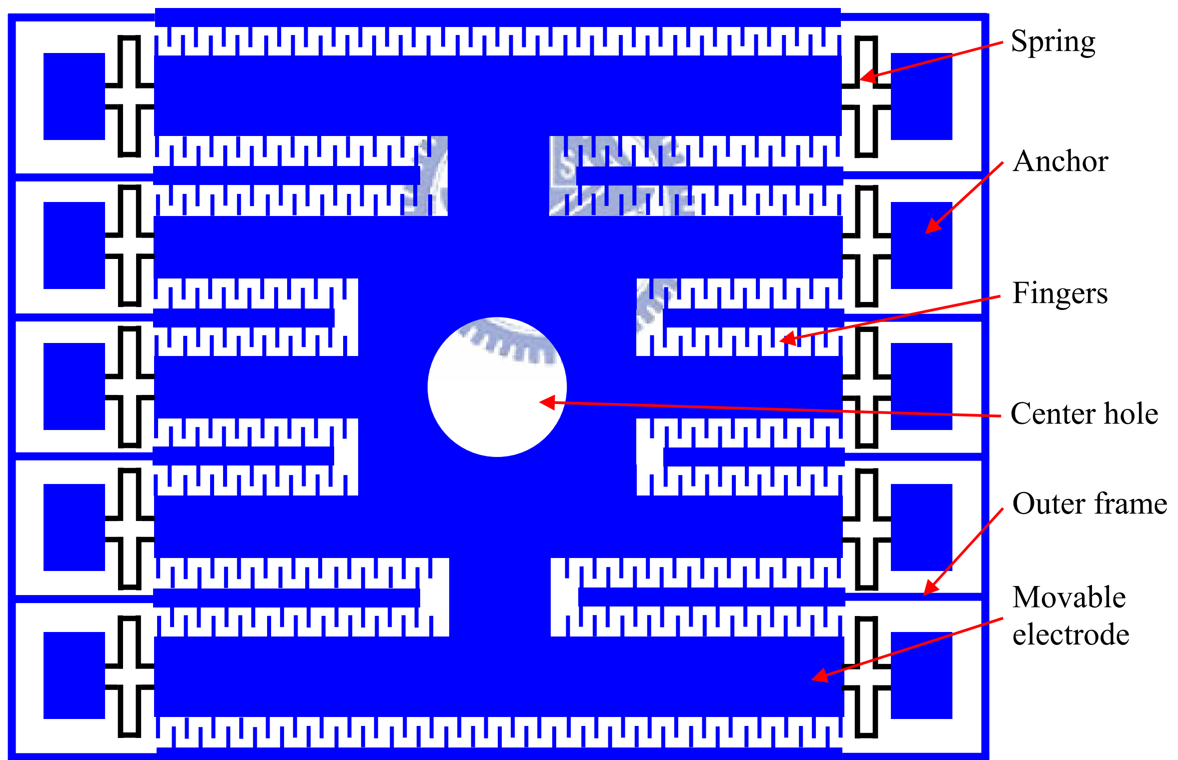


Fig. 2.25 Layout schematic view of the variable capacitor

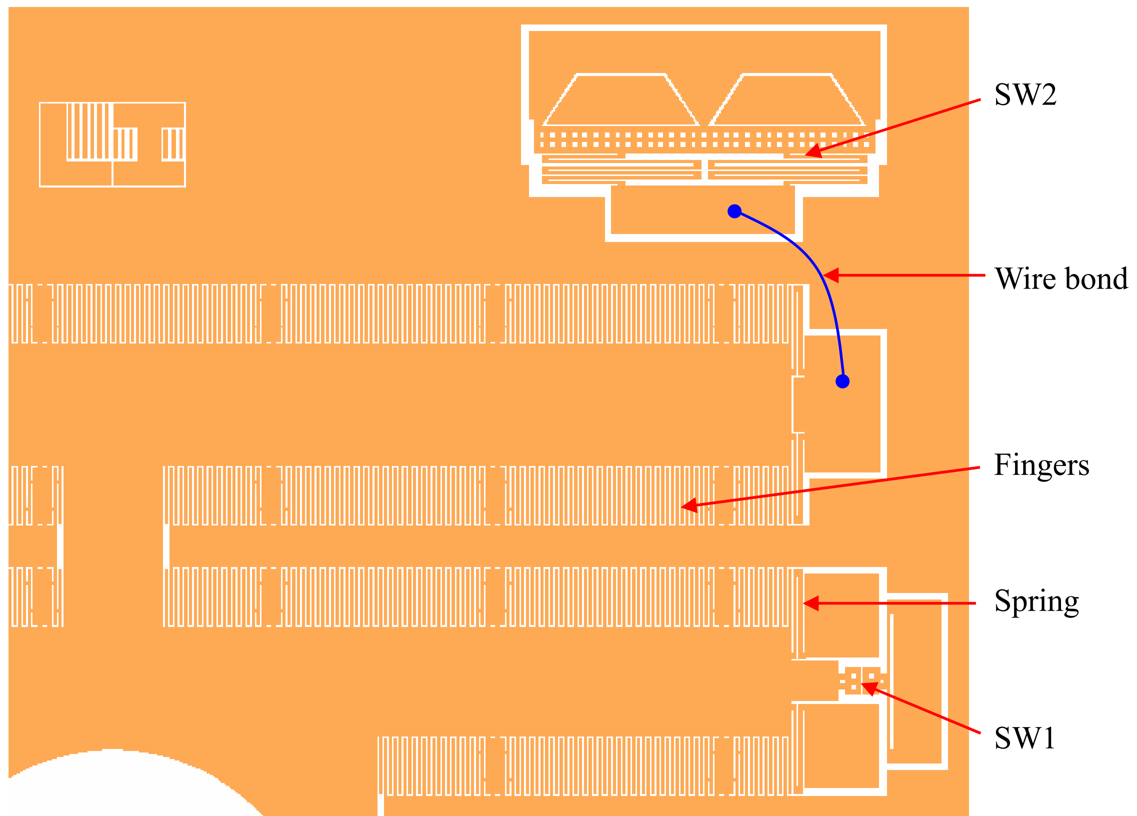


Fig. 2.26 Layout view of the variable capacitor and switches

2.6 Conclusion

The design and analysis of a capacitive vibration-to-electric energy converter with integrated mechanical switches is presented. With an area constraint of 1 cm^2 and an auxiliary battery voltage supply of 3.6 V, the device is designed to generate an output power of 31 μW and an output saturation voltage of 40 V for the input vibration with frequency of 120 Hz and peak acceleration of 2.25 m/s^2. A 4 gram tungsten metal ball is needed as an external mass. The charge-discharge conversion process is controlled by a novel lateral contact mechanical switching mechanism operating synchronously to the variable capacitor transducer unit. All parameters were decided through analytical design, dynamic simulation and FEM simulation. Fabrication and measurement of the device will be discussed in the following two chapters.

Chapter 3 Fabrication process

The detailed fabrication process of the SOI based device is presented in this chapter. Various unwanted fabrication issues were encountered, such as residual stress in the SOI buried oxide layer, non-ideal deep silicon etching process, device damage during dicing process, etching of silicon nitride in the HF release process, and difficulty to form metallized contact pads on the high aspect ratio structures. The fabrication process was modified and devices were successfully fabricated.

3.1 Fabrication process flow

SOI MEMS technology and Inductively Coupled Plasma (ICP) deep silicon etching is a convenient way for fabricating high aspect ratio MEMS structures. Other difficulties in MEMS fabrication such as electrical insulation and device flatness can also be overcome easily by the SOI technology.

In order to reduce resistive loss and maintain high operation speed, the p-type device layer is heavily doped with resistivity less than 0.02 Ω-cm to minimize contact and parasitic resistance. The orientation of the device layer is <100>. The device thickness should be as large as possible within the ICP fabrication capability to define the finger structures. Thus, an SOI wafer with a 200 μm device layer is chosen. The buried oxide layer is 2 μm thick for better electrical insulation. The handle layer is 400 μm thick for a firm structural support.

The fabrication process is illustrated in Fig. 3.1. Several steps are merged into one for clarity, whereas dicing and cleaning procedures are not shown.

Process parameters

Step A: Wafer cleaning

Standard RCA wafer cleaning procedure was performed to remove organic contaminants from the wafer surface, then remove the thin oxide layer that may have built up, and finally remove any ionic or heavy metal contaminants. Notice that the RCA clean should be performed prior to any crucial steps, especially those involving high temperatures. Detailed parameters are given as below. Every step begins and ends with a 5 minute de-ionized water (DI water) rinse.

Step	Process parameters	Function
1	$H_2SO_4 : H_2O_2$ = 3 : 1 (10 min 85 °C)	Organic removal
2	HF : H2O = 1 :100 (room temperature 30 seconds)	Chemical oxide removal
3	$NH_4OH : H_2O_2 : H_2O$ = 1 : 4 : 20 (10 min 85 °C)	Particle removal
4	HCL : $H_2O_2 : H_2O$ = 1 : 1 : 6 (10 min 85 °C)	Ionic removal
5	HF : H2O = 1 :100 (room temperature 30 seconds)	Chemical oxide removal

Step B: Back side silicon oxide deposition

Silicon oxide with a thickness of 4.5 μm was deposited by a BR-2000LL plasma enhanced chemical vapor deposition (PECVD) system on the handle layer of the SOI wafer, as shown in Fig. 3.1 (a). The silicon oxide will be used as the hard mask for the 400 μm back side ICP etching process since it makes the subsequent double side photolithography more convenient. Heat dissipation during the ICP etching is also improved. The thickness was chosen according to the minimum selectivity of 100:1 between silicon and oxide in the ICP process. Deposition was divided into several 1.5 μm steps to prevent cracking of the oxide layer. Detailed parameters are given as below.

Description	Process parameters	Remarks
SiH_4 flow rate	5 sccm	BR-2000LL
N_2O flow rate	90 sccm	BR-2000LL
Process pressure	400 mTorr	BR-2000LL
Process temperature	350 °C	BR-2000LL
RF power	10 W	BR-2000LL
Deposition rate	20 minutes resulting in 1.5 μm	Repeat 3 times

Step C: Back side photolithography on silicon oxide

The back side photolithography was performed by a EV620 aligner on the deposited silicon oxide, as shown in Fig. 3.1 (b). AZ4620 was spin coated and patterned as a 7 μm thick photoresist mask. Detailed parameters are given as below.

Step	Description	Process parameters	Remarks
1	Pre-bake	150 °C 30 minutes	YES – 5
2	HMDS coating		YES – 5
3	1st spin (spread cycle)	500 rpm 10 seconds	TSC-150M
4	2nd spin (spin cycle)	2000 rpm 40 seconds	TSC-150M
5	Static settlement	10 minutes	
6	Soft bake	90 °C 12 minutes	Hot plate
7	Exposure	20 seconds	EV620
8	Development	75 seconds	EDP1000
9	Rinse	90 seconds	DI water
10	Hard bake	120 °C at least 1 hour	Hot plate

Step D: Back side hard mask definition by wet etching

As shown in Fig. 3.1 (b), the 4.5 μm silicon oxide below the photoresist mask is etched by a NH_4F:HF = 6:1 buffered oxide etchant (BOE) with an etch rate of roughly 1 μm per minute. The reason for using BOE isotropic etching instead of reactive ion etching (RIE) is the relatively low selectivity between silicon oxide and photoresist in the RIE process, which means an excessively thick photoresist mask is needed to etch

the thick oxide layer. The undercutting effect of wet etching is rather irrelevant to the back side pattern for partial substrate removal. The photoresist mask must be hard baked for at least 1 hour before immersing into the BOE solvent, or else peeling off of the photoresist mask may happen.

Step E: Front side photolithography

As shown in Fig. 3.1 (c), the front side photolithography is done by an EV620 double side aligner to define the photoresist mask for the subsequent ICP etching of the device layer. This is the main process to define the device structure. Parameters have been carefully tuned to produce all patterns correctly, especially the finger bump structures. The minimum selectivity of ICP etching between silicon and AZ4620 photoresist is 40:1. Thus, the photoresist thickness is chosen as 5 μm. It should not be too thick; otherwise it becomes difficult to produce small line width structures. Hard baking should be as long as possible in order for the photoresist to withstand the ICP process. Detailed parameters are given as below.

Step	Description	Process parameters	Remarks
1	Pre-bake	150 °C 30 minutes	YES – 5
2	HMDS coating		YES – 5
3	1st spin (spread cycle)	500 rpm 10 seconds	TSC-150M
4	2nd spin (spin cycle)	4000 rpm 40 seconds	TSC-150M
5	Static settlement	10 minutes	
6	Soft bake	90 °C 7 minutes	Hot plate
7	Exposure	11 seconds	EV620
8	Development	55 seconds	EDP1000
9	Rinse	90 seconds	DI water
10	Hard bake	120 °C at least 1 hour	Hot plate

Step F: Front side deep silicon etching

The deep silicon etching of the device layer is performed by using a STS MESC multiplex ICP reactor with the standard Bosch process, as shown in Fig. 3.1 (d). Additional guarding structures are used to reduce the influence of non-ideal etching effects, as discussed later. The averaged etch rate is roughly 2.2 μm per minute. Front side ICP etching is done on the wafer level. It provides a better etching profile and a more uniform etch rate due to the better heat dissipation. Detailed parameters are given as below.

Description	Etch phase parameters	Passivation phase parameters
Time per cycle	11.5 seconds	7.0 seconds
SF_6 flow rate	130 sccm	0 sccm
C_4F_8 flow rate	0 sccm	85 sccm
O_2 flow rate	13 sccm	0 sccm
Coil RF power	600 W	600 W
Platen RF power	11.5 W	0 W
Process pressure	APC position = 81.2 % Base pressure = 0.3 mTorr	
Helium back side cooling	Helium back side pressure = 10 Torr Maximum helium leak up rate = 20 mTorr/min	
Etch rate	0.6-0.7 μm per cycle depending on pattern	

Step G: Silicon nitride deposition

As shown in Fig. 3.1 (e), low stress silicon-rich nitride is deposited as the dielectric layer by low pressure chemical vapor deposition (LPCVD) due to its better step coverage, higher dielectric constant and higher density of the deposited film. The remaining photoresist mask from the ICP process must be removed completely, and the wafer must go through RCA cleaning once more before the LPCVD process. In order to have a 500 Å thick silicon nitride on the device sidewalls, deposition time was expanded to 8 minutes. Detailed parameters are given as below.

Description	Process parameters	Remarks
SiH_2Cl_2 flow rate	85 sccm	NFC LPCVD
NH_3 flow rate	17 sccm	NFC LPCVD
Process pressure	180 mTorr	NFC LPCVD
Process temperature	850 °C	NFC LPCVD
Deposition rate	75 Å/minute (12 wafer cassette)	8 minute process

Step H: Wafer dicing

Since the back side substrate will be removed by ICP deep etching to reduce parasitic capacitance, large areas of silicon will be removed and buried oxide layer will be exposed. This causes two problems. One is that the entire wafer becomes very fragile and may disintegrate in the reactor chamber. The other is that the residual stress in the oxide can damage the structures in the front side device layer. Therefore, the wafer is diced first by a Disco 2H/6T system. The front side silicon structures are protected during the dicing process by a AZ4620 photoresist coating. The subsequent back side etching will be conducted with the individual chips bonded to a carrier wafer by heat dissipation paste. This process greatly improves the fabrication yield.

Step I: Top side silicon nitride removal

Before the back side ICP process, the top side silicon nitride layer should be removed by RIE (SAMCO RIE-10N) in order to provide electrical contact to the silicon device, as shown in Fig. 3.1 (g). An etching time of 30 seconds is enough to completely remove the 500 Å silicon nitride layer. Over etching will reduce sidewall nitride thickness and device thickness. Detailed parameters are given as below.

Description	Process parameters	Remarks
SF_6 flow rate	30 sccm	RIE-10N
CHF_3 flow rate	10 sccm	RIE-10N
Helium back side cooling	Helium flow rate about 15 sccm	RIE-10N
Process pressure	50 mTorr	RIE-10N
RF power	100 W	RIE-10N
Etch rate	1000 Å per minute	Silicon nitride

Step J: Back side deep silicon etching

After the diced chips were bonded on a carrier wafer, the back side ICP etching was performed, as shown in Fig. 3.1 (g). A thick layer of oxide was deposited on the carrier wafer to prevent it from being etched and becoming from fragile during the ICP etching. Performing ICP processes on bonded chips will degrade the helium cooling capability and spoil the selectivity and vertical profiles of the ICP process. Fortunately, the back side structure is rather insensitive to or even benefiting from the non vertical etching profiles. The silicon oxide hard mask also alleviates the problem with decreased selectivity. Additional blocking structures are used to protect the device from the residual stress in the buried oxide layer. Severe etch rate lagging effect happens between wide and thin open areas, resulting in a rather long etching time needed to complete the entire etching process. Process parameters are identical to those for the front side ICP process.

Step K: Device release

As shown in Fig. 3.1 (h), the device is released by exposing device chips to HF vapor at 30-40°C to remove the unwanted buried oxide beneath the movable structures. HF vapor release helps prevent the stiction which may happen in SW2. Selectivity of silicon oxide to silicon nitride in HF vapor is assumed to be very high. The release time is 1 hour and the oxide layer is over etched in order to prevent

shortage during metal deposition. Released device is cleaned by rinsing in de-ionized water and isopropanol (IPA) solution.

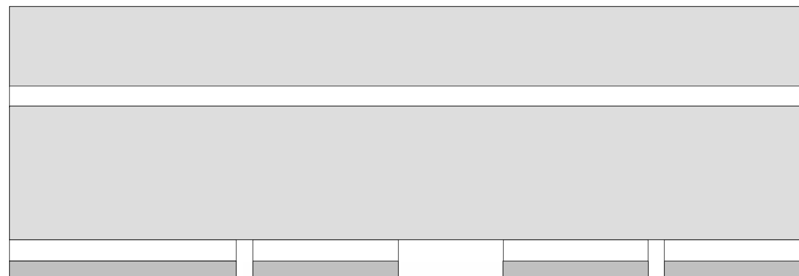
Step L: Metallization

A metal layer is deposited on contact pads and the lateral contacts in the mechanical switches, as shown in Fig. 3.1 (i). Ideally, gold should be used due to its slower oxidization in contact operation. In our prototype devices, aluminum is used instead to verify the fabrication feasibility. Sputtering is used due to the better step coverage. With a shadow mask, aluminum is only applied to the contact pad and switch gap areas while the fingers are protected from the deposition.

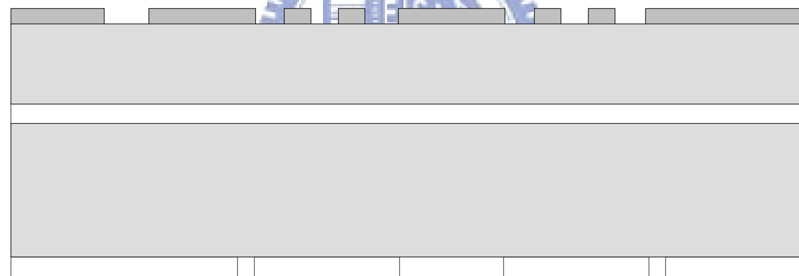
Step M: Wire bonding and external metal mass attachment

As shown in Fig. 3.1 (j), the last two steps are to wire bond the contact pads to a PCB for further vibration test and then attach the external tungsten ball to the center hole with glue or epoxy. The tungsten ball has a mass of 4 grams and a size of approximately 4 mm in diameter. This assembly step must be done with care; otherwise the device will be destroyed.

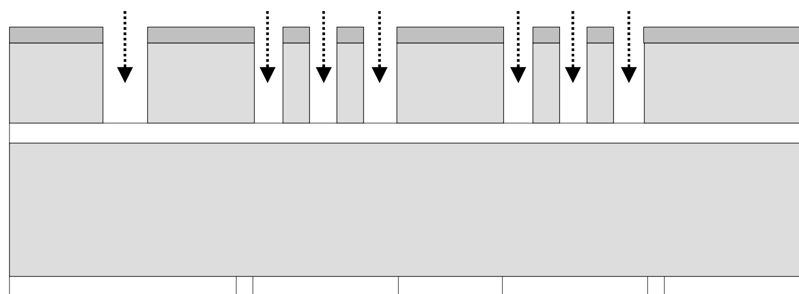
(a) Back side silicon oxide deposition by PECVD



(b) Silicon oxide hard mask patterning and etching by BOE



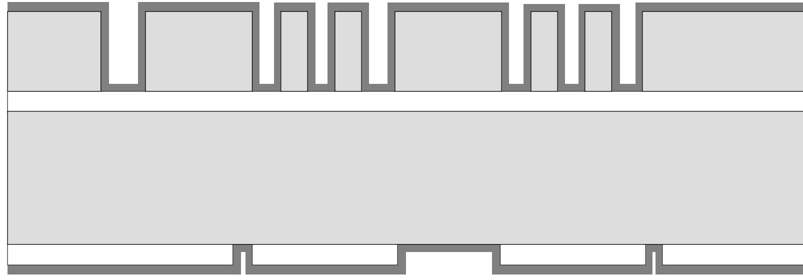
(c) Front side mask patterning by double side photolithography



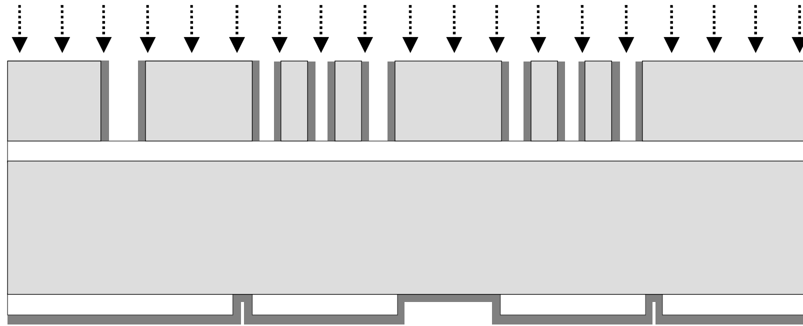
(d) Front side ICP deep silicon etching

Silicon Oxide Photo resist Nitride Aluminum

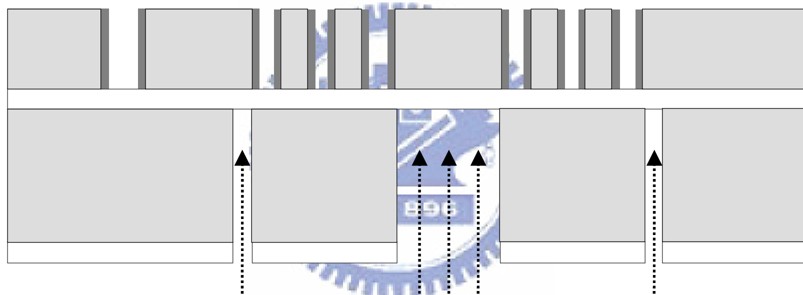
Fig. 3.1 Fabrication process flow of the SOI device



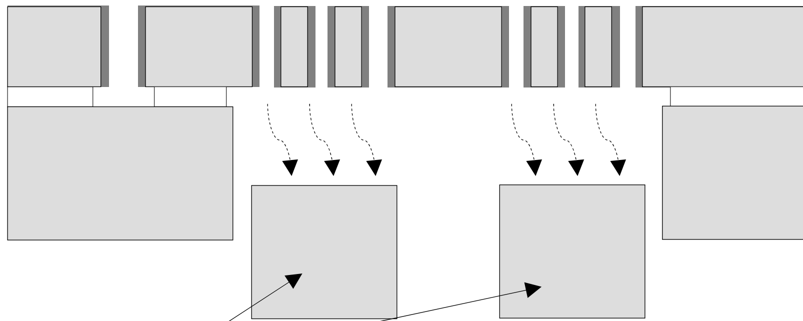
(e) Silicon nitride deposition by LPCVD



(f) Top side silicon nitride removal by RIE



(g) Bottom side ICP deep silicon etching



Blocking structures

(h) Device release in HF vapor
(guarding and blocking structures removed by rinsing)

Fig. 3.1 Fabrication process flow of the SOI device (continued)

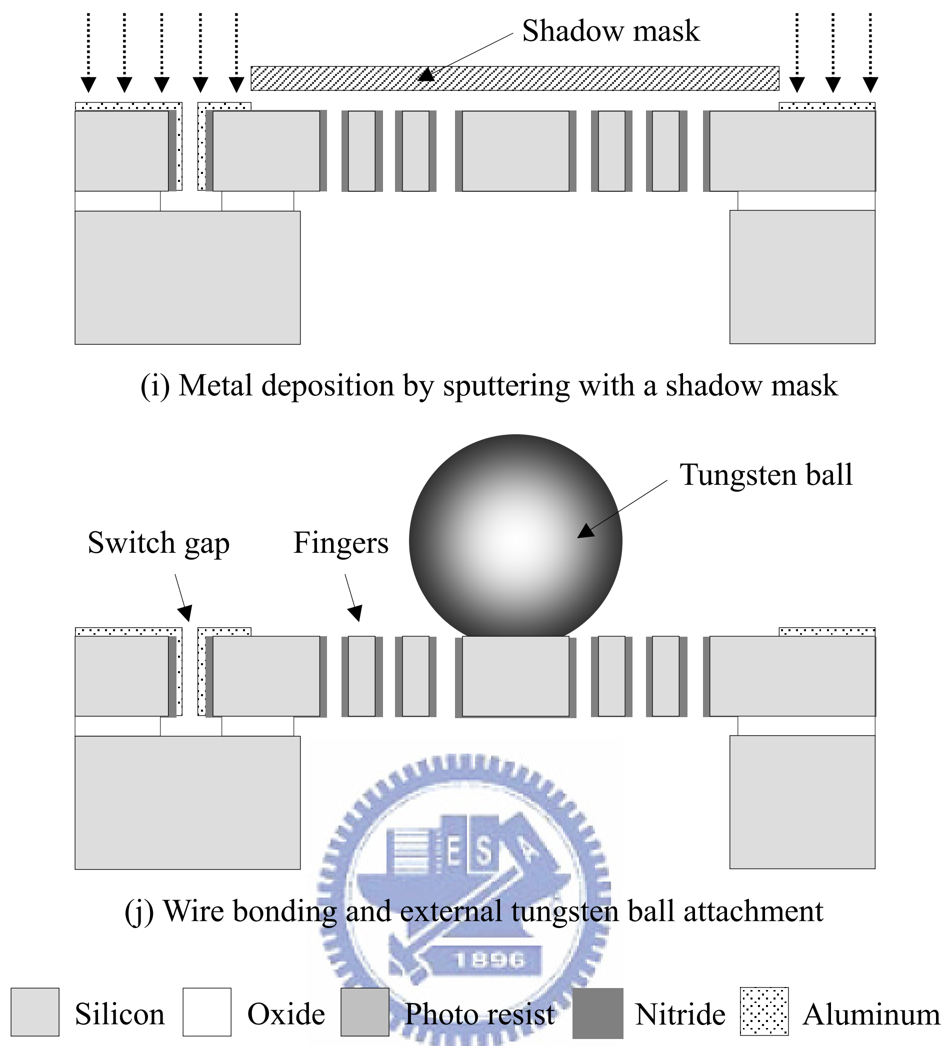


Fig. 3.1 Fabrication process flow of the SOI device (continued)

This is the original fabrication process. It depends heavily on ICP etching. Other important issues are: the silicon nitride sidewall must survive the whole fabrication process to provide proper electrical insulation; the metallization must be done with care to avoid shortage between electrodes.

Fabrication process was conducted in the Nano Facility Center at National Chiao Tung University, the Nano Science and Technology Center at National Tsing Hua University, the Nano-Electro-Mechanical-System Research Center at National Taiwan University and the National Applied Instrument Technology Research Center.

3.2 Processing issues

Several issues were encountered in the fabrication process. Those related to the ICP etching were taken into consideration in the original process mentioned above, while others emerged with the progressing of the fabrication. To solve all the issues, a modified process was proposed and explained in the next section.

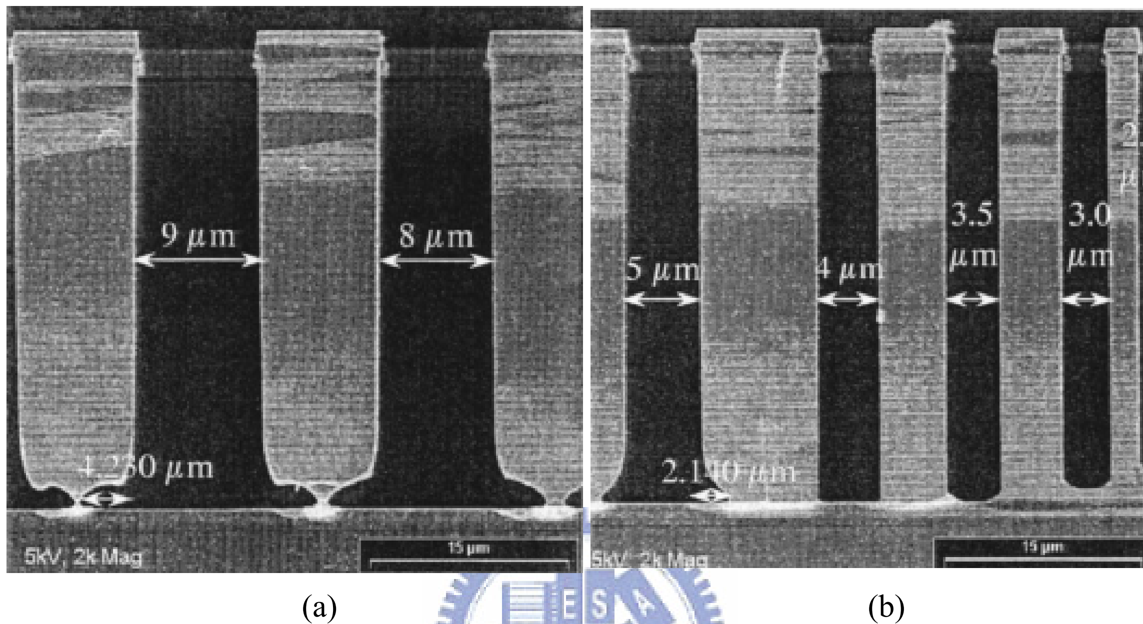
3.2.1 Non ideal effects of the ICP process

The notorious notching effect (aka footing effect) in conventional deep ICP etching of SOI wafers occurs at the silicon/oxide interface and results in a long narrow concave groove due to over etching. Analysis of the phenomenon [38] shows that it originates from the positive charge accumulation in the buried oxide layer which causes further deflection of reactant ion and forward scattering. Thus, etching time must be controlled accurately to prevent over etching; otherwise the structure height will be reduced from the bottom, and the device performance will be degraded.

The etch rate reduction is another annoying problem. There are three main reasons for the severe etch rate reduction in high aspect ratio deep silicon ICP etching process [39-42]. They are addressed as the RIE lag effect, the aspect ratio dependent etch rate (ARDE), and the microloading effect. The RIE lag effect describes the smaller etch rate in smaller opening features; ARDE explains the fact that the etch rate continues to decrease (or even stop) for increasing etch depth; the microloading effect indicates that the etch rate is severely reduced when the percentage of the open area is too large. These effects interact with one another and limit the device fabrication.

Consider the composite notching and etch rate lagging effect caused by the RIE lag and the ARDE effect. In order to complete the whole etching process, the narrowest trenches will take the longest time, while the larger gaps will experience

severe notching effects. Figure 3.2 shows the lagging effect in smaller features and the notching effect in the wider trenches that arrive at the insulator etch stop layer first [43].



(a) (b)

Fig. 3.2 (a) Notching and (b) etch rate lagging effect [43]

In our device, the unwanted composite effect can happen in the regions with narrow gaps (such as fingers and SW2) and wide openings (such as springs). In order to alleviate this defect, the device layout is modified and additional guarding structures are added. These guarding structures are designed so that all openings have nearly the same trench width. Therefore, it results in a more uniformed etch rate through out the whole wafer. The modified layout of SW1 and SW2 is shown in Fig. 3.3. This concept is applied to the entire device design, where all primary gaps and release holes are adjusted to have similar etch rates [41]. The guarding structures will be removed in the rinsing procedure after releasing.

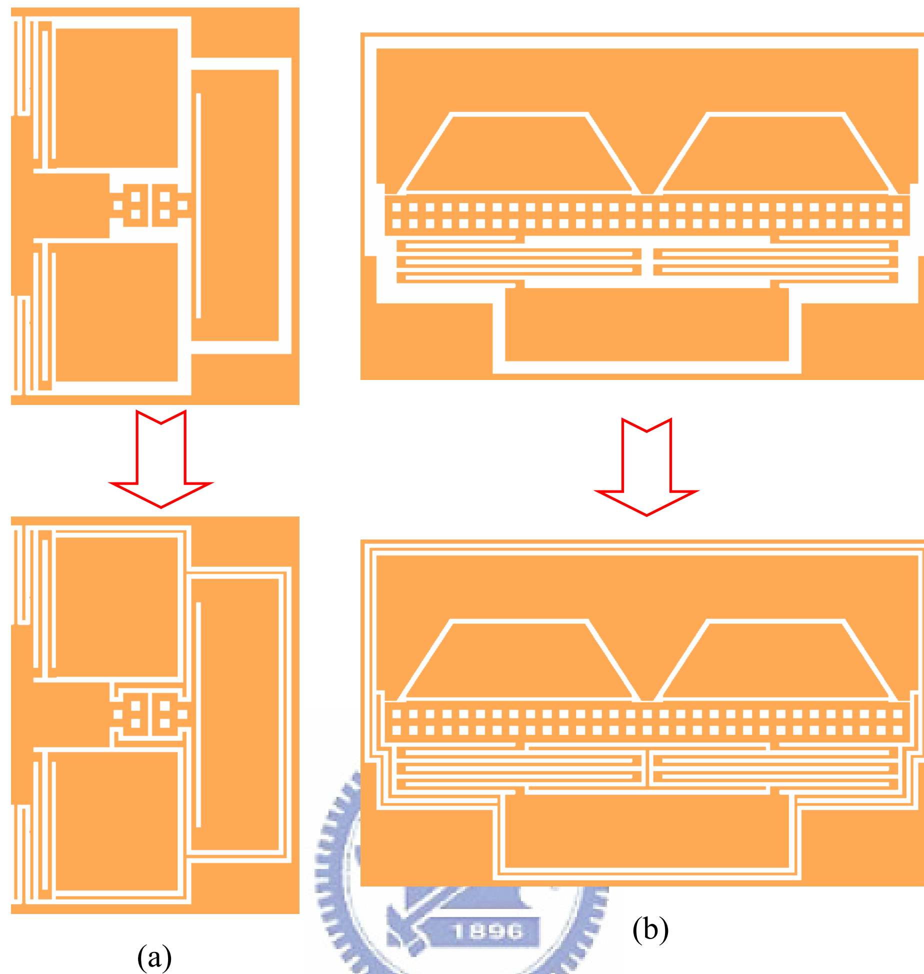
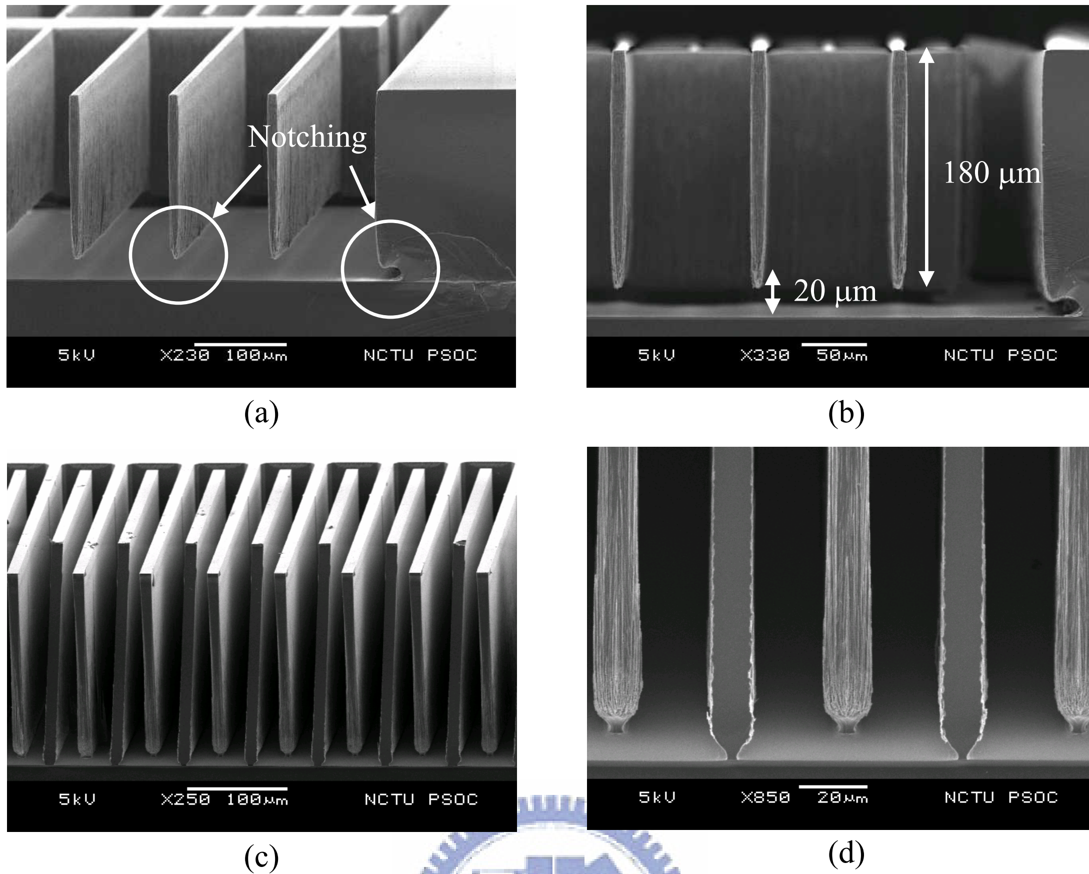


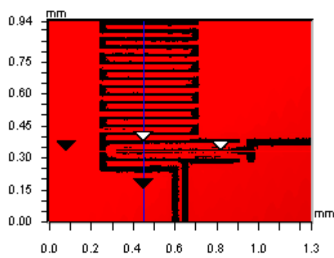
Fig. 3.3 Modified layout with guarding structures, (a) SW1, (b) SW2

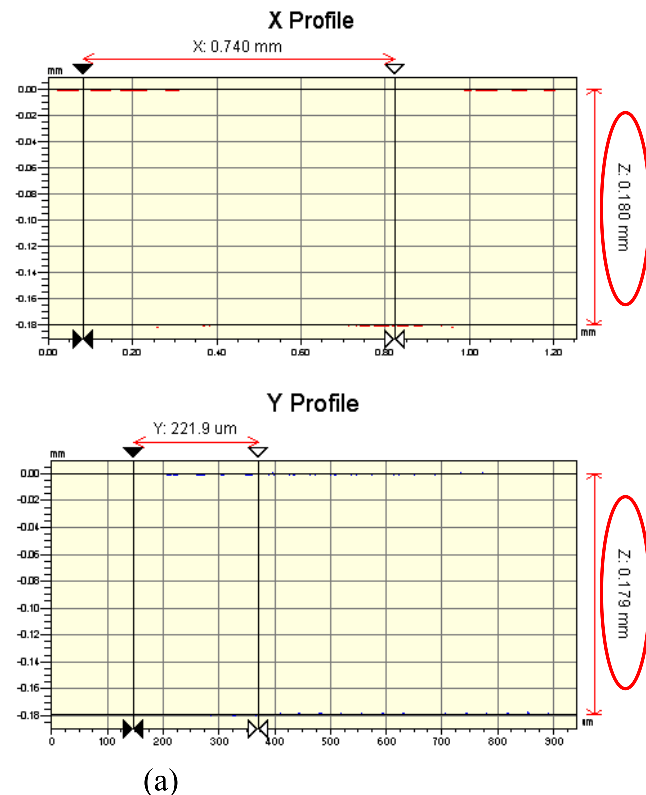
The fabricated devices are shown in Fig. 3.4. The device without guarding structures suffered from severe notching effect. 20 μm of the device height at the bottom was consumed due to over etching. The device with guarding structures has a rather uniform etch rate. It takes approximately 88 minutes and 30 seconds to complete the etching process. The notching effect is less obvious and less device thickness is consumed. The WYKO interferometer measurement of the etched depth at several locations of the modified design after 80 minute etching is shown in Fig. 3.5. The etched depth is 180 ± 2 μm at all locations. Thus, the guarding structures can be used to obtain a more uniform etch rate.



(a) (b) (c) (d)

Fig. 3.4 Experimental results of the notching effect, (a) (b) devices without guarding structures, (c) (d) devices with guarding structures



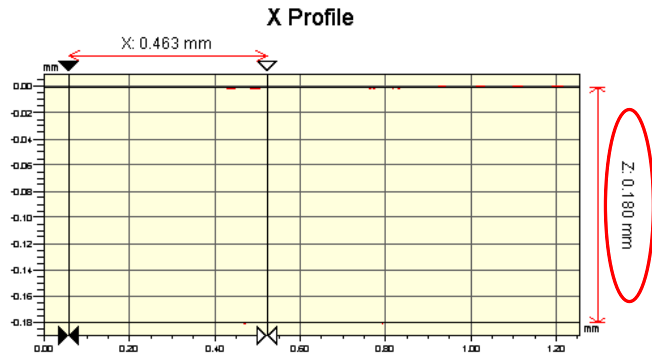


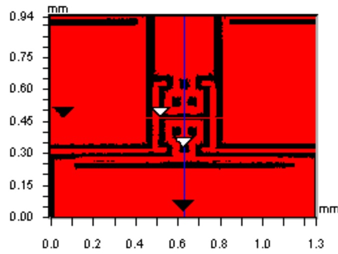
X	0.45	-	-	mm
Y	0.33	-	-	mm
Ht	-171.48	-	-	um
Dist			-	mm
Angle			-	°

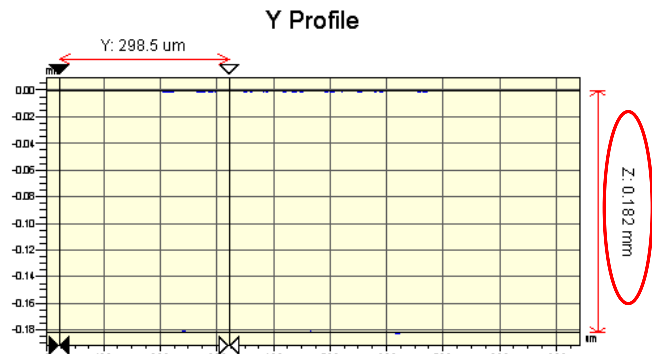
Title:

(a)

Fig. 3.5 ICP depth measurement after 80 minute etching, (a) fingers and spring trench



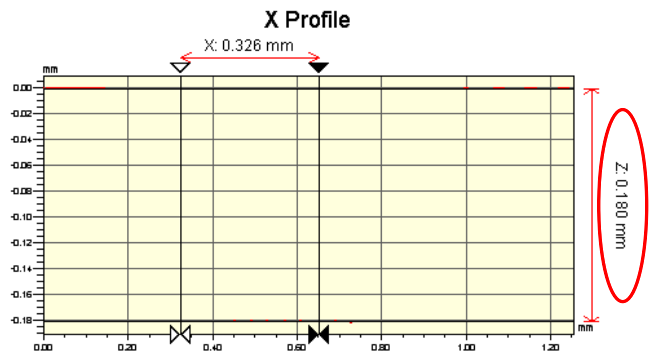


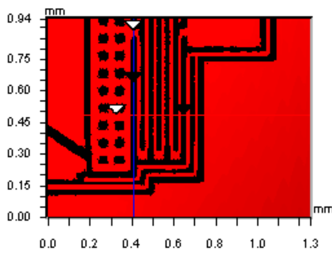


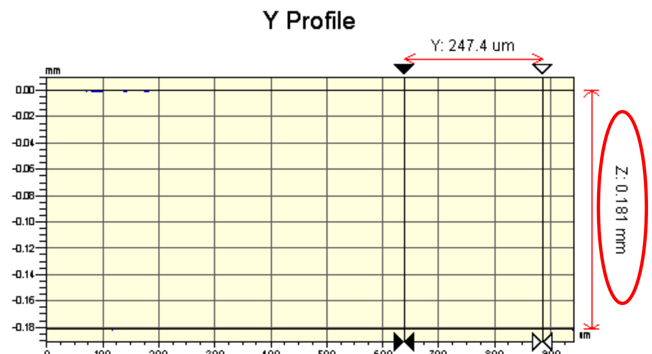
X	0.63	-	-	mm
Y	0.46	-	-	mm
Ht	-	-	-	um
Dist			-	mm
Angle			-	°

Title:

(b)







X	0.41	-	-	mm
Y	0.48	-	-	mm
Ht	-	-	-	um
Dist			-	mm
Angle			-	°

Title:

(c)

Fig. 3.5 ICP depth measurement after 80 minute etching, (b) SW1 trench, (c) SW2 trench (continued)

Another problem in ICP etching is the residual stress in the buried oxide layer. This stress shows destructive buckling effect when the back side etching exposes large areas of silicon oxide without sufficient bulk silicon support. The blocking structure proposed in [44] is used to prevent this stress effect. As seen in Fig. 3.6, additional blocking structures are added to both front and back sides to ensure that no large area of oxide is exposed without bulk silicon support after the etching process. The fingers and center hole are covered from the back side; the center hole is also protected on the front side. The blocking structures also help protect the fingers during the back side etching and prevent large microloading effect. Blocking

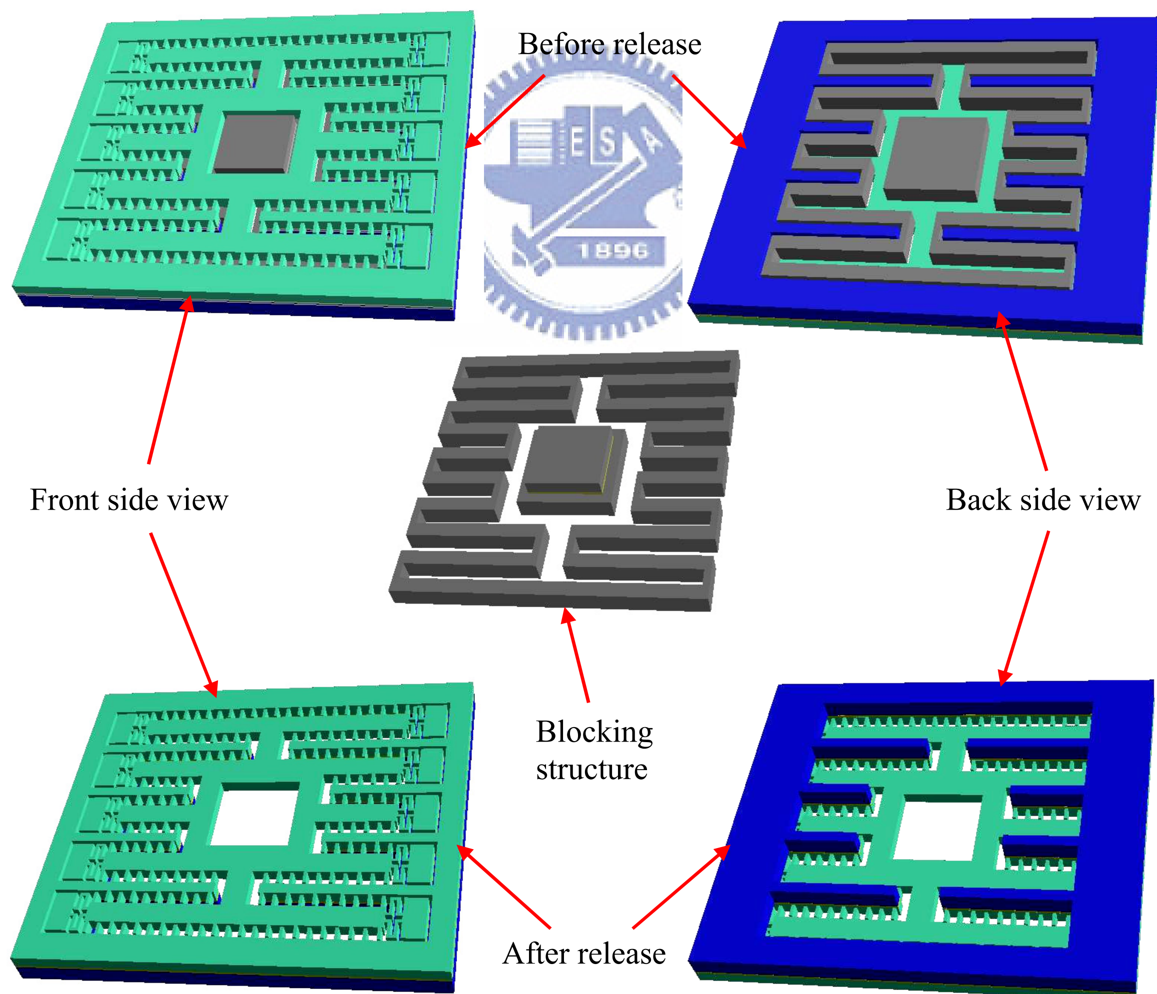


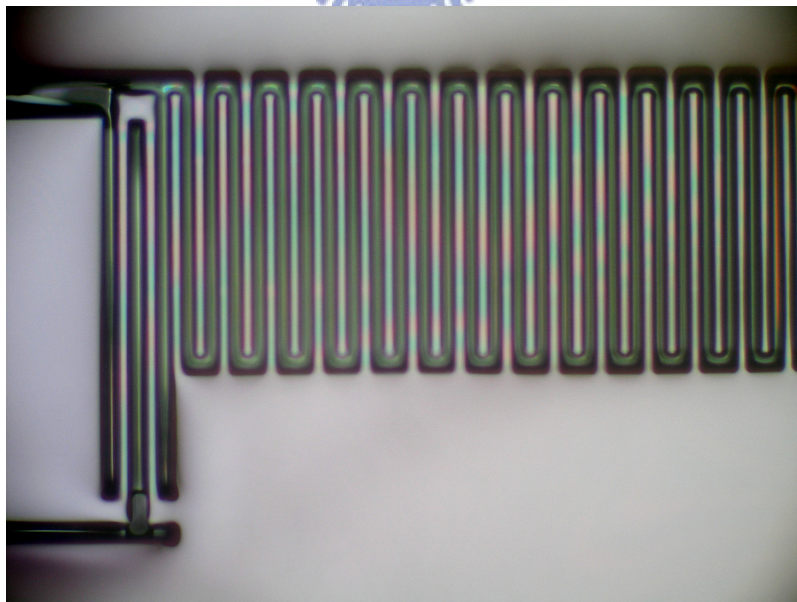
Fig. 3.6 Schematic view of device with blocking structure

structures are also removed by the rinsing procedure after the releasing.

Other issues of the ICP process, such as sidewall barreling and initial mask undercutting (about 1-1.5 μm) can be eased by using a more moderate ICP etching recipe and layout pre-enlargement.

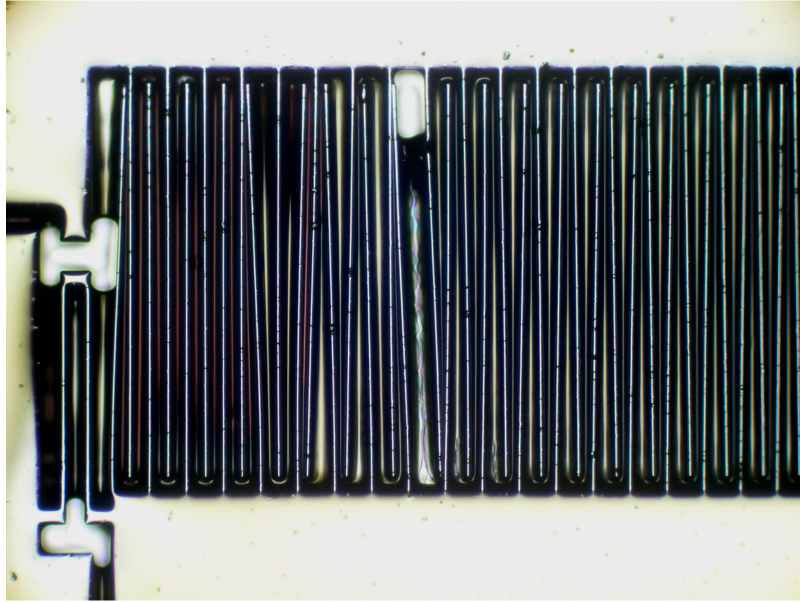
3.2.2 Damaging in dicing process

MEMS devices can be damaged during the dicing process by the cooling water and dust impact. The typical approach to solving this problem is to apply a thick photoresist to fill the gaps of the MEMS structure and provide a nearly planar protection layer on top of the device. In our work, AZ4620 photo resist is applied and waited until it completely permeates the trenches. The wafer is then spun at a spread cycle speed of 500 rpm, and a spin cycle speed of 1800 rpm, and at last soft baked for 30 minutes. Notice that the device will still be damaged even if it faces down during the dicing process. This is due to the suction force of the wafer chuck. Figure 3.7



(a)

Fig. 3.7 Device with photoresist protection coating, (a) current design with finger length of 425 μm, (b) previous design with finger length 1225 μm



(b)

Fig. 3.7 Device with photoresist protection coating, (a) current design with finger length of 425 μm, (b) previous design with finger length 1225 μm (continued)

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shows the photoresist protection applied to the current (finger length 425 μm) and the previous (finger length 1225 μm) devices. It is clear that the shorter fingers are more rigid to survive the photoresist coating process.

3.2.3 Etching of silicon nitride during release

As mentioned earlier, the LPCVD silicon nitride is supposed to survive the release process with an ideal etch rate of 1-10 Å per minute in the HF vapor. However, experimental results show that the selectivity between oxide and nitride is overestimated. The etch rate of nitride in HF vapor or 49 % HF solution is at least 100 Å per minute, which results in the total removal of silicon nitride after the release process. Measurements show shortage between fingers when they are in contact at the C_{max} position, as will be presented in Chapter 4. Two solutions for this problem are proposed. One solution is to increase the silicon nitride thickness until it can

withstand the release process. This approach was not chosen due to the lack of precise knowledge on the etch rate of silicon nitride in HF. In the second solution, the silicon nitride was deposited after the release process. It was then patterned by RIE with another shadow mask. PECVD instead of LPCVD was used due to facility compatibility with chip level process. A 2500 Å thick silicon nitride was deposited on the top and bottom sides of the released chips. The sidewall nitride thickness was expected as 500 Å due to poor PECVD step coverage. Silicon nitride deposition parameters by PECVD are given below. Results will be presented in following sections.

Description	Process parameters	Remarks
SiH_4 flow rate	20 sccm	BR-2000LL
NH_3 flow rate	80 sccm	BR-2000LL
Process pressure	400 mTorr	BR-2000LL
Process temperature	350 °C	BR-2000LL
RF power	10 W	BR-2000LL
Deposition rate	15 minutes resulting in 2500 Å	Silicon nitride

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3.2.4 Metal deposition issues

Aluminum is deposited after the release process to prevent the metal layer from the HF attack. Since the buried oxide under the anchors and the pads is over etched during release, the electrodes are not electrically connected presumably. Fingers are protected from the metal deposition by a shadow mask. Unfortunately, the device still showed electrical shorting after metallization. This is probably due to the conformal aluminum deposition at the bottom of the anchor, as shown in Fig. 3.8. A more accurately aligned shadow mask must be employed to limit the metal deposition only on the contact pads. Another solution is to deposit gold and pattern it by lift off before the device structure is defined. Gold is more resistant to HF solutions [45]. Due to the

lack of the accurately aligned shadow mask in current fabrication, a remedy aluminum thermal coating process was adopted. Since thermal coating has a worse step coverage, the possibility of shortage between electrodes is reduced.

Another issue that needs to be verified is the metallization of the lateral contact surfaces of the switches. One solution is to use oblique metal deposition to apply the metal on the lateral contact surfaces.

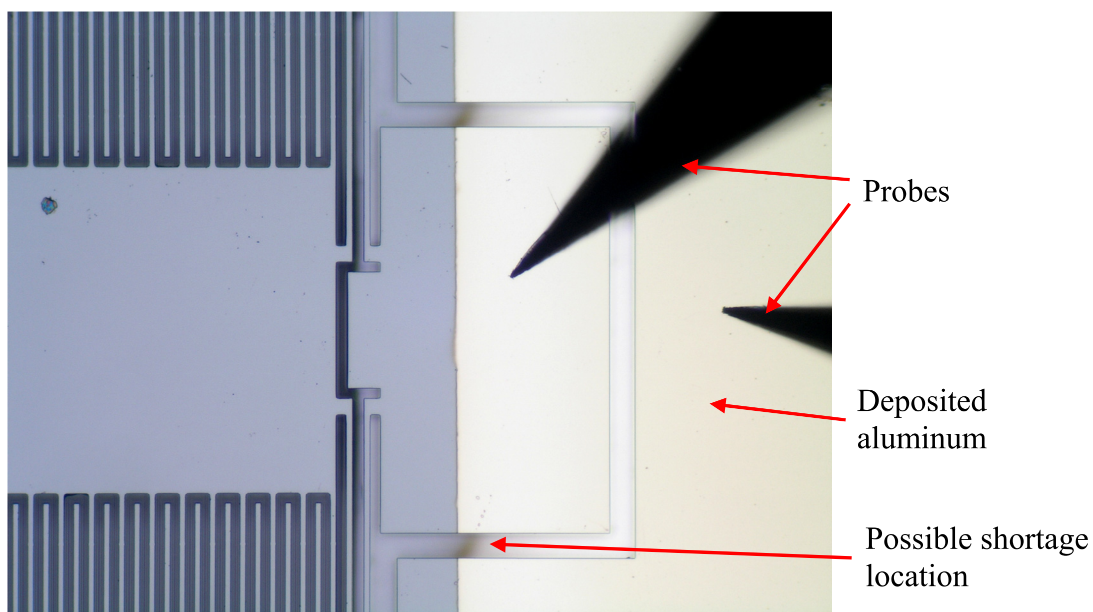
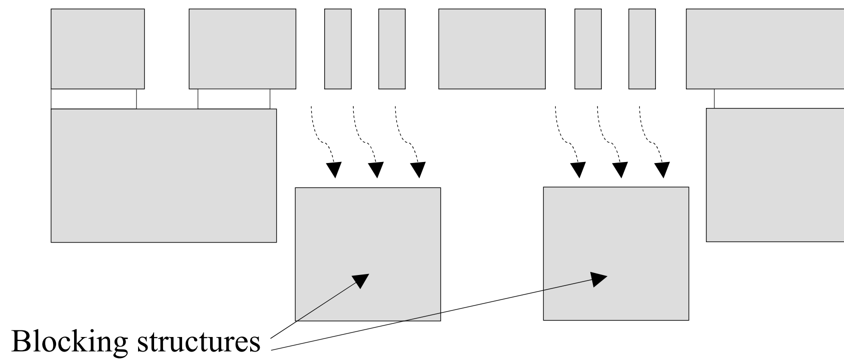


Fig. 3.8 Device after aluminum deposition

3.3 Modified fabrication process

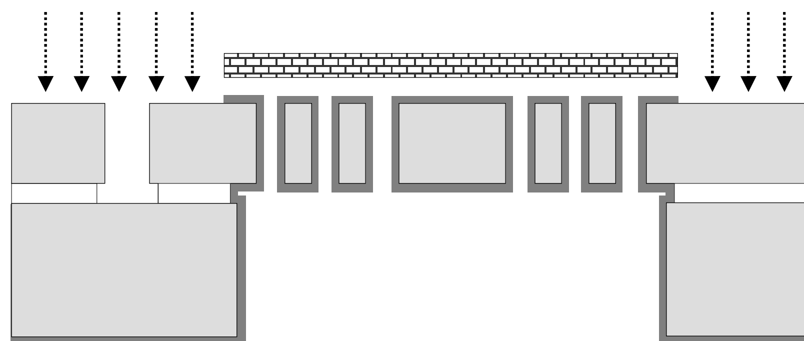
Based on the previous discussion of the silicon nitride survivability in HF release and the electrical shortage due to metal deposition, a modified fabrication process is proposed to solve the issues in the original process. In the modified process, silicon nitride is deposited and patterned after the release process. A more accurately aligned shadow mask in the metal sputtering process is also used. Figure 3.9 shows the modified steps beginning from the release process. Processes before the release step

are the same as the original except for the omitted silicon nitride deposition.



(a) Device release in HF vapor

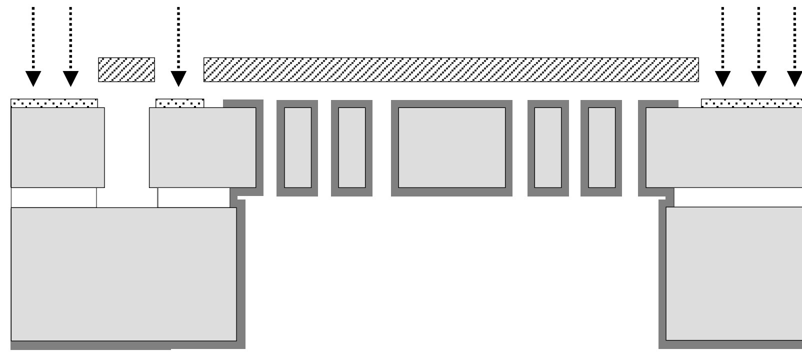
(b) Silicon nitride deposition by PECVD on both sides



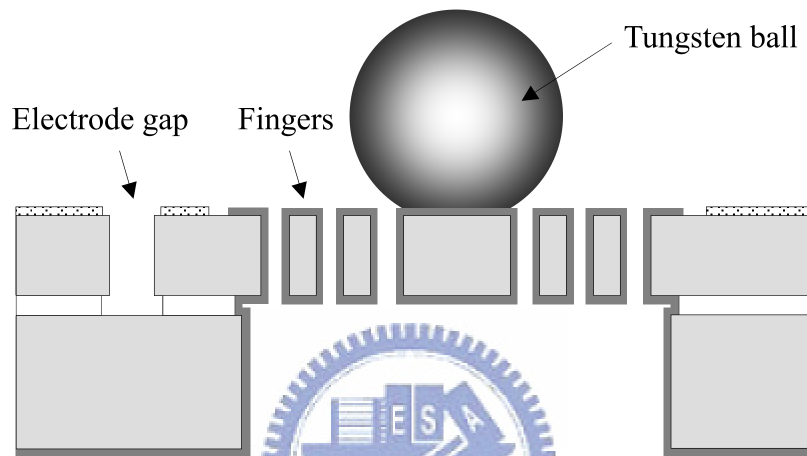
(c) Silicon nitride patterning by RIE and shadow mask

Silicon Oxide Photo resist Nitride Aluminum

Fig. 3.9 Modified fabrication process flow beginning from the release step



(d) Metal deposition with a shadow mask



(e) Wire bonding and external tungsten metal mass ball attachment

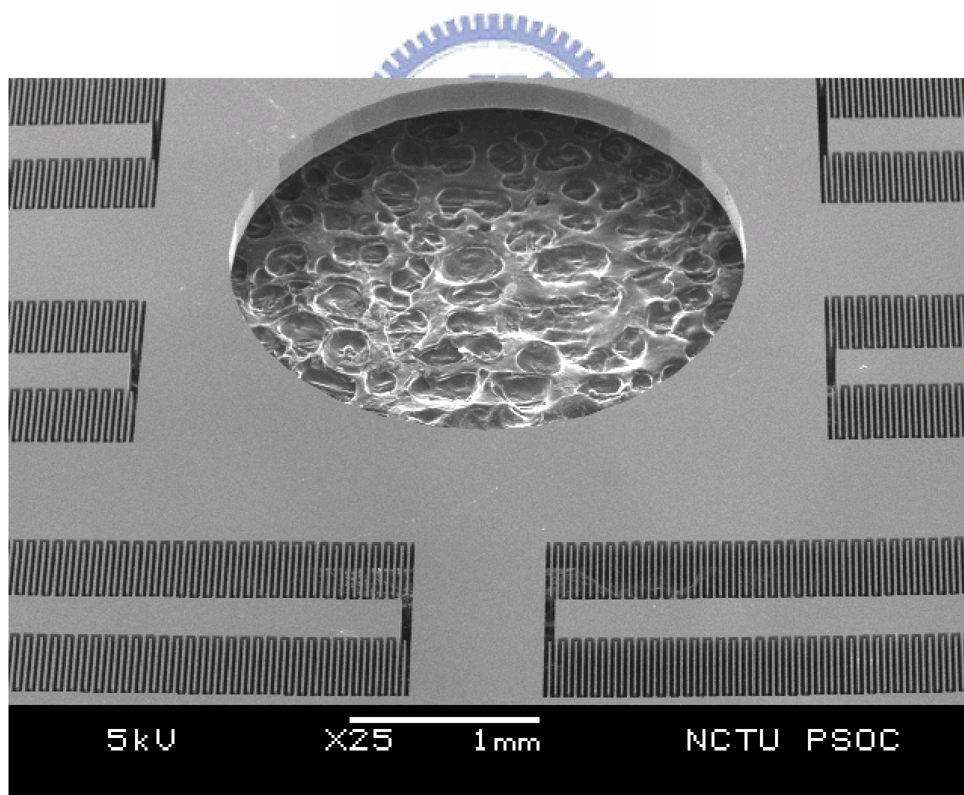
Fig. 3.9 Modified fabrication process beginning from the release step (continued)

The device needs to be carefully cleaned before the PECVD silicon nitride deposition. If particles exist between the electrodes during the deposition, they may lead to parasitic resistance. The current devices are robust to ultrasonic acetone cleaning and activated sulfuric acid cleaning. This increases the possibility to remove all unwanted particles on the device. Silicon nitride patterning and metallization are subsequently performed. The metal is only applied to the contact pad areas in order to eliminate parasitic resistance and shortage between electrodes.

3.4 Fabricated device

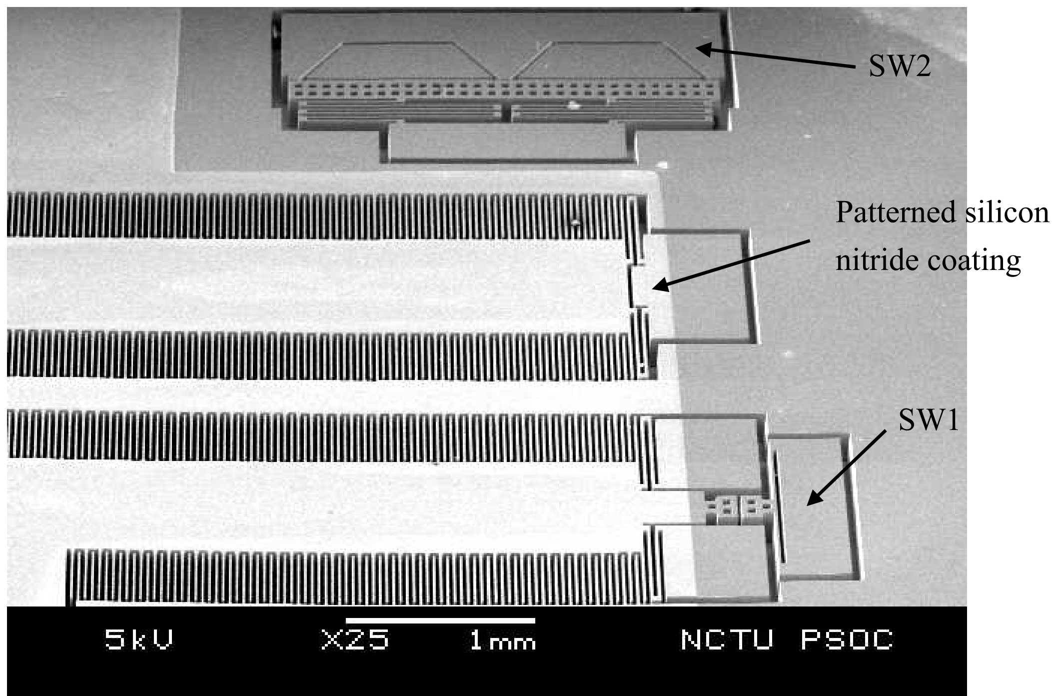
The scanning electron microscope (SEM) overview of the SOI device fabricated by the modified process is shown in Fig. 3.10. The device here does not yet have the metal layer due to the lack of suitable shadow mask.

Close-up SEM photographs of the successfully fabricated finger bumps are also shown in Fig. 3.11. The stick-out length of the bump structure is measured to be 0.5 μm, which is the same as the designed value. The finger bumps can withstand the ICP etching process inaccuracy and maintain designed stick-out distance as long as the notching effect is properly avoided.



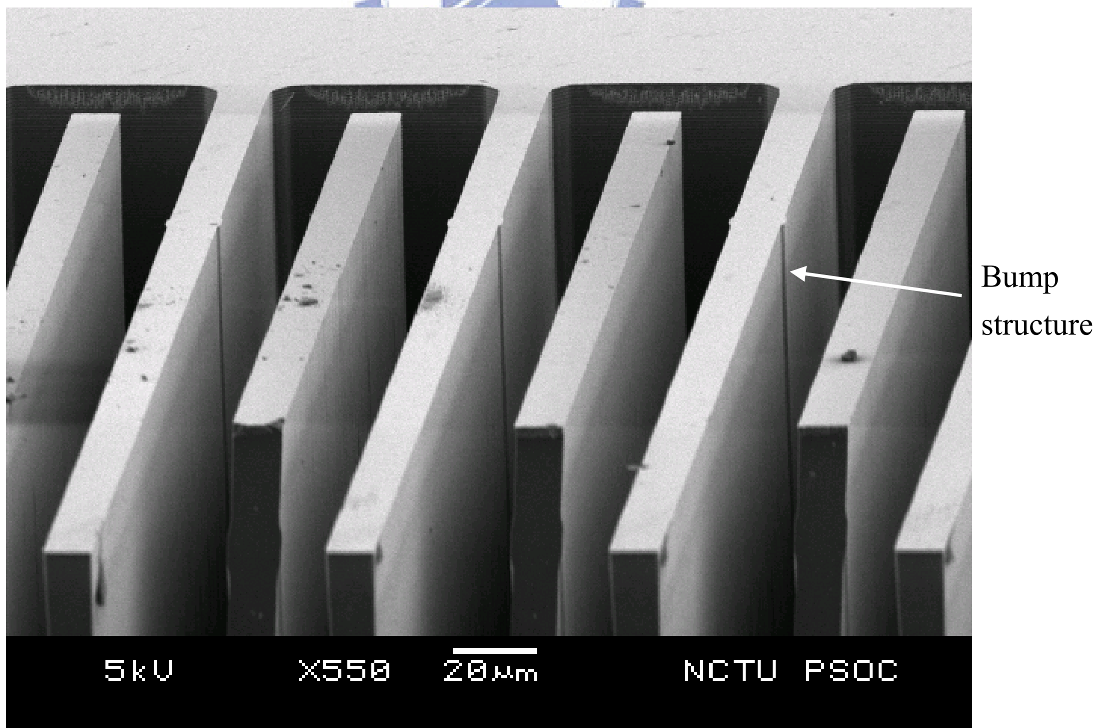
(a)

Fig. 3.10 SEM overview of the fabricated device, (a) center, (b) corner



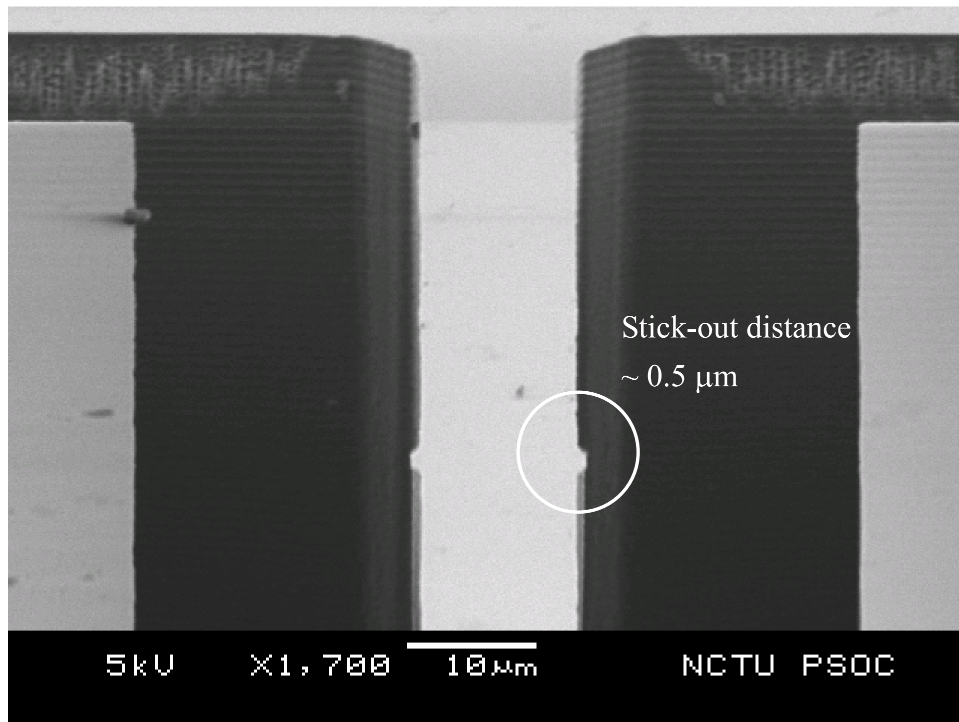
(b)

Fig. 3.10 SEM overview of the fabricated device (a) center (b) corner (continued)



(a)

Fig. 3.11 SEM photograph of finger bumps, (a) over view, (b) close up view



(b)

Fig. 3.11 SEM photograph of finger bumps, (a) over view, (b) close up view (continued)

Other critical locations of the device are shown in Fig. 3.12. The initial mask undercut is 0.5 μm per side, which is below expectation and results in a thicker finger width of 12 μm (Fig. 3.12 (a)). The measured finger height is 200 μm and the notching effect is minimal (Fig. 3.12 (b)). The perpendicularity is approximately 89 ± 0.9 degrees, indicating minimum sidewall barreling. The switches SW1 and SW2 have the same geometry as the layout (Fig. 3.12 (c), (d)). With the initial mask undercut as mentioned above, the switch gaps are 24.5 μm and 18 μm, respectively. All guarding and blocking structures were removed successfully.

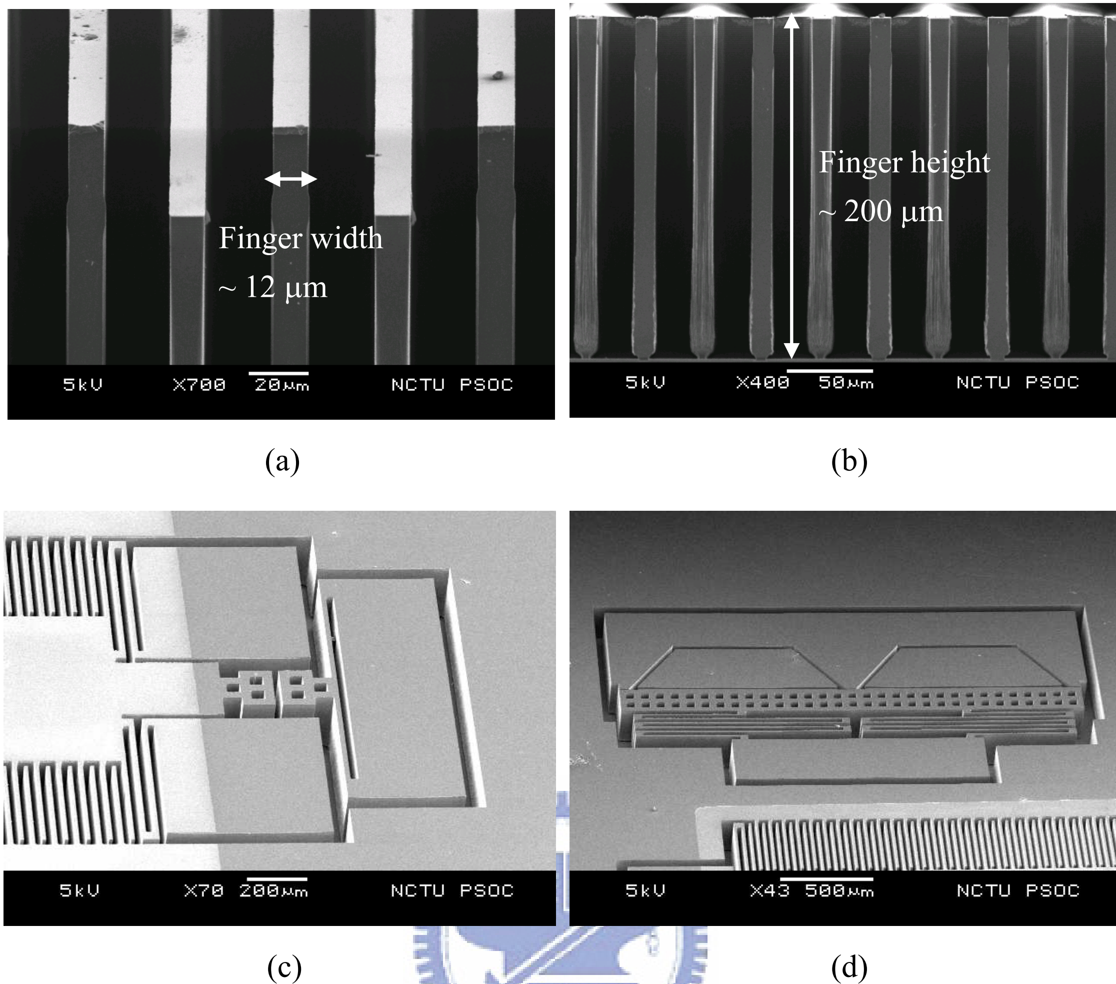
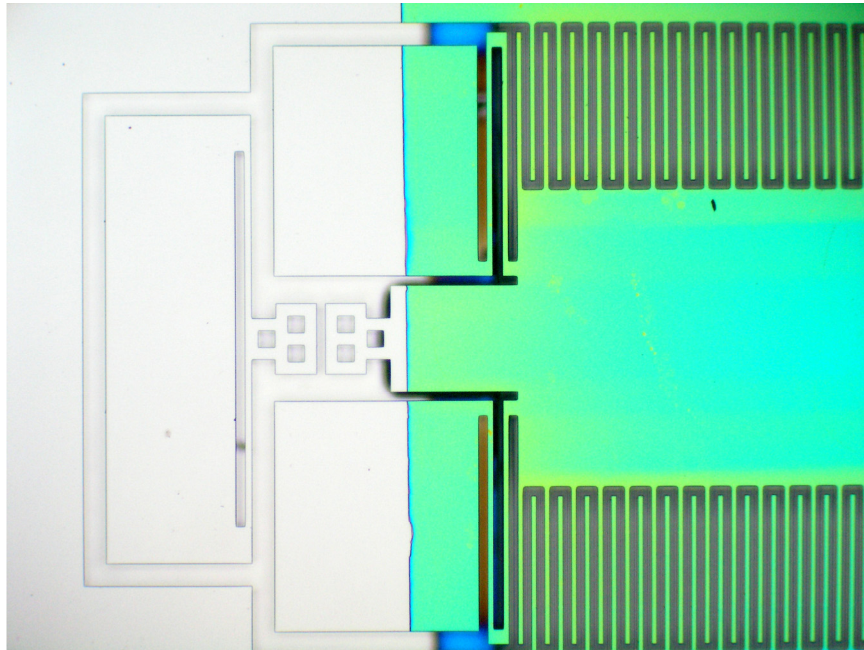
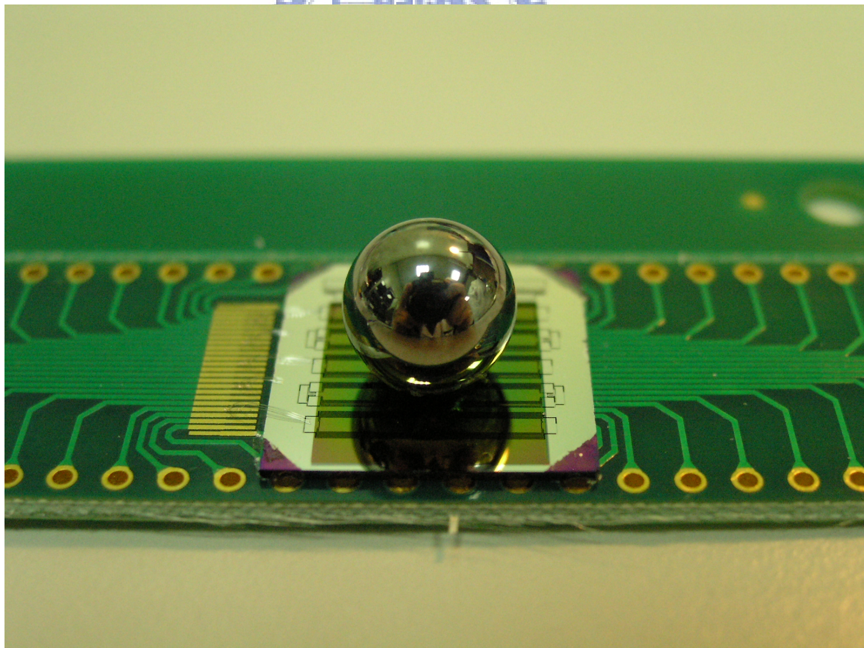


Fig. 3.12 SEM of the fabricated SOI device, (a) finger width, (b) finger height, (c) SW1, (d) SW2

Figure 3.13 (a) shows the optical microscopic view of the device with nitride coating on fingers and springs. Figure 3.13 (b) shows the overview of the whole device with external tungsten ball attached and bonded to a PCB for testing. Adhesion glue was used to attach the external mass and silver paste was used to bond the chip to the PCB for further wire bonding. Aluminum was deposited on the contact pads by thermal coating with a shadow mask. Anchor pads were then wire bonded to the PCB. SW2 was also wire bonded to the variable capacitor.



(a)

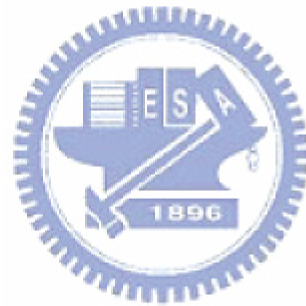


(b)

Fig. 3.13 (a) Overview of the fabricated SOI device, (b) device with external tungsten mass attached

3.5 Conclusion

The fabrication of the high aspect ratio SOI device with the back side substrate removed was successful. With silicon oxide hard mask, front side guarding and back side blocking structures and moderately tuned standard Bosch ICP process, most of the issues in the deep silicon etching process were eliminated. Electrical shortage between fingers was overcome by a post release silicon nitride deposition and patterning using an additional shadow mask. Metal deposition caused electrical shortage was found and an accurately aligned shadow mask was proposed to solve the problem. Further measurements on the device will be presented in the next chapter.

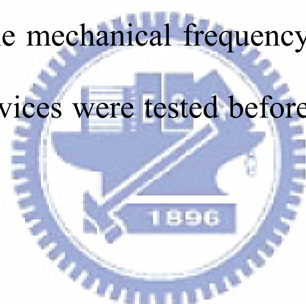


Chapter 4 Measurement and Experimental Results

The measurement of the capacitive vibration-to-electric energy converter fabricated by SOI deep silicon etching technology is presented in this chapter. Device measurements include mechanical measurement, static electrical measurement, and dynamic electro-mechanical measurement. Measured data are compared with the device design in Chapter 2 in order to obtain information of device deviations.

4.1 Mechanical measurement

Mechanical characteristics of the device are measured with input vibration. The main concern is to measure the mechanical frequency response of the device around its resonant frequency. The devices were tested before and after the external tungsten mass ball attachment.



4.1.1 Mechanical characteristics without external mass

The devices were first tested by a probe station to see if they were properly released. The devices without external mass attachment were then measured by the MEMS Motion Analyzer (MMA) system at the National Chip Implementation Center (CIC). The MMA system utilizes image processing technique and measures the periodic relative motion between the movable and the still structures of the device. A shaker was used to provide the input vibration. The photograph of the MMA measurement setup provided by CIC is shown in Fig. 4.1 (a). The device under static condition is shown in Fig. 4.1 (b) and the device driven by the input vibration is shown in Fig. 4.1 (c).

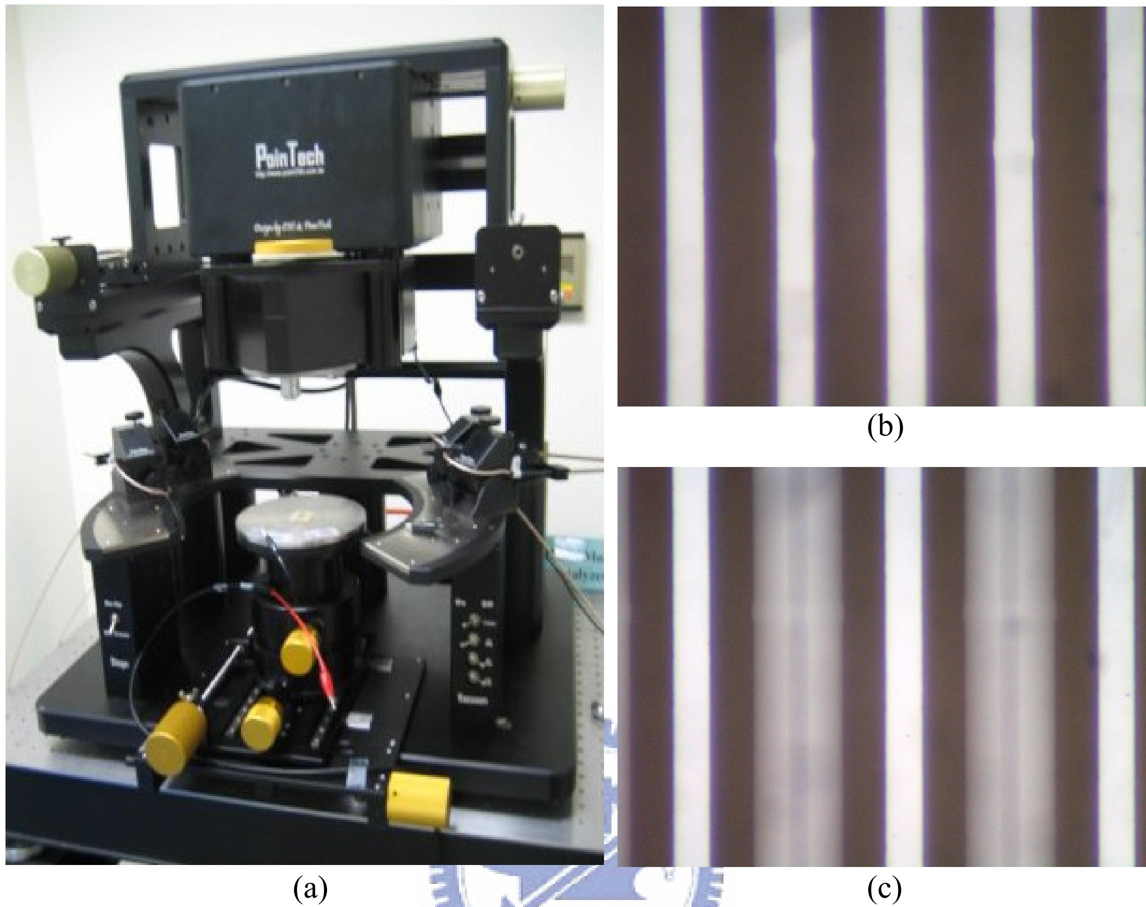
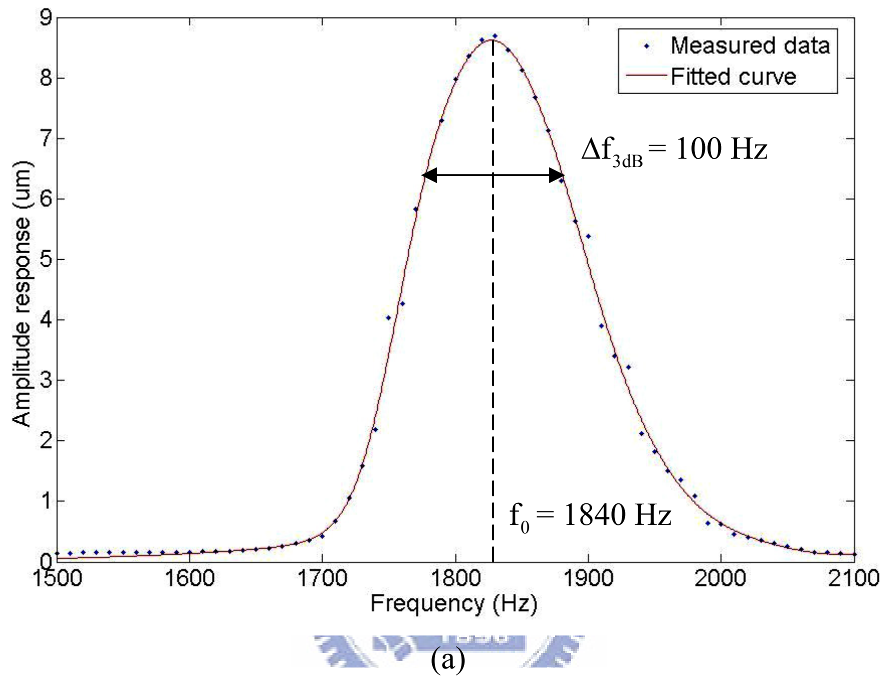


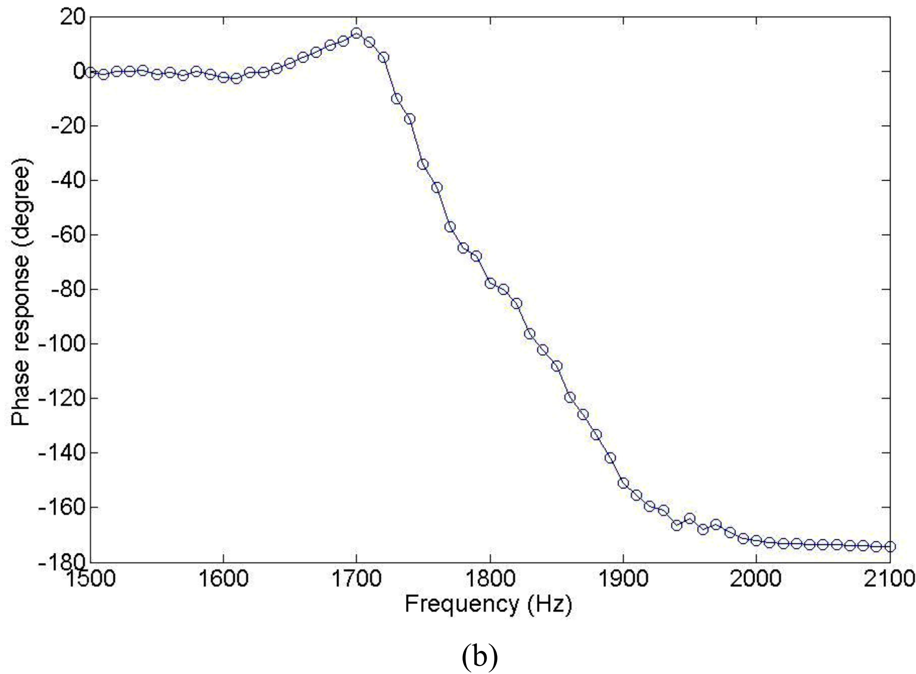
Fig. 4.1 MMA system, (a) instrument setup, (b) device under static condition, (c) device driven by input vibration at 1.84 kHz

The MMA measurement results are plotted in Fig. 4.2. The resonant frequency is about 1840 Hz with a corresponding -90° phase shift at resonant. The data are compared with the designed resonant frequency of 1730 Hz from the CoventorWare simulation, as discussed in Chapter 2. The slight increase of the measured resonant frequency is due to the increase of the mechanical spring constant. Because of the smaller than predicted mask undercut during the ICP etching process, the spring width is enlarged to from 11 μm to 11.7 μm, and the corresponding spring constant enlarged from 2425 to 2780 N/m. Thus, the resonant frequency is enlarged from 1730 Hz to 1840 Hz, which matches the measured data. From the measured amplitude response curve, it is seen that the 3dB bandwidth is about Δf_{3dB} = 100 Hz. With the resonant

frequency of $f_0 = 1840$ Hz, the quality factor $Q = f_0/\Delta f_{3dB}$ is approximately 18.4. This relatively low quality factor compared with conventional MEMS resonating devices is possibly due to two reasons. First, the number of finger gaps is extremely large compared with conventional MEMS devices. This results in a large mechanical



(a)

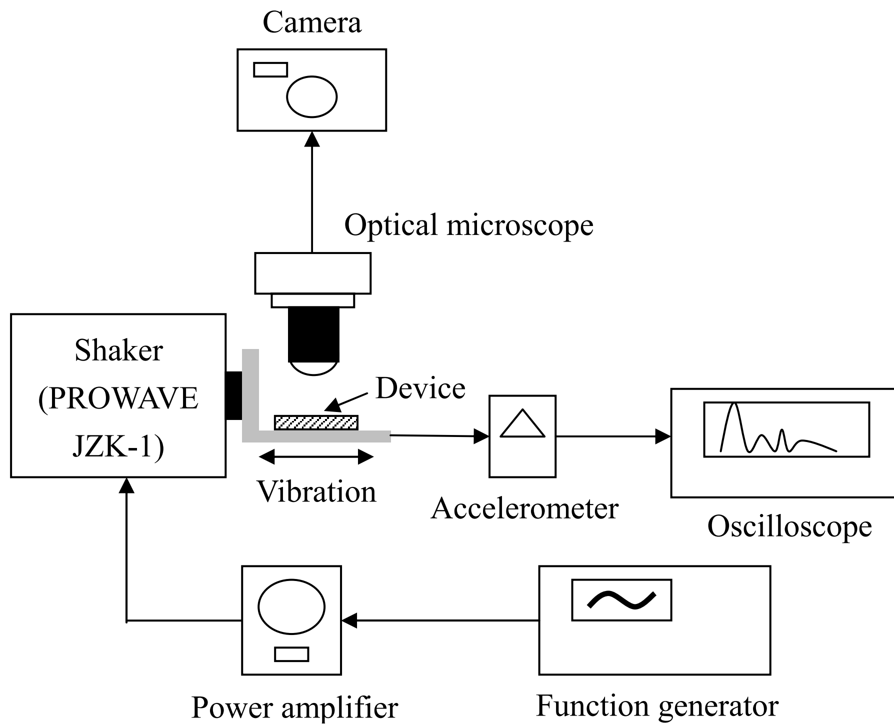


(b)

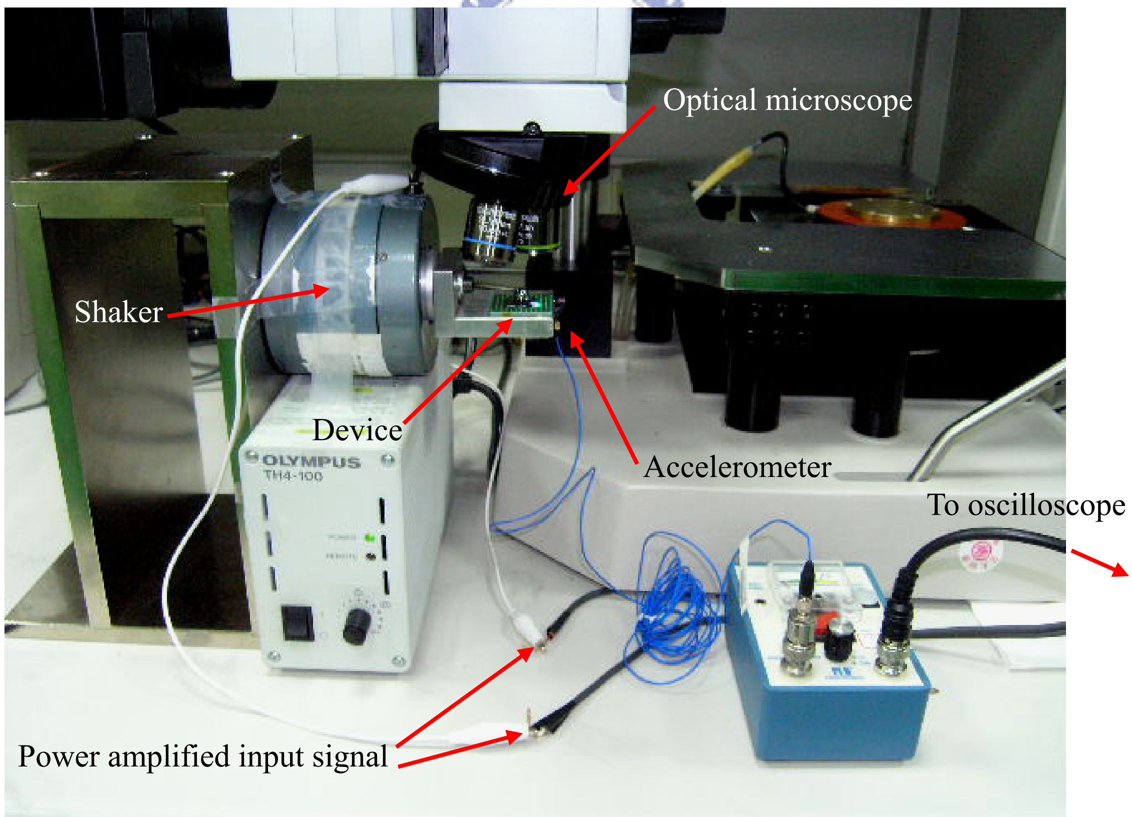
Fig. 4.2 MMA measurement results of the device without external mass, (a) amplitude response, (b) phase response

damping force for large device displacement, limiting the amplitude response peak. Second, in the long, deep and narrow structure, residual particles have high possibility of getting stuck between the fingers. This also tends to limit the maximum allowable displacement of the proof mass.

The mechanical behavior of other devices without the external mass was also measured by our own measurement system, as shown in Fig. 4.3. The output of the function generator was power amplified in order to drive the PROWAVE JZK-1 shaker. The input vibration was measured by a piezoelectric accelerometer module connected to an oscilloscope while the resonance of the device was observed by an optical microscope. Relative displacement was extracted from images captured by a digital camera. The observed resonant frequency is between 1890 Hz to 1915 Hz, which is slightly higher than the MMA results. The input acceleration measured by the accelerometer module is shown in Fig. 4.4 (a) with the sensor sensitivity of 10 mV/ms^{-2}. For the input vibration amplitude of about 24 m/s^2, the maximum relative displacement is about 9.5 μm, as shown in Fig 4.4 (b). The large output acceleration of the shaker is slightly distorted, as observed by the accelerometer (Fig. 4.4 (a)). Both the MMA measurement and our own measurement show that the deviation of the resonance frequency of the fabricated devices is small.

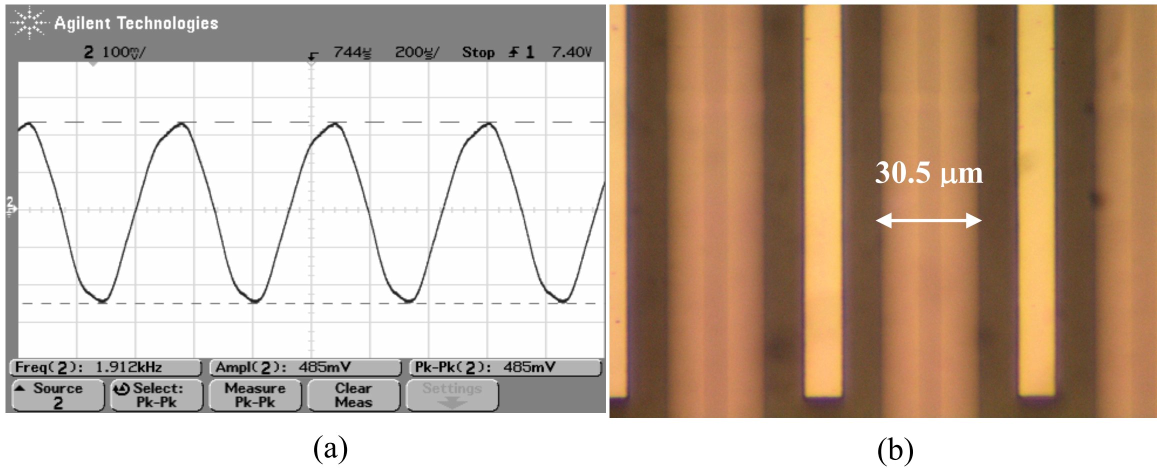


(a)



(b)

Fig. 4.3 (a) Measurement system schematics, (b) photograph of the measurement system setup



(a) (b)

Fig. 4.4 (a) Measured acceleration by the piezoelectric accelerometer at 1912 Hz, (b) device at resonance (relative displacement is about 9.5 µm)

4.1.2 Mechanical characteristics with external mass

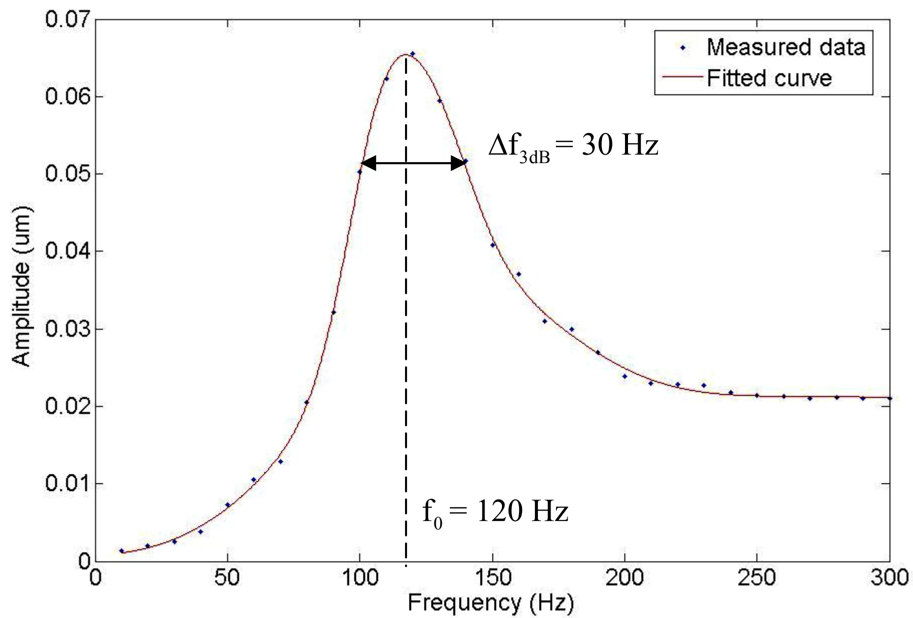
After the mechanical measurement on the devices without the external mass, a 4 gram (Φ 4 mm) tungsten ball was carefully bonded to the device, and the same mechanical measurements were performed again. The MMA measurement is shown in Fig. 4.5. The resonant frequency is around 120 Hz, close to the expected value. This amplitude response matches a spring-damper-mass system characterized by the equation

$$\left|\tilde{X}_r\right| = \frac{m\omega^2}{\sqrt{(k-m\omega^2)^2+b^2\omega^2}}\left|\tilde{X}_i\right|. \tag{4.1}$$

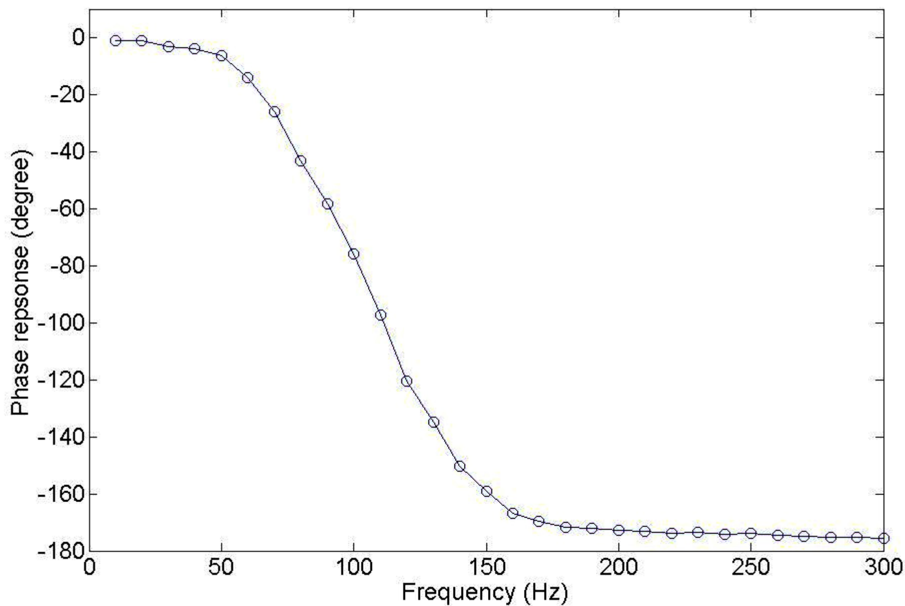
With X_i as the input displacement amplitude and X_r as the output displacement amplitude, the response is zero at DC frequency and constant when frequency is over the resonant frequency. The amplitude response indicates a 3dB bandwidth of about $\Delta\omega$ = 30 Hz, and the quality factor is therefore 4. Such a low value does not match the expectation by the equation

$$Q = \sqrt{\frac{km}{b^2}}, \tag{4.2}$$

which indicates that the quality factor should increase with increasing proof mass. The effect is assumed to originate from the unpredictable damping and inertial force caused by the external mass. Further study on this effect will be conducted in the future.



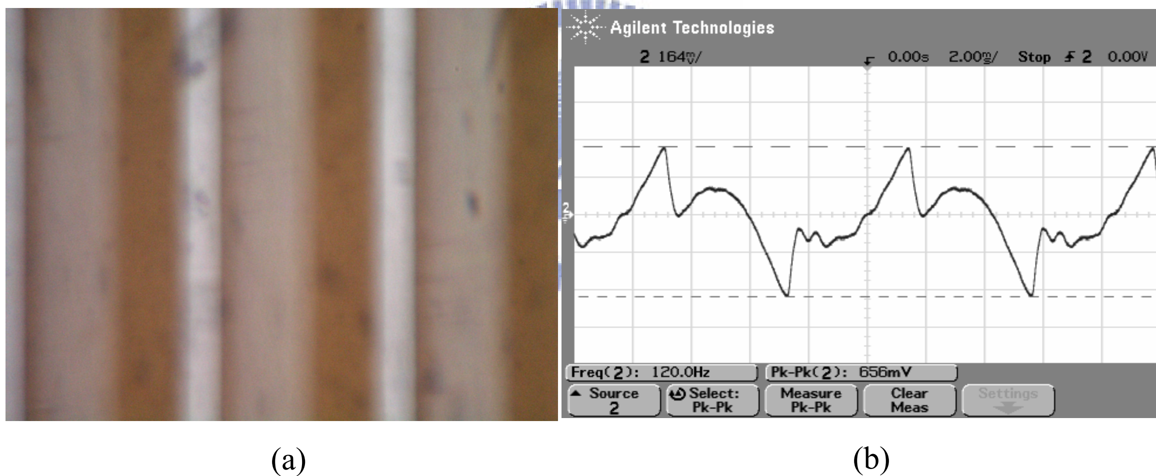
(a)



(b)

Fig. 4.5 MMA measurement of the device with external mass attached, (a) amplitude response, (b) phase response

Measurement using our own measurement system was also performed. The observed resonant frequencies of the devices with external mass attached were similar to the MMA data. The device resonance ranged from 105 to 130 Hz. Due to the large inertial force caused by the proof mass, the device has large displacement for a small input vibration acceleration of about 10 m/s^2. The device at resonance at 120 Hz is shown in Fig. 4.6 (a). The image is blurred due to the large input and output displacement. The performance of the shaker at this low frequency is not very well. Thus, the input vibration acceleration signal is severely distorted, as shown in Fig. 4.6 (b).



(a) (b)

Fig. 4.6 (a) Device with the external mass attached at resonance, (b) measured acceleration at 120 Hz

4.2 Static electrical measurement

In static electrical measurement, the variable capacitance and parasitic effects were measured. In order to obtain more accurate and confident results, several measurement circuits and instruments were employed.

4.2.1 Measurement circuit

Static electrical measurement was conducted to measure the voltage increase on the variable capacitor in the kinetic to electrical energy conversion cycles. Measurement circuits are shown as in Fig. 4.7. The basic operation of the circuit in Fig. 4.7 (a) is to pre-charge the variable capacitor C_v by V_T through SW_T at the C_{max} position. When SW_T is opened and the capacitance is decreased simultaneously, the voltage increasing effect is observed. A TLC279 CMOS operational amplifier with high input impedance (above 1 TΩ) in a unity gain buffer configuration was used to decouple the resistance and capacitance load of the measurement system on the variable capacitor. The single-supply TLC279 operation amplifier can tolerant a V_{DD} up to 18 V, which sets the limit on the input terminals.

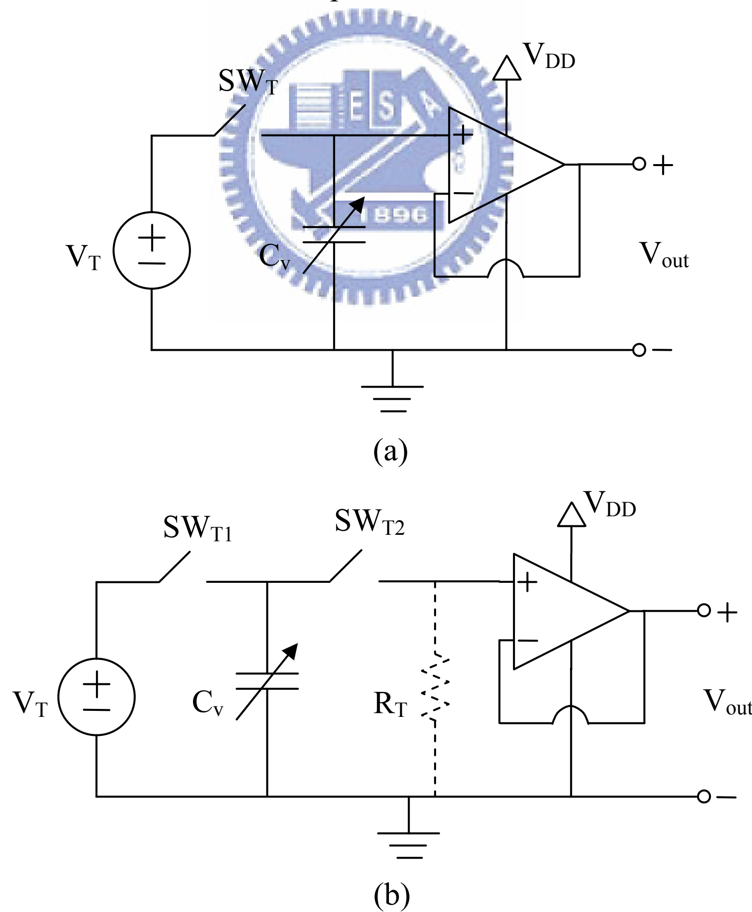


Fig. 4.7 (a) Circuit used to measure the voltage increasing effect, (b) circuit with additional resistance and switch

Unfortunately, the attempt to utilize such a measurement circuit was not successful. The measured signal exhibited erroneous floating or discharging condition. Possible reasons are the parasitic resistance in the device and network. Another circuit shown in Fig. 4.7 (b) was employed. After SW_{T1} was opened, C_v was decreased. SW_{T2} was then closed to observe of the RC discharge of the output voltage. The results were the same as previous experiments. There seemed to be no charge stored in C_v, indicating the existence of a parasitic resistance.

According to the above experience, the above measurement was abandoned. Attention was then focused on the measurement of capacitance change. A new measurement circuit, as shown in Fig. 4.8, was constructed to measure the RC discharge time constant versus capacitance change. In this case, SW_r is a relay controlled by a 5 V input V_{tri}. The relay SW_r is initially closed and the variable capacitor is charged to V_T. The relay SW_r is subsequently opened at the falling edge of the control voltage V_{tri} and the charge on C_v is discharged through R_T. The falling edge of V_{tri} is also utilized to trigger the single run measurement of the oscilloscope. Measurement of different RC time constants is conducted. This capacitance change is compared with the data acquired by an INSTEK-LCR-816 LCR meter and information on the variable capacitance and parasitic effects can be obtained. Notice that the input capacitance of the unity gain buffer is only a few pF, and the input resistance is above 10^{12} Ω, thus the load effect can be neglected during measurement. The parasitic capacitance of the discrete 10 MΩ resistor R_T is measured to be about 42 pF. This parasitic effect must be considered during data analysis.

Another measurement circuit is setup to measure the parasitic resistance in the device, as shown in Fig. 4.9. The DC current through the device is zero if no parasitic resistance exists, resulting in a zero voltage drop across R_T. The input bias current of the TLC279 CMOS operational amplifier is below 100 pA, and the output voltage

offset caused by the buffer can be neglected.

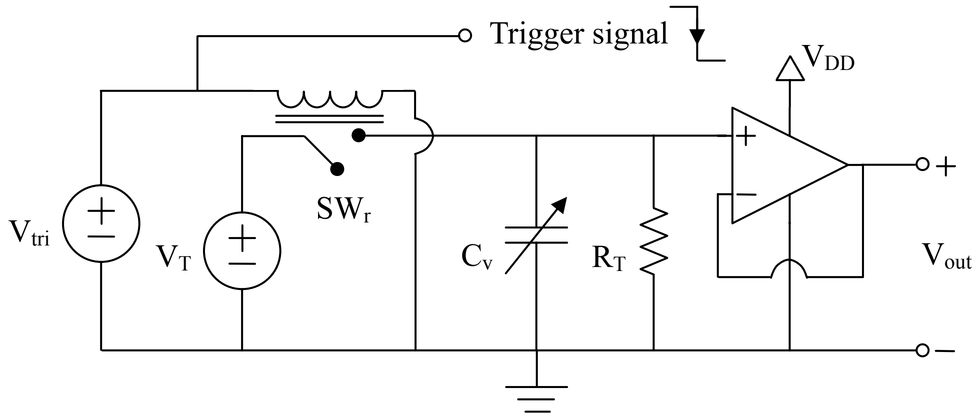


Fig. 4.8 Circuitry used for capacitance variation measurement

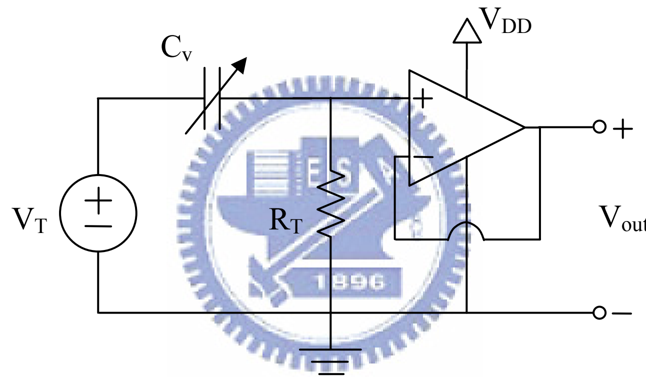


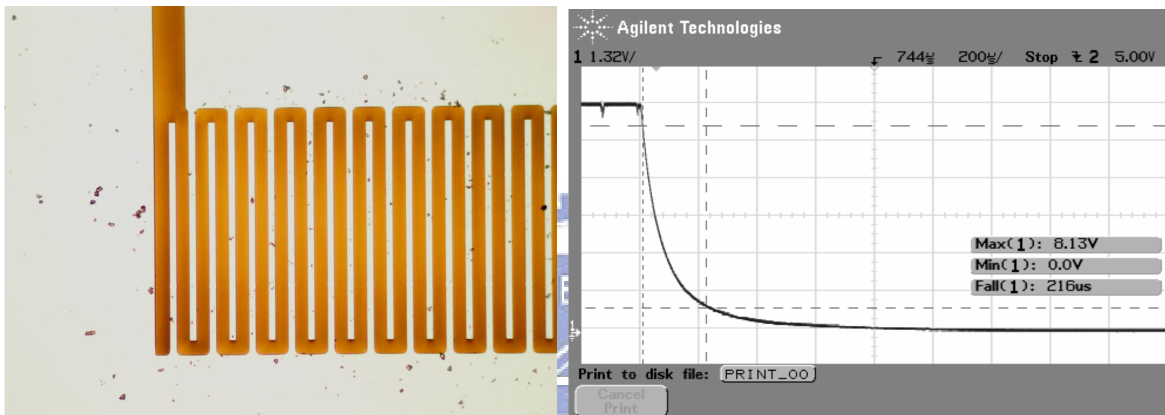
Fig. 4.9 Parasitic resistance measurement circuit

4.2.2 Variable capacitor measurement

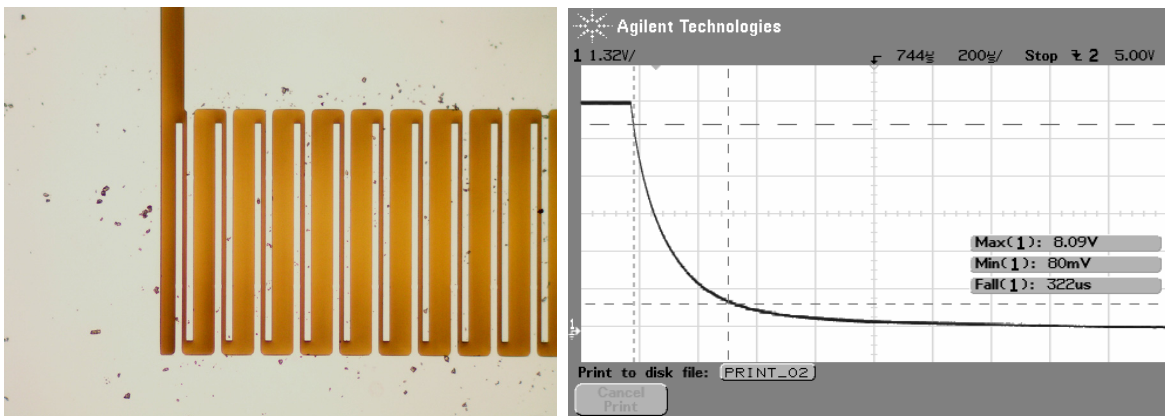
Measurement was first conducted on the devices fabricated using the original fabrication process. The silicon nitride layer was removed by the release process and aluminum deposition was done by sputtering. By the LCR meter, the variable capacitance C_v ranges from 120 pF to about 300 pF. Compared to the theoretical variable capacitance ranging from 62 pF to 1570 pF, the results indicate a parasitic capacitance of about 60 pF in the device. Furthermore, the maximum achievable C_{max} of the device is much lower than the predicted value. A parasitic resistance between

800 kΩ to 1 MΩ was also observed by the LCR meter. Using the measurement circuit in Fig. 4.9 with V_T = 8 V and R_T = 10 MΩ, the output voltage was 7.3 V, indicating a parasitic resistance of about 810 kΩ. This result agrees with the LCR meter results.

Utilizing the measurement circuit in Fig. 4.8 with a R_T of 10 MΩ and a V_T of 8 V, the RC discharge time constant versus capacitance variation is measured. Figure 4.10 shows the RC discharge for different positions of the variable capacitor. The variable capacitor is displaced by a microprobe and the static displacement is measured from

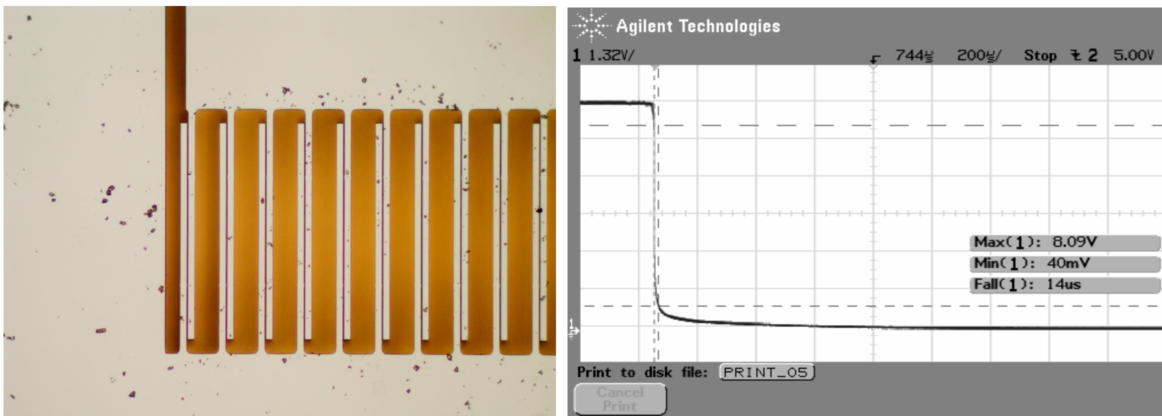


Static displacement ~ 0 μm RC discharging time constant ~ 80 μs



Static displacement ~ 17.5 μm RC discharging time constant ~ 110 μs

Fig. 4.10 RC discharge time constant measurement at different positions of the variable capacitor (original fabrication process)



Static displacement ~ 25 μm

RC discharging time constant ~ 5 μs

Fig. 4.10 RC discharge time constant measurement at different positions of the variable capacitor (original fabrication process) (continued)

the images captured by an optical microscope. RC discharge time constant is defined as the 100 % to 37 % voltage drop time span. The measured RC discharge time constant versus displacement is plotted in Fig. 4.11. From the plot, it is seen that the time constant does indeed increase with increasing displacement, indicating that the capacitance increases. As the capacitor approaches the maximum displacement, the time constant suddenly decreases, indicating discharge due to shortage between the fingers. This is a proof of the silicon nitride removal during the release process. With the parasitic capacitance considered, the theoretical RC discharge time constant is also plotted in Fig. 4.11. The measured time constant is close to the theoretical values at smaller displacements. At larger displacements before shortage, the measured time constant falls below the theoretical value. This indicates a smaller capacitance change in the variable capacitor. The parasitic capacitance introduced by the measurement circuit should be related with this smaller capacitance change. Further research is needed to construct a more accurate variable capacitor model as well as decouple the parasitic effect of the measurement circuit.

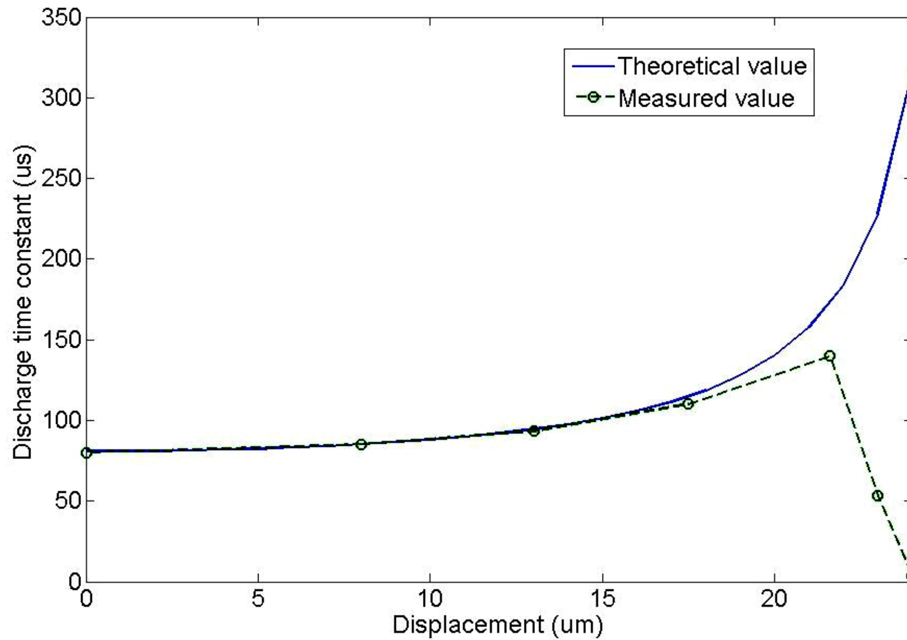
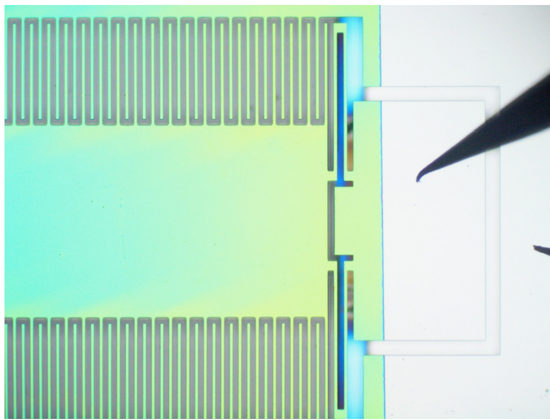
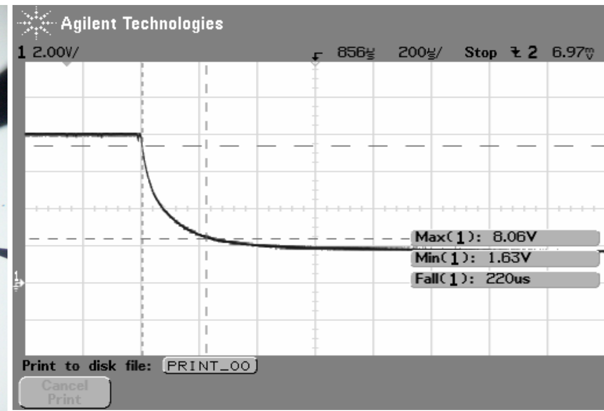


Fig. 4.11 Measured and theoretical RC discharge time constant versus displacement (original fabrication process)

The same measurement was performed on the devices fabricated with the modified fabrication process. The silicon nitride coating was successfully preserved and the aluminum was deposited by thermal coating. The LCR meter shows that the variable capacitance ranges from 120 pF to about 385 pF, which is similar to the previous measurement. A parasitic resistance of about 9000 kΩ was also observed. Using the measurement circuit of Fig. 4.9 with the same measurement conditions, the output voltage was 5.4 V. This indicates a parasitic resistance of 5000 kΩ. The measurements show that the metal thermal coating process provides a larger parasitic resistance.

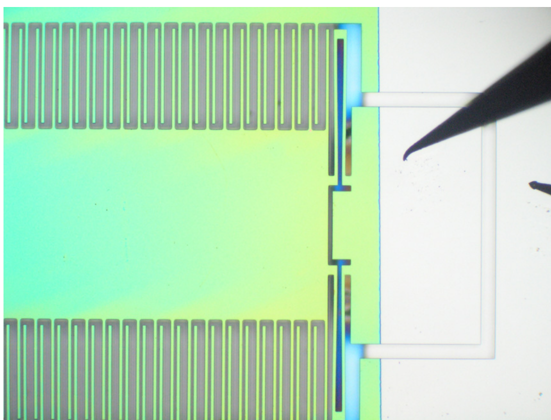
The discharge time constant measurement is shown in Fig. 4.12 with V_T = 8 V and R_T = 5 MΩ. The discharge time constant increases with increasing displacement. No severe discharging is observed even when fingers touch, indicating that the silicon nitride coating was successfully preserved in the modified fabrication process. In this case, the discharge resistance is equal to the parallel connection of R_T and the

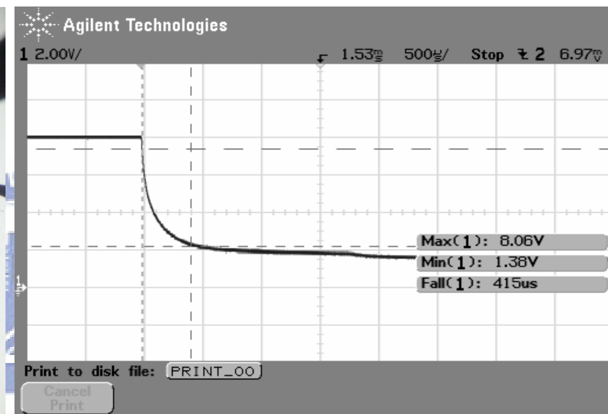




Static displacement ~ 0 μm

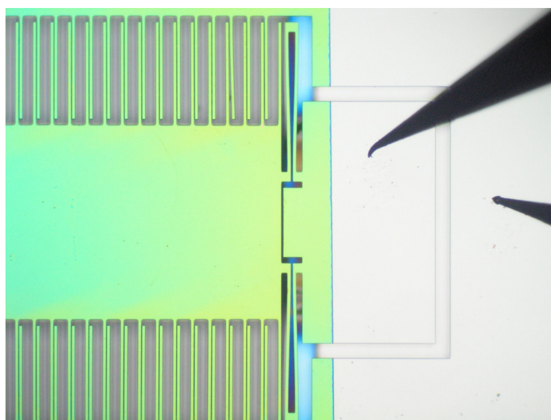
RC discharging time constant ~ 80 μs

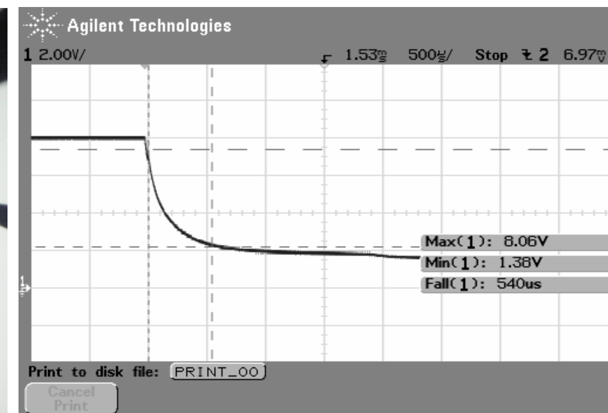




Static displacement ~ 13 μm

RC discharging time constant ~ 150 μs





Static displacement ~ 25 μm

RC discharging time constant ~ 200 μs

Fig. 4.12 RC discharge time constant measurement at different positions of the variable capacitor (modified fabrication process) (continued)

parasitic resistance. Thus, the variable capacitance can be calculated, as shown in Fig. 4.13. The measured capacitance is close to the theoretical values at smaller displacements, but still falls behind the theoretical values at larger displacements. Higher C_{max} can be achieved in this case since a larger displacement can be reached without shortage.

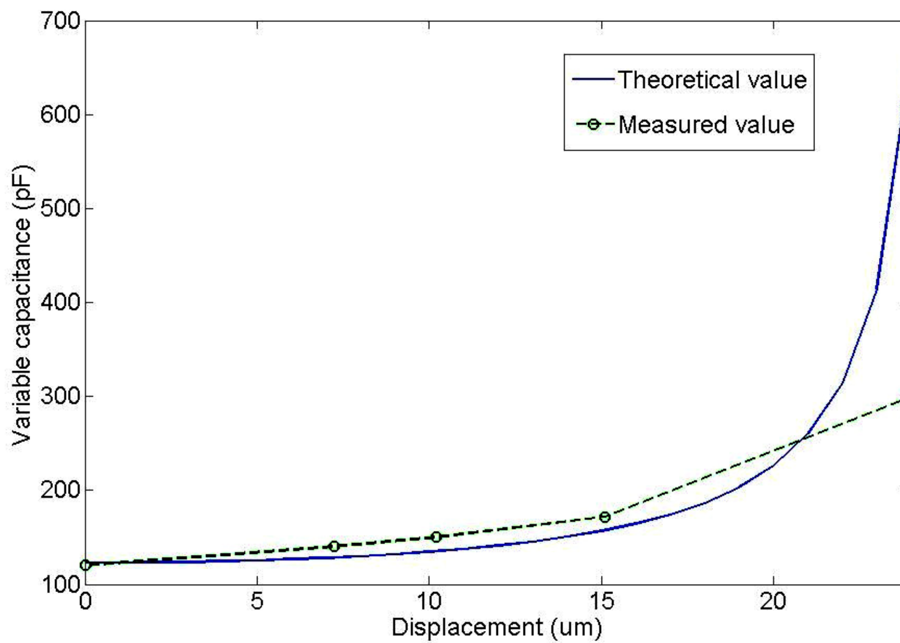


Fig. 4.13 Measured and theoretical capacitance versus displacement (modified fabrication process)

From the above static electrical measurements, it is seen that the modified fabrication process successfully preserves the silicon nitride dielectric layer to prevent shortage between fingers. Parasitic capacitance of the device is successfully limited to below 60 pF by partially removing the back side substrate. Nevertheless, parasitic resistance still exists in the device, possibly due to unwanted metal conformal deposition. Further effort is needed to discover the origin of the parasitic resistance and eliminate the effect.

4.3 Dynamic electro-mechanical measurement

The output electrical measurement of the device with input vibration is discussed in this section. Due to the parasitic resistance in the device, the device operation with the mechanical switches could not be accomplished. Alternatively, another circuit was constructed to measure the AC output power. The DC output power measurement utilizing the circuitry proposed by Roundy [15] was also conducted.

4.3.1 AC output power measurement

The measurement circuit of Fig. 4.9 was utilized to measure the AC output power of the device. In the operation, an AC current is generated due to the change of C_v and results in an AC output power to the load R_T. The device does not need to reach the maximum displacement to deliver output power. Therefore, it can serve as an alternative energy conversion mechanism when the input vibration amplitude is low.

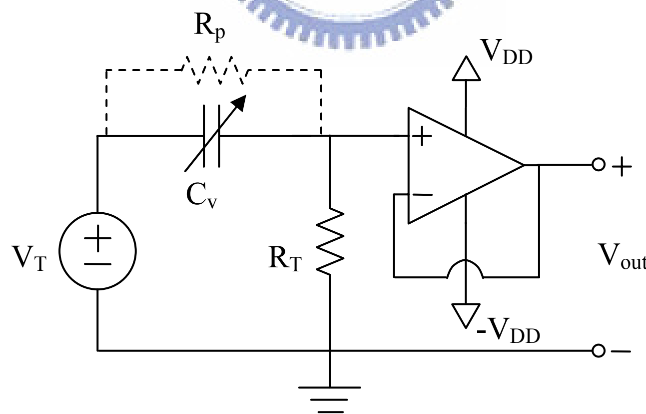


Fig. 4.14 Circuitry used for AC power measurement

With the parasitic resistance, the circuitry is modified to Fig. 4.14. With R_T = 5 MΩ and V_T = 8 V, the devices without external mass attachment were measured first. The measurement of a device operating at 2045 Hz is shown in Fig. 4.15. The output

voltage amplitude is measured to be 178.5 mV when the vibration acceleration amplitude is 22.5 m/s^2. There is a -90° phase shift between the input acceleration and the output voltage at resonance. The output voltage has a DC bias of about 6.5 V due to the parasitic resistance R_p. The small output voltage amplitude is mainly due to the parasitic resistance on the device, which limits the amount of charge variation on C_v during AC operation. The DC bias indicates a constant current flowing through R_T, leading to static power consumption of the device. Therefore, AC output power in this case is not considered.

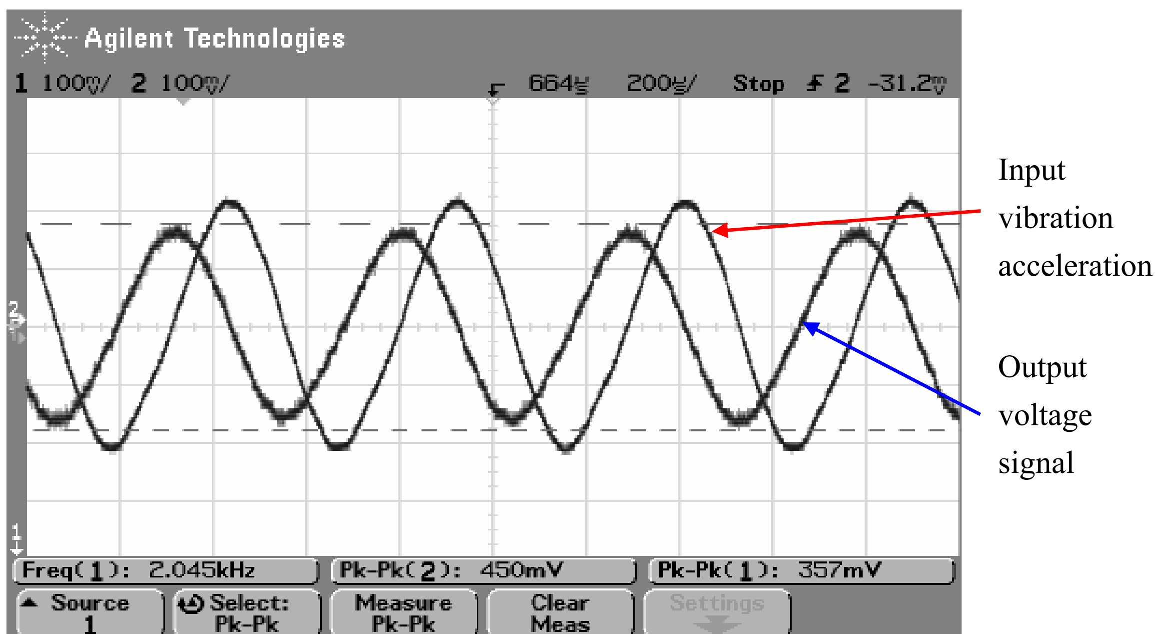


Fig. 4.15 AC output measurement without external mass

Another modified circuitry is shown in Fig. 4.16. Two additional 10 pF capacitors C_T are used to block the DC path of the variable capacitor. Thus, the DC bias level of the output voltage is reduced to zero, eliminating the static power consumption of the device. A 9 V battery supply is used for V_T in this measurement.

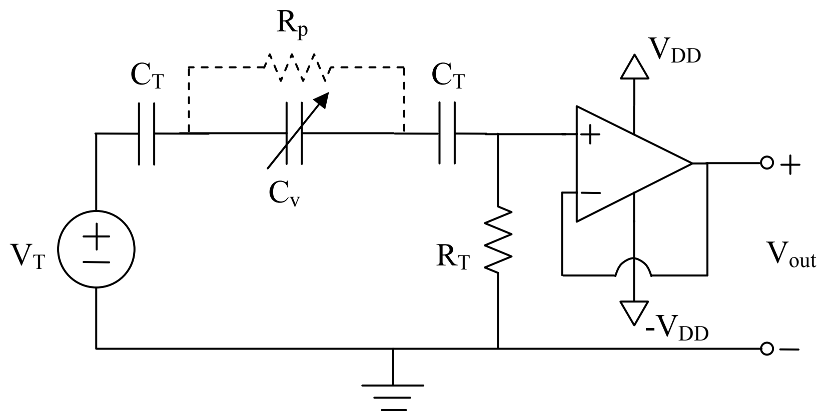
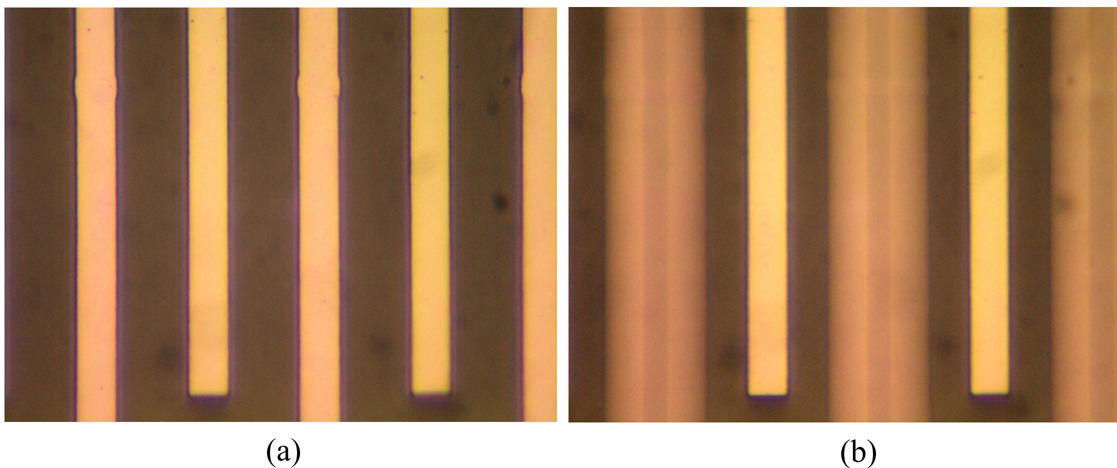


Fig. 4.16 Modified circuitry used for AC power measurement

Measurement of the AC output power with different values of R_T was conducted. The vibration acceleration amplitude is maintained at about 32.5 m/s^2. The devices under static condition and operating at the 1880 Hz resonant frequency are shown in Fig. 4.17. The device has a relative displacement of about 9.7 μm, and C_{max} is estimated as 170 pF (Fig. 4.13). Measured AC output power for various R_T is shown in Fig. 4.18. It can be seen that the output voltage is approximately sinusoidal, and the amplitude increases with R_T. If the parasitic capacitance of the network and the C_v change from 120 pF to 170 pF is considered, the AC output current amplitude is

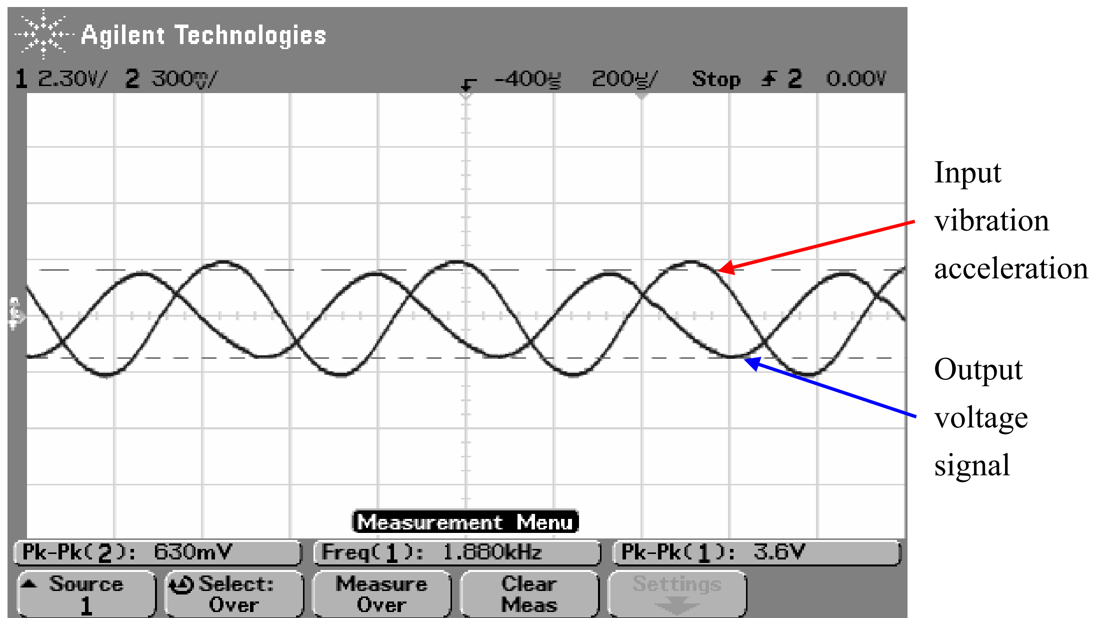


(a) (b)

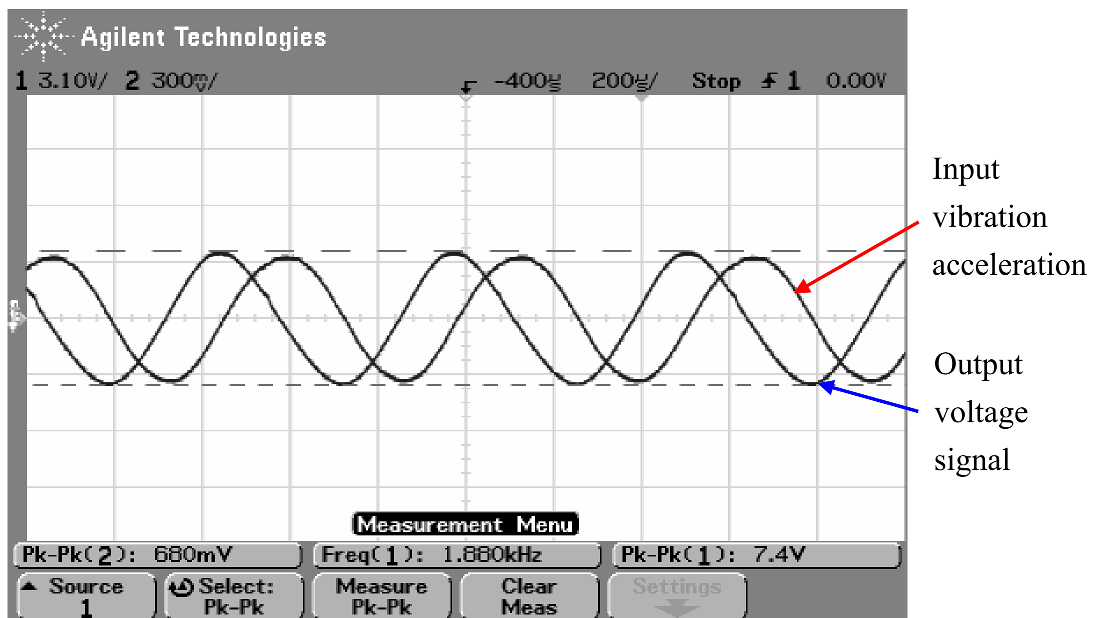
Fig. 4.17 Device during AC output power measurement, (a) static condition, (b) resonance at 1870 Hz

estimated as 0.672 μA. When R_T is 5 MΩ, the output voltage amplitude should be about 3.36 V, which is close to the measured value. The output AC power can be estimated by

$$P_{out} = \frac{V_{out}^{2}}{2R_T}. \tag{4.3}$$

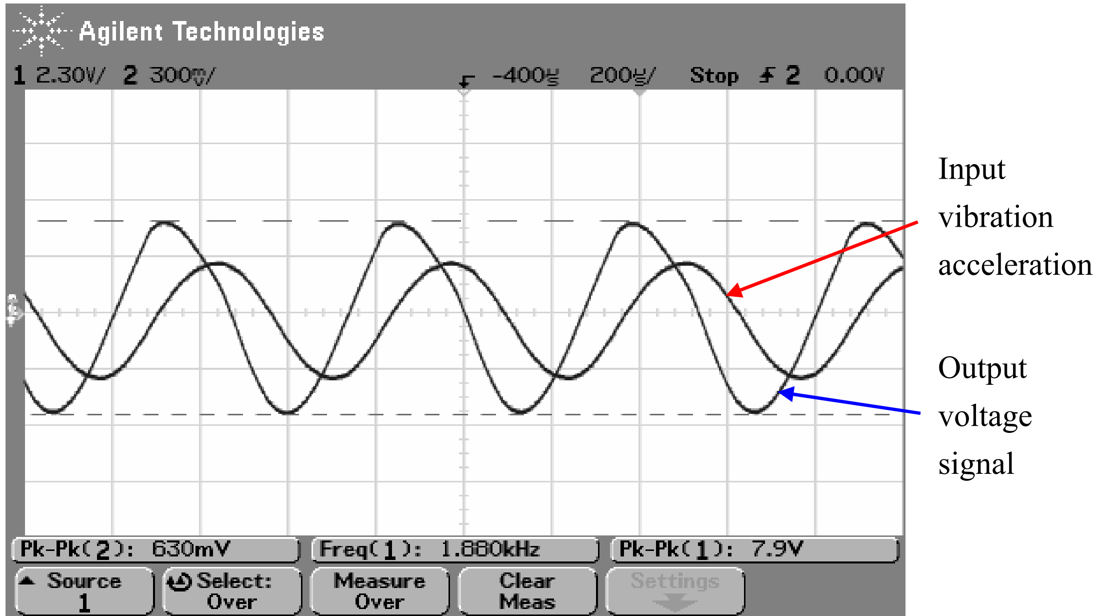


R_T = 1.667 MΩ

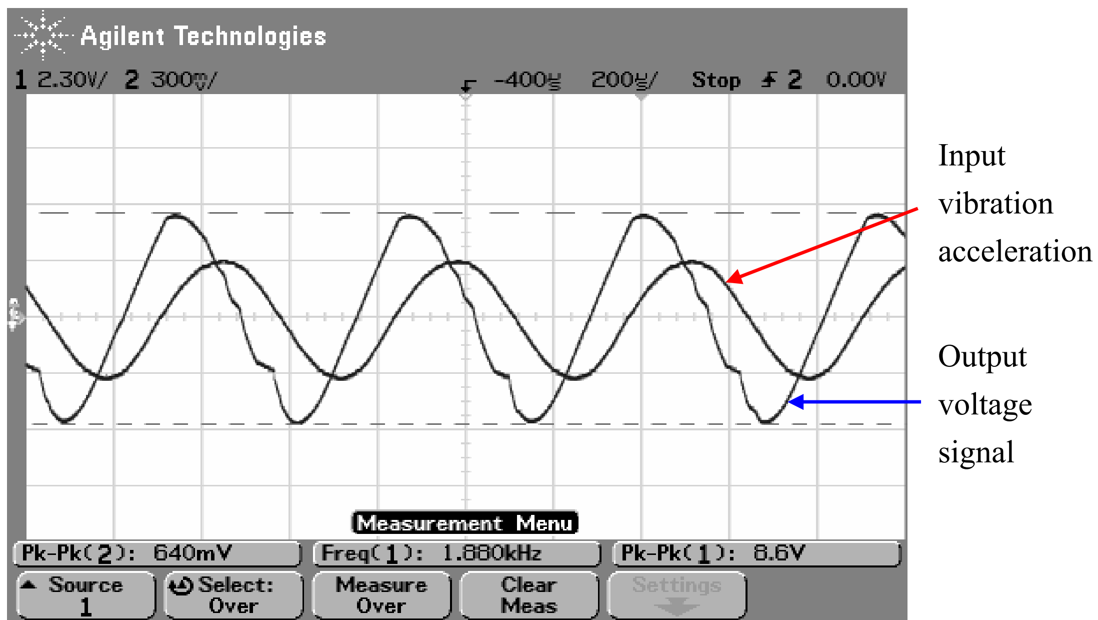


R_T = 5 MΩ

Fig. 4.18 Measurement of AC output power for various R_T



$R_T = 10$ MΩ



$R_T = 15$ MΩ

Fig. 4.18 Measurement of AC output power for various R_T (continued)

The measured output power versus R_T is plotted in Fig. 4.19. The maximum output power is 1.2 μW when the load resistance R_T is about 5 MΩ. If the relative displacement is increased to the maximum value of 23 μm, the variable capacitance can change from 120 pF to about 310 pF (Fig. 4.13). Under the same operation

frequency, the maximum output power with R_T = 5 MΩ should be 16 μW.

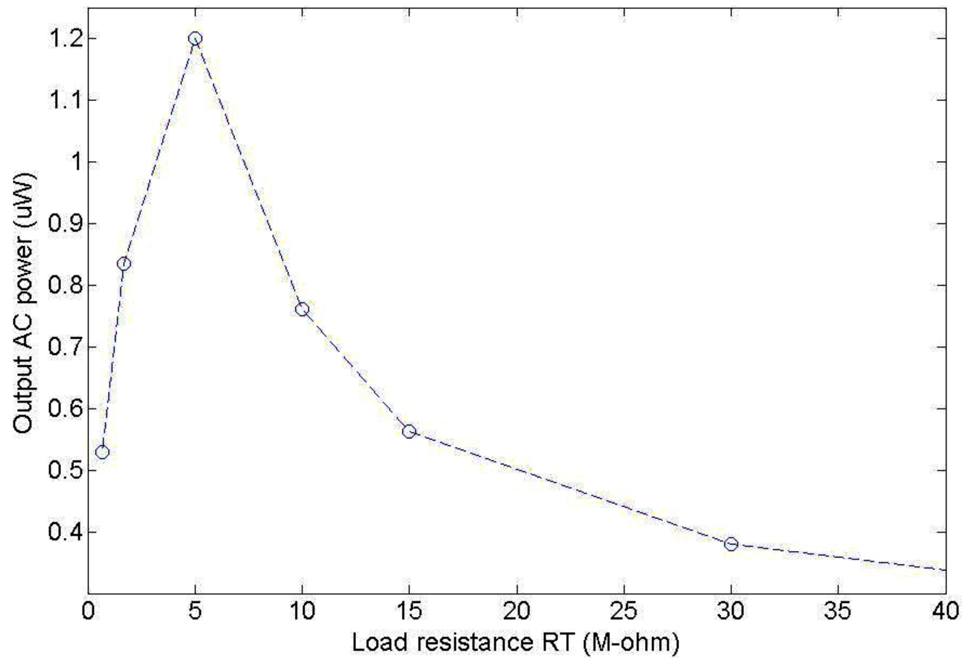


Fig. 4.19 Measured AC output power versus load resistance R_T

The AC output power measurement of the devices with the external mass attached was not conducted yet due to the shaker instability at the low frequency. Measurement instrument upgrade is in progress. With the external mass attached, the relative displacement can reach the maximum value at lower vibration acceleration. With the operation frequency of 120 Hz, the AC output power is expected to be in the range of 200 nW to 650 nW. This lower output power is due to the slower rate of change of capacitance, resulting in a lower output AC current. The optimal load R_T that can provide maximum output power needs to be known. Modeling and optimization of the conversion operation will be done in the future in order to obtain maximum energy conversion efficiency.

4.3.2 DC output power measurement

Due to the parasitic resistance, the mechanical switches in the current device could not function with the variable capacitor correctly. Therefore, we utilized the measurement circuit proposed by Roundy [15], as shown in Fig. 4.20, to measure the DC output power. The charge-discharge switches were realized by diodes. MOSFET and JFET can be connected as diodes and provide low reverse leakage current. However, the output power still could not be measured. The main reason could be the underestimated diode reverse leakage current. Voltage increase on C_v is also too low for the circuit to properly function.

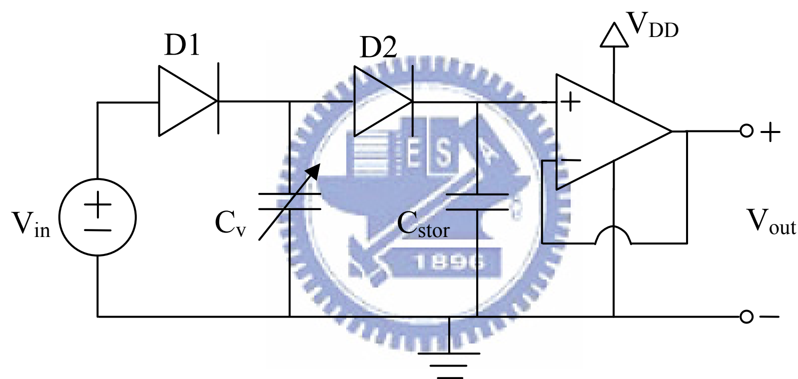
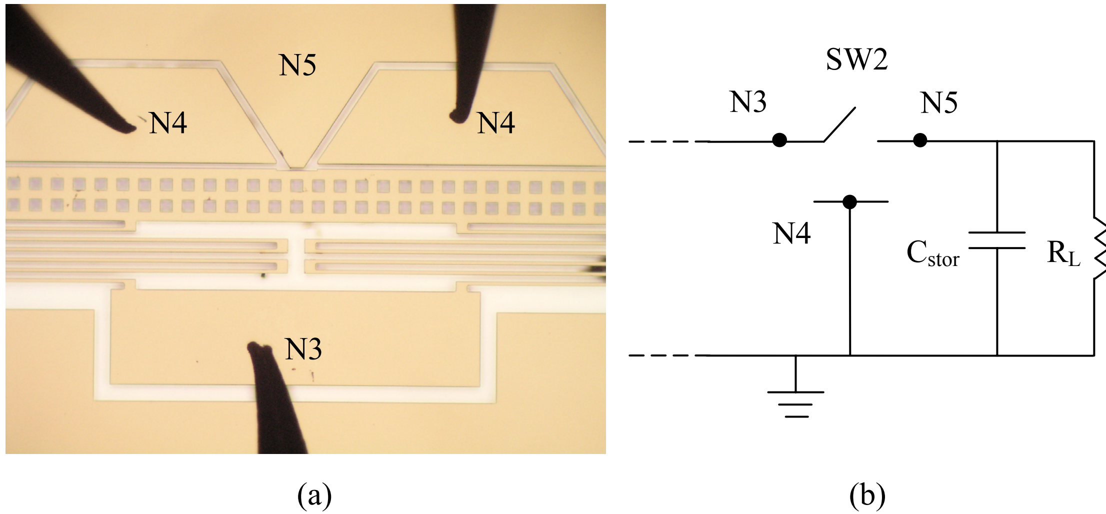


Fig. 4.20 Measurement circuit proposed by Roundy [15]

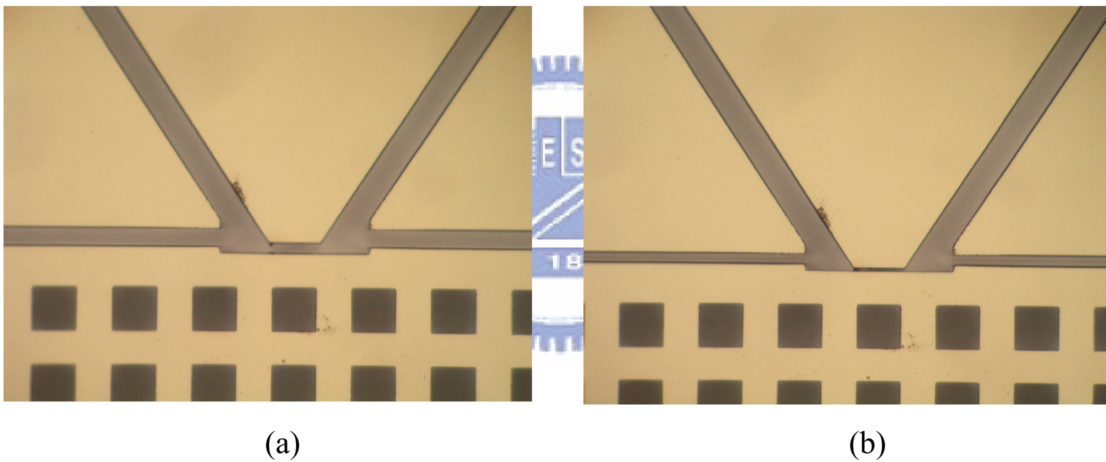
4.4 Switch measurement

The pull-in voltage of SW2 was measured by applying a voltage between nodes N3 and N4 while the displacement was observed through a microscope (Fig 4.21). The measurement shows that the pull-in voltage of SW2 is between 95 V and 100 V. A relatively tight contact can be achieved for a 120 V applied voltage. Compared to the designed value of 74 V, this slightly higher value is also a result of the spring width enlargement, as discussed in sec. 4.1.1. SW2 with and without the applied voltage are shown in Fig. 4.22.



(a) (b)

Fig. 4.21 (a) SW2 overview, (b) SW2 schematic circuit



(a) (b)

Fig. 4.22 SW2 with (a) no applied voltage, (b) 100 V applied voltage (pull-in)

4.5 Conclusion

The measurements on the capacitive energy converter are presented in this chapter. The resonant frequencies of the device before and after the external mass attachment are close to the design values. Electrical measurements of the variable capacitor showed that the parasitic capacitance is minimized to 60 pF, while the parasitic resistance still exists due to metal deposition. Capacitance change is lower than theoretical value. Circuitry was constructed to measure the AC output power of

the device. The results agree with the theoretical expectation. DC output power could not be measured due to the existence of parasitic resistance. Finally, the characteristics of SW2 were measured and compared with design values.

Chapter 5 Conclusion and Future Work

5.1 Conclusion

In this thesis, a MEMS-based capacitive vibration-to-electric energy converter with integrated mechanical switches was designed and fabricated. With a device area constraint of 1 cm^2 and an auxiliary battery supply of 3.6 V, the device was designed to generate an output power of 31 μW at an output saturation voltage of 40 V. An external mass of 4 grams was needed to adjust the resonant frequency of the device. The two charge-discharge timing switches were realized as lateral contact mechanical switches. They were timed precisely with the conversion cycle to provide maximum conversion efficiency.

The device was fabricated in an SOI wafer. Fabrication issues encountered were overcome and a modified fabrication process was proposed. Current fabrication is successful in silicon nitride preserving and partial substrate removal. All fabricated device dimensions are close to the design parameters. Parasitic resistance in the device is assumed to originate from the metal deposition, and an accurately aligned shadow mask will be utilized to eliminate this effect.

The measurements were done to verify the mechanical and electrical characteristics of the device. The resonant frequencies of the device before and after the external mass attachment agreed well with the designed values. Capacitance change was lower than expected. Parasitic capacitance was minimized due to the successful partial substrate removal. The mechanical switches could not operate correctly with the device due to parasitic resistance. Another circuit was constructed to measure the AC output power of the device. Without the external mass, the measured AC output power was 1.2 μW with a load of 5 MΩ at 1880 Hz. The

maximum output power in this condition is expected to be 16 μW. AC output power measurement of the devices with external mass attached is still in progress.

5.2 Future work

The device fabrication must be improved in two ways. First of all, a modified shadow mask must be employed to prevent parasitic resistance between electrodes. Second, the lateral contacts of the mechanical switches must be metallized as well. In oblique metal deposition as shown in Fig. 5.1, the device is fixed at a constant angle during the metal deposition. The process needs to be done twice to metallize both lateral contacts. In order to prevent the shortage between the two switch electrodes, the substrate beneath the switch gap also needs to be removed.

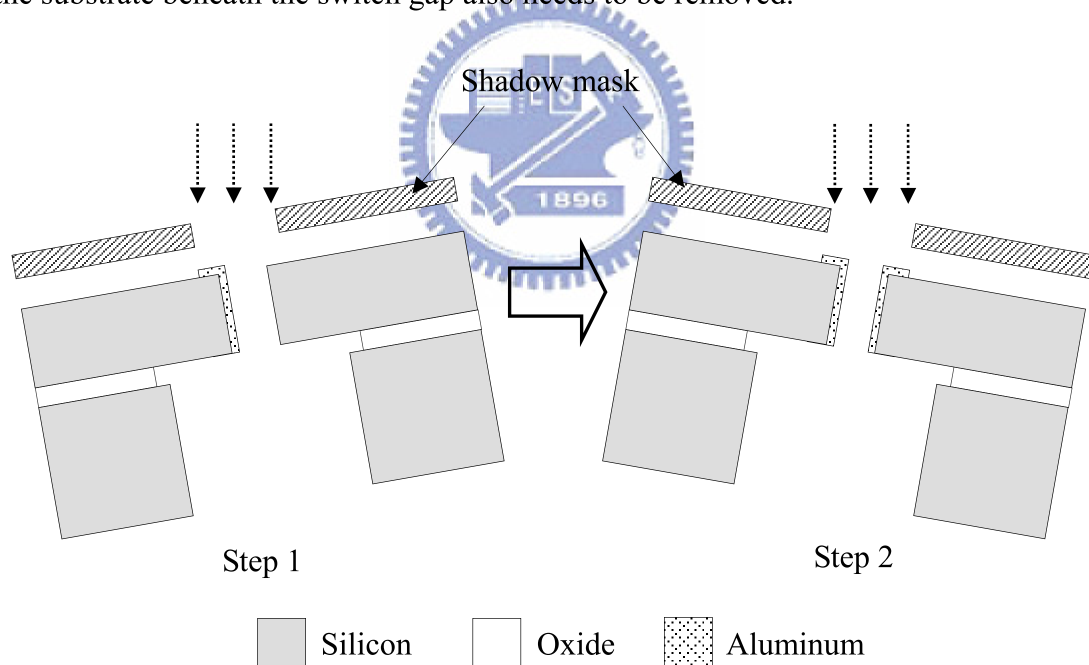


Fig. 5.1 Oblique metal deposition of the switch gaps

Vacuum packaging can be utilized to improve the device performance. The MEMS device is sealed away from environmental influence such as atmospheric pressure, temperature gradients and contamination. Vacuum packaging should

significantly improve the quality factor of the device by decreasing the squeeze film damping effect between the movable structures. Another benefit from the vacuum packaging is the slower oxidation of the metal contact surfaces of the mechanical switches. Thus, the life time of the device can be expanded.

The mechanical switches will only operate when the device reaches maximum displacement. In order to provide output power in lower displacement conditions, the AC output power circuitry should be utilized. The device design under this operation will be done in the future. The auxiliary battery supply can be replaced by a pre-charged electret. Fig. 5.2 shows the schematic of the electret-based energy converter [46]. Without the need of the auxiliary battery supply, the application potential of the capacitive energy converter is extended.

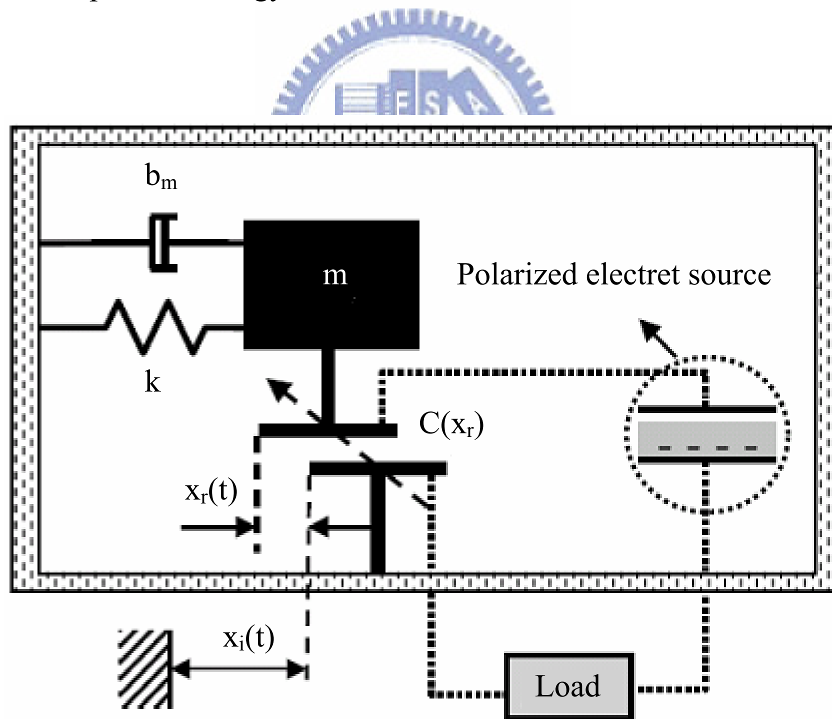


Fig. 5.2 Principle of electret-based generator [46]

References

[1] J. Rabaey, M. Ammer, J. Silva, Jr, D. Patel, and S. Roundy, "PicoRadio Supports Ad Hoc Ultra-low Power Wireless Networking," *IEEE Computer*, vol. 33, no. 7, pp. 42-48, 2000.

[2] R. Russ, "Battery Power Trade-offs, Low Voltage or Higher Capacity?" *EE Times*, July, 2002.

[3] B. Linden and T. Reddy, *Handbook of Batteries*, New York: McGraw-Hill, 2002.

[4] J. N. Harb, R. M. LaFollette, R. H. Selfridge, and L. L. Howell, "Microbatteries for Self- sustained Hybrid Micropower Supplies," *Journal of Power Sources*, vol. 104, no. 1, pp. 46-51, 2002.

[5] A. Heinzel, C. Hebling, M. Muller, M. Zedda, and C. Muller, "Fuel Cells for Low Power Applications," *Journal of Power Sources*, vol. 105, no. 2, pp. 250-255, 2002.

[6] www.nec-tokin.net/now/english/product/hypercapacitor/outline02.html, 2003.

[7] C. Lee, S. Arslan, Y. Liu, and L. Frechette, "Design of a Microfabricated Rankine Cycle Steam Turbine for Power Generation," *Proceedings of IMECE '03, ASME International Mechanical Engineering Congress & Exposition*, pp. 42082, 2003.

[8] H. Li and A. Lal, "Self-reciprocating Radioisotope Powered Cantilever," *Journal of Applied Physics*, vol. 92, no. 2, pp. 1122-1127, 2002.

[9] A. Chandrakasan and R. Amirtharajah, "Self-powered Signal Processing Using Vibration-based Power Generation," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp. 687-695, 1998.

[10] S. Roundy, P. Wright, and J. Rabaey, *Energy Scavenging for Wireless Sensor Networks with Special Focus on Vibrations,* Kliwer Academic Press, 2003.

[11] S. Kasap, *Optoelectronics and Photonics: Principles amd Practices*, Prentice-Hall, 2001.

[12] S. Lee, "Development of High-efficiency Silicon Solar Cells for Commercialization," *Journal of Korean Physical Society*, vol. 39, no.2, pp. 369-373, 2001.

[13] E. Castano, E. Revuelto, M. Martin, A. Garcia-Alonso, and F. Garcia, "Metallic Thin-film Thermoelectric Microgenerator," *Sensors and Actuators A*, vol. 60, no. 1-3, pp. 65-67, 1997.

[14] M. Stordeur and I. Stark, "Low Power Thermoelectric Generator-self-sufficient Energy Supply for Micro Systems," *Proceedings of XVI ICT '97, 16th International Conference on Thermoelectrics*, pp. 575-577, 1997.

[15] S. Roundy, D. Steingart, L. Frechette, P. Wright, and J. Rabaey, "Power sources for Wireless Sensor Networks," *Proceedings of EWSN 2004, Wireless Sensor Networks, First European Workshop,* pp. 1-17, 2004.

[16] E. Torres and G. Rincón-Mora, "Long-Lasting, Self-Sustaining, and Energy-Harvesting System-in-Package (SIP) Wireless Micro-Sensor Solution," *Proceedings of International Conference on Energy, Environment and Disasters (INCEED 2005)*, pp. 1-33, 2005.

[17] T. Starner, "Human-powered Wearable Computing," *IBM Systems Journal*, vol. 35, no. 3-4, pp. 618-629, 1996.

[18] N. Shenck and J. Paradiso, "Energy Scavenging with Shoe-mounted Piezoelectrics," *IEEE Micro*, vol. 21, no. 3, pp. 30-42, 2001.

[19] C. Williams and R. Yates, "Analysis of a Micro-electric Generator for Microsystems," *Sensor and Actuators A*, vol. 52, no. 1-3, pp. 8-11, 1996.

[20] C. Shearwood and R. Yates, "Development of an Electromagnetic Microgenerator," *Electronics Letters*, vol. 33 pp. 1883-1884, 1997.

[21] A. Chandrakasan and R. Amirtharajah, "Self-powered Signal Processing Using Vibration-based Power Generation," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp. 687-695, 1998.

[22] S. Meninger, J. Mur-Miranda., R. Amirtharajah, A. Chandrakasan, and J. Lang, "Vibration-to-electric Conversion," *Proceedings of 1999 International Symposium on Low Power Electronics and Design*, pp. 48-53*,* 1999.

[23] S. Meninger, J. Mur-Miranda., R. Amirtharajah, A. Chandrakasan, and J. Lang, "Vibration-to-electric Conversion," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 9, no. 1, pp. 64-76, 2001.

[24] G. Ottman, H. Hofmann, and G. Lesieutre, "Optimized Piezoelectric Energy Harvesting Circuit using Step-down Converter in Discontinuous Conduction Mode," *IEEE Transactions on Power Electronics*, vol. 18, no. 2, pp. 696-703, 2003.

[25] G. Ottman, H. Hofmann, A. Bhatt, and G. Lesieutre, "Adaptive Piezoelectric Energy Harvesting Circuit for Wireless Remote Power Supply," *IEEE Transactions on Power Electronics*, vol. 17, no. 5, pp. 669-76, 2002.

[26] S. Roundy, E.S. Leland, J. Baker, E. Carleton, and E. Reilly, "Improving Power Output for Vibration-based Energy Scavengers," *IEEE Pervasive Computing,* vol. 4, no. 1, pp. 28-36, 2005.

[27] B. C. Yen, J. H. Yang, "A Variable-Capacitance Vibration-to-Electric Energy Harvester," *IEEE Transactions on Circuits and Systems*, vol. 53, no. 2, pp. 288-295, 2006.

[28] J. O. Mur-Miranda, "MEMS-enabled electrostatic vibration-to-electric energy conversion," Ph.D. dissertation, Massachusetts Institute of Technology, Cambridge, USA, 2003.

[29] M. Miyazaki, H. Tanaka, G. Ono, T. Nagano, N. Ohkubo, T. Kawahara, K. Yano, "Electric-energy generation using variable-capacitive resonator for power-free LSI: efficiency analysis and fundamental experiment," *Proceedings of ISPLED'03, The International Symposium on Low Power Electronics and Design*, pp. 193-198, 2003.

[30] Y. Chiu, C. T. Kuo, Y. S. Chu, "MEMS design and fabrication of an electrostatic vibration-to-electricity energy converter," *Microsystem Technologies*, vol. 13, no. 11-12, pp. 1663-1669, 2007.

[31] J. Bates, N. Dudney, B. Neudecker, A. Ueda, and C. Evans, “Thin-film Lithium and Lithium-ion Batteries,” *Solid State Ionics, Diffusion & Reactions*, vol. 135, no. 1-4, pp. 33-45, 2000.

[32] S. Roundy, P. Wright, and K. Pister, “Micro-electrostatic vibration-to-electricity Converters,” *Proceedings of IMECE ’02, ASME International Mechanical Engineering Congress & Exposition*, pp. 17-22, 2002.

[33] J. Starr, “Squeeze-film Damping In Solid-state Accelerometers,” *IEEE Solid-State Sensor and Actuator Workshop. Digest of Technical Papers*, pp. 44-47, 1990.

[34] M. Andres, I. Harris, and G. Turner, “A Comparison of Squeeze-film Theory with Measurements on a Microstructure,” *Sensor and Actuators A*, vol. 36, no. 1, pp. 79-87, 1993.

[35] R. Legtenberg, A.W. Groeneveld, and M Elwenspoek, “Comb-drive Actuators for Large Displacements,” *Journal of Micromechanics & Microengineering*, vol. 6 no. 3, pp. 320-329, 1996.

[36] M. Judy, “Micromechanisms Using Sidewall Beams,” Ph.D. dissertation, University of California, Berkeley, USA, 1994.

[37] D. Hyman, M. Mehregany, “Contact Physics of Gold Microcontacts for MEMS Switches,” *IEEE Transactions on Components and Packaging Technology*, vol. 22, no. 3, pp. 357-364, 1999.

[38] G. S. Hwang, K. P. Giapis, “On the Origin of the Notching Effect during Etching in Uniform High Density Plasmas,” *Journal of Vacuum Science and Technology B*, vol. 15, no. 1, pp. 70-87, 1997.

[39] S. Franssila, J. Kiihamaki, J. Karttunen, “Etching Through Silicon Wafer in Inductively Coupled Plasma,” *Microsystem Technologies*, vol. 6, no. 4, pp. 141-144, 2000.

[40] J. Karttunen, S. Franssila, J. Kiihamaki, “Loading Effects in Deep Silicon Etching,” *Proceedings of SPIE 2000 International Society of Optical Engineering*, vol. 4174, pp. 90-97, 2000.

[41] S. Franssila, J. Kiihamaki, " Pattern Shape Effects and Artefacts in Deep Silicon Etching," *Journal of Vacuum Science and Technology A*, vol. 17, no. 4, pp. 2280-2285, 1999.

[42] J. Yeom, Y. Wu, M.A. Shannon, "Critical Aspect Ratio Dependence in Reactive Ion Etching of Silicon," *Proceedings of the 12th International Conference on Solid-State Sensors, Actuators and Microsystems*, vol. 2, pp. 1631-1634, 2003.

[43] J. Li, Q. X. Zhang, A. Q. Liu, W. L. Goh, J. Ahn, "Technique for Preventing Stiction and Notching Effect on Silicon-on-insulator Microstructure" *Journal of Vacuum Science & Technology B*, vol. 21, no. 6, pp. 2530-2539, 2003.

[44] Y. Chiu, J. H. Pan, "Micro Knife-edge Optical Measurement Device in a Silicon-on-insulator Substrate," *Optics Express*, vol. 15, no. 10, pp. 6367-6373, 2007.

[45] K. R. Williams, K. Gupta, M. Wasilik, "Etch Rates for Micromaching Processing-Part II," *Journal of Micro-electro-mechanical Systems*, vol. 12, no. 6, pp. 761-778, 2003.

[46] T. Sterken, P Fiorini, K Baert, R. Puers, and G. Borghs, "An Electret-based Electrostatic μ-Generator," *Proceedings of the 12th International Conference on Solid-State Sensors, Actuators and Microsystems*, vol. 2, pp. 1291-1294, 2003.

Appendix A Detailed Simulink Models

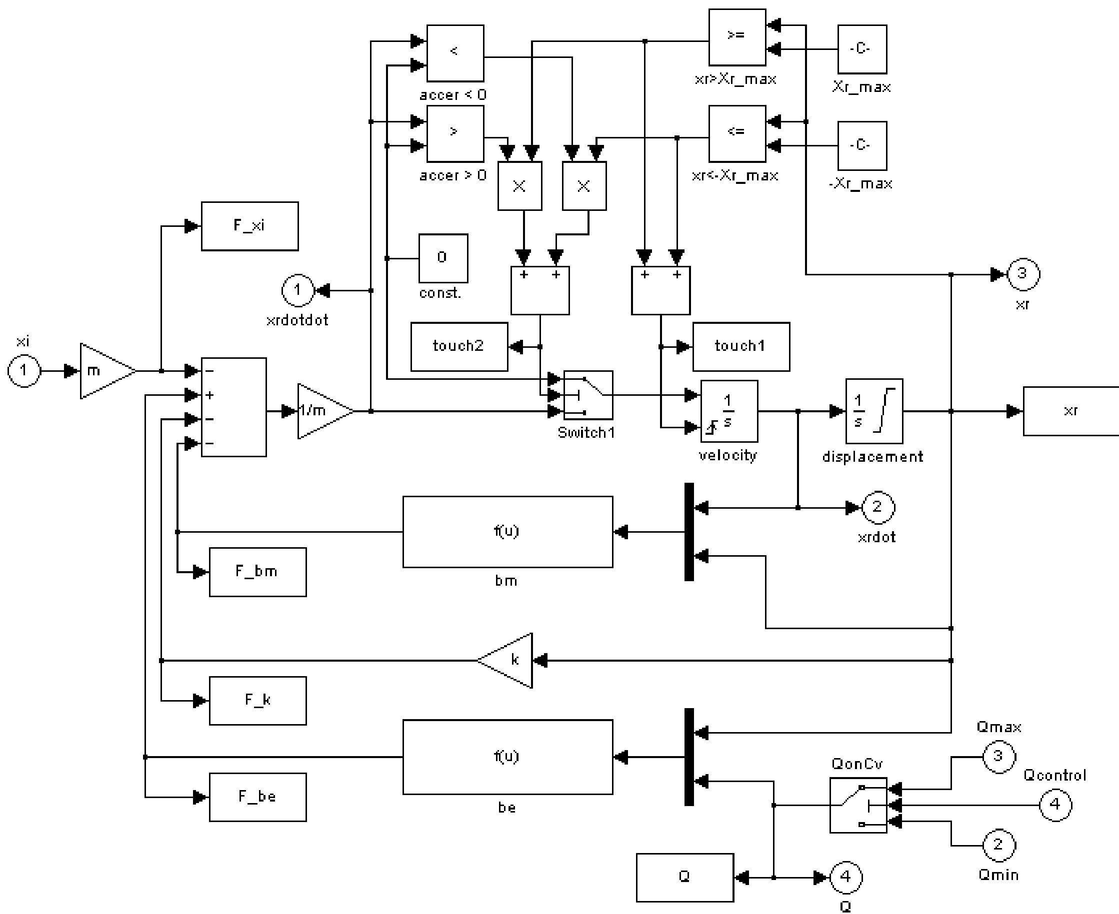


Fig. A.1 “MEMS_structure” subsystem

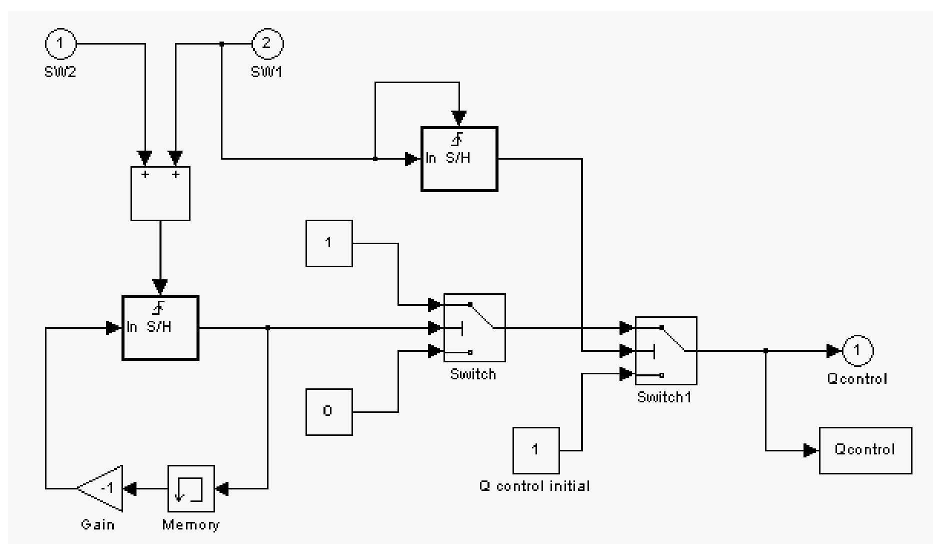


Fig. A.2 “Qcontrol” subsystem

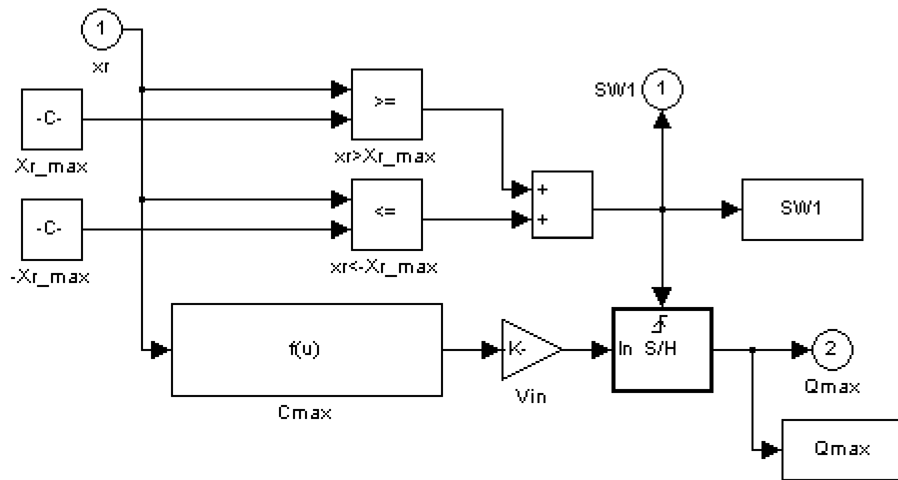


Fig. A.3 “Qmax_SW1” subsystem

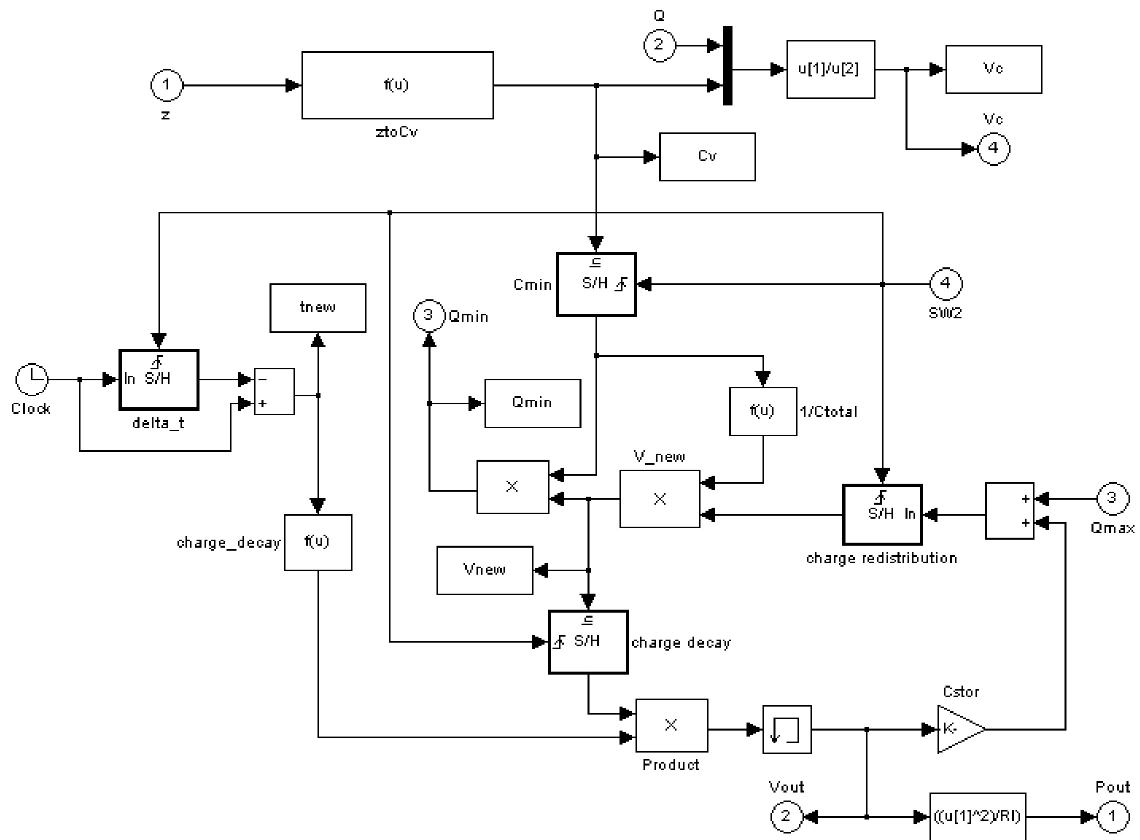


Fig. A.4 “Qmax_SW1” subsystem

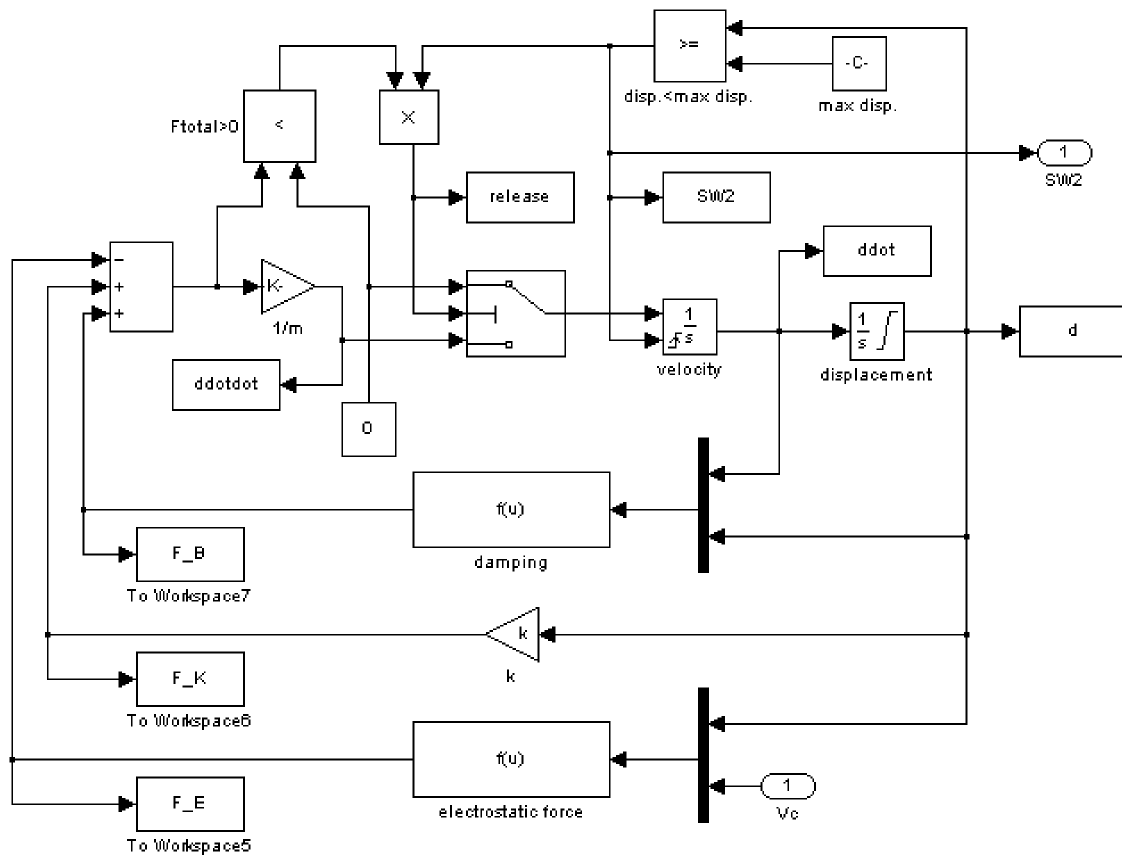


Fig. A.5 “SW2” subsystem