國 立 交 通 大 學

電機與控制工程研究所

碩 士 論 文

可程式化展頻時脈產生器

Programmable Spread Spectrum Clock Generator

研 究 生：程議賢

指導教授：蘇朝琴　教授

中 華 民 國 九 十 七 年 一 月

可程式化展頻時脈產生器

Programmable Spread Spectrum Clock Generator

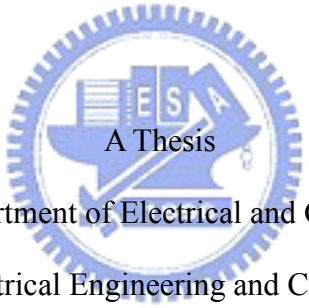
研 究 生：程議賢　　Student : YiSian Cheng

指導教授：蘇朝琴　教授　　Advisor : ChauChin Su

國 立 交 通 大 學

電機與控制工程研究所

碩士論文



A Thesis

Submitted to Department of Electrical and Control Engineering

College of Electrical Engineering and Computer Science

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master

in

Electrical and Control Engineering

January 2008

Hsinchu, Taiwan, Republic of China

中華民國九十七年一月

可程式化展頻時脈產生器

研究生：程議賢　　指導教授：蘇朝琴 教授

國立交通大學電機與控制工程研究所

摘　要

在電子系統中，伴隨著高頻時脈的需要帶來了嚴重的電磁干擾(EMI)效應。而近年來如展頻時脈技術的發展已經能有效地解決這問題。

本論文提出一個可程式化展頻時脈產生器。它是利用三角積分調變器(ΣΔ modulator)的非整數頻率合成(fractional-N)技術來設計，且達到一三角波調變的展頻功能。此外，在時脈展頻上它可以產生調變頻率從 30 khz 至 300 khz 之間變化；展頻比例從 2500 ppm 至 50000 ppm 之間變化。

可程式化展頻時脈產生器是使用台積電 0.13μm 1P8M RF 製程來實現。經模擬結果顯示非展頻情況下的時脈抖動為 5.6 ps；功率消耗為 18 毫瓦；晶片面積約為 750μm×750μm。而各個時脈展頻皆達到我們所期許的展頻行為。

關鍵字：鎖相迴路、非整數頻率合成器、展頻時脈產生器、三角積分調變器

Programmable Spread Spectrum Clock Generator

Student: Yi Sian Cheng Advisor: Chau Chin Su

Department of Electrical and Control Engineering

National Chiao Tung University

Abstract

In electronic systems, along with a high frequency of clock often comes series *electromagnetic interference* (EMI) effects. A technique, referred to as spread spectrum clock generation, is recently proposed to solve effectively.

In this thesis, we propose a programmable *spread spectrum clock generator* (SSCG). It is based on the fractional-N technique using the ΣΔ modulator. The programmable SSCG achieves the spread spectrum function with triangular waveform modulation. In addition, it generates the clock with the various modulation frequencies from 30 kHz to 300 kHz and the various spread ratios from 2500 ppm to 50000 ppm.

The programmable SSCG is implemented in TSMC 0.13 um 1P8M RF technology. The simulation results show that the non spreading clock has a peak-to-peak jitter of 5.6 ps, the power dissipation is 18 mW and the chip size is $750\mu m \times 750\mu m$. This architecture does achieve various spread spectrum profiles as expected.

Keyword: phase-locked loop, fractional-N frequency synthesizer, spread spectrum clock generator, sigma-delta modulator

致　謝

我首先要感謝我的指導教授 蘇朝琴老師，謝謝老師在學業研究上的指導，讓我這兩年收穫良多。

另外，實驗室裡的大家也是我碩士生活的支持。鴻文、丸子、仁乾、煜輝、盈杰幾位學長；小馬、小潘潘、方董、村鑫、教主、祥哥、存遠、忠傑、汝敏等等一起打拚的伙伴們；還有已畢業的學長及很多實驗室裡學弟妹們，除了對於在專業領域上的討論，還有更多的是日常生活的互相打氣，在 918 實驗室的研究生活裡，能和你們在一起，總是充滿了活力。

最後要感謝我的家人，一直以來提供了我無慮的求學環境，也謝謝我的女友美嘉，至終都能給予最大的體諒與支持，我愛你們。

感謝大家。未來我會繼續加油、繼續努力。

程議賢

2008・1・10

List of Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation

In today's electronic products, a higher operation frequency is required to obtain a greater performance and throughput. For instance, the clock frequency in *personal computers* (PCs) reaches several gigahertz. However, along with a high frequency often comes series *electromagnetic interference* (EMI) effects. Clock signals or any signals derived from the clock like data and address buses radiate electromagnetic noise and cause the larger interference for the other devices.

To solve this problem effectively, a lot of EMI reduction techniques have been developed. They are divided into two classifications. One is to enclose the EMI radiations from emission. It includes the use of the *Printed Circuit Broads* (PCB) layout techniques, metal shielding, and passive components. However, it increases area and cost overhead. The other is to reduce the EMI at the source. It adopts a dithering clock oscillation technique such as *Spread Spectrum Clock Generation* (SSCG) [1]. This approach generates a clock signal whose frequency is modulated within a certain frequency range. Similarly, the peak spectral energy of the clock signal in the spectrum is effectively reduced. Therefore, the dithering clock oscillation technique is widely used in electronic systems.

This thesis implements a programmable SSCG using fractional-N technique with sigma-delta modulator. It comprises six chapters summarized as below.

Chapter 1 introduces the motivation and the organization. It also discusses the fundamental theory of *spread spectrum clock* (SSC). That includes the basic properties, the relationship between the EMI attenuation and various parameters of SSC in the frequency domain, and the timing impacts in the clock signal. In addition, we also take a brief summary with various solutions used for the EMI reduction.

In Chapter 2, a frequency synthesizer is introduced. It includes the PLL theory and the fractional-N mechanism. Furthermore, the sigma-delta modulator concepts are also described here.

In Chapter 3, we realize the programmable spread spectrum clock generator. It controls the multiphase output of the VCO for the frequency modulation. The entire circuit consists of a conventional PLL, a programmable triangle generator, a second-order MASH 1-1 sigma-delta modulator, and a multiplexer controller.

In Chapter 4, we show the simulation results including the behavior simulation and the post-layout circuit-level simulation. Finally, the conclusion is described in Chapter 5.

1.2 Spread Spectrum Fundamentals

Figure 1.1 shows a spectral energy distribution of SSC [2]. Instead of a constant frequency, SSC modulates the clock frequency along a predetermined profile. Through spreading the clock frequency slightly, the spectral energy in the spectrum is spread out. The higher order harmonics have similar characteristics as well. The spread amounts and the attenuations are proportional to the order of the harmonic frequency.

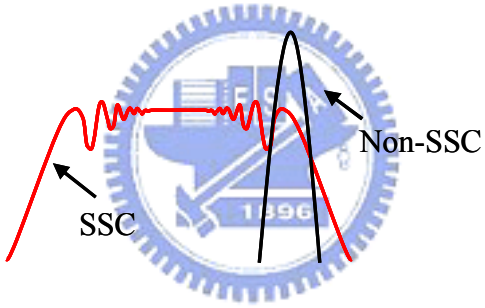


Figure 1.1 Spread fundamental frequency comparison

To comprehend the spread spectrum with the frequency modulation, we consider a carrier signal modulated by another sinusoidal signal in frequency modulation as

$$A(t) = A_c \cdot cos[2\pi f_c t + \frac{\Delta f}{f_m} sin(2\pi f_m t)]. \quad (1.1)$$

This is a cosine waveform with an amplitude of A_c, and a carrier frequency of f_c. Its instantaneous frequency is affected by a modulation frequency, f_m, and a maximum frequency deviation, Δf. They set the bandwidth over that the spectral energy is spread. The ratio between Δf and f_m is defined as the modulation index β [3] and written as

$$\beta = \frac{\Delta f}{f_m}. \tag{1.2}$$

The spectral content of a frequency-modulated signal is best described using the Bessel functions or Carson's Rule. The resulting signal includes a spectral component on the carrier frequency and an infinite number of sidebands. As shown in Figure 1.2, they are the frequency-modulated sinusoidal waveform in time domain and frequency domain.

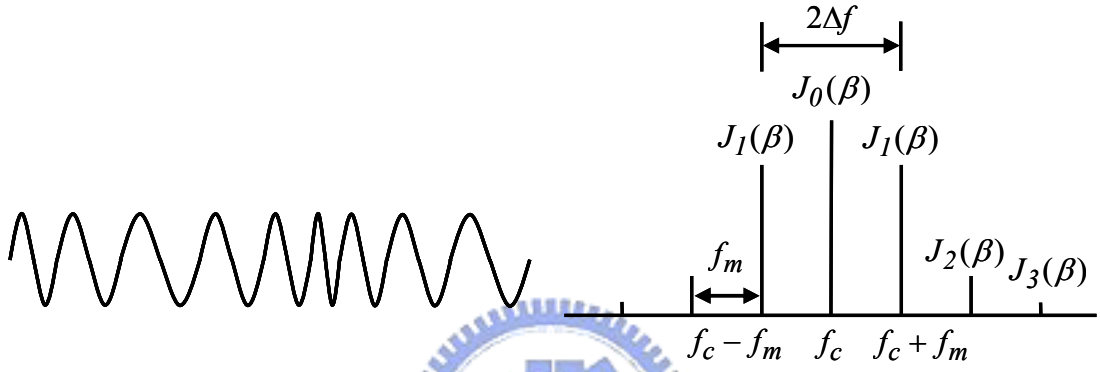
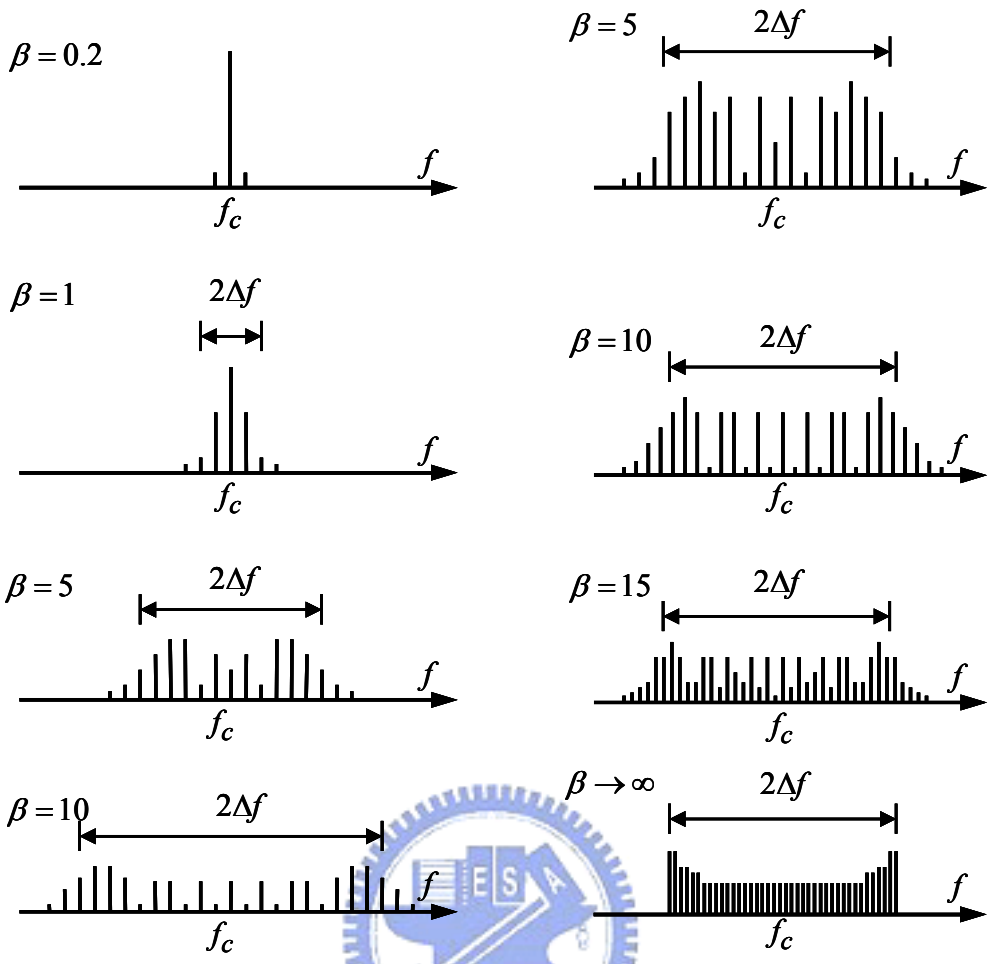


Figure 1.2 Frequency-modulated signal at (a) time domain, (b) frequency domain

The amplitudes of sidebands are proportional to the order of $J_n(\beta)$ and frequency spacing of f_m. Specifically, $J_n(\beta)$ is negligible for $n > \beta + 2$ and a finite number of sidebands is resulted. Therefore, the bandwidth of a frequency-modulated signal is obtained in (1.3). Considering a wideband frequency-modulated signal, $\beta \gg 1$, the bandwidth is approximated as $2\Delta f$.

$$BW = 2nf_m = 2(\beta + 1)f_m = 2(\Delta f + f_m) \approx 2\Delta f. \tag{1.3}$$

Figure 1.3 shows the effects of modulation index on the spectral content. β is increased by increasing Δf or decreasing f_m. As β increases, the spectral energy is distributed evenly in the band and resulting in a greater overall amplitude reduction.



(a) fixed f_m and varied Δf (b) fixed Δf and varied f_m

Figure 1.3 β effects of the frequency-modulated signal

It is also known that a frequency-modulated signal has the spectral energy redistributed in the frequency domain. The shape in the spectrum is determined by the frequency modulation profile in the time domain. There are various modulation profiles for the SSC technique, such as random pulses, sinusoidal, and triangle profiles [3], [4], [5]. Among these profiles, the triangular modulation profile has the most evenly distributed shape in the frequency domain. Thus, the greatest EMI attenuation can be achieved. It easily achieves the emission standards for a given EMI limitations.

1.3 EMI Attenuation for Spread Spectrum Clock

As the description in prior section, $J_n(\beta)$ is negligible for a significantly large n; and the bandwidth is approximated as $2\Delta f$. Considering a clock without inherent jitters, the EMI attenuation A_{dB} is estimated by [6]

$$Attenuation = A_{dB} \approx 10 \cdot log_{10}(\frac{\delta \cdot n \cdot f_o}{f_m}). \quad (1.4)$$

Where $n \cdot f_o$ is the harmonic frequency, f_m is the modulation frequency, and δ is the spread ratio. δ specifies the total amount of spreading as a relative percentage of the carrier frequency. A_{dB} is directly proportional to the spread ratio and the harmonic frequency and inversely proportional to the modulation frequency. To achieve the maximum attenuation, the spread ratio has to be increased, and the modulation frequency has to be decreased.

In addition, we consider the effect of the EMI attenuation with the random period jitter δ_{JNMC} in the spread spectrum clock. (1.5) represents a small decrement of D_{dB} between the amplitude with and without jitter [6]. D_{dB} is described by (1.6). f_{D1dB} means that the decrement is $1\,dB$ and is determined by (1.7). f_{D1dB} is directly proportional to the square root of f_o and f_m, and inversely proportional to δ_{JNMC}. Therefore, D_{dB} is decreased along with the increment of f_m. Thus, to obtain more EMI attenuation with jitter, δ_{JNMC} must be minimized.

$$A_{dB(with\ jitter)} = A_{dB(without\ jitter)} - D_{dB} \pm 1 \quad (1.5)$$

$$D_{dB} = \left(\frac{n \cdot f_o}{f_{D1dB}} \right)^{0.8} \quad (1.6)$$

$$f_{D1dB} = \sqrt{\frac{K \cdot f_0 \cdot f_m}{\delta_{JNMC}^2}}, \qquad K = 0.5 \tag{1.7}$$

As shown in Figure 1.4, the spread spectrum clock without jitter obtains the maximum EMI attenuation. Oppositely, if there is the jitter disturbance in the spread spectrum clock, the uneven shape of the spectral energy is observed in the frequency domain. The EMI attenuation caused by δ_{JNMC} is decreased.

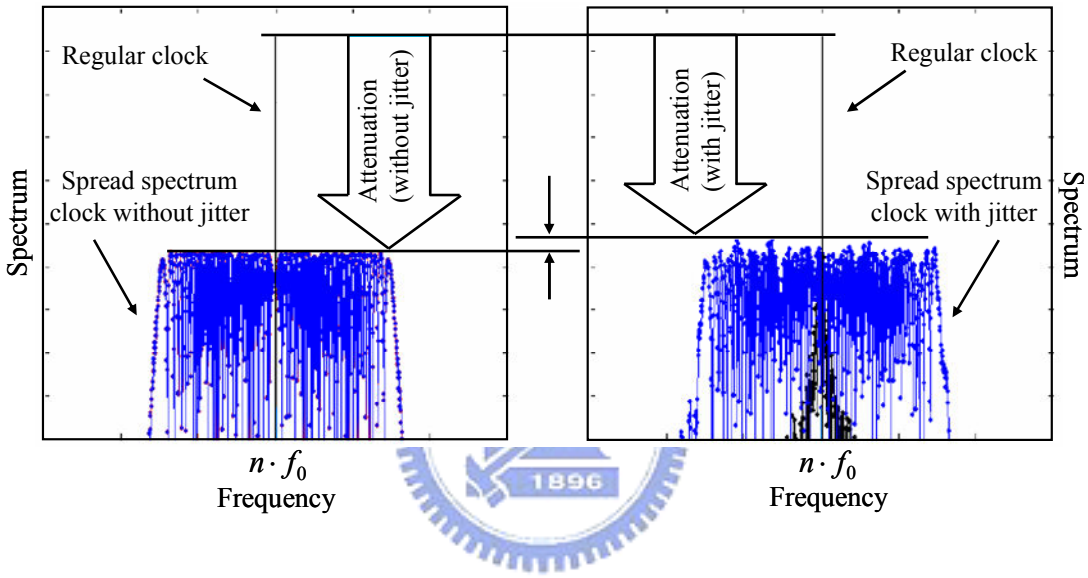


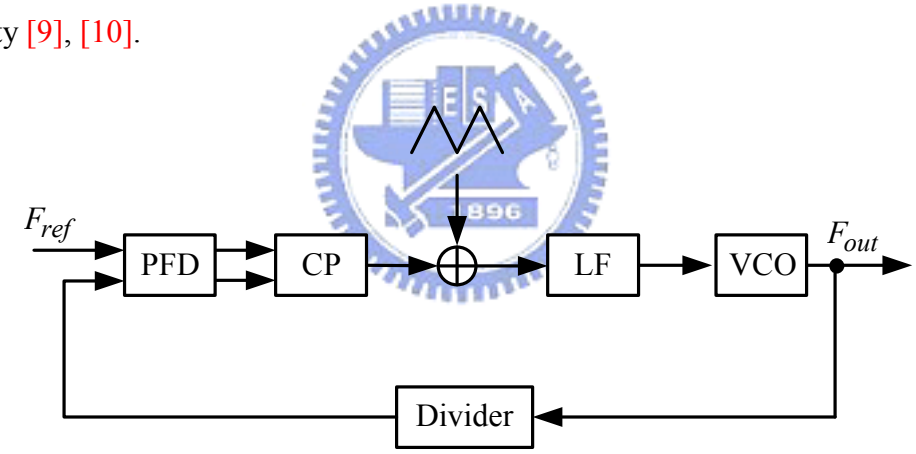
Figure 1.4 Decrement of attenuation without/with respect to jitter

1.4 Implementation of SSCG

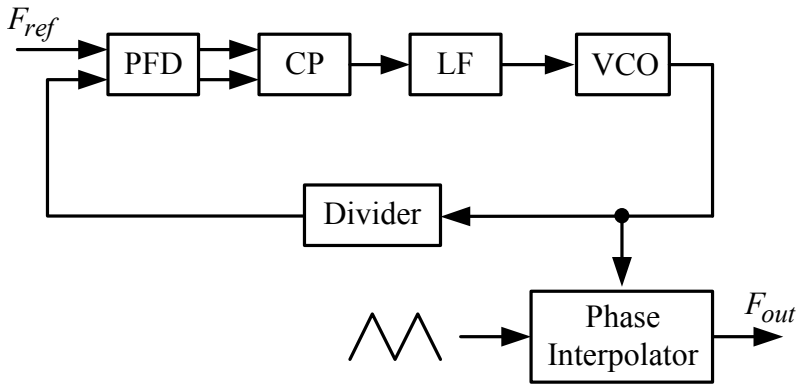
Changing the carrier frequency is a widely adopted technique to reduce the EMI radiation. There are three types of *spread spectrum clock generators* (SSCGs) for the frequency synthesizer presented in Figure 1.5 (a), (b), and (c).

The circuit shown in Figure 1.5(a) is an analog technique [7]. It is composed of two charge pump. One is to be in the primitive PLL loop, and the other is an inserted charge pump current. Through the integration of a loop filter, the additional current creates the periodical triangular modulation signal at the input node of the VCO. This

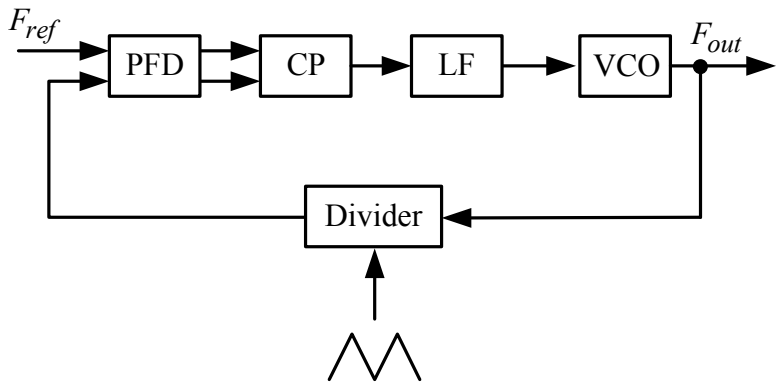
technique is usually called “VCO modulation.” It simply achieves a wider modulation bandwidth, so it is used in many applications such as the Bluetooth FM transmitters. However, the approach creates an additional jitter from modulating the VCO. One alternative to the analog modulation is phase interpolation [8]. Shown in Figure 1.5 (b), the modulation signal is applied to the coherent frequency by controlling the output phases in the phase interpolator. However, achieving a reasonable EMI reduction, such as 10 dB, is much difficult. This is because that the integrated phase interpolator does not have accurate phase linearity. Finally, Figure 1.5 (c) shows the circuit that uses the digital modulation in the PLL feedback loop. It is based on the fractional-N technique to attain to the spread spectrum clock at the output. By modulating the feedback loop of PLL, a modulated clock will be generated in the output. Compared with the other modulation technique, it provides a good triangular linearity [9], [10].



(a) VCO modulation



(b) Phase interpolation



(c) Divider modulation

Figure 1.5 Three types of SSCGs implementation

1.5 Impacts of SSC on Timing

For a spread spectrum clock, the frequency varies periodically with time, so does the period. As illustrated in Figure 1.6, the period of modulated signal varies with time and it is changed depending on the modulation profile. Because of the variation of the modulated clock period, the impacts on time are important [11].

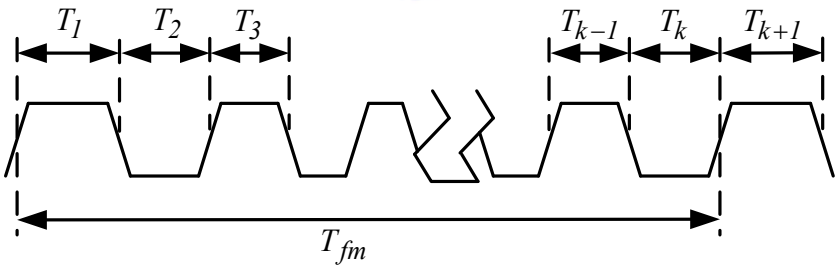


Figure 1.6 Spread spectrum clock at time domain

A. Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is the change in a clock's output transition from its corresponding position in the previous cycle. Figure 1.7 shows a graphical representation of cycle-to-cycle jitter [12].

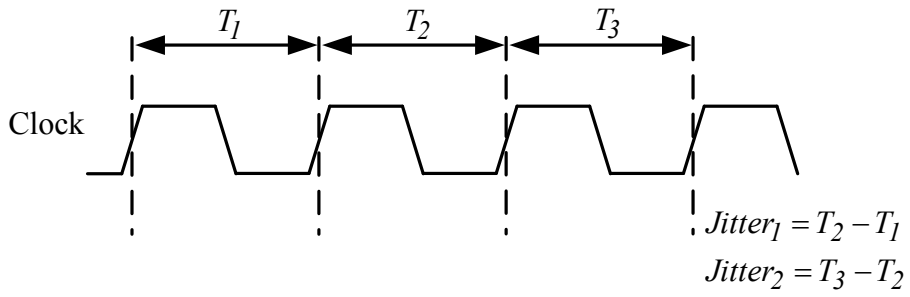


Figure 1.7 Graphical representation of cycle-to-cycle jitter

The period difference between the maximum and minimum frequencies in a SSC system is

$$\Delta T_{total} = \frac{1}{(1-\delta) f_o} - \frac{1}{f_o} \approx \frac{\delta}{f_o}. \tag{1.8}$$

The number of clock cycles that exist in the time interval that the modulated clock migrates from f_o to $(1-\delta) f_o$ can be found as

$$N = f_{avg} \cdot \frac{1}{f_m} \cdot \frac{1}{2} = \frac{f_{avg}}{2 f_m}, \tag{1.9}$$

where f_{avg} is the average frequency of the spread spectrum clock.

Because the modulation profile is symmetric, we can only consider the f_{avg} in the middle of the modulation period,

$$f_{avg} = (1 - 0.5\delta) \cdot f_o. \tag{1.10}$$

We rewrite (1.10) as

$$N = \frac{f_{avg}}{2 f_m} = (1 - 0.5\delta) \cdot \frac{f_o}{2 f_m}. \tag{1.11}$$

Combining (1.8) and (1.11), the cycle-to-cycle period change can be expressed as

$$\Delta T_{c-c} = \frac{\Delta T_{total}}{N} = \frac{2\delta}{(1 - 0.5\delta)} \cdot \frac{f_m}{f_o^2}. \tag{1.12}$$

Considering a 1.25GHz spread spectrum clock with the spread ratio of 5000ppm and the modulation frequency of 30kHz, the increase in cycle-to-cycle jitter is

$$\Delta T_{c-c} = \frac{2 \cdot 0.5\%}{(1 - 0.5 \cdot 0.5\%)} \cdot \frac{30 \cdot 10^3}{(1.25 \cdot 10^9)^2} = 1.925 \cdot 10^{-16} sec . \quad (1.13)$$

B. Long-Term Jitter

Long-term jitter is defined as the maximum change in a clock's output transition from its ideal position. Figure 1.8 shows the graphical representation of the long-term jitter [12].

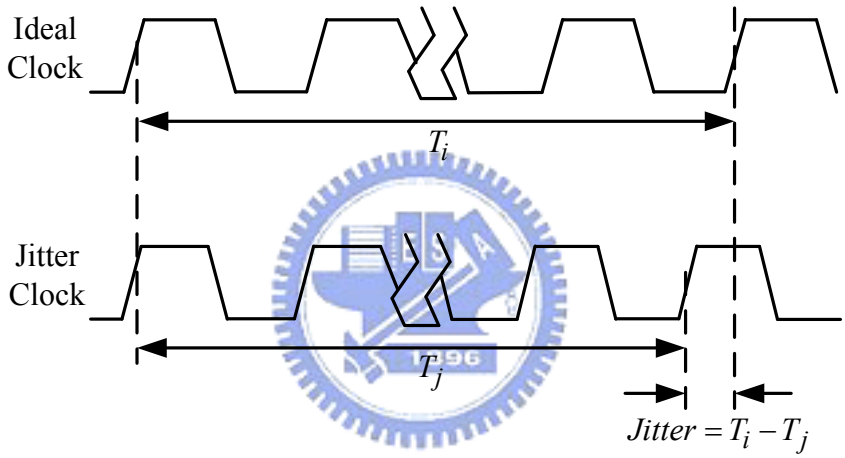


Figure 1.8 Graphical representation of long-term jitter

Because there exists the spreading frequency modulation, there are many clock cycles passed by the reference period. The long-term jitter of the spread spectrum modulated signal is tremendous.

1.6 Considerations for Using Spread Spectrum Clocking

SSCG is utilized in many systems to reduce the radiated emissions. Theses systems are composed of microprocessors, ASICs, RAM, and other logic circuits. They are usually designed to complete some operations within one clock cycle. Because of the throughput requirement, a general method is to increase the internal or core frequency through the clock multiplication. It is often implemented by using frequency multiplying PLL. In addition, it is necessary to minimize the timing difference between the system clock and the I/O signals in the system. This is because that an excessive delay in the operation significantly reduces a system's throughput.

One of the SSCG concerns is the clock skew [13]. If the input signal is a SSC clock and its frequency migrates from f_o to $(1-\delta)f_o$, the PLL does not identically track the input clock and instantaneously update the output clock. The accumulation from the period difference results in a significant amount of the phase error. This phase error is defined as the PLL tracking skew between the input clock and its output clock. The tracking skew decreases the setup and hold margins in the corresponding interfaces. It affects the device timing margins in reading or writing data.

In General, SSC has triangle modulation profiles and contains higher-order harmonic contents than the carrier frequency. The maximum frequency change happens when the triangle profile changes the polarity of the slew rate at the corners. Thus, in order to accurately track the SSC signal in the PLL, the closed-loop bandwidth must be large enough to pass the sufficient number of high-order harmonic contents. This closed-loop bandwidth is determined by the PLL transfer function. With a second-order loop filter, this transfer function is defined as $H(s) = \theta_{out}(s)/\theta_{in}(s)$ and written as

$$H(s)=\frac{\theta_{out}(s)}{\theta_{in}(s)}=\frac{I_{CP}\cdot K_{VCO}}{N_{FB}\cdot C_1}\cdot\frac{s+\dfrac{1}{R\cdot C_2}}{s^3+s^2\cdot\dfrac{C_1+C_2}{R\cdot C_1\cdot C_2}+s\cdot\dfrac{I_{CP}\cdot K_{VCO}}{N\cdot C_1}+\dfrac{I_{CP}\cdot K_{VCO}}{R\cdot C_1\cdot C_2}}, \tag{1.15}$$

where I_{CP} is the charge pump current, K_{VCO} is the VCO's gain, N_{FB} is the divider division ratio, and C_1, C_2, and R are the values of the loop filter components.

However, a larger bandwidth results in diminishing the PLL stability and raises susceptibility to noise. Therefore, the bandwidth considerations of the downstream PLL must be made to accommodate the spread spectrum clock to minimize the timing problems in the system.

Chapter 2

Fractional-N Phase-Locked Loop with ΣΔ Modulator

In traditional PLL based on frequency synthesizers, division ratios in the feedback path are restricted to the integers. When a finer frequency resolution is required, the lower reference frequency results in narrow bandwidth and low switching speed. The larger division ratio also causes larger noise amplification from the reference to the synthesizer output. Recently, fractional-N synthesis techniques are widely adopted in the wireless applications. This technique overcomes the shortcomings of traditional PLL frequency synthesizers. *Sigma-delta modulator* (ΣΔ modulator) is the most suitable scheme for the fractional-N synthesis technique. In this chapter, we will discuss the fundamental theory of PLLs and the fractional-N mechanism.

2.1 Phase-Locked Loop Fundamentals

Today's *phase-locked loops* (PLL) are preferred choices for generating stable, low-noise, and particularly tunable oscillation frequency in the communications. A basic PLL architecture we discuss is shown in Figure 2.1. It consists of a *Phase Frequency Detector* (PFD), a *Charge Pump* (CP), a *loop Filter* (LF), a *Voltage Controlled Oscillator* (VCO), and a divider.

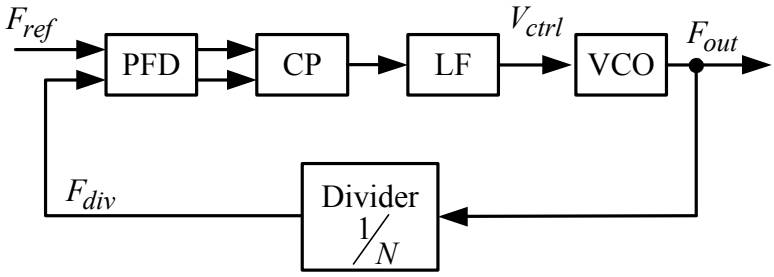


Figure 2.1 Block diagram of a typical PLL

After a locking process, all the signals in the loop finally reach a steady state and the PLL operates as follows. The internal feedback signal F_{div} from the divider is compared to the external reference signal F_{ref} by PFD. PFD serves as an error amplifier in the loop and attempts to reduce the input phase difference. It generates two messages to CP, Lead/Lag message and the phase difference between F_{ref} and F_{div}. CP charges and discharges the loop filter according to the input phase difference and produces a control voltage V_{ctrl} to vary VCO output frequency. VCO oscillates at a frequency that is equal to the N times the internal feedback frequency F_{div}. Finally, F_{div} is adjusted according to the synchronous input signal. F_{out} is $N \times F_{ref}$ in the steady state.

Figure 2.2 displays a block diagram of the linear model. We use mathematical analysis to determine the parameters [14]. It also provides the overall s-domain transfer function. PFD and CP have a gain of K_{PFD}. It is the charge pump current divided by 2π. LF transfer function in the s-domain is represented as $Z_{LF}(s)$. It is

usually designed as a second-order or a third-order filter. K_{VCO} is the VCO's gain for the phase expression. Since integration is a linear operation on the VCO's output frequency, the output phase is also divided by a factor of N in the frequency divider.

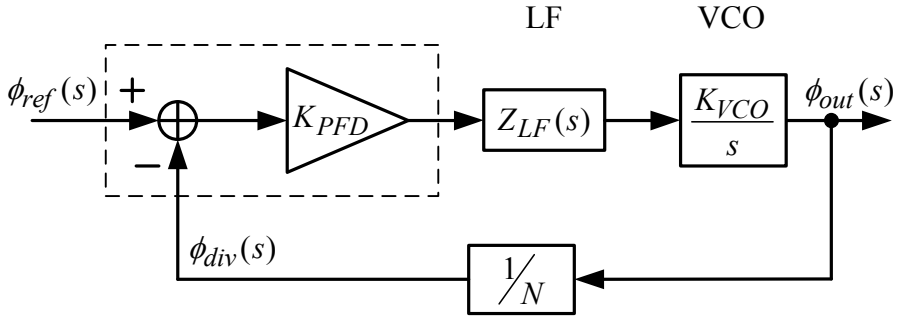


Figure 2.2 Block diagram of a PLL linear model

The forward gain is therefore derived as

$$G(s)=\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{s}. \tag{2.1}$$

The feedback gain is

$$H(s)=\frac{1}{N}. \tag{2.2}$$

Then, the close loop transfer function is expressed as

$$\frac{\phi_{out}(s)}{\phi_{ref}(s)}=\frac{G(s)}{1+G(s)H(s)}=\frac{\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{s}}{1+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{s\cdot N}}. \tag{2.3}$$

The order of the PLL transfer function is determined by the loop filter. We consider a linear model charge-pump PLL and the loop filter transfer function as

$$Z_{LF}(s)=R+\frac{1}{sC}. \tag{2.4}$$

We rewrite the close loop transfer function as

$$T(s)=\frac{\phi_{out}(s)}{\phi_{ref}(s)}=\frac{\frac{K_{PFD}K_{VCO}}{C}(sRC+1)}{s^2+\frac{K_{PFD}K_{VCO}}{N\cdot C}RC\cdot s+\frac{K_{PFD}K_{VCO}}{NC}}=\frac{\frac{K_{PFD}K_{VCO}}{C}(sRC+1)}{s^2+2\zeta\omega_n\cdot s+\omega_n^2} \quad (2.5)$$

The natural frequency ω_n and damping factor ζ of the system can be derived as

$$\omega_n=\sqrt{\frac{K_{PFD}K_{VCO}}{N\cdot C}} \quad , \quad \zeta=\frac{RC}{2}\omega_n . \quad (2.6)$$

2.2 Types of Noise Sources in PLL

By the above mathematical analysis, we now will discuss noise effects and its influence in PLL. Shown in Figure 2.3 is the PLL model with three noise sources being added. $V_{n1}(s)$ is associated with PFD and CP. It is also known as the input reference noise. $V_{n2}(s)$ is introduced by the loop filter. $V_{n3}(s)$ is the phase noise generated by the VCO.

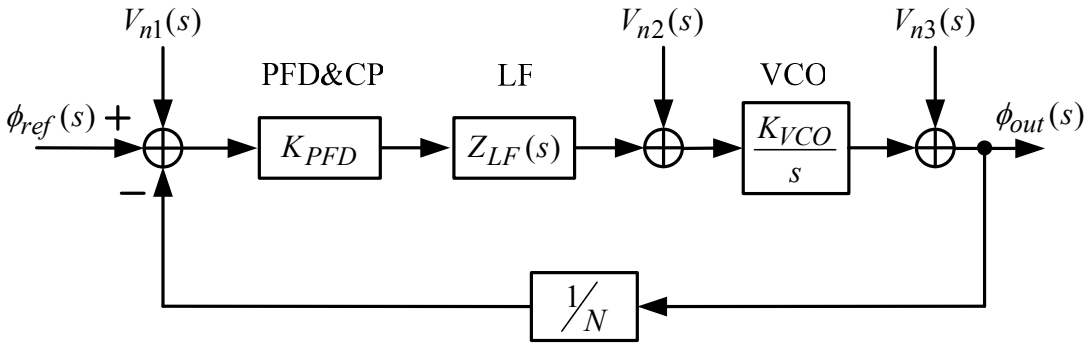


Figure 2.3 Linear model of PLL with the noise sources

The equations representing the noise transfer function of $V_{n1}(s)$, $V_{n2}(s)$, $V_{n3}(s)$ are

$$\frac{\phi_{out}(s)}{V_{n1}(s)} = \frac{\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{s}}{1+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{s\cdot N}} = \frac{K_{PFD}Z_{LF}(s)K_{VCO}}{s+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{N}}, \tag{2.7}$$

$$\frac{\phi_{out}(s)}{V_{n2}(s)} = \frac{\frac{K_{VCO}}{s}}{1+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{s\cdot N}} = \frac{K_{VCO}}{s+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{N}}, \tag{2.8}$$

$$\frac{\phi_{out}(s)}{V_{n1}(s)} = \frac{1}{1+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{s\cdot N}} = \frac{s}{s+\frac{K_{PFD}Z_{LF}(s)K_{VCO}}{N}}. \tag{2.9}$$

First, considering the input reference noise, the noise transfer function has as a low-pass property. If the input reference noise varies rapidly, the output phase will not fully track the variations. In other words, only the slowly varying input reference noise can propagate to the output. Second, the noise effect of $V_{n2}(s)$ has the same property as $V_{n1}(s)$. Finally, VCO tends to accumulate its noise fluctuations and passes them to the output. Figure 2.4 shows the summary of the noise responses. In order to receive suppressed noise fluctuations in the output, a moderate loop bandwidth should be chosen. This is because that there exists a trade-off between the VCO's noise and the input reference noise [15].

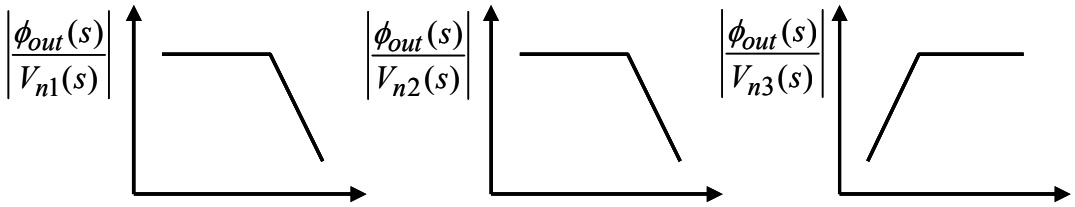


Figure 2.4 Frequency response of noise sources

2.3 Fractional-N Frequency Synthesis

The fractional-N frequency synthesis technique has an advantage of synthesizing non-integer multiplications between the output frequency and the reference signal. It improves the phase noise and the switching speed. Using this technique has no limited loop bandwidth as integer frequency synthesizers.

In general, the fractional-N PLL is classified into two types. One is based on the integer divider. It achieves fractional-N synthesis through averaging the divider division ratio in a long time. By switching the division ratio among two or more values, the divider divides by a non-integer number. The other is using the ΣΔ modulation concept [16]. It results in a beneficial noise shaping of the phase noise introduced by the fractional-N division. Thus, the technique provides the low phase noise and the reduced spurious impacts compared to the first type.

Figure 2.5 shows a dual-modulus prescaler introduced in the PLL [17]. It divides VCO's output frequency by either N or $N+1$. Together, two synchronous counters are combined to construct a variable frequency divider.

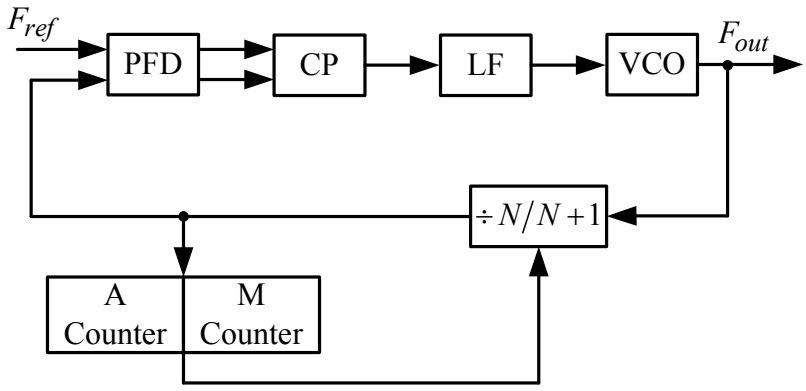


Figure 2.5 PLL with the dual-modulus prescaler

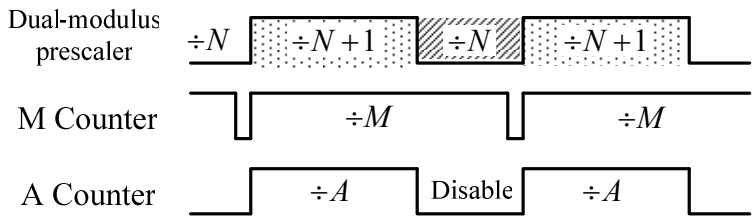


Figure 2.6 Dual-modulus prescaler operation mechanism

Figure 2.6 is a timing diagram of a dual-modulus prescaler. Initially, both A counter and M counter start at the same time. PLL tracks the frequency and locks at a division of $N+1$ until A counter is ended. Then, A counter is disabled and the divider jumps to N before the M counter is overflow. The process is repeated periodically. Finally, the average division ratio is obtained as

$$N_{avg} = \frac{(N+1)\cdot A + N\cdot(M-A)}{M} = N + \frac{A}{M}. \tag{2.10}$$

Therefore, using the PLL frequency synthesizer with the dual-modulus prescaler can obtain an average division ratio between the two dividers. However, there is a serious problem in this structure. It results in spurious frequencies in the output spectrum. Shown in Figure 2.7, a periodically sawtooth phase error is produced in PFD. The phase error from the difference of the input signals accumulates and goes back to zero. It presents a periodic behavior and generates the fractional spurs in the output spectrum.

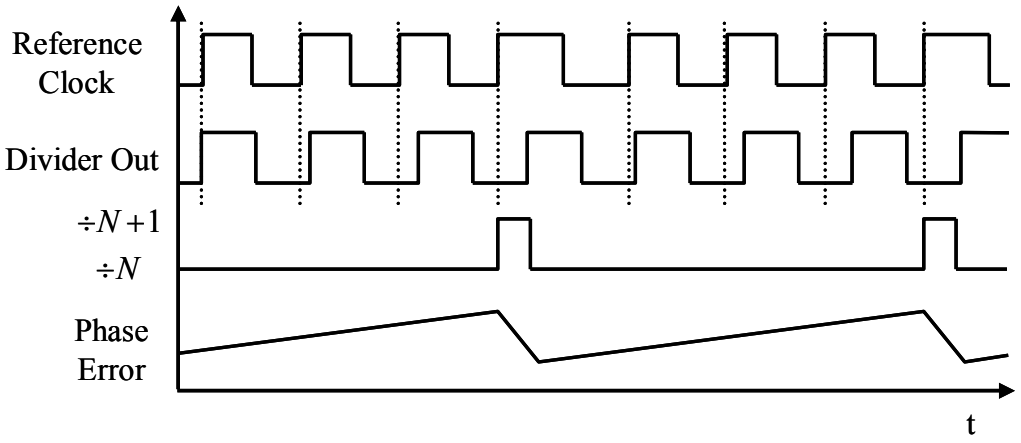


Figure 2.7 Sawtooth phase error

Figure 2.8 shows the resulting fractional spur which are typically only 20 or 30 dB below center frequency. It seriously degrades the signal purity in the output spectrum [18]. Thus, how to constrain the fractional spur is a serious subject. For this, the *sigma-delta modulator* (ΣΔ modulator) technique can overcome this problem. It is most suitable for the fractional-N frequency synthesis.

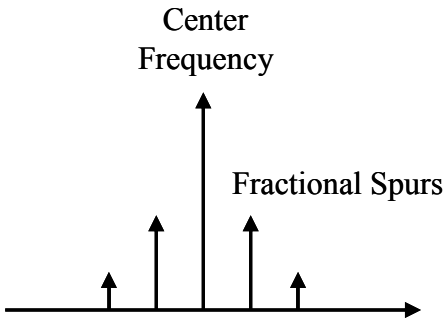


Figure 2.8 Spurious noise in the PLL output spectrum

2.4 Sigma-Delta Modulator

A ΣΔ modulator technique is widely used for ADC and DAC application [19]. This technique pushes the quantization noise to a higher frequency, suppresses the in-band quantization noise, and increases the *signal to noise ratio* (SNR).

As shown in Figure 2.9, a ΣΔ modulator has an integrator at the input and a differentiator behind a quantizer. In conventional ΣΔ modulator application, the output is followed by a low-pass filter in order to remove the high-frequency quantization noise. Because there exists a low-pass characteristic in the PLL, the out-of-band quantization noise is suppressed by higher order poles.

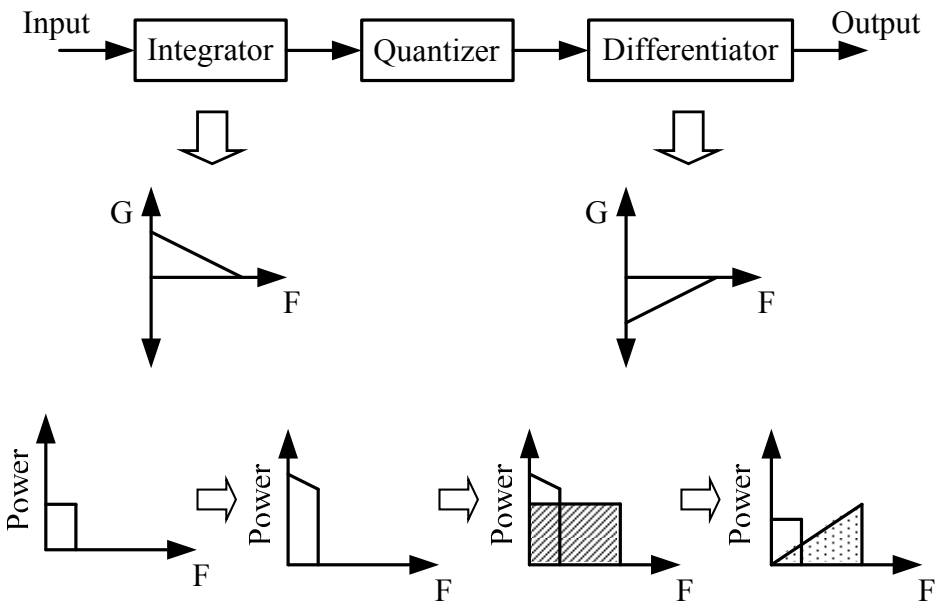


Figure 2.9 Fundamental theory of ΣΔ modulator

A 1-order ΣΔ modulator is shown in Figure 2.10. Both the integrator and the differentiator are first-order and complementary. However, the 1-order ΣΔ modulator encounters an overflow problem due to the high dc gain of the integrator. In order to solve the problem, the subtraction section in the differentiator is moved to the front of the integrator as a negative feedback system. But the transfer function is not changed. Figure 2.11 shows the improved 1-order ΣΔ modulator.

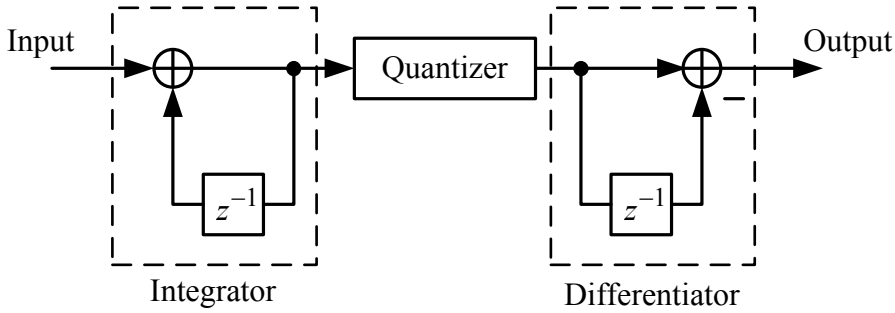


Figure 2.10 Original structure of first-order ΣΔ modulator

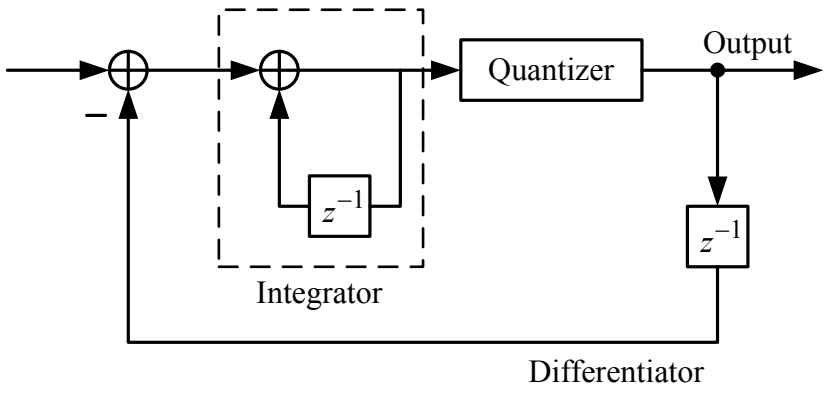
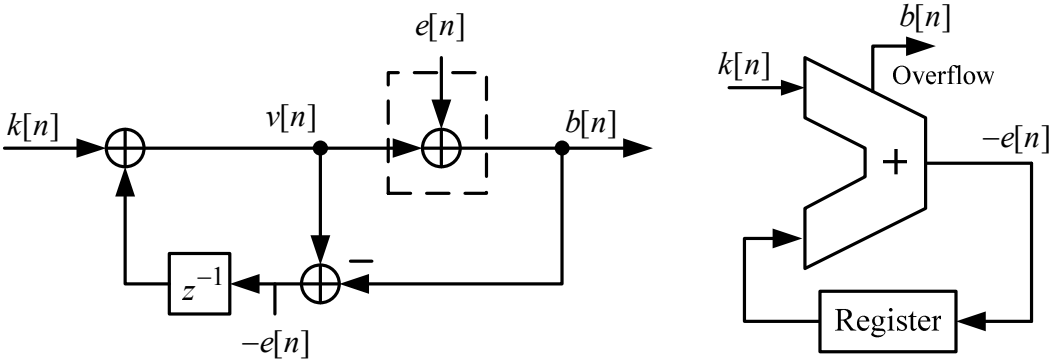


Figure 2.11 Modified structure of first-order ΣΔ modulator

A first-order ΣΔ modulator in its digital implementation is illustrated in Figure 2.12 (a). The equivalent circuit diagram is shown in Figure 2.12 (b), where $e[n]$ is the quantization noise added at the quantizer. The input signal $k[n]$ is integrated to produces the signal $v[n]$. A 1-bit quantization process is accomplished by taking the most significant bit (MSB) of $v[n]$. It is represented as the accumulator overflow. Besides the MSB of $v[n]$, the residue signal is the negative quantization error. It is then stored in the register. Therefore, the modulator with error feedback can be fully implemented with digital circuit.



(a) digital implementation (b) equivalent block diagram

Figure 2.12 First-order SDM implementation

In z-domain [20], the transfer function is written as

$$B(z) = K(z) + (1 - z^{-1})E(z), \tag{2.11}$$

where the $(1 - z^{-1})$ term is a zero in the origin referred as the *noise transfer function* (NTF). It is known that an additional zero in the origin in the transfer function produces a slope shaper by $20\,\mathrm{dB/dec}$. More zeros in the origin push the quantization noise to a higher frequency. The higher-order NTF is written as $(1 - z^{-1})^m$, where m is the order of the modulator. In addition, from (2.11), the *power spectral density* (PSD) is rewritten as

$$\begin{aligned} S_B(f) &= S_K(f) + S_f(f) \\ &= S_K(f) + \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 \cdot S_E(f) \end{aligned}, \tag{2.12}$$

where f_s is the sampling frequency.

Assume that 1-bit quantizer has an uniform quantization error and the power is spread over a bandwidth of f_s. Consequently, the PSD of the quantization error is $1/(12 f_s)$. Thus, the second term is also represented by a general formula and written as

$$S_f(f) = \frac{1}{12 \cdot f_s} \cdot \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^{2m}, \tag{2.13}$$

2.5 MASH 1-1 Sigma-Delta Modulator

For today's fractional-N frequency synthesizers with the ΣΔ modulators, it is implemented by using the *multi-stage-noise-shaping* (MASH) architecture. This is because that the MASH architecture is unconditionally stable and easy for the digital implementation. In general, the second-order and the third-order ΣΔ modulator are usually adopted. Fourth-order or even higher order ΣΔ modulator are rarely adopted

oppositely. This is because the output phase noise is difficult to suppress at high frequency by a finite order of the loop filter.

As shown in Figure 2.13, a second-order MASH 1-1 modulator is formed by cascading two first-order ΣΔ modulators [21], [22]. In order to reduce the quantization noise, the quantization error from the first stage is fed into the second stage. Then, through the error cancellation mechanism, the quantization noise from the first stage is cancelled in the output. The quantization noise from the second stage is remained and shaped to a high frequency.

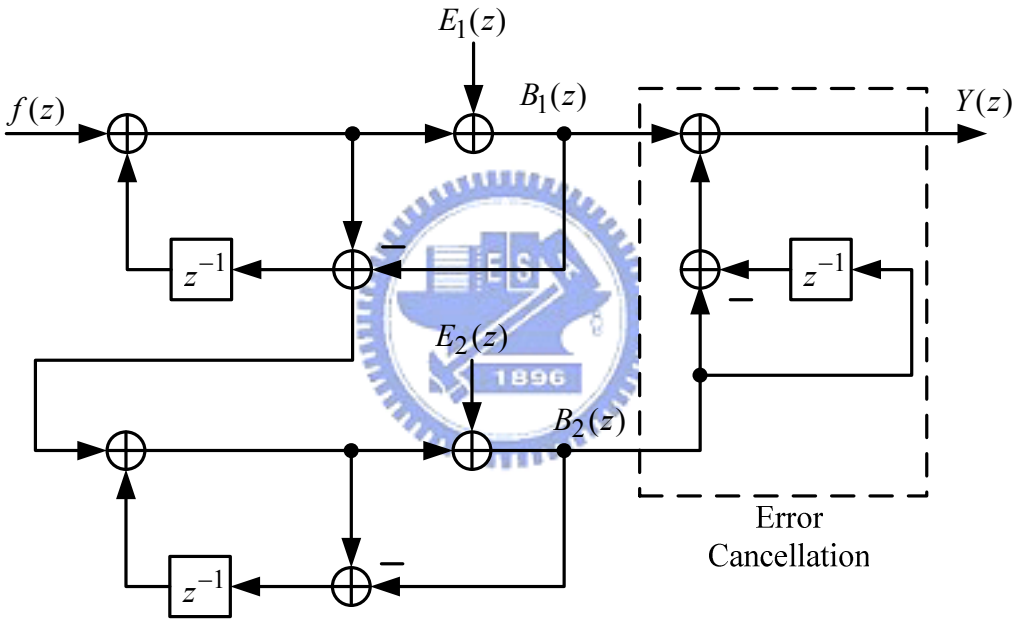


Figure 2.13 Second-order MASH 1-1 ΣΔ modulator

The equations of the individual first-order modulator are written as

$$\begin{aligned} B_1(z) &= f(z) + (1 - z^{-1}) \cdot E_1(z) \\ B_2(z) &= -E_1(z) + (1 - z^{-1}) \cdot E_2(z) \end{aligned}, \tag{2.14}$$

where $f(z)$ is the fractional number. $E_1(z)$ and $E_2(z)$ represent the quantization noise in two stages respectively. Therefore, the output of the ΣΔ modulator is

$$\begin{aligned} Y(z) &= f(z) + (1-z^{-1}) \cdot E_1(z) + \left[-E_1(z) + (1-z^{-1}) \cdot E_2(z) \right] \cdot (1-z^{-1}) \\ &= f(z) + (1-z^{-1})^2 \cdot E_2(z) \end{aligned} . \quad (2.15)$$

Considering a PLL with a second-order MASH 1-1 ΣΔ modulator, the inherent division ratio N_{div} of the divider is

$$N_{div} = Nf(z) + (1-z^{-1})^2 \cdot E_2(z), \quad (2.16)$$

where the first term is the wanted division ratio determined by the ΣΔ modulator.

Figure 2.14 shows the digital circuit implementation. The total divider division ratio N_{div} is summed with the nominal number N and the ΣΔ modulator output $Y(z)$.

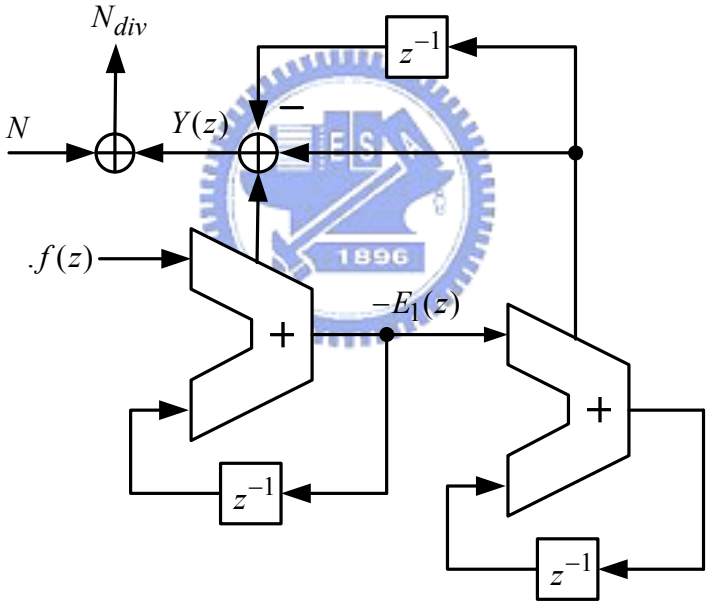


Figure 2.14 MASH 1-1 ΣΔ modulator implementation

In order to determine the effect of the ΣΔ quantization noise in the out-of-band, we consider the PLL whose divider is controlled by the ΣΔ modulator. From (2.16), we derive the PLL output frequency $F_{out}(z)$ as

$$F_{out}(z) = Nf(z) \cdot f_{ref} + \left[(1-z^{-1})^2 \cdot E_2(z) \cdot f_{ref} \right] \cdot T(z), \quad (2.17)$$

where the second term consists of the frequency fluctuations due to the ΣΔ quantization noise, which crosses over the closed loop transfer function of PLL, T(z).

For $E_2(z)$ being $1/(12f_s)$, the PSD of the frequency fluctuations is calculated as

$$\begin{aligned} S_{f_E}(z) &= \left|(1-z^{-1})^2 \cdot f_{ref}\right|^2 \cdot \frac{1}{12f_s} \\ &= \left|(1-z^{-1})\right|^4 \cdot \frac{f_s}{12} \end{aligned} . \tag{2.18}$$

To receive the phase fluctuations, we convert the frequency fluctuations to the phase fluctuations.

$$\phi(t) = \int f_E dt . \tag{2.19}$$

Employing a simple rectangular integration to represent $\int dt$ in the z-domain,

$$\Phi(z) = \frac{2\pi}{f_{ref}(1-z^{-1})} F_E(z) . \tag{2.20}$$

With (2.20), we obtain

$$S_\Phi(z) = \frac{(2\pi)^2}{12f_{ref}} \cdot \left|1-z^{-1}\right|^2 \text{ rad}^2/\text{Hz} . \tag{2.21}$$

Generally,

$$S_E(f) = \frac{(2\pi)^2}{12f_{ref}} \left[2sin\left(\frac{\pi f}{f_{ref}}\right)\right]^{2(m-1)} \text{ rad}^2/\text{Hz} . \tag{2.22}$$

From (2.22), it reflects that the m th-order ΣΔ modulator provides a $20\cdot(m-1)\,\text{dB/dec}$ slope characteristic. It shapes the noise to high frequency. Such as the MASH 1-1 ΣΔ modulator also provides the high-frequency noise shape by $20\,\text{dB/dec}$. As shown in Figure 2.15, the phase noise generated by the ΣΔ quantization noise is plotted with second-order, third-order, and fourth-order structures respectively. Their shapes are clearly observed there.

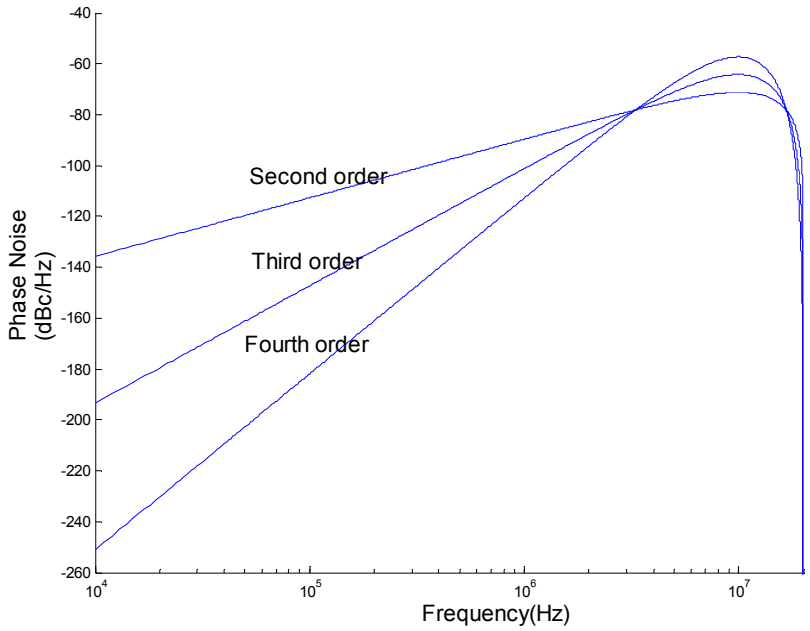


Figure 2.15 Quantization noise of second to fourth-order ΣΔ modulator

2.6 Design Consideration for PLL Loop Bandwidth

As the prior description, the quantization noise shaped by the ΣΔ modulator is concentrated at high frequency. Here, we discuss a third-order PLL with the MASH 1-1 ΣΔ modulator. Due to the low-pass characteristics in a PLL, there exists an in-band phase noise with a positive $20\,\mathrm{dB/dec}$ slope and an out-of-band phase noise with a negative $40\,\mathrm{dB/dec}$ slope. So it is necessary to choose the narrow loop bandwidth in order to reduce the output phase noise. According to [23], the dynamic range of the L th-order ΣΔ modulator must be higher than the dynamic range of the synthesizer.

$$\frac{3}{2}\cdot\frac{2L+1}{\pi^{2L}}\cdot\left(\frac{f_{PFD}}{2f_c}\right)^{2L+1} > \frac{8}{\theta_{rms}^2}\left(\frac{f_{PFD}}{2f_c}\right)^2, \tag{2.23}$$

where f_c and θ_{rms} are the noise bandwidth and the in-band phase error of the frequency synthesizer respectively. So the approximated upper bound of the loop bandwidth is obtained as

$$f_c < \left[\frac{3}{8} \cdot \theta_{rms}^2 \cdot \frac{2L+1}{(2\pi)^{2L}} \right]^{(1/2L-1)} \cdot f_{PFD}, \tag{2.24}$$

where θ_{rms} is the in-band phase error.

In addition, considering the SSCG based on the fractional-N technique by using the ΣΔ modulator, the PLL loop bandwidth must be wide enough. This is because that there are some distortions on the triangle modulation profile under such a narrow loop bandwidth. Therefore, to make sure that the triangle modulation profile can be preserved, the loop bandwidth must be at least one order of magnitude higher than the modulation frequency [24]. According to this rule, we can obtain the desired loop bandwidth.

Chapter 3

Programmable Spread Spectrum Clock Generator Implementation

3.1 Architecture of the Proposed Programmable SSCG

Figure 3.1 shows the block diagram of the proposed programmable SSCG. The circuit consists of an integer-N 1.25GHz 8-phase PLL, a programmable triangle generator, a ΣΔ modulator, a *multiplexer* (MUX) controller, and a programmable divider. Basically, the design is based on the fractional-N and the ΣΔ modulation technique. But it is different in the way that the programmable SSCG generates various spread spectrum clocks through modulating the multi-phase of the PLL output [25]. The divider in the feedback loop combining with the phase selection of the VCO output attains to a smaller division ratio. It also leads to a less frequency jump in the

output. The approach has an advantage of the low-jitter compared to the direct division modulation.

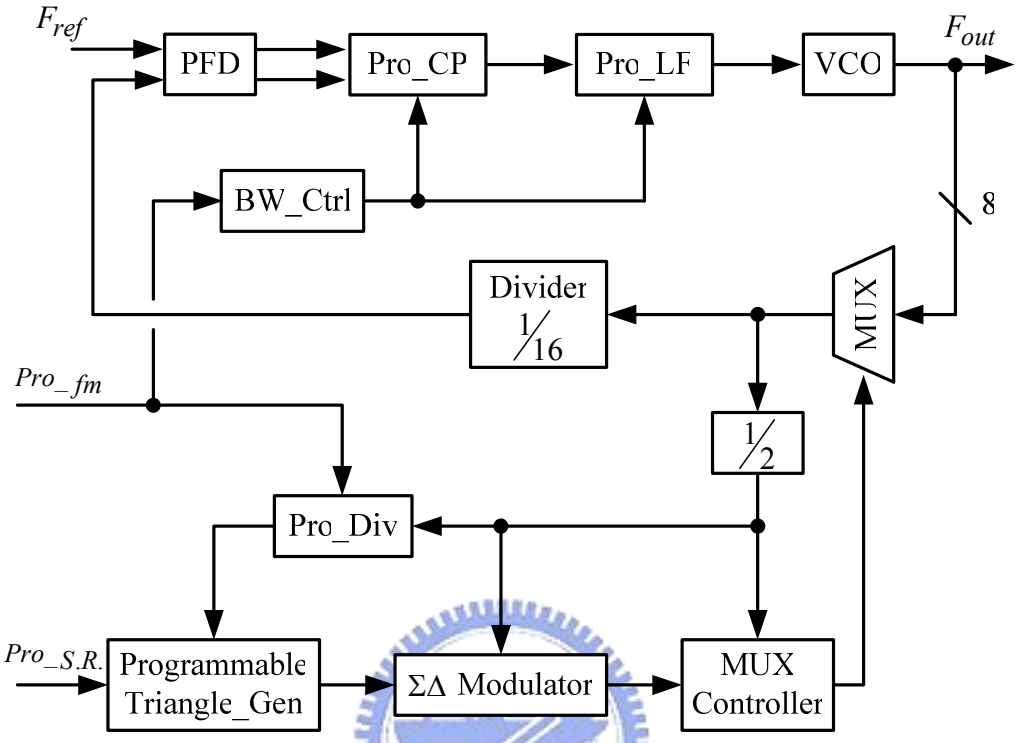
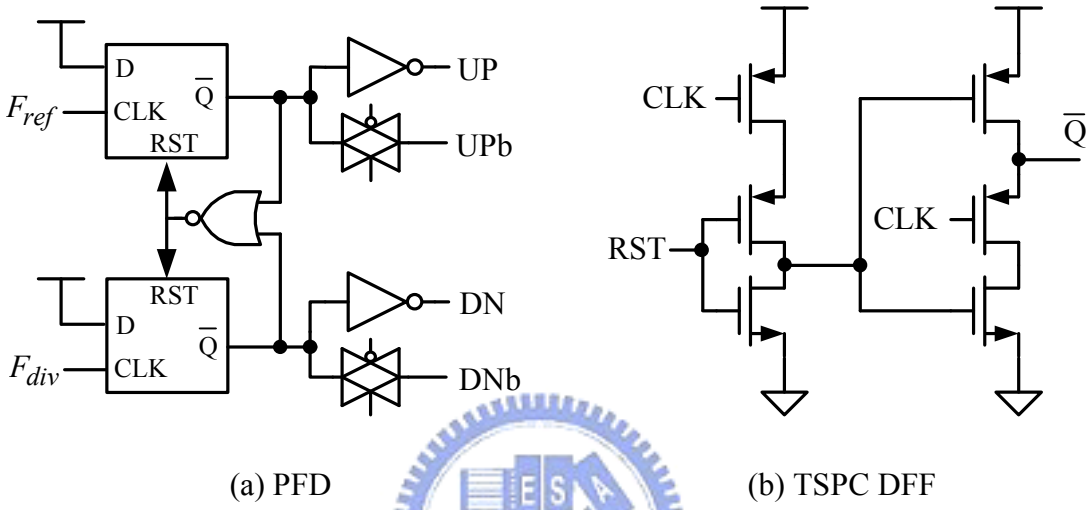


Figure 3.1 Architecture of the proposed programmable SSCG

The programmable divider produces a different clock frequency which is then fed into the programmable triangle generator. Its division ratio is related to the modulation frequency. The programmable triangle generator creates various triangle profiles. It is used to determine the modulation frequencies from 30 kHz to 300 kHz and the spread ratios from 2500 ppm to 50000 ppm. The ΣΔ modulator shapes the noise to a higher frequency. Furthermore, the smoothing effect of the PLL loop results in a continuous frequency modulation from the discrete staircase output of the programmable triangle generator. The MUX controller receives the modulation signal from the ΣΔ modulator and controls the MUX to select a suitable clock phase for the divider. In addition, it is necessary to have a tunable loop bandwidth according to the different modulation frequency in the programmable SSCG.

■ Phase Frequency Detector

Figure 3.2 (a) is a *phase frequency detector* (PFD). It is composed of two *D flip-flops* (DFFs) and a NOR gate. The DFFs are *true single phase clock* (TSPC) type DFFs as shown in Figure 3.2(b) [26]. Compared with the conventional PFD, the PFD with TSPC DFFs overcomes the speed limitation and reduces the dead zone.



(a) PFD (b) TSPC DFF

Figure 3.2 Circuit schematic of (a) PFD, (b) TSPC DFF

Figure 3.3 shows the timing diagram. If the input clocks, F_{ref} and F_{div}, are in-phase, both UP and DOWN pulses are produced in a same short period of time. If there is a phase difference between the input clocks, the difference between the widths of UP and DN pulses is proportional to the input phase difference.

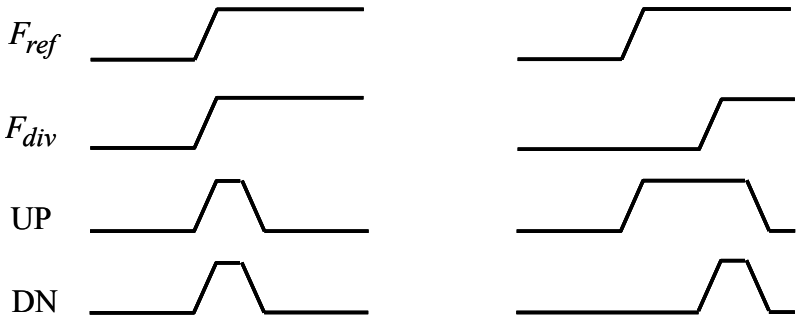


Figure 3.3 PFD timing diagram

■ Programmable Charge Pump

The proposed programmable charge pump is illustrated in Figure 3.4. The biasing current mirror based on a *digital-to-analog converter* (DAC) technique is illustrated in Figure 3.5 [27]. The programmable charge pump converts the phase difference of the input clocks to a voltage signal to control VCO. It is composed of two current sources, four switches, a unit-gain buffer, and a programmable biasing circuit. The charged and discharged currents are programmed by a 2-bit control word. The unit-gain buffer is used to clamp the terminal voltage of the current sources when there is no current pumping into the loop filter. In such way, the voltage glitch due to charge sharing is eliminated.

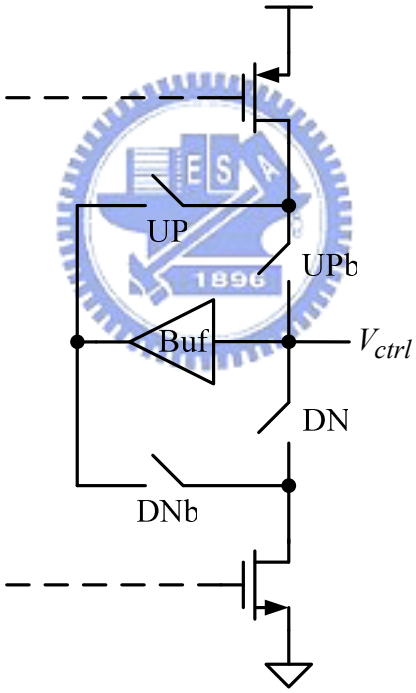


Figure 3.4 Programmable charge pump circuit

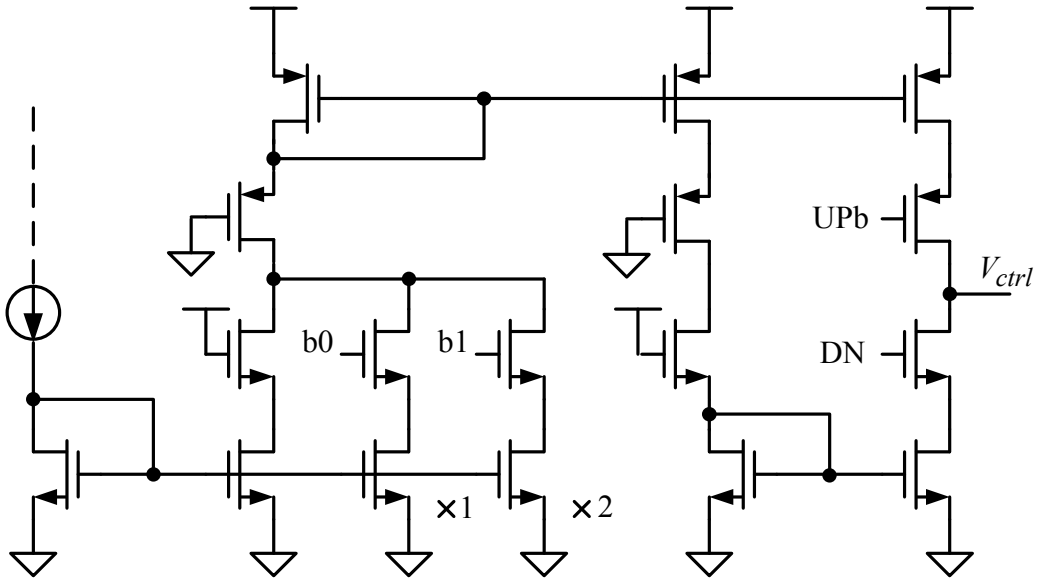


Figure 3.5 Programmable biasing current mirror

■ Programmable Loop Filter

According to the prior chapter, it is known that using a narrow loop bandwidth reduces the output phase noise generated from the $\Sigma\Delta$ modulator. But there occurs some distortions on the triangle modulation profile. To compromise both requirements, one must be careful in determining the loop bandwidth of the system. Here, in order to achieve a finer triangle modulation profile and a smaller output phase noise from the $\Sigma\Delta$ modulator, we design a programmable loop bandwidth. Figure 3.6 shows a second-order loop filter where R_2 is programmed by a 2-bit control word.

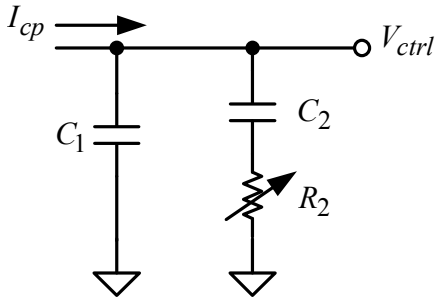


Figure 3.6 Schematic of the second-order loop filter

This transfer function is written as

$$LF(s) = \frac{V_{ctrl}}{I_{cp}} = K_{lf} \cdot \frac{s + \omega_z}{s \cdot (s + \frac{1}{\omega_{p1}})}, \tag{3.1}$$

where $K_{lf} = \frac{R_2 \cdot C_2}{C_1 + C_2}$, $\omega_z = \frac{1}{T_z} = \frac{1}{R_2 \cdot C_2}$, and $\omega_{p1} = \frac{1}{T_{p1}} = \frac{1}{R_2 \cdot (C_1 // C_2)}$.

Figure 3.7 shows the Bode plot of the open loop gain in PLL with a second-order loop filter. Here, we must design the sufficient phase margin ϕ_p to ensure the maximum stability.

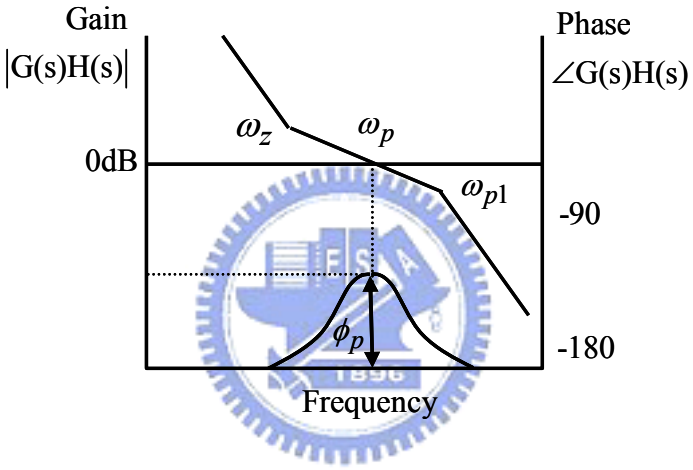


Figure 3.7 Bode plot of PLL with the second-order loop filter

According to [28], we calculate the equations to recide the passive component values as

$$C_1 = \frac{T_{p1}}{T_z} \frac{K_{PFD} K_{VCO}}{\omega_p^2 \cdot N} \sqrt{\frac{1 + (\omega_p \cdot T_z)^2}{1 + (\omega_p \cdot T_{p1})^2}}, \tag{3.2}$$

$$C_2 = C_1 \cdot (\frac{T_z}{T_{p1}} - 1), \tag{3.3}$$

$$R_2 = \frac{T_z}{C_2}, \tag{3.4}$$

where ω_p, K_{PFD}, K_{VCO}, N are the unit gain bandwidth, the PFD's gain, the VCO's gain, and the divider division ratio respectively.

In addition, in order to effectively suppress the out-of-band quantization noise from the ΣΔ modulator at higher frequency, a third pole composed of R_3 and C_3 is added to the loop filter. Figure 3.8 shows this circuit schematic diagram.

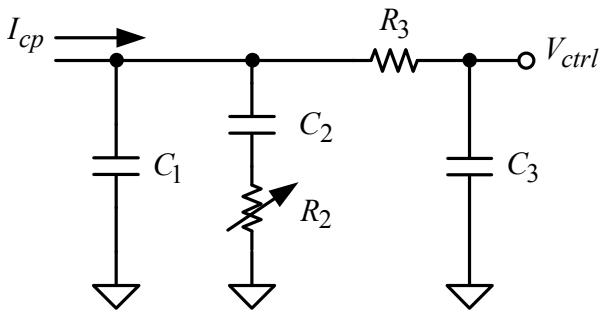


Figure 3.8 Schematic of the third-order loop filter

Thus, the transfer function is

$$LF(s) = K_{lf} \cdot \frac{s + \omega_z}{\frac{1}{\omega_{p1} \cdot \omega_{p2}} s^3 + \left[\frac{1}{\omega_{p1}} + \left(1 + \frac{K_{lf}}{R_2} \right) \cdot \frac{1}{\omega_{p2}} \right] \cdot s^2 + \left(1 + \frac{K_{lf} \cdot \omega_z}{R_2 \cdot \omega_{p2}} \right)^2}, \quad (3.5)$$

where $\omega_{p2} = \frac{1}{R_3 \cdot C_3}$.

We analyze the relationship between the third pole and the added attenuation. It is used as the design criterion in determining the third pole.

$$Attenuation = 10 \cdot \log \left[\left(\frac{\omega_{ref}}{\omega_{p2}} \right)^2 + 1 \right]. \quad (3.6)$$

■ Voltage Controlled Oscillator

In a conventional ring oscillator, the oscillation frequency is decided by a delay time of the delay element. The delay time can not be smaller than a single inverter delay. Therefore, the maximum frequency of the VCO is limited. To solve this frequency limitation problem, a technique using a negative skewed delay scheme has

been proposed. Figure 3.9 shows the VCO structure. It is composed of four-stage fully differential delay cells and dual-delay paths. With the negative skewed delay scheme, it decreases the unit delay time. As a result, a higher operation frequency is obtained [29].

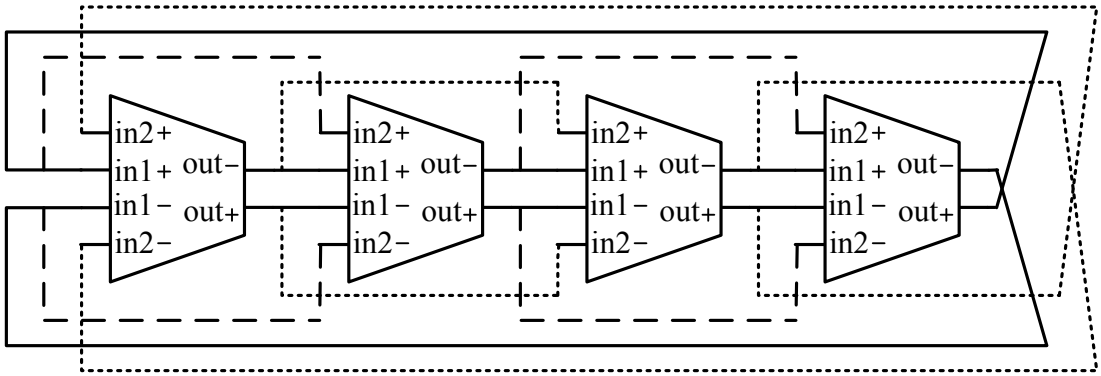


Figure 3.9 Four-stage ring oscillator with dual-delay paths

Figure 3.10 is a four-input differential delay element. When V_{ctrl} is low, the latch becomes weak and the output driving current from the PMOS increases. Therefore, the state is changed easily and the delay time is reduced. Oppositely, when V_{ctrl} is high, the latch becomes strong. It resists the voltage switching in the differential delay cell and the delay time increases. Consequently, with the normal delay paths and the negative skewed delay paths simultaneously, it achieves a higher oscillation frequency and obtains a wider tuning range.

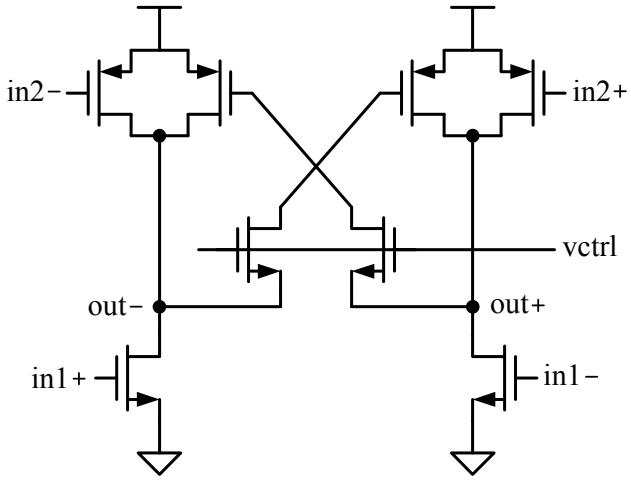


Figure 3.10 Four-input differential delay cell

■ Programmable Triangle Generator

The programmable triangle generator is designed to create a different triangle profiles. It determines the modulation frequencies from 30 kHz to 300 kHz and the spread ratios from 2500 ppm to 50000 ppm. Figure 3.11 is the proposed programmable triangle generator including an accumulator and a counter. It generates the triangle waveform with discrete staircases for the ΣΔ modulator. Through the different clock frequency of $CLK_{\_tri}$ from the programmable divider, it generates different clock cycles of *Sel* at a fixed count number of the counter. Thus, the various modulation frequencies are produced and illustrated in Figure 3.12 (a). In addition, the programming signal $Pro_{\_S.R.}$ decides the frequency deviation. As illustrated in Figure 3.12 (b), it is accumulated increasingly or decreasingly along with $CLK_{\_tri}$ until *Sel* changes state. Therefore, by programming $CLK_{\_tri}$ and $Pro_{\_S.R.}$, we obtain the desired triangle profile.

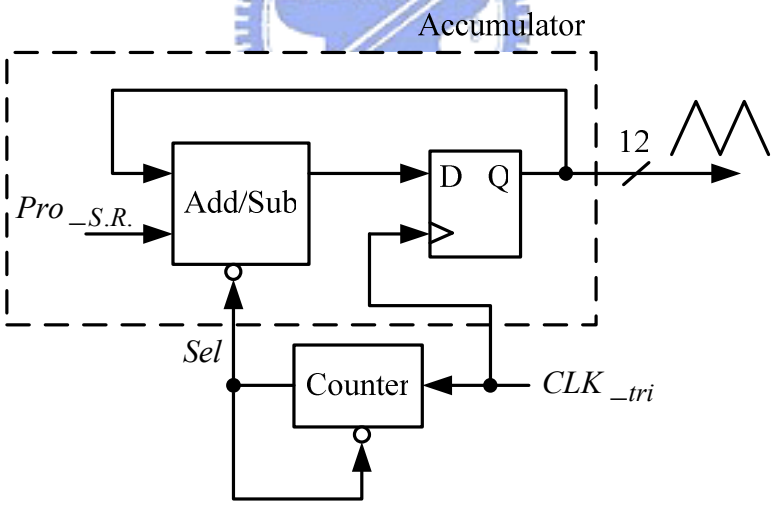
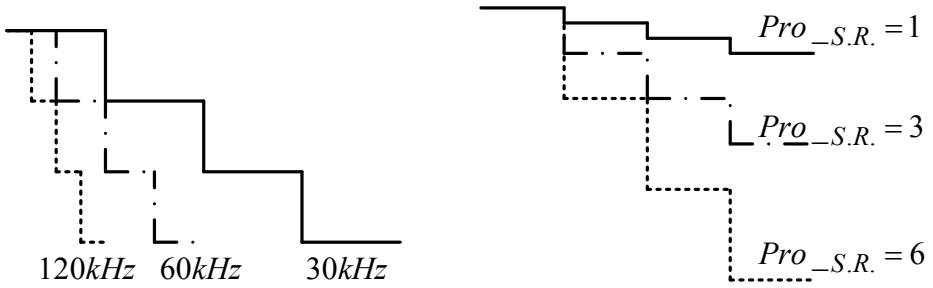


Figure 3.11 Scheme of the programmable triangle generator



(a) Different modulation frequencies (b) Different spread ratios

Figure 3.12 Difference discrete staircases of the triangle profile

■ MASH 1-1 Sigma-Delta Modulator

As described in Chapter 3, the ΣΔ modulator implemented in the PLL provides the low phase noise and reduces the spurious impact. It overcomes the shortcomings in traditional PLL frequency synthesizers. In addition, the MASH architecture is unconditionally stable and easy for the digital implementation.

Shown in Figure 3.13 is the digital implementation of a modified second-order MASH 1-1 ΣΔ modulator. The output $Y(z)$ is a 2-bit word and fed into the MUX controller.

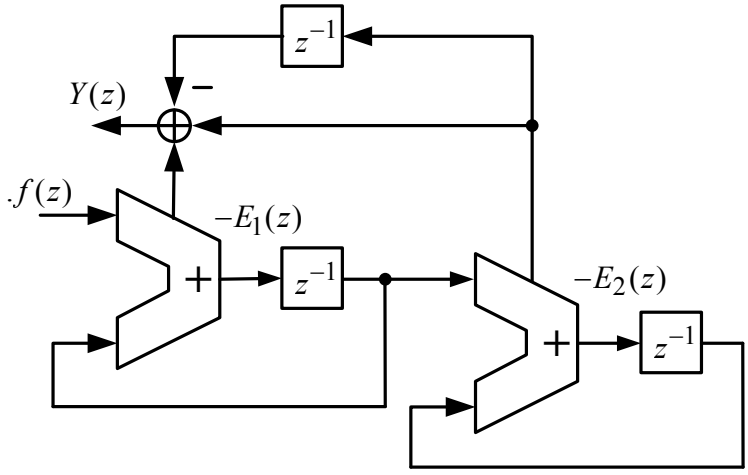


Figure 3.13 Digital implementation of MASH 1-1 ΣΔ modulator

The transfer function is written as

$$Y(z) = f(z) \cdot z^{-2} + (1 - z^{-1})^2 \cdot E_2(z), \tag{3.7}$$

where $f(z)$ is the wanted output frequency and $E_2(z)$ is the quantization noise from the second stage. (3.7) shows that the first term includes the delay of z^{-2} and the second term is the same as (2.15). It has the output signal delays for two clock cycles. However, it does not influence the noise-shaping behavior of the ΣΔ quantization noise.

■ Multiplexer Controller

Figure 3.14 shows the *multiplexer* (MUX) controller. It includes an accumulator and a decoder. The MUX controller is placed between the MASH 1-1 ΣΔ modulator and the MUX. It receives the modulation signals from the ΣΔ modulator and transfers them to one-hot code. Then, MUX controller controls the MUX for the phase selection. Table 3.1 shows the output state of the ΣΔ modulator and the corresponding behavior with the phase selection. It executes to rotate right or left one phase in the MUX.

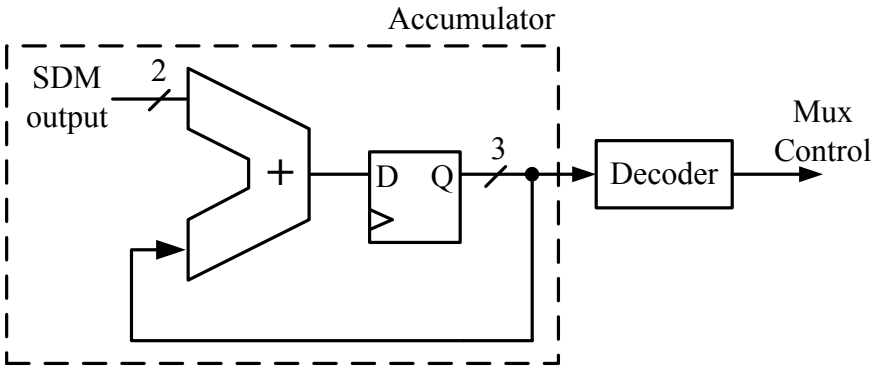


Figure 3.14 Scheme of the multiplexer controller

Table 3.1 Output state table of the ΣΔ modulator

SDM Output	Shift Phase	Shift Type
11	1	Shift right 1 phase
00	0	Hold
01	-1	Shift left 1 phase
10	-2	Shift left 2 phase

Through the transformation of the decoder, the output signal of the accumulator is decoded to an one-hot code. Shown in Table 3.2 is the relationship between the 3-bit output signal of the accumulator and the MUX control signals. The MUX control signals correspond to the multiphase output of the VCO respectively. According to the different signal from the ΣΔ modulator, we obtain the desired MUX control signal and the suitable phase clock in the MUX.

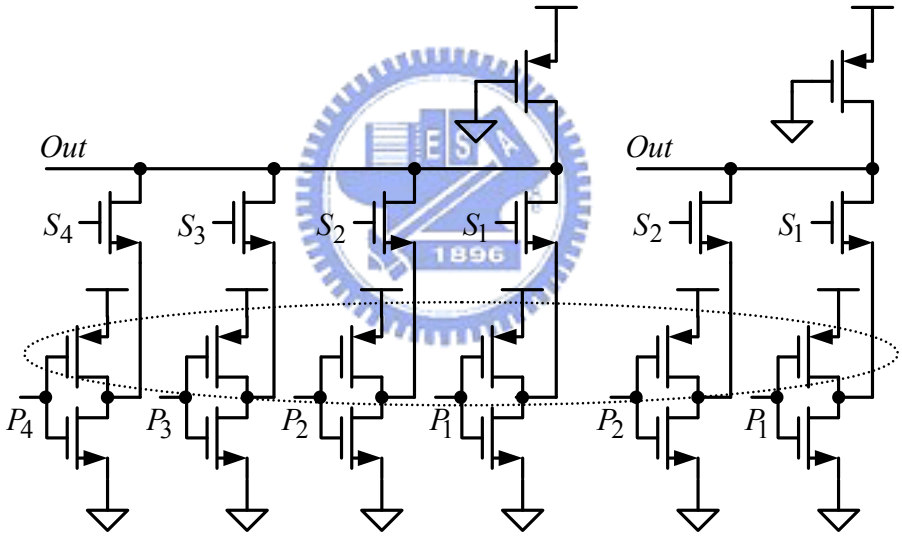
Table 3.2 Relationship between accumulator output and MUX control signals

Accumulator Output	Mux Control Signals							
	S1	S2	S3	S4	S5	S6	S7	S8
000	1	0	0	0	0	0	0	0
001	0	1	0	0	0	0	0	0
010	0	0	1	0	0	0	0	0
011	0	0	0	1	0	0	0	0
100	0	0	0	0	1	0	0	0
101	0	0	0	0	0	1	0	0
110	0	0	0	0	0	0	1	0
111	0	0	0	0	0	0	0	1

■ Multiplexer

Through receiving the modulation signals from the ΣΔ modulator, the MUX selects the suitable phase clock for the divider. Here, the 8-to-1 MUX in our design is composed of two 4-to-1 MUX and a 2-to-1 MUX and shown in Figure 3.15 [26]. The extra PMOS transistors in the phase clock input is to precharge the internal node to a high level when the phase clock is low. Therefore, it has a benefit of reducing the charge sharing effect and alleviating the clock jitter.

Furthermore, with different phase selection sequences, it realizes different frequency division ratios in PLL. Moreover, the spreading clock is obtained by modulating the multiphase clock output in the programmable SSCG.



(a) 4-to-1 MUX (b) 2-to-1 MUX

Figure 3.15 Circuit scheme of the (a) 4-to-1 MUX, (b) 2-to-1 MUX

■ Programmable Divider

The programmable divider produces clocks of different frequency to be fed into the programmable triangle generator. Its division ratio is determined by an assigned program to determine the modulation frequency. Shown in Figure 3.16 is the architecture of the 6-bit programmable frequency divider. It includes a 6-bit counter, an *end-of-count* (EOC) detector, and a reload circuit [30].

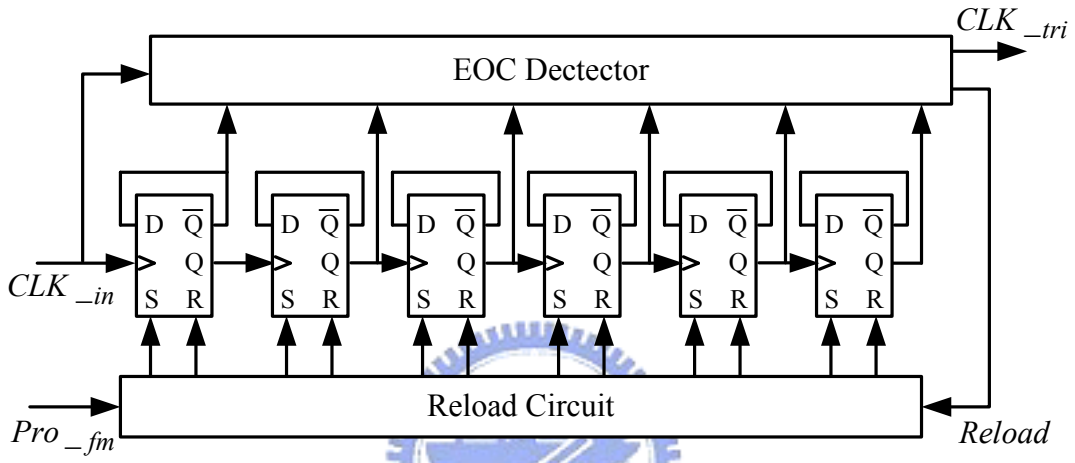


Figure 3.16 Architecture of the 6-bit programmable frequency divider

The circuit principle is assumed as a countdown counter. First, a certain preset number is loaded in the counter and the counter starts counting. Once the counter reaches the terminal count state 000010, the EOC detector delivers a *Reload* signal to the reload circuit. Then, the counter is commanded to set the initial value N and starts counting again. Therefore, the relationship between the input clock frequency and the output clock frequency is $f_{tri} = f_{in}/N$. With 6 counter stages, the frequency division ratio N can be varied from 2 to $2^6 - 1$.

Chapter 4

Simulation Results and Layout

The programmable SSCG implementation is based on a fractional-N technique by using a $\Sigma\Delta$ modulation. There are some design issues to be considered such as the system stability problem, the PLL responses, and the loop bandwidth design, etc. In this chapter, we verify the spread spectrum clocking behavior by MATLAB simulation tool and the circuit simulation by HSPICE simulation tool. Finally, we show the global chip layout and the test environment.

4.1 Programmable SSCG Behavior Simulation

In order to verify the behavior and the function of the programmable SSCG, we

use the MATLAB simulation tool to analyze. Figure 4.1 shows the SIMULINK model. It is based on a charge-pump PLL with a third-order filter. The programmable triangle generator, MASH 1-1 ΣΔ modulation, and MUX controller are also added to modulate the output clocks. We obtain the various triangle modulation clocks through the 6-bit programming modulation frequency and the 5-bit programming spread ratio. This system is simulated as far as the circuit-level is concerned.

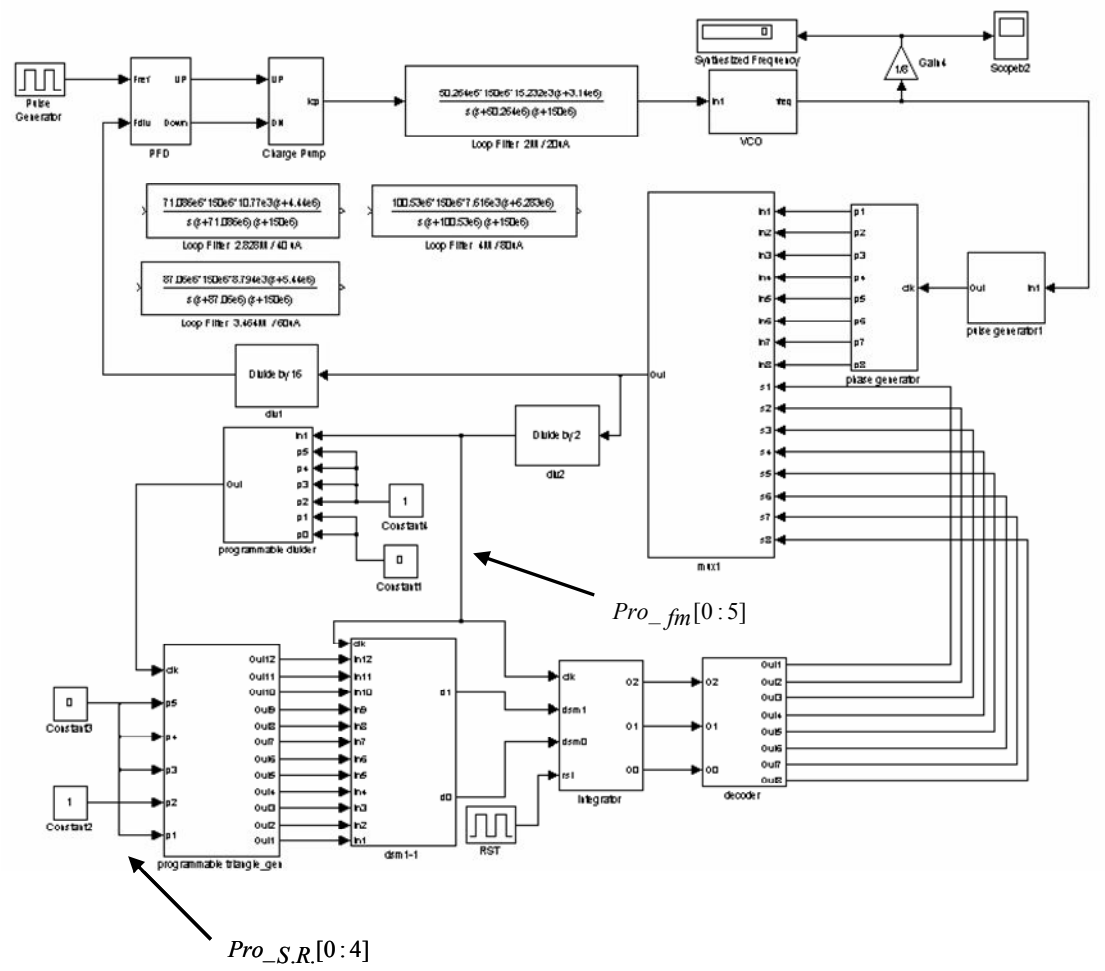


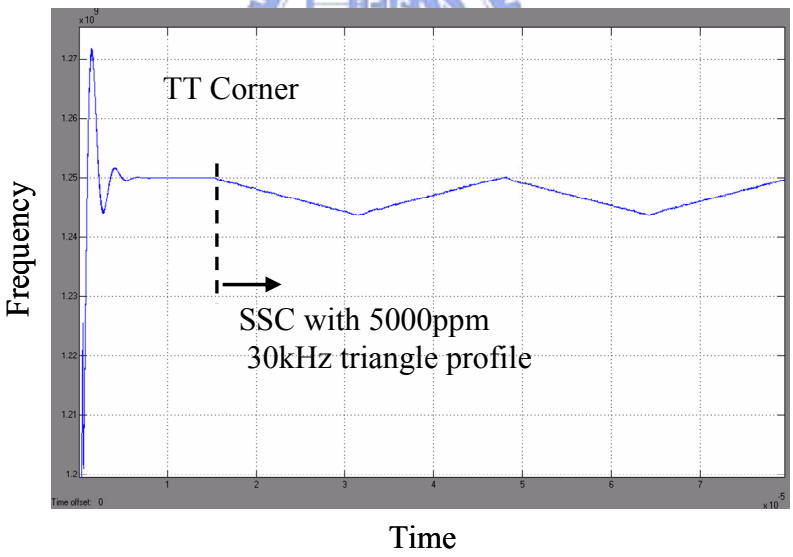
Figure 4.1 SIMULINK model of the programmable SSCG

In addition, we extract from the post-layout simulation results of each fundamental element with corner model variations and arrange them in Table 4.1. Including the data of an inverter delay, a NOR delay, and a DFF delay, etc, are added in this SIMULINK model. Thus, the more precise results can be obtained by the SIMULINK simulation.

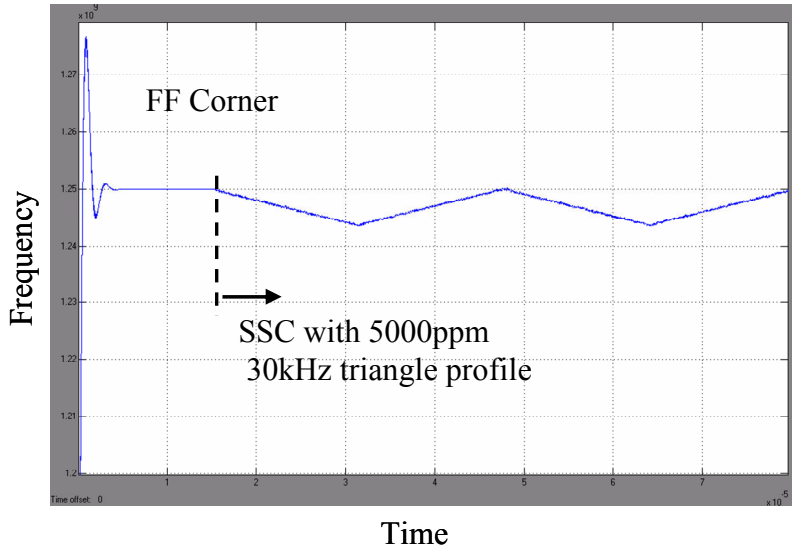
Table 4.1 Post-layout simulation delay time of each fundamental element

		SS	TT	FF
Inverter, NAND, NOR…		50ps	40ps	32ps
XOR		30ps	27ps	25ps
DFF		160ps	125ps	115ps
Full Adder (12bit)	SUM	1160ps	930ps	750ps
	CARRY OUT	1230ps	990ps	800ps
Half Adder	SUM	23ps	19ps	16ps

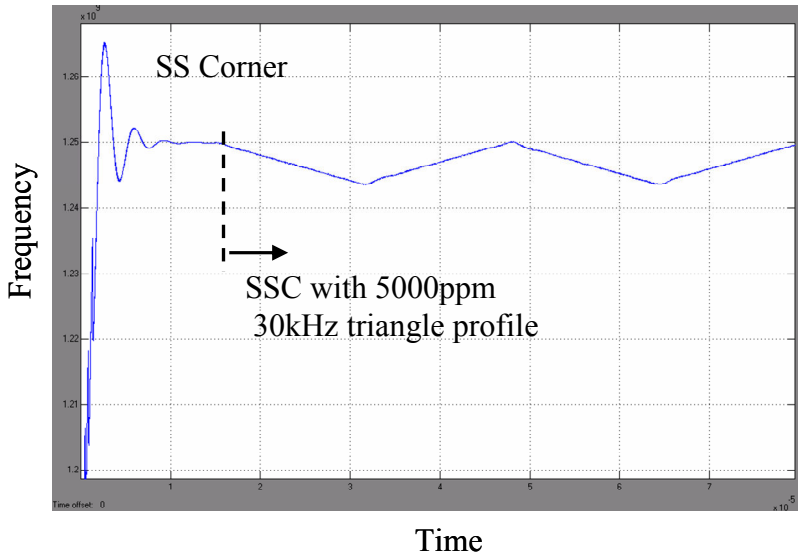
According to Table 4.1, the behavior simulation results with similar corner model variations in time-domain are respectively shown in Figure 4.2 (a), (b), (c). They all exhibit the cases that the frequency is down spreading with a spread ratio of 5000 ppm and a modulation frequency of 30 kHz.



(a) TT corner



(b) FF corner



(c) SS corner

Figure 4.2 Behavior simulation of SSC at the difference corners

We analyze this design in FFT with the spread ratio of 5000 ppm and the modulation frequency of 30 kHz. The compared results between SSC mode and non-SSC mode are shown Figure 4.3. The results display that there is about 20 dB reduction of the peak energy.

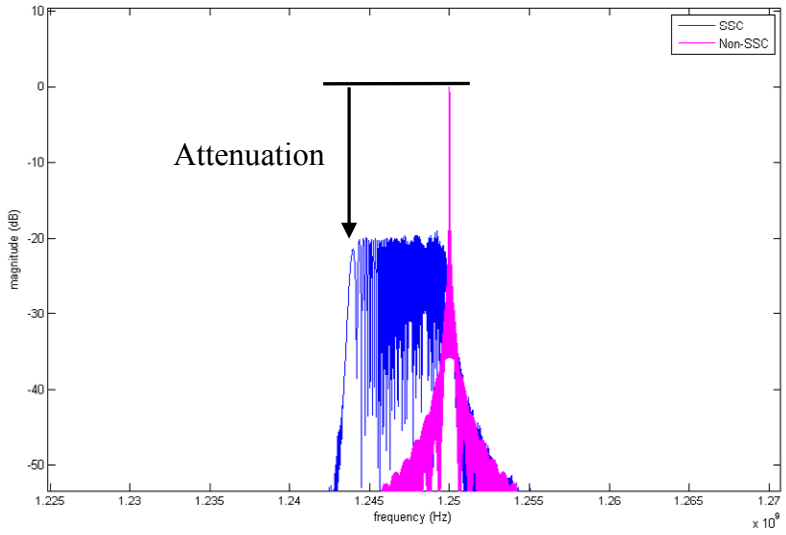


Figure 4.3 FFT of the programmable SSCG at SSC mode and non-SSC mode

4.2 Programmable SSCG Circuit-Level Simulation

In order to receive the more precise simulation result, we use the HSPICE simulation tool to analyze. Figure 4.4 shows the post-layout simulation result of the VCO with corner model variations. The VCO's gain is about 680 MHz/V at 1.25 GHz.

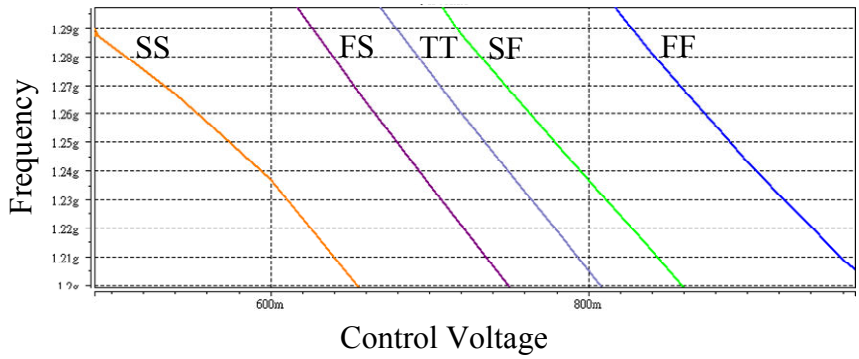
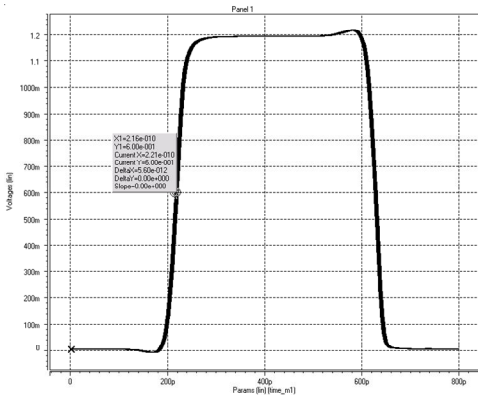
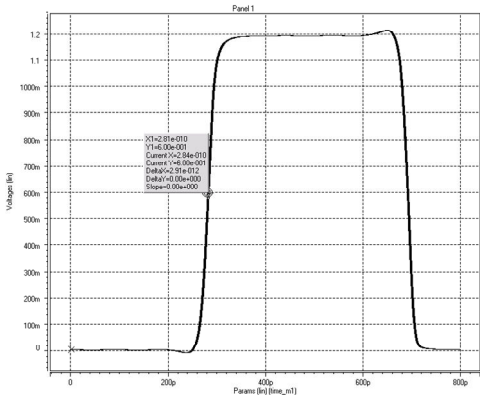


Figure 4.4 Characteristic curves of VCO with corner model variations

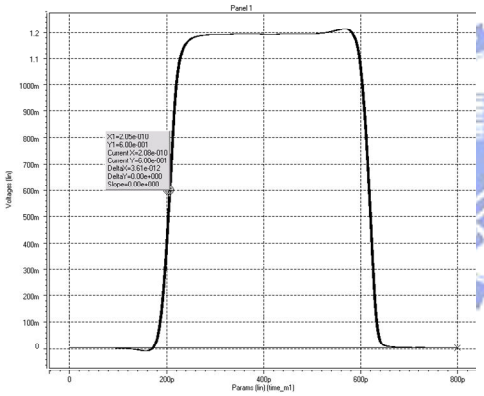
The output eye diagram at non-SSC mode with five corner model variations are shown in Figure 4.5 respectively. The simulation results of the jitter are shown in Table 4.2.



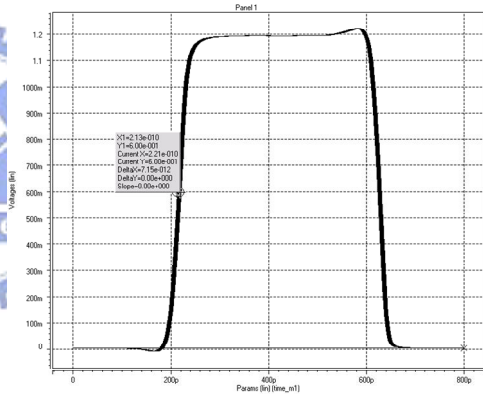
(a) TT corner



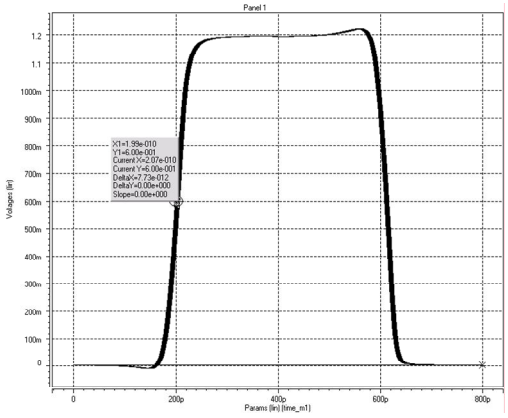
(b) FF corner



(c) FS corner



(d) SF corner



(e) SS corner

Figure 4.5 Output eye diagram at non-SSC mode

Table 4.2 Jitter of the Output eye diagram at non-SSC mode

	TT	SS	FF	SF	FS
$Jitter_{(p-p)}$	5.6ps	7.75ps	2.9ps	7.2ps	3.6ps

In order to verify the function in SSC mode, we select several cases for the simulation. We can see various frequency-modulation results with triangular waveform in time domain and frequency domain obviously.

First, Figure 4.6 shows the control voltage variation in SSC mode with a spread ratio of 32500 ppm and a modulation frequency of 30 kHz. Figure 4.7 shows its spectrum with spreading.

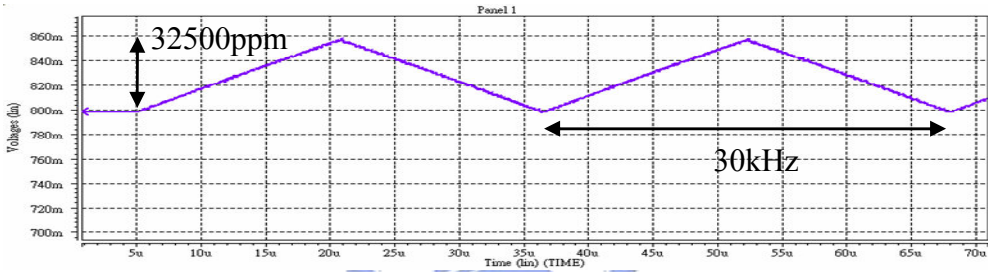


Figure 4.6 Control voltage of SSCG with 32500 ppm and 30 kHz spread

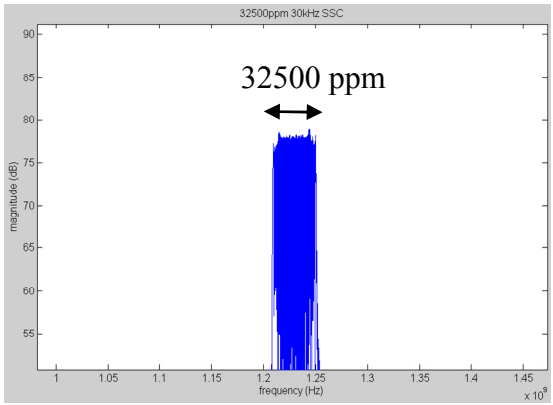


Figure 4.7 FFT of SSCG with 32500 ppm and 30 kHz spread

Second, Figure 4.8 shows the control voltage variation in SSC mode with a spread ratio of 50000 ppm and a modulation frequency of 30 kHz. Figure 4.9 shows its spectrum with spreading.

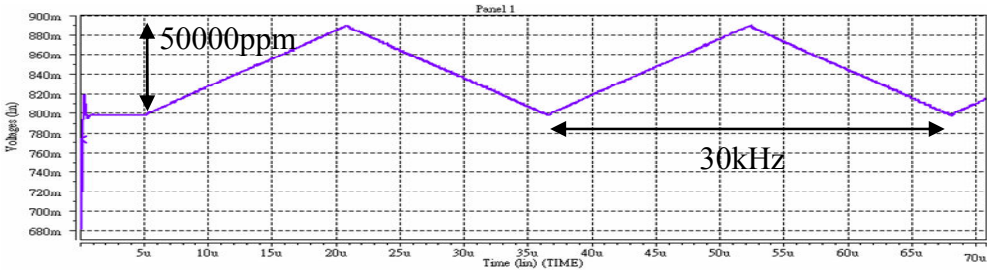


Figure 4.8 Control voltage of SSCG with 50000 ppm and 30 kHz spread

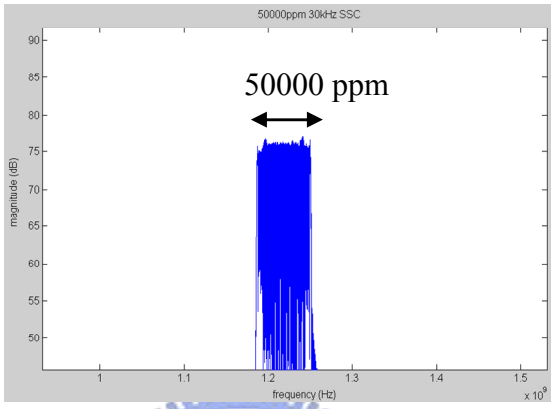


Figure 4.9 FFT of SSCG with 50000 ppm and 30 kHz spread

Third, Figure 4.10 shows the control voltage variation in SSC mode with a spread ratio of 5000 ppm and a modulation frequency of 150 kHz. Figure 4.11 shows its spectrum with spreading.

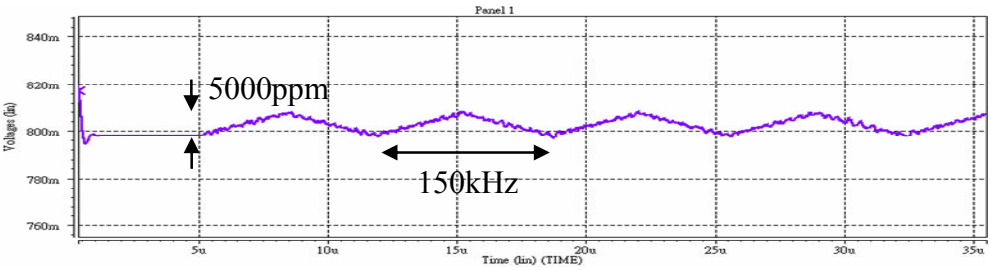


Figure 4.10 Control voltage of SSCG with 5000 ppm and 150 kHz spread

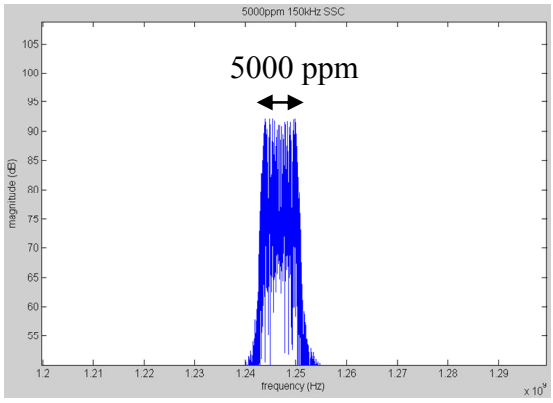


Figure 4.11 FFT of SSCG with 5000 ppm and 150 kHz spread

Finally, Figure 4.12 shows the control voltage variation in SSC mode with a spread ratio of 5000 ppm and a modulation frequency of 300 kHz. Figure 4.13 shows its spectrum with spreading.

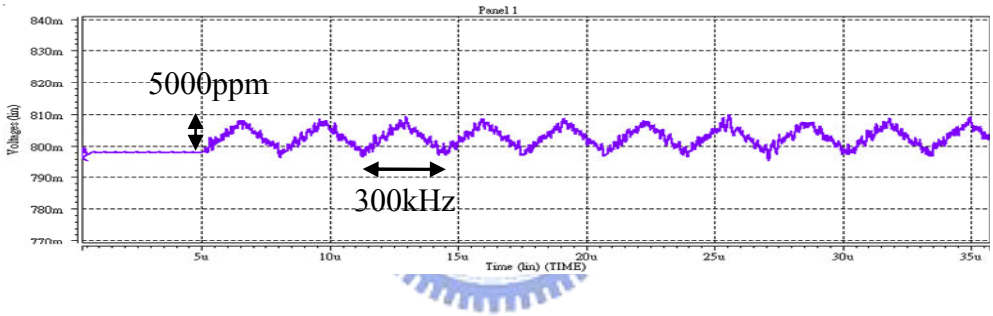


Figure 4.12 Control voltage of SSCG with 5000 ppm and 300 kHz spread

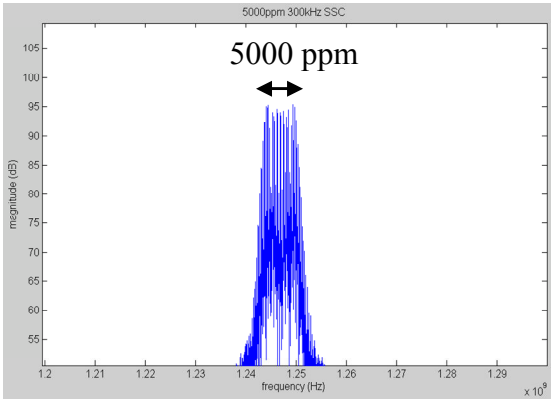


Figure 4.13 FFT of SSCG with 5000 ppm and 300 kHz spread

According to the previous simulation results, we illustrate a graph for comparison. Shown in Figure 4.14 is the EMI attenuation versus the different spread ratio and the different modulation frequency. Here, the relationship between EMI attenuation and theses parameters corresponds with (1.4) as expected. However, the simulation curve is under the ideal curve from 1.3 dB to 3 dB. This is because the use of the modulation of PLL feedback loop and the SSCG jitter influence.

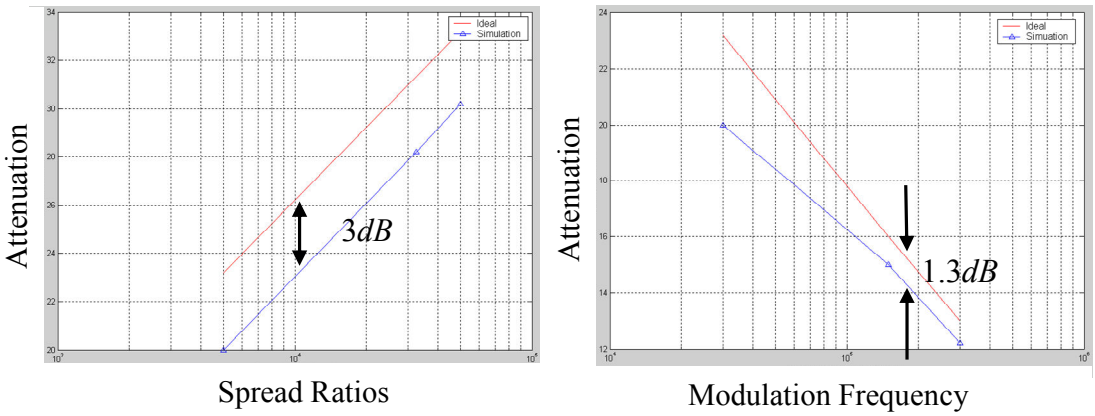


Figure 4.14 EMI attenuation versus the spread ratios and the modulation frequency

4.3 Layout and Measurement Setup

A chip layout of the proposed programmable SSCG is shown in Figure 4.15. It consists of a conventional PLL and the proposed programmable triangle modulation circuit. The rest area is filled up with decouple capacitance to bypass power noise. This chip is implemented in TSMC 0.13um RF 1P8M technology and the chip size is $750\mu m \times 750\mu m$.

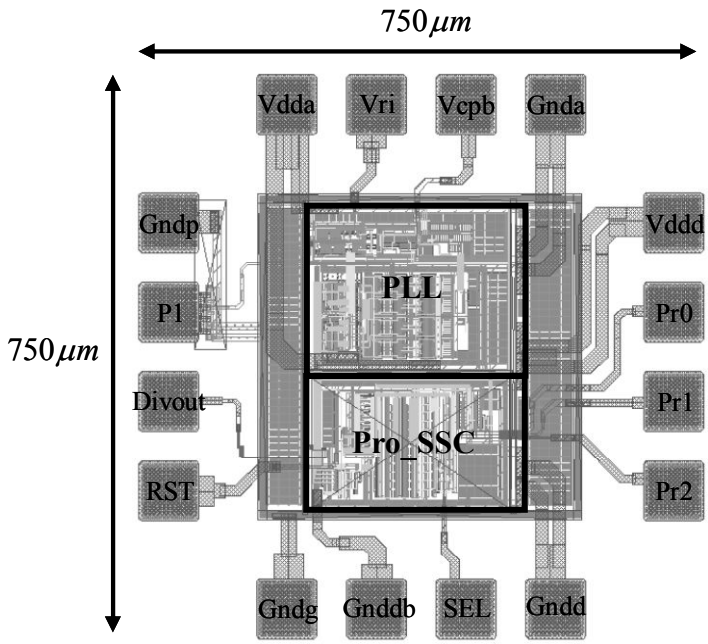


Figure 4.15 Chip layout of the programmable SSCG

The test environment is shown in Figure 4.16. The power is divided into analog power and digital power in order to avoid interfering with each other. The test pin *Sel* is probed by a logic analyzer and observed the modulation frequency of SSC. A spectrum analyzer and an oscilloscope are used to obtain some information with the SSCG output signals including the jitter measurement, the spectrum, and the spread ratio, etc. Finally, with programming the 3-bit control word, the programmable SSCG generates eight types of spreading spectrum clocks.

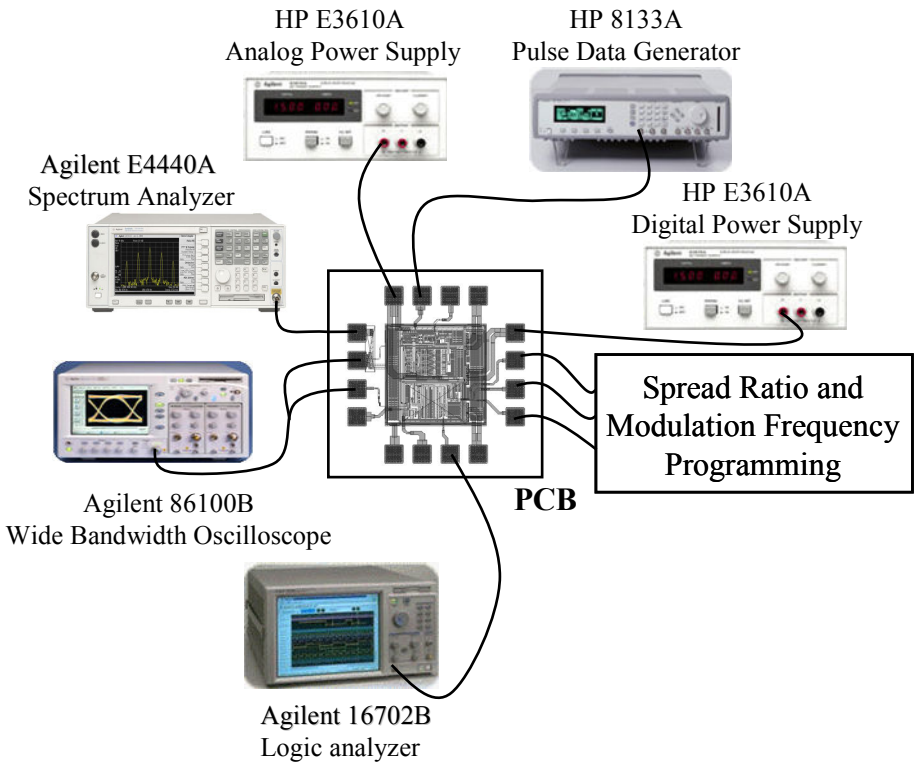


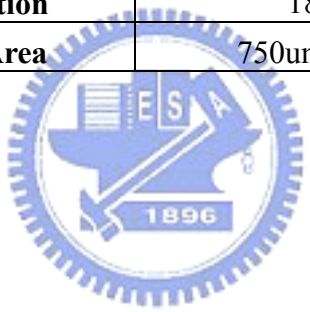
Figure 4.16 Measurement setup

4.4 Summary and Comparison

The summary of the simulation results of the programmable SSCG is shown in Table 4.3. We realize the circuit with the various modulation frequencies from 30 kHz to 300 kHz and the various spread ratios from 2500 ppm to 50000 ppm. The peak-to-peak jitter at non-SSC mode is 5.6 ps. The power dissipation is 18 mW.

Table 4.3 Summary with simulation results of the programmable SSCG

	This work
Technology	TSMC 0.13um RF
Supply Voltage	1.2V
Modulation Profile	Triangle
Modulation Type	Down-Spread
Output Frequency (non-SSC)	1.25 GHz
Spread Ratios	2500 ~ 50000 ppm
Modulation Frequency	30 ~ 300 kHz
Peak-to-Peak Jitter (non-SSC) (TT)	5.6 ps
Peak Reduction	20 dB @ 30 kHz, 5000 ppm spread
Power Dissipation	18 mW
Chip Layout Area	750um×750um



Chapter 5

Conclusion

In this thesis, we realize a programmable SSCG. The circuit consists of a conventional PLL generating 1.25GHz, 8-phase clocks, a programmable triangle generator, a digital ΣΔ modulator, a MUX controller, and a programmable divider. It is based on the fractional-N technique by using the ΣΔ modulator. The programmable SSCG achieves the spread spectrum function with triangular waveform modulation. It generates the clock with the various modulation frequencies from 30 kHz to 300 kHz and the various spread ratios from 2500 ppm to 50000 ppm. In addition, it has a variable loop bandwidth for different triangle profiles. Through modulating the multiphase output, it avoids large frequency jump in the feedback divider.

Finally, the programmable SSCG is implemented in TSMC 0.13 um 1P8M RF technology. The simulation results show that the non spreading clock has a peak-to-peak jitter of 5.6 ps, the reduction of peak energy is 20 dB at 30 kHz 5000 ppm spread, the power dissipation is 18 mW and the chip size is $750\mu m \times 750\mu m$. This architecture does achieve various spread spectrum profiles as expected.

Bibliography

[1] "Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor: Spread-Spectrum Clocking to Reduce EMI," Sep. 2003.

[2] S. Johnson, Y. Yin, R. Zane, "Custom spectral shaping for EMI reduction in electronic ballasts," in Proc. IEEE Appl. Power Electron. Conf. Expo., Anaheim, CA, pp. 137-142, February 2004.

[3] F. Lin and D. Y. Chen, "Reduction of Power Supply EMI Emission by Switching Frequency Modulation," in The VPEC Tenth Annual Power Electronics Seminar, Virginia Power Electronics Center, Blacksburg, Virginia, September 20-22,1992.

[4] Keith B. Hardin, John T. Fessler, and Donald R. Bush, "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions," in IEEE International Symposium on Electromagnetic Compatibility, pp. 227-231, 1994.

[5] Keith B. Hardin, John T. Fessler, Nicole L. Webb, John B. Berry, Andrew L. Cable, and Mike L. Pulley, "Design considerations of phase-locked loop systems for spread spectrum clock generation compatibility," in IEEE International Symposium on Electromagnetic Compatibility, pp 302 -307, 1997.

[6] J. Kim, P. Jun, J. Byun, J Kim, "Design Guidelines of Spread Spectrum Clock for Suppression of Radiation and Interference from High-speed Interconnection Line," in Proc. IEEE Workshop on Signal Propagation on Interconnect, pp.189-192, 2002.

[7] H. H. Chang, I. H. Hua and S. J. Liu, "A spread-spectrum clock generator with triangular modulation," IEEE J. Solid-State Circuits, Vol.38, No.4, April, 2003

[8] H. Mair and L. Xiu, "An Architecture of High-Performance Frequency and Phase Synthesis," IEEE J. Solid-State Circuits, vol. 35, pp. 835-846, June. 2000.

[9] M. Kokubo, T. Kawamoto, T. Oshuma, T. Noto, M. Suzuki, S. Suzuki, T. Hzyasaka, T. Takahashi and J. Kasai "Spread-spectrum Clock Generator for Serial

ATA using Fractional PLL controlled by ΔΣ Modulator with Level Shifter," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp. 160-590, 2005.

[10] W. T. Chen, J. C. Hsu, H. W. Lune and C. C. Su, " A spread spectrum clock for SATA-II" IEEE international symposium on circuit and systems, vol. 3, pp. 2643-2646, May 2005.

[11] Heredia, N.J., "Spread spectrum clock-an EMC solution for new generation portable computers," Electromagnetic Interference and Compatibility, 2002. Proceedings of the International Conference. pp. 146-151, 2002.

[12] "Jitter in PLL-Based System: Causes, Effects, and Solutions," http://www.cypress.com, July 1997.

[13] M. T. Zhang, "Notes on SSC and Its Timing Impacts," http://www.intel.com, February 1998.

[14] Roland E. Best, Phase-Locked Loops Theory Design, Simulation, and Applications, McGraw-Hill international editions, 1993.

[15] Behzad Razavi, Design of analog CMOS integrated circuits, McGraw-Hill international editions, 2001.

[16] T. A. D. Riley, M. A. Copeland, and T. A. Kawasniewski, "Delta-Sigma Modulation in Fractional-N Frequency Synthesis," IEEE Journal of Solid-State Circuits, pp.553-559, 1993.

[17] "Parallel-input PLL frequency synthesizer MC145152-2," Semiconductor technical data, Motorola, Inc., 1999.

[18] Behzad Razavi, RF Microelectronics, Pretice-Hall, Inc., 1998

[19] Steven R. Norsworthy, Richard Schreier and Gabor C. Temes, Delta-Sigma Data Converters, IEEE press

[20] R. M. Gray, "Quantization noise spectra," IEEE Trans. Of information theory, vol. 36, no. 6, pp. 1220-1244, Nov. 1990.

[21] Woogenun Rhee, Multi-bit Delta-sigma Modulation Technique for Fractional-N Frequency Synthesizers, Ph.D. thesis, University of Illinois at Urbana-Champaign, 2001.

[22] M. Kozak and I. Kale, "A pipelined noise shaping coder for fractional-N frequency synthesis," IEEE Trans. Instrumentation and Measurement, vol. 50, pp. 1154-1160, Oct. 2001.

[23] B. D. Muer and M. S. J. Steyaert, "On The Analysis of Fractional-N Frequency Synthesizers for High-Spectral Purity" IEEE Trans. Circuits Syst., vol. 50, pp. 784-793, Nov. 2003.

[24] D. S. Kim and D. K. Jeong, "A Spread Spectrum Clock Generation PLL with Dual-tone Modulation Profile" in Symposium on VLSI Circuits Dig. Tech. Papers, pp.96-99, 2005.

[25] H. R. Lee, O. Kim, G. Ahn and D. K. Jeong, "A low-jitter 5000ppm spread spectrum clock generator for multi-channel SATA transceiver in 0.18μm CMOS," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp. 162-590, 2005.

[26] Shi-Dai Mai, "Multi-module synchronization methodology" Master Degree dissertation of National Central University 2002.

[27] S. Sidiropoulos, D. Liu, J. Kim, G. Wei, M. Horowitz, "Adaptive Bandwidth DLLs and PLLs using regulated supply CMOS buffers," in VLSI Circuit Symp., pp. 124-127, 2000.

[28] William O. Keese, "An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phase-Locked Loops" National Semiconductor Application Note, May 1996.

[29] C. H. Park and B. Kim, "A Low-Noise, 900-MHz VCO in 0.6-μm CMOS" IEEE J. Solid-State Circuits, vol. 34, pp. 586-591, May 1999.

[30] H.–H. Chang and J.–C. Wu, "A 723-MHz 17.2-mW CMOS programmable counter," IEEE J. Solid-state Circuits, pp. 1572-1575, Oct. 1998.