國立交通大學

電子工程學系電子研究所

博士論文

低電壓互補式金氧半製程下的高電壓電路設計

HIGH-VOLTAGE CIRCUIT DESIGN IN LOW-VOLTAGE CMOS PROCESSES

研 究 生 ：陳 世 倫（Shih-Lun Chen)
指導教授 ：柯 明 道（Ming-Dou Ker)

中華民國九十五年七月


E
S
A
1896

低電壓互補式金氧半製程下的高電壓電路設計

HIGH-VOLTAGE CIRCUIT DESIGN IN LOW-VOLTAGE CMOS PROCESSES

研究生：陳世倫 Student: Shih-Lun Chen
指導教授：柯明道 Advisor: Ming-Dou Ker

國立交通大學
電子工程學系電子研究所
博士論文

A Dissertation
Submitted to Department of Electronics Engineering
and Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy
in
Electronic Engineering

July 2006
Hsinchu, Taiwan, Republic of China

中華民國九十五年七月

E
S
A
1896

低電壓互補式金氧半製程下的高電壓電路設計

研究生：陳世倫 **指導教授：柯明道 博士**

國立交通大學電子工程學系電子研究所

摘要

本論文提出數個在低電壓互補式金氧半(CMOS)製程下所設計的高電壓電路。隨著互補式金氧半製程的進步，積體電路(Integrated Circuit)的操作速度越來越快而電晶體(Transistor)的面積越來越小。由於積體電路可靠度(Reliability)的問題，電晶體的正常操作電壓(Normal Operation Voltage)必需隨著製程進步而降低。另一方面，由於系統晶片(System-on-a-Chip，SOC)的設計趨勢，單一晶片裡將包含許多不同類形的電路。所以在一個系統晶片裡，部分電路仍然必需操作在高電壓的環境裡。如果利用低電壓製程所設計的積體電路操作在高電壓的環境，閘極氧化層可靠度(Gate-Oxide Reliability)、熱載子衰退效應(Hot-Carrier Degradation)、漏電流(Leakage Current)等現象將會發生。所以本論文提出了數個低電壓互補式金氧半製程下所設計的高電壓電路，且無閘極氧化層可靠度、熱載子衰退效應、漏電流等問題。本論文所提出的電路適合實現在深次微米(Deep Sub-Micron Meter)，甚至是奈米(Nano Meter)互補式金氧半製程裡。本論文共包含七個章節。

在第二章中，本論文提出了兩個利用低電壓元件所實現的混合電壓介面輸入輸出電路(Mixed-Voltage I/O Buffer)。這兩個混合電壓介面輸入輸出

電路擁有新型的動態N阱偏壓電路(Dynamic N-Well Bias Circuit)和閘極電壓追蹤電路(Gate-Tracking Circuit)來避免混合電壓介面(Mixed-Voltage Interface)所造成的漏電流的問題。此外，這兩個混合電壓介面輸入輸出電路也避免了閘極電壓過高所造成的閘極氧化層可靠度問題。跟先前的混合電壓介面輸入輸出電路比較，本論文所提出的兩個利用低電壓元件所實現的混合電壓介面輸入輸出電路擁有較小的面積。此外，本論文所提出的第二個混合電壓介面輸入輸出電路解決了浮接N阱(Floating N-Well)的現象，將可大量減少次臨介漏電流(Subthreshold Leakage Current)的問題。其更適用於先進製程下的設計。本論文所提出的兩個利用低電壓元件所實現的混合電壓介面輸入輸出電路已經在2.5伏0.25微米互補式金氧半製程裡實現並驗證。

由於系統晶片的需求，單一晶片內可能包含數位電路以及類比電路。以1/2.5伏0.13微米互補式金氧半製程來說，數位電路用1伏元件來實現以減少功率消耗(Power Consumption)和矽面積(Silicon Area)，類比電路以2.5伏元件來實現以保持電路的效能(Performance)，但此系統晶片的介面是3.3伏，例如PCI-X的介面。因此，在第三章中，提出了應用在3.3伏的環境且利用1/2.5伏製程所實現的輸入電路和輸出電路。此外，一個新型的史密特觸發器(Schmitt Trigger)和電壓準位轉換器(Level Converter)分別被應用在所提出的輸入電路和輸出電路。本論文所提出應用在3.3伏環境的輸入電路和輸出電路已經在1/2.5伏0.13微米互補式金氧半製程裡實現並已在3.3伏的操作環境下驗證。

有別於傳統的混合電壓介面輸入輸出電路使用動態N阱偏壓電路和閘極電壓追蹤電路來避免漏電流以及閘極氧化層可靠度的問題。在第四章中，本論文提出了用N型金氧半場效電晶體(NMOS)阻隔的技巧來設計混合電壓介面輸入輸出電路。使用此N型金氧半場效電晶體阻隔的技巧不但

能設計出接收兩倍操作電壓輸入訊號的混合電壓介面輸入輸出電路，甚至可設計三倍、四倍、五倍操作電壓輸入訊號的混合電壓介面輸入輸出電路。其限制在於寄生 PN 接面(PN-Junction)的崩潰電壓(Breakdown Voltage)。利用所提出的 N 型金氧半場效電晶體阻隔的技巧所設計的接收兩倍操作電壓輸入訊號的混合電壓介面輸入輸出電路已經在 2.5 伏 0.25 微米互補式金氧半製程裡實現並在 2.5/5 伏的混合電壓介面下驗證。而利用所提出的 N 型金氧半場效電晶體阻隔的技巧所設計的接收三倍操作電壓輸入訊號的混合電壓介面輸入輸出電路已經在 1 伏 0.13 微米互補式金氧半製程裡實現並在 1/3 伏的混合電壓介面下驗證。

電荷幫浦電路(Charge Pump Circuit)是用來產生一個高於電源電壓(Power Supply Voltage)的輸出電壓。當利用低電壓元件來設計傳統的電荷幫浦電路時，將會發生嚴重的閘極氧化層可靠度問題。因此，在第五章中，本論文提出了一個新型的電荷幫浦電路，其避免了閘極電壓過高所造成的閘極氧化層可靠度問題。此外，本論文所提出的電荷幫浦電路有較好的效能(Performance)其輸出的漣波電壓(Output Voltage Ripple)也比傳統的電荷幫浦電路小。本論文所提出的電荷幫浦電路已經在 3.3 伏 0.35 微米互補式金氧半製程裡實現並驗證。

在互補式金氧半製程裡實現電荷幫浦電路，其輸出電壓將會被寄生 PN 接面的崩潰電壓所限制。此外，隨著互補式金氧半製程的進步，寄生 PN 接面的崩潰電壓也隨著降低。由於系統晶片的需求，在低電壓製程裡產生一個高電壓是必需的。因此，在第六章中，本論文提出了用多晶矽二極體(Polysilicon Diode)所實現的電荷幫浦電路。此多晶矽二極體利用淺溝隔絕層(Shallow Trench Isolation Layer)與基底(Substrate)相隔絕，所以流經此多晶矽二極體的電荷不會經由寄生 PN 接面的崩潰流失到基底。換句話說，本論文提出用多晶矽二極體所實現的電荷幫浦電路，其輸出電壓不會被寄

生 PN 接面的崩潰電壓所限制。此外，多晶矽二極體並不會增加額外的製程步驟，其與標準的互補式金氧半製程相容(Compatible)。本論文提出用多晶矽二極體所實現的電荷幫浦電路已經在 2.5 伏 0.25 微米標準互補式金氧半製程裡實現並驗證。其輸電壓遠高於寄生 PN 接面的崩潰電壓。

在本博士論文中提出數個在低電壓互補式金氧半製程下所設計的高電壓電路。所提出的電路已在實際晶片上成功驗証，並有相對應的國際會議論文、國際期刊論文發表與專利申請。

HIGH-VOLTAGE CIRCUIT DESIGN IN LOW-VOLTAGE CMOS PROCESSES

Student: Shih-Lun Chen **Advisor: Dr. Ming-Dou Ker**

Department of Electronics Engineering and Institute of Electronics
National Chiao Tung University

ABSTRACT

The scaling trend of the CMOS technology is toward the nanometer region to increase the speed and density of the transistors in integrated circuits. Due to the reliability issue, the power supply voltage is also decreased with the advanced technologies. However, in an electronic system, some circuits could be still operated at high voltage levels. If the circuits realized with low-voltage devices are operated at high voltage levels, the gate-oxide breakdown, hot-carrier degradation, leakage issues, and so on will occur. Therefore, designing the high-voltage circuits in low-voltage CMOS processes is an important topic in today and future VLSI (very large scale integration) design. In this dissertation, several circuits designed in low-voltage CMOS processes but operated in high-voltage environments are presented. There are seven chapters included in this dissertation.

Two new mixed-voltage I/O buffers realized with low-voltage devices are presented in Chapter 2 to prevent the undesired leakage current paths and the gate-oxide reliability problem, which occur in the conventional CMOS I/O buffer. These two new mixed-voltage I/O buffer have novel gate-tracking circuits and dynamic n-well bias circuits. Compared with the prior designs of mixed-voltage I/O buffers, these two new mixed-voltage I/O buffers occupy smaller silicon area. Besides, the new proposed mixed-voltage I/O buffer 2 can be applied for high-speed applications without the gate-oxide reliability problem and the circuit leakage issue. The new proposed mixed-voltage I/O buffers realized with 1×VDD devices

can be easily applied in 1×VDD/2×VDD mixed-voltage interface.

Due to the high-integration trend of SOC (system-on-a-chip), an electronic system may be integrated into a single chip. Hence, there are digital circuits and analog circuits integrated in a single chip. For example, the digital part of the SOC is designed with 1-V devices to decrease its power consumption, the analog part is designed with 2.5-V devices to improve the circuit performance, and the chip-to-chip interface is 3.3-V PCI-X in a 0.13-μm 1/2.5-V CMOS process. Thus, the traditional I/O circuits are not suitable for this application. An input buffer with the proposed Schmitt trigger circuit and an output buffer with the proposed level converter in a 0.13-μm 1/2.5-V CMOS process are presented in Chapter 3 for 3.3-V applications.

An NMOS-blocking technique for mixed-voltage I/O buffer design is presented in Chapter 4. Unlike the traditional mixed-voltage I/O buffer design, the mixed-voltage I/O buffer realized with only 1×VDD devices by using the NMOS-blocking technique can receive 2×VDD, 3×VDD, and even 4×VDD input signals without the gate-oxide reliability issue. In this dissertation, the 2×VDD input tolerant mixed-voltage I/O buffer by using the NMOS-blocking technique has been verified in a 0.25-μm 2.5-V CMOS process to serve 2.5/5-V mixed-voltage interface. The 3×VDD input tolerant mixed-voltage I/O buffer by using the NMOS-blocking technique has been verified in a 0.13-μm 1-V CMOS process to serve 1/3-V mixed-voltage interface. The NMOS-blocking technique can be extended to design the 4×VDD, 5×VDD, and even 6×VDD input tolerant mixed-voltage I/O buffers. The limitation of the NMOS-blocking technique is the breakdown voltage of the pn-junction in the given CMOS process.

A new charge pump circuit without the gate-oxide overstress is presented in Chapter 5. Because the charge transfer switches of the new proposed charge pump circuit can be fully turned on and turned off, as well as the output stage doesn't have the threshold drop problem, its pumping efficiency is higher than that of the prior designs. The gate-drain and the gate-source voltages of all devices in the new charge pump circuit don't exceed VDD, so the new charge pump circuit doesn't suffer the gate-oxide reliability problem. Besides, the proposed charge pump circuit has two pumping branches pumping the output node alternately so the output voltage ripple is small. The proposed circuit is suitable in low-voltage CMOS processes because of its high pumping efficiency and no overstress across the gate oxide of devices.

In general, the output voltage of the charge pump circuit will be limited by the breakdown voltage of the parasitic pn-junction in the given CMOS process. Chapter 6 presents an on-chip ultra-high-voltage charge pump circuit designed with the polysilicon diodes in low-voltage standard CMOS processes. Because the polysilicon diodes are fully isolated from the silicon substrate, the output voltage of the charge pump circuit is not limited by the junction breakdown voltage of parasitic pn-junction. The polysilicon diodes can be implemented in the standard (bulk) CMOS processes without extra process steps. The proposed charge pump circuit designed with the polysilicon diodes has been fabricated and verified in a 2.5-V 0.25-μm bulk CMOS process.

In summary, several circuits designed in low-voltage CMOS processes but operated in high-voltage environments are presented in this dissertation. The proposed circuits have been implemented and verified in silicon chips. The proposed circuits are very useful and cost-efficient for the advanced SOC applications.

E
S
A
1896

ACKNOWLEDGEMENTS

在交通大學電子研究所的生涯中，首先要感謝我的指導教授柯明道教授在這些年來耐心的指導與鼓勵，使我能順利完成博士學業。不只在專業領域上的知識，從柯教授認真的研究態度和嚴謹的處事原則，也讓我學習到克服困難、解決問題的正確態度與方法。此外，感謝307實驗室另外四位師長，吳重雨教授、吳錦川教授、吳介琮教授以及陳巍仁教授給我的指導與建議。

感謝黃弘一教授帶領我進入積體電路設計的殿堂，奠定了我在電路設計上的基礎。還有感謝周世傑教授、馬金溝博士、鄭國興教授在百忙之中抽空來擔任我的口試委員，給我指導跟建議，讓整個論文更加完整。

感謝廖以義博士，在我初來到交通大學時，給我許多生活、學業上的建議與幫助。還有謝謝其他307實驗室的成員陳東暘博士、林子超博士、施育全博士、周忠昀博士、徐國鈞博士、林坤賢博士，林俐如、周儒明、李瑞梅、范啟威、王文傑、范振麟、翟芸、陳榮昇、許勝福、鄧至剛、徐新智、蘇烜毅、虞繼堯、張瑋仁、曾偉信、顏承正、蕭淵文、李健銘、陳世宏、陳志豪、陳煒明、王暢資、王資閔等學長姐、同學、學弟們在課業、研究、生活上的幫忙與協助，讓我順利完成我的博士論文、並學習到做人處事上的態度與方法。此外，感謝歷任307實驗室的助理李婷媛小姐、卓慧貞小姐在實驗室行政事務上的許多協助。

致上最深的感謝給我親愛的家人們，祖母林玉雲女士、父親陳祐榮先生、母親鄭素嬌女士、弟弟陳亞倫、妹妹陳亞雯以及其他家人們。有了您們的支持、鼓勵、陪伴和照顧，才能讓我順利完成學業。還要謝謝女友鄭立欣小姐，一路上陪伴著我。最後謝謝所有幫助我、陪著我成長的人。謝謝你們。

陳世倫
誌於風城交大
95年夏

CONTENTS

TABLE CAPTIONS

FIGURE CAPTIONS

CHAPTER 1

Introduction

In this chapter, the background of this dissertation is discussed. First, the scaling trend of the CMOS technology is introduced. The reliability issue about the gate-oxide breakdown and the hot-carrier degradation in the advanced technology are also discussed. Then, the issues of the high-voltage circuits realized in low-voltage CMOS processes are discussed. Finally, the rest of this dissertation is organized.

1.1. Scaling Trend of CMOS Technology

The scaling trend of the CMOS technology is to increase the speed and density of the transistors in integrated circuits. The increase of speed requires the higher current density of the transistor due to the charge or discharge the load capacitance if the load capacitance is kept the same. Equation 1.1 expresses the drain current (I_d) of the NMOS transistor in the saturation region, where μ_n is the mobility of the NMOS transistor, C_{ox} is the gate capacitance per unit area of the NMOS transistor, W and L are the channel width and channel length of the NMOS transistor, Vt is the threshold voltage of the NMOS transistor, λ is the channel-length modulation parameter.

$$I_d = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (Vgs - Vt)^2 \cdot (1 - \lambda \cdot Vds) \tag{1.1}$$

If ignoring the channel-length modulation, equation 1.1 can be simplified as equation 1.2.

$$I_d = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (Vgs - Vt)^2 \tag{1.2}$$

Hence, the dimension and the threshold voltage of the devices are the key parameters as the semiconductor technology is scaled down. For speed consideration, the operation voltage of device is as high as possible to maximize the current density. However, the operation voltage of the device is decreased owing to the reliability issue. Table 1.1 summarizes the key features of the semiconductor scaling trend, which are predicted by the Semiconductor Industry Association (SIA) [1]. As shown in Table 1.1, the gate length (L), the threshold voltage (Vt), and the thickness (t_{ox}) of the gate oxide are decreased in the future technologies so the drain current is increased. However, due to the reliability issue, the power supply voltage is decreased in the future technologies. Although the scaling trend is toward to increase the speed and the density of transistor, the reliability issue becomes more responsible in the future technologies. Because the thickness of gate oxide is getting thinner and thinner, and the channel length is getting shorter and shorter in the future technologies, the gate-oxide breakdown [2]-[5] and hot-carrier degradation [6], [7] issues become more important.

1.1.1. Gate-Oxide Breakdown

The thinner gate oxide is required in the advanced processes due to the current density of the device. If the other device dimensions are scaled down and the gate oxide is kept the same, the device suffers from the short-channel effect. However, the larger electric field is across the gate oxide if the thickness of the gate oxide is scaled down and the operation voltage is not. The large electric field on the gate oxide may cause the gate-oxide breakdown. The gate oxide can be broken down instantaneously or broken down over time [8], [9]. Equation 1.3 expresses the lifetime of gate oxide over the voltage stress [8].

$$\frac{1}{\tau_0}\int_0^{t_{BD}} \exp\left(-\frac{G\cdot X_{eff}}{V_{ox}(t)}\right)\cdot dt = 1 \tag{1.3}$$

In equation 1.3, τ_0 and G are two constants, X_{eff} is the effective thickness of the gate oxide due to the defeats, and $V_{ox}(t)$ is the time-dependent voltage across the gate oxide. As expressed in equation 1.3, the accumulation of the voltage stress over time determines the gate-oxide breakdown. Thus, the DC stress is more serious than the AC stress (transient stress). For the DC stress and the defeat-free gate oxide, equation 1.3 can be simplified as equation 1.4, where t_{ox} is the thickness of the gate oxide.

$$t_{BD} = \tau_0 \cdot \exp\left(\frac{G\cdot t_{ox}}{V_{ox}}\right) \tag{1.4}$$

As expressed in equation 1.4, the operating voltage of devices must be scaled down to keep the same life time when the gate-oxide thickness is scaled down to improve the performance.

1.1.2. Hot-Carrier Degradation

As the semiconductor technology has been scaled down, the channel length of the device becomes shorter. If the drain-source voltage is not scaled down with the channel length, the electric field between the drain and the source is large so that the electrons in the channel are accelerated to damage the device. The damage by the accelerated electrons degrades the device performance over time or causes the device breakdown instantaneously. Similar to the gate-oxide overstress, the AC hot-carrier stress (transient stress) is less harmful than the DC stress. Lightly doped drain (LDD) structure is used in the advanced processes to allow the higher drain-source voltage without the hot-carrier degradation [10]-[13]. However, the LDD structure increases the series drain resistance, which degrades the speed performance. Thus, the power supply voltage (VDD) maximizes the speed for a fixed reliability level.

As described in sections 1.1.1 and 1.1.2, the power supply voltage (VDD) for a CMOS technology is a trade-off of the speed performance, the power consumption, and the reliability issue. For speed performance, the higher supply voltage makes the device having the larger drain current to charge and to discharge the capacitive load. The gate-oxide breakdown over time and hot-carrier stress set the maximum supply voltage.

1.2. Issues of High-Voltage Circuit Design in Low-Voltage CMOS Processes

The device dimension of transistor has been scaled toward the nanometer region and the power supply voltage of chips in the nanoscale CMOS technology has been also decreased due to the reliability and power consumption issues [1]. Obviously, the shrunk device dimension makes the chip area smaller to save silicon cost. The lower power supply voltage (VDD) results in lower power consumption. Therefore, chip design quickly migrates to the lower voltage level with the advancement of the nanoscale CMOS technology. Fig. 1.1 shows the scaling trends of the power supply voltage (VDD) and the oxide thickness (t_{ox}) [1]. As shown in Fig. 1.1, the power supply voltage is decreased and the oxide thickness is thinner when the process is scaled down. However, in order to save the chip area or have the speed performance, some circuits are still designed in the same voltage level but fabricated in the advanced (low-voltage) processes [14]-[18]. Besides, some peripheral components or other ICs in an electronic system are still operated at the higher voltage levels, such as 3.3 V or 5 V [19], [20]. In other words, an electronic system could have chips operated at different voltage levels. Thus, some circuits must be design in low-voltage process, but still operated in the high-voltage or mixed-voltage (high-voltage and low-voltage) environments. However, the gate-oxide breakdown, the hot-carrier degradation, and the leakage current issues may arise in the low-voltage circuits operated in the high-voltage or mixed-voltage environment.

Figs. 1.2 and 1.3 show a CMOS inverter and an NMOS load amplifier realized with low-voltage (2.5-V) devices but operated in high-voltage (5-V) environment, respectively. As shown in Fig. 1.2, transistors MP and MN have the overstress on their gate oxides anytime, and the hot-carrier stress during the signal transitions in the high-voltage environment. As shown in Fig. 1.3, transistors MN1 and MN2 have the gate-oxide overstress and hot-carrier overstress anytime in the high-voltage environment. Fig. 1.4 shows two inverters realized with 2.5-V devices in mixed-voltage (2.5/5-V) interface. As shown in Fig. 1.4, transistors MP2 and MN2 have the gate-oxide overstress and hot-carrier overstress in the mixed-voltage interface. Besides, a leakage path occurs from 5-V power supply to ground through transistors MP2 and MN2. Thus, the circuits realized with the low-voltage devices in the high-voltage or mixed-voltage environment must be designed carefully to prevent the gate-oxide breakdown, the hot-carrier degradation, and the leakage current issues. Some circuits designed with low-voltage devices but applied in high-voltage environment have been reported. Reference [14] has reported a CMOS operational amplifier (OPAMP) fabricated in a 0.13-μm 1-V CMOS process but operated with 2.5-V power supply (VDD=2.5 V) without gate-oxide reliability issue. The analog-to-digital converters (ADCs) realized with low-voltage devices without gate-oxide reliability issue have been reported in [21], [22]. In [15], [16], I/O circuits realized in a 0.25-μm 2.5-V CMOS technology are operated with the power supply voltage of 5.5 V and 7.5 V without gate-oxide overstress, respectively. In [17], a 5.5-V line driver fabricated in a 0.13-μm 1.2-V CMOS technology has been reported. Reference [18] has reported a high-voltage charge pump circuit realized with low-voltage devices without gate-oxide reliability. In [23]-[25], the I/O buffers realized in low-voltage processes for mixed-voltage applications without reliability and leakage issues have been reported. Therefore, in this dissertation, several high-voltage circuits realized with low-voltage devices are presented.

1.3. Organization of This Dissertation

In Chapter 2, a new mixed-voltage I/O buffer realized with only the thin gate-oxide (low-voltage) devices is presented. The new proposed mixed-voltage I/O buffer with simpler dynamic n-well bias circuit and gate-tracking circuit can prevent the undesired leakage current paths and the gate-oxide reliability problem, which occur in the conventional CMOS I/O buffer. The new mixed-voltage I/O buffer has been fabricated and verified in a 0.25-µm 2.5-V CMOS process to serve 2.5/5-V I/O interface. Besides, another 2.5/5-V mixed-voltage I/O buffer without the subthreshold leakage problem for high-speed applications is also presented in this chapter. The speed, power consumption, area, and noise among these mixed-voltage I/O buffers are also compared and discussed. The new proposed mixed-voltage I/O buffers realized with 1×VDD devices can be easily applied in 1×VDD/2×VDD mixed-voltage interface.

In Chapter 3, an input buffer and an output buffer realized with 1-V and 2.5-V low-voltage devices for 3.3-V applications are presented. Due to the high-integration trend of SOC (system-on-a-chip), an electronic system may be integrated into a single chip. Thus, there are digital circuits and analog circuits in a chip. For example, the digital part of a chip is designed with 1-V devices to decrease its power consumption, the analog part is designed with 2.5-V devices to improve the circuit performance, and the chip-to-chip interface is 3.3-V PCI-X in a 0.13-µm 1/2.5-V CMOS process. Thus, the traditional I/O circuits are not suitable for this application. An input buffer with the proposed Schmitt trigger circuit in a 0.13-µm 1/2.5-V CMOS process is presented first. Then, an output buffer with the proposed level converter in a 0.13-µm 1/2.5-V CMOS process is also presented in this chapter.

Chapter 4 presents an NMOS-blocking technique for mixed-voltage I/O buffer. Unlike the traditional mixed-voltage I/O buffer design, the mixed-voltage I/O buffer realized with only 1×VDD devices by using the NMOS-blocking technique can receive 2×VDD, 3×VDD, and even 4×VDD input signal without the gate-oxide reliability issue. In this chapter, the 2×VDD input tolerant mixed-voltage I/O buffer by using the NMOS-blocking technique has been verified in a 0.25-µm 2.5-V CMOS process to serve 2.5/5-V mixed-voltage interface. The 3×VDD input tolerant mixed-voltage I/O buffer by using the NMOS-blocking technique has been verified in a 0.13-µm 1-V CMOS process to serve 1/3-V mixed-voltage interface. The proposed NMOS-blocking technique can be extended to design the 4×VDD, 5×VDD, and even 6×VDD input tolerant mixed-voltage I/O buffers. The limitation of the NMOS-blocking technique is the breakdown voltage of the pn-junction in the given CMOS process.

Chapter 5 presents a new charge pump circuit with consideration of gate-oxide reliability issue. Because the charge transfer switches of the new proposed charge pump circuit can be fully turned on and turned off, as well as the output stage doesn’t have the threshold drop problem, its pumping efficiency can be higher than that of the prior designs. The gate-drain and the gate-source voltages of all devices in the proposed charge pump circuit don’t exceed VDD, so the proposed charge pump circuit doesn’t suffer the gate-oxide reliability problem. Besides, the proposed charge pump circuit has two pumping branches pumping the output node alternately so the output voltage ripple is small. In this work, two test chips have been implemented in a 0.35-µm 3.3-V CMOS process to verify the proposed charge pump circuit. The measured output voltage of the new proposed 4-stage charge pump circuit with each pumping capacitor of 2 pF to drive the capacitive output load is around 8.8 V under 3.3-V power supply (VDD=3.3 V), which is limited by the junction breakdown voltage of the parasitic pn-junction in the given process. The new proposed circuit is suitable for applications in low-voltage CMOS processes because of its high pumping efficiency and no overstress across the gate oxide of devices.

Chapter 6 presents an on-chip ultra-high-voltage charge pump circuit designed with the polysilicon diodes in low-voltage standard CMOS processes. Because the polysilicon diodes are fully isolated from the silicon substrate, the output voltage of the charge pump circuit is not limited by the junction breakdown voltage of MOSFETs. The polysilicon diodes can be implemented in the standard (bulk) CMOS processes without extra process steps. The proposed ultra-high-voltage charge pump circuit has been fabricated in a 0.25-µm 2.5-V standard CMOS process. The measured output voltage of the 12-stage charge pump circuit with 2.5-V power supply voltage (VDD=2.5 V) can be pumped up to 28.08 V, which is much higher than the n-well/p-substrate breakdown voltage (~18.9 V) in the 0.25-µm 2.5-V standard CMOS process.

Chapter 7 summarizes the main results of this dissertation. Then, some suggestions for the future works are also addressed in this chapter.

Table 1.1

Key Features of the Semiconductor Scaling Trend

(High-Performance Logic Technology) [1]

	2005	2006	2007	2008	2009	2010	2011	2012
Gate Length, L (nm)	32	28	25	22	20	18	16	14
Oxide Thickness, t_{ox} (Å)	12	11	11	9	7.5	6.5	5	5
Power Supply Voltage, VDD (V)	1.1	1.1	1.1	1	1	1	1	0.9
Threshold Voltage, Vt (mV)	195	168	165	160	159	151	146	148
NMOS Drain Current (μA/μm)	1020	1130	1200	1570	1810	2050	2490	2300

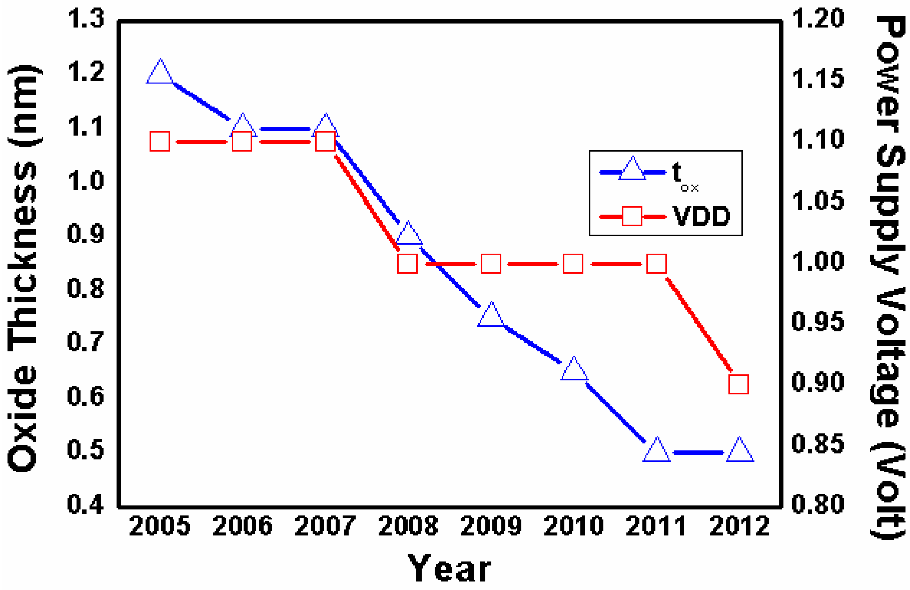


Fig. 1.1. Scaling trends of the oxide thickness and the power supply voltage [1].

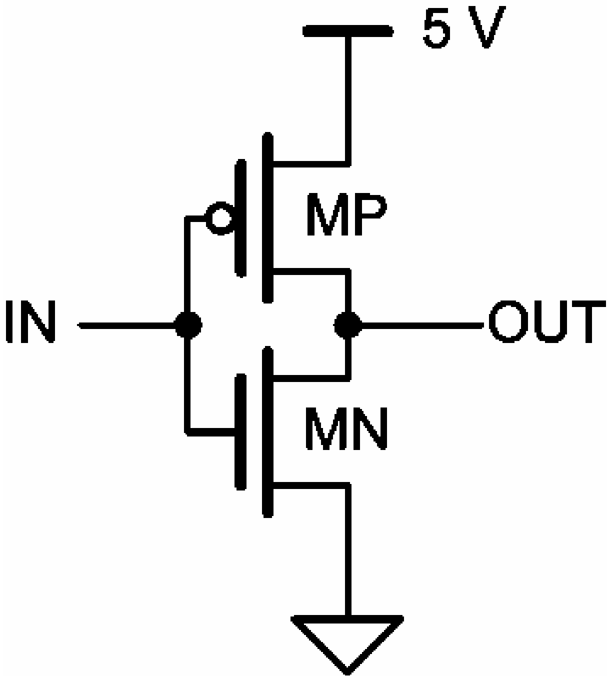


Fig. 1.2. A CMOS inverter realized with 2.5-V devices in 5-V environment.

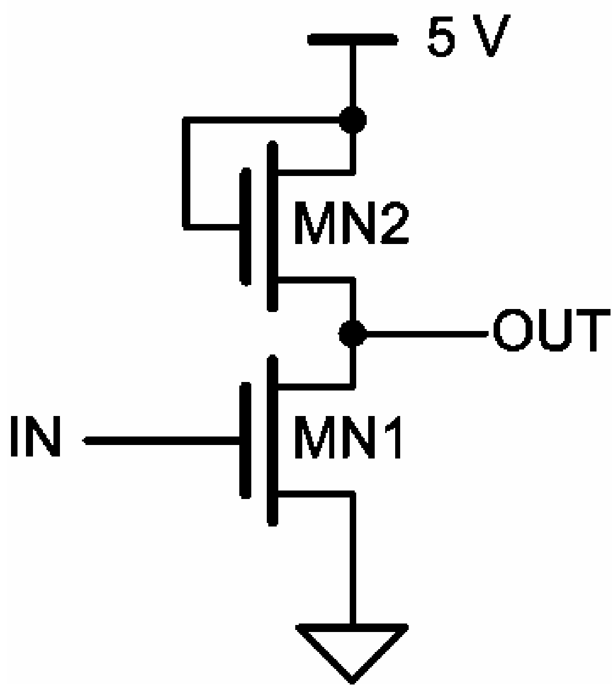


Fig. 1.3. An NMOS load amplifier realized with 2.5-V devices in 5-V environment.

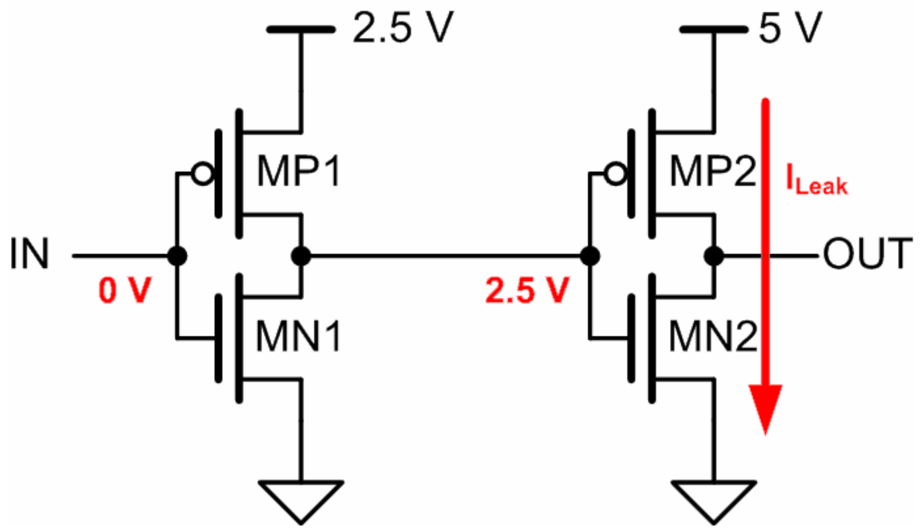


Fig. 1.4. Two CMOS inverters realized with 2.5-V devices in 2.5/5-V mixed-voltage interface.

CHAPTER 2

Mixed-Voltage I/O Buffers With Only Thin Gate-Oxide Devices

In this chapter, the prior designs of mixed-voltage I/O buffers are overviewed first. Then, two new mixed-voltage I/O buffers realized with only thin-oxide devices are presented [26]. The new proposed mixed-voltage I/O buffer 1 with simpler dynamic n-well bias circuit and gate-tracking circuit can prevent the undesired leakage current paths and the gate-oxide reliability problem, which occur in the conventional CMOS I/O buffer. The new mixed-voltage I/O buffer 1 has been fabricated and verified in a 0.25-μm CMOS process to serve 2.5/5-V I/O interface.

The subthreshold leakage problem is more serious in the advanced CMOS processes, such as the 0.13-μm CMOS process. Therefore, the new proposed mixed-voltage I/O buffer 2 for high-speed applications is also presented to alleviate this problem. The speed, power consumption, area, and noise among these mixed-voltage I/O buffers (new proposed circuits and prior arts) are also compared and discussed. The new proposed mixed-voltage I/O buffers realized with 1×VDD devices can be easily applied in 1×VDD/2×VDD mixed-voltage interface.

2.1. Issues of Mixed-Voltage I/O Interface

The conventional tri-state I/O buffer with 2.5-V gate-oxide devices in a 0.25-μm CMOS process is shown in Fig. 2.1, where the power supply voltage (VDD) is 2.5 V. However, the input signal at the I/O pad in the mixed-voltage I/O interface may rise up to 5 V in the tri-state input (receive) mode. In the receive mode, the gate voltages of the pull-up PMOS device and the pull-down NMOS device in the I/O buffer are traditionally controlled at 2.5 V and 0 V to turn off the pull-up PMOS device and the pull-down NMOS device by the pre-driver circuit, respectively. When the input signal at the I/O pad rises up to 5 V in the tri-state input mode, the parasitic drain-to-well pn-junction diode in the pull-up PMOS device will be forward biased. Therefore, an undesired leakage current path flows from the I/O pad to the power supply voltage (VDD) through the parasitic pn-junction diode. Besides, because the gate voltage of the pull-up PMOS device is 2.5 V and the input signal at I/O pad is 5 V, the pull-up PMOS device will be turned on in such tri-state input mode to conduct another undesired leakage current path from the I/O pad to the power supply voltage (VDD). Such undesired leakage currents cause not only more power consumption in the electronic system but also malfunction in the whole electronic system.

Moreover, because the gate-drain voltage (Vgd) of the pull-down NMOS device and the gate-source voltage (Vgs) of the input buffer in Fig. 2.1 with 5-V input signal are larger than their voltage levels in the normal operation, such high voltage across the thin gate oxide of the pull-down NMOS device and the input buffer results in the gate-oxide overstress reliability issue [27]-[29]. In addition, the pull-down NMOS device and the input buffer with a 5-V input signal may suffer serious hot-carrier degradation if their drain-source voltages are too large [13].

Fig. 2.2 shows the mixed-voltage I/O buffer with the dual-oxide (thick-oxide and thin-oxide) devices and an external n-well bias voltage. For such mixed-voltage interface applications, the dual-oxide process provided by foundry is used to avoid the gate-oxide reliability problem [30]-[32]. Since the thick oxide can sustain higher gate voltage, the devices which have the gate-oxide reliability problem can be replaced by the thick-oxide devices to prevent the high-voltage overstress on the thin gate oxide. Therefore, the core circuits in a chip are designed with thin-oxide devices to decrease the chip area and power consumption, but the I/O circuits are designed with thick-oxide devices to avoid the gate-oxide reliability issue. In order to avoid leakage current path from the I/O pad to the power supply (VDD) through the parasitic drain-to-well pn-junction diode in the pull-up PMOS device, the body terminal of the pull-up PMOS must be connected to an extra pad that provides a higher external voltage (VDDH) to bias the body of the pull-up PMOS device. In addition, a gate-tracking circuit is needed to avoid the leakage current path induced by the incorrect conduction of the pull-up PMOS device.

Although the traditional mixed-voltage I/O buffer with dual-oxide devices and an external n-well bias can be used to solve the aforementioned problems, there are still some limitations in this I/O buffer. Using an external bias voltage needs an extra pad to provide another power supply (VDDH), the silicon area and the cost of the whole system are increased. The threshold voltage of the thick-oxide devices is so high that their driving capacities are decreased when their gates are controlled by the pre-driver circuit with low-voltage devices. In addition, because the body terminal of the pull-up PMOS device is connected to a higher voltage (VDDH), the threshold voltage of the pull-up PMOS device is also increased due to the body effect. Because the driving capacity is decreased, the larger device dimension is required for the pull-up PMOS device to support the desired driving specifications. In turn, it increases the silicon area for such I/O buffer. Therefore, the mixed-voltage I/O buffer with dual-oxide devices and an external n-well bias is unsuitable for the low-cost commercial ICs. Considering these limitations, several mixed-voltage I/O buffers have been reported in [23]-[25], [33], [34], which will be overviewed in this chapter.

2.2. Overview on the Prior Designs of Mixed-Voltage I/O Buffers

2.2.1. Design Concept of Mixed-Voltage I/O Buffers With Thin-Oxide Devices

Fig. 2.3 shows the mixed-voltage I/O buffer realized with thin-oxide devices, a dynamic n-well bias circuit, and a gate-tracking circuit. The stacked NMOS devices, MN0 and MN1, are used to avoid the high-voltage overstress on their gate oxide. In a 0.25-µm CMOS process, the power supply voltage (VDD) is 2.5 V and the threshold voltage of the devices is about 0.6 V. Because the gate terminal of transistor MN0 is connected to 2.5 V (VDD), the drain voltage of transistor MN1 is about 1.9 V (2.5–0.6=1.9) when the input signal at the I/O pad is 5 V in the tri-state input mode. Hence, the gate-drain voltages and the gate-source voltages of the stacked NMOS devices, MN0 and MN1, are limited below 2.5 V even if the input signal at the I/O pad is 5 V. Therefore, the stacked NMOS devices, MN0 and MN1, can solve the gate-oxide reliability problem.

The gate-tracking circuit shown in Fig. 2.3 is used to prevent the leakage current path due to the incorrect conduction of the pull-up PMOS device when the input signal at the I/O pad is higher than VDD. In the transmit mode, the gate-tracking circuit must transfer the signal from the pre-driver circuit to the gate terminal of the pull-up PMOS device exactly. In the tri-state input mode (receive mode) with 5-V input signal, the gate-tracking circuit will charge the gate terminal of the pull-up PMOS device to 5 V to turn off the pull-up PMOS device completely, and to avoid the leakage current from the I/O pad to the power supply (VDD). On the contrary, the gate-tracking circuit will keep the gate terminal of the pull-up PMOS device at 2.5 V to turn off the pull-up PMOS device completely, and to prevent the overstress on the gate oxide of the pull-up PMOS device, when the input signal at the I/O pad is 0 V in the tri-state input mode.

The dynamic n-well bias circuit shown in Fig. 2.3 is designed to prevent the leakage current path due to the parasitic drain-to-well pn-junction diode in the pull-up PMOS device. In the transmit mode, the dynamic n-well bias circuit must keep the floating n-well bias at 2.5 V. So, the threshold voltage of the pull-up PMOS device isn't increased by the body effect. In the tri-state input mode with a 5-V input signal, the dynamic n-well bias circuit will charge the floating n-well to 5 V to prevent the leakage current from the I/O pad to the power supply (VDD) through the parasitic pn-junction diode. When the input signal at the I/O pad is 0 V, the dynamic n-well bias circuit will bias the floating n-well at 2.5 V.

Because the floating n-well is clamped to 2.5 V or 5 V through the parasitic diodes by some dynamic n-well bias circuits [24], [33], [34], the voltage on the floating n-well will be a little lower than 2.5 V or 5 V. The lower floating n-well voltage results in the lower threshold voltage of the pull-up PMOS transistor. Thus, the subthreshold leakage current becomes large when the pull-up PMOS transistor is in off state. If the given process has serious subthreshold leakage issue, such as the 0.13-μm or below processes, the dynamic n-well bias circuit must clamp the floating n-well directly to the desired voltage level by the MOS transistor to decrease the subthreshold leakage.

As shown in Fig. 2.3, the extra transistors, MN2 and MP1, are added in the input buffer. Transistor MN2 is used to limit the voltage level of input signal reaching to the gate oxide of inverter INV. Because the gate terminal of transistor MN2 is connected to the power supply voltage (VDD), the input terminal of inverter INV will rise up to 1.9 V (2.5–0.6=1.9) when the input signal at the I/O pad is 5 V in the tri-state input mode. Then, transistor MP1 is used to pull up the input node of inverter INV to 2.5 V when the output node of inverter INV is pulled down to 0 V. Thus, the gate-oxide reliability occurring in the input buffer can be solved.

2.2.2. Prior Designs of Mixed-Voltage I/O Buffers

Fig. 2.4 re-draws the mixed-voltage I/O buffer with stacked pull-up PMOS devices reported in [33]. Signal OE is the output-enable control signal. In the transmit mode, transistor MN1 is turned on and transistor MP2 is turned off, so that this I/O buffer drives the I/O pad according to the output signal Dout. In the tri-state input mode, transistor MN1 is turned off and transistor MP2 is turned on by the control signal OE at logic zero. If the input signal at the I/O pad is 5 V, the gate voltage of transistor MP1 and the floating n-well are pulled up to 5 V through transistor MP2 and the parasitic drain-to-well pn-junction diode in transistor MP0 to prevent the undesired leakage current paths from I/O pad to power supply voltage (VDD), respectively. Although this I/O buffer is simple, transistors MN0, MN1, and MP2 have the gate-oxide reliability problem in the tri-state input mode when the input signal has a 5-V voltage level. Besides, because the stacked PMOS devices with the floating n-well to prevent the leakage current is applied to this I/O buffer, the PMOS devices in stacked configuration occupy more silicon area.

Fig. 2.5 re-draws another mixed-voltage I/O buffer with stacked pull-up PMOS devices and stacked pull-down NMOS devices [34]. This I/O buffer uses transistors MP2, MN3, and MN4 as the gate-tracking circuit and transistors MP0, MP3, and MP4 as the dynamic n-well bias circuit. In the tri-state input mode with the control signal OE at GND, transistor MN4 is turned off and transistor MP2 is turned on. If the input signal at the I/O pad is 5 V, the gate voltage of transistor MP3 is biased at 5 V through transistors MP0 and MP2 to avoid the undesired leakage current path due to the incorrect conduction of transistor MP3. The floating n-well is biased at ~5 V through the parasitic drain-to-well pn-junction diode of transistor MP0. In the transmit mode with the OE control signal at VDD, transistor MN4 is turned on so that transistor MP3 is turned on, and transistor MP2 is kept off. Hence, this I/O buffer drives the I/O pad according to the output signal Dout. When the signal at the I/O pad is 0 V, the floating n-well is biased at 2.5 V through transistor MP4. When the input signal at the I/O pad is 2.5 V, the floating n-well is biased at ~2.5 V through the parasitic source-to-well pn-junction diodes of transistors MP3 and MP4. However, transistor MP2 has the gate-oxide reliability problem when the input signal at the I/O pad is 5 V in the tri-state mode. Besides, because the I/O buffer uses two PMOS devices, MP0 and MP3, in stacked configuration to drive the I/O pad, the stacked devices occupy more silicon area.

The mixed-voltage I/O buffer with a depletion PMOS device is re-drawn in Fig. 2.6 [23]. The depletion PMOS device MP2 in the I/O buffer is used as the gate-tracking circuit. In the tri-state mode, if the input signal at I/O pad is 5 V, the gate voltage of transistor MP0 is biased at 5 V through the depletion PMOS device MP2 to avoid the undesired leakage current path through the transistor MP0. This I/O buffer uses an extra pad that is connected to 5-V power supply (VDDH) to avoid the undesired leakage current path through the parasitic drain-to-well pn-junction diode. However, using the depletion device increases mask layer and process modification. Thus, the fabrication cost of such I/O buffer design will be increased. In addition, using the extra n-well bias (VDDH) not only degrades the driving capacity of output device MP0 due to the body effect, but also increases the system cost.

Fig. 2.7 re-draws the mixed-voltage I/O buffer realized with only thin-oxide devices reported in [24]. In Fig. 2.7, the gate-tracking circuit and the dynamic n-well bias circuit are formed by transistors MP1, MP2, MP3, MP4, MN2, MN3, MN4, and MN5. In the transmit mode with signal OE at logic “1”, transistor MN4 is turned on to keep transistors MP3 and MP4 on. Thus, this I/O buffer drives the I/O pad according to signal Dout. Besides, because transistor MP3 is turned on, the floating n-well is biased at 2.5 V by transistor MP3 in the transmit mode. In the tri-state input mode with signal OE at logic “0”, transistor MN4 is kept off. If the input signal at the I/O pad is 5 V, the gate voltages of transistors MP0 and MP4 are biased at 5 V through transistor MP1 and MP2 to avoid the undesired leakage paths through the transistors MP0 and MP4. Besides, the floating n-well is also biased at ~5 V to avoid the undesired leakage path through the parasitic drain-to-well pn-junction diode of transistor MP0 when the voltage at the I/O pad is 5 V in tri-state input mode. When the input signal at the I/O pad is 0 V in the tri-state input mode, transistor MN3 is turned on to keep transistor MP3 on. So, the floating n-well is biased at 2.5 V.

Another mixed-voltage I/O buffer realized with only thin-oxide devices is re-drawn in Fig. 2.8 [25]. The gate-tracking circuit in Fig. 2.8 is composed of transistors MN3, MN4, MP2, MP3, and MP4. The dynamic n-well bias circuit in Fig. 2.8 is formed by transistors MN5, MP5, MP6, and MP7. Besides, the body terminals of all PMOS transistors in the gate-tracking circuit and the dynamic n-well bias circuit are connected to the floating n-well. Such I/O circuit shown in Fig. 2.8 can overcome the gate-oxide reliability problem and avoid the undesired leakage paths. However, too many devices are used to realize the desired functions of the gate-tracking circuit and the dynamic n-well bias circuit. More devices used in the mixed-voltage I/O buffer often cause more complex metal routing connection in the I/O cells.

2.3. New Mixed-Voltage I/O Buffer 1

2.3.1. Circuit Implementation

Fig. 2.9 shows the new proposed mixed-voltage I/O buffer with the new dynamic n-well bias circuit and gate-tracking circuit. The new proposed I/O buffer is realized by only the thin gate-oxide devices, and occupies smaller silicon area than the prior designs of mixed-voltage I/O buffers. When the tri-state control signal OE is at 2.5 V (logic “1”), the new mixed-voltage I/O buffer is operated in the transmit mode. The signal at the I/O pad rises or falls according to signal Dout, which is controlled by the internal circuits of IC. The lower output port of the pre-driver circuit is directly connected to the gate terminal of the pull-down NMOS device, MN1. The upper output port of the pre-driver circuit is connected to the gate terminal of the pull-up PMOS device, MP0, through the gate-tracking circuit. If the voltage level at the upper port is 0 V, the signal can be fully transmitted to the gate terminal of the pull-up PMOS device MP0 through transistor MN2, and the signal at the I/O pad is pulled up to 2.5 V. Besides, transistor MP4 is also turned on to bias the floating n-well at 2.5 V. When the voltage level at the upper port is 2.5 V, the gate terminal of transistor MP0 is charged to VDD–|Vtp| through transistor MN2 first. Consequently, the voltage at the I/O pad and the gate voltage of transistor MP1 are discharged to 0 V through transistors MN0 and MN1. Transistor MP1 is turned on until the gate terminal of transistor MP2 is discharged to |Vtp|. At this moment, transistor MP2 is turned on to continually pull the gate voltage of transistor MP0 up to 2.5 V. The pull-up PMOS device MP0 can be completely kept off. The floating n-well is also biased at ~2.5 V through the parasitic pn-junction diodes of transistors MP0 and MP4 at this moment.

When the proposed I/O buffer is operated in the tri-state input (receive) mode, the upper and lower output ports of the pre-driver circuit are kept at 2.5 V and 0 V, respectively, to turn off transistors MP0 and MN1. Signal Din rises or falls according to the signal at the I/O pad in the tri-state input mode. In order to prevent the undesired leakage current from the I/O pad to the power supply (VDD) through the pull-up PMOS device MP0, transistor MP3 is used to track the signal at the I/O pad and to control the gate voltage of transistor MP0. When the voltage level at the I/O pad exceeds VDD+|Vtp|, such as 5 V, transistor MP3 is turned on to charge the gate terminal of transistor MP0 up to 5 V. Transistor MP0 is completely turned off to prevent the leakage current through its channel. Transistor MP4 is also turned off and the floating n-well is biased at 5 V through the parasitic pn-junction diode. Thus, there is no leakage current path from the I/O pad to the power supply (VDD). Besides, transistor MP1 is also turned on to keep transistor MP2 off in order to prevent another leakage path from the gate terminal of transistor MP0 to the upper port of the pre-driver, when the signal at the I/O pad is 5 V.

Transistors MN0 and MP5 with inverter INV are used to transfer the input signal from the I/O pad to the internal node Din in the tri-state input mode. Transistor MN0 is used to limit the voltage level of input signal reaching to the gate oxide of inverter INV. Because the gate terminal of transistor MN0 is connected to the power supply voltage (2.5 V), the input voltage of inverter INV is limited to 1.9 V (2.5–0.6=1.9) when the voltage level at the I/O pad is 5 V. Then, transistor MP5 will pull the input node of inverter INV up to 2.5 V when the output node of inverter INV is pulled down to 0 V. The signal at the I/O pad can be successfully transferred to the internal input node Din. This I/O buffer can be correctly operated with neither gate-oxide reliability problem nor any circuit leakage issue in the tri-state input mode.

2.3.2. Simulation and Experimental Results

A 0.25-µm 2.5-V CMOS device model is used to verify the design of the new proposed mixed-voltage I/O buffer by HSPICE simulation. Figs. 2.10(a) and 2.10(b) show the simulated waveforms of the new proposed mixed-voltage I/O buffer with a 20-pF output load at the pad and 50-MHz I/O signal in the transmit mode and in the tri-state input mode, respectively. As shown in Fig. 2.10(a), the new proposed mixed-voltage I/O buffer can successfully drives the I/O pad according to signal Dout in the transmit mode. As shown in Fig. 2.10(b), the new proposed mixed-voltage I/O buffer can successfully transfer the signal at the I/O pad to the signal Din when it receives the 5-V signals in the tri-state input mode. This simulation also verifies that the gate-drain voltages (Vgd) and gate-source voltages (Vgs) of all devices in the new proposed mixed-voltage I/O buffer do not exceed 2.5 V. Fig. 2.10(b) only shows the gate-drain voltage (Vgd) of the pull-up PMOS device MP0. With the new gate-tracking circuit, the Vgd of the pull-up PMOS device MP0 is always controlled within the normal operation voltage (VDD). Thus, the gate-tracking circuit can solve the gate-oxide reliability problem in the new proposed mixed-voltage I/O buffer.

Fig. 2.11 shows the die photograph of the new proposed mixed-voltage I/O buffer fabricated in a 0.25-µm 2.5-V 1P5M CMOS process. The measured waveforms of the new proposed mixed-voltage I/O buffer with 1-MHz I/O signal in the transmit mode, the tri-state input mode with 2.5-V input, and the tri-state input mode with 5-V input are shown in Figs. 2.12(a), 2.12(b), and 2.12(c), respectively. As shown in Figs. 2.12(a), 2.12(b), 2.12(c), the new proposed mixed-voltage I/O buffer can be successfully operated in such a 2.5/5-V mixed-voltage I/O environment. The maximum operation frequency of the proposed I/O buffer depends on the output load and the device size of output circuit. Typically, the proposed mixed-voltage I/O buffer in this work has been successfully verified in silicon that can be operated up to 200 MHz with 20-pF load.

2.4. New Mixed-Voltage I/O Buffer 2

2.4.1. Circuit Implementation

The floating n-well of the proposed mixed-voltage I/O buffer 1 in Fig. 2.9 is biased at ~2.5 V and ~5 V through the parasitic pn-junction diode in the transmit mode with 0-V output signal and in the receive mode with 5-V input signal, respectively. Thus, the voltage level of the floating n-well may be coupled with transient noise when the operating frequency of the mixed-voltage I/O buffer becomes higher. The lower floating n-well voltage results in the lower threshold voltage (Vtp) of the pull-up PMOS, so that the subthreshold leakage current becomes large when the pull-up PMOS is in off state. Considering the coupled noise and the subthreshold leakage current issue due to the floating n-well, another new modified design of the proposed mixed-voltage I/O buffer without n-well floating is shown in Fig. 2.13. Comparing to the design in Fig. 2.9, the gate of transistor MP4 in Fig. 2.13 is connected to the gate of transistor MP2. Besides, two extra NMOS devices, MN3 and MN4, are added to pull the gate voltage of transistor MP4 to 0 V when the I/O buffer in Fig. 2.13 is operated in the transmit mode. In Fig. 2.13, transistor MN3 is used to protect transistor MN4 without the gate-oxide overstress, because the gate voltage of transistor MP4 may be as high as 5 V in the tri-state input mode. In the transmit mode, the gate voltage of transistor MP4 in Fig. 2.13 is pulled down to 0 V through transistors MN3 and MN4. Transistor MP4 is always turned on to bias the floating n-well at 2.5 V whenever the signal at I/O pad is 2.5 V or 0 V. In the receive mode with 5-V input signal, another PMOS device MP6 is turned on to bias the floating n-well at 5 V. Thus, whenever the proposed mixed-voltage I/O buffer 2 is in the transmit mode or the receive mode, the floating n-well is biased at 2.5 V or 5 V directly. The subthreshold leakage problem can be completely solved in the new proposed mixed-voltage I/O buffer 2.

2.4.2. Simulation Results

The proposed mixed-voltage I/O buffer 2 is also simulated in a 0.25-μm 2.5-V CMOS process. Figs. 2.14(a) and 2.14(b) show the simulated waveforms of the proposed mixed-voltage I/O buffer 2 operating in the transmit mode and the tri-state input mode, respectively. As shown in Figs. 2.14(a) and 2.14(b), the new proposed mixed-voltage I/O buffer 2 can be operated correctly in the transmit mode and the tri-state input mode. Figs. 2.15(a) and 2.15(b) compare the simulated waveforms on the floating n-wells of the proposed mixed-voltage I/O buffer 1 (Fig. 2.9) and the proposed mixed-voltage I/O buffer 2 (Fig. 2.13) in the transmit mode and in the receive mode, respectively. As shown in Figs. 2.15(a) and 2.15(b), the floating n-well of the proposed mixed-voltage I/O buffer 2 is always kept at 2.5 V in the transmit mode and kept at 2.5 V and 5 V in the receive mode. Thus, the proposed mixed-voltage I/O buffer 2 is recommended for high-speed and low-power applications.

2.5. Discussions and Comparisons

2.5.1. Speed

The output loadings of these mixed-voltage I/O buffers include the I/O pad, the bonding wire, the package pin, the PCB trace, and so on. Therefore, the output loadings of these I/O buffers are usually very large. These mixed-voltage I/O buffers are simulated in a 0.25-µm 2.5-V CMOS process to compare their speed performances under the condition of the same output loading. Table 2.1 shows the simulated delay times from the node Dout to the I/O pad when these I/O buffers are in the transmit mode to drive a 20-pF output loading. As shown in Table 2.1, the delay times of these I/O buffers in Figs. 2.6, 2.7, 2.8, 2.9, and 2.13 are almost the same, expect those of the I/O buffers in Figs. 2.4 and 2.5. Although the driving capacities (by adjusting the device dimensions of output transistors) and the output capacitances of these I/O buffers are kept the same, the parasitic capacitances of the stacked PMOS devices in the output stage of the mixed-voltage I/O buffers in Figs. 2.4 and 2.5 are large. Besides, the larger threshold voltage of transistor MP0 in Fig. 2.4 (Fig. 2.5) owing to the body effect results in the lower driving capacity. Thus, these two I/O buffers in Figs. 2.4 and 2.5 have a little longer delay times than the other mixed-voltage I/O buffers.

2.5.2. Power Consumption

The power consumption of CMOS digital circuit includes three parts: the dynamic power consumption due to charging and discharging the capacitance, the short-circuit power consumption, and the power consumption due to the dc leakage current. Because there should be no dc leakage current in the design of these mixed-voltage I/O buffers whenever they operate in the receive mode or transmit mode, the power consuming on the output loading dominates the total power consumption in these I/O buffers. Hence, the power consumptions of these mixed-voltage I/O buffers are almost the same if the output loadings are kept the same and the operating frequency is fixed. These mixed-voltage I/O buffers are simulated in a 0.25-μm 2.5-V CMOS process. The simulated power consumptions of these mixed-voltage I/O buffers in the transmit mode to drive the 20-pF output loading at the frequency of 50 MHz are compared in Table 2.2. Although the output loadings of these mixed-voltage I/O buffers are all the same of 20 pF, the power consumptions of the I/O buffers in Figs. 2.4 and 2.5 are somewhat larger than those of the other I/O buffers. The reason is that the parasitic self output capacitances of the mixed-voltage I/O buffers in Figs. 2.4 and 2.5 are larger than those of the other I/O buffers.

2.5.3. Area

The total area of these mixed-voltage I/O buffers can be evaluated by calculating the total channel widths of transistors in these I/O buffers if the channel lengths of all devices in these I/O buffers are kept the same. Table 2.3 shows the calculated total widths of these mixed-voltage I/O buffers, where Wp and Wn are the unit width of the PMOS and NMOS devices, respectively. The total width is calculated including the widths of the devices in the pull-up and pull-down paths, the dynamic n-well bias circuit, the gate-tracking circuit, and the protecting devices of input buffer. Expect the devices in the pull-up and pull-down paths, the widths of the PMOS and NMOS devices in these I/O buffers are kept as Wp and Wn, respectively. For fair comparison, the driving capacities of the output stages in these mixed-voltage I/O buffers must be kept the same. Therefore, the widths of the PMOS and NMOS devices in the output stage of stacked configuration are twice as those in the output stage of single device. In this calculation, the widths of the PMOS and NMOS devices in the output stage of single device are 3Wp and 3Wn, respectively. The widths of the PMOS and NMOS devices in the output stage of stacked configuration are 6Wp and 6Wn, respectively. Generally, Wp is triple as large as Wn in CMOS digital circuits [35]. Hence, the total widths of these mixed-voltage I/O buffers can be shown in terms of Wn for comparison. As shown in Table III, the total widths of the proposed mixed-voltage I/O buffers 1 and 2 are 37Wn and

42Wn, respectively. Although the total width of the I/O buffer in Fig. 2.6 is 19Wn, this I/O buffer needs an extra pad to provide the external voltage to bias the n-well of the pull-up PMOS device. The area of this I/O buffer in Fig. 2.6, when it includes the extra pad into the chip, will become larger than that of the proposed I/O buffers.

2.5.4. *Noise, Latch-Up, and Subthreshold Leakage Issues*

The n-wells of the pull-up PMOS devices in some mixed-voltage I/O buffers will be floated in some operation conditions. The I/O coupling noise into the floating n-wells of the pull-up PMOS devices could induce the latch-up issue. Therefore, the pull-up PMOS devices in these mixed-voltage I/O buffers must be carefully drawn in the layout. The guard rings must be used to surround the pull-up PMOS devices to isolate the I/O noise against the latch-up problem [36]. In addition, the lower threshold voltage of the pull-up PMOS device due to the lower floating n-well voltage results in the subthreshold leakage current. The proposed mixed-voltage I/O buffer 2 and the prior design [25] don't have the floating n-well issue. Thus, these two mixed-voltage I/O buffers are suitable for low-power applications.

2.5.5. *Transient Stress*

The stacked NMOS technique is used avoid the gate-oxide overstress in the mixed-voltage I/O interface, as shown in Fig. 2.3. However, in some specified operation state, the upper transistor (MN0) may still suffer the hot-carrier issue. When the voltage on the I/O pad is initially kept at 5 V and then the transistor MN1 in Fig. 2.3 is turned on by its pre-driver circuit to pull down the pad voltage to 0 V, the drain-source voltage of transistor MN0 may exceed 2.5 V during this transient condition to suffer the hot-carrier degradation. Nevertheless, this transient-stress problem can be further solved by using three stacked devices and dynamically controlling the gate voltage of the top device [15].

2.5.6. *Comparisons*

Table 2.4 lists the features among these mixed-voltage I/O buffers. Since the new proposed mixed-voltage I/O buffers and the prior I/O buffers reported in [24], [25], [33], and

[34] use the dynamic n-well biased technique, no extra pad and power supply is required. The new proposed mixed-voltage I/O buffers in this work occupy smaller silicon area than the I/O buffers reported in [23]-[25], [33], [34]. Although the circuit structures of the mixed-voltage I/O buffers reported in [33], [34] are simpler, these two I/O buffers have the gate-oxide reliability problem. In Fig. 2.4, transistors MN0, MN1, and MP2 have the gate-oxide reliability problem in the tri-state input mode when the input signal has a 5-V voltage level. In Fig. 2.5, transistor MP2 has the gate-oxide reliability problem when the input signal at the I/O pad is 5 V in the tri-state mode. Besides, since the depletion PMOS is used to improve the gate-tracking circuit of the mixed-voltage I/O buffer reported in [23], extra mask and process modification are required to realize the depletion device. The prior mixed-voltage I/O buffers reported in [24], [33], [34] and the proposed mixed-voltage I/O buffer 1 may have the subthreshold leakage problem, but the prior mixed-voltage I/O buffer reported in [25] and the proposed mixed-voltage I/O buffer 2 don't have. However, the proposed mixed-voltage I/O buffers occupy smaller silicon area than the prior I/O buffers [24], [25], [33], [34]. Thus, if the subthreshold leakage issue in the given CMOS process is not serious, the proposed mixed-voltage I/O buffer 1 is more recommended than the prior designs reported in [24], [33], [34]. If the subthreshold leakage problem in the given CMOS problem is serious, such as the 0.13-µm, 90-nm or below CMOS process, the proposed mixed-voltage I/O buffer 2 is recommended.

2.6. Summary

Two new mixed-voltage I/O buffers with the stacked NMOS technique, dynamic n-well technique, and gate-tracking circuit have been presented in this chapter. The new proposed mixed-voltage I/O buffer 1 has been implemented in a 0.25-µm 2.5-V CMOS process, which can be operated in the 2.5/5-V signal environment without the gate-oxide reliability problem. The new proposed mixed-voltage I/O buffer 2 can be applied for high-speed applications without the gate-oxide reliability problem and the circuit leakage issue. The new proposed mixed-voltage I/O buffers realized with 1×VDD devices can be easily applied in 1×VDD/2×VDD mixed-voltage interface.

TABLE 2.1

COMPARISON ON DELAY AMONG THE MIXED-VOLTAGE I/O BUFFERS IN THE TRANSMIT MODE

Mixed-voltage I/O designs	Delay time (Dout to I/O pad)
Fig. 2.4 [33]	2.26 ns
Fig. 2.5 [34]	2.13 ns
Fig. 2.6 [23]	1.88 ns
Fig. 2.7 [24]	1.89 ns
Fig. 2.8 [25]	1.90 ns
Fig. 2.9 (This work 1)	1.81 ns
Fig. 2.13 (This work 2)	1.81 ns

TABLE 2.2

COMPARISON ON POWER CONSUMPTION AMONG THE MIXED-VOLTAGE I/O BUFFERS IN THE TRANSMIT MODE

Mixed-voltage I/O designs	Average power consumption (Output load =20 pF, frequency=50 MHz)
Fig. 2.4 [33]	11.1 μW
Fig. 2.5 [34]	11.6 μW
Fig. 2.6 [23]	8.4 μW
Fig. 2.7 [24]	8.7 μW
Fig. 2.8 [25]	8.8 μW
Fig. 2.9 (This work 1)	9 μW
Fig. 2.13 (This work 2)	8.6 μW

TABLE 2.3

Comparison on Area (Device Sizes) among the Mixed-Voltage I/O Buffers

Mixed-voltage I/O designs	PMOSs in pull-up path	NMOSs in pull-down path	Other PMOSs	Other NMOSs	Total width of PMOSs in pull-up path	Total width of NMOSs in pull-down path	Total width of other PMOSs	Total width of other NMOSs	Total width of I/O buffer	Total width of I/O buffer in terms of Wn*
Fig. 2.4 [33]	MP0, MP1	MN0	MP2, MP3	MN1, MN2	12Wp	3Wn	2Wp	2Wn	14Wp+ 5Wn	47Wn
Fig. 2.5 [34]	MP0, MP1	MN0, MN1	MP2~4	MN2~4	12Wp	12Wn	3Wp	3Wn	15Wp+ 15Wn	60Wn
Fig. 2.6 [23]	MP0	MN0, MN1	MP1, MP2	MN2, MN3	3Wp	12Wn	2Wp	2Wn	5Wp+ 14Wn	29Wn
Fig. 2.7 [24]	MP0	MN0, MN1	MP1~5	MN2~6	3Wp	12Wn	5Wp	5Wn	8Wp+ 17Wn	41Wn
Fig. 2.8 [25]	MP0	MN0, MN1	MP1~8	MN2~5	3Wp	12Wn	8Wp	4Wn	11Wp+ 16Wn	49Wn
Fig. 2.9 (This work 1)	MP0	MN0, MN1	MP1~5	MN2	3Wp	12Wn	5Wp	1Wn	8Wp+ 13Wn	37Wn
Fig. 2.13 (This work 2)	MP0	MN0, MN1	MP1~6	MN2~4	3Wp	12Wn	6Wp	3Wn	9Wp+ 15Wn	42Wn

*Wp=3Wn

TABLE 2.4

COMPARISON ON FEATURES AMONG THE MIXED-VOLTAGE I/O BUFFERS

Mixed-voltage I/O designs	N-well bias	Extra pad for n-well bias	Gate-oxide reliability issue	With special device	Subthreshold leakage issue	Area
Fig. 2.4 [33]	Dynamic bias	No	Yes	No	Yes	47Wn
Fig. 2.5 [34]	Dynamic bias	No	Yes	No	Yes	60Wn
Fig. 2.6 [23]	Fixed bias	Yes	No	Yes, Depletion PMOS	No	29Wn
Fig. 2.7 [24]	Dynamic bias	No	No	No	Yes	41Wn
Fig. 2.8 [25]	Dynamic bias	No	No	No	No	49Wn
Fig. 2.9 (This work 1)	Dynamic bias	No	No	No	Yes	37Wn
Fig. 2.13 (This work 2)	Dynamic bias	No	No	No	No	42Wn

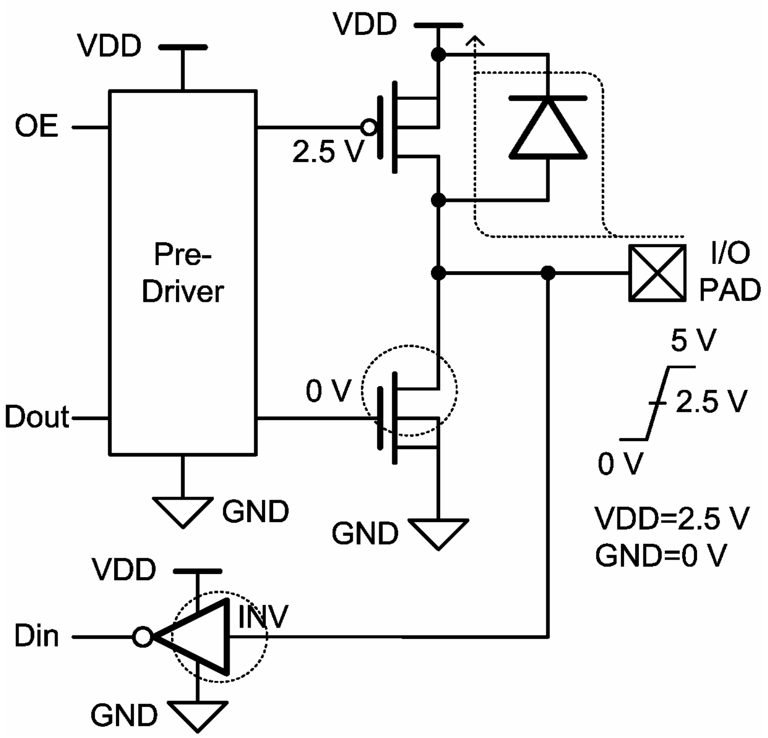


Fig. 2.1. Conventional tri-state I/O buffer in a 0.25-μm CMOS process that will suffer the circuit leakage and gate-oxide reliability issue in the mixed-voltage I/O interface.

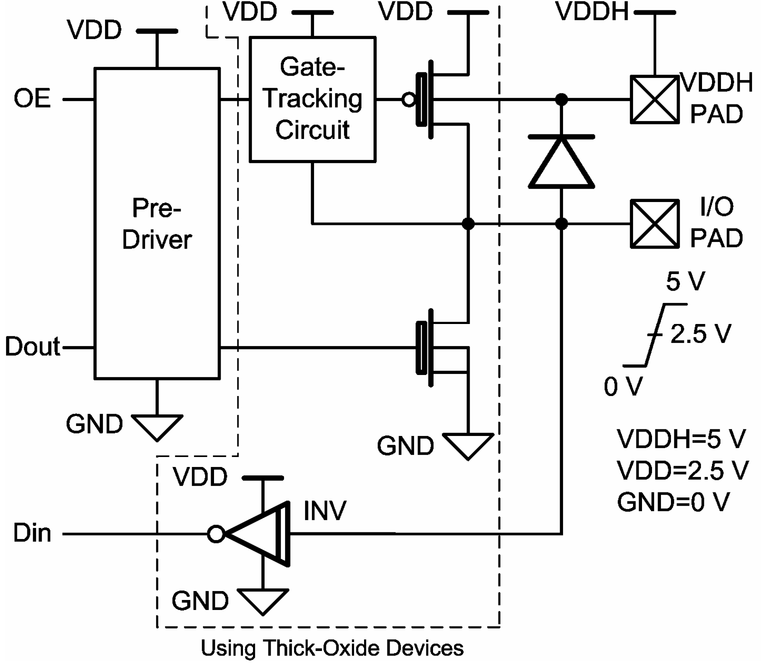


Fig. 2.2. Mixed-voltage I/O buffer with dual-oxide option and an external n-well bias.

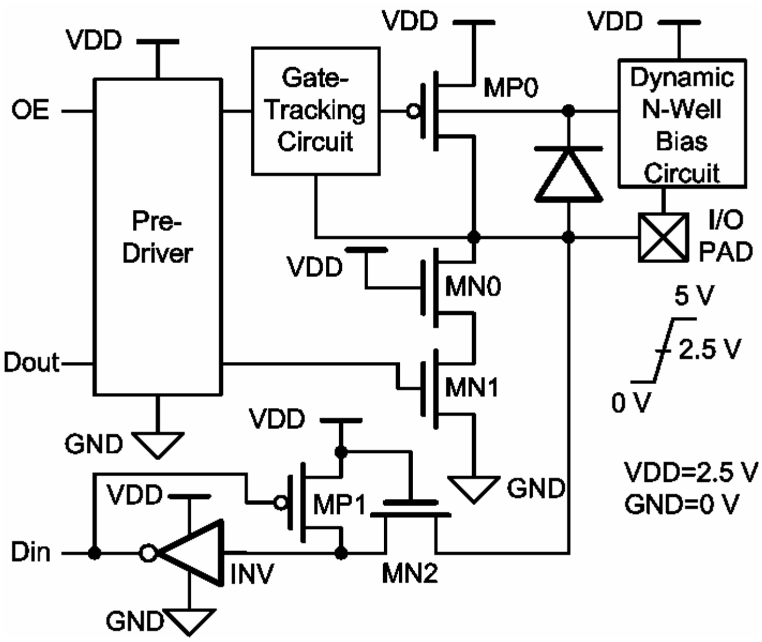


Fig. 2.3. Basic design concept for mixed-voltage I/O buffer realized with only thin-oxide devices.

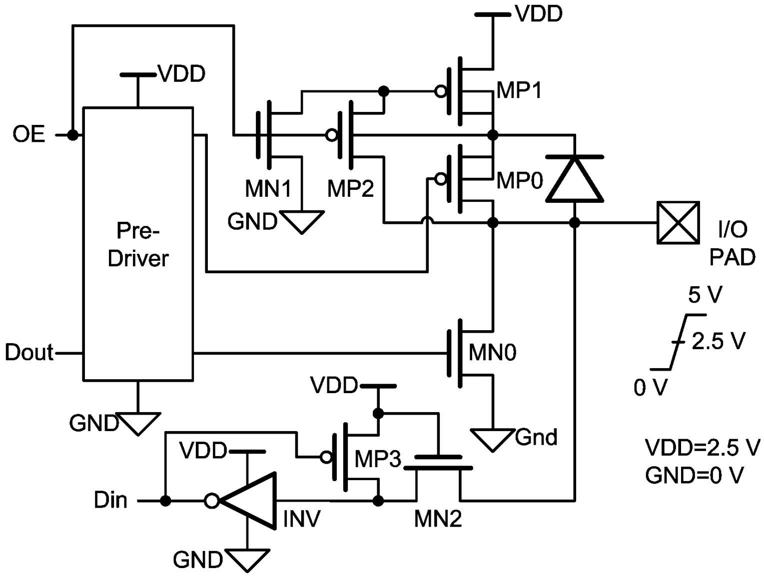


Fig. 2.4. Mixed-voltage I/O buffer with stacked pull-up PMOS devices [33].

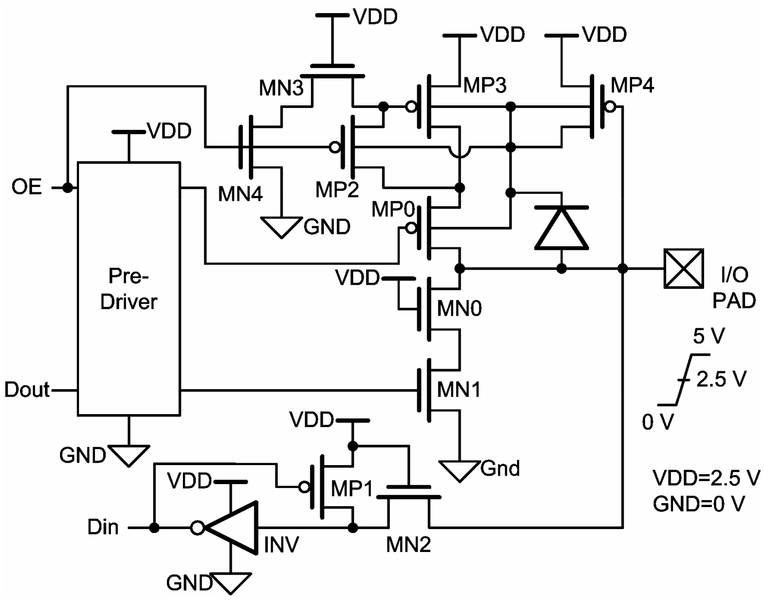


Fig. 2.5. Mixed-voltage I/O buffer with stacked pull-up PMOS devices and stacked pull-down NMOS devices [34].

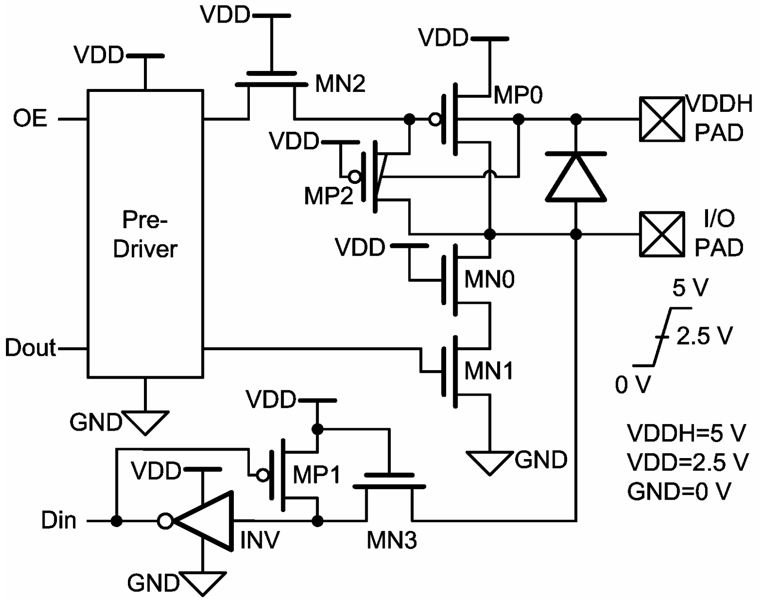


Fig. 2.6. Mixed-voltage I/O buffer with a depletion PMOS device MP2 [23].

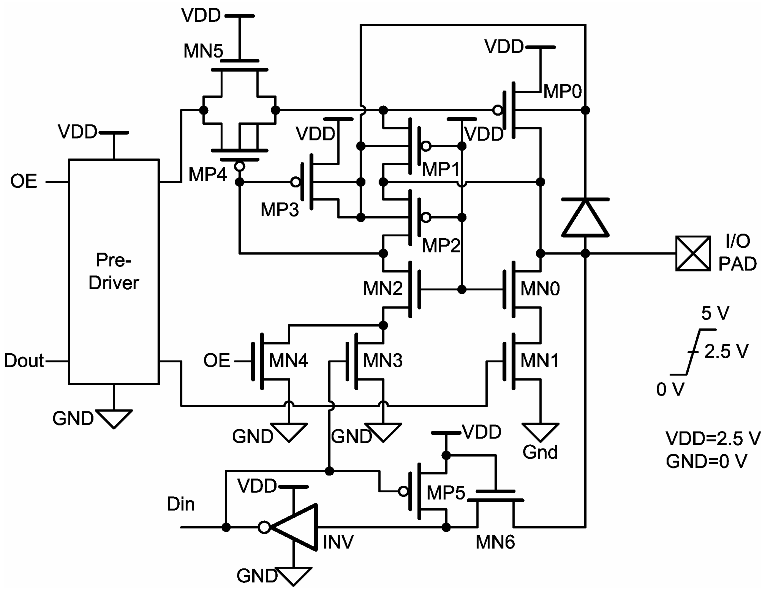


Fig. 2.7. Mixed-voltage I/O buffer realized with only thin-oxide devices [24].

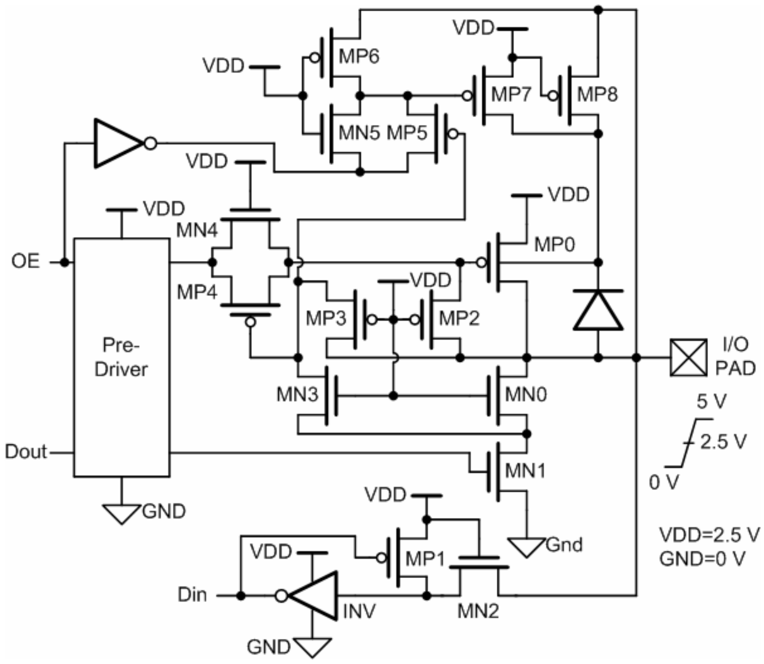


Fig. 2.8. Mixed-voltage I/O buffer realized with only thin-oxide devices [25].

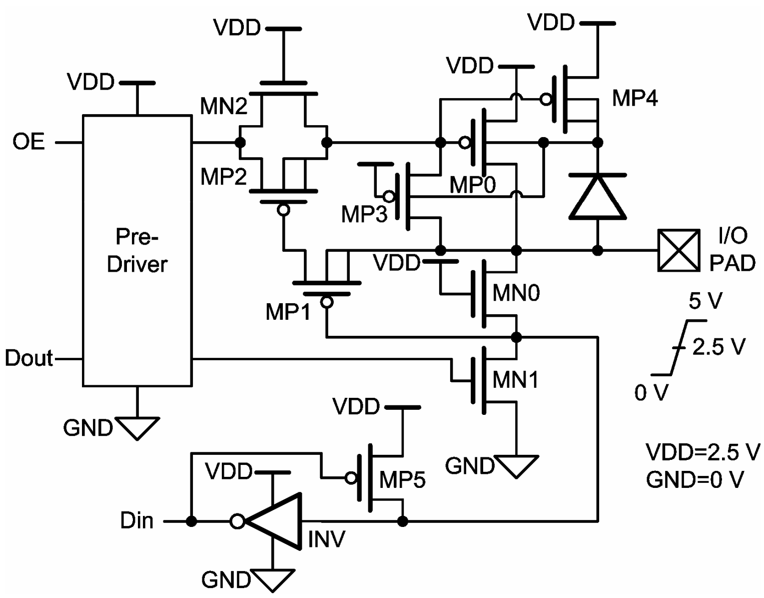
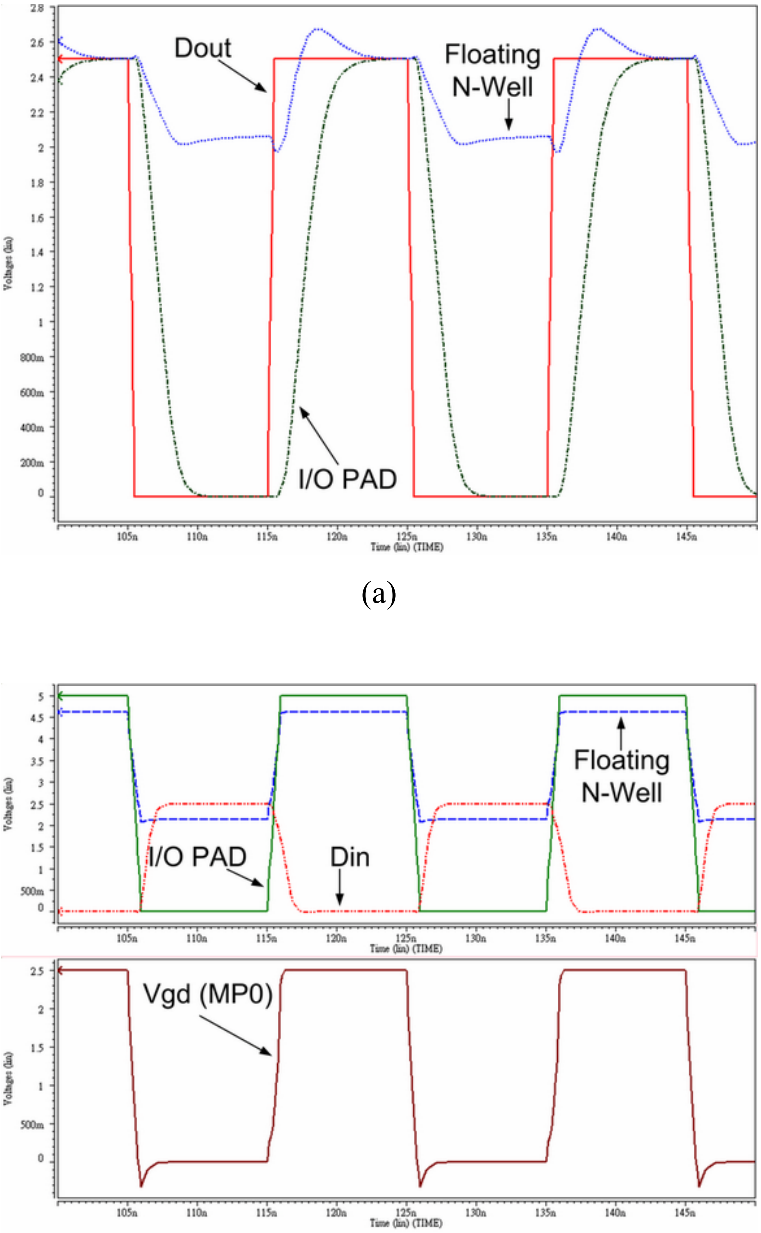


Fig. 2.9. New mixed-voltage I/O buffer 1 with only thin-oxide devices.



(a)

(b)

Fig. 2.10. Simulated waveforms of the new proposed mixed-voltage I/O buffer 1 with a 20-pF load and 50-MHz I/O signal in (a) the transmit mode, and (b) the tri-state (receive) mode.

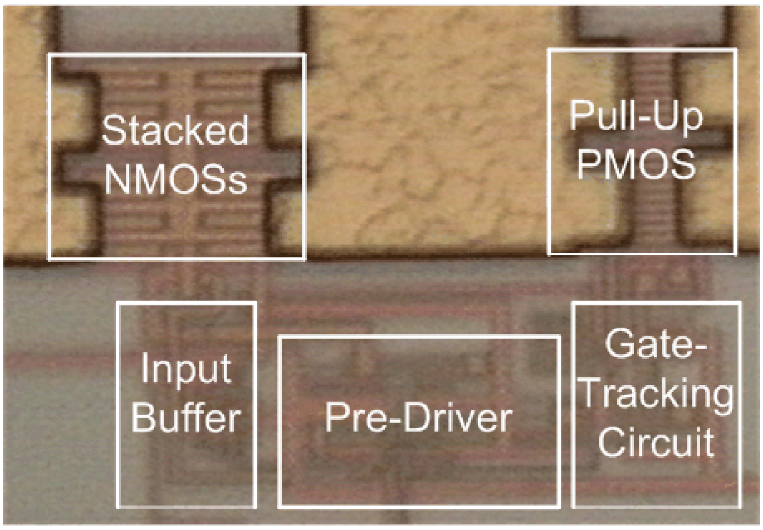
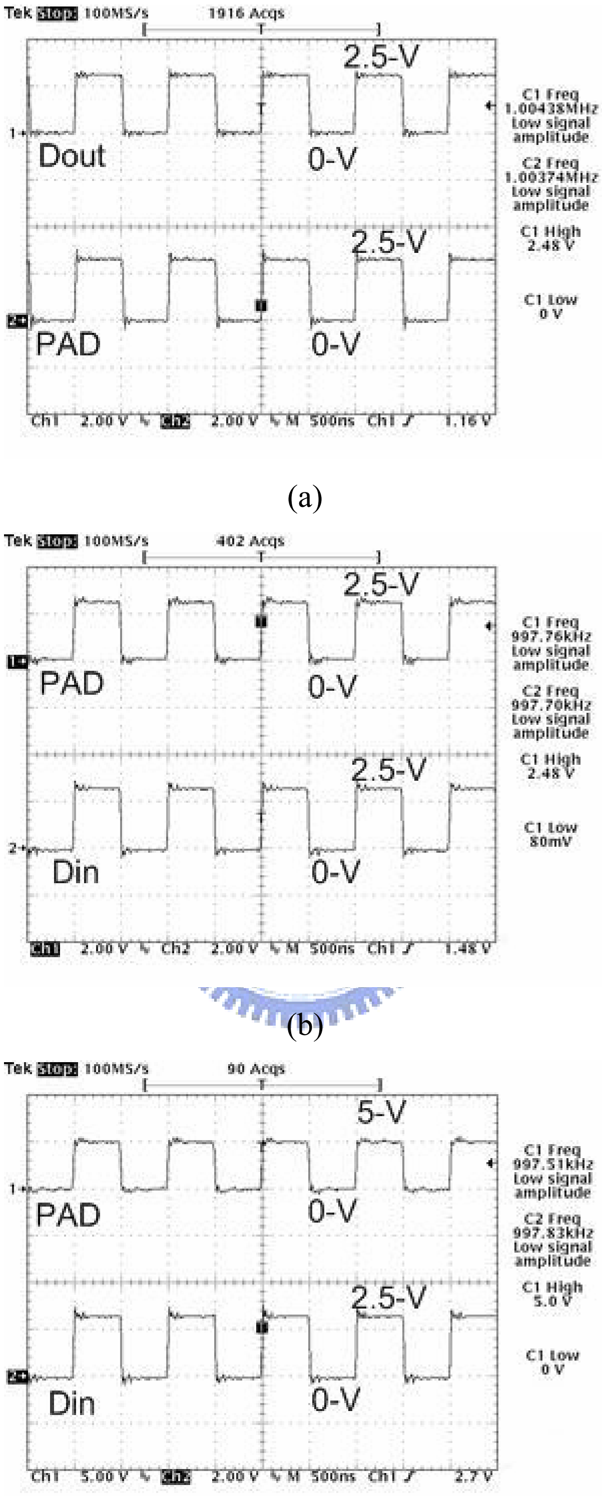


Fig. 2.11. Die photograph of the new proposed mixed-voltage I/O buffer 1 fabricated in a 0.25-µm 2.5-V CMOS process.



(a)

(b)

(c)

Fig. 2.12. Measured waveforms of the new proposed mixed-voltage I/O buffer 1 with 1-MHz I/O signal in (a) the transmit mode, (b) the tri-state input mode with 2.5-V input, and (c) the tri-state input mode with 5-V input.

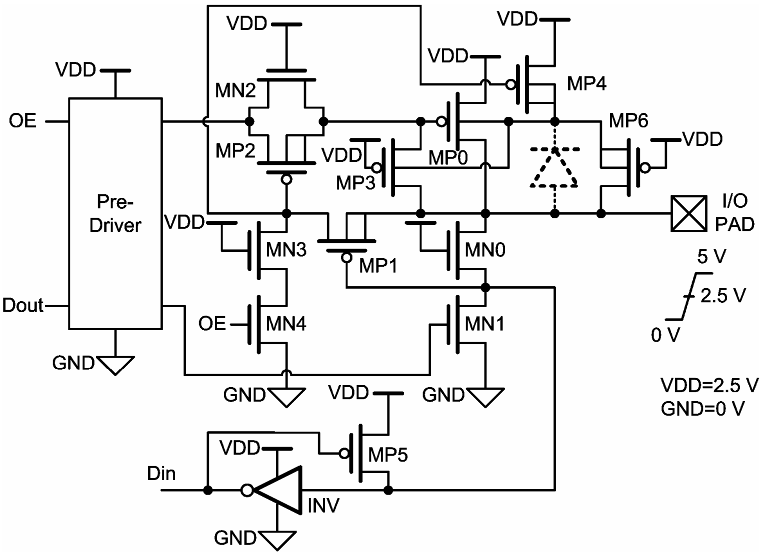
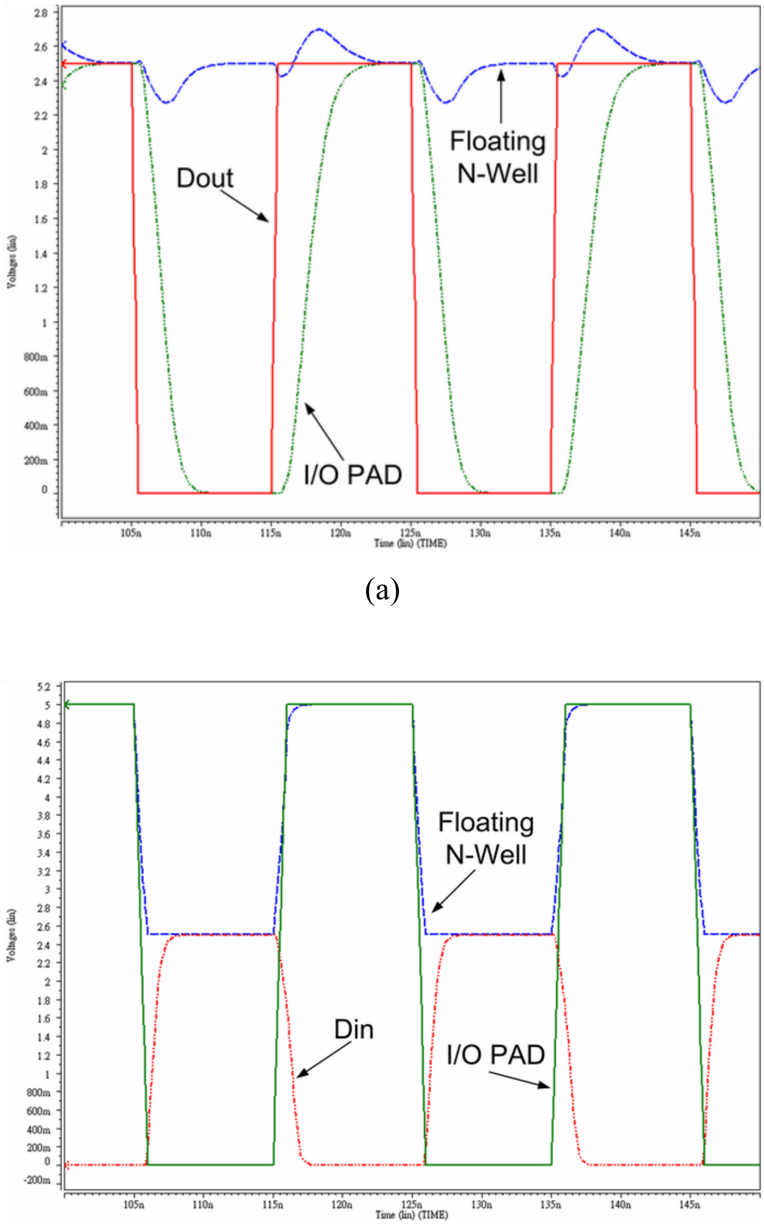


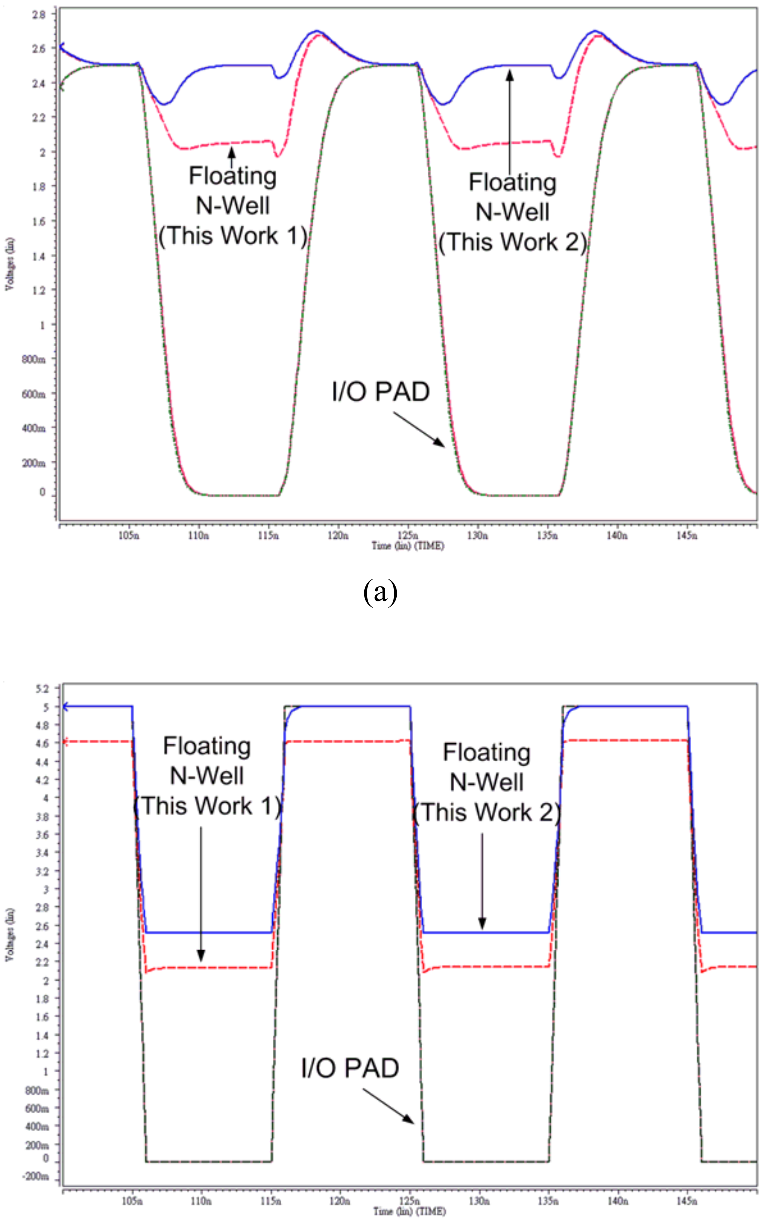
Fig. 2.13. New proposed mixed-voltage I/O buffer 2 with only thin-oxide devices.



(a)

(b)

Fig. 2.14. Simulated waveforms of the new proposed mixed-voltage I/O buffer 2 with a 20-pF load and 50-MHz I/O signal in (a) the transmit mode, and (b) the tri-state input (receive) mode.



(a)

(b)

Fig. 2.15. Simulated waveforms to compare the voltage levels of the floating n-well in the new mixed-voltage I/O buffers 1 and 2, during the signal transition on the I/O pad. (a) In transmit mode, and (b) in receive mode.

CHAPTER 3

3.3-V Input Buffer and Output Buffer in 0.13-μm 1/2.5-V CMOS Process

With 3.3-V interface, such as PCI-X application, the high-voltage overstress on the gate oxide is a serious reliability problem to design the I/O circuits by only using 1/2.5-V low-voltage devices in a 0.13-μm CMOS process. Thus, an input buffer [37] and an output buffer [38] realized with 1/2.5-V low-voltage devices for 3.3-V applications are presented in this chapter, respectively. Besides, a new Schmitt trigger circuit [37] and a new level converter [38] are also presented in this chapter.

3.1. Input Buffer

3.1.1. Background

As the semiconductor process is scaled down, the thickness of gate oxide becomes thinner in order to decrease the core power supply voltage (VDD) [1]. However, the board voltage (VCC) is still kept as high as 3.3 V (or 5 V), such as PCI-X interface [39]. There are three problems on a MOSFET when the operating voltage is higher than its normal voltage. Higher drain-to-source voltage (Vds) may cause the serious hot-carrier effect which results in the long-term lifetime issue [6]. The drain-to-bulk pn-junction breakdown may occur if the operating voltage is too high. The high-voltage stress across the thinner gate oxide could also destruct the gate oxide [27]. Thus, the I/O circuit must be designed carefully to overcome these problems, especially the high-voltage gate-oxide stress [23]-[29].

Schmitt trigger circuit has been widely used in the input buffers to increase noise immunity. The conventional input buffer, which consists of a Schmitt trigger and a level-down converter, is shown in Fig. 3.1. The Schmitt trigger circuit receives input signals from the I/O pad and rejects input noise. Then, the level-down converter can convert the signal swing from VCC to VDD, where VCC is the board voltage and VDD is the core power supply voltage. The circuit and the transfer curve of the conventional Schmitt trigger circuit [40], [41] are shown in Figs. 3.2(a) and 3.2(b), respectively. Transistors P1, P2, P3, N1, N2, and N3 in Fig. 3.2(a) are the I/O devices with the normal operation voltage of VDD. If the board voltage (VCC) is equal to VDD, the gate-drain and gate-source voltages of transistors P1, P2, P3, N1, N2, and N3 in Fig. 3.2(a) will not exceed VDD. Thus, the conventional Schmitt trigger circuit can be operated safely without suffering high-voltage gate-oxide overstress. As shown in Fig. 3.2(b), the conventional Schmitt trigger circuit with different high-to-low and low-to-high transition threshold voltages (V_H and V_L) has better noise immunity than the inverter. When the input signal IN goes up to VCC from GND, the threshold voltage of the conventional Schmitt trigger circuit is V_H. In other words, the output signal OUT is pulled low when the signal IN exceeds the high-to-low threshold voltage (V_H). Similarly, when the input signal IN goes down to GND from VCC, the threshold voltage of the conventional Schmitt trigger circuit is V_L. In other words, the output signal OUT is pulled up when the input signal IN is lower than the low-to-high threshold voltage (V_L). Hence, the noise immunity of the conventional Schmitt trigger circuit is better than that of inverter. The threshold voltages V_H and V_L can be adjusted by controlling the device dimensions of those transistors [35].

Several modified Schmitt trigger circuits were reported for different applications [42]-[45]. Fig. 3.3(a) shows the Schmitt trigger circuit reported in [42]. The extra bias voltage VB and the extra transistors P4 and N4 are used to adjust the two threshold voltages V_L and V_H. In [43], a multi-layer Schmitt trigger circuit was reported to increase the voltage difference between the two threshold voltages V_H and V_L. The two-layer Schmitt trigger circuit is shown in Fig. 3.3(b). However, as the power supply voltage is scaled down, the multi-layer Schmitt trigger circuit can not be operated correctly. In [44], a low-power Schmitt trigger circuit was reported. An alternative circuit, which has the hysteresis characteristic similar to that of a conventional Schmitt trigger, was reported in [45].

However, the aforementioned Schmitt trigger circuits have high-voltage gate-oxide overstress problem if the board voltage (VCC) is higher than VDD. For example, the digital part of a chip is designed with 1-V devices to decrease its power dissipation, the analog part is designed with 2.5-V devices to improve the circuit performance, and the chip-to-chip interface is 3.3-V PCI-X in a 0.13-μm 1/2.5-V CMOS process. The gate-source voltages and the gate-drain voltages of transistors P1, P2, P3, N1, N2, and N3 in Fig. 3.2(a) will be higher than 2.5 V if the board voltage (VCC) is 3.3 V and the I/O devices are 2.5-V devices. Thus, all transistors in Fig. 3.2(a) will suffer the high-voltage gate-oxide overstress problem.

Furthermore, the other Schmitt triggers [42]-[45] also suffer the gate-oxide reliability problem in such a mixed-voltage interface. Thus, a new Schmitt trigger circuit for the input buffer is presented in this section. Then, the whole input buffer realized with the 1/2.5-V devices to receive 3.3-V input signals is presented.

3.1.2. Schmitt Trigger Design

The new proposed Schmitt trigger circuit is shown in Fig. 3.4. All devices of the proposed Schmitt trigger circuit in Fig. 3.4 are the I/O devices with the normal operating voltage of 2.5 V. In a 0.13-µm 1/2.5-V CMOS process, the I/O devices is realized with 2.5-V gate oxide and the core circuits are operated with 1-V power supply. Therefore, the voltage across the gate oxide of the I/O devices in this process can not exceed 2.5 V. As shown in Fig. 3.4, because the drains of transistors P3 and N3 are connected to 1 V (VDD), the gate-drain voltages of transistors P3 and N3 will not exceed 2.5 V. The maximum gate-drain and gate-source voltages of transistors P3 and N3 are around 2.3 V (3.3−1=2.3). Because the gates of transistors P2 and N2 are connected to 1 V (VDD), the gate-drain voltages and gate-source voltages of transistors P2 and N2 will not exceed 2.5 V. The maximum gate-drain voltages of transistors P2 and N2 are also around 2.3 V (3.3−1=2.3). If the gate voltage of transistor P1 (node A) is kept higher than 0.8 V (3.3−2.5=0.8) and the gate voltage of transistor N1 (node B) is kept lower than 2.5 V, transistors P1 and N1 don't have the high-voltage gate-oxide overstress problem. Hence, in order to prevent the gate voltage of transistor P1 under 0.8 V, transistors P4, P5, P6, and P7 are added. Similarly, transistors N4, N5, N6, and N7 are designed to prevent the gate voltage of transistor N1 over 2.5 V.

When the input signal (IN) stays at 3.3 V (VCC), the voltage on node A is also kept at 3.3 V because transistor P6 is turned on. When the input signal (IN) goes to 0 V, the voltage on node A is kept at 2·|Vtp| because transistors P4 and P5 are in diode-connected structure. In the 0.13-µm 1/2.5-V CMOS process, |Vtp| of 2.5-V device is about 0.6 V. Therefore, the minimum gate voltage of transistor P1 (node A) is about 1.2 V. However, the diode-connected transistors P5 and P6 may make the voltage on node A to 0 V when the input signal (IN) stays at 0 V for a long time, because of the subthreshold current of transistors P5 and P6. An extra transistor P7 is added to avoid the voltage on node A under 1 V caused by the subthreshold current of transistors P5 and P6. Hence, as the voltage on node A is under 1 V, transistor P7 will be turned on to keep the voltage at 1 V.

When the input signal (IN) stays at 0 V, the voltage on node B is kept at 0 V because transistor N6 is turned on. When the input signal (IN) goes to 3.3 V, the voltage on node B is kept at 3.3−2·|Vtn|, because transistors N4 and N5 are in diode-connected structure. In the 0.13-µm 1/2.5-V CMOS process, |Vtn| of 2.5-V device is about 0.5 V. Therefore, the maximum gate voltage of transistor N1 (node B) is about 2.3 V. However, the diode-connected transistors N5 and N6 may make the voltage on node B to 3.3 V, when the input signal (IN) stays at 3.3 V for a long time, due to the subthreshold current of transistors N5 and N6. Hence, a weak transistor (long-channel transistor) N7 is added to avoid the voltage on node B over 2.5 V caused by the subthreshold current of transistors N5 and N6. If node B goes to 3.3 V, transistor N7 provides a small current to keep the gate voltage of transistor N1 under 2.5 V.

In addition, transistor N6 in Fig. 3.4 can be a 2.5-V native-Vt transistor instead of a 2.5-V normal-Vt transistor. The threshold voltage of the native-Vt transistor is close to 0 V, which is lower than that of the normal-Vt transistor [46], [47]. In the 0.13-µm 1/2.5-V CMOS process, the threshold voltage of the 2.5-V native-Vt transistor is about 0.03 V. Because the gate-source voltage of transistor N6 is small, the voltage on node B follows input signal IN to 0 V slowly. Thus, a native-Vt transistor is more suitable than a normal-Vt transistor to implement the transistor N6 for high-speed applications. Because the native-Vt device has been one of the standard devices in a 0.13-µm 1/2.5-V CMOS process, no extra process or mask is needed [47]. Fig. 3.5 compares the voltage waveforms at node B when transistor N6 is a native-Vt transistor or a normal-Vt transistor in the 0.13-µm 1/2.5-V CMOS process. As shown in Fig. 3.5, the voltage on node B is pulled down more quickly when transistor N6 is implemented by a native-Vt transistor.

A 0.13-µm 1/2.5-V CMOS SPICE model is used to simulate the new proposed Schmitt trigger circuit. The simulated waveforms at the nodes IN, OUT, A, and B of the new proposed Schmitt trigger circuit are shown in Fig. 3.6. The input signal can be correctly translated to the output by the proposed Schmitt trigger circuit. Besides, the voltage level at node A is indeed kept higher than 0.8 V, and that of node B is kept lower than 2.5 V. Therefore, transistors P1 and N1 of the proposed Schmitt trigger circuit don't suffer high-voltage gate-oxide reliability issue in a 3.3-V environment. Besides, the Vgs and Vgd of all devices are not over 2.5 V. The Vds of all devices are also not over 2.5 V when the input signal is high or low. Hence, the new proposed Schmitt trigger circuit can receive the high-voltage input signals without suffering gate-oxide reliability and hot-carrier degradation issues, whereas it is realized by only using the low-voltage devices with thin gate oxide.

The simulated transfer curve of the new proposed Schmitt trigger circuit is shown in Fig. 3.7. The new proposed Schmitt trigger circuit has an obvious hysteresis characteristic. In Fig. 3.7, the transition threshold voltages V_L and V_H of the new proposed Schmitt trigger circuit are around 1.1 V and 2.6 V, respectively.

3.1.3. Whole Input Buffer Design

Fig. 3.8 shows the whole input buffer design with the proposed Schmitt trigger circuit and the level-down converter. The proposed Schmitt trigger circuit receives the input signals from the I/O pad and rejects input noise. Then, the level-down converter can convert the signal swing from VCC (3.3 V) to VDD (1 V). In the level-down converter, transistor N2 is a 2.5-V (thick-oxide) device and transistors P1, P2, and N1 are 1-V (thin-oxide) devices. As the input voltage of the level-down converter is GND, the voltage on node A is also at GND due to transistor N2 and the voltage on node OUT is at VDD. As the input voltage of the level-down converter is VCC, the voltage on node A is limited at VDD−Vt due to transistor N2, whose gate is bias at VDD. Because the voltage on node A is at VDD−Vt, the voltage on node OUT is pulled down to ground and then transistor P2 is turned on. Finally, the voltage on node A is at VDD. Thus, the level-down converter can convert the signal swing from VCC to VDD.

3.1.4. Experimental Results

The new proposed Schmitt trigger circuit and the whole input buffer have been fabricated in a 0.13-μm 1/2.5-V 1P8M CMOS process with Cu interconnects. The layout of the new proposed Schmitt trigger circuit is shown in Fig. 3.9. Because the proposed Schmitt trigger circuit is connected to an input pad, some guard rings surrounding the whole Schmitt trigger circuit are used to prevent the latch-up problem [36]. The layout area of the new proposed Schmitt trigger circuit including the guard rings is only 8.7 μm × 19 μm.

The measured waveforms at the input node and the output node of the new proposed Schmitt trigger circuit are shown in Fig. 3.10. The new proposed Schmitt trigger can operate correctly with 0-to-3.3-V input signals. In Fig. 3.11, the input signal is applied with a slow triangular waveform. Therefore, the transition threshold voltages V_L and V_H of the new proposed Schmitt trigger circuit can be measured at the crossing points between the input signal and output signal. The measured DC transfer curve of the new proposed Schmitt trigger circuit is shown in Fig. 3.12. These two transition threshold voltages V_L and V_H of the fabricated Schmitt trigger circuit are around 1 V and 2.5 V, respectively. Due to the process variation, the measured transition threshold voltages are slightly different from the simulated transition threshold voltages.

The measured waveforms at the nodes IN and OUT of the whole input buffer are shown in Fig. 3.13 with a 133-MHz 3.3-V input signal. The 3.3-V input signal is received by the proposed Schmitt trigger circuit, and then the signal swing is converted from 3.3 V to 1 V by the level-down converter. As shown in Fig. 3.13, the input buffer can be successfully operated in the 133-MHz 3.3-V environment.

3.1.5. Summary

A new Schmitt trigger circuit realized with only low-voltage devices to receive the high-voltage signals is proposed. The new Schmitt trigger circuit has been fabricated in a 0.13-μm 1/2.5-V 1P8M CMOS process. The proposed Schmitt trigger circuit, which consists of low-voltage (2.5-V) devices, can be operated correctly without suffering high-voltage gate-oxide overstress in a 3.3-V interface environment. The measured results have shown that the two transition threshold voltages V_L and V_H of the new proposed Schmitt trigger are 1 V and 2.5 V, respectively. The whole input buffer, which is consisted with the proposed Schmitt trigger and a level-down converter, has been verified to be successfully operated in the 133-MHz 3.3-V environment.

3.2. Output Buffer

3.2.1. Background

The thickness of gate oxide becomes thinner in order to decrease the core power supply voltage (VDD) as the semiconductor technology is scaled down [1]. This results in lower power consumption. However, the board voltage (VCC) is still kept as high as 3.3 V (or 5 V), such as PCI-X interface [39]. There are three problems on a MOSFET when the operating voltage is higher than its normal voltage. Higher drain-to-source voltage (Vds) may cause the serious hot-carrier effect which results in the long-term lifetime issue [6]. The drain-to-bulk pn-junction breakdown may occur if the operating voltage is too high. The high-voltage overstress across the thinner gate oxide could also destruct the gate oxide [27], [28]. Therefore, the I/O circuits must be designed carefully to overcome these problems, especially the high-voltage gate-oxide overstress [23]-[26].

Recently, the dual-oxide (thin-oxide and thick-oxide) processes have been supported by some manufacturing companies [32], [47], [48]. For example, the thin-oxide devices are 1-V or 1.2-V devices and the thick-oxide devices are 1.8-V, 2.5-V, or 3.3-V devices in a 0.13-µm CMOS process [47], [48]. The thin-oxide devices are used to design the digital circuits to decrease silicon area and power consumption. The thick-oxide devices are used to design the analog circuits to improve circuit performance or the I/O circuits to avoid the gate-oxide reliability issue. Fig. 3.14 shows the conventional tri-state I/O buffer co-designed with thin- and thick-oxide devices. As shown in Fig. 3.14, transistors P1 and N1 are the thick-oxide devices, which can sustain the voltage level of VCC to avoid the gate-oxide reliability issue. Since the core circuits are operated at VDD, the voltage swing of signals IN, EN, ENB is from GND to VDD. However, the voltage swing of the output signal is from GND to VCC. Thus, the level converter is required to convert the GND-to-VDD signal to the GND-to-VCC signal in order to prevent the high-voltage overstress across the core devices. The conventional level converter co-designed with thin-oxide and thick-oxide devices is shown in Fig. 3.15, where transistors P1, P2, N1, and N2 are thick-oxide devices, but transistors P3 and N3 are thin-oxide devices. The voltage swing of signals IN and INB is from GND to VDD, whereas the voltage swing of signals OUT is from GND to VCC. If the voltage gap between VDD and VCC is too large, such conventional level converter can not be operated correctly. Some techniques have been reported to solve this problem [49]-[52]. Using precharging devices to increase the pull-up capacity was reported in [49]. A boosting technique was reported to pump the input voltage swing of the level converter [50], [51]. The zero-Vt (or called as native-Vt) NMOS transistor was used to design the level converter for higher driving capability [52].

Due to the high-integration trend of SOC (system on a chip), a system may be integrated into a single chip. Therefore, there are digital circuits and analog circuits in a chip. For example, the digital part of a chip is designed with 1-V devices to decrease its power dissipation, the analog part is designed with 2.5-V devices to improve the circuit performance, and the chip-to-chip interface is 3.3-V PCI-X in a 0.13-µm 1/2.5-V CMOS process. Thus, a new output buffer is designed in a 0.13-µm 1/2.5-V CMOS process to drive 3.3-V output signals without the gate-oxide reliability issue in this section. Besides, a new level converter, which can convert 0/1-V signals to 1/3.3-V signals, is also presented in this section.

3.2.2. Output Stage Design

Because the proposed output buffer is designed in a 0.13-μm 1/2.5-V CMOS process, the gate-to-source voltages and gate-to-drain voltages of the thin-oxide devices can not exceed 1 V. The gate-to-source voltages and gate-to-drain voltages of the thick-oxide devices can not exceed 2.5 V. However, VCC of PCI-X specification is 3.3 V [39]. Therefore, the output stage must be stacked and the gate voltages must be well controlled to prevent high-voltage overstress on their gate oxides. The new proposed output stages are shown in Figs. 3.16(a) and 3.16(b). To avoid the body effect resulting in a lower driving capacity, the bulks of the transistors in Figs. 3.16(a) and 3.16(b) are connected to their sources individually. In Fig. 3.16(a), the pull-up path and pull-down path have two stacked 2.5-V PMOS transistors (P1 and P2) and 2.5-V NMOS transistors (N1 and N2), respectively. Since the gate voltages of transistors P2 and N2 are biased at VDD (1 V), the extra bias generator is not required. Because the gate voltages of transistors P2 and N2 are biased at 1 V, the gate-to-source voltages (Vgs) and the gate-to-drain voltages (Vgd) of transistors P2 and N2 don’t exceed 2.5 V. The maximum Vgs and Vgd of transistors P2 and N2 are around 2.3 V (3.3−1=2.3). Transistors P2 and N2 are used to protect transistors P1 and N1 against the high-voltage gate-oxide overstress, respectively. However, the source voltage of transistor P1 is 3.3 V. In this design, the minimum voltage level of signal PU can’t be lower than 0.8 V (3.3−2.5=0.8). The voltage swing of signal PU can be designed between 1 V (VDD) to 3.3 V (VCC) to control the gate of transistor P1. Hence, a level converter that can convert 0/1-V voltage swing to 1/3.3-V voltage swing is demanded for the proposed output buffer.

In Fig. 3.16(a), transistors N1 and N2 are 2.5-V normal-Vt NMOS transistors with threshold voltage of 0.6 V, which is still too high for high speed operation when the Vgs of the normal-Vt NMOS transistor is only 1 V. Hence, the driving capability of the pull-down path in Fig. 3.16(a) needs to be improved. Therefore, a modified version of output stage is shown in Fig. 3.16(b). Transistor N2 in Fig. 3.16(b) is a 2.5-V native-Vt NMOS transistor, which has a threshold voltage of −0.1 V. Transistor N1 in Fig. 3.16(b) is a 1-V NMOS transistor. The native-Vt NMOS transistor is one of standard devices in a 0.13-μm CMOS process without extra process modification [47]. Therefore, the driving capability of the output buffer in Fig. 3.16(b) can be increased. Because the gate of transistor N2 is biased at 1

V, transistor N1 in Fig. 3.16(b) can be safely operated without suffering high-voltage gate-oxide overstress. However, since transistor N2 is a native-Vt NMOS transistor, the sub-threshold leakage current could be serious. If the voltage on node OUT in Fig. 3.16(b) is 3.3 V, the sub-threshold current of transistor N2 may occur. Thus, the voltage on node A in Fig. 3.16(b) may exceed 1 V. An extra PMOS transistor P3 is added in Fig. 3.16(b) to keep the maximum voltage on node A at 1 V. When signals PU and PD are at logic "0" (1 V and 0 V), the voltage on node OUT is VCC (3.3 V). Because signal PD is at 0 V, transistor P3 is turned on to keep the voltage on node A at 1 V. Hence, the high-voltage gate-oxide overstress caused by sub-threshold leakage of transistor N2 can be avoided. Because transistor P3 is a weak device that keeps the voltage on node A at 1 V, it can be a 2.5-V normal-Vt PMOS transistor. Fig. 3.17 shows the simulated waveforms of the output stages in a 0.13-µm CMOS process with 1-V and 2.5-V devices. In this simulation, the transistor sizes of these two output stages are kept the same. As shown in Fig. 3.17, the driving (pull-down) speed of the output stage in Fig. 3.16(b) is better than that of the output stage in Fig. 3.16(a).

3.2.3. Level Converter Design

Fig. 3.18 shows the new proposed level converter that can convert 0/1-V voltage swing to 1/3.3-V voltage swing. In Fig. 3.18, the bulks of the transistors are connected to their sources, respectively, because of the body effect issue. Transistors N1A and N1B are 1-V normal-Vt NMOS transistors, whereas transistors N2A and N2B are 2.5-V native-Vt NMOS transistors, so the driving capability can be increased. The other transistors are all 2.5-V normal-Vt transistors. Transistors P3A can keep the voltage on node A1 at 1 V when the voltage on node B1 is 3.3 V. Similarly, transistor P3B is used to keep the voltage on node A2 at 1 V when the voltage on node B2 is 3.3 V. The voltage swing of input signals IN and INB is from 0 V to 1 V. When signal IN is 1 V and signal INB is 0 V, the voltage on node B1 is pulled down to 0 V and transistor P5A is turned on. After transistor P5A is turned on, the voltage on node OUTB is pulled down to 1 V, and then transistors P4B and P1B are turned on. Therefore, the voltages on nodes OUT and B2 are both pulled up to 3.3 V.

When signal IN is 0 V and signal INB is 1 V, the voltage on node B2 is pulled down to 0 V and transistor P5B is turned on. After transistor P5B is turned on, the voltage on node OUT is pulled down to 1 V, and then transistors P4A and P1A are turned on. Therefore, the voltages on nodes OUTB and B1 are both pulled up to 3.3 V.

Because using PMOS transistors to pull down nodes OUT and OUTB could be too slow, two cross-coupled NMOS transistors N3A and N3B are added to increase the pull-down speed. Fig. 3.19 shows the simulated waveforms of the new proposed level converter in a 0.13-μm 1/2.5-V CMOS process. The pull-down speed of the proposed level converter with transistors N3A and N3B is faster than that of the level converter without N3A and N3B.

3.2.4. Whole Output Buffer Design

Fig. 3.20 depicts the whole output buffer, which consists of an output stage, a level converter, a tri-state control circuit, and two kinds of taper buffers (taper buffer 1 and taper buffer 2). In Fig. 3.20, a CMOS NAND gate and a NOR gate are used to implement the tri-state control circuit. When control signal EN is 0 V and control signal ENB is 1 V, the output buffer is in the high-impendence state. When control signal EN is 1 V and control signal ENB is 0 V, the output buffer drives the output pad according to the signal IN from the core circuits. Fig. 3.21(a) shows another tri-state control circuit, which consists of only six transistors [24]. Compared with the traditional tri-state control circuit in Fig. 3.20, the circuit in Fig. 3.21(a) may have the smaller silicon area and input capacitance. Thus, the tri-state control circuit in Fig. 3.21(a) can be used to replace the traditional tri-state control circuit in Fig. 3.20. The output stage of this whole output buffer is the same as that in Fig. 3.16(b). The level converter that can transfer the signal swing from 0/1 V to 1/3.3 V has been shown in Fig. 3.18. Taper buffer 1 and taper buffer 2 are demanded to drive the output stage because the transistors in the output stage are large-size devices. Because the voltage swing of signal PU is from 1 V to 3.3 V, the INV1 in taper buffer 1 is shown in Fig. 3.21(b). The PMOS and NMOS transistors of INV1 are 2.5-V normal-Vt devices. Because the voltage swing of signal PD is from 0 V to 1 V, the INV2 in taper buffer 2 is shown in Fig. 3.21(c), where the PMOS and NMOS transistors of INV2 are 1-V normal-Vt transistors. In order to keep the signal PU and signal PD in phase, the delay of taper buffer 1 and level converter must be adjusted equal to that of taper buffer 2. In Fig. 3.21, the bulks of the transistors are connected to their sources, respectively, because of the body effect.

Fig. 3.22 shows the simulated waveforms on nodes IN, OUT, PU, and PD in the proposed output buffer with a 133-MHz 3.3-V output signal in a 0.13-μm 1/2.5-V CMOS process. The output load is 10 pF in this simulation. Because the parasitic inductance (15 nH) of the bond wire is also included in this simulation, the overshooting and undershooting of the output waveform can be found in Fig. 3.22. Table 3.1 summarizes the other simulation results of the proposed output buffer. The delay times are measured from the input signal (IN) of 0.5×VDD (0.5-V) voltage level to the output signal (OUT) of 0.5×VCC (1.65-V) voltage level. As shown in Table 3.1, the simulated rising delay time ($T_{d\text{-}rising}$) and falling delay time ($T_{d\text{-}falling}$) are 1.15 ns and 1.08 ns, respectively. The output rising time (T_{rising}) and falling time ($T_{falling}$) are defined form 0.1×VCC (0.33 V) to 0.9×VCC (2.97 V) and from 0.9×VCC (2.97 V) to 0.1×VCC (0.33 V), respectively. As shown in Table 3.1, the simulated T_{rising} and $T_{falling}$ are 0.85 ns and 0.73 ns, respectively. The output low current (I_{OL}) is defined when the output voltage is at 0.1×VCC (0.33 V). The output high current (I_{OH}) is defined when the output voltage is at 0.9×VCC (2.97 V). As shown in Table 3.1, the simulated I_{OL} and I_{OH} are 59.3 mA and 39.4 mA, respectively. The simulated power consumption is 29.77 mW when the proposed output buffer is operated in 133 MHz with 10-pF load at the pad. In this simulation, the proposed output buffer successfully drives the I/O pad according to the input signal IN.

3.2.5. Experimental Results

The proposed output buffer has been fabricated in a 0.13-μm 1/2.5-V 1P8M CMOS process with Cu interconnects. Fig. 3.23 shows the layout of the proposed output buffer. The layout area of the proposed output buffer is around 125 μm × 253 μm. Besides, the testchip also includes the stand-alone level converter to verify its logic functions and voltage levels. Fig. 3.24 shows the measured waveforms of the new proposed level converter. As shown in Fig. 3.24, the proposed level converter can successfully transfer the voltage swing from 0/1 V to 1/3.3 V. Fig. 3.25 shows the measured waveforms of the proposed output buffer operating with a 133-MHz 3.3-V output signal. As shown in Fig. 3.25, the proposed output buffer can successfully drive the output pad without gate-oxide overstress. Besides, the measured I_{OL} and I_{OH} of the proposed output buffer are 69.2 mA and 44.1 mA, respectively. Due to process variation, the measured I_{OL} and I_{OH} are slightly different from the simulated I_{OL} and I_{OH}.

3.2.6. Discussions

The hot-carrier degradation and the drain-to-bulk breakdown issues are the other reliability issues in the high-voltage-tolerant circuits. To avoid the hot-carrier degradation, the drain-to-source voltage (Vds) of the device operated in the saturation region can not be higher than the normal operating voltage [6]. For example, the Vds of the 1-V (2.5-V) device can not be higher than 1 V (2.5 V). The maximum Vds of 1-V devices and 2.5-V devices in the proposed output buffer are about 1 V and 2.3 V, respectively. Thus, the proposed output buffer not only considers the gate-oxide reliability issue but also the hot-carrier degradation issue. In general, the drain-to-bulk breakdown voltage is at least as twice as the normal operating voltage in the standard CMOS process [47], [48]. Hence, the drain-to-bulk breakdown issue can be ignored in the proposed output buffer.

3.2.7. Summary

An output buffer realized with low-voltage devices to drive high-voltage output signals is presented in this section. The proposed output buffer has been fabricated in a 0.13-μm 1/2.5-V CMOS process to drive 3.3-V signals without suffering high-voltage gate-oxide overstress. The experimental results have shown that the proposed output buffer can be successfully operated with a 133-MHz 3.3-V output signal. Moreover, a new level converter, which can convert the 0/1-V signal swing to 1/3.3-V signal swing, has been also verified in this section. The proposed output buffer and level converter are suitable for mixed-voltage interface applications in the nanometer CMOS processes.

3.3. Conclusion

In this chapter, an input buffer and an output buffer realized with 1/2.5-V low-voltage devices without gate-oxide reliability issue for 3.3-V applications are presented. Besides, a Schmitt trigger circuit for the input buffer and a level converter for output buffer are also presented in this chapter. The proposed input buffer and output buffer have been fabricated in a 0.13-μm 1/2.5-V CMOS process for 3.3-V application. The experimental results show that the proposed circuits can be operated in 133-MHz 3.3-V environment correctly.

TABLE 3.1

Simulation Results of the Proposed Output Buffer

Rising Delay Time ($T_{d\text{-rising}}$)	1.15 ns
Falling Delay Time ($T_{d\text{-falling}}$)	1.08 ns
Rising Time (T_{rising})	0.85 ns
Falling Time ($T_{falling}$)	0.73 ns
Output Low Current (I_{OL})	59.3 mA
Output High Current (I_{OH})	39.4 mA
Power Consumption	29.77 mW

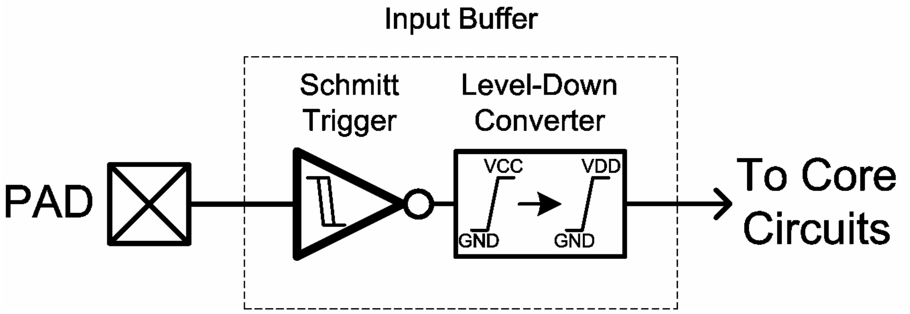
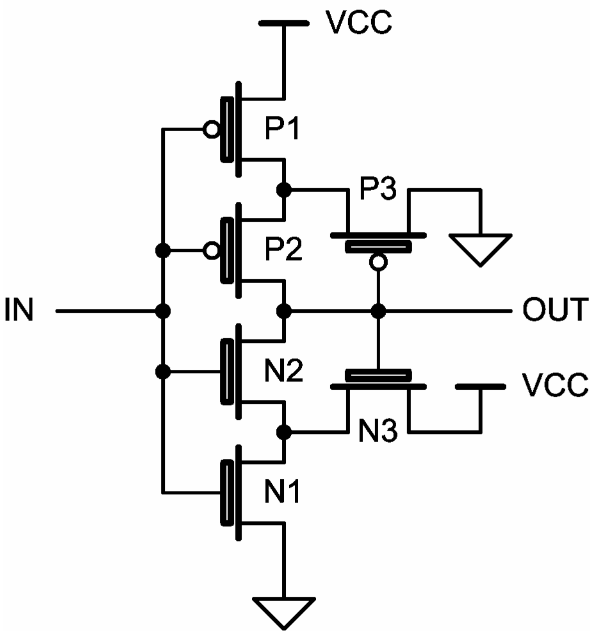
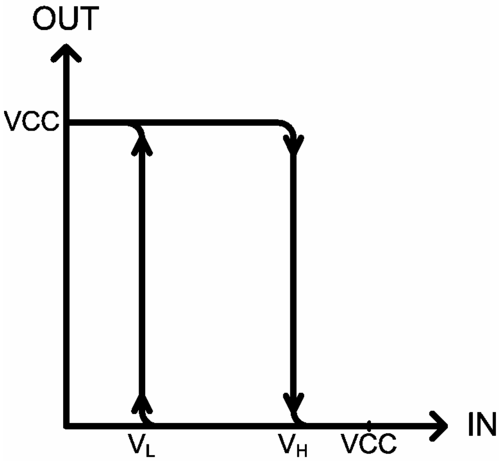


Fig. 3.1. Conventional input buffer in mixed-voltage interface.

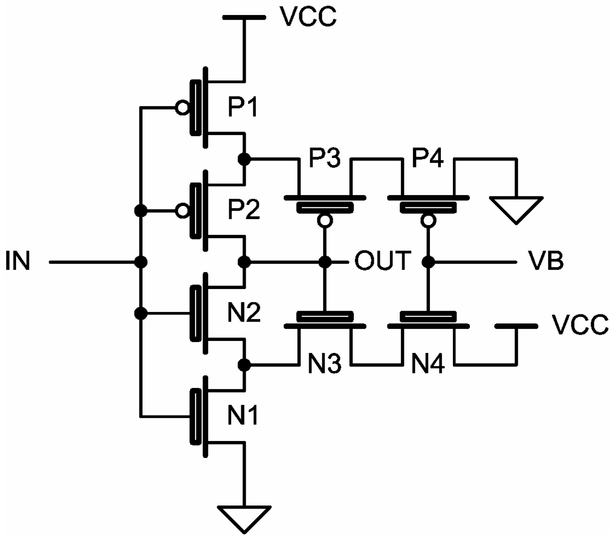


(a)

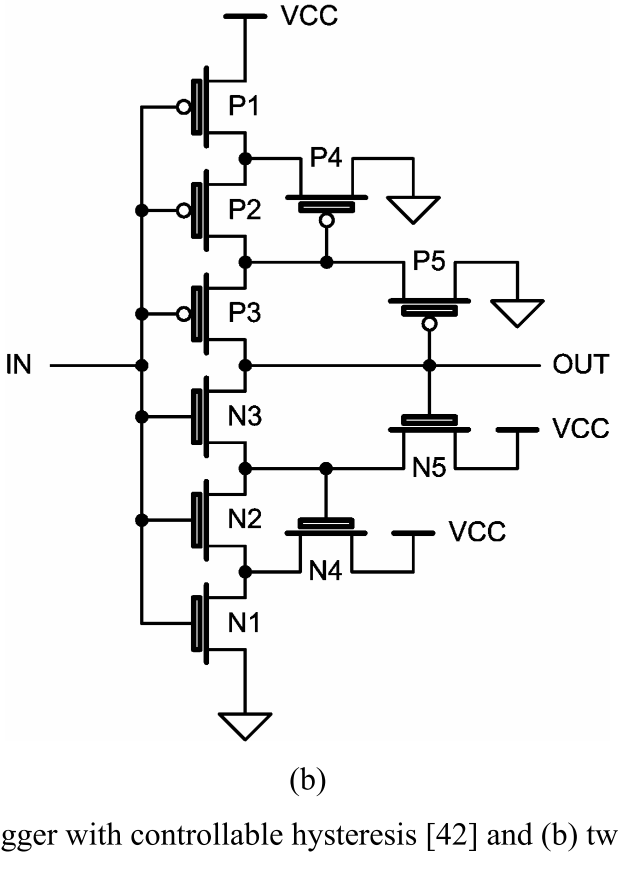


(b)

Fig. 3.2. (a) Circuit and (b) transfer curve of the conventional Schmitt trigger.



(a)



(b)

Fig. 3.3. (a) Schmitt trigger with controllable hysteresis [42] and (b) two-layer Schmitt trigger [43].

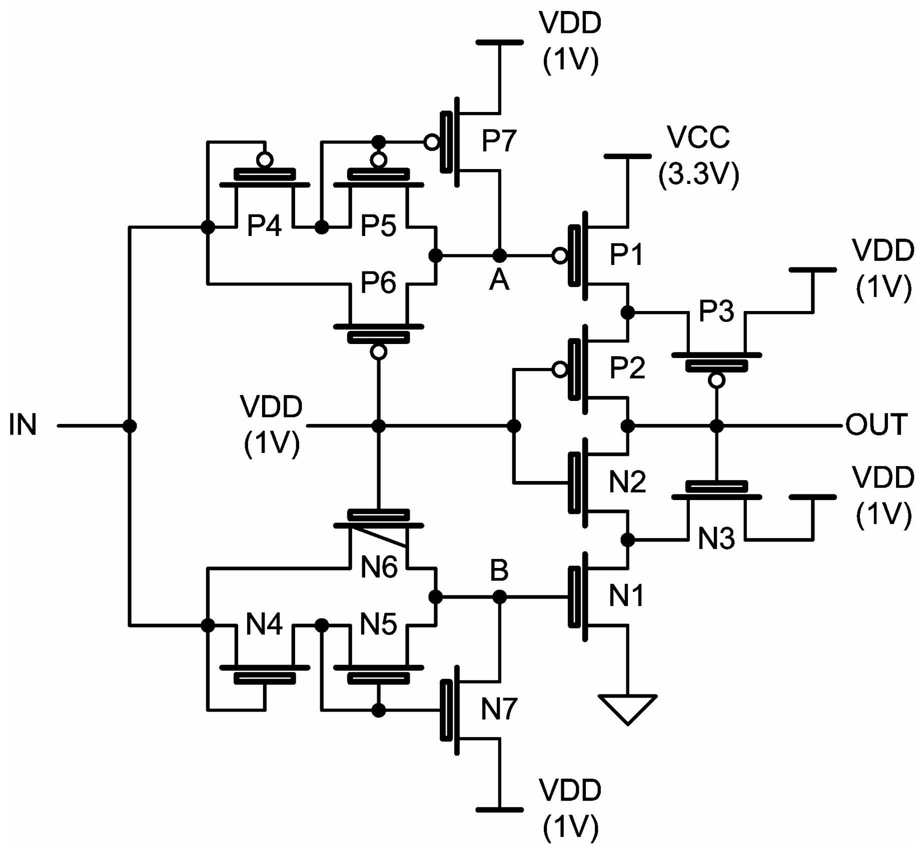


Fig. 3.4. New proposed Schmitt trigger (N6 is a native NMOS transistor).

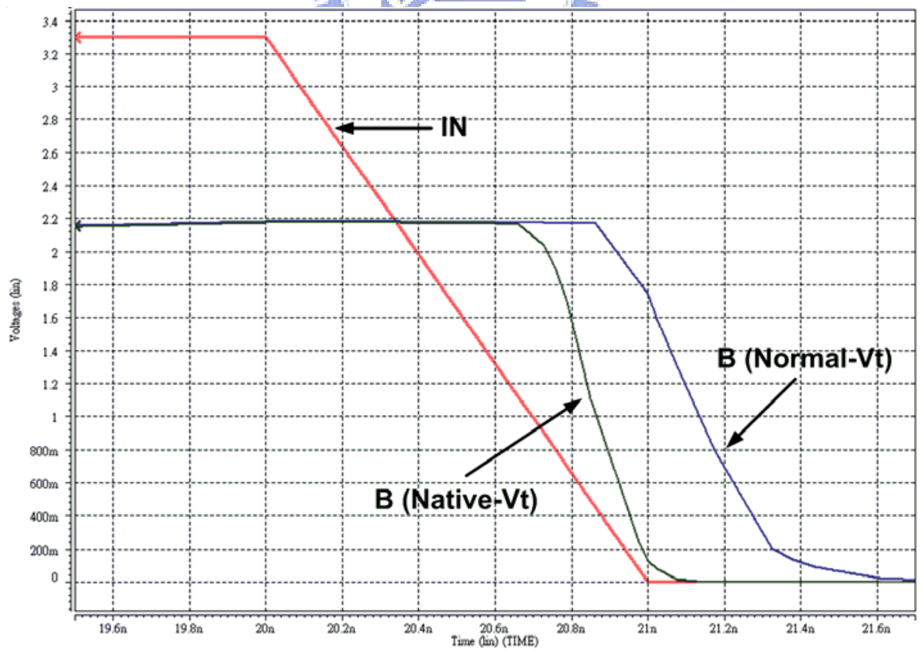


Fig. 3.5. Simulated waveforms at the nodes IN and B to compare the pull-down speed on the node B, when the transistor N6 is implemented by a native Vt device or a normal Vt device.

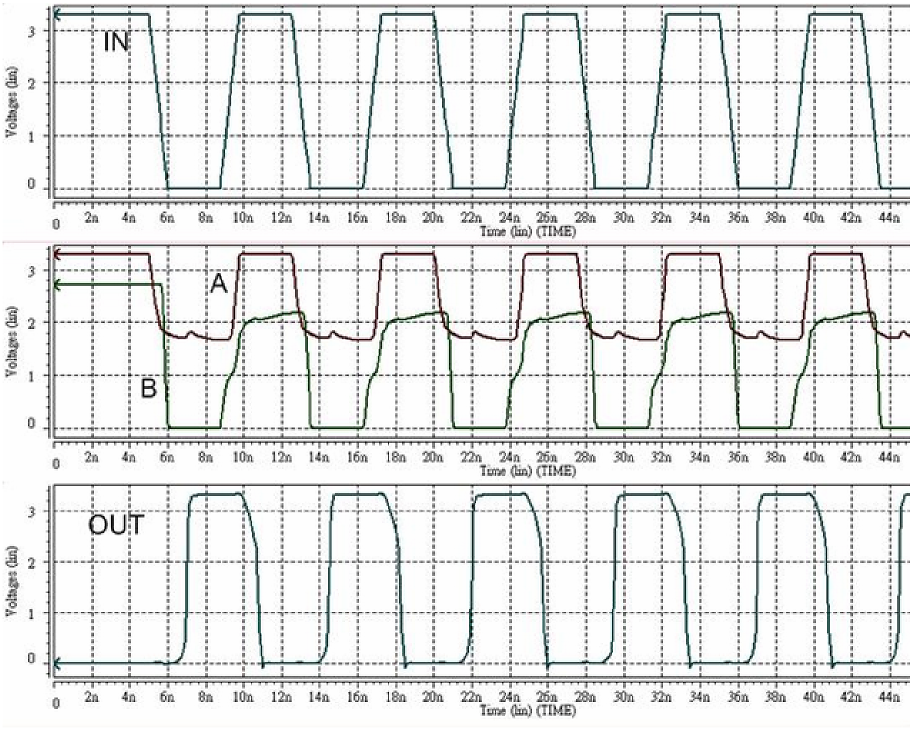


Fig. 3.6. Simulated waveforms at the nodes IN, OUT, A, and B of the new proposed Schmitt trigger circuit operating at 133 MHz.

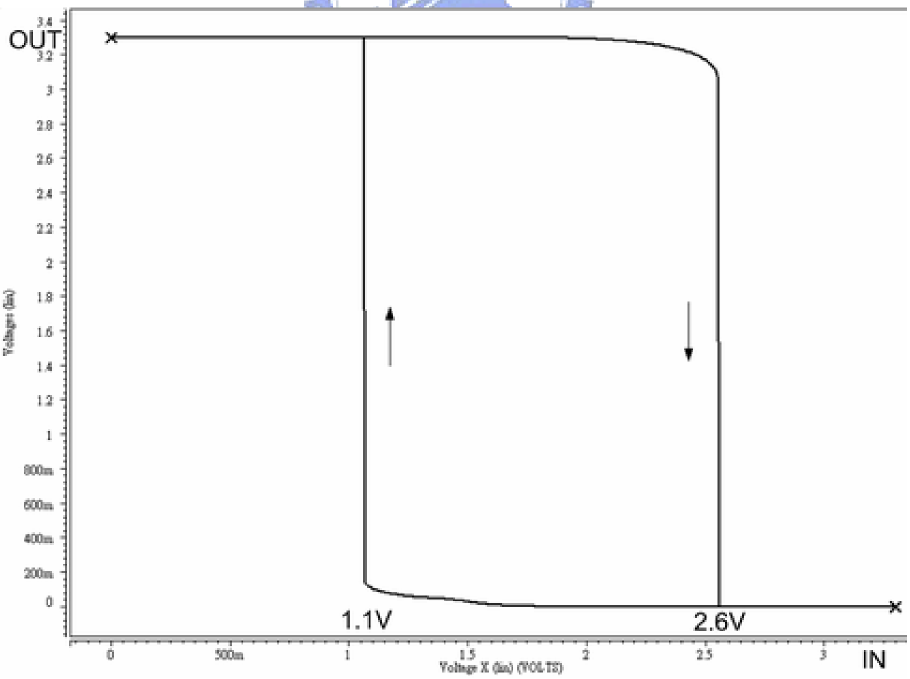


Fig. 3.7. Simulated transfer curve of the new proposed Schmitt trigger circuit.

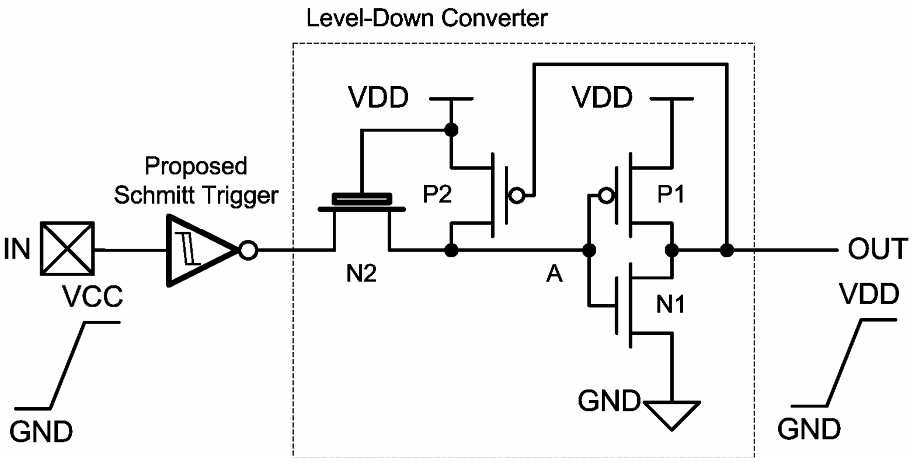


Fig. 3.8. Whole input buffer with the proposed Schmitt trigger circuit and the level-down converter.

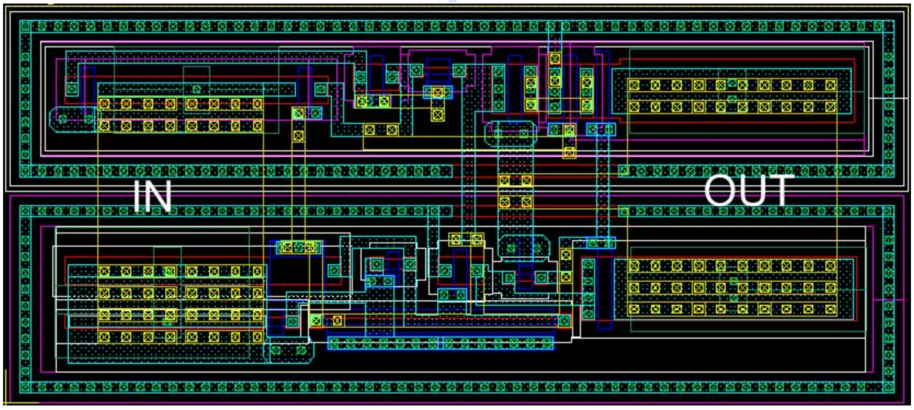


Fig. 3.9. Layout of the new proposed Schmitt trigger circuit in the 0.13-μm 1/2.5-V CMOS process.

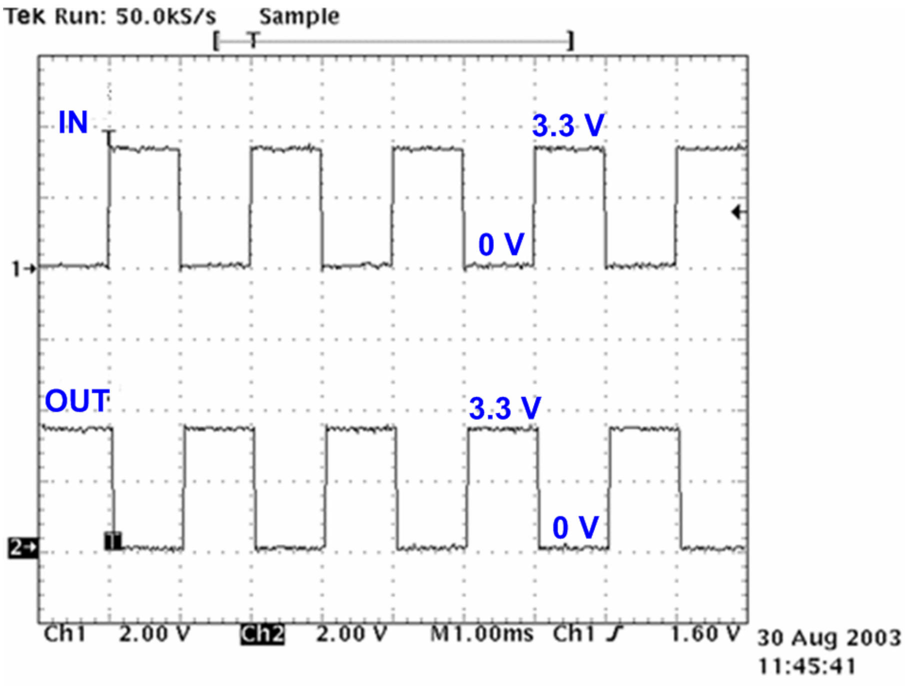


Fig. 3.10. Measured waveforms on nodes IN and OUT of the new proposed Schmitt trigger circuit.

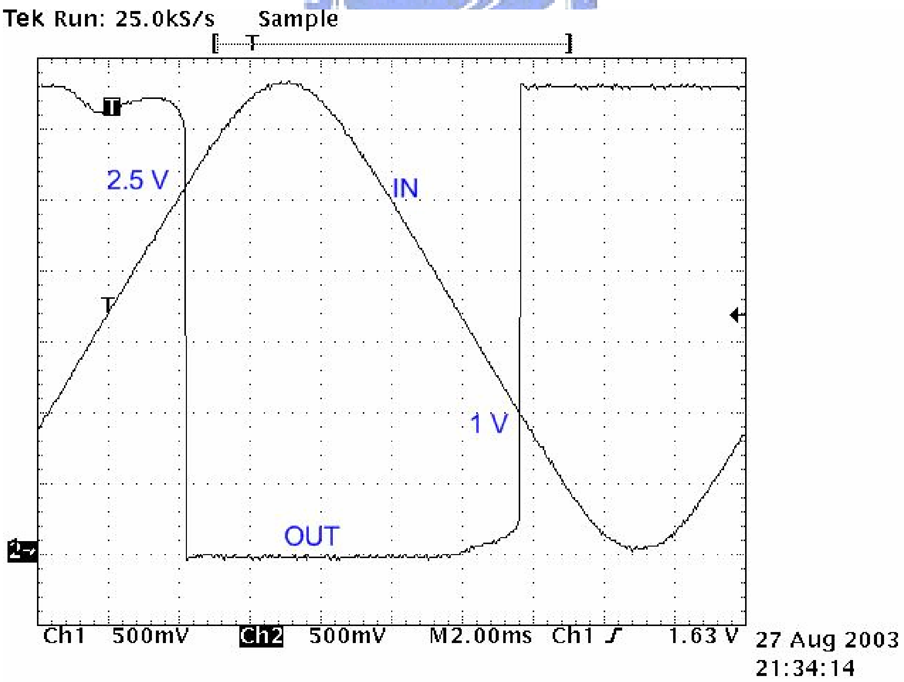


Fig. 3.11. Measured transition threshold voltages V_L and V_H of the new proposed Schmitt trigger circuit.

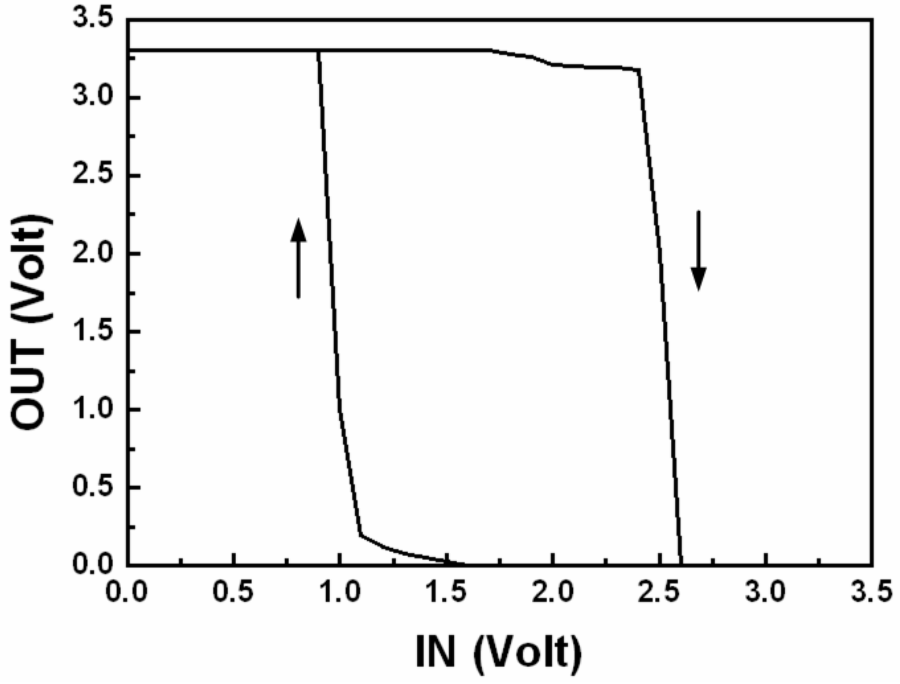


Fig. 3.12. Measured transfer curve of the new proposed Schmitt trigger circuit.

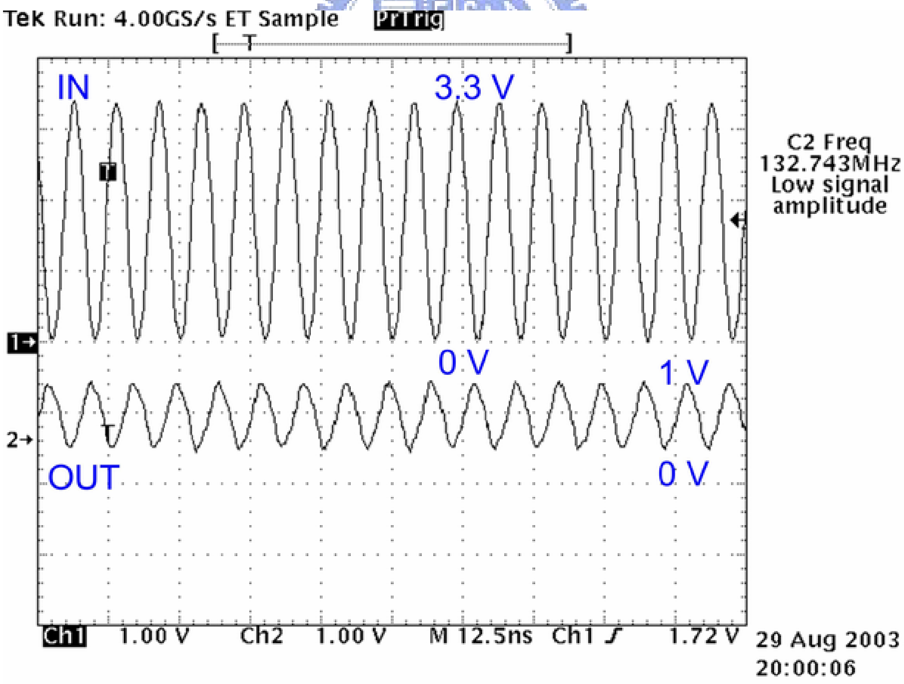


Fig. 3.13. Measured waveforms on node IN and OUT of the whole input buffer shown in Fig. 3.8.

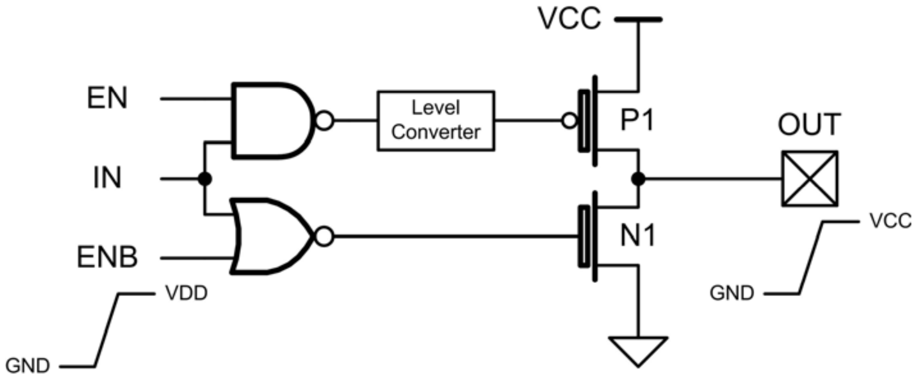


Fig. 3.14. Conventional tri-state output buffer co-designed with thin- and thick-oxide devices.

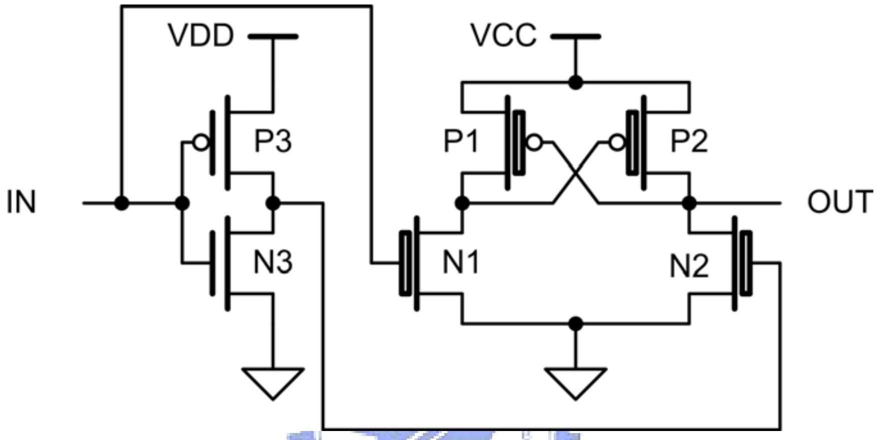


Fig. 3.15. Conventional level converter co-designed with thin-oxide and thick-oxide devices.

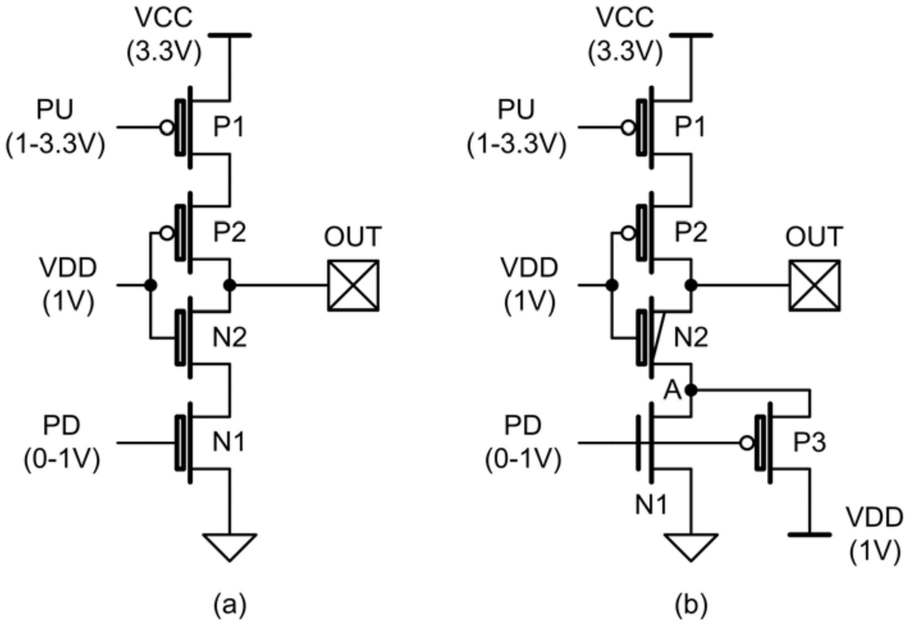


Fig. 3.16. The new proposed output stages realized in a 0.13-μm 1/2.5-V CMOS process (a) with all 2.5-V normal-Vt transistors, and (b) with 2.5-V native-Vt transistor N2 and 1-V normal-Vt transistor N1.

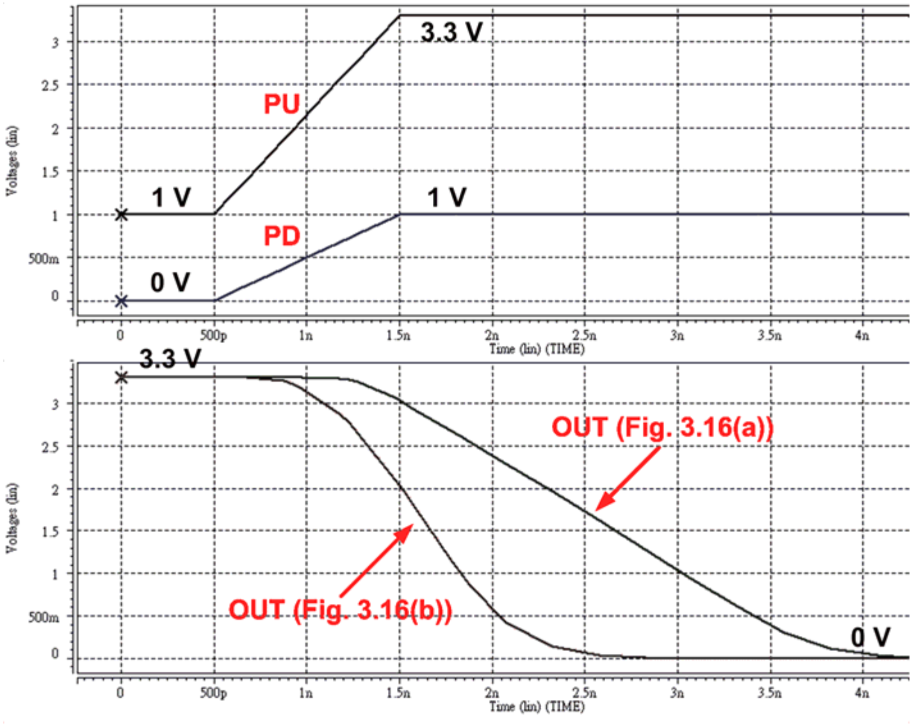


Fig. 3.17. Simulated waveforms of the output stages.

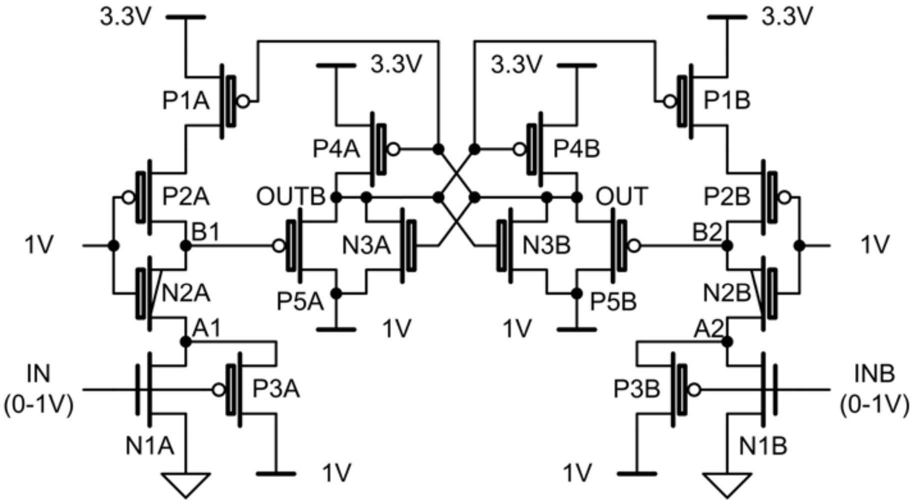


Fig. 3.18. Proposed level converter which can convert the 0/1-V signal swing to 1/3.3-V signal swing.

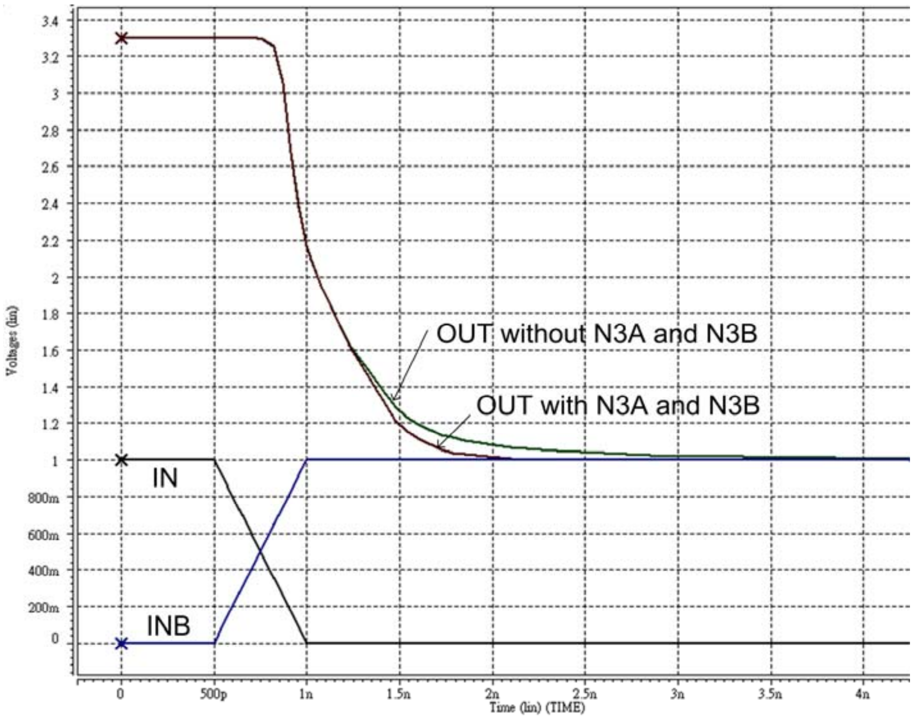


Fig. 3.19. Simulated waveforms of the new proposed level converter with or without transistors N3A and N3B.

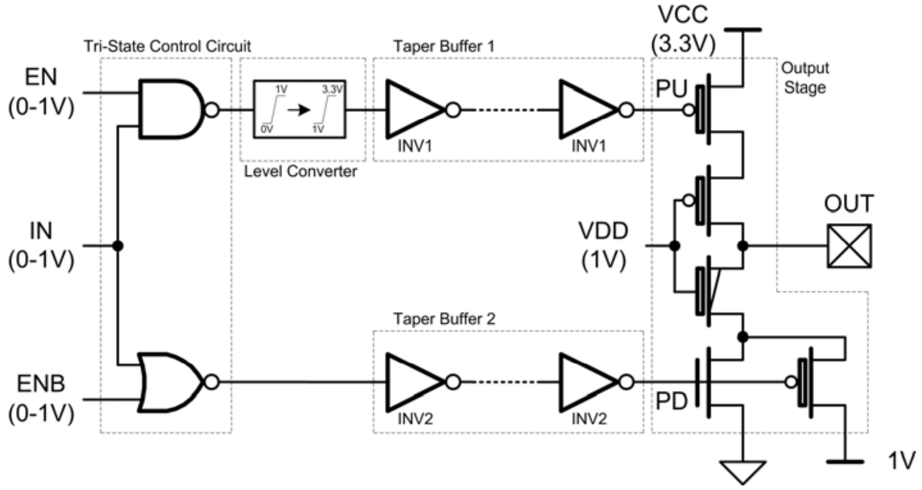


Fig. 3.20. Whole output buffer which drives 3.3-V output signal in the 0.13-μm CMOS process with only 1-V and 2.5-V devices.

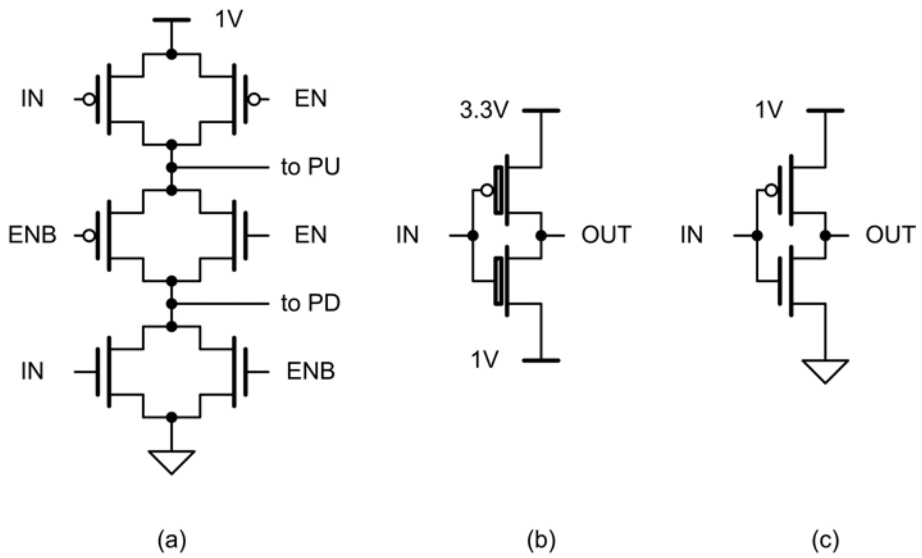


Fig. 3.21. Circuit implementation to realize the (a) tri-state control circuit, (b) INV1, and (c) INV2 in the whole output buffer.

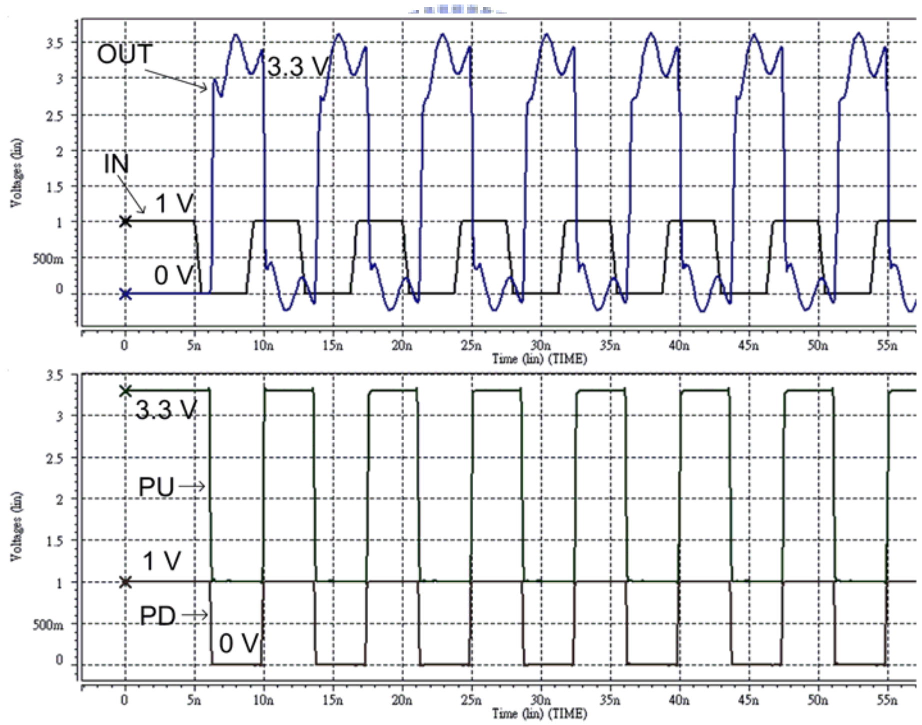


Fig. 3.22. Simulated waveforms of the proposed output buffer operating with a 133-MHz 3.3-V output signal in a 0.13-µm CMOS process with only 1-V and 2.5-V devices.

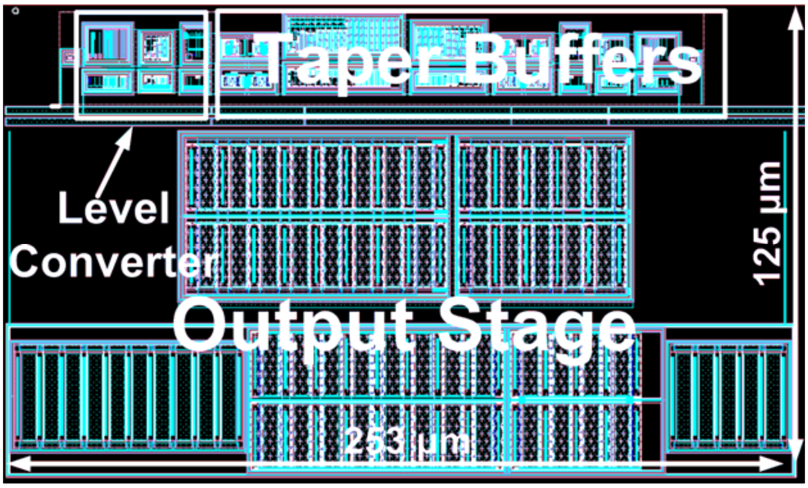


Fig. 3.23. Layout of the whole output buffer in a 0.13-µm 1/2.5-V CMOS process with Cu interconnects.

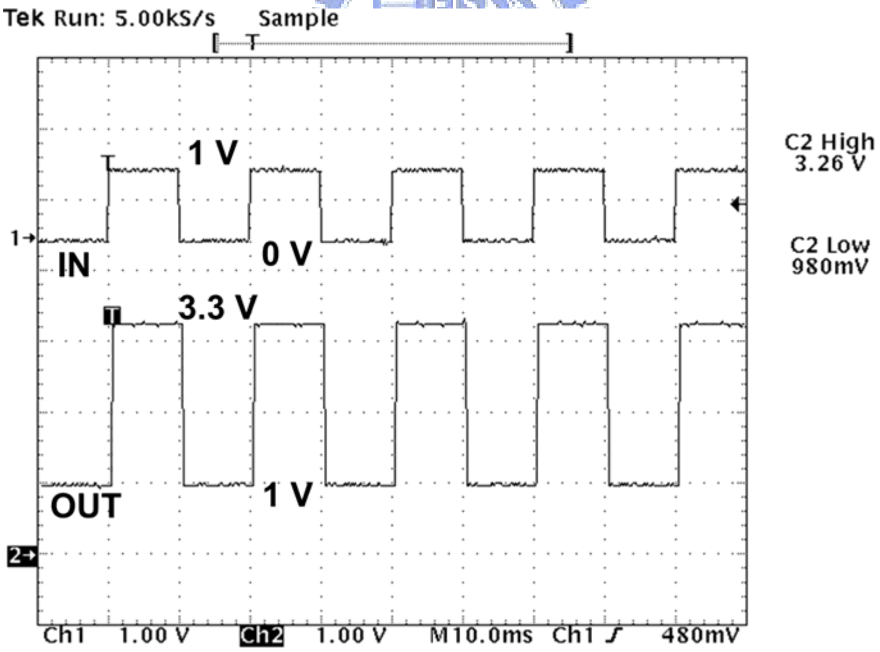


Fig. 3.24. Measured waveforms of the new proposed level converter, which convert the 0/1-V signal to a 1/3.3-V signal.

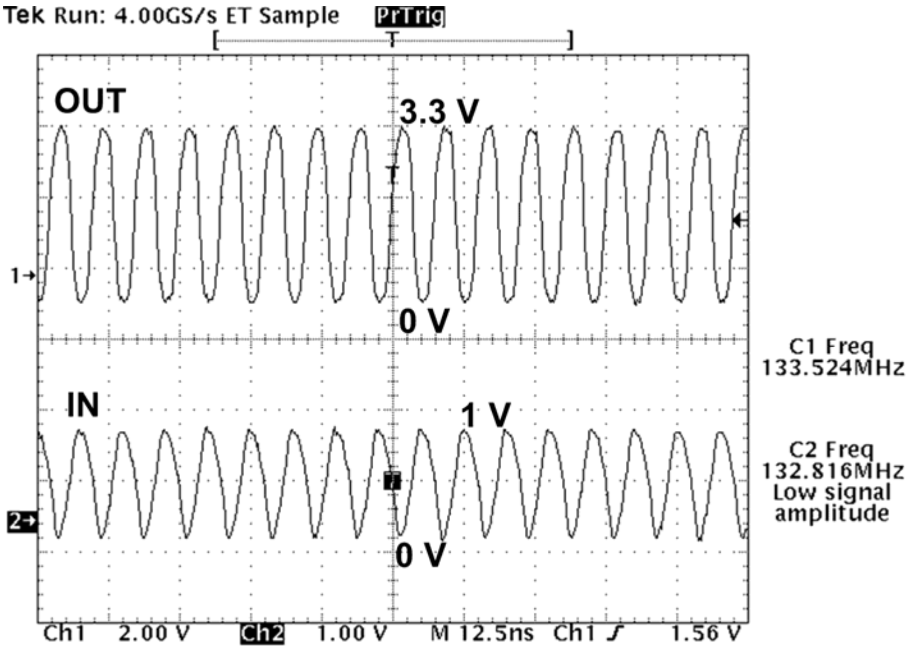


Fig. 3.25. Measured waveforms of the proposed whole output buffer operating with a 133-MHz 3.3-V output signal in a 0.13-µm CMOS process with only 1-V and 2.5-V devices.

CHAPTER 4

NMOS-Blocking Technique for Mixed-Voltage I/O Buffer Design

An NMOS-blocking technique for mixed-voltage I/O buffer realized with only 1×VDD devices can receive 2×VDD, 3×VDD, and even 4×VDD input signal without the gate-oxide reliability issue is presented in this paper. The 2×VDD input tolerant mixed-voltage I/O buffer by using the NMOS-blocking technique has been fabricated and verified in a 0.25-μm 2.5-V CMOS process to serve 2.5/5-V mixed-voltage interface. The 3×VDD input tolerant mixed-voltage I/O buffer by using the NMOS-blocking technique has been fabricated and verified in a 0.13-μm 1-V CMOS process to serve 1/3-V mixed-voltage interface. The proposed NMOS-blocking technique can be extended to design the 4×VDD, 5×VDD, and even 6×VDD input tolerant mixed-voltage I/O buffers. The limitation of the NMOS-blocking technique is the breakdown voltage of the pn-junction in the given CMOS process.

4.1. NMOS-Blocking Technique

4.1.1. Background

Several mixed-voltage I/O buffers realized with the low-voltage (thin-oxide) devices have been reported to save the wafer fabrication cost [24]-[26]. Fig. 4.1 depicts the design concept of the traditional mixed-voltage I/O buffer realized with only low-voltage devices [24]-[26]. As shown in Fig. 4.1, the stacked NMOS devices, MN0 and MN1, are used to overcome the high-voltage overstress on their gate oxide. Because the gate terminal of the transistor MN0 is connected to VDD, the maximum drain voltage of the transistor MN1 is about VDD−Vt, where Vt is the threshold voltage of NMOS. Hence, the gate-drain voltages and the gate-source voltages of the stacked devices, MN0 and MN1, are limited below VDD even if the input signal on the I/O pad is 2×VDD in the receive mode. The dynamic n-well bias circuit and the gate-tracking circuit in Fig. 4.1 are designed to prevent the leakage current path through the parasitic drain-to-well pn-junction diode in the pull-up PMOS device and the leakage current path due to the incorrect conduction of the pull-up PMOS device, respectively. In the transmit mode, the dynamic n-well bias circuit has to keep the floating n-well at VDD. So, the threshold voltage of the pull-up PMOS device isn't increased due to the body effect. In the transmit mode, the dynamic gate-tracking circuit should pass the output signal from the upper port of the pre-driver to the gate terminal of the pull-up PMOS device. In the receive mode with a 2×VDD input signal, the dynamic n-well bias circuit will charge the floating n-well to 2×VDD to prevent the leakage current from the I/O pad to the power supply (VDD) through the parasitic pn-junction diode. When the input signal at the I/O pad is GND, the dynamic n-well bias circuit will keep the floating n-well at VDD. In the receive mode, the gate voltage of the pull-up PMOS device is controlled at VDD or 2×VDD according to the input signal on the I/O pad in order to prevent the leakage current path from the I/O pad to the power supply (VDD) through the pull-up PMOS. As shown in Fig. 4.1, the extra transistors, MN2 and MP1, are added in the input buffer. Transistor MN2 is used to limit the voltage level of the input signal reaching to the gate oxide of the inverter INV. Because the gate terminal of transistor MN2 is connected to VDD, the input node of the inverter INV will rise up to VDD−Vt when the input signal at the I/O pad is 2×VDD in the tri-state input mode. Then, the transistor MP1 is used to pull up the input node of inverter INV to VDD when the output node of the inverter INV is pulled down to GND. Therefore, the gate-oxide reliability problem occurring in the input buffer can be solved.

Realized with the low-voltage devices, the prior mixed-voltage I/O buffers [24]-[26] only can receive 2×VDD input signals without suffering the gate-oxide overstress. In this chapter, the NMOS-blocking technique is presented to design the mixed-voltage I/O buffers. By using the proposed NMOS-blocking technique, not only the 2×VDD input tolerant mixed-voltage I/O buffer but also the 3×VDD and even 4×VDD input tolerant mixed-voltage I/O buffers can be achieved [53], [54]. The 2×VDD and 3×VDD input tolerant mixed-voltage I/O buffers designed with the proposed NMOS-blocking technique have been successfully verified in a 0.25-μm 2.5-V CMOS process to serve the 2.5/5-V mixed-voltage interface and in a 0.13-μm 1-V CMOS process with Cu interconnects to serve the 1/3-V mixed-voltage interface, respectively. The proposed NMOS-blocking technique can be extended to design the 4×VDD, 5×VDD, and even 6×VDD input tolerant mixed-voltage I/O buffers. The limitation of the NMOS-blocking technique is the breakdown voltage of the pn-junction in the given CMOS process.

4.1.2. NMOS-Blocking Technique

In an NMOS transistor as shown in Fig. 4.2, if its drain voltage (Vd) is higher than its gate voltage (Vg), the source voltage (Vs) of this NMOS device will be pulled up to Vg−Vt, where Vt is the threshold voltage of the NMOS transistor. For example, when the Vg is controlled at VDD and Vd is at 2×VDD, Vs is only pulled up to VDD−Vt. Therefore, the feature of NMOS device can be applied to design the mixed-voltage I/O buffer without the gate-oxide reliability issue and the undesired leakage currents.

Fig. 4.3 depicts the design concept of the proposed NMOS-blocking technique for mixed-voltage I/O buffer. The protection devices in Fig. 4.3 are used to block from the high-voltage input signal on the I/O pad to stress the input buffer and the output buffer of the mixed-voltage I/O circuit. As the I/O buffer is in the transmit mode, the protection devices in Fig. 4.3 have to pass the signal from node 1 to the I/O pad. As the I/O buffer is in the receive mode, the protection devices not only limit the high-voltage level of the input signal but also pass the signal information from the I/O pad to node 1. The gate voltages of the protection devices must be well controlled in both the transmit mode and the receive mode. As shown in Fig. 4.3, the mixed-voltage I/O buffer can receive (n+1)×VDD input signal without gate-oxide reliability issue by using n protection devices, where n is an integer.

4.2. 2×VDD Input Tolerant Mixed-Voltage I/O Buffer

4.2.1. Circuit Implementation

Fig. 4.4 shows the proposed 2×VDD input tolerant mixed-voltage I/O buffer by using the NMOS-blocking technique [53]. In Fig. 4.4, VDDH is as high as 2×VDD, which can be generated by an on-chip charge pump circuit with 1×VDD devices or other high-voltage generators. As shown in Fig. 4.4, transistor MN1 is used to protect the conventional I/O buffer from the input high-voltage overstress. The pre-driver can generate signals PU and PD to control the output transistors, MP0 and MN0. The dynamic gate-bias circuit in Fig. 4.4 is used to control the gate voltage of the protection transistor MN1. Table 4.1 lists the operation of the dynamic gate-bias circuit in the proposed 2×VDD input tolerant mixed-voltage I/O buffer. When this I/O buffer is in the receive mode, the gate terminal (node 2) of transistor MN1 is biased at VDD by the dynamic gate-bias circuit, whereas transistors MP0 and MN0 are both turned off by the pre-driver. At this moment, if an input signal of logic low (GND) is received from the I/O pad, node 1 is discharged to GND through transistor MN1, and this input signal can be successfully transferred to the node Din of the input buffer. When a logic high (2×VDD) signal is received from the I/O pad, the gate terminal of transistor MN1 is still biased at VDD, so the voltage on node 1 is pulled up to VDD−Vt. Because the voltage on node 1 is at VDD−Vt, the signal Din is pulled down to GND. A feedback device MP1 is added to restore the voltage level on node 1 to VDD, which avoids the undesired static dc current through the inverter INV in the input buffer. In this design, transistors MN1 and MP1 with the inverter INV can convert the 2×VDD input signal to VDD signal successfully. Therefore, transistor MN1 can protect the I/O buffer without suffering high-voltage overstress on the gate oxide.

Fig. 4.5 depicts the dynamic gate-bias circuit in the proposed 2×VDD input tolerant I/O buffer, where transistors MP2 and MP3 are designed with the cross-coupled structure. If the gate voltage of transistor MP2 (or MP3) is pulled down, this transistor is turned on and pulls up the gate voltage of the other transistor to VDDH to turn it off. For example, if the voltage on node 5 in Fig. 4.5 is lower than VDDH−Vt and the voltage on node 6 is VDDH, transistor MN2 is turned on to keep the node 5 at VDD. In Fig. 4.5, capacitors C1 and C2 are used to couple the signals from nodes 3 and 4 to nodes 5 and 6, respectively. The voltages across these capacitors, C1 and C2, are always VDD, because the voltage levels on the top and bottom plates of capacitors C1 and C2 are either VDD and GND or 2×VDD and VDD. With these capacitors, when the voltage level on node 3 is changed from VDD to GND, the voltage on node 5 is pulled down to VDD and then the voltage level on node 6 is pulled up to 2×VDD by transistor MP3. On the contrary, when the voltage level on node 4 is converted from VDD to GND, that on node 6 is pulled to VDD, and that on node 5 is pulled up to 2×VDD by transistor MP2.

Initially, the voltages on nodes 3, 4, 5, and 6 in Fig. 4.5 could be unknown. If the voltages on nodes 5 and 6 are 2×VDD and VDD, and the voltages on nodes 3 and 4 are GND and VDD, the voltages across capacitors C1 and C2 are 2×VDD and VDD, respectively, instead of both VDD. In order to overcome this initial problem, the diode strings, DS1 and DS2, are added. The turn-on voltages of the diode strings are designed to a little higher than VDD by using multiple diodes in stacked configuration. In order to prevent the leakage current path to the grounded p-type substrate, the diode-connected MOSFET or polysilicon diode [55] is suggested. With these diode strings, if the voltage on node 3 is at GND and that on node 4 is at VDD, the voltage on node 5 is clamped at the turn-on voltage, which is a little higher than VDD, of the diode string DS1. Therefore, transistor MP3 is turned on to pull up the voltage on node 6 to 2×VDD. Thus, the voltages across capacitors C1 and C2 are both VDD.

In the proposed 2×VDD input tolerant mixed-voltage I/O buffer, the bulk of the protection device, MN1, can be coupled to GND without the gate-oxide overstress, even if the gate voltage of transistor MN1 may be as high as 2×VDD. The reason is that this protection device, MN1, is always turned on and the voltage across the gate oxide of transistor MN1 is from the gate to the conducting channel, but not from the gate to its bulk. Thus, the gate oxides of all NMOS devices in the dynamic gate-bias circuit are also safe because these NMOS devices are turned on when their gates are pulled up to 2×VDD.

4.2.2. Simulation and Experimental Results

The proposed 2×VDD input tolerant mixed-voltage I/O buffer has been verified in a 0.25-μm 2.5-V CMOS process to serve 2.5/5-V mixed-voltage interface. Fig. 4.6 shows the simulated waveforms of the proposed 2×VDD input tolerant mixed-voltage I/O buffer in the receive mode to receive the input signal of 0-to-5 V. As shown in Fig. 4.6, the gate voltage (node 2) of the transistor MN1 is always kept at 2.5 V in the receive mode, and the voltage swing on node 1 is from 0 V to 2.5 V. Fig. 4.7 shows the simulated waveforms of the proposed 2×VDD input tolerant mixed-voltage I/O buffer in the transmit mode. When the voltage on node 1 is raised up to 2.5 V, the gate voltage of the transistor MN1 is also raised to ~5 V at the same time to turn on the transistor MN1. Then, the voltage on the I/O pad is pulled up to 2.5 V. When the voltage on node 1 is dropped to 0 V, the gate voltage of the transistor MN1 is kept at 2.5 V to prevent from the high-voltage overstress on the gate oxide of the protection device MN1. The voltage on the I/O pad is therefore dropped to 0 V. With the dynamic gate-bias circuit, the proposed mixed-voltage I/O buffer can successfully transfer signals in full swing to the I/O pad through the protection device MN1.

Fig. 4.8 shows the chip photograph of the proposed 2×VDD input tolerant I/O buffer fabricated in a 0.25-μm 2.5-V CMOS process. Figs. 4.9 and 4.10 show the measured voltage waveforms on the node Dout and the I/O pad of the proposed 2×VDD input tolerant I/O buffer in the receive mode and in the transmit mode, respectively. As shown in Figs. 4.9 and 4.10, the proposed 2×VDD mixed-voltage I/O buffer by using the NMOS-blocking technique can be correctly operated in the 2.5/5-V mixed-voltage interface.

4.3. 3×VDD Input Tolerant Mixed-Voltage I/O Buffer

4.3.1. Circuit Implementation

Fig. 4.11 depicts the proposed 3×VDD input tolerant mixed-voltage I/O buffer by using the NMOS-blocking technique [54]. VDD is the applied power supply voltage, whereas VDDH (2×VDD) can be generated by an on-chip charge pump circuit with 1×VDD devices from VDD. The output voltage of the on-chip charge pump circuit is shared by all mixed-voltage I/O circuits in the same chip. The protection devices, MN1 and MN2, controlled by the dynamic gate-bias circuit are used to avoid the high-voltage overstress on the gate oxide. The detailed operation of the dynamic gate-bias circuit is listed in Table II. When this I/O buffer transmits a logic low (GND), the gate voltages of transistors MN1 and MN2 are controlled at VDD, so the logic low can be transmitted from node 1 to the I/O pad. When this I/O buffer transmits a logic high (VDD), the gate voltages of transistors MN1 and MN2 are controlled at VDDH, so the logic high can be transmitted from node 1 to the I/O pad. When this I/O buffer receives a logic low (GND), the gate voltages of transistors MN1 and MN2 are biased at VDD. Thus, the logic low signal can be transmitted to node 1 from the I/O pad. When this I/O buffer receives a logic high (3×VDD), the gate voltages of transistors MN1 and MN2 are biased at VDD and VDDH, respectively. In the 3×VDD receive mode, the voltage on node 2 (node 1) is pulled up to VDDH−Vt (VDD−Vt), where Vt is the threshold voltage of transistors. Then, the signal Din is pulled down to GND to turn on transistor MP1. Finally, the voltage on node 1 is fully restored to VDD, so the inverter INV has no dc leakage current. In this 3×VDD input tolerant mixed-voltage I/O buffer, the gate-drain, gate-source, and drain-source voltages of every transistor don't exceed VDD. Thus, the proposed mixed-voltage I/O buffer with 1×VDD devices in Fig. 4.11 can tolerate 3×VDD input signals without the gate-oxide reliability issue.

According to Table 4.2, the dynamic gate-bias circuit in the proposed 3×VDD input tolerant mixed-voltage I/O buffer can be designed. Fig. 4.12 shows the dynamic gate-bias circuit in the proposed 3×VDD input tolerant mixed-voltage I/O buffer. In both transmit and receive modes, the signal PU has an inverting logic level of node 3. The voltage swing of signal PU is from GND to VDD, but that of node 3 is from VDD to VDDH. Thus, a GND/VDD-to-VDD/VDDH level converter followed by an inverter can be used to generate the signal level of node 3 to control the gate of the transistor MN1. In the transmit mode, node 3 has the same signal level of node 4. Thus, nodes 3 and 4 are connected by the transistor MP4, whose gate is connected to node 2 to avoid the gate-oxide overstress. The voltage on node 5 must be biased at VDD and VDDH alternately in the transmit mode due to the gate-oxide reliability issue of the transistor MN3. When the I/O buffer transmits a logic low, the gate voltages of transistors MN1 and MN2 are kept at VDD, and transistor MP3 is turned on to keep the voltage level on node 5 at VDD. When the I/O buffer transmits a logic high (GND), the gate voltages of transistors MN1 and MN2 are kept at VDDH, and transistor MN6 is turned on to keep the voltage level on node 5 at VDD. The gate-drain and gate-source voltages of transistor MN3 are always lower than VDD in the transmit mode, so there is no gate-oxide overstress issue on transistor MN3.

The gate voltage (node 3) of transistor MN1 is always kept at VDD in the receive mode. The gate voltage (node 4) of transistor MN2 is controlled at VDD or VDDH by the input signal on the I/O pad. When the I/O buffer receives a logic high (3×VDD), the voltage on node 5 is pulled up to the voltage level of 3×VDD−Vt through the diode-connected transistor MN8. At this moment, transistors MN3 and MN4 are turned on to pull the voltages on nodes 4 and 2 both up to VDDH. When the I/O buffer receives a logic low (GND), transistor MP4 is turned on to pull the voltage on node 4 down to VDD because the voltage on node 3 is VDD. At this moment, transistor MP3 is turned on to pull the voltage on node 5 down to VDD to prevent the gate-oxide overstress on transistor MN3. In addition, transistors MP2, MN5, and MN7 can protect transistors MN4, MP3, and MN6 against the gate-oxide overstress.

4.3.2. Simulation and Experimental Results

The proposed 3×VDD input tolerant mixed-voltage I/O buffer has been verified in a 0.13-μm 1-V CMOS process with Cu interconnect to serve 1/3-V mixed-voltage interface. Fig. 4.13 shows the simulated voltage waveforms of the proposed 3×VDD input tolerant mixed-voltage I/O buffer in the receive mode to receive 3-V input signals. The simulated waveforms in Fig. 4.13 are all consistent to our design expectation. Although the transient peak voltage on node 4 could be larger than 2 V due to the parasitic gate-drain capacitance (Cgd) of transistor MN2, the gate-drain and gate-source voltages of transistor MN2 are still kept lower than 1 V. Fig. 4.14 shows the simulated voltage waveforms of the proposed 3×VDD input tolerant mixed-voltage I/O buffer in the transmit mode to drive 1-V output signals. The simulated waveforms in Fig. 4.14 are also consistent to our design expectation. The gate-drain and gate-source voltages of all devices in the proposed 3×VDD mixed-voltage I/O buffer don't exceed 1 V, which has been confirmed in SPICE simulation.

Fig. 4.15 shows the layout of the proposed 3×VDD input tolerant I/O buffer fabricated in a 0.13-µm 1-V CMOS process with Cu interconnects. The active area of the proposed 3×VDD input tolerant I/O buffer is around 70×150 μm^2. Figs. 4.16 and 4.17 show the measured voltage waveforms of the proposed 3×VDD input tolerant I/O buffer in the receive mode and in the transmit mode, respectively. As shown in Fig. 4.16, the proposed 3×VDD input tolerant I/O buffer can successfully receive 3-V input signals in the receive mode. As shown in Fig. 4.17, the proposed 3×VDD input tolerant I/O buffer can successfully drive 1-V output signals in the transmit mode.

4.4. Discussions

4.4.1. Limitation of the NMOS-Blocking Technique

Ideally, the proposed NMOS-blocking technique can be used to design the (n+1)×VDD input tolerant mixed-voltage I/O buffer when n protection devices are applied, as shown in Fig. 4.3. Fig. 4.18 shows the design example of the 4×VDD input tolerant mixed-voltage I/O buffer by using the proposed NMOS-blocking technique. Three protection devices, MN1, MN2, and MN3, are applied in Fig. 4.18, so this mixed-voltage I/O buffer can receive 4×VDD input signals. Thus, the dynamic gate-bias circuit requires the VDDH1 (2×VDD) and VDDH2 (3×VDD) voltage levels to control the gates of the protection devices, MN1, MN2, and MN3. In Fig. 4.18, the charge pump circuits realized with 1×VDD devices can also generate the VDDH1 and VDDH2 voltage levels.

Actually, the NMOS-blocking technique will be limited by the pn-junction breakdown voltage in the CMOS process. If the input voltage is larger than the pn-junction breakdown voltage, the parasitic pn-junction diode of the protection device which is closed to the I/O pad will break down. For example, the pn-junction breakdown voltage is around 8~9 V in the 0.13-µm 1-V CMOS process. Thus, the 8×VDD input tolerant mixed-voltage I/O buffer could be designed in the 0.13-µm 1-V CMOS process by using the proposed NMOS-blocking technique.

4.4.2. Gate-Oxide Overstress

Gate-oxide breakdown is a time-dependent issue [9], [56], [57]. The time period during the voltage overstress on the gate oxide of device is accumulated to induce the oxide breakdown. Therefore, the DC stress is more harmful to the gate oxide than the short AC stress (transient stress). Most of the I/O circuits in mixed-voltage applications only focus on the DC stress because the DC stress will damage the gate oxide shortly [24]-[26]. In order to solve the AC stress, the precise resistors and (or) capacitors with special bias circuit are required to detect the transient voltages and then to bias the output transistors [15], [16]. However, these resistors and capacitors occupy large silicon area. In addition, the special bias circuit [16] may consume DC current because of using the resistors and capacitors to implement the bias circuit.

In the mixed-voltage I/O buffers by using the proposed NMOS-blocking technique, the gate-drain and gate-source voltages of devices don’t exceed VDD in both receive and transmit modes. Thus, the proposed mixed-voltage I/O buffers don’t have the DC gate-oxide reliability issue. Due to the parasitic resistance, inductance, and capacitances, the gate-source voltage and gate-drain voltage may exceed VDD when the input or output signals have transitions. However, the AC overstress on the gate oxide is less serious than the DC overstress.

4.4.3. Hot-Carrier Degradation

The hot-carrier degradation becomes serious when the drain-source voltage of transistor operated in saturation mode is larger than the normal operating voltage (VDD). The hot-carrier degradation is also a time-dependent issue [6]-[8]. In both receive and transmit modes, the drain-source voltages of transistor in the proposed mixed-voltage I/O buffers don’t exceed VDD. In the proposed mixed-voltage I/O buffers, the hot-carrier degradation may occurs only during the transition when the proposed mixed-voltage I/O buffers receive high-voltage input signals and then transmit the GND output signals. To reduce this hot-carrier impact, the devices which suffer the hot-carrier issue in the proposed mixed-voltage circuits should be drawn with longer channel width. In [15], the special bias technique can also be used to prevent the hot-carrier degradation.

4.4.4. Speed Degradation of the NMOS-Blocking Technique

The proposed NMOS-blocking technique uses the NMOS protection devices to block from high-voltage input signals on the I/O pad. Thus, the mixed-voltage I/O buffer designed with this NMOS-blocking technique can be simply seen as a traditional tri-state I/O buffer cascaded with a resistor (R), as shown in Fig. 4.19. This resistor represents the equivalent resistance of the protection devices. If the equivalent resistance of the protection devices is large, the speed performance will be degraded. Thus, the dimensions of the protection devices must be designed large enough to minimize the equivalent resistance. However, the large dimension device has large drain (source) capacitance, so that the parasitic capacitance on node 1 in Fig. 4.19 is also somewhat increased to degrade the speed performance. Thus, the dimensions of the protection devices should be optimized according to the given CMOS process.

4.4.5. Advantages of the NMOS-Blocking Technique

Generally, the traditional mixed-voltage I/O buffers can only receive 2×VDD input signal without gate-oxide reliability issue [24]-[26]. However, the proposed NMOS-blocking technique can be extended to design not only the 2×VDD but also 3×VDD and even 4×VDD input tolerant mixed-voltage I/O buffers. Besides, the dynamic n-well bias technique is usually applied in the traditional mixed-voltage I/O buffers [24]-[26], where the voltage on the n-well is not fixed. The latch-up guard rings must be well surrounded when the voltage on the n-well is changed. Because the voltage of the n-well in the proposed mixed-voltage I/O buffers by using the NMOS-blocking technique is fixed, there is no transient latchup problem in the proposed mixed-voltage I/O circuits.

4.4.6. Duty Cycle

Due to the protection devices, the duty cycle of the signal on node Din is not 50% when the mixed-voltage I/O buffer is operated in receive mode. For example, as shown in Fig. 4.10, the signal Din is not a 50%-duty-cycle signal when the 2×VDD input-tolerant mixed-voltage I/O buffer receives the 2×VDD input signal. The pulsewidth control loop circuit can be applied to adjust the duty cycle of signal Din to 50% [89], [90].

4.5. Summary

The NMOS-blocking technique has been proposed to design the mixed-voltage I/O buffer in low-voltage CMOS processes. By using the proposed NMOS-blocking technique, the mixed-voltage I/O buffer realized only with 1×VDD devices can receive 2×VDD, 3×VDD, and even 4×VDD input signals without the gate-oxide reliability issue. The 2×VDD and 3×VDD input tolerant mixed-voltage I/O buffer by using the NMOS-blocking technique have been successfully verified in a 0.25-μm 2.5-V CMOS process to serve 2.5/5-V mixed-voltage interface and in a 0.13-μm 1-V CMOS process with Cu interconnects to serve 1/3-V mixed-voltage interface, respectively. The proposed NMOS-blocking technique can be extended to design the 4×VDD, 5×VDD, and even 6×VDD input tolerant mixed-voltage I/O buffers. The limitation on the proposed NMOS-blocking technique is the pn-junction breakdown voltage of the given CMOS process.

TABLE 4.1

Operation of the Dynamic Gate-Bias Circuit in the Proposed 2×VDD Input Tolerant Mixed-Voltage I/O Buffer

Mode	Transmitted Signal	Received Signal	Gate Voltage of MP0 (PU)	Gate Voltage of MN1 (Node 2)
Receive Mode	X	Low (GND)	VDD	VDD
High-Voltage Receive Mode	X	High (2×VDD)	VDD	VDD
Transmit Mode	Low (GND)	X	VDD	VDD
Transmit Mode	High (VDD)	X	GND	VDDH

TABLE 4.2

Operation of the Dynamic Gate-Bias Circuit in the Proposed 3×VDD Input Tolerant Mixed-Voltage I/O Buffer

Mode	Transmitted Signal	Received Signal	Gate Voltage of MN1 (Node 3)	Gate Voltage of MN2 (Node 4)
Receive Mode	X	Low (GND)	VDD	VDD
High-Voltage Receive Mode	X	High (3×VDD)	VDD	VDDH
Transmit Mode	Low (GND)	X	VDD	VDD
Transmit Mode	High (VDD)	X	VDDH	VDDH

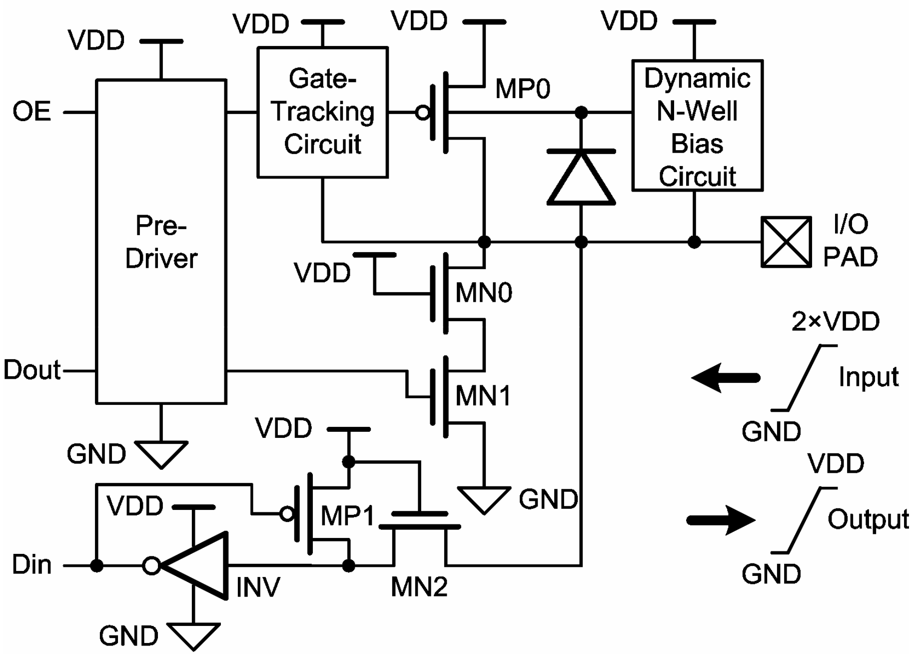


Fig. 4.1. Mixed-voltage I/O buffer realized with only thin-oxide devices in the mixed-voltage interface.

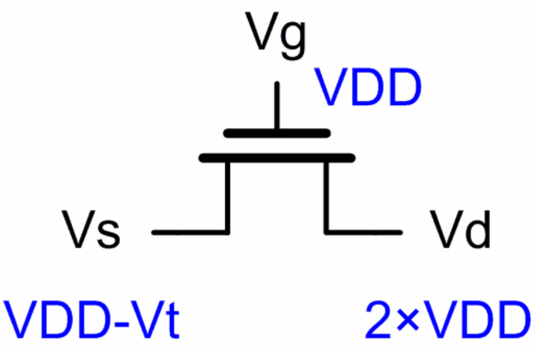


Fig. 4.2. An NMOS transistor, whose gate and drain are biased at VDD and 2×VDD, respectively.

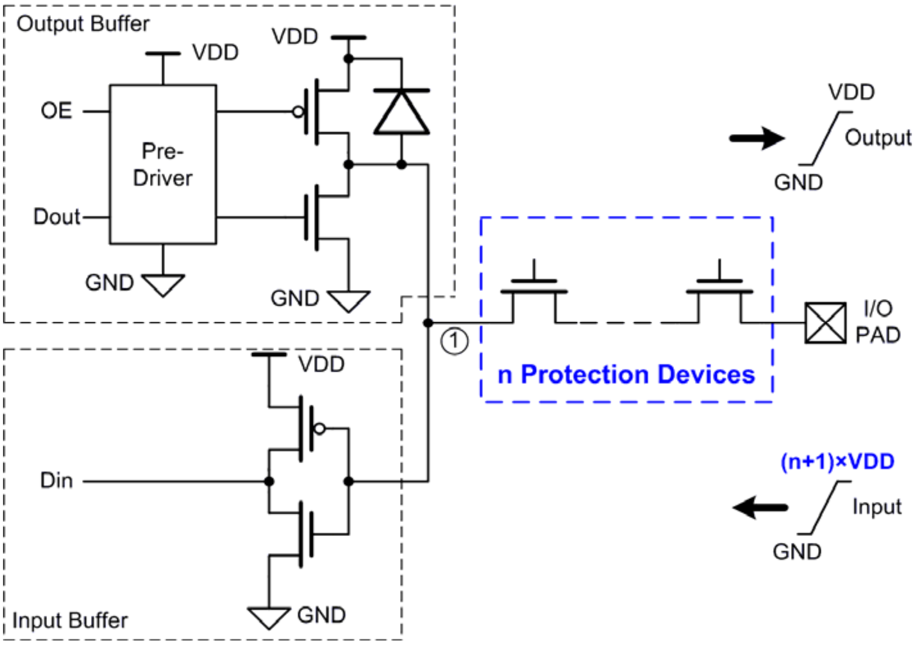


Fig. 4.3. Proposed NMOS-blocking technique for mixed-voltage I/O buffer.

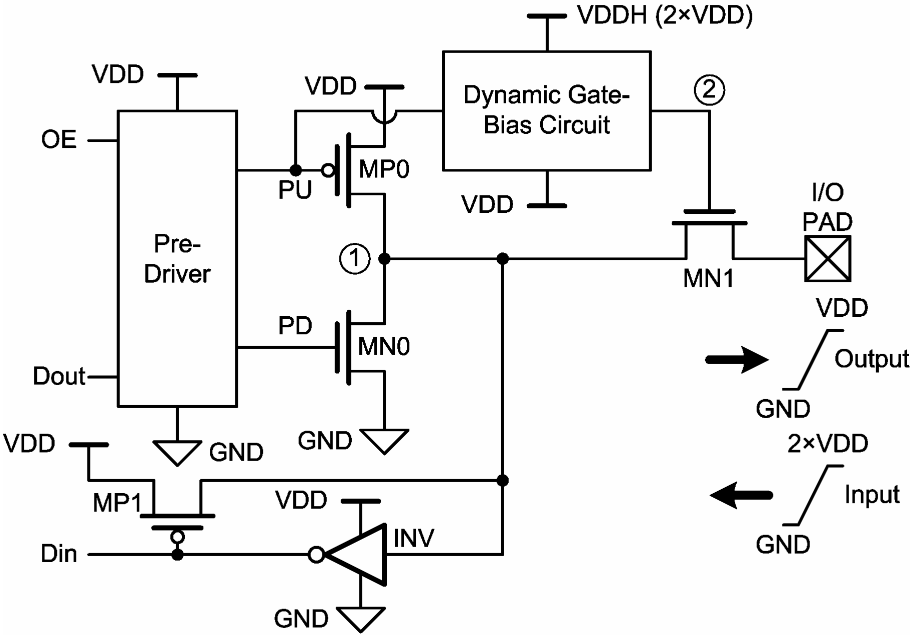


Fig. 4.4. 2×VDD input tolerant mixed-voltage I/O buffer by using the proposed NMOS-blocking technique.

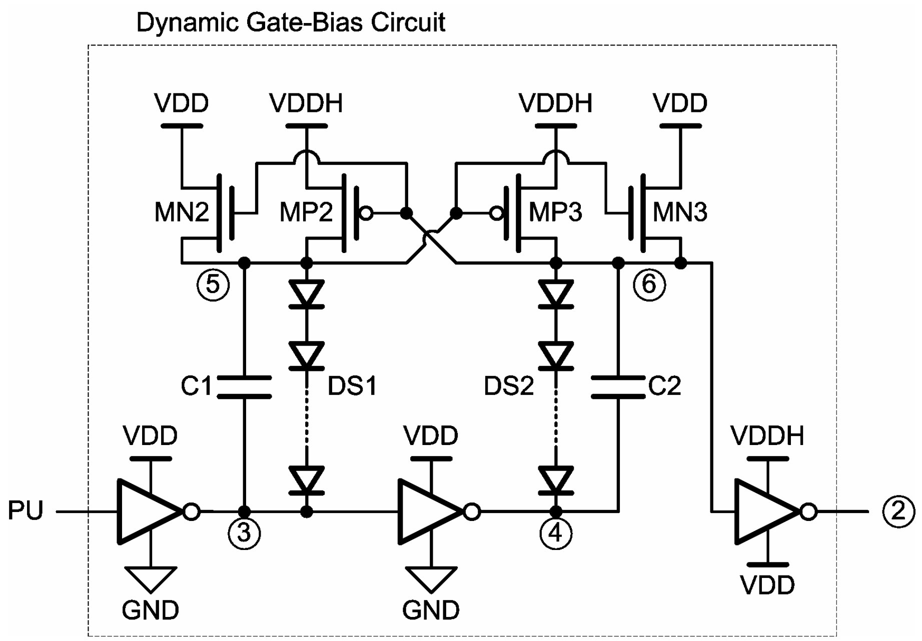


Fig. 4.5. Dynamic gate-bias circuit in the proposed 2×VDD input tolerant mixed-voltage I/O buffer.

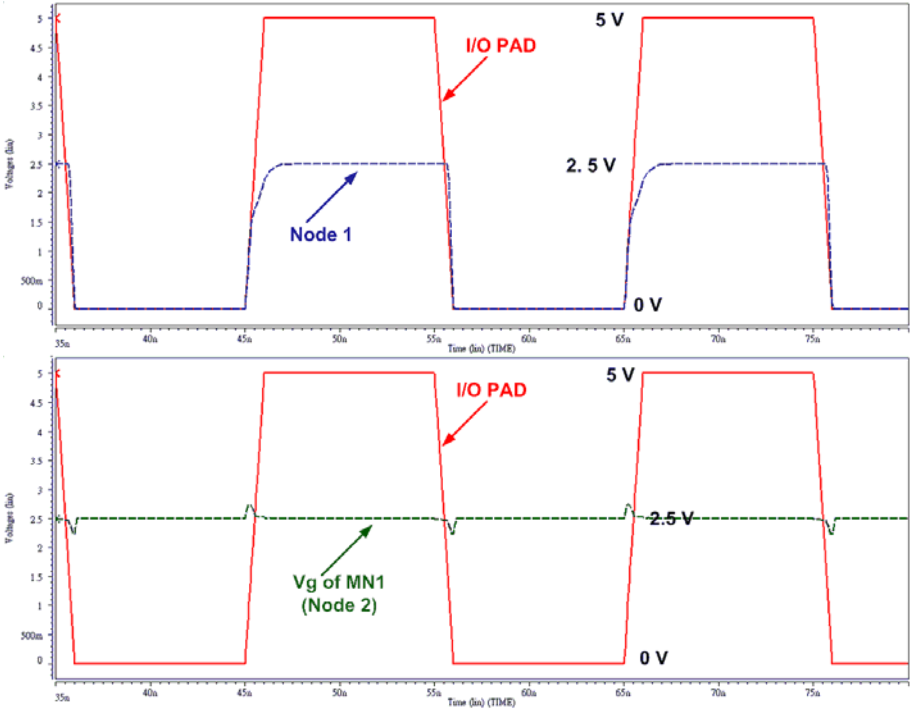


Fig. 4.6. Simulated waveforms of the proposed 2×VDD input tolerant mixed-voltage I/O buffer in the receive mode with 5-V input signals.

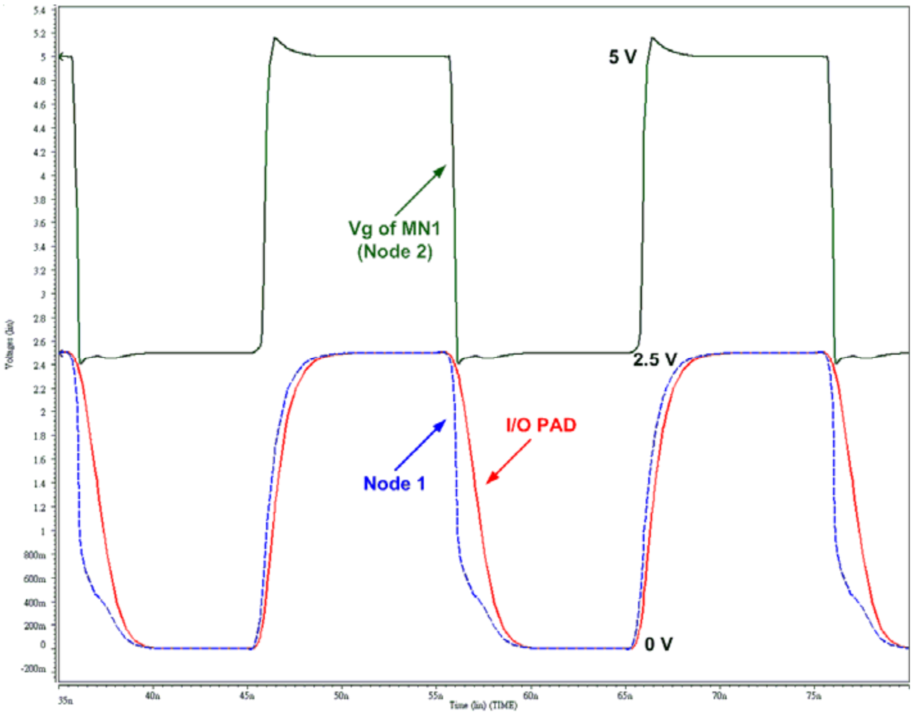


Fig. 4.7. Simulated waveforms of the proposed 2×VDD input tolerant mixed-voltage I/O buffer in the transmit mode.

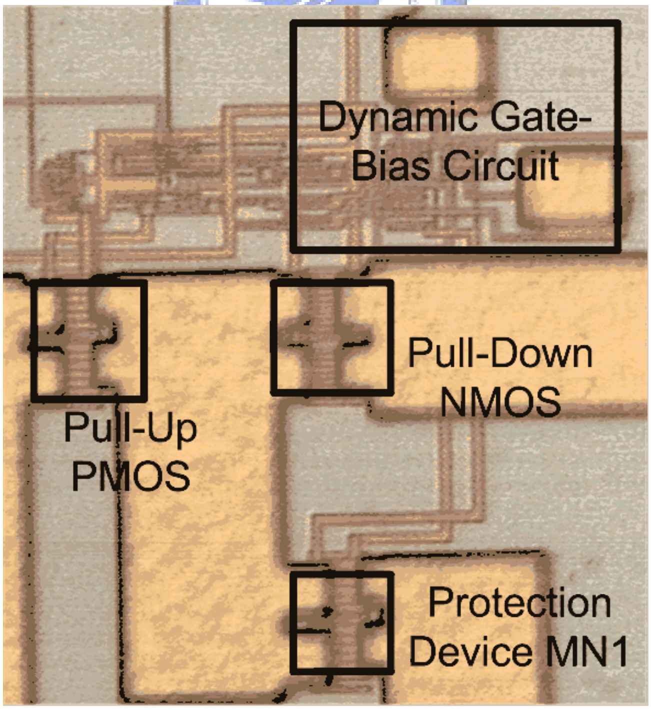


Fig. 4.8. Chip photograph of the proposed 2×VDD input tolerant mixed-voltage I/O buffer in a 0.25-µm 2.5-V CMOS process.

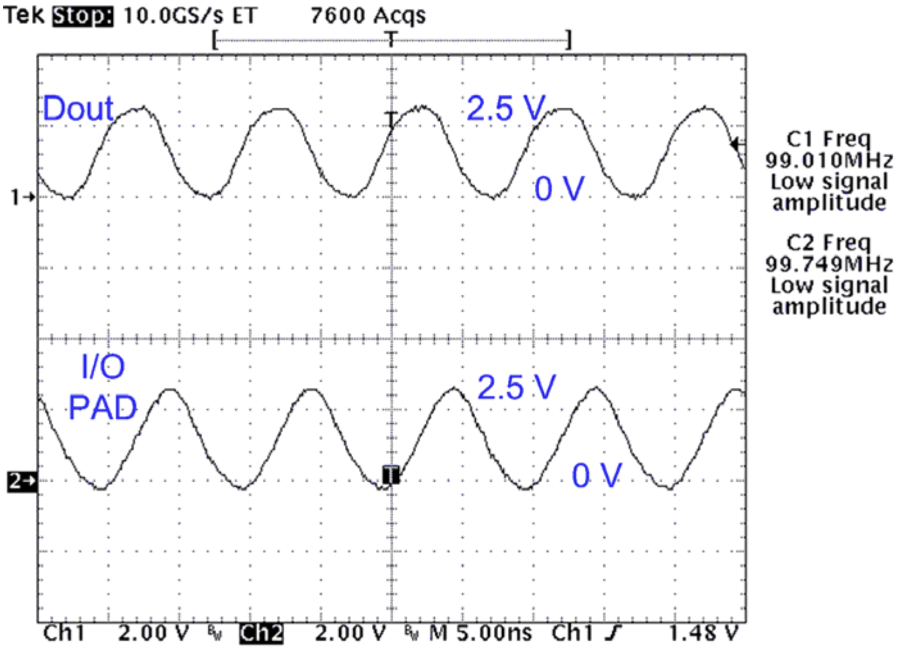


Fig. 4.9. Measured waveforms on the node Din and I/O pad of the proposed 2×VDD input tolerant mixed-voltage I/O buffer in the receive mode with 5-V input signals.

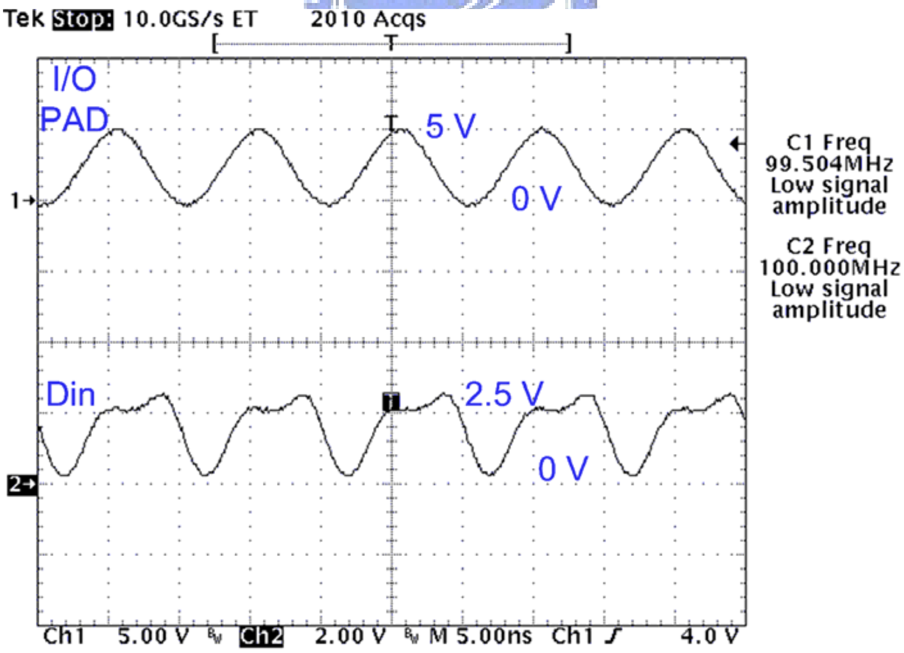


Fig. 4.10. Measured waveforms on the node Dout and I/O pad of the proposed 2×VDD input tolerant mixed-voltage I/O buffer in the transmit mode with 2.5-V output signals.

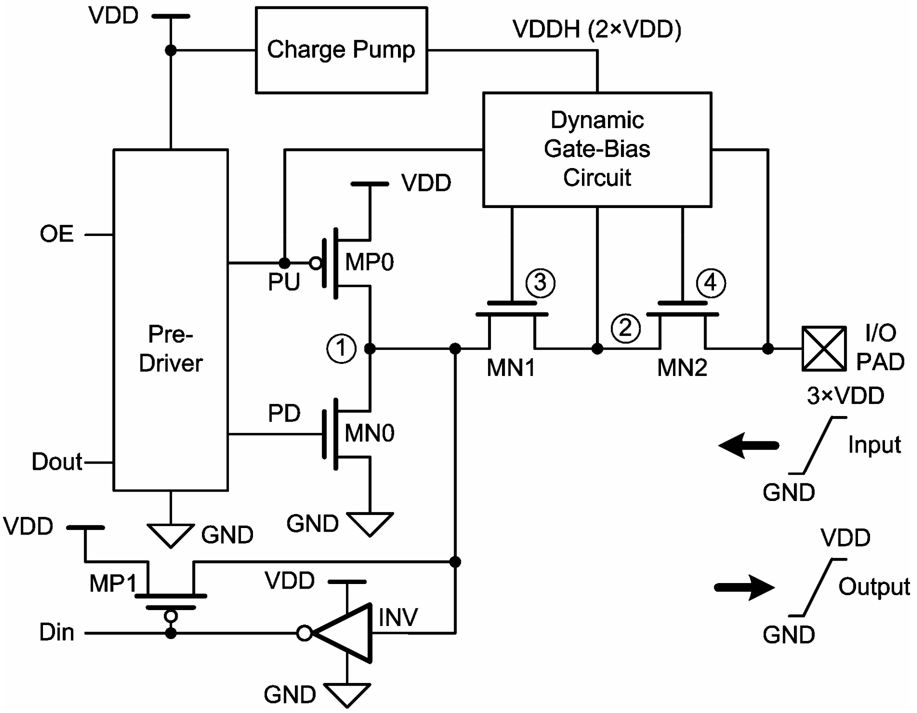


Fig. 4.11. 3×VDD input tolerant mixed-voltage I/O buffer by using the proposed NMOS-blocking technique.

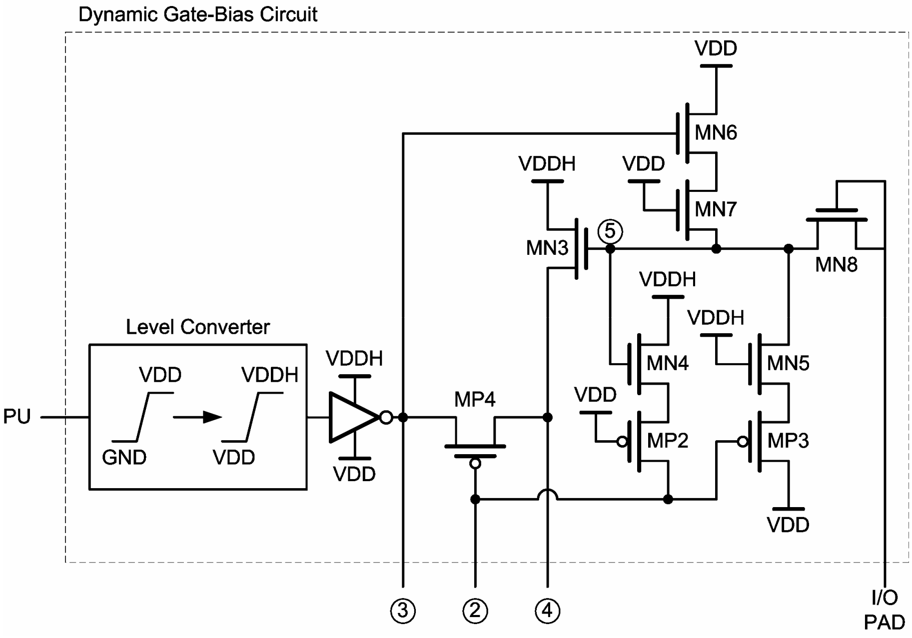


Fig. 4.12. Dynamic gate-bias circuit in the proposed 3×VDD input tolerant mixed-voltage I/O buffer.

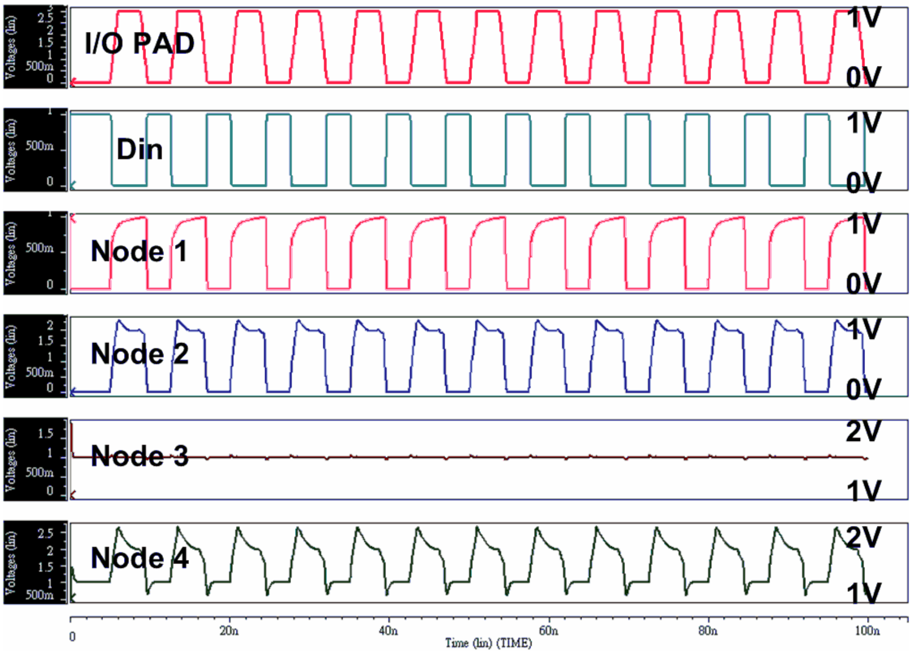


Fig. 4.13. Simulated waveforms of the proposed 3×VDD input tolerant mixed-voltage I/O buffer in the receive mode to receive 133-MHz 3×VDD (3-V) input signals. The waveforms are shown to observe the voltages at the nodes of I/O pad, Din, node 1, node 2, node 3, and node 4 in Fig. 4.11.

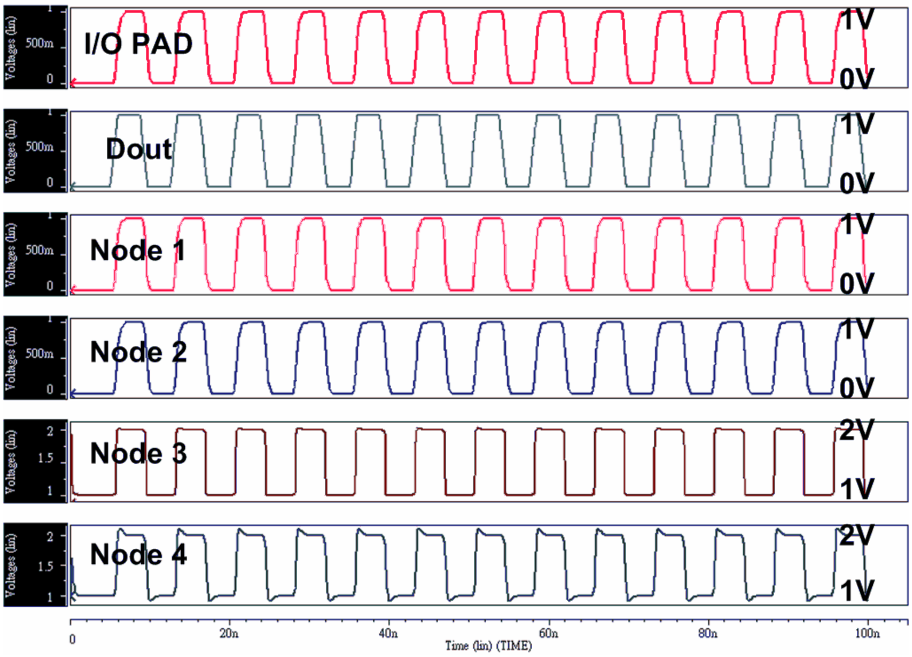


Fig. 4.14. Simulated waveforms of the proposed 3×VDD input tolerant mixed-voltage I/O buffer in the transmit mode to drive 133-MHz 3×VDD (3-V) output signals. The waveforms are shown to observe the voltages at the nodes of I/O pad, Din, node 1, node 2, node 3, and node 4 in Fig. 4.11.

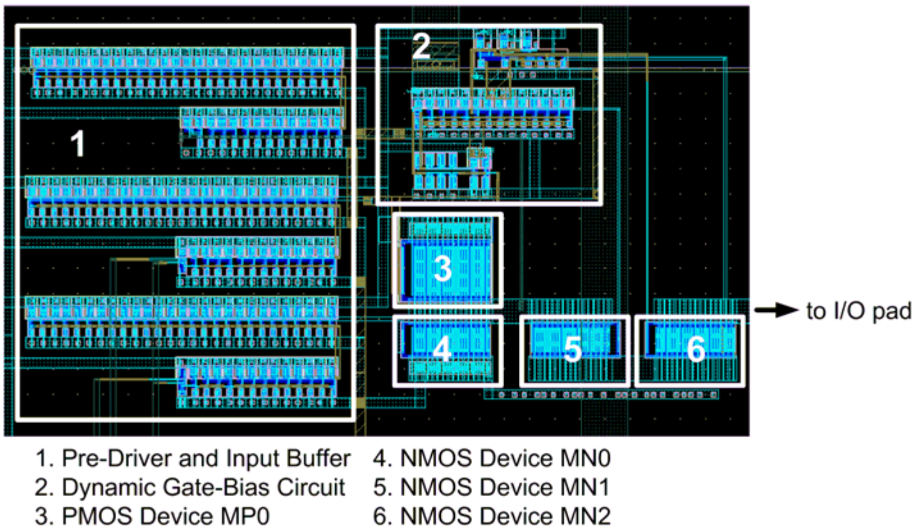


Fig. 4.15. Layout of the proposed 3×VDD input tolerant mixed-voltage I/O buffer in a 0.13-µm 1-V CMOS process with Cu interconnects.

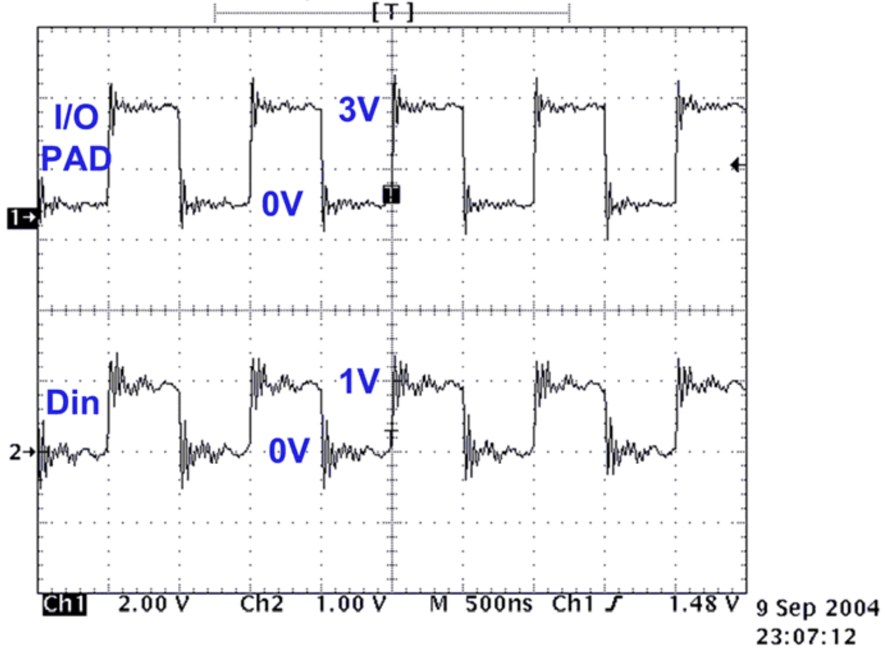


Fig. 4.16. Measured voltage waveforms of the proposed 3×VDD input-tolerant mixed-voltage I/O buffer in the receive mode to successfully receive 3×VDD (3-V) input signals.

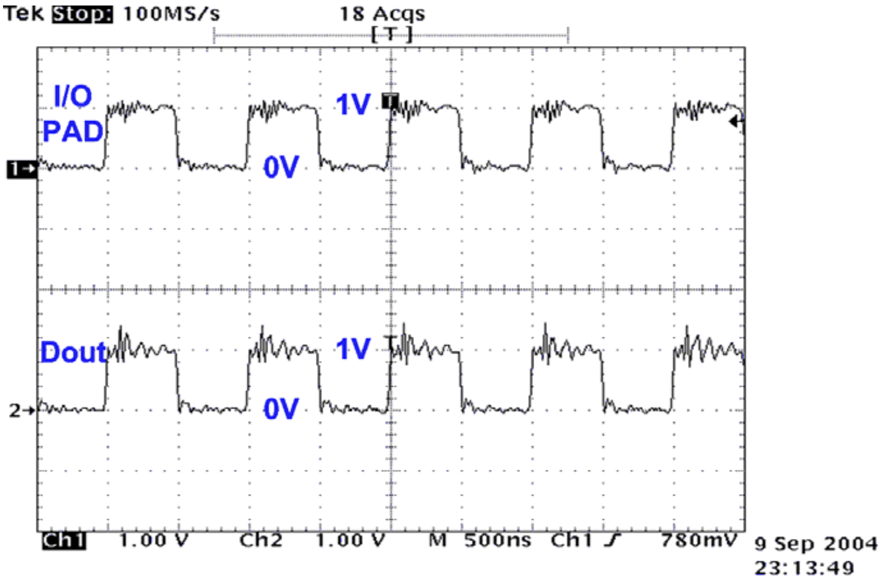


Fig. 4.17. Measured voltage waveforms of the proposed 3×VDD input-tolerant mixed-voltage I/O buffer in the transmit mode to drive 1×VDD (1-V) output signals.

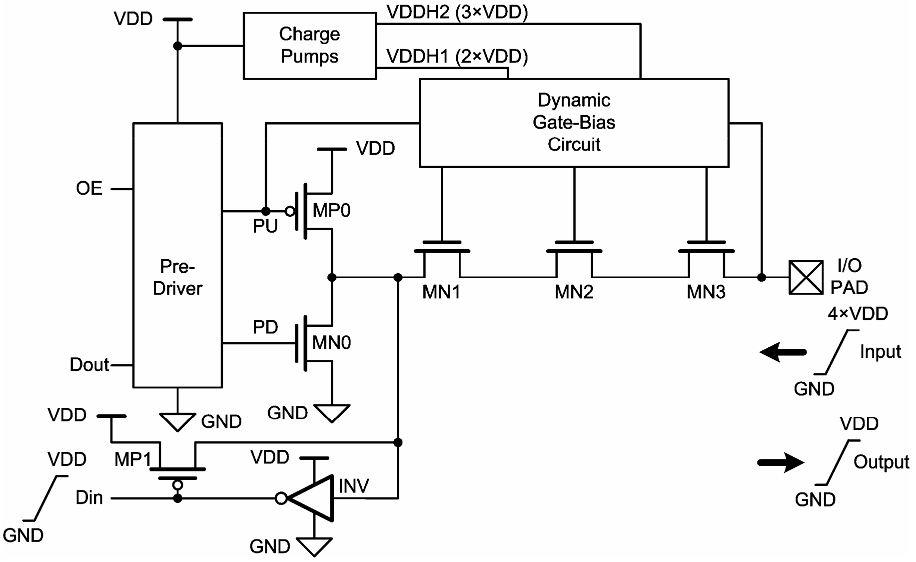


Fig. 4.18. 4×VDD input tolerant mixed-voltage I/O buffer by using the proposed NMOS-blocking technique.

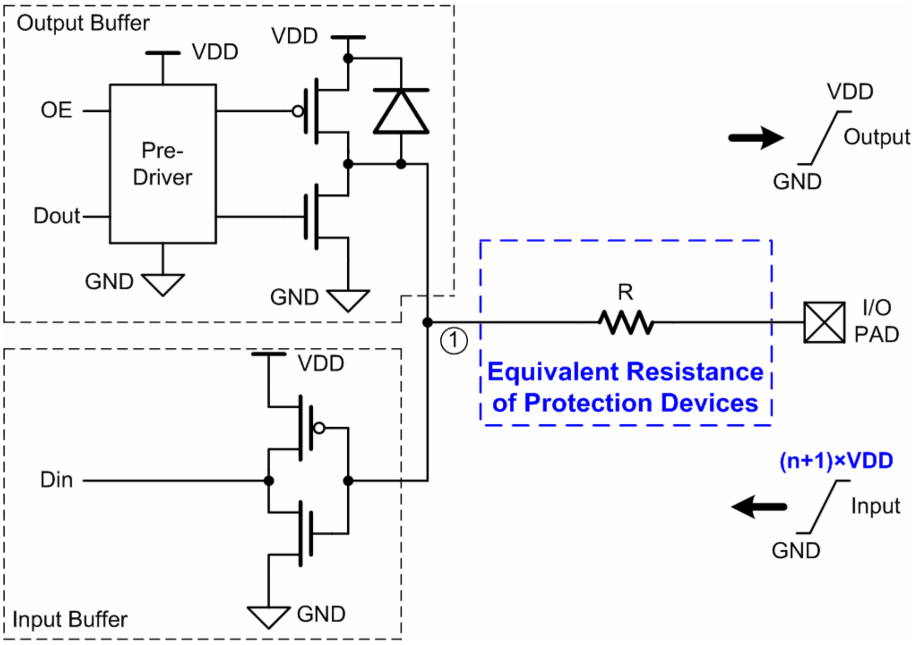


Fig. 4.19. Equivalent circuit of the mixed-voltage I/O buffer designed with the proposed NMOS-blocking technique.

CHAPTER 5

Charge Pump Circuit Without Gate-Oxide Reliability Issue in Low-Voltage Processes

In this chapter, a new charge pump circuit with consideration of gate-oxide reliability is designed with two pumping branches. The charge transfer switches in the new proposed circuit can be completely turned on and turned off, so its pumping efficiency is higher than that of the traditional designs. Moreover, the maximum gate-source and gate-drain voltages of all devices in the proposed charge pump circuit don’t exceed the normal operating power supply voltage (VDD). Two test chips have been implemented in a 0.35-μm 3.3-V CMOS process to verify the new proposed charge pump circuit. The measured output voltage of the new proposed 4-stage charge pump circuit with each pumping capacitor of 2 pF to drive the capacitive output load is around 8.8 V under 3.3-V power supply (VDD=3.3 V), which is limited by the junction breakdown voltage of the parasitic pn-junction in the given process. The new proposed circuit is suitable for applications in low-voltage CMOS processes because of its high pumping efficiency and no overstress across the gate oxide of devices.

5.1. Background

Charge pump circuits have been often used to generate dc voltages those are higher than the normal power supply voltage (VDD) or lower than the ground voltage (GND) of the chip. Charge pump circuits are usually applied to the nonvolatile memories, such as EEPROM or flash memories, to write or to erase the floating-gate devices [58]-[61]. In addition, charge pump circuits had been used in some low-voltage designs to improve the circuit performance [21], [62]. The 4-stage diode charge pump circuit using the pn-junction diodes as the charge transfer devices is shown in Fig. 5.1(a). The charges are pushed from the power supply (VDD) to the output node (Vout), stage by stage. Thus, the output voltage of the charge pump circuit can be pumped high. The voltage fluctuation of each pumping node can be expressed as

$$\Delta V = V_{clk} \cdot \frac{C_{pump}}{C_{pump} + C_{par}} - \frac{I_o}{f \cdot \left(C_{pump} + C_{par}\right)}, \tag{5.1}$$

where V_{clk} is the voltage amplitude of the clock signals, C_{pump} is the pumping capacitance, C_{par} is the parasitic capacitance at each pumping node, I_o is output current, and f is the clock frequency. If C_{par} and I_o are small enough and C_{pump} is large enough, C_{par} and I_o can be ignored from equation 5.1. Because V_{clk} is usually with the same voltage level as the normal power supply voltage (VDD), the voltage fluctuation of each pumping node can be simply expressed as

$$\Delta V \approx V_{clk} = \mathrm{VDD}. \tag{5.2}$$

Hence, the output voltage of the 4-stage charge pump circuit with diodes can be expressed as

$$\mathrm{Vout} = 5 \cdot (\mathrm{VDD} - V_D), \tag{5.3}$$

where V_D is the cut-in voltage of the pn-junction diode. However, it is difficult to implement the fully independent diodes in the common silicon substrate. In other words, the charge pump circuit with diodes shown in Fig. 5.1(a) can not be easily integrated into the standard CMOS process. Therefore, most charge pump circuits are based on the circuit proposed by Dickson [63]-[65]. Fig. 5.1(b) shows the 4-stage Dickson charge pump circuit, where the diode-connected MOSFETs are used to transfer the charges from the present stage to the next stage. Thus, it can be easily integrated into standard CMOS processes. However, the voltage difference between the drain terminal and the source terminal of the diode-connected MOSFET is the threshold voltage when the diode-connected MOSFET is turned on. Therefore, the output voltage of the 4-stage Dickson charge pump circuit has been derived as

$$\mathrm{Vout} = \sum_{i=1}^{5} (\mathrm{VDD} - V_{t(Mi)}), \tag{5.4}$$

where $V_{t(Mi)}$ denotes the threshold voltage of the diode-connected MOSFET *Mi*. Traditionally, the bulk terminals of the diode-connected MOSFETs in the Dickson charge pump circuit are connected to ground (GND). The threshold voltage ($V_{t(Mi)}$) of the diode-connected MOSFET becomes larger due to the body effect when the voltage on each pumping node is pumped higher. Therefore, the pumping efficiency of the Dickson charge pump circuit is degraded by the body effect when the number of pumping stages is increased.

Several modified charge pump circuits based on the Dickson charge pump circuit were reported to enhance the pumping efficiency [66]-[74]. In the triple-well process, the floating-well technique [66] or the source-bulk connected devices were used to eliminate the body effect issue on the diode-connected MOSFETs in the Dickson charge pump circuit. But, the floating-well technique may generate substrate current in the floating-well devices to influence other circuits in the same chip. The source-bulk connected technique increases the parasitic capacitance at each pumping node due to the large bulk-to-well pn-junction capacitance, so the pumping capacitors have to be enlarged. The auxiliary MOSFETs used to dynamically control the body terminals of the diode-connected MOSFETs [67] may also generate the substrate current in the floating-well devices. Four-phase clock generator was applied in the charge pump circuits to improve pumping efficiency [68]-[71], but the complex clock generator would consume more power. In [72], [73], an extra small charge pump circuit, which has more pumping stages than the main charge pump circuit, was used to control the main charge pump circuit, so the pumping efficiency of the main charge pump circuit can be enhanced. However, the charge pump circuits [72], [73] occupy larger silicon area than others because of the extra charge pump circuits. In addition, the extra small charge pump circuit consumes extra power. In [74], the charge sharing concept was used in the charge pump circuit to reduce the power consumption. However, the charge sharing concept requires the special clock generator. The 4-stage charge pump circuit reported by Wu and Chang [75] is shown in Fig. 5.2(a). The charge transfer switch (CTS) controlled by the dynamic control circuit in the Wu and Chang's charge pump circuit is used to transfer the charges from the present stage to the next stage without suffering the limitation of threshold voltage. Fig. 5.2(b) shows the corresponding voltage waveforms of the 4-stage Wu and Chang's charge pump circuit. When the clock signal CLK is low and the clock signal CLKB is high during the time interval T1 in Fig. 5.2(b), the voltage on node 1 is VDD and the voltage on node 2 is 3×VDD. Because transistor MN1 is turned off and transistor MP1 is turned on, the charge transfer switch, MS1, can be completely turned on to transfer charges from the power supply (VDD) to node 1. During the time interval T2, the voltage on node 2 can be pumped as high as 2×VDD to turn on transistor MN1 and to turn off transistor MP1. Thus, the charge transfer switch, MS1, can be completely turned off to prevent the charges back to the power supply (VDD). The operation of next stages in Wu and Chang's charge pump circuit is similar to that of the first stage. Because the CTS's can be completely turned on or turned off by the dynamic control circuits, the pumping efficiency has been enhanced with ideal output voltage of 5×VDD. However, the output stage (MDO) of Wu and Chang's charge pump circuit is still a diode-connected MOSFET, so it also suffers the body effect issue. Besides, because the maximum voltage difference of each stage is 2×VDD, all devices of Wu and Chang's charge pump circuit suffer the high-voltage overstress on their gate oxides.

With the advanced CMOS processes, the thickness of the gate oxide becomes thinner so the operation voltage of transistor must be lowered due to the reliability issue [1]. Thus, the gate-oxide reliability issue [76] must be also considered into the design of charge pump circuits, especially in the low-voltage CMOS processes. In this chapter, a new charge pump circuit that has better pumping efficiency but without the gate-oxide reliability issue in low-voltage processes is presented [77]. The new proposed charge pump circuit has been successfully verified in a 0.35-μm 3.3-V CMOS process.

5.2. New Charge Pump Circuit Without Gate-Oxide Reliability Issue

The circuit and the corresponding voltage waveforms of the new proposed charge pump circuit with 4 stages are shown in Figs. 3(a) and 3(b), respectively. To avoid the body effect, the bulks of the devices in the proposed charge pump circuit are recommended to be connected to their sources respectively if the given process provides the deep n-well layer. Clock signals CLK and CLKB are out-of-phase but with the amplitudes of VDD. As shown in Fig. 5.3(a), there are two charge transfer branches, branch A and branch B, in the new proposed charge pump circuit. Branch A is comprised of transistors MN1, MN2, MN3, MN4, MP1, MP2, MP3, and MP4 with the capacitors C1, C2, C3, and C4. Branch B is comprised of transistors MN5, MN6, MN7, MN8, MP5, MP6, MP7, and MP8 with the capacitors C5, C6, C7, and C8. The control signals of branches A and B are intertwined. Besides, clock signals of branches A and B are out-of-phase. When the clock signals of the first and the third pumping stages in the branch A are CLK, those in the branch B are CLKB. Similarly, when the clock signals of the second and the forth pumping stages in the branch A are CLKB, those in the branch B are CLK. Thus, branches A and B can see as two independent charge pump circuits but their output nodes are connected together. Because the clock signals of the branch A and those of the branch B are out-of-phase, the voltage waveforms of nodes 1-4 and those of nodes 5-8 are also out-of-phase. Hence, branches A and B can pump the output voltage to high, alternately. The detailed operations of the new proposed charge pump circuit are described below.

As illustrated in Fig. 5.3(b), the clock signal CLK is low and the clock signal CLKB is high during the time interval T1. At this moment, the voltage difference (V_{15}) between node 1 and node 5 is –VDD. Therefore, transistor MN1 is turned on to transfer the charges from the power supply (VDD) to node 1, but the transistor MN5 is turned off to cut off the path from node 5 back to the power supply. Similarly, V_{15} becomes VDD during the time interval T2. Transistor MN1 is turned off to cut off the leakage path from node 1 back to the power supply, but the transistor MN5 is turned on to transfer the charges from the power supply to node 5.

In the second stage, when the clock signal CLK is low and the clock signal CLKB is high during the time interval T1, V_{15} and the voltage difference (V_{26}) between node 2 and node 6 are –VDD and VDD, respectively. Therefore, transistors MP5 and MN6 are turned on to transfer the charges from node 5 to node 6, but transistors MP1 and MN2 are turned off to cut off the path from node 2 back to node 1. Similarly, V_{15} and V_{26} are VDD and –VDD during the time interval T2, respectively. Transistors MP5 and MN6 are turned off in order to cut off the path from node 6 back to node 5, but transistors MP1 and MN2 are turned on to transfer the charges from node 1 to node 2. The operation of the third pumping stage is similar to that of the second pumping stage.

As shown in Fig. 5.3(a), the output nodes of braches A and B are connected together. When the clock signal CLK is low and the clock signal CLKB is high during the time interval T1, the voltage difference (V_{48}) between node 4 and node 8 is VDD. Therefore, transistor MP4 is turned on to transfer the charges from node 4 to the output node, but transistor MP8 is turned off to cut off the path from the output node back to node 8. On the other hand, V_{48} is –VDD during the time interval T2. Hence, the transistor MP4 is turned off and the current path from the output node back to node 4 is cut off. In addition, the transistor MP8 is turned on to transfer the charges from node 8 to the output node.

As shown in Fig. 5.3 (b), the gate-source voltages (Vgs) and gate-drain voltages (Vgd) of all MOSFETs in the new proposed charge pump circuit do not exceed VDD. Thus, there is no high-voltage overstress on the gate oxide of the devices in the new proposed charge pump circuit.

5.3. Verifications and Discussions

5.3.1. Simulation Results and Comparisons

A 0.18-μm 1.8-V CMOS device model is used to verify the design of the new proposed charge pump circuit in HSPICE simulation. Fig. 5.4 shows the simulated voltage waveforms of the new proposed 4-stage charge pump circuit with each pumping capacitor of 1 pF and

5-μA output current. The expected waveforms shown in Fig. 5.3(b) are similar to the simulated waveforms shown in Fig. 5.4. Ideally, the output voltage of the new proposed 4-stage charge pump circuit with 1.8-V power supply voltage (VDD=1.8 V) should be as high as 9 V (1.8×5=9). However, due to the parasitic capacitance at each pumping node and the loading of the output current, the simulated output voltage of the new proposed charge pump circuit is around 8.39 V.

Fig. 5.5 shows the simulated output voltages of the proposed charge pump circuit under different output currents and power supply voltages (VDD). When the output current is increased, the output voltages of the proposed charge pump circuit under different power supply voltages (VDD) are decreased. If the new proposed charge pump circuit only drives the capacitive load, the output voltages of the proposed charge pump circuit under different power supply voltages (VDD) are close to 5×VDD. If the supply voltage is too low and the output current is too high, the proposed charge pump circuit can not pump the output voltage high.

The simulated output voltages of the Dickson charge pump circuit [63], Wu and Chang's charge pump circuit [75], and the new proposed charge pump circuit with different output currents are compared in Fig. 5.6. Actually, the pumping capacitors of a charge pump circuit take a great part in silicon area. For fair comparison, the total pumping capacitors of these charge pump circuits must be equaled. Therefore, the pumping capacitors in the proposed charge pump circuit, in Wu and Chang's charge pump circuit, and in the Dickson charge pump circuit are set to 1 pF, 1.6 pF (1×8/5=1.6), and 2 pF (1×8/4=2), respectively. As shown in Fig. 5.6, the output voltages of the proposed charge pump circuit with different output currents are much higher than those of other charge pump circuits. Especially, with the higher output current of 30 μA, the proposed charge pump circuit still has the better pumping performance than others. Since the proposed charge pump circuit has two pumping branches pushing the charges to the output node alternately, the degradation of the output voltage is smaller while the output current increases. Besides, the MOSFET switches in the new proposed charge pump circuit are fully turned on to transfer the charges, but all MOSFET switches in the Dickson charge pump circuit and the output stage of Wu and Chang's charge pump circuit are diode-connected transistors, which have the threshold voltage drop problem. Therefore, the proposed charge pump circuit has better pumping performance than others, as shown in Fig. 5.6.

Fig. 5.7 compares the simulated output voltages of the Dickson, Wu and Chang's, and the new proposed charge pump circuits under different power supply voltages (VDD) without output current loading. As shown in Fig. 5.7, the output voltages of these three charge pump circuits are degraded when the power supply voltage is decreased. However, the new proposed charge pump circuit still has higher output voltages under the lower power supply voltage because the proposed charge pump circuit has better pumping efficiency. Thus, the proposed charge pump circuit is more suitable in low-voltage processes than the prior designs.

Branches A and B in the new proposed charge pump circuit can pump the output voltage alternately, but Wu and Chang's charge pump circuit and the Dickson charge pump circuit only pump the charges to the output node per clock cycle. The simulated output waveforms of these charge pump circuits with 20-μA output current are shown in Fig. 5.8, where ΔV is the amplitude of the output voltage ripple. As shown in Fig. 5.8, the output voltage ripple of the proposed charge pump circuit (0.166%) is much smaller than those of Wu and Chang's charge pump circuit (0.457%) and the Dickson charge pump circuit (0.762%). Therefore, the output voltage of the new proposed charge pump circuit is more stable than those of the other charge pump circuits. If the output voltage ripple is still large, a low-pass filter should be connected to the output node of the charge pump circuit to filter the voltage ripple [78] or a feedback loop can be applied in the charge pump circuit to stabilize the output voltage [91], [92].

5.3.2. Silicon Verifications

In this work, two test chips have been fabricated in a 0.35-μm 3.3-V CMOS process to verify the proposed charge pump circuit. Fig. 5.9 shows the simulated output voltages of proposed charge pump with each pumping capacitor of 2 pF, the Dickson charge pump circuit with each pumping capacitor of 4 pF, and Wu and Chang's charge pump circuit with each pumping capacitor of 3.2 pF in the 0.35-μm 3.3-V CMOS process. As shown in Fig. 5.9, the proposed charge pump circuit has better pumping performance. The photographs of these two test chips are shown in Figs. 10(a) and 10(b), respectively. These two test chips include the proposed 4-stage charge pump circuit with each pumping capacitors of 2 pF, the proposed 2-stage charge pump circuit with each pumping capacitor of 2 pF, Wu and Chang's 4-stage charge pump circuit with each pumping capacitor of 2 pF, Wu and Chang's 4-stage charge pump circuit with each pumping capacitor of 3.2 pF, the Dickson 4-stage charge pump circuit with each pumping capacitor of 2 pF, the Dickson 4-stage charge pump circuit with each pumping capacitor of 4 pF, the proposed 4-stage charge pump circuit with each pumping capacitor of 4 pF, and the proposed 3-stage charge pump circuit with each pumping capacitor of 2 pF. To drive capacitive load, the measured output voltage of the new proposed 4-stage charge pump circuit with each pumping capacitor of 2 pF is around 8.8 V under 3.3-V power supply voltage (VDD=3.3 V). Fig. 5.11 shows the measured output voltages of the 4-stage charge pump circuits with different output currents. The measured results in Fig. 5.11 is little lower than the simulated results in Fig. 5.9 because of the parasitic resistance and capacitance from the test chips, the bonding wires, and the packages. The parasitic resistance and capacitance may results in the overlapping clock signals, which will lower the pumping efficiency. However, similar to the simulation results, the proposed charge pump circuit has better pumping performance than others, as shown in Fig. 5.11. Besides, the output voltage (~9 V) of the proposed charge pump circuit is limited by the breakdown voltage of the parasitic drain-to-bulk pn-junction diode under the low output current. If the output voltage of the charge pump circuit is larger than the breakdown voltage of the pn-junction diode, the charges leak through this diode and the output voltage of the charge pump circuit is kept at the breakdown voltage. Fig. 5.12 compares the measured output voltages of the proposed 2-stage, 3-stage, and 4-stage charge pump circuits with each pumping capacitor of 2 pF under 2-V power supply (VDD=2 V), respectively. Similarly, the measured output voltage of the proposed 4-stage charge pump circuit in Fig. 5.12 is also limited by the breakdown voltage of the parasitic pn-junction diode at low output current.

5.3.3. Discussions

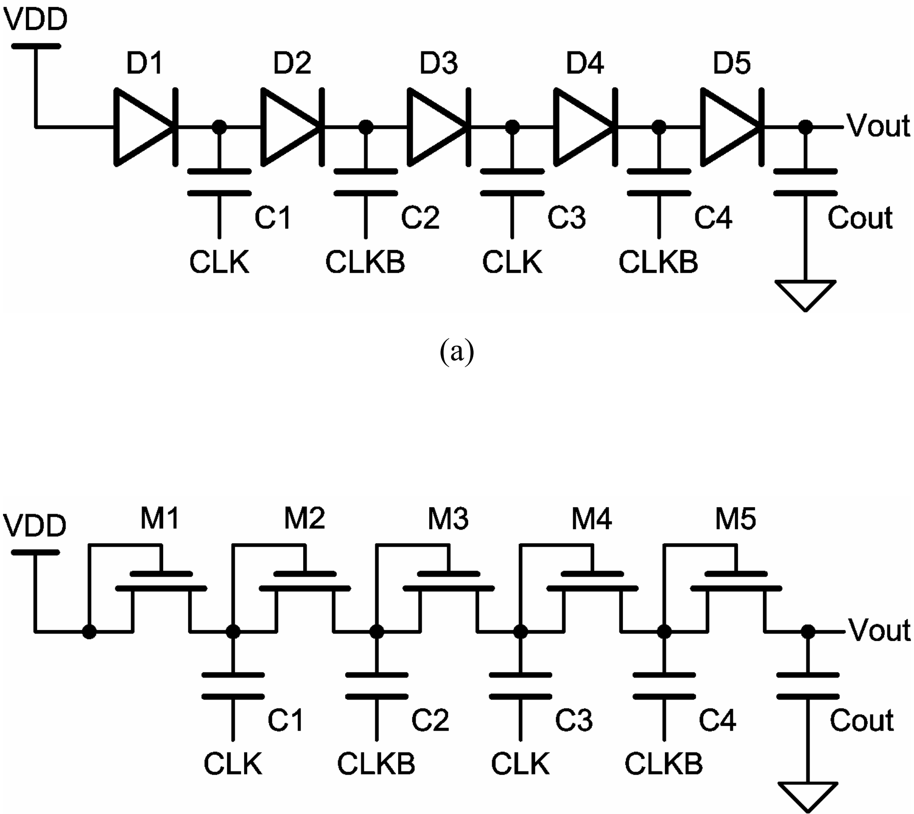
Gate-oxide reliability is a time-dependent issue [8], [57]. The time period during the voltage overstress on the gate oxide is accumulated to induce the oxide breakdown. Hence, the DC stress is more harmful to the gate oxide than the short AC stress (transient stress). The diode-connected MOSFET in the Dickson charge pump circuit is used to transfer charges from the present stage to the next stage. When the diode-connected MOSFET is turned off to prevent the charges flowing back to the previous stage, the voltage across the gate oxide of the diode-connected MOSFET is around 2×VDD–Vt, where Vt is the threshold voltage of the diode-connected MOSFET. The diode-connected MOSFET will suffer serious gate-oxide overstress, so the gate oxide of the diode-connected MOSFET may be damaged after operation. In Wu and Chang’s charge pump circuit, not only these diode-connected

MOSFETs but also the charge transfer switches (CTSs) and their control circuits will suffer serious high-voltage overstress on the gate oxide. In the proposed charge pump circuit, the gate-oxide reliability issue has been considered. The gate-source voltages (Vgs) and gate-drain voltages (Vgd) of devices in the proposed charge pump circuit don't exceed VDD whenever it is in the normal operation, start-up, or turn-off states. Therefore, the proposed charge pump circuit is better for applications in low-voltage CMOS processes.

As shown in Figs. 5.11 and 5.12, the output voltage of the proposed charge pump circuit will be limited by the breakdown voltages of the parasitic pn-junctions. As the CMOS process is scaled down, the breakdown voltages of the parasitic pn-junctions become lower. Thus, the output voltage limitation of the charge pump circuit will become more serious. In [79], the charge pump circuit is designed in the SOI (silicon-on-insulator) process without the limitation of the breakdown voltages of the pn-junctions. However, the SOI process is more expensive than the bulk CMOS process. The charge pump circuit consisting of the polysilicon diodes, which is fully compatible to the standard bulk CMOS process, may be a good candidate to implement the charge pump circuit without the limitation of the breakdown voltages of the parasitic pn-junctions in the future [80]. The charge pump circuit designed with the polysilicon diodes will be presented in Chapter 6.

5.4. Summary

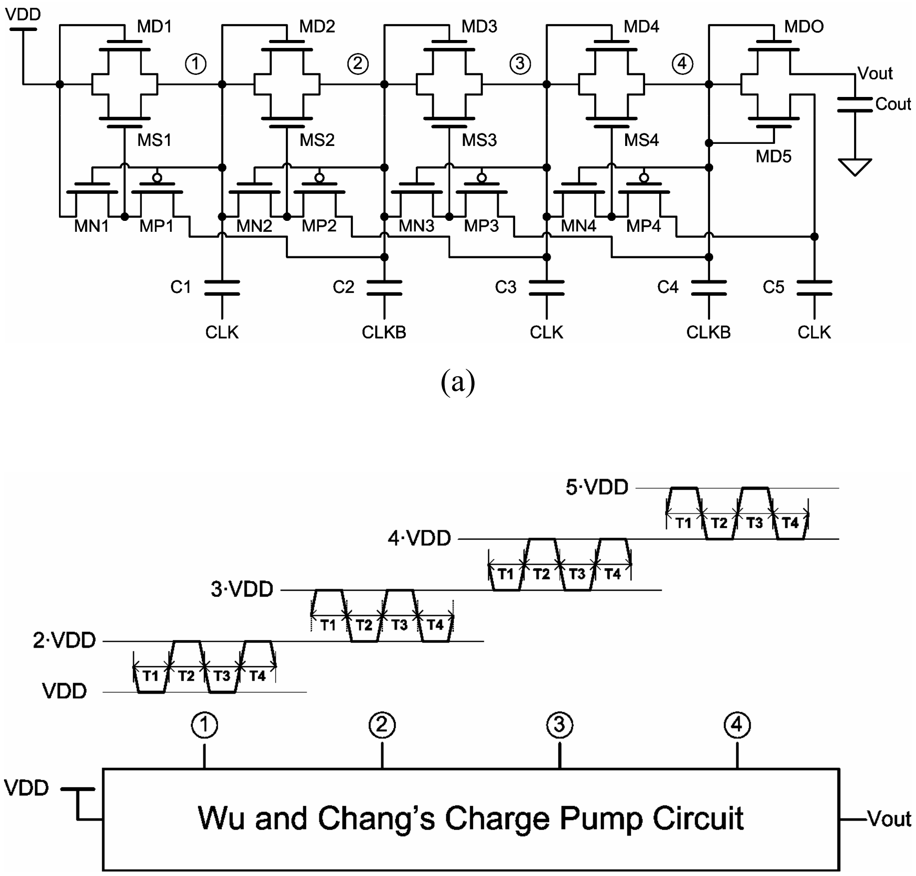
A new charge pump circuit realized with only low-voltage devices without suffering the gate-oxide reliability issue has been presented. Because the charge transfer switches of the new proposed charge pump circuit can be fully turned on and turned off, as well as the output stage doesn't have the threshold drop problem, its pumping efficiency is higher than that of the prior designs. The gate-drain and the gate-source voltages of all devices in the proposed charge pump circuit don't exceed VDD, so the proposed charge pump circuit doesn't suffer the gate-oxide reliability problem. Two test chips have been implemented in a 0.35-µm 3.3-V CMOS process. The experimental results have shown that the new proposed 4-stage charge pump circuit with each pumping capacitor of 2 pF to drive the capacitive load is around 8.8 V under 3.3-V power supply (VDD=3.3 V). With the higher pumping gain and no overstress across the gate oxide, the new proposed charge pump circuit is more suitable for applications in low-voltage CMOS integrated circuits to generate the specified high voltage.



(a)

(b)

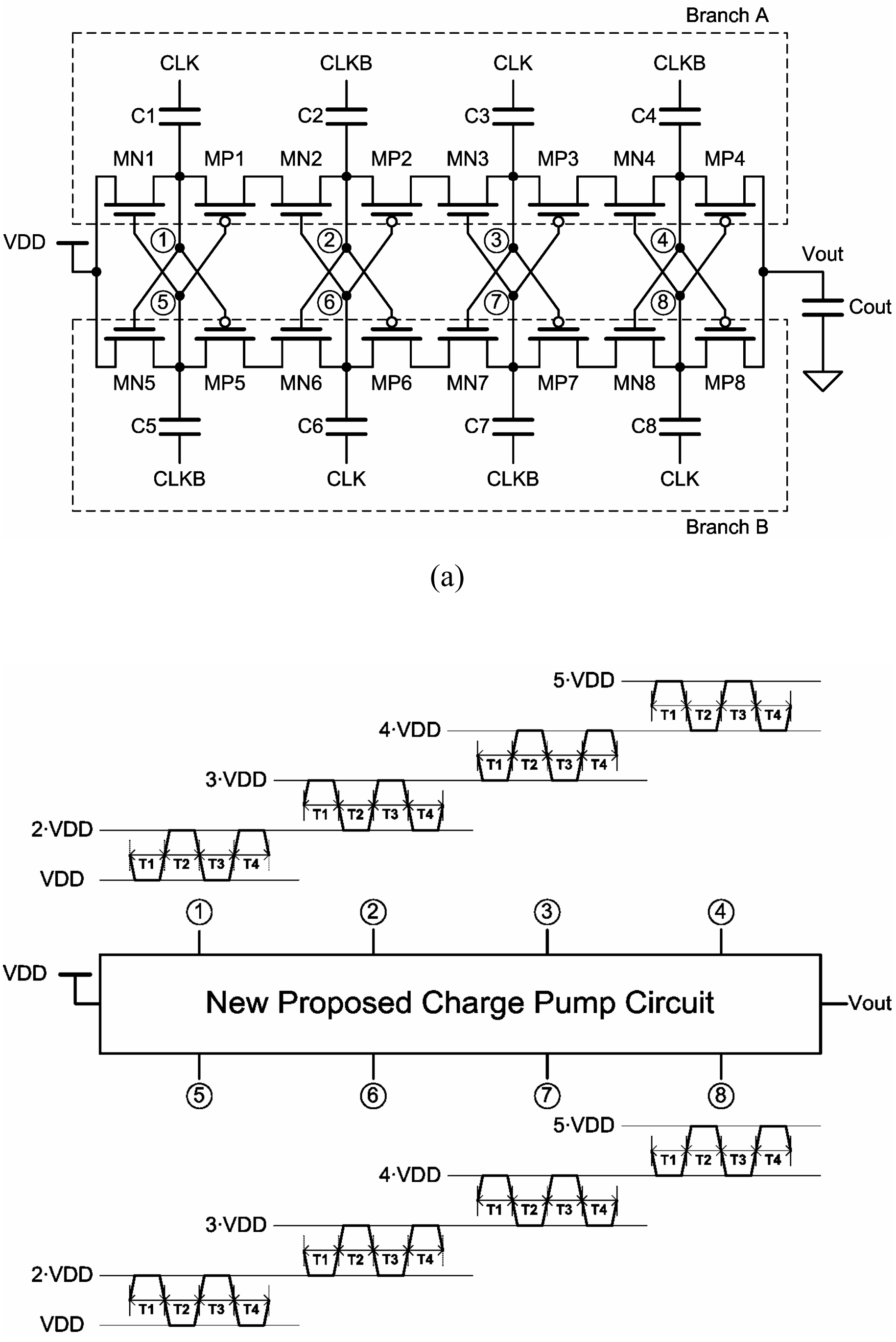
Fig. 5.1. 4-stage (a) diode, and (b) Dickson, charge pump circuits.



(a)

(b)

Fig. 5.2. (a) Circuit, and (b) Corresponding voltage waveforms, of the 4-stage Wu and Chang's charge pump circuit.



(a)

(b)

Fig. 5.3. (a) Circuit, and (b) Corresponding waveforms, of the new proposed charge pump circuit with 4 pumping stages.

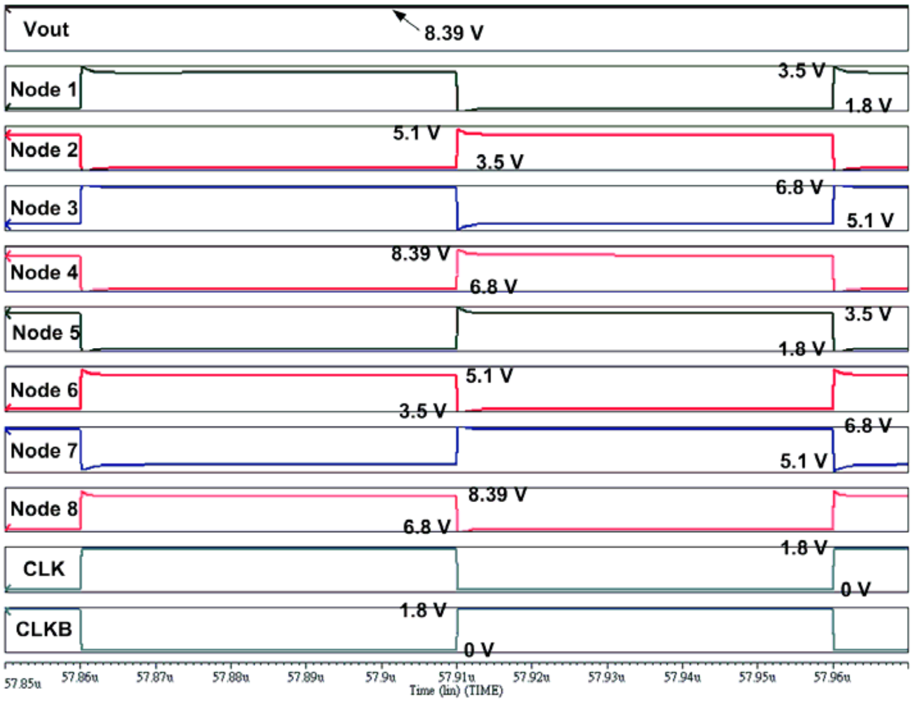


Fig. 5.4. Simulated waveforms on CLK, CLKB, nodes 1-8, and Vout in the new proposed 4-stage charge pump circuit.

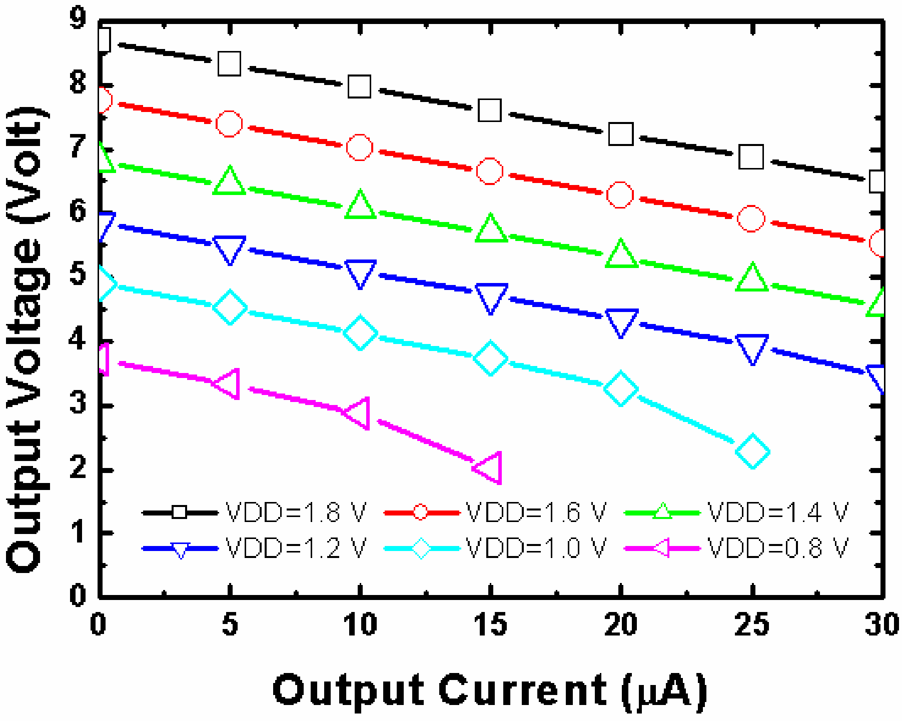


Fig. 5.5. Simulated output voltages of the new proposed 4-stage charge pump circuit under different output currents and power supply voltages (VDD).

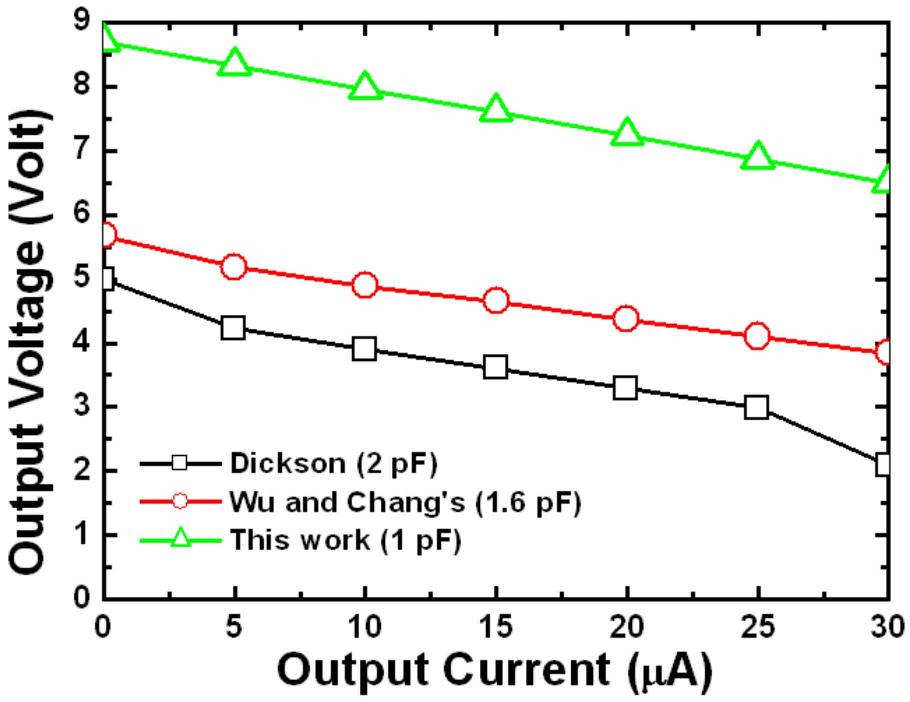


Fig. 5.6. Simulated output voltages of the Dickson, Wu and Chang's, and the proposed charge pump circuits with 4 stages under different output currents with 1.8-V power supply (VDD=1.8 V).

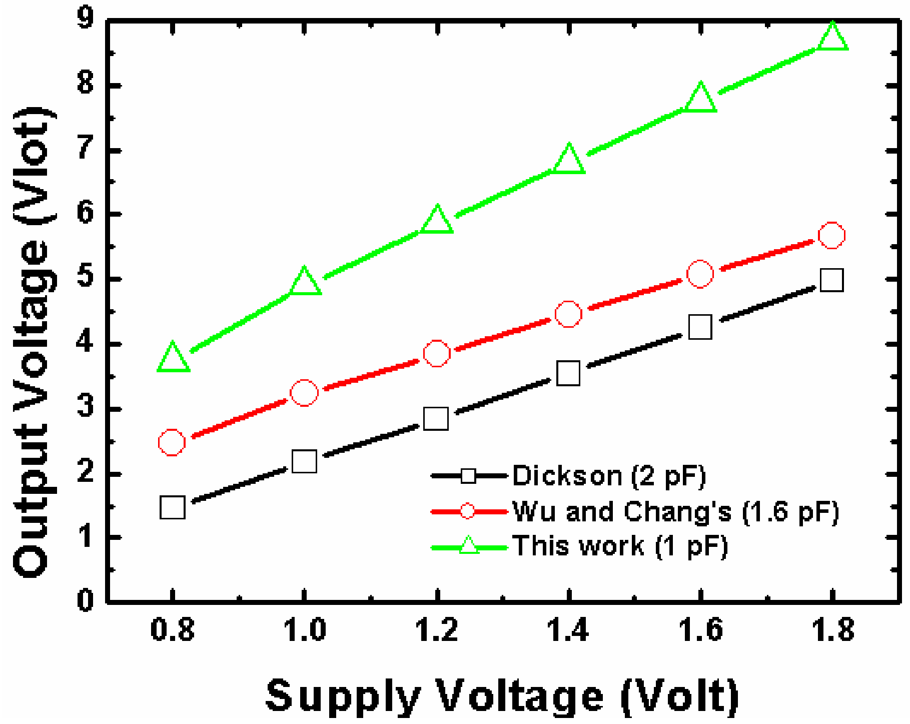


Fig. 5.7. Simulated output voltages of the Dickson, Wu and Chang's, and the proposed charge pump circuits with 4 stages under different VDD without output current loading.

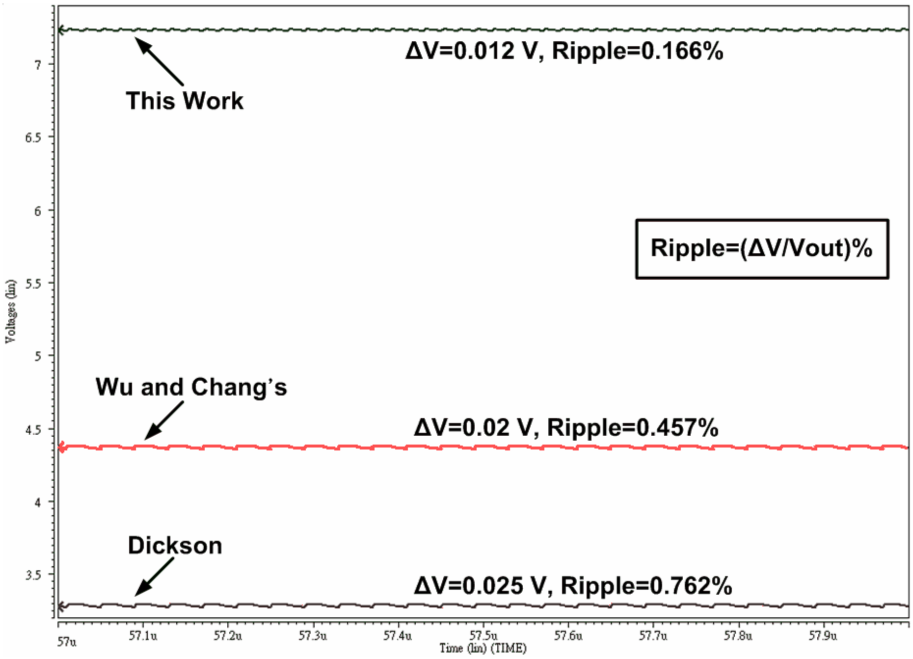


Fig. 5.8. Simulated output waveforms of the Dickson, Wu and Chang's, and the proposed charge pump circuits of 4 stages with 20-μA output current and 1.8-V power supply (VDD=1.8 V).

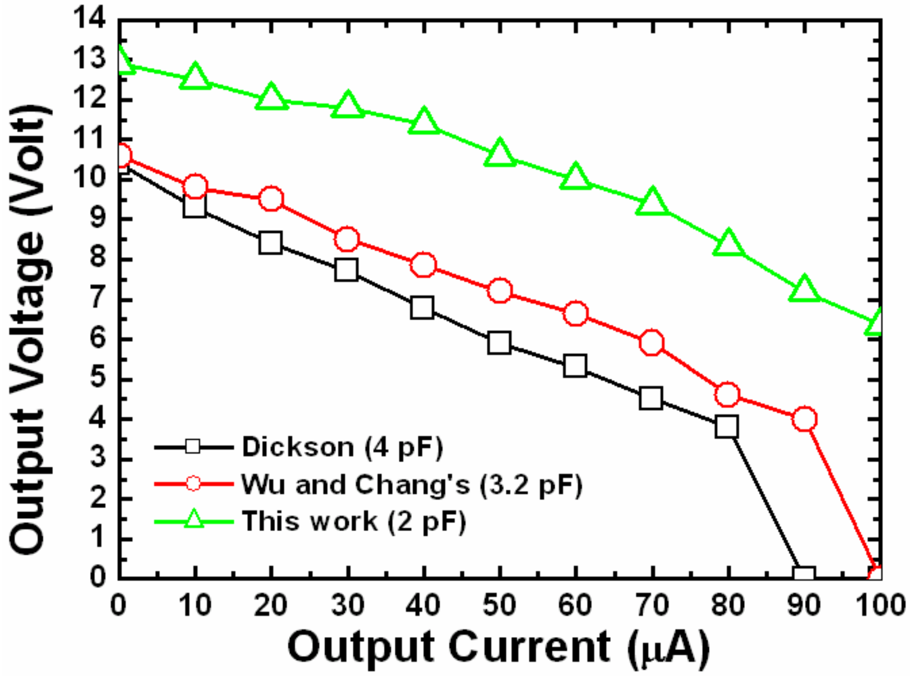
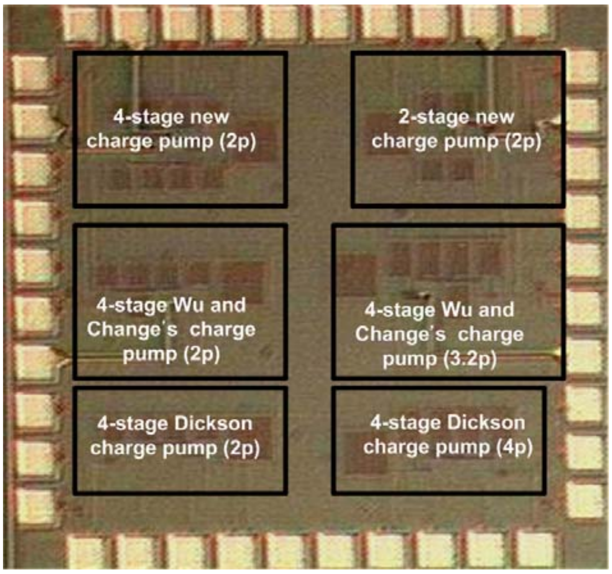
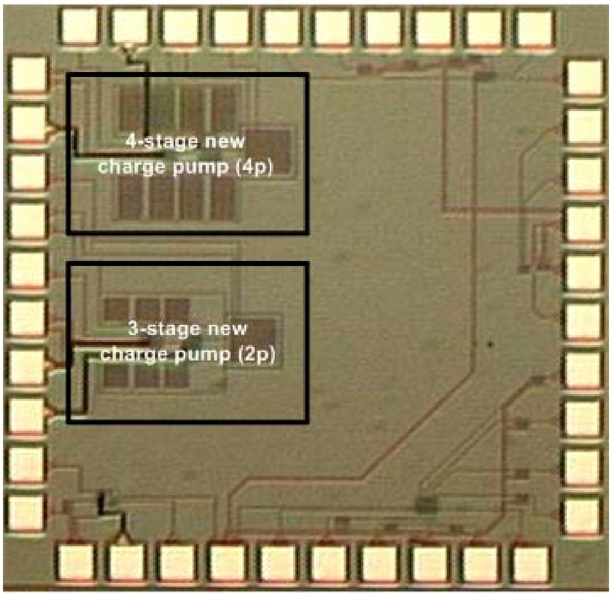


Fig. 5.9. Simulated output voltages of different 4-stage charge pump circuits in the 0.35-μm 3.3-V CMOS process under different output currents with the power supply voltage (VDD) of 3.3 V.



(a)



(b)

Fig. 5.10. Photographes of charge pump circuits in (a) chip 1, and (b) chip 2, fabricated in the 0.35-μm 3.3-V CMOS process.

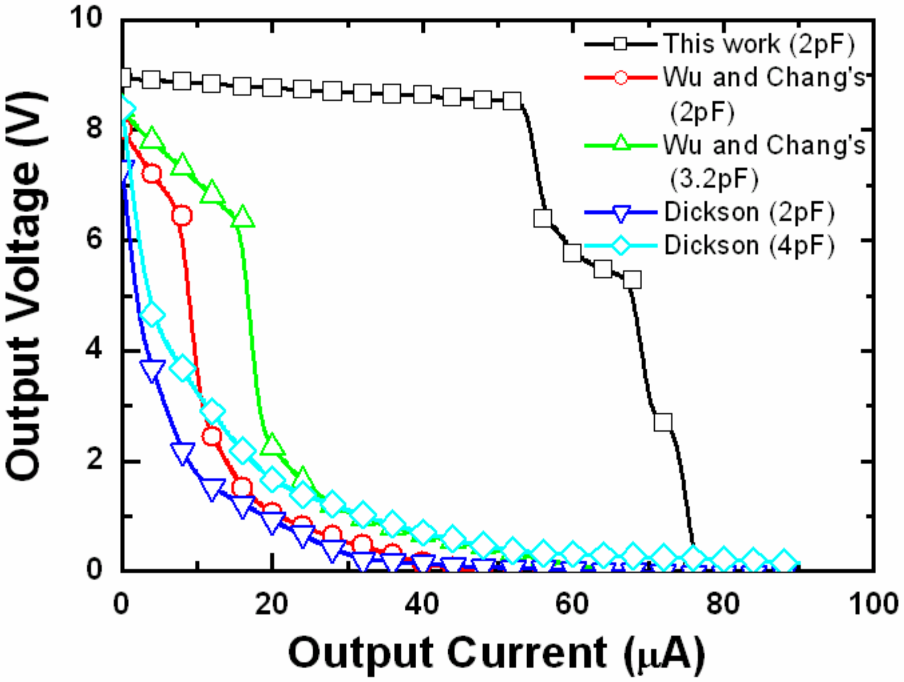


Fig. 5.11. Measured output voltages of different charge pump circuits with 3.3-V power supply (VDD=3.3 V), where the stage number is 4.

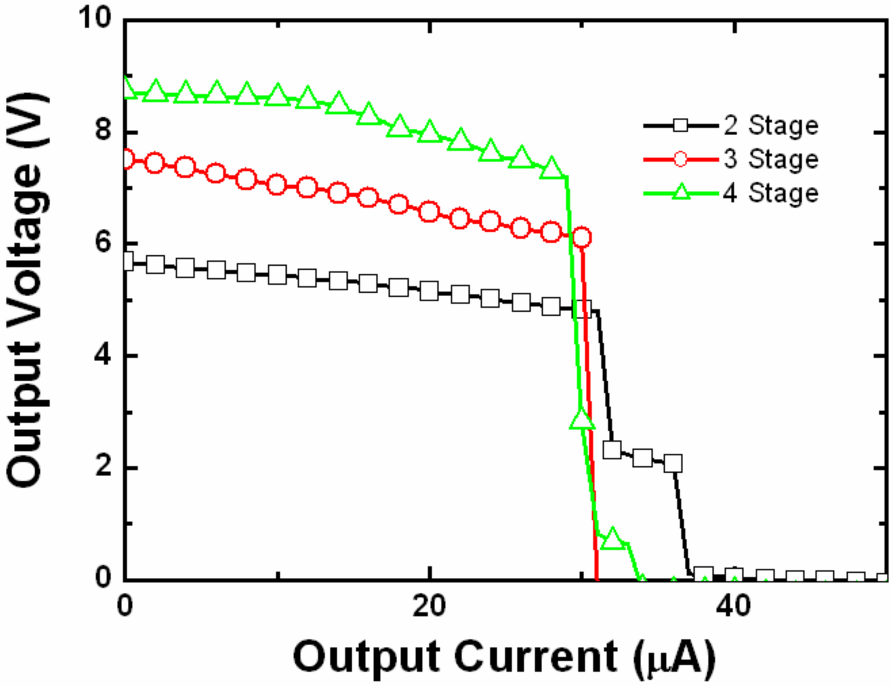


Fig. 5.12. Measured output voltages of the new proposed 2-stage, 3-stage, and 4-stage charge pump circuits with 2-V power supply (VDD=2 V) under different output currents.

CHAPTER 6

Ultra-High-Voltage Charge Pump Circuit With Polysilicon Diodes in Low-Voltage Standard CMOS Processes

This chapter presents an on-chip ultra-high-voltage charge pump circuit realized with the polysilicon diodes in the low-voltage standard CMOS processes. Because the polysilicon diodes are fully isolated from the silicon substrate, the output voltage of the charge pump circuit is not limited by the junction breakdown voltage of MOSFETs. The polysilicon diodes can be implemented in the standard CMOS processes without extra process steps. The proposed ultra-high-voltage charge pump circuit has been fabricated in a 0.25-μm 2.5-V standard CMOS process. The output voltage of the 4-stage charge pump circuit with 2.5-V power supply voltage (VDD=2.5 V) can be pumped up to 28.08 V, which is much higher than the n-well/p-substrate breakdown voltage (~18.9 V) in a 0.25-μm 2.5-V bulk CMOS process.

6.1. Background

Charge pump circuits can generate the dc voltages those are higher than the normal power supply voltage (VDD) or lower than the ground voltage (GND). Charge pump circuits are usually applied to the nonvolatile memories, such as EEPROM and flash memories, to write or to erase the floating-gate devices [59]. Besides, charge pump circuits can be also used in some low-voltage designs to improve the circuit performance [81]. In the MEMS (micro electro mechanical systems) and electroluminescent display applications, the charge pump circuit must provide the output voltage higher than 15 V, even up to 60 V [79], [82]-[84]. Early, the pn-junction diodes were applied in the charge pump circuit. However, it is difficult to implement the fully independent pn-junction diodes in the common silicon substrate. The charge pump circuit realized with transistors in the diode-connected style was reported by Dickson [63]. Owing to the body effect, the pump efficiency of the Dickson charge pump circuit is degraded as the number of the stages increases. Several modified charge pump circuits based on the Dickson charge pump circuit were reported to enhance the pumping efficiency [75], [77].

As the semiconductor process is scaled down, the normal circuit operation voltage (VDD) of the integrated circuits (ICs) is also decreased. The reliability issue must be considered to design the charge pump circuit in the deep-sub-micron CMOS processes, such as the gate-oxide overstress problem [77]. Fig. 6.1(a) shows the cross section of the p+/n-well diode in the grounded p-substrate with the shallow-trench isolation (STI). The p+/n-well diode is one kind of the pn-junction diodes in the bulk CMOS process. In Fig. 6.1(a), an undesired parasitic pn-junction exists between the n-well and the grounded p-type substrate. If the voltage on the cathode of the p+/n-well diode is larger than the junction breakdown voltage between the n-well and the grounded p-substrate, the charges on the cathode will leak to ground through the parasitic pn-junction. Fig. 6.1(b) shows the cross section of the diode-connected NMOS, whose gate and drain are connected together, in the grounded p-substrate. In Fig. 6.1(b), an undesired pn-junction parasitizes between the n+ region (source/drain) and the grounded p-type substrate. Similarly, if the voltages on the cathode or anode of the diode-connected NMOS are larger than the junction breakdown voltage between the n+ region (source/drain) and the grounded p-type substrate, the charges on the cathode or anode will also leak to ground through the parasitic junction. Thus, whenever the p+/n-well (pn-junction) diodes or the diode-connected MOSFETs are used to design the charge pump circuit, the maximum output voltage will be limited by the breakdown voltage of the undesired junctions in the standard CMOS process. In the SOI (silicon-on-insulator) CMOS process, the devices are isolated to others by the insulator layer. Thus, the charge pump circuits realized in the SOI process can pump the output voltage higher without the limitation of the parasitic pn-junctions [79], [82]. However, the SOI CMOS process is more expensive than the standard (bulk) CMOS process.

In this chapter, an on-chip ultra-high-voltage charge pump circuit realized with the polysilicon diodes is proposed. The polysilicon diodes have been used in the negative charge pump circuit [55] and the on-chip ESD protection circuit [85]. Because the anode and the cathode of the polysilicon diodes are fully isolated from the silicon substrate, the voltages on the anode or the cathode of the polysilicon diodes are not limited by the breakdown voltage of the undesired parasitic pn-junction. The proposed on-chip ultra-high-voltage charge pump circuit with the polysilicon diodes has been successfully implemented and verified in a 0.25-μm 2.5-V standard (bulk) CMOS process.

6.2. Polysilicon Diodes

6.2.1. Device Structure of the Polysilicon Diode

The gates of PMOS and NMOS are both realized with the n-type doped polysilicon in the early standard CMOS processes. Due to the work function consideration, the gate of PMOS and the gate of NMOS are realized with the p-type doped polysilicon and the n-type doped polysilicon, respectively, in the recent sub-quarter-micron standard CMOS processes. In order to implement the different types of the polysilicon gates, the intrinsic polysilicon layer is deposited first, and then the p-type and n-type impurities are doped into the intrinsic polysilicon layer to form the PMOS gate and the NMOS gate, respectively. Hence, the diode can be realized on the polysilicon layer in the recent standard CMOS processes those have separated doping impurities for PMOS and NMOS gates.

Fig. 6.2 depicts the cross section of the polysilicon diode in the bulk CMOS process. As shown in Fig. 6.2, the STI layer is located above the silicon substrate. The polysilicon layer is deposited on the STI layer. Then, the p-type and n-type highly doped regions on the polysilicon are doped with the same process step of the PMOS and NMOS source/drain ion implantation, respectively. Thus, the polysilicon diode is fully compatible to the standard CMOS process without any extra process modification. Because the polysilicon diode is implemented on the STI layer, it is isolated from the silicon substrate. The charges on the anode and the cathode of the polysilicon diode don’t leak to the silicon substrate. Therefore, the polysilicon diodes can be applied to the charge pump circuit without the limitation of the parasitic junctions. In the polysilicon diode, an extra un-doped (intrinsic) polysilicon region (i) can be inserted between the p-type and n-type doped polysilicon regions. The length (Lc) of the un-doped region can be used to adjust the I-V characteristics of the polysilicon diode.

6.2.2. Characteristics of the Polysilicon Diode

The polysilicon diodes with different lengths (Lc) of the un-doped region have been fabricated in a 0.25-μm 2.5-V bulk CMOS process, where the Lc is changed from 0.25 to 1.5 μm. Fig. 6.3 shows the measured I-V curves of the polysilicon diodes with different Lc. Fig.

6.4 shows the measured cut-in voltages of the polysilicon diodes with different Lc, where the cut-in voltages are defined at the 1-μA forward biased current. In Fig. 6.4, the cut-in voltages of these polysilicon diodes vary from 0.47 to 0.58 V. As the length of the un-doped region is larger than 0.9 μm, the cut-in voltage saturates at around 0.58 V.

Fig. 6.5 shows the measured reverse breakdown voltages and the measured reverse leakage currents of the polysilicon diodes with different lengths (Lc) of the un-doped center region, where the reverse breakdown voltages are defined at the 1-μA reverse biased current and the reverse leakage currents are defined at the 2.5-V reverse biased voltage. In Fig. 6.5, the reverse breakdown voltage increases when the Lc increases. As the Lc is longer than 1.2 μm, the reverse breakdown voltage is higher than 20 V. Moreover, the reverse breakdown voltage is 33 V when the length of the un-doped region is 1.5 μm. Hence, the reverse breakdown voltage of the polysilicon diode can be adjusted by changing the length of the un-doped center region (Lc) for different applications. Besides, as shown in Fig. 6.5, because the polysilicon diodes (Lc=0.2, 0.3, 0.5, and 0.7 μm) under 2.5-V reverse biased voltage are operated at the reverse breakdown region, the reverse leakage currents of the polysilicon diodes (Lc=0.2, 0.3, 0.5, and 0.7 μm) are much larger than those of the polysilicon diodes (Lc=0.9, 1.0, 1.2, 1.3, and 1.5 μm). Because the polysilicon diodes (Lc=0.9, 1.0, 1.2, 1.3, and 1.5 μm) under 2.5-V reverse biased voltage are operated at the reverse saturation region, the leakage currents saturate lower than 1 nA.

6.3. Ultra-High-Voltage Charge Pump Circuit

6.3.1. Circuit Implementation

Fig. 6.6 depicts the 4-stage charge pump circuit designed with 5 polysilicon diodes (PD1~PD5), where the clock signals, CLK and CLKB, are out-of-phase with the amplitudes of VDD. RL and CL in Fig. 6.6 represent the output loading of resistance and capacitance, respectively. CL can make the output voltage of the charge pump circuit more stable. As shown in Fig. 6.6, the charge pump circuit uses the polysilicon diodes as the charge transfer devices. The charges are pushed from the power supply (VDD) to the output node (Vout) stage by stage every clock cycle. The voltage fluctuation between each stage can be expressed as

$$\Delta V = V_{clk} \cdot \frac{C_{pump}}{C_{pump} + C_{par}} - \frac{I_o}{f \cdot \left(C_{pump} + C_{par}\right)}, \tag{6.1}$$

where V_{clk} is the voltage amplitude of the clock signals, CLK and CLKB, C_{pump} is the pumping capacitance, C_{par} is the parasitic capacitance at each pumping node, I_o is output current, and f is the clock frequency. The output voltage of the charge pump circuit can be expressed as

$$\mathrm{Vout} = (\mathrm{VDD} - \mathrm{V_D}) + \mathrm{n} \cdot (\Delta V - \mathrm{V_D}), \tag{6.2}$$

where $\mathrm{V_D}$ is the cut-in voltage of the polysilicon diode and n is the number of stages in the charge pump circuit. If C_{par} and I_o are small enough and C_{pump} is large enough, C_{par} and I_o can be ignored in equation 6.1. Because V_{clk} is usually with the same voltage level as the normal power supply voltage (VDD), the voltage fluctuation between each stage can be simply expressed as

$$\Delta V \approx V_{clk} = \mathrm{VDD}. \tag{6.3}$$

Hence, equation 6.2 can be simplified as

$$\mathrm{Vout} = (\mathrm{n}+1) \cdot (\mathrm{VDD} - \mathrm{V_D}). \tag{6.4}$$

The power efficiency of the charge pump circuit is defined as

$$\mathrm{Efficiency} = \frac{\mathrm{Vout} \cdot Io}{\mathrm{VDD} \cdot I_{VDD}}. \tag{6.5}$$

In equation 6.5, I_{VDD} is the total current flows from the power supply (VDD). I_{VDD} can be derived as [86]

$$I_{VDD} = [(\mathrm{n}+1) + \frac{C_{par}}{C_{pump}} \cdot \frac{\mathrm{n}^2 \cdot (\mathrm{VDD} - \mathrm{V_D})}{(\mathrm{n}+1) \cdot (\mathrm{VDD} - \mathrm{V_D}) - Vout}] \cdot Io. \tag{6.6}$$

Thus, equation 6.6 can be substituted in equation 6.5. The power efficiency of the charge pump circuit can be easily calculated.

6.3.2. Experimental Results

The 4-stage, 8-stage, and 12-stage charge pump circuits with 10-pF on-chip (MIM) pumping capacitors and the polysilicon diodes of 0.5-µm and 1-µm un-doped region have been fabricated in a 0.25-µm 2.5-V bulk CMOS process. The photograph of the 4-stage charge pump circuit realized with 5 polysilicon diodes (Lc=0.5 µm) is shown in Fig. 6.7. The independent polysilicon diodes with different lengths of the un-doped region are also implemented in this testchip.

Fig. 6.8 shows the measured waveforms of the 12-stage charge pump circuit with the polysilicon diodes (Lc=0.5 µm) to drive the capacitive output load. In Fig. 6.8, the power supply voltage (VDD) and the amplitude of the clock signals (CLK and CLKB) are 2.5 V, and the clock frequency is 1 MHz. As shown in Fig. 6.8, the output voltage of the charge pump circuit to drive the capacitive load is as high as 28.08 V, which is much higher than the n-well/p-substrate breakdown voltage (~18.9 V) in the given 0.25-µm 2.5-V bulk CMOS process.

Fig. 6.9 shows the measured output voltages of the 4-stage, 8-stage, and 12-stage charge pump circuits with the polysilicon diodes of 0.5-µm or 1-µm un-doped region (Lc). In Fig. 6.9, the proposed charge pump circuits drive only the capacitive loads with the clock frequency of 1 MHz and the power supply voltage (VDD) of 2.5 V. As shown in Fig. 6.9, the measured output voltages of the proposed charge pump circuits with the polysilicon diodes (Lc=0.5 or 1 µm) are almost the same. The length of the un-doped region (Lc) doesn't obviously affect the output voltage of the proposed charge pump circuit because the voltage across each polysilicon diode doesn't exceed VDD (2.5 V), which is much smaller than the reverse breakdown voltages of the polysilicon diodes (Lc=0.5 or 1 µm).

Fig. 6.10 shows the measured output voltages of the 4-stage charge pump circuit with the polysilicon diodes (Lc=1 µm) under different clock frequencies, where the power supply voltage (VDD) is 2.5 V. When the clock frequency is increased, the output voltages of the charge pump circuit are also increased. But, when the clock frequency is low, the output voltages of the charge pump circuit are degraded, especially with a small RL. In Fig. 6.10, the charge pump circuit can pump the output voltage close to the ideal value in equation 6.4 when the RL is large and the clock frequency is high.

Fig. 6.11 compares the measured output voltages of the 4-stage charge pump circuits with the polysilicon diodes of 0.5-µm and 1-µm un-doped region under different power supply voltages (VDD). In Fig. 6.11, the charge pump circuits drive only the capacitive loads, and the clock frequency is 100 kHz. As shown in Fig. 6.11, the polysilicon diode with long length (Lc=1 µm) can generate a higher output voltage level than that with short length (Lc=0.5 µm) As the power supply voltage (VDD) is higher than the breakdown voltage of the polysilicon diode with 0.5-µm un-doped region but still lower than that of the polysilicon diode with 1-µm un-doped region, the charge pump circuit with the polysilicon diode of 1-µm un-doped region still pumps the output voltage higher, but the output voltage of the charge pump circuit with the polysilicon diode of 0.5-µm un-doped region is degraded.

Fig. 6.12 shows the measured output voltage of the 4-stage charge pump circuit (Lc=1 μm) with the output resistors of 1 MΩ, 10 MΩ, and without the output resistor when the clock frequency is 100 kHz. As shown in Fig. 6.13, the output voltage is degraded when the RL is small.

6.3.3. Discussions

Table 6.1 compares the polysilicon diode (this work), pn-junction diode, MOS diode (Dickson) [63] charge pump circuits. The voltage fluctuations between each stage in the polysilicon diode, pn-junction diode, and MOS diode (diode-connected MOS) charge pump circuits are $VDD–V_{D\text{-}P}$, $VDD–V_{D\text{-}PN}$, and $VDD–V_t$, respectively. $V_{D\text{-}P}$ and $V_{D\text{-}PN}$ are the cut-in voltages of the polysilicon and pn-junction diodes, respectively, and V_t is the threshold voltage of the MOS diode.

However, V_t increases due to the body effect as the number of stages increases. The power efficiencies of the polysilicon diode, pn-junction diode, MOS diode charge pump circuits only depends on the parasitic capacitance (*Cpar*) at each stage if the charge pump circuits are applied with the same number (n) of stages, the same pumping capacitance (*Cpump*), and the same clock frequency (*f*) [87]. The parasitic capacitance of the polysilicon diode has been discussed in [88]. The parasitic capacitance of the polysilicon diode is smaller than other, because the polysilicon diode is formed on the STI layer, the pn-junction diode has larger parasitic capacitance between n-well and p-substrate, and the MOS diode has larger gate capacitance. Thus, the power efficiency of the polysilicon diode chare pump circuit is better than others. The area of the charge pump circuit is dominated by the on-chip pumping capacitors, so these three kinds of the charge pump circuits occupy almost the same chip area with the same pumping capacitors and the same number (n) of the stages. As described in the previous section, the output voltages of the pn-junction diode and MOS diode charge pump circuits are limited by the parasitic pn-junctions, but that of the polysilicon diode charge pump circuit isn’t.

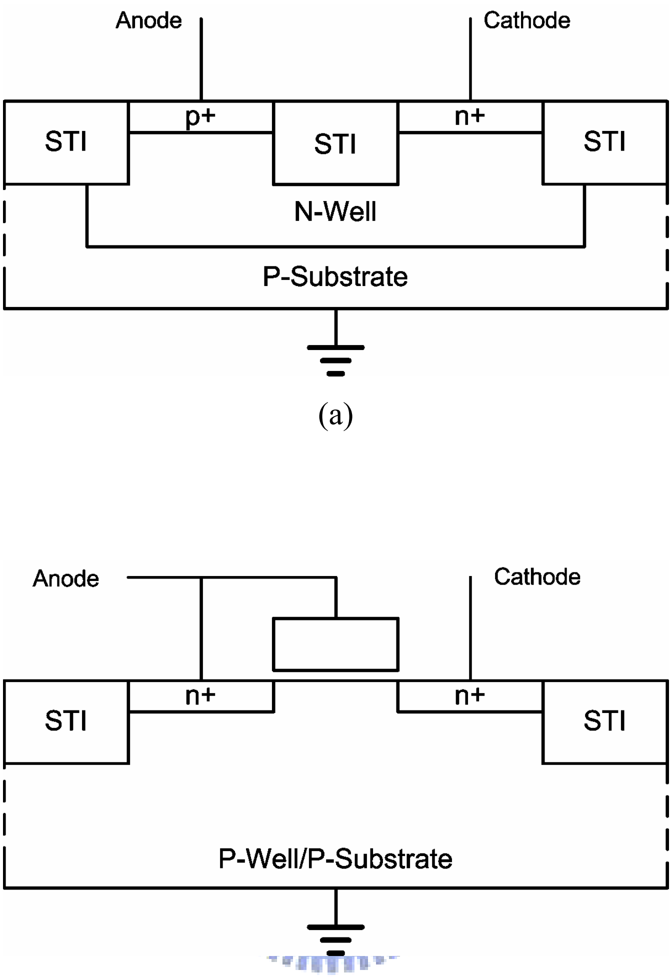
6.4. Summary

An ultra-high-voltage charge pump circuit realized with the polysilicon diodes has been successfully verified in a 0.25-µm 2.5-V bulk CMOS process. The polysilicon diodes are implemented on the STI layer, which are fully isolated from the silicon substrate. Therefore, the maximum output voltage of the proposed charge pump circuit with the polysilicon diodes isn't limited by the junction breakdown voltage. In addition, the polysilicon diodes are fully compatible to the bulk CMOS processes without any extra process modification. The 4-stage, 8-stage, and 12-stage charge pump circuits with 10-pF on-chip pumping capacitors and the polysilicon diodes of 0.5-µm and 1-µm un-doped center region have been fabricated in a 0.25-µm 2.5-V bulk CMOS process. To drive the capacitive load, the measured results show that the 4-stage charge pump circuit with the polysilicon diodes (Lc=0.5 µm) can pump the output voltage as high as 28.08 V, whereas the power supply voltage (VDD) is 2.5 V. The output loading effect and the dependence of clock frequency on the output voltage of the proposed charge pump circuit have been also measured. The proposed scheme can be applied to the ultra-high-voltage applications, such as MEMS or electroluminescent displays.

TABLE 6.1

SUMMARY OF THE POLYSILICON DIODE (THIS WORK), PN-JUNCTION DIODE, MOS DIODE CHARGE PUMP CIRCUITS

	Voltage Fluctuation	Power Efficiency	Area	Output Voltage Limitation
Polysilicon diode	$VDD - V_{D\text{-}P}$	Better	Same	No
pn-junction diode	$VDD - V_{D\text{-}PN}$	Good	Same	Yes
MOS diode	$VDD - V_t$	Good	Same	Yes



(a)

(b)

Fig. 6.1. Schematic cross sections of (a) the p+/n-well diode, and (b) the diode-connected NMOS, in grounded p-type substrate.

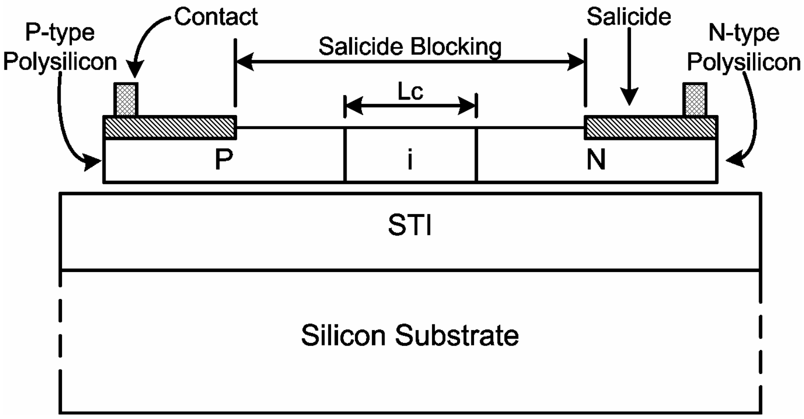


Fig. 6.2. Schematic cross section of the polysilicon diode in the bulk CMOS process.

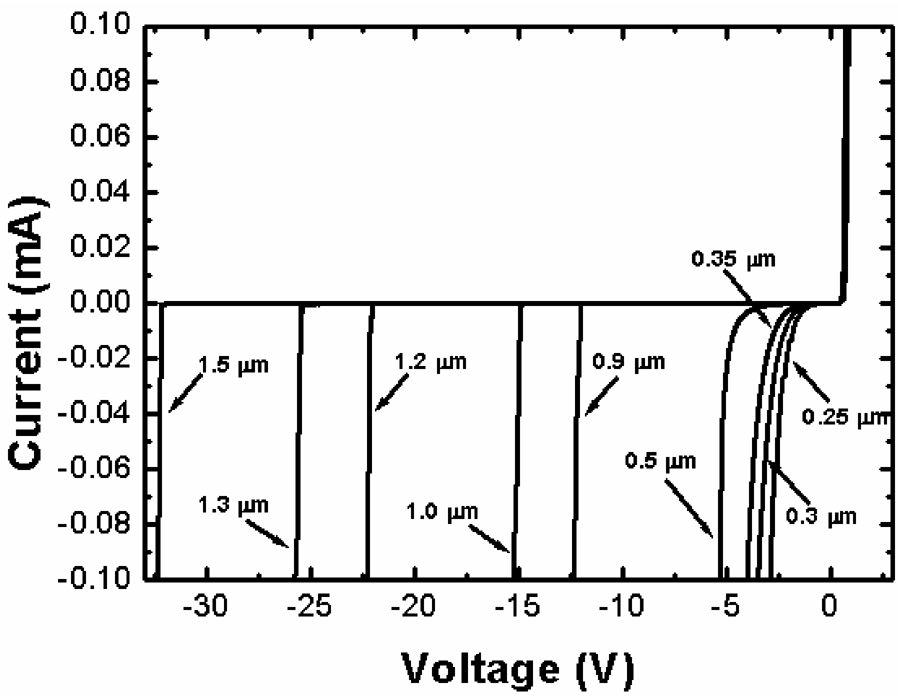


Fig. 6.3. Measured I-V curves of the polysilicon diodes with different lengths (Lc) of the un-doped region.

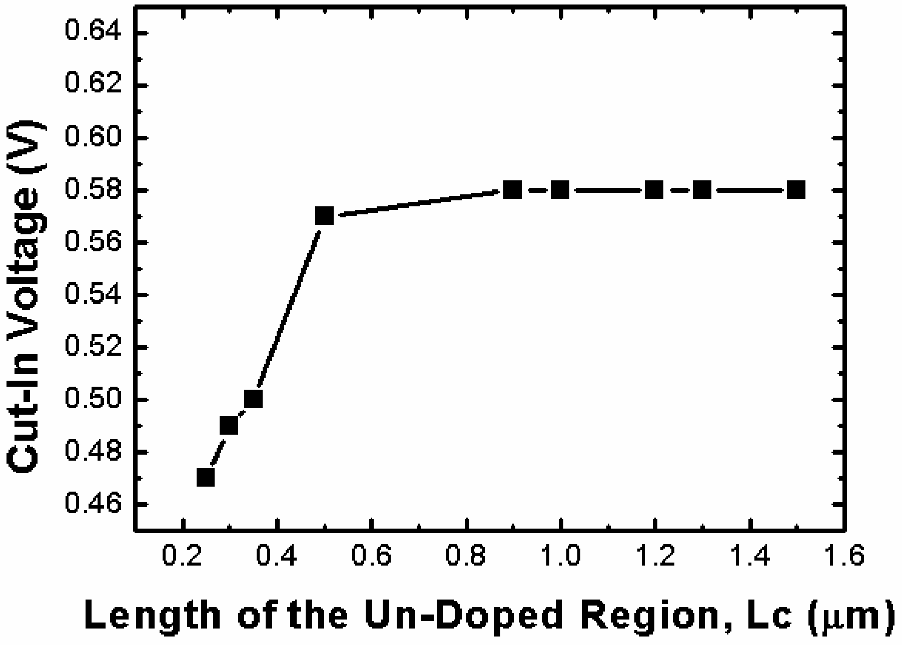


Fig. 6.4. Measured cut-in voltages of the polysilicon diodes with different lengths (Lc) of the un-doped region. The cut-in voltages are defined at the 1-μA forward biased current.

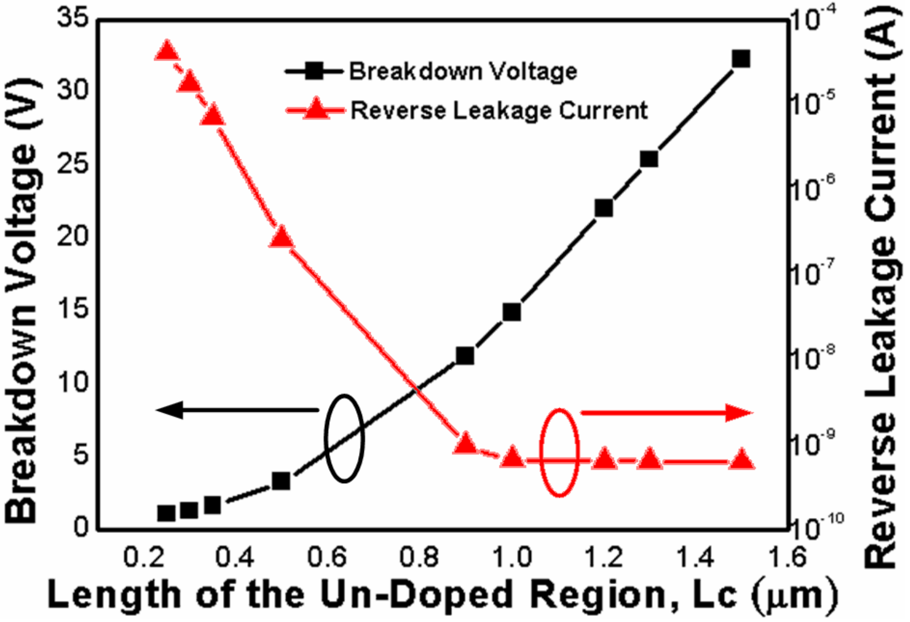


Fig. 6.5. Measured reverse breakdown voltages (@ 1-μA reverse biased current) and the reverse leakage currents (@ 2.5-V reverse biased voltage) of the polysilicon diodes with different lengths of un-doped region.

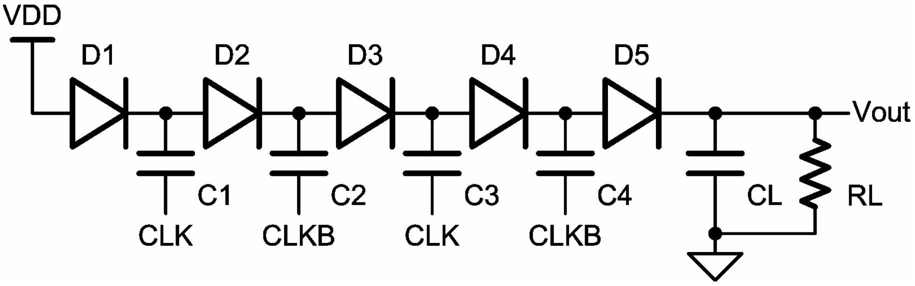


Fig. 6. 4-stage charge pump circuit realized with 5 polysilicon diodes.

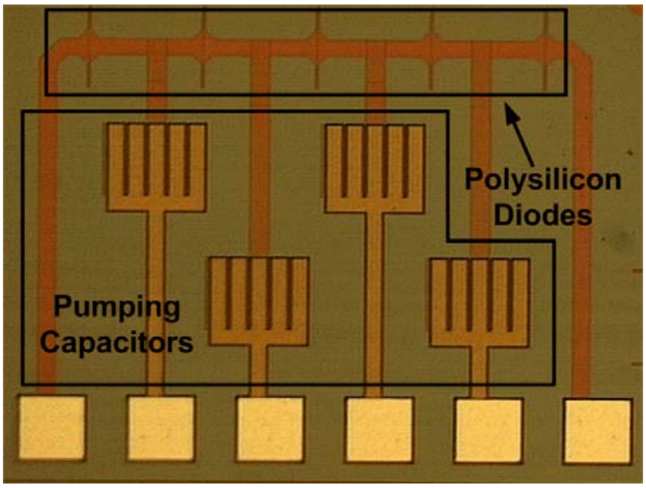


Fig. 6.7. Photograph of the 4-stage charge pump circuit with 5 polysilicon diodes (Lc=0.5 µm) fabricated in a 0.25-µm 2.5-V bulk CMOS process.

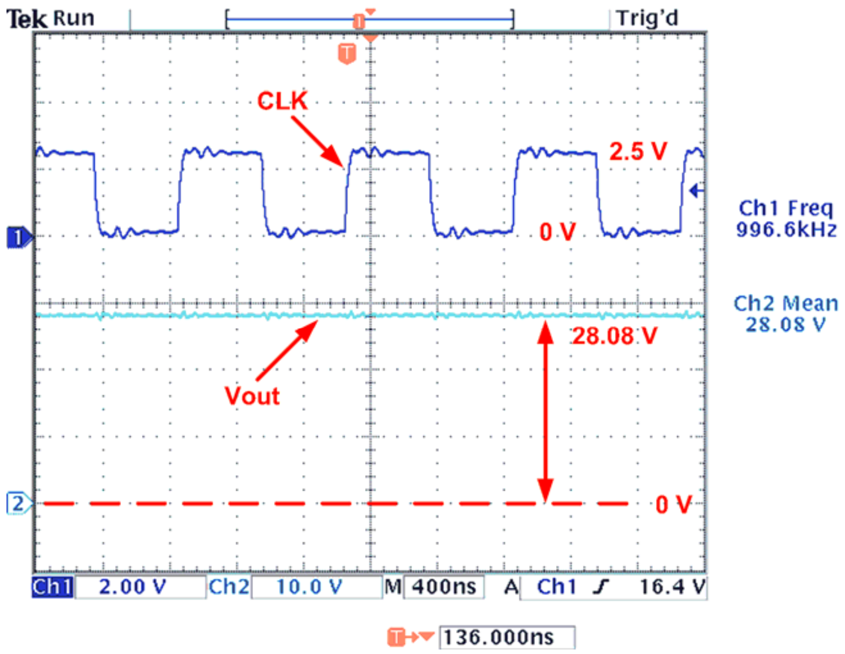


Fig. 6.8. Measured waveforms (CLK and Vout) of the 12-stage charge pump circuit with the polysilicon diodes (Lc=0.5 µm) to drive capacitive output load. The clock frequency is 1 MHz and VDD is 2.5 V.

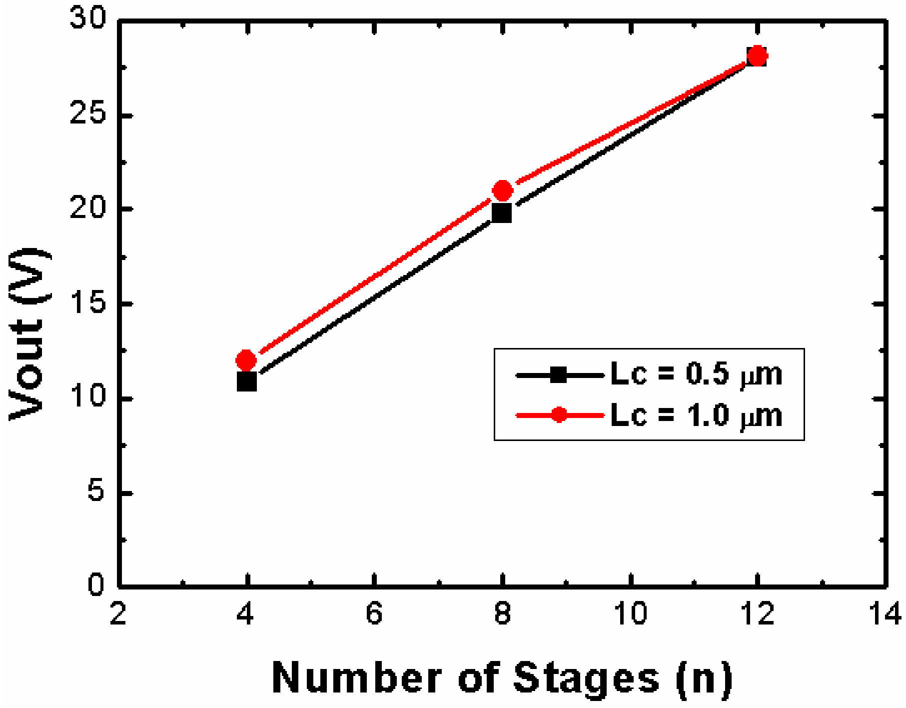


Fig. 6.9. Measured output voltages of the 4-stage, 8-stage, and 12-stage charge pump circuits with the polysilicon diodes of 0.5-µm and 1-µm un-doped region to drive capacitive load. The clock frequency is 1 MHz and VDD is 2.5 V.

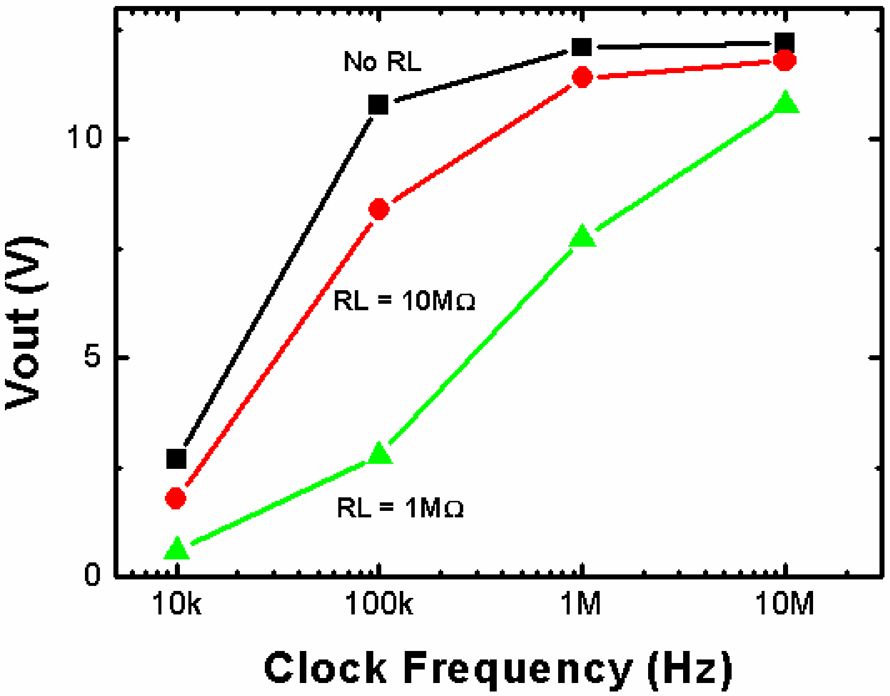


Fig. 6.10. Measured output voltages of the 4-stage charge pump circuit (Lc=1 μm) with the output loading of 1 MΩ, 10 MΩ, or without the output resistor under different clock frequencies. The power supply voltage (VDD) is 2.5 V.

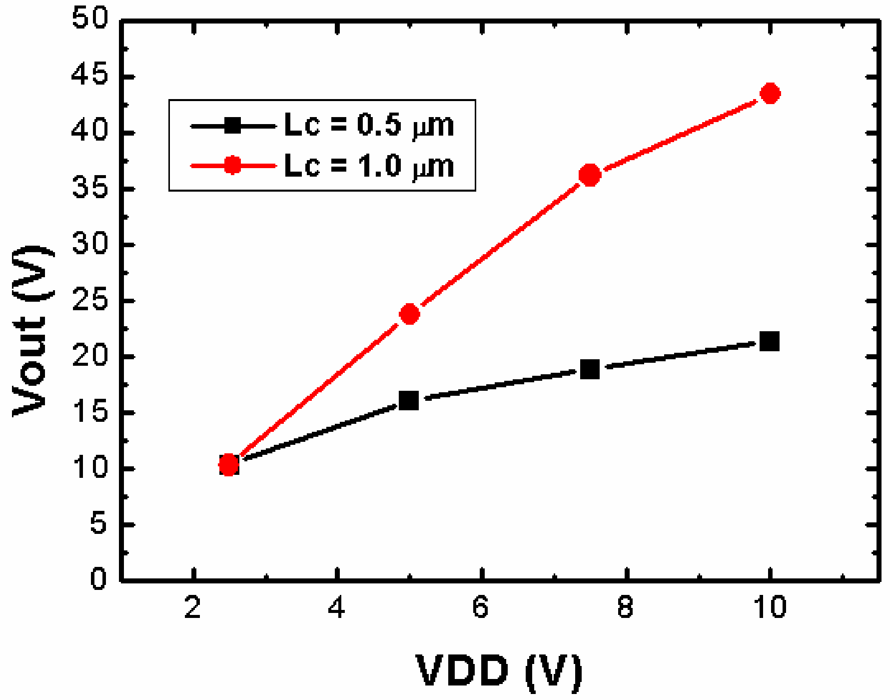


Fig. 6.11. Measured output voltages of the 4-stage charge pump circuits with the polysilicon diodes of 0.5-μm and 1-μm un-doped region to drive capacitive loads under different VDD. The clock frequency is 100 kHz.

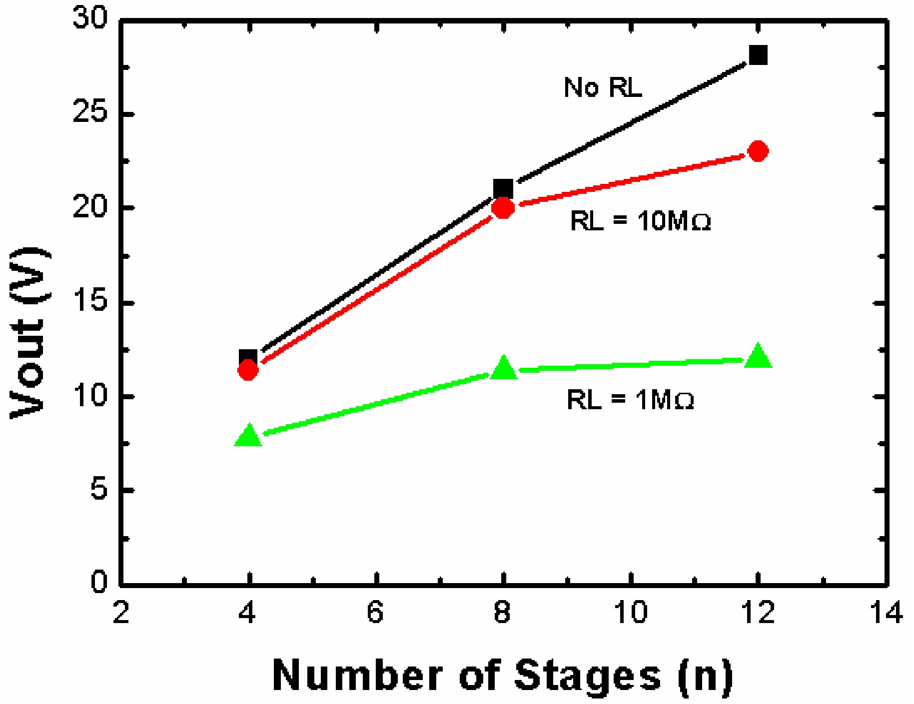


Fig. 12. Measured output voltages of the 4-stage charge pump circuits (Lc=1 μm) with the output resistors of 1 MΩ and 10 MΩ and without the output resistor under different VDD. The clock frequency is 100 kHz.

CHAPTER 7

Conclusions and Future Works

This chapter summarizes the main results of this dissertation. Then, some suggestions for the future works about the high-voltage circuit design in low-voltage CMOS processes are also addressed in this chapter.

7.1. Main Results of This Dissertation

As the semiconductor process is scaled down, the thickness of gate oxide becomes thinner in order to increase the current density of device. Besides, due to the reliability issue, the power supply voltage (VDD) must be decreased in the advanced processes. However, in an electronic system, some chips are operating at different voltage levels. Thus, some circuits must be designed in low-voltage processes but still operated at high-voltage environments. In this dissertation, several circuits operating in high-voltage environments but realized with low-voltage devices have been presented.

Chapter 2 has presented a new mixed-voltage I/O buffer realized with only thin gate-oxide (low-voltage) devices. The proposed mixed-voltage I/O buffer with simpler dynamic n-well bias circuit and gate-tracking circuit can prevent the undesired leakage current paths and the gate-oxide reliability problem, which occur in the conventional CMOS I/O buffer. The new mixed-voltage I/O buffer has been fabricated and verified in a 0.25-μm 2.5-V CMOS process to serve 2.5/5-V I/O interface. Besides, another 2.5/5-V mixed-voltage I/O buffer without the subthreshold leakage problem for high-speed applications has also been presented in Chapter 2. The speed, power consumption, area, and noise among these mixed-voltage I/O buffers have been compared and discussed. The new proposed mixed-voltage I/O buffers realized with 1×VDD devices can be easily applied in any 1×VDD/2×VDD mixed-voltage interface.

Chapter 3 has presented an input buffer and an output buffer realized with 1/2.5-V low-voltage devices for 3.3-V applications. Due to the high-integration trend of SOC (system-on-a-chip), an electronic system may be integrated into a single chip. Therefore, there are digital circuits and analog circuits in a chip. For example, the digital part of a chip is designed with 1-V devices to decrease its power consumption, the analog part is designed with 2.5-V devices to improve the circuit performance, and the chip-to-chip interface is 3.3-V PCI-X in a 0.13-µm 1/2.5-V CMOS process. Thus, the traditional I/O circuits are not suitable for this application. An input buffer with the proposed Schmitt trigger circuit in a 0.13-µm 1/2.5-V CMOS process has been presented first. Then, an output buffer with the proposed level converter in a 0.13-µm 1/2.5-V CMOS process has been also presented in this chapter.

An NMOS-blocking technique for mixed-voltage I/O buffer design has been presented in Chapter 4. Unlike the traditional mixed-voltage I/O buffer design, the mixed-voltage I/O buffer realized with only 1×VDD devices by using the NMOS-blocking technique can receive 2×VDD, 3×VDD, and even 4×VDD input signal without the gate-oxide reliability issue. In this chapter, the 2×VDD input tolerant mixed-voltage I/O buffer by using the NMOS-blocking technique has been verified in a 0.25-µm 2.5-V CMOS process to serve 2.5/5-V mixed-voltage interface. The 3×VDD input tolerant mixed-voltage I/O buffer by using the NMOS-blocking technique has been verified in a 0.13-µm 1-V CMOS process to serve 1/3-V mixed-voltage interface. The proposed NMOS-blocking technique can be extended to design the 4×VDD, 5×VDD, and even 6×VDD input tolerant mixed-voltage I/O buffers. The limitation of the NMOS-blocking technique is the breakdown voltage of the pn-junction in the given CMOS process.

Chapter 5 has presented a new charge pump circuit without the gate-oxide overstress. Because the charge transfer switches of the new proposed charge pump circuit can be fully turned on and turned off, as well as the output stage doesn’t have the threshold drop problem, its pumping efficiency is higher than that of the prior designs. The gate-drain and the gate-source voltages of all devices in the proposed charge pump circuit don’t exceed VDD, so the proposed charge pump circuit doesn’t suffer the gate-oxide reliability problem. Besides, the proposed charge pump circuit has two pumping branches pumping the output node alternately so the output voltage ripple is small. In this work, two test chips have been implemented in a 0.35-µm 3.3-V CMOS process to verify the proposed charge pump circuit. The measured output voltage of the new proposed 4-stage charge pump circuit with each pumping capacitor of 2 pF to drive the capacitive output load is around 8.8 V under 3.3-V power supply (VDD=3.3 V), which is limited by the junction breakdown voltage of the parasitic pn-junction in the given process. The new proposed charge pump circuit is suitable for applications in low-voltage CMOS processes because of its high pumping efficiency and no overstress across the gate oxide of devices.

An on-chip ultra-high-voltage charge pump circuit designed with the polysilicon diodes in low-voltage standard CMOS processes has been presented in Chapter 6. Because the polysilicon diodes are fully isolated from the silicon substrate, the output voltage of the charge pump circuit is not limited by the junction breakdown voltage of MOSFETs. The polysilicon diodes can be implemented in the standard (bulk) CMOS processes without extra process steps. The proposed ultra-high-voltage charge pump circuit has been fabricated in a 0.25-μm 2.5-V standard CMOS process. The measured output voltage of the 4-stage charge pump circuit with 2.5-V power supply voltage (VDD=2.5 V) can be pumped up to 28.08 V, which is much higher than the n-well/p-substrate breakdown voltage (~18.9 V) in the 0.25-μm 2.5-V standard CMOS process.

7.2. Future Works

In this dissertation, five I/O circuits realized with low-voltage devices for high-voltage applications have been presented. However, the traditional electrostatic discharge (ESD) protection circuits are not suitable for these applications. In addition, the more robust ESD protection circuits are required in the nanometer processes. Therefore, new ESD protection circuits realized in low-voltage processes must be developed in the future.

Although the DC overstress on the gate oxide is more harmful than AC overstress, the operation frequency becomes higher in the advanced ICs. The AC overstress is also an important issue when the operation frequency is high. Thus, not only the DC overstress on the gate oxide but also the AC overstress must be considered in the high-voltage circuits realized with low-voltage devices in the future IC design.

Due to the trends of SOC and CMOS technology, more circuits will be deigned with low-voltage processes and integrated in a single chip. Thus, not only the I/O circuits and charge pump circuits but also other circuits, such as OPAMP (operational amplifier), ADC (analog-to-digital converter), and so on, must be designed in low-voltage CMOS processes for high-voltage applications. Such design topic still continues to the future research.

References

[1] Semiconductor Industry Association (SIA), *International Technology Roadmap for Semiconductors (ITRS)*, 2005.

[2] R. S. Scott, N. A. Dumin, T. W. Hughes, D. J. Dumin, and B. T. Moore, "Properties of high-voltage stress generated traps in thin silicon oxide," *IEEE Trans. Electron Devices*, vol. 43, no. 7, pp. 1133–1143, July 1996.

[3] H. Iwai and H. S. Momose, "Ultra-thin gate oxides-performance and reliability," in *IEDM. Tech. Dig.*, 1998, pp. 163–166.

[4] J. H. Stathis, "Gate-oxide reliability for nano-scale CMOS," in *Proc. Int. Symp. Physcial and Failure Analysis of Integrated Circuits*, 2005, pp. 127–130.

[5] J. S. Suehle, "Ultrathin gate oxide reliability: physical models, statistics, and characterization," *IEEE Trans. Electron Devices*, vol. 49, no. 6, pp. 958–971, June 2002.

[6] Y. Leblebici, "Design consideration for CMOS digital circuits with improved hot-carrier reliability," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 1014–1024, July 1996.

[7] J. Y. Choi, P. K. Ko, and C. Hu, "Hot-carrier-induced MOSFET degradation under AC stress," *IEEE Electron Device Lett.*, vol. 8, no. 8, pp. 333–335, Aug. 1987.

[8] E. R. Minami, S. B. Kuusinen, E. Rosenbaum, P. K. Ko, and C. Hu, "Circuit-level simulation of TDDB failure in digital CMOS circuits," *IEEE Trans. Semiconduct. Manufact.*, vol. 8, no. 3, pp. 370–377, Aug. 1995.

[9] A. M. Yassine, H. E. Nariman, M. McBride, M. Uzer, and K. R. Olasupo, "Time dependent breakdown of ultrathin gate oxide," *IEEE Trans. Electron Devices*, vol. 47, no. 7, pp. 1416–1420, Jul. 2000.

[10] K.-H. Lee, B. R. Jones, C. Burke, L. V. Tran, J. A. Shimer, and M. L. Chen, "Lightly doped drain structure for advanced CMOS (Twin-Tub IV)," in *IEDM Tech. Dig.*, 1985, 242–245.

[11] T.-Y. Huang, I-W. Wu, and J. Y. Chen, "A MOS transistor with self-aligned polysilicon source-drain," *IEEE Electron Device Lett.*, vol. 7, no.5, pp. 314–316, May 1986.

[12] M.-L. Chen, C.-W. Leung, W. T. Cochran, W. Hungling, C. Dziuba, and T. Yang, "Suppression of Hot-Carrier Effects in Submicrometer CMOS Technology," *IEEE Trans. Electron Devices*, vol. 35, no. 12, pp. 2210–2220, Dec. 1988.

[13] I.-C. Chen, J. Y. Choi, and C. Hu, "The effect of channel hot-carrier stressing on

gate-oxide integrity in MOSFETs," *IEEE Trans. Electron Devices*, vol. 35, no.12, pp. 2253–2258, Dec. 1988.

[14] J.-S. Chen and M.-D. Ker, "Impact of MOSFET gate-oxide reliability on CMOS operational amplifiers in a 130-nm low-voltage CMOS process," in *Proc. IEEE Int. Reliability Physics Symp.*, 2005, pp. 423–430.

[15] A.-J. Annema, G. Geelen, and P. C. De Jong, "5.5-V I/O in a 2.5-V 0.25-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 528–538, Mar. 2001.

[16] B. Serneels, T. Piessens, M. Steyaert, and W. Dehaene, "A high-voltage output driver in a standard 2.5V 0.25μm CMOS technology," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2004, pp. 146–147.

[17] B. Serneels, M. Steyaert, and W. Dehaene, "A 5.5 V SOPA line driver in a standard 1.2 V 0.13 μm CMOS technology," in *Proc. IEEE European Solid-State Circuits Conf.*, 2005, pp. 303–306.

[18] T. Hasan, T. Lehmann, and C. Y. Kwok, "On-chip high voltage charge pump in standard low voltage process," *Electronics Lett.*, vol. 41, no. 15, pp. 840–842, July 2005.

[19] J. Williams, "Mixing 3 V and 5 V ICs," *IEEE Spectrum*, pp. 40–42, Mar. 1993.

[20] M.-D. Ker and C.-H. Chung, "Electrostatic discharge protection design for mixed-voltage I/O buffers," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1046–1055, Aug. 2002.

[21] A. M. Abo and P. R. Gray, "A 1.5 V, 10 bits 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[22] J.-B. Park, S.-M. Yoo, S.-W. Kim, Y.-J. Cho, and S.-H. Lee, "A 10-b 150-Msample/s 1.8 V 123-mW CMOS A/D converter with 400-MHz input bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1335–1337, Aug. 2004.

[23] M. Takahashi, T. Sakurai, K. Sawada, K. Nogami, M. Ichida, and K. Matsuda, "3.3V-5V compatible I/O circuit without thick gate oxide," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1992, pp. 23.3.1–23.3.4.

[24] D.-Y. Chen, "Design of a mixed 3.3 V and 5 V PCI I/O buffer," in *Proc. IEEE Int. ASIC Conf.*, 1996, pp. 336–339.

[25] M. J. M. Pelgrom and E. C. Dijkmans, "A 3/5 V compatible I/O buffer," *IEEE J. Solid-State Circuits*, vol. 30, no. 7, pp. 823–825, July 1995.

[26] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Overview and design of mixed-voltage I/O buffers with low-voltage thin-oxide CMOS transistors," *IEEE Trans. Circuits Syst. I:*

Regular Papers, 2006, *in press*.

[27] R. S. Scott, N. A. Dumin, T. W. Hughes, D. J. Dumin, and B. T. Moore, “Properties of high-voltage stress generated traps in thin silicon oxide,” *IEEE Trans. Electron Devices*, vol. 43, no. 7, pp. 1133–1143, July 1996.

[28] T. Furukawa, D. Turner, S. Mittl, M. Maloney, R. Serafin, W. Clark, L. Longenbach, and J. Howard, “Accelerated gate-oxide breakdown in mixed-voltage I/O circuits,” in *Proc. IEEE Int. Reliability Physics Symp.*, 1997, pp. 169–173.

[29] G. P. Singh and R. B. Salem, “High-voltage-tolerant I/O buffers with low-voltage CMOS process,” *IEEE J. Solid-State Circuits*, vol. 34, no. 11, pp. 1512–1525, Nov. 1999.

[30] K. Bult, “Analog broadband communication circuits in pure digital deep sub-micron CMOS,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1999, pp. 76–77.

[31] S. Poon, C. Atwell, C. Hart, D. Kolar, C. Lage, and B. Yeargain, “A versatile 0.25 micron CMOS technology,” in *IEDM. Tech. Dig.*, 1998, pp. 751–754.

[32] M. Hargrove, S. Crowder, E. Nowak, R. Logan, L. K. Han, H. Ng, A. Ray, D. Sinitsky, P. Smeys, F. Guarin, J. Oberschmidt, E. Crabbé, D. Yee, and L. Su, “High-performance sub-0.08 μm CMOS with dual gate oxide and 9.7 ps inverter delay,” in *IEDM. Tech. Dig.*, 1998, pp. 627–630.

[33] H.-C. Chow, “Bidirectional buffer for mixed-voltage applications,” in *Proc. IEEE Int. Symp. Circuits Syst.*, 1999, vol. 1, pp. 270–273.

[34] R. D. Adams, R. C. Flaker, K. S. Gray, and H. L. Kalter, “CMOS off-chip driver circuit,” U.S. Patent 4782250, Nov. 1, 1988.

[35] J. M. Rabaey, *Digital Integrated Circuits: A Design Perspective*, 2nd Edition, Prentice Hall, 2003.

[36] M.-D. Ker and W.-Y. Lo, “Methodology on extracting compact layout rules for latchup prevention in deep-submicron bulk CMOS technology,” *IEEE Trans. Semiconduct. Manufact.*, vol. 16, no. 2, pp. 319–334, May 2003.

[37] S.-L. Chen and M.-D. Ker, “A new Schmitt trigger circuit in a 0.13-μm 1/2.5-V CMOS process to receive 3.3-V input signals,” *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 52, no. 7, pp. 361–365, July 2005.

[38] S.-L. Chen and M.-D. Ker, “A new output buffer for 3.3-V PCI-X application in a 0.13-μm 1/2.5-V CMOS process,” in *Proc. IEEE Asia-Pacific Conf. Advanced Syst. Integrated Circuits*, 2004, pp. 380–383.

[39] PCI Special Interest Group (PCI-SIG), *PCI-X 1.0 Specification*, 1999.

[40] O. H. Schmitt, “A thermionic trigger,” *J. Science Instruments*, vol. 15, pp. 24–26, Jan. 1938.

[41] D. A. Hodges and H. G. Jackson, *Analysis and Design of Digital Integrated Circuits*, MaGraw-Hill, 1983.

[42] A. Pfister, “Novel CMOS Schmitt trigger with controllable hysteresis,” *Electronics Letters*, vol. 28, pp. 639–641, Mar. 1992.

[43] J.-B. Kuang and C.-T. Chuang, “PD/SOI CMOS Schmitt trigger circuits with controllable hysteresis,” in *Proc. IEEE Int. Symp. VLSI Technology, Syst., Applications*, 2001, pp. 283–285.

[44] S. F. Al-Sarawi, “Low-power Schmitt trigger circuit,” *Electronics Letters*, vol. 38, pp. 1009–1010, Aug. 2002.

[45] D. Kim, J. Kih, and W. Kim, “A new waveform-reshaping circuit: an alternative approach to Schmitt trigger,” *IEEE J. Solid-State Circuits*, vol. 28, pp. 162–164, Feb. 1993.

[46] M. H. Chang *et al.*, “A highly manufacturable 0.25 μm multiple-Vt dual gate oxide CMOS process for logic/embedded IC foundry technology,” in *Symp. VLSI Technology Dig. Tech. Papers*, 1998, pp. 150–151.

[47] K.-K. Young *et al.*, “A 0.13 μm CMOS technology with 93 nm lithography and Cu/low-k for high performance applications,” in *IEDM Tech. Dig.*, 2000, pp. 563–566.

[48] C. S. Chang *et al.*, “Extended 0.13 μm CMOS technology for ultra high-speed and MS/RF application segments,” in *Symp. VLSI Technology Dig. Tech. Papers*, 2003, pp. 68–69.

[49] C.-C. Yu, W.-P. Wang, and B.-D. Liu, “A new level converter for low-power applications, in *Proc. IEEE Int. Symp. Circuits Syst.*, 2001, vol. 1, pp. 113–116.

[50] N. Otsuka and M. A. Horowitz, “Circuit techniques for 1.5-V power supply flash memory,” *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1217–1230, Aug. 1997.

[51] Y. Kanno, H. Mizuno, K. Tanaka, and T. Watanabe, “Level converter with high immunity to power-supply bouncing for high-speed sub-1-V LSIs,” in *Symp. VLSI Circuits Dig. Tech. Papers*, 2000, pp. 202–203.

[52] W.-T. Wang, M.-D. Ker, M.-C. Chiang, and C.-H. Chen, “Level shifters for high-speed 1-V to 3.3-V interfaces in a 0.13-μm Cu-interconnection/low-k CMOS technology,” in *Proc. IEEE Int. Symp. VLSI Technology, Syst., Applications*, 2001, pp. 307–310.

[53] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design on mixed-voltage I/O buffer with blocking NMOS and dynamic gate-controlled circuit for high-voltage-tolerant applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2005, pp. 1859−1862.

[54] M.-D. Ker and S.-L. Chen, "Mixed-voltage I/O buffer with dynamic gate-bias circuit to achieve 3×VDD input tolerance by using 1×VDD devices and single VDD power supply," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2005, pp. 524−525, 624.

[55] M.-D. Ker, C.-Y. Chang, and H.-C. Jiang, "Design of negative charge pump circuit with polysilicon diodes in a 0.25-μm CMOS process," in *Proc. IEEE Asia-Pacific Conf. Advanced Syst. Integrated Circuits*, 2002, pp. 145−148.

[56] E. R. Minami, S. B. Kuusinen, E. Rosenbaum, P. K. Ko, and C. Hu, "Circuit-level simulation of TDDB failure in digital CMOS circuits," *IEEE Trans. Semiconduct. Manufact.*, vol. 8, no. 3, pp. 370–377, Aug. 1995.

[57] R. Moazzami and C. Hu, "Projecting oxide reliability and optimizing burn-in," *IEEE Trans. Electron Devices*, vol. 37, no. 7, pp. 1642–1650, July 1990.

[58] M. Kuriyama, S. Atsumi, A. Umezawa, H. Banba, K.-I. Imamiyu, K. Naruke, S. Yamada, E. Obi, M. Oshikiri, T. Suzuki, M. Wada, and S. Tanaka, "A 5V-only 0.6μm flash EEPROM with row decoder scheme in triple-well structure," in *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, 1992, pp. 152–153.

[59] T. Tanzawa, Y. Takano, K. Watanabe, and S. Atsumi, "High-voltage transistor scaling circuit techniques for high-density negative-gate channel-erasing NOR flash memory," *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp. 1318–1325, Oct. 2002.

[60] T. Tanzawa, T. Tanaka, T. Takeuchi, and K. Nakamura, "Circuit techniques for a 1.8-V-only NAND flash memory," *IEEE J. Solid-State Circuits*, vol. 37, no. 1, pp. 84–89, Jan. 2002.

[61] T. Kawahara, T. Kobayashi, Y. Jyouno, S.-I. Saeki, N. Miyamoto, T. Adachi, M. Kato, A. Sato, J. Yugami, H. Kume, and K. Kimura, "Bitline clamped sensing multiplex and accurate high voltage generator for quarter-micron flash memories," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1590–1600, Nov. 1996.

[62] R. S. Pierre, "Low-power BiCMOS op-amp with integrated current-mode charge pump," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1046–1050, Jul. 2000.

[63] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, pp.

374–378, Jun. 1976.

[64] J. S. Witters, G. Groeseneken, and H. E. Maes, "Analysis and modeling of on-chip high-voltage generator circuit for use in EEPROM circuits," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1372–1380, Oct. 1989.

[65] T. Tanzawa and T. Tanaka, "A dynamic analysis of the Dickson charge pump circuit," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1231–1240, Aug. 1997.

[66] K.-H. Choi, J.-M. Park, J.-K. Kim, T.-S. Jung, and K.-D. Suh, "Floating-well charge pump circuits for sub-2.0V single power supply flash memories," in *Symp. VLSI Circuits Dig. Tech. Papers*, 1997, pp. 61–62.

[67] J. Shin, I.-Y. Chung, Y. J. Park, and H. S. Min, "A new charge pump without degradation in threshold voltage due to body effect," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 1227–1230, Apr. 2000.

[68] J. C. Chen, T. H. Kuo, L. E. Cleveland, C. K. Chung, N. Leong, Y. K. Kim, T. Akaogi, and Y. Kasa, "A 2.7V only 8Mbx16 NOR flash memory," in *Symp. VLSI Circuits Dig. Tech. Papers*, 1996, pp. 172–173.

[69] K. Sawada, Y. Sugawara, and S. Masui, "An on-chip high-voltage generator circuit for EEPROMs with a power supply voltage below 2V," in *Symp. VLSI Circuits Dig. Tech. Papers*, 1992, pp. 75–76.

[70] S. Atsumi, M. Kuriyama, A. Umezawa, H. Banba, K. Naruke, S. Yamada, Y. Ohshima, M. Oshikiri, Y. Hiura, T. Yamane, and K. Toshikawa, "A 16-Mb flash EEPROM with a new self-data-refresh for a sector erase operation," *IEEE J. Solid-State Circuits*, vol. 29, no. 4, pp. 461–469, Apr. 1998.

[71] H. Lin and N.-H. Chen, "New four-phase generation circuits for low-voltage charge pumps," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2001, vol. I, pp. 504–507.

[72] S.-Y. Lai and J.-S. Wang, "A high-efficiency CMOS charge pump circuit," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2001, vol. IV, pp. 406–409.

[73] H. Lin, K.-H. Chang, and S.-C. Wong, "Novel high positive and negative pumping circuits for low supply voltage," in *Proc. IEEE Int. Symp. Circuits Syst.*, 1999, vol. I, pp. 238–241.

[74] C. Lauterbach, W. Weber, and D. Rőmer, "Charge sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 719–723, May 2000.

[75] J.-T. Wu and K.-L. Chang, "MOS charge pump for low-voltage operation," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 592–597, Apr. 1998.

[76] B. Kaczer, R. Degraeve, M. Rasras, K. Van de Mieroop, P. J. Roussel, and G. Groeseneken, “Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability,” *IEEE Trans. Electron Devices*, vol. 49, pp. 500−506, Mar. 2002.

[77] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, “A new charge pump circuit dealing with gate-oxide reliability issue in low-voltage processes,” in *Proc. IEEE Int. Symp. Circuits Syst.*, 2004, vol. I, pp. 321–324.

[78] R. Perigny, U.-K. Moon, and G. Temes, “Area efficient CMOS charge pump circuits,” in *Proc. IEEE Int. Symp. Circuits Syst.*, 2001, vol. I, pp. 492–495.

[79] M. R. Hoque, T. McNutt, J. Zhang, A. Mantooth, and M. Mojarradi, “A high voltage Dickson charge pump in SOI CMOS, in *Proc. IEEE Custom Integrated Circuits Conf.*, 2003, pp. 493–496.

[80] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, “Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage process,” *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp, 1100–1107, May 2006.

[81] J.-S. Wang, H.-Y. Li, C. Yeh, and T.-F. Chen, “Design technique for single-low-VDD CMOS systems,” *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1157–1165, May 2005.

[82] M. R. Hoque, T. Ahmad, T. McNutt, A. Mantooth, and M. Mojarradi, “Design technique of an on-chip, high-voltage charge pump in SOI,” in *Proc. IEEE Symp. Circuits Syst.*, 2005, pp. 133–136.

[83] J. De Vos, H. De Smet, A. M. De Cubber, and A. Van Calster, “High-voltage CdSe-Ge TFT driver circuits for passive AC-TFEL Displays,” *IEEE J. Solid-State Circuits*, vol. 34, no. 2, pp. 228–232, Feb. 1999.

[84] K. Muhlemann, “A 30-V row/column driver for flat-panel liquid crystal displays,” *IEEE J. Solid-State Circuits*, vol. 23, pp. 442–449, Apr. 1988.

[85] C.-Y. Chang and M.-D. Ker, “On-chip ESD protection design for GHz RF integrated circuits by using polysilicon diodes in sub-quarter-micron CMOS process,” in *Proc. IEEE Int. Symp. VLSI Technology Syst. Applications*, 2001, pp. 240–243.

[86] G. Palumbo, D. Pappalardo, and M. Gaibotti, “Charge-pump circuits: power-consumption optimization,” *IEEE Trans. Circuits Syst. I*, vol. 49, no. 11, pp. 1535−1542, Nov. 2002.

[87] D. Baderna, A. Cabrini, G. Torelli, and M. Pasotti, “Efficiency comparison between doubler and Dickson charge pumps,” in *Proc. IEEE Int. Symp. Circuits Syst.*, 2005, pp. 1891−1894.

[88] Y.-D. Shiu, C.-H. Chunag, and M.-D. Ker, “Investigation on RF characteristics of stacked P-I-N polyslilcon diodes for ESD protection design in 0.18-µm CMOS technology,” in *Proc. IEEE Int. Symp. VLSI Technology, Syst., Applications*, 2006, pp. 56–57.

[89] P.-H. Yang and J.-S. Wang, “Low-voltage pulsewidth control loops for SOC applications,” *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp. 1348–1351, Oct. 2002.

[90] W.-M. Lin and H.-Y. Huang, “A low-jitter mutual-correlated pulsewidth control loop circuit,” *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1366–1369, Aug. 2004.

[91] H. Tanaka, M. Aoki, T. Sakata, S. Kimura, N. Sakashita, H. Hidaka, T. Tachibana, and K. Kimura, “A precise on-chip voltage generator for gigascale DRAM with negative word-line scheme,” *IEEE J. Solid-State Circuits*, vol. 34, no. 8, pp. 1084–1090, 1999.

[92] S.-E. Kim, S.-J. Song, J.-K. Kim, S. Kim, J.-Y. Lee, and H.-J. Yoo, “A small ripple regulated charge pump with automatic pumping control schemes,” in *Proc. IEEE European Solid-State Circuits Conference*, 2004, pp. 383–386.

VITA

姓　　名：陳世倫 (Shih-Lun Chen)

性　　別：男

出生日期：民國 65 年 10 月 13 日

出 生 地：台北市

住　　址：台北市松山區吉仁里 1 鄰八德路 3 段 120 號 6 樓

學　　歷：私立輔仁大學電子工程系畢業 (84 年 9 月 - 88 年 6 月)

私立輔仁大學電子工程系碩士班畢業 (88 年 9 月 - 90 年 6 月)

國立交通大學電子研究所博士班 (90 年 9 月入學)

論文名稱：低電壓互補式金氧半製程下的高電壓電路設計

High-Voltage Circuit Design in Low-Voltage CMOS Processes

PUBLICATION LIST

(A) Regular Journal Papers

[1] H.-Y. Huang and **Shih-Lun Chen**, "Interconnect accelerating techniques for sub-100 nm giga-scale systems," *IEEE Trans. VLSI Systems*, vol.12, pp. 1192−1200, Nov. 2004.

[2] M.-D. Ker, **Shih-Lun Chen**, and C.-S. Tsai, "Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage process," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1100−1107, May 2006.

[3] M.-D. Ker, **Shih-Lun Chen**, and C.-S. Tsai, "Overview and design of mixed-voltage I/O buffers with low-voltage thin-oxide CMOS transistors," *IEEE Trans. Circuits Syst. I: Regular Papers*, in press, 2006.

[4] M.-D. Ker and **Shih-Lun Chen**, "Design of mixed-voltage I/O buffer by using NMOS-blocking technique," *IEEE J. Solid-State Circuits*, in press, 2006.

(B) Brief Journal Papers

[1] **Shih-Lun Chen** and M.-D. Ker, "A new Schmitt trigger circuit in a 0.13-μm 1/2.5-V CMOS process to receive 3.3-V input signals," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 52, no. 7, pp. 361−365, July 2005.

[2] **Shih-Lun Chen** and M.-D. Ker, "An output buffer for 3.3-V applications in a 0.13-μm 1/2.5-V CMOS process," Revised by *IEEE Trans. Circuits Syst. II: Express Briefs*.

[3] M.-D. Ker and **Shih-Lun Chen**, "Ultra-high-voltage charge pump circuit in low-voltage bulk CMOS processes with polysilicon diodes," Accepted by *IEEE Trans. Circuits Syst. II: Express Briefs*.

(C) International Conference Papers

[1] H.-Y. Huang and **Shih-Lun Chen**, "Input isolated sense amplifiers," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Scottsdale, Arizona, USA, May 2002, vol. 4, pp. 587−590.

[2] H.-Y. Huang and **Shih-Lun Chen**, "Self-isolated gain-enhanced sense amplifier," in *Proc. IEEE Asia-Pacific Conf. ASIC (AP-ASIC)*, Taipei, Taiwan, Aug. 2002, pp, 57−60.

[3] H.-Y. Huang and **Shih-Lun Chen**, “High-speed receivers for on-chip interconnections in deep-submicron process,” in *Proc. IEEE Int. Conf. Electronics, Circuits, Syst. (ICECS)*, Sept. 2002, vol. 2, pp. 769−772.

[4] H.-Y. Huang and **Shih-Lun Chen**, “Threshold triggers and accelerator for deep submicron interconnection,” in *Proc. IEEE Asia-Pacific Conf. Circuits Syst. (APCCAS)*, Oct. 2002, vol. 2, pp. 143−146.

[5] M.-D. Ker, **Shih-Lun Chen**, and C.-S. Tsai, “A new charge pump circuit dealing with gate-oxide reliability issue in low-voltage process,” in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Vancouver, British Columbia, Canada, May 2004, vol. 1, pp. 321−325.

[6] **Shih-Lun Chen** and M.-D. Ker, “A new Schmitt trigger circuit in a 0.13 μm 1/2.5 V CMOS process to receive 3.3 V input signals,” in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Vancouver, British Columbia, Canada, May 2004, vol. 2, pp. 573−576.

[7] **Shih-Lun Chen** and M.-D. Ker, “A new output buffer for 3.3-V PCI-X applications in a 0.13 μm 1/2.5 V CMOS process,” in *Proc. IEEE Asia-Pacific conf. ASIC (AP-ASIC)*, Fukuoka, Japan. Aug. 2004, pp. 112−115.

[8] H.-Y. Huang, C.-C. Wu, and **Shih-Lun Chen**, “Simultaneous current-mode bi-directional signaling for on-chip interconnection,” in *Proc. IEEE Asia-Pacific conf. ASIC (AP-ASIC)*, Fukuoka, Japan, 2004, pp. 380−383.

[9] M.-D. Ker and **Shih-Lun Chen**, “Mixed-voltage I/O buffer with dynamic gate-bias circuit to achieve 3×VDD input tolerance by using 1×VDD devices and single VDD power supply,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2005, pp. 524−525, 614.

[10] M.-D. Ker, **Shih-Lun Chen**, and C.-S. Tsai, “Design on mixed-voltage I/O buffer with blocking NMOS and dynamic gate-controlled circuit for high-voltage-tolerant applications,” in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Kobe, Japan, May 2005, pp. 1859−1862.

[11] M.-D. Ker and **Shih-Lun Chen**, “On-chip high-voltage charge pump circuit in standard CMOS process with polysilicon diodes,” in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Hsinchu, Taiwan, Nov. 2005, pp.157−160.

(D) Local Conference Papers

[1] H.-Y. Huang and **Shih-Lun Chen**, “Sense amplifiers for high-speed interconnection design,” in *Proc. 12th VLSI Design/CAD Symp.*, Hsinchu, Taiwan, Aug. 2001.

[2] H.-Y. Huang and **Shih-Lun Chen**, “Deep submicron interconnection triggers and accelerator,” in *Proc. 13th VLSI Design/CAD Symp.*, Taitung, Taiwan, Aug. 2002.

[3] **Shih-Lun Chen** and M.-D. Ker, “Schmitt trigger circuit realized by only thin-gate-oxide devices to receive high-voltage input signals in a 0.13-μm CMOS process,” in *Proc. 15th VLSI Design/CAD Symp.*, Kenting, Taiwan, Aug. 2004.

[4] H.-Y. Huang, C.-C. Wu, and **Shih-Lun Chen**, “Simultaneous current-mode bi-directional transceiver,” in *Proc. 15th VLSI Design/CAD Symp.*, Kenting, Taiwan, Aug. 2004.

(E) U.S. Patents

[1] H.-Y. Huang and **Shih-Lun Chen**, “Apparatus for capacitor-coupling acceleration,” U.S. Patent 6850089, Feb. 1, 2005.

[2] **Shih-Lun Chen** and M.-D. Ker, “Output buffer with low-voltage devices to drive high-voltage signals for PCI-X applications,” U.S. Patent 7046036, May 16, 2006.

[3] **Shih-Lun Chen** and M.-D. Ker, “Schmitt trigger circuit realized with low-voltage devices for high-voltage signal application,” U.S. Patent pending.

[4] M.-D. Ker and **Shih-Lun Chen**, “Mixed-voltage I/O buffer with low-voltage devices,” U.S. Patent pending.

[5] M.-D. Ker and **Shih-Lun Chen**, “Small output ripple charge pump regulator by using multi-phase clock signals,” U.S. Patent pending.

(F) R.O.C. Patents

[1] **陳世倫**、柯明道,“利用低電壓元件組成的高電壓共容輸出緩衝器,” 中華民國發明專利,” April 1, 2005. (專利證書號 #230507)。

[2] **陳世倫**、柯明道,“可容忍高電壓輸入且用低電壓元件組成的史密特觸發器,” 中華民國發明專利,” April 1, 2005. (專利證書號 #230510)。