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碩 士 論 文

操作於弱反轉層場效電晶體之極低功率損耗與
極小面積 CMOS 參考電壓之設計與實現

The Design and Implementation of an Ultra Low Power and Small Area CMOS Voltage Reference Based on MOSFET Operated in Weak Inversion Region

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西元二〇〇七年十月

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中文摘要

本篇論文使用 0.18 微米互補式金氧半標準製程設計並實現一個與溫度無關的穩定參考電壓源。最近幾年電池供應的系統越來越廣泛使用，隨著這個趨勢，在設計電路時都要求小面積、低功率、高效能，而很多類比電路都會需要一個穩定的參考電壓，因此本論文設計一個低功率與小面積的參考電壓去運用在電池供應的系統中。本電路工作在弱反轉區可用來取代傳統電路中的雙極性電晶體去實現與溫度無關的參考電壓，其功率消耗只有幾百奈瓦且面積只有幾百平方微米。另外，溫度範圍也可以從-80℃到 165℃，而其電壓誤差也僅有幾十毫伏特。因此，本設計可以運用在電池供應的系統去供應一個穩定的參考電壓。

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ABSTRACT

This thesis uses standard CMOS 0.18μm process technique to design and realize a stable voltage reference which does not change with temperature. In the recent years, battery-operated systems are used extensively. Along with this tendency, we demand low-power, small-area, and high performance when designing circuits. Many analog circuits need a stable voltage reference, so the thesis shows a low-power and small-area voltage reference to apply in battery-operated systems. Proposed circuits work in weak inverse region to replace the bipolar devices in conventional circuit and using proposed circuits realize CMOS voltage reference which does not change with temperature. Its power consumption only has several hundred nano-Watt and its area is only several hundred squre nanometer. In addition, the voltage derivation only has several dozens milli-Volt when temperature range is from -80℃ to 165℃. Therefore, proposed architectures can supply a stable voltage reference in battery-operated systems.

誌謝

本論文可以順利完成，首先要感謝我的指導教授闕河鳴博士，他指導我如何去完成本論文，很多該注意我沒注意的重點，教授都會仔細一步一步的告訴我該如何去做，適時給予我意見與正確的方向，我覺得老師教導我的不只是如何去完成一本論文的方法，而是去完成很多做事情的方法，這是我最受益良多的。

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最後，我要感謝我家人，沒有他們就沒有今天的我，還有我女朋友宛樺，她總是在精神上給予我最大的支持，不論遇到任何問題，她都會安慰我、鼓勵我，真的非常感謝。

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CHAPTER 1

Introduction

This chapter will introduce battery-operated system and illustrate motivation. Then, we show that voltage reference is an important circuit in analog circuits and voltage reference needs to become small-area and low-power.

1.1 Overview of Battery-Operated System

In recently these years, battery-operated systems are used widely. For example, cell phone, PDA, GPS, digital watch, notebook, etc, see Figure 1.1. Those give people convenient and support, and those machines will be more and more widespread. Therefore we know that battery-operated system is inseparable with the humanity. Because battery-operated system is already a trend, we should understand battery-operated system. Roughly, battery-operated system has fundamental characteristics which are battery-operated, small-area, portable, and multi-function. Beside, battery-operated systems have a very serious issue which is hot. Now, we will discuss every characteristics in the below parts individually.

1. Battery

Battery-operated systems use battery to supply it working. Battery-operated systems are requested to reach low-power, so the batteries can use longer and save more power. It is good for consumers, because no one want to bring a lot of batteries on body. Therefore designers should take the low power as the goal to design circuit architectures for battery-operated systems.

2. Portable Function

Portable function is convenient for people. Because people can bring powerful electronic products on body and use them anytime and anywhere. Therefore, electronic products want to have portable function, designers should notice that using small-area to design circuit architecture. Using small area and achieving high performance is already a trend at battery-operated systems.

Figure 1.1: Feature and Examples of Battery-Operated System

3. Multi-Function

Multi-function means that providing the most functions in a finite area. In other words, multi-function implies system integration and small area. It is very efficient to accomplish in battery-operated system. Therefore, we need to treasure every area by system integration and small circuit architectures which also request high performance.

4. Thermal Issue

Nowadays, battery-operated systems are quite small, and the situation will cause thermal issue. Because a lot of circuit architectures integrate in finite and small area, the heat will increase quickly and be not easy to radiate heat. Therefore battery-operated systems must need smart temperature sensors which can sense

temperature and admonish system. Smart temperature sensors need two voltages which are V_{PTAT} and V_{REF} to compare. And a stable V_{REF} is our goal at battery-operated system.

In the above introduction, we know that battery-operated systems have some key point which are low-power and small-area and need to solve thermal issue. In the next section, we will explain the motivation of voltage reference at battery-operated system.

1.2 Motivation

Voltage reference is a key element in many circuit architectures. For example, PLL, oscillator, data converter, voltage regulator, DRAM(Dynamic Random Access Menory), flash, and temperature sensor, etc. Those circuit architectures are important and conventional circuit architectures in analog systems. If those want to have high performance, they must need a stable voltage reference which is independent strongly with temperature, process variation, and supply voltage. Therefore, we should not ignore the importance of voltage reference.

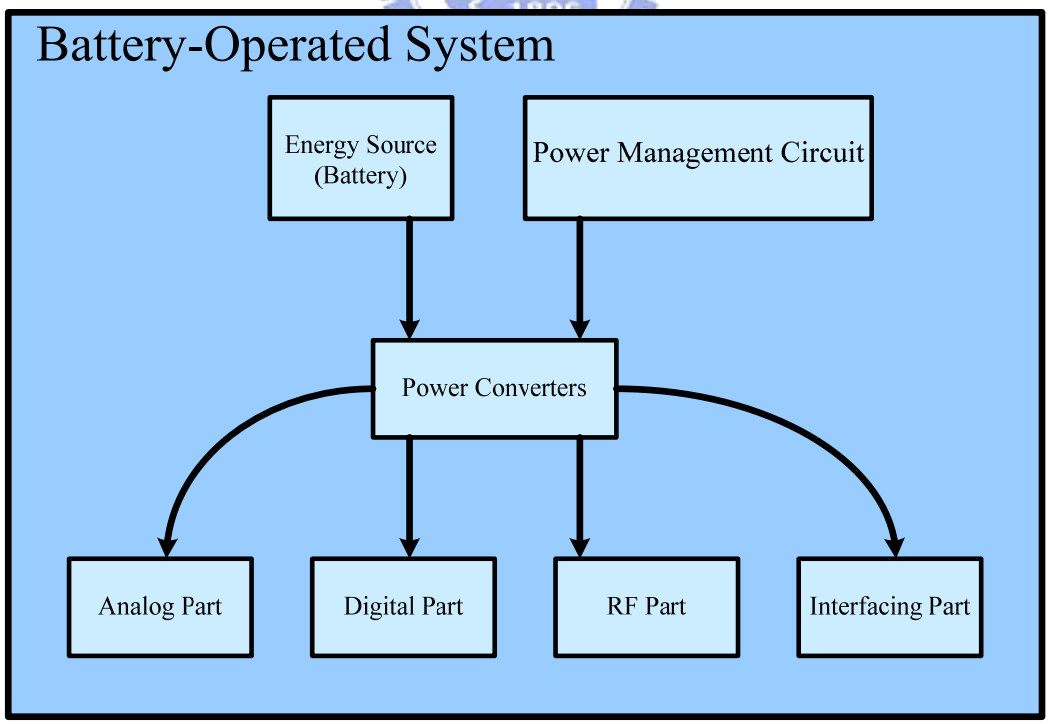


Figure 1.2: Block Diagram of Battery-Operated System

It is block diagram of battery-operated system in Figure 1.2. We can know that those above circuits are always used at analog part, power converter, and power management circuit. So, those circuits are designed in battery-operated system, they must need an adaptable voltage reference. It means that a low-power, small-area, and high performance voltage reference is needed in battery-operated systems.

1.3 Organization

Chapter 2 begins with introduction of conventional voltage reference, and three bandgap references are shown and discussed. Then bandgap reference and CMOS voltage reference are compared. Finally, we assort five voltage references of MOS and advance that voltage mode of V_{PTAT} and V_{CTAT} is as our excogitative architecture.

Chapter 3 shows that V_{CTAT} is produced by MOS transistor which works in subthreshold region and V_{PTAT} is produced by V_{CTAT}. Then proposed design architectures are implemented and described in detail. Comparison with proposed design architectures and researches is presented finally.

In Chapter 4, measured method and measurement environment are presented. Experimental results for the voltage references fabricated in a standard 0.18-μm CMOS technology are reported and discussed in this chapter.

The conclusions of this work are given in Chapter 5.

CHAPTER 2

Review of Voltage Reference

First, this chapter introduces general method of voltage reference. Conventional bandgap references are presented and illustrated. Comparison with bandgap reference and CMOS (Complementary MOS) voltage reference is shown after understanding conventional bandgap references. Then CMOS voltage reference is chosen because it is better than bandgap reference at our design goal. And, CMOS voltage reference is assorted five types at many researches. Finally, choosing voltage mode of V_{PTAT} and V_{CTAT} is the better adaptable design architecture of voltage reference.

2.1 Background

Nowadays, voltage reference has developed maturely. We can know how to produce voltage reference in many books and researches. And Figure 2.2.1 is block diagram of voltage reference which shows that a stable voltage is produced by two different voltages. In Figure 2.1.2, a traditional V_{REF} which does not change with temperature is added by V_{PTAT} and V_{CTAT}. If V_{PTAT} and V_{CTAT} are high linearity, V_{REF} will be a stable voltage. The method is suitable for voltage reference of BJT (Bipolar transistor) or MOS because V_{CTAT} can be produced easily by characteristic of BJT or MOS, and V_{PTAT} is produced by V_{CTAT}. Underside will show what V_{PTAT} and V_{CTAT} are?

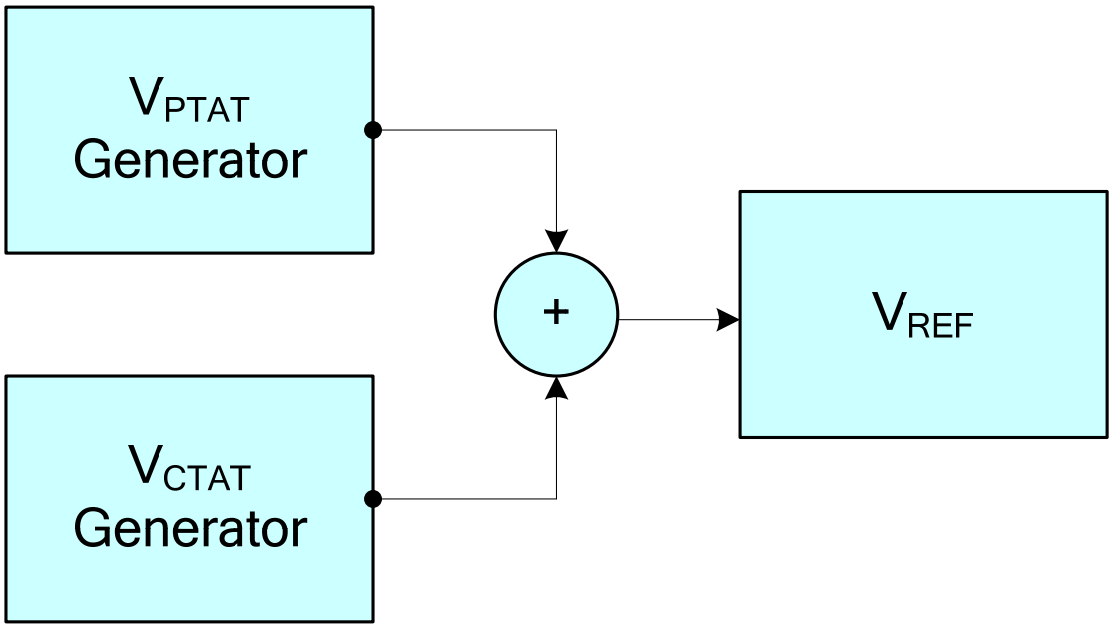


Figure 2.1.1: Block Diagram of Conventional Voltage Reference

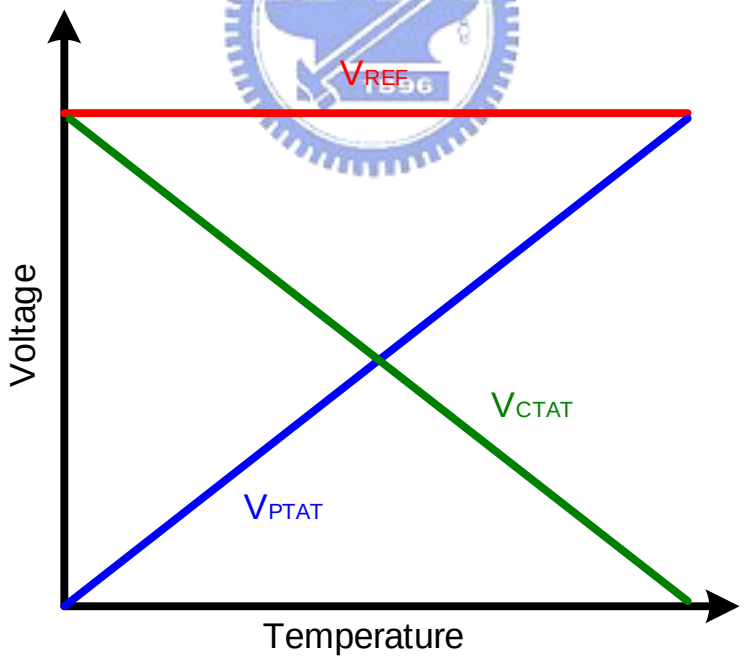


Figure 2.1.2: The Curvature of V_{REF} Formed by V_{PTAT} and V_{CTAT}

If analog circuits want to have a stable voltage reference, two important elements which are V_{PTAT} and V_{CTAT} are needed. CTAT is complementary to absolute temperature. It means that a voltage decreases with temperature. V_{CTAT} is used to compensate V_{PTAT}, so V_{REF} will not change with temperature. It is always produced by V_{BE} of BJT or V_{GS} of MOS which work in subthreshold region. In addition, V_{CTAT} is also used to produce V_{PTAT} by two different V_{CTAT} which subtract each other. Therefore, the linearity of V_{CTAT} is important at circuits of voltage reference.

PTAT is proportional to absolute temperature. It means that a voltage increases with temperature. The above paragraph has said that V_{PTAT} is always produced by two different V_{CTAT}. This is a significant issue how to reach high linearity of V_{PTAT} in circuits of voltage reference, because it will affect V_{REF} directly. V_{PTAT} is always used to another purpose which is as a compared voltage in smart temperature sensor. First stage of smart temperature sensor needs two voltages to compare, and the result is an authority of temperature difference which delivers to second stage of smart temperature sensor. Usually, V_{PTAT} is compared with V_{REF}. By this, smart temperature sensor can have an accurate temperature difference. But, premise is that smart temperature sensor needs high precise V_{REF} and V_{PTAT}.

After knowing the produced method of voltage reference, we need to notice three issues which relate very much to voltage reference. There are supply voltage variation, temperature variation, and process variation. If we can overcome the three issues, a stable voltage reference is produced.

The above principle is often used to produce voltage references, but the principle can derive many different circuits of voltage reference. The traditional voltage reference is designed by BJT, and it is called bandgap reference. In the next section, bandgap reference will be introduced and illustrated.

2.2 Conventional Bandgap Reference

This section will illustrate bandgap reference and show bandgap reference's architectures. Then a comparison with BJT and MOS is shown and explained. Finally, we choose MOS to design voltage reference because MOS is more suitable to apply in battery-operated system.

2.2.1 Bandgap Reference

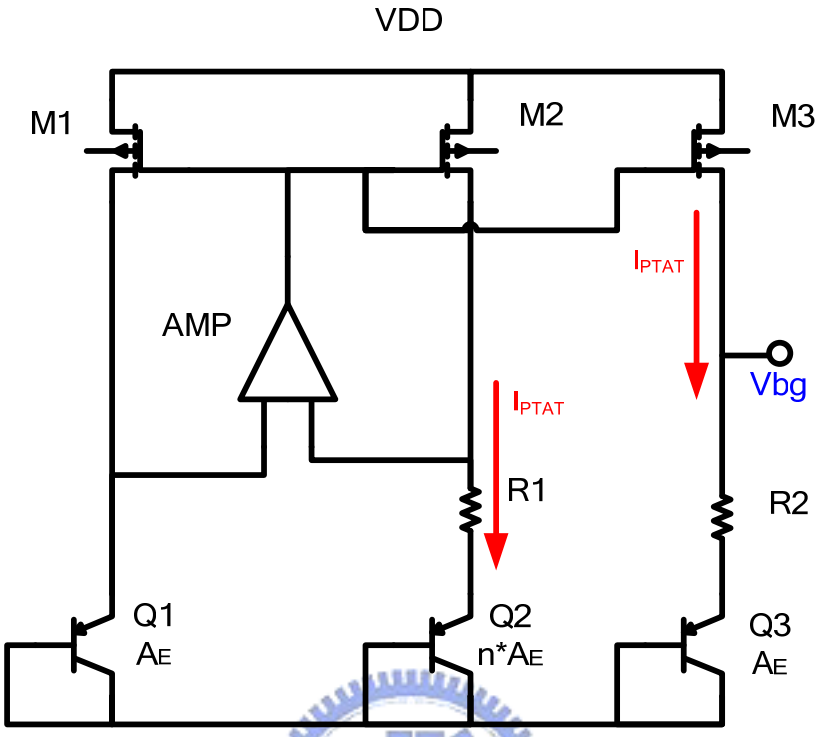


Figure 2.2.1: Conventional Bandgap Reference

In Figure 2.2.1, bandgap reference has been shown. M1~M2, Q1~Q2, and operational amplifier is used to produce I_{PTAT}. By mirroring from M2 to M3, we have the function which is shown as follows,

$$V_{bg} = V_{PTAT} + V_{CTAT} = \Delta V_{BE} + V_{BE} \tag{2-12}$$

$$\text{And} \quad \Delta V_{BE} = \frac{R_2}{R_1} V_T \ln(n) \tag{2-13}$$

$\triangle V_{BE}$ is a voltage of positive TC, and V_{BE} is a voltage of negative TC. Then, V_{REF} will be independent of temperature by adding $\triangle V_{BE}$ and V_{BE}.

After bandgap reference has been illustrated, we will be curious that the difference of voltage reference which use MOS or BJT to design. Why are researches of CMOS voltage reference more and more? What are they advantages and disadvantages? In the next section, we will compare CMOS voltage reference and

bandgap reference. Finding out the advantages and disadvantages of voltage references which are designed by MOS and BJT is very important. Why do we use MOS to design voltage reference, not BJT? The answer will explain afterward.

2.2.2 BJT and MOS comparison

We have understood bandgap reference how to produce in the above section. Now, the focus is that bandgap reference compares with CMOS voltage reference. We list some key points which more important when designing voltage reference. The comparison of voltage references which use MOS or BJT to design is shown in Table 2.1.

Table 2.1: The Comparison between MOS and BJT

	MOS	**BJT**
Advantages	1. V_{TH}=0.45V 2. Small area 3. V_{REF}<1.21V, low-voltage	1. Low process variation 2. Low supply voltage variation
Disadvantages	1. Process variation 2. Supply voltage variation	1. V_{BE}=0.6V 2. Large area 3. Vbg=1.21V

Let's see the advantages of MOS which are also the disadvantages of BJT. First, V_{TH} of MOS is lower than V_{BE} of BJT. We know that MOS operates in subthreshold region is like V_{BE} which is a voltage of negative TC. It means that V_{GS} has the inverse ratio with the temperature when $V_{GS} < V_{TH}$(about 0.45V in TSMC 0.18um process). Therefore, the same circuit architecture of voltage reference, MOS's supply voltage is lower than BJT's supply voltage. In the recent years, a lot of architectures are demanded for low-power, low-voltage, and small-area. The trend is ineluctability and more and more attention, and voltage reference is also following the trend. Therefore, CMOS voltage reference is more ascendant than bandgap reference in low-power architectures.

Second, area of MOS is smaller than area of BJT in the standard CMOS process and the same conditions. So area of voltage reference will decrease when using MOS to design it. The excellence is very useful to design in battery-operated system,

because battery-operated systems usually have some characteristics which are light, small, and portable. Therefore, MOS is easy to reach system integration and decrease the area.

Third, curvature compensation techniques are often used at bandgap reference. Because the linearity of V_{BE} is not very good at overall temperature range, it needs additional circuit which means curvature compensation techniques to compensate the linearity of V_{bg}. On the other hand, V_{TH} of MOS has superior linearity, and MOS does not need curvature compensation technique at wide temperature range. Therefore, the area of voltage reference circuit can be reduced. But, the performance is still good or even better.

Even if MOS has a lot of advantages which is very adaptable in battery-operated system, we still need to attend to process variation when we want to design CMOS voltage reference. Process variation of MOS is more serious than that of BJT, but it can be got over by every corner simulation. We need to run every corner and limit corners at an acceptive range when we simulate voltage reference.

In the above comparison, we know that MOS is better than BJT when designing voltage reference in battery-operated system, so we decide that using MOS to design voltage reference. Before design, we should review researches of MOS voltage reference in the recent six years. Because we can understand how to design CMOS voltage reference by reviewing researches. And it is important to find out advantages and disadvantages from every circuit architectures of voltage reference in researches. The introduction of CMOS voltage reference will be presented in the next section. In addition, we will compare five circuit architectures of voltage reference and choose the best adaptable architecture to discuss in depth.

2.3 CMOS Voltage References

Bandgap reference is a traditional voltage reference. It is formed by V_{BE} of BJT. V_{BE} is a voltage of negative temperature coefficient, and two different V_{BE} subtract to produce V_{PTAT} which is a voltage of positive temperature coefficient. So, a stable voltage reference which is not change with temperature, supply voltage, and process is produced by V_{PTAT} and V_{CTAT}. As the process advances, voltage references request more and more seriously for low power and small area. But, BJT is hard to accord

with the goal at the present age. Therefore, BJT was replaced by MOS when designing voltage reference. The source had been illustrated them in the above sections.

Near present year, someone discover MOS work in subthreshold region has a characteristic which is analogous to BJT. It means that V_{GS} of MOS which works in subthreshold region is a voltage of negative temperature coefficient. So voltage reference starts to use MOS. In the above sections, we know that MOS has two main advantages. First, it is low voltage, because V_{GS} is lower than V_{BE}. Second, MOS's area is small. Because having the two advantages, researches of CMOS voltage references are increasing in the recent six years.

In the recent six years, a lot of researches of CMOS voltage references are designed. CMOS can be assorted five types by those researches. The classified basis is produced method of voltage reference. All types have advantages and disadvantages by themselves. In the following sections, we will illustrate and discuss. Now, the five types are shown below.

1. **Voltage Mode of V_{PTAT} and V_{CTAT}:**
   CMOS voltage reference is produced by I_{PTAT} and $V_{CTAT}(V_{GS})$.

2. **Current Mode of V_{PTAT} and V_{CTAT}:**
   CMOS voltage reference is produced that I_{PTAT} and I_{CTAT}. I_{REF} multiplies resistor to produce V_{REF}.

3. **Voltage Reference Uses Parallel Voltages:**
   The circuit uses that two V_{GS} which have the same slope to subtract, then CMOS voltage reference is produced.

4. **Zero Temperature Coefficient Point (ZTC):**
   When MOS work at a fixed point, the V_{GS} and I_D will not change with temperature. The point is called zero temperature coefficient point. So V_{GS} can be designed as voltage reference.

5. **Voltage Reference Uses Non-standard Process:**
   CMOS voltage reference which does not use standard CMOS process technique is designed.

The five types will be showed in the below sections. In addition, I choose five researches to illustrate the five types and list the performance of five types. Then the comparison of researches will be shown and discussed. We will illustrate that voltage mode of VPTAT and VCTAT is more suitable than other architectures to design voltage reference in battery-operated system.

2.3.1 Voltage Mode of V_{PTAT} and V_{CTAT}

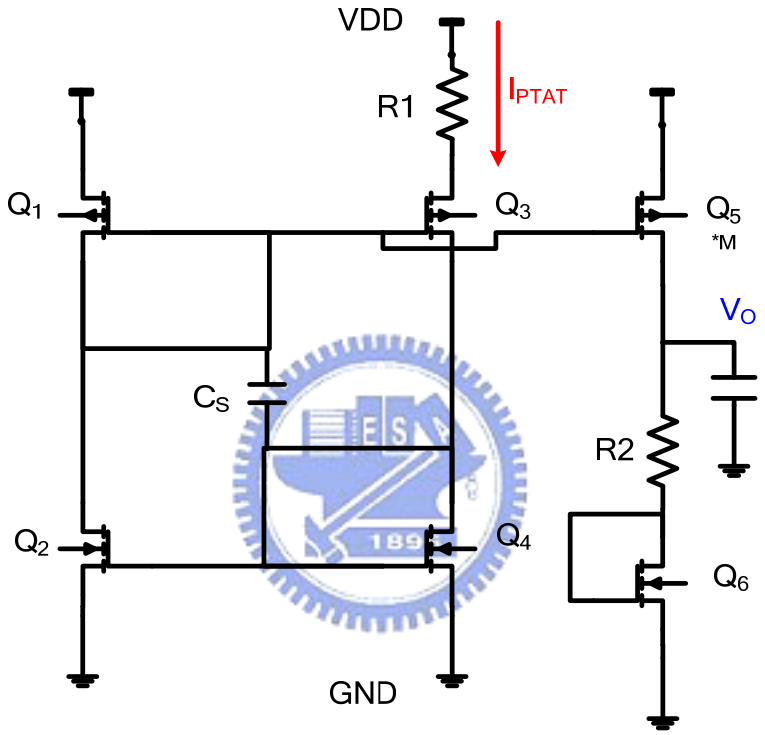


Figure 2.3.1: Circuit Architecture for Voltage Mode of V_{PTAT} and V_{CTAT} (REF[2])

In the last few years, CMOS voltage reference's circuits can work under 1V. But, those circuits present a high level of complexity. It may cause undesirable behavior and a high quiescent current. Consequently, efforts have been made to develop a simple circuit of voltage reference which has a power supply lower than the bandgap voltage.

The circuit refers to Ref [2]: A CMOS Voltage Reference Based on Threshold Voltage for Ultra Low-Voltage and Ultra Low-Power. It is assorted to voltage mode of V_{PTAT} and V_{CTAT}. Voltage reference uses only resistors and transistors working in weak inversion, without any bipolar transistors. The circuit was implemented in a standard

0.35μm TSMC CMOS process. V_{REF} is 514mV for a power supply of 900mV, and temperature coefficient is 39 ppm/℃ for temperature range from 0℃ to 100℃. (Ref: [2])

The derivative is as follows:

All MOS operate in subthreshold region, and the function is (2-14) (2-15),

$$I_{DS}(T) = I_S\left(\frac{W}{L}\right)\exp\left(\frac{V_{GS}(T)-V_{th}(T)}{n\left(\frac{kT}{q}\right)}\right) \tag{2-14}$$

$$V_{GS}(T) = V_{th}(T) + n\frac{kT}{q}\ln\left(\frac{I_{DS}(T)}{I_S\left(\frac{W}{L}\right)}\right) \tag{2-15}$$

Using two V_{GS} to produce $\triangle V_{GS}$ which is proportional to absolute temperature (PTAT), see (2-16),

$$\Delta V_{GS} = V_{GS1} - V_{GS3} = n\frac{kT}{q}\ln\left(\frac{\left(W/L\right)_3\left(W/L\right)_2}{\left(W/L\right)_1\left(W/L\right)_4}\right) \tag{2-16}$$

Deciding the slope of $\triangle V_{GS}$ is feasible by adjusting (W/L). And, we can know I_{PTAT} is $\triangle V_{GS}$ / R_1, see (2-17),

$$I_{PTAT} = \frac{\Delta V_{GS}}{R_1} \tag{2-17}$$

I_{Q5} is M*I_{PTAT}, beside V_{GS} is complementary to absolute temperature (CTAT). So, voltage reference (V_{REF}) is the function of (2-18),

$$V_{REF} = V_{GS6} + \frac{M * I_{PTAT}}{R_2}$$

$$V_{REF}(T) = V_{Q6}(T) + n\left(\frac{kT}{q}\right)\frac{R_2(T_0)\left(\frac{W}{L}\right)_5}{R_1(T_0)\left(\frac{W}{L}\right)_1}\ln\left[\frac{\left(\frac{W}{L}\right)_2\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_4\left(\frac{W}{L}\right)_1}\right] \quad (2\text{-}18)$$

The architecture of CMOS voltage reference has some advantages:

1. **Low power and low supply voltage:** All MOS operate in subthreshold region. The power and voltage will be very low.
2. **Small area:** Resistors of the above architecture occupies a half above area. If the resistors can be decreased or deleted, area will be very small. It is conform to design in battery-operated system.
3. **Simple:** It uses no curvature compensation technique, but it has high performance. The circuit has only three current paths, so the power can scale down.

Those advantages are very powerful help for designing voltage reference in battery-operated system. In Table 2.2, it shows researches for voltage mode of V_{PTAT} and V_{CTAT}. The power can scale down to several dozens nano-Amp and the area can reach μm^2. Under comparison, the performance certainly does not lose to bandgap reference.

Table 2.2: Researches for Voltage Mode of V_{PTAT} and V_{CTAT}

PAPER (year)	VDD (V)	Temperature Range (℃)	Temperature Coefficient (ppm/℃)	VREF (mV)	Tech. (μm)	AREA (mm^2)	PSRR (dB)	POWER (W)
Voltage Mode of V_{PTAT} and V_{CTAT}								
*[1] 2004	4.5~5	25~90	347	1320	0.18			
*[2] 2005	0.9	0~100	39	514	0.35	0.12	22	780n
*[3] 2005	2	0~70	62	579	0.35	0.126	84	4.6u
*[4] 2006	0.9~4	0~80	10	670	0.35	0.045	40	63n
[5] 2004	1.1~2.2	-10~70	85	504	0.18			176u
[6] 2005	3.3	0~150	26	711	0.35			
[7] 2006	1.3	-50~130	9	546	0.18		100	80u
[8] 2006	0.5	-40~100	2.2	319	0.13	0.0002	14	40n

2.3.2 Current Mode of V_{PTAT} and V_{CTAT}

The circuit refers to Ref [10]: A Simple Subthreshold CMOS Voltage Reference Circuit With Channel-Length Modulation Compensation. It is assorted to current mode of V_{PTAT} and V_{CTAT}. The circuit uses MOS works in subthreshold region to produce a reference voltage of 221mV at supply voltage of 0.85V. The power consumption has only 3.3μW at room temperature uses TSMC 0.18μm technology. The area of proposed circuit is less than 0.0238 mm^2, and the reference voltage variation is 2mV/V for supply voltage from 0.9 to 2.5V. Beside, the temperature variation is 6mV in the range from -20℃~120℃. (Ref: [10])

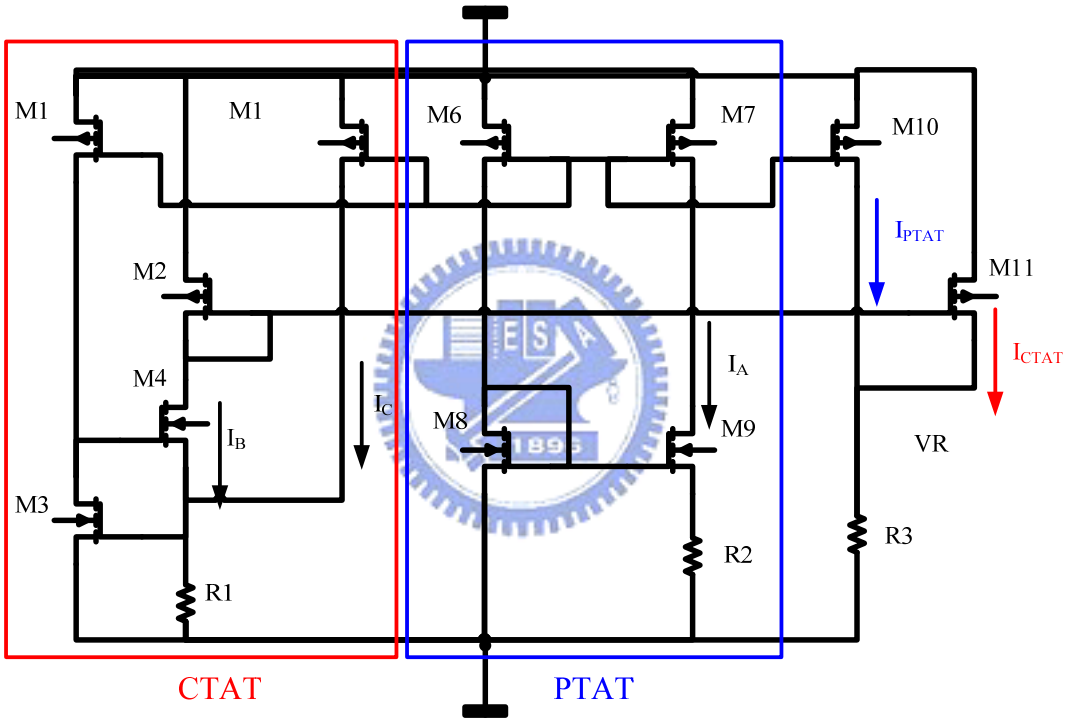


Figure 2.3.2: Circuit Architecture for Current Mode of VPTAT and VCTAT (REF[10])

The circuit is a typical current mode of V_{PTAT} and V_{CTAT}, and it is divided into three parts.

1. **CTAT part:** It is made of transistors M1 to M5 and resistor R1. To analyze the circuit, M3 operates in subthreshold region. V_{GS3} is negative-temperature voltage. So, we can know that (2-19).

$$I_B = {V_{GS3}}/{R_1} - I_C \tag{2-19}$$

I_C is used to compensate channel-length modulation. I_B is a current of negative-temperature coefficient, so I_{CTAT} is produced in this part.

2. **PTAT part:** A general I_{PTAT} generator is made of transistors M6 to M9 and resistor R2. Transistors M8 and M9 operate in subthreshold region, and the function is as follows : (2-20)

$$I_A = \frac{(V_{GS8} - V_{GS9})}{R_2} = \frac{\Delta V_{GS}}{R_2} \tag{2-20}$$

ΔV_{GS} is positive-temperature voltage, so I_A is positive-temperature current. Therefore I_{PTAT} is produced in the part.

3. **V_{REF} part:** Using transistors M10 to M11 and resistor R3, we can get $V_{REF.}$ The function of V_{REF} is as follows : (2-21)

$$V_{REF} = \left(\frac{(W/L)_{10}}{(W/L)_7} I_A + \frac{(W/L)_{11}}{(W/L)_2} I_B \right) * R_3 \tag{2-21}$$

Although, those circuit can be designed in low voltage architecture, but they always need resistors. It must cause big area, so it is not easy to accord with our goal which is design in battery-operated system. Besides, resistors have more variation in standard CMOS process. It may decrease the accuracy of voltage reference. Further, voltage reference is the currents to multiply the resistor. If V_{REF} needs a higher value, the currents and resistor must be large enough to reach the value. Therefore, power is hard to decrease.

In Table 2.3, it shows researches for current mode of V_{PTAT} and V_{CTAT}. We can discover that temperature coefficient of current mode is not better than voltage mode. Because current mode of V_{PTAT} and V_{CTAT} needs current mirror and resistors, they will cause deviation of voltage reference. Therefore, temperature coefficient is difficult to scale down. The power is hard to scale down, too. Those issues have been illustrated in the above section.

Table 2.3: Researches for Current Mode of V_{PTAT} and V_{CTAT}

PAPER (year)	VDD (V)	Temperature Range (℃)	Temperature Coefficient (ppm/℃)	VREF (mV)	Tech. (μm)	AREA (mm^2)	PSRR (dB)	POWER (W)
Current Mode of V_{PTAT} and V_{CTAT}								
*[9] 2003	1.2	-25~125	119	295	1.2	0.23	40	4.32u
*[10]2006	0.85	-20~120	194	221	0.18	0.0238		3.3u
[11] 2003	0.6	-40~100	93	400	0.13			
[12] 2003	1.5	-40~125	37.88	800	0.13			120u
[13] 2003	0.6~1.8	0~80	80	405	0.18	0.1	82	25u
[14] 2004	3~5	-60~100	4	1165.4	1.2	0.18		30u
[15] 2004	1	-20~80	200	400	0.35			3u
[16] 2004	0.8	0~100	33	592	0.6	0.05	50	0.88u
[17] 2005	1	-40~125	66.7	225	0.5			4u
[18] 2005	1.8	0~70	32.5	615.1	0.18	0.1	35	1.6u
[19] 2006	1.2	-20~90	61.64	718	0.09			1.6u
[20] 2006	0.8~2.6	-20~120	64.2	278	0.18	0.04		5.4u

2.3.3 Voltage Reference Uses Parallel Voltages

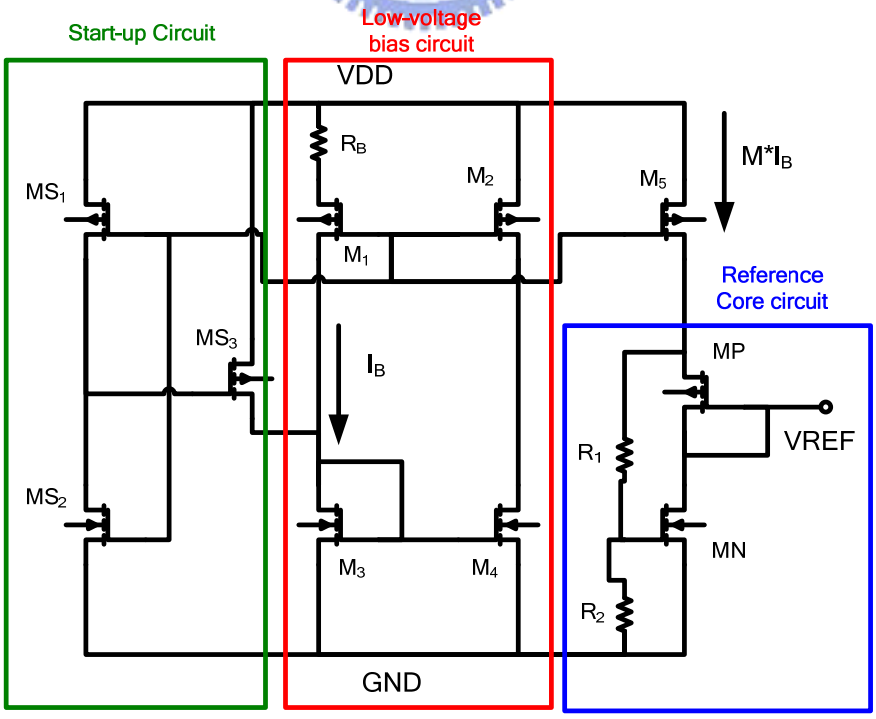


Figure 2.3.3: Circuit Architecture of Parallel Voltages (REF[21])

A voltage reference is necessary for LDO design, and it provides a low-supply-dependence and low-temperature-drift reference voltage to define the LDO output voltage. The circuit refers to Ref[21]: A CMOS Voltage Reference Based On Weighted △Vgs For CMOS Low-Dropout Linear Regulators. It is assorted to parallel voltages. A CMOS voltage reference been implemented in a standard 0.6μm CNOS technology. The area is 0.055mm^2, and the lowest supply voltage is 1.4V. A typical temperature coefficient is 36.9 ppm/℃. (Ref: [21])

The proposed CMOS voltage reference is based on the different temperature dependencies of the threshold voltages of an NMOS and a PMOS. See Fig 2.3.3, it can be divided into three parts.

1. **Start-up circuit:** It is formed by MS1-MS3. It uses to trigger this circuit, when the circuit operates in wrong state.
2. **Low-voltage bias circuit:** It is formed by M1-M4 and R_B. It provides a stable bias current.
3. **Reference core circuit:** It is formed by M5, MP, MN, R_1 and R_2. Its function of V_{REF} is showed as follows: (2-22)

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right) V_{GSn} - \left|V_{GSp}\right| \tag{2-22}$$

Using two parallel voltages which mean two V_{GS} to subtract is a method to produce voltage reference. But, the architecture has two disadvantages. First, two slopes of VGS is not parallel, because the two MOS is not in the same situation which means different V_{BS} and different MOS type. This will cause inexactitude voltage reference. See Table 2.4, we discover temperature coefficient of the architecture is not bad, but they almost do not have good temperature range. Second, these circuits have a disadvantage which is resistors. Because we need most current (M*I_B) run through MP and MN, resistors R_1 and R_2 must be large enough. This causes the resistor derivation to increase.

Table 2.4: Researches of Voltage Reference of Parallel Voltages

PAPER (year)	VDD (V)	Temperature Range (℃)	Temperature Coefficient (ppm/℃)	VREF (mV)	Tech. (μm)	AREA (mm^2)	PSRR (dB)	POWER (W)
Voltage Reference Uses Parallel Voltages								
*[21]2003	1.4	0~100	36.9	309	0.6	0.055	20	13.58u
*[22]2004	5	-10~80	32	2670	0.5	0.0936		970u
*[23]2005	1.5	0~80	25	168	0.35	0.08	59	3.6u
*[24]2006	1.5~4.3	0~80	12	891.1	0.35	0.015	59	300n
[25] 2005	0.6~1.8	0~75	70	332	0.18			
[26] 2006	0.9~3.3	-40~100	33	181	0.35			1.1u

2.3.4 Zero Temperature Coefficient Point (ZTC)

The circuit refers to Ref[27]: Mutual Compensation of Mobility and Threshold Voltage Temperature Effects with Applications in CMOS Circuits. It is assorted to ZTC. Mutual compensation of mobility and threshold voltage temperature variations may result in a ZTC (zero temperature coefficient) bias point of a MOS transistor. The circuit can be applied in voltage reference circuits and temperature sensors with linear dependence of voltage versus temperature. (Ref: [27])

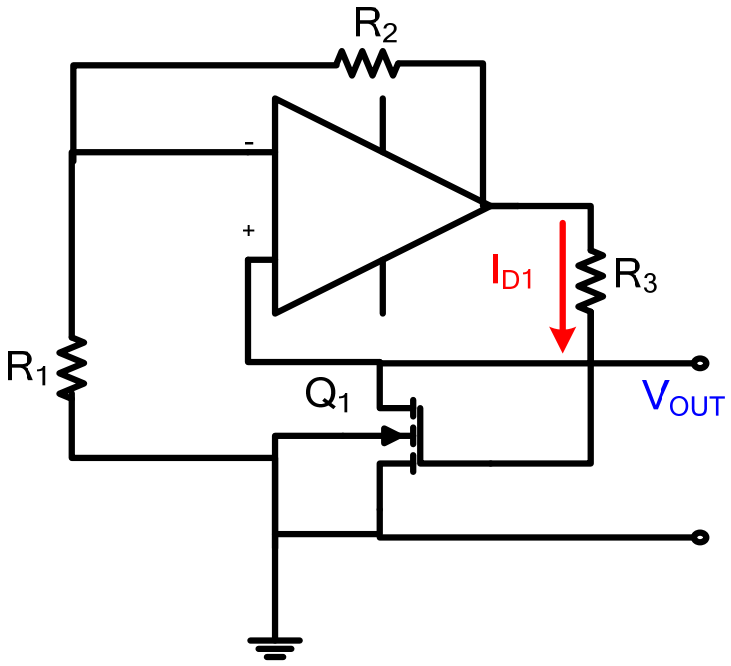


Figure 2.3.4: Circuit Architecture of ZTC (REF[26])

See Figure 2.3.4, Q1 operates on ZTC point. To use feedback to stabilize MOS Q1, so variations will decrease. In the circuit, for transistor Q1 the following design relationship should be satisfied

$$I_{D1} = I_{DF} = V_{GS1}\frac{R_2}{R_1 R_3} = V_{GSF}\frac{R_2}{R_1 R_3} \tag{2-23}$$

The values of I_{DF} = 192μA and V_{GSF} = 869mV were considered as the parameters of the ZTC bias point at $T=T_0$=300°K.

But ZTC has a problem that V_{REF} is hard to be designed in ultra low voltage. That is because MOS has no ZTC point in ultra low voltage. In Table 2.5, V_{REF} can't be lower than 600mV, even if supply voltage scales down 1V. Therefore, the architecture is hard to apply in battery-operated system.

Table 2.5: Researches of ZTC

PAPER (year)	VDD (V)	Temperature Range (℃)	Temperature Coefficient (ppm/℃)	VREF (mV)	Tech. (μm)	AREA (mm^2)	PSRR (dB)	POWER (W)
ZTC								
*[27]2001	3~3.3	-20~100	15	799	0.35	0.0204		
[28]2004	1	-50~150	4	640	0.18			
[29]2005	3.3	-50~120	50	821 1264	0.35			36.3u

2.3.5 Voltage Reference Uses Non-standard Process

The circuit refers to Ref [30]: CMOS Voltage Reference Based on Gate Work Function Differences in Poly-Si Controlled by Conductivity Type and Impurity Concentration. It is assorted to special process. A new CMOS reference circuit consisting of two pairs of transistors is presented. One pair exhibits a threshold voltage difference with a negative temperature coefficient, while the other exhibits a positive temperature coefficient. (Ref: [30])

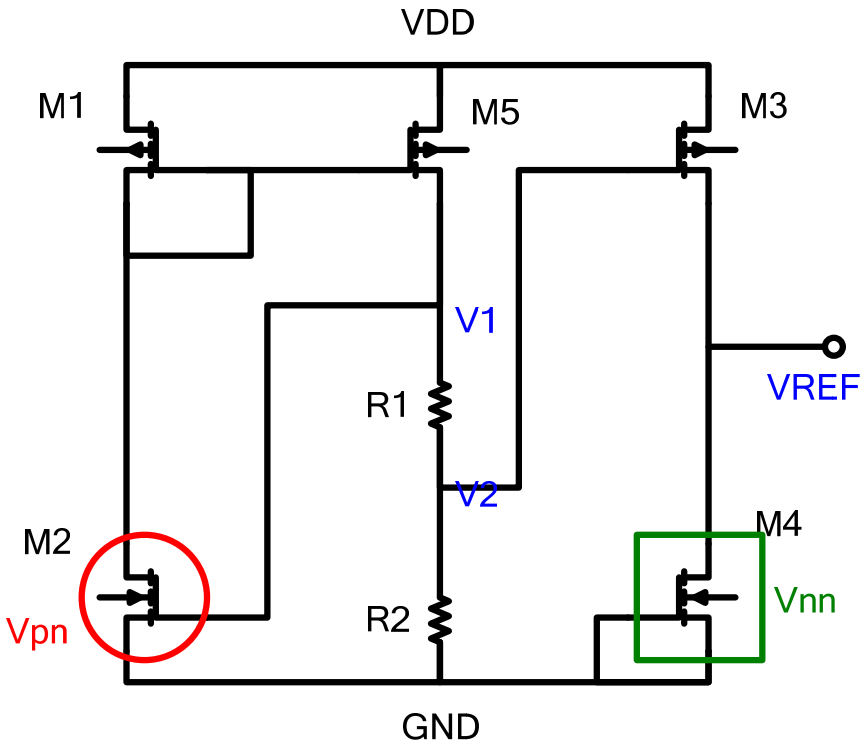


Figure 2.3.5: Circuit Architecture of Non-standard Process (REF[30])

For a pair of MOS transistors with gates of different conductivity types or different impurity concentrations, it will produce V_{PTAT} or V_{CTAT}, see Figure 2.3.6.

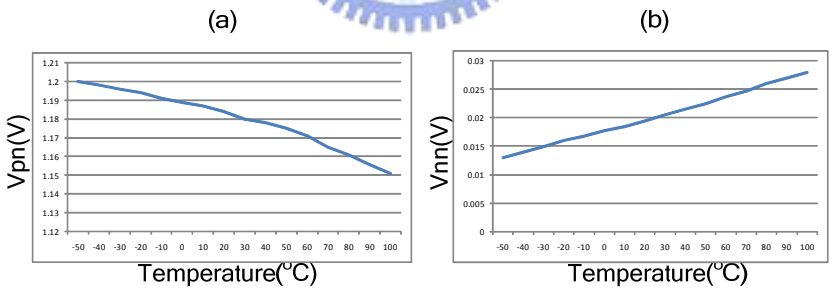


Figure 2.3.6: (a) Vpn and (b) Vnn as a Function of Temperature

In Figure 2.3.5, we can know

$$V_2 = \frac{R_2}{R_1 + R_2} V_1 = \frac{R_2}{R_1 + R_2} V_{pn} \,. \tag{2-24}$$

V_{pn} is V_{CTAT}, and V_{nn} is V_{PTAT}. V_{REF} can be shown

$$V_{REF} = V_{nn} + \frac{R_2}{R_1 + R_2} V_{pn} \quad (2\text{-}25)$$

We just adjust R_1 and R_2, so V_{REF} can be designed very well.

Although, special process needs not only standard CMOS process technique, so it may want to have special or additional process. This will cause more cost and resource, but we don't hope to see. In Table 2.6, it is researches of Non-standard Process. Some researches use floating-gate to design voltage reference, and it is also Non-standard Process.

Table 2.6: Researches of Voltage Reference of Non-standard Process

PAPER (year)	VDD (V)	Temperature Range (℃)	Temperature Coefficient (ppm/℃)	VREF (mV)	Tech. (μm)	AREA (mm^2)	PSRR (dB)	POWER (W)
Voltage Reference Uses Non-standard Process								
*[30]2003	1	-50~100	80	410				0.6u
*[31]2004	2.8~5.5	-20~100	54.6	0.8~1.5	0.5	0.081	80	500u
*[32]2005	4.5~9	-40~85	1	1250~5000	1.5	1.6	67	3.15u
*[33]2006	1.2	-60~140	130	400	0.35	0.0022		40u

2.3.6 Comparison of Voltage Reference

See Table 2.7, it is comparison of the above five circuit architectures. Our goal is to design voltage reference in battery-operated systems which demand low-power and small-area. Because there is no ZTC in ultra low voltage, ZTC architecture does not match with our goal. On the other hand, current mode of PTAT and CTAT architecture and parallel voltages architecture always need resistances which occupy the bigger area and cause more derivation, so they do not match our goal, too. Special process always needs additional process steps which will increase cost that we do not want to see.

Table 2.7: Comparison for Five Kinds of CMOS Voltage References

	Comparison
Voltage Mode of V_{PTAT} and V_{CTAT}	1. Can no resistor 2. Power arrives to nano-Watt
Current Mode of V_{PTAT} and V_{CTAT}	1. Resistor and current trade off
Voltage Reference Uses Parallel Voltages	1. Need resistors
ZTC	1. No ZTC in ultra low voltage
Voltage Reference Uses Non-standard Process	1. No apply in standard process

See Table 2.8, it is researches for CMOS voltage reference, and five circuit architectures has been assorted. We can discover that performance of voltage mode is better than performance of other architectures. First, temperature coefficient is low generally at voltage mode of V_{PTAT} and V_{CTAT}, and temperature range is wide enough. Second, power of voltage mode of V_{PTAT} and V_{CTAT} can scale down to several dozens nW. It is very beneficial to design voltage reference in battery-operated system. Third, small area is achieved at voltage mode of V_{PTAT} and V_{CTAT}. We can see that area is several hundred μm^2, and no other architectures are batter than voltage mode of V_{PTAT} and V_{CTAT}. Although, special process has the same small area, it needs additional process steps which will increase costs. Therefore, we don't consider special process.

Table 2.8: Researches for All CMOS Voltage Reference

PAPER (year)	**VDD (V)**	**Temperature Range (℃)**	**Temperature Coefficient (ppm/℃)**	**VREF (mV)**	**Tech. (μm)**	**AREA (mm^2)**	**PSRR (dB)**	**POWER (W)**
Voltage Mode of V_{PTAT} and V_{CTAT}					* is that research has experimental result			
*[1]2004	4.5~5	25~90	347	1320	0.18			
*[2]2005	0.9	0~100	39	514	0.35	0.12	22	780n
*[3]2005	2	0~70	62	579	0.35	0.126	84	4.6u
*[4]2006	0.9~4	0~80	10	670	0.35	0.045	40	63n
[5] 2004	1.1~2.2	-10~70	85	504	0.18			176u
[6] 2005	3.3	0~150	26	711	0.35			
[7] 2006	1.3	-50~130	9	546	0.18		100	80u
[8] 2006	0.5	-40~100	2.2	319	0.13	0.0002	14	40n

Current Mode of V_{PTAT} and V_{CTAT}								
*[9]2003	1.2	-25~125	119	295	1.2	0.23	40	4.32u
*[10]2006	0.85	-20~120	194	221	0.18	0.0238		3.3u
[11] 2003	0.6	-40~100	93	400	0.13			
[12] 2003	1.5	-40~125	37.88	800	0.13			120u
[13] 2003	0.6~1.8	0~80	80	405	0.18	0.1	82	25u
[14] 2004	3~5	-60~100	4	1165.4	1.2	0.18		30u
[15] 2004	1	-20~80	200	400	0.35			3u
[16] 2004	0.8	0~100	33	592	0.6	0.05	50	0.88u
[17] 2005	1	-40~125	66.7	225	0.5			4u
[18] 2005	1.8	0~70	32.5	615.1	0.18	0.1	35	1.6u
[19] 2006	1.2	-20~90	61.64	718	0.09			1.6u
[20] 2006	0.8~2.6	-20~120	64.2	278	0.18	0.04		5.4u
Voltage Reference Uses Parallel Voltages								
*[21]2003	1.4	0~100	36.9	309	0.6	0.055	20	13.58u
*[22]2004	5	-10~80	32	2670	0.5	0.0936		970u
*[23]2005	1.5	0~80	25	168	0.35	0.08	59	3.6u
*[24]2006	1.5~4.3	0~80	12	891.1	0.35	0.015	59	300n
[25] 2005	0.6~1.8	0~75	70	332	0.18			
[26] 2006	0.9~3.3	-40~100	33	181	0.35			1.1u
ZTC								
*[27]2001	3~3.3	-20~100	15	799	0.35	0.0204		
[28] 2004	1	-50~150	4	640	0.18			
[29] 2005	3.3	-50~120	50	821 1264	0.35			36.3u
Voltage Reference Uses Non-standard Process								
*[30]2003	1	-50~100	80	410				0.6u
*[31]2004	2.8~5.5	-20~100	54.6	0.8~1.5	0.5	0.081	80	500u
*[32]2005	4.5~9	-40~85	1	1250~5000	1.5	1.6	67	3.15u
*[33]2006	1.2	-60~140	130	400	0.35	0.0022		40u

In researches for voltage mode of V_{PTAT} and V_{CTAT}, Ref [2] is good to discuss in depth, because it has several characteristics.

1. **Low power:** In researches for voltage mode of V_{PTAT} and V_{CTAT}, Ref[2] is sole circuit architecture at which all MOS work in subthreshold region. It is very worth to investigate in depth, because MOS work in subthreshold region can reach the least power consumption.

2. **Small area:** The area of circuit architecture which is Ref[2] is (400*300)μm^2, and we find that resistors occupy a lot of area. Therefore, we try to delete the resistors, and we will save very big area to reach the goal of small area.
3. **Simple:** Circuit architectures will demand simple and high performance in the future. Simple doesn't produce needless performance which effect accuracy, and simple circuit can decrease power consumption.

Choosing voltage mode of V_{PTAT} and V_{CTAT} architecture as our design architecture is possible to implement our goal. Because of no resistances, the area can diminish largely and decrease resistor's error. Besides, MOS which works in subthreshold region is adaptable to design in low-power architectures.

2.3.7 Summary

In this chapter, we know that voltage references are produced by V_{PTAT} and V_{CTAT}. Introducing bandgap references, and comparing BJT and MOS. Making sure that MOS is better than BJT under our requests. Afterward we introduce five architectures of voltage references and understand how they work. Finally, comparison is shown in the last section. After comparison, we choose voltage mode of V_{PTAT} and V_{CTAT} as our design architecture.

In the next chapter, two propose design architectures will be shown carefully. We will introduce principle, derivation, and simulation gradually, and my propose architectures compare with researches which is presented in the recent six years.

CHAPTER 3

Circuitry Architecture

In this chapter, proposed architectures will be shown and implemented. Before this, we should define specification explicitly. At least, proposed design can work in battery-operated system, and it still has high performance. Then, we start to find out V_{CTAT} which must be produced by MOS, and using V_{CTAT} produces V_{PTAT} if it could be implemented. When having V_{CTAT} and V_{PTAT}, we can design voltage reference stage by stage. Two proposed architectures will be shown and simulated, and we discuss their advantages and problems. Finally, two proposed architectures compare to researches, and explain that proposed architectures are better then researches in the recent six years.

3.1 Design Process

First, we introduce two papers, and those are source of my proposed architectures. So we need to understand the two reference papers step by step. Then we will be clear to know how proposed architectures are designed.

3.1.1 Reference Paper

In Figure 3.1.1, all MOS work in subthreshold region, so V_{GS} is V_{CTAT}. See M8, V_{G8} is V_{DD} and V_{GS8} is V_{CTAT}, so we can know that V_{S8} will be V_{PTAT}. But the current which pass through M7 and M8 changes V_{GS8} by the current function, so V_{S8} becomes V_{REF}. We can design the bias circuit which produces V_{PTAT} by this principle. In next section, the bias circuit will be presented and illustrated.

$$V_{PTAT} = V_{DD} - V_{CTAT} \tag{3-1}$$

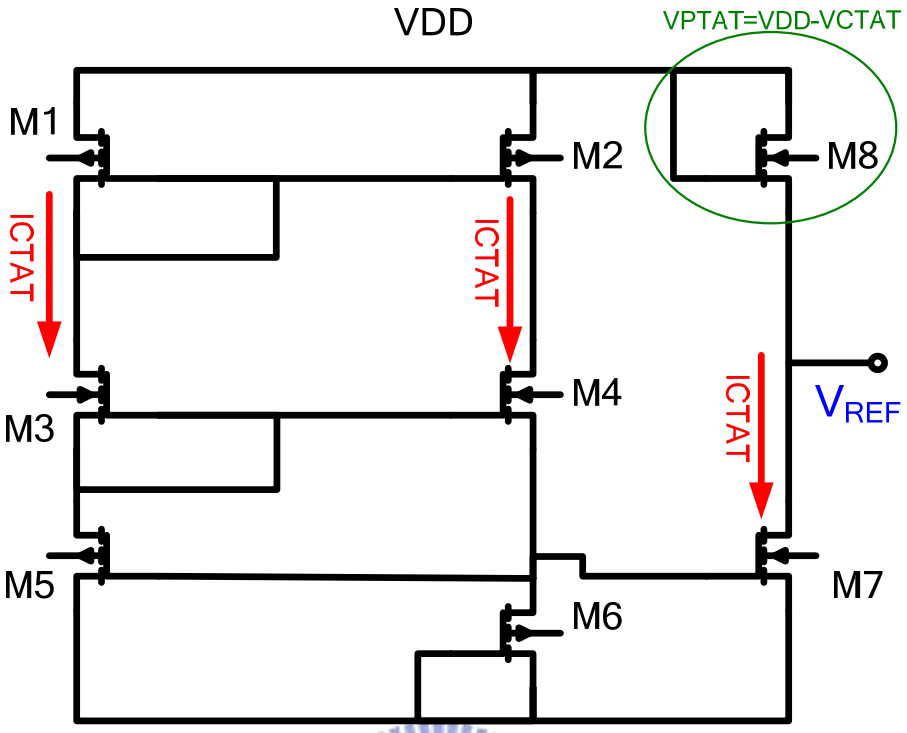


Figure 3.1.1: Circuit Architecture of REF[8]

3.1.2 V_{PTAT} (Proportional to Absolute Temperature)

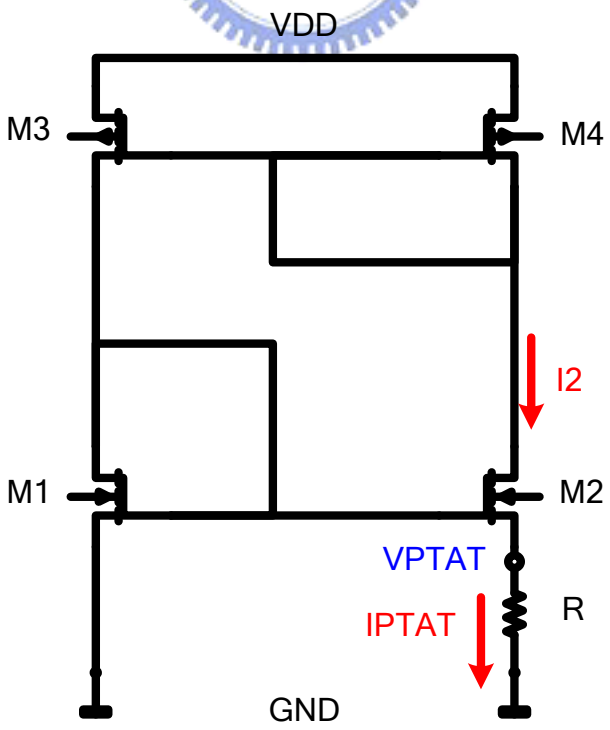


Figure 3.1.2: Conventional V_{PTAT} Circuit Architecture

The conventional method which produces V_{PTAT} is shown Figure 3.1.2. The circuit composes of four MOS (M1~M4) and a resistor (R). M1 and M2 work in subthreshold region, and M3 and M4 work in saturation region. R is stable value which doesn't change with temperature. The derivation is as follows:
Because M1 and M2 work in subthreshold region, the function is (3-2)

$$V_{GS}(T) = V_{th}(T) + n\frac{kT}{q}\ln\left(\frac{I_{DS}(T)}{I_S\left(\frac{W}{L}\right)}\right) \tag{3-2}$$

,and $V_{GS1} = V_{GS2} + V_{PTAT}$ (3-3)

Using (3-2) into (3-3) can be shown as follows:

$$V_{TH}(T) + n\frac{kT}{q}\ln\left[\frac{I_{DS1}(T)}{I_S\left(\frac{W}{L}\right)_1}\right] = V_{TH}(T) + n\frac{kT}{q}\ln\left[\frac{I_{DS2}(T)}{I_S\left(\frac{W}{L}\right)_2}\right] + V_{PTAT} \tag{3-4}$$

,then we get the function of (3-5)

$$V_{PTAT} = n\frac{kT}{q}\ln\left[\frac{I_{DS1}}{I_{DS2}}\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\right] \tag{3-5}$$

$I_{DS1} : I_{DS2} = I_{DS3} : I_{DS4}$, so $\left(\frac{W}{L}\right)_1 : \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 : \left(\frac{W}{L}\right)_4$

The function of (3-5) can be written as (3-6)

$$V_{PTAT} = n\frac{kT}{q}\ln\left[\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_4}\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\right] \quad (3\text{-}6)$$

Because $\ln\left[\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_4}\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\right]$ is a positive value, V_{PTAT} is in positive proportion to temperature. And $V_{PTAT}=I_2*R$, we can know that $I_2=I_{PTAT}$. Therefore, we get V_{PTAT} and I_{PTAT}.

Although, the circuit is better than bandgap reference. But, it has some disadvantages. First, supply voltage is difficult below 1V. The minimum V_{DD} = V_{GS4}(saturation) + V_{GS1}(subthreshold) + V_{PTAT}, and $V_{GS4} > V_{TH}$, $V_{GS1} < V_{TH}$, V_{PTAT} should have a value. V_{TH} is about 0.45V at TSMC 0.18μm process. Therefore, we can know that supply voltage will be more 1V. Second, resistor must be used, and it will cause additional inaccuracy and more area. Because V_{PTAT} must reach a fixed value, the R and I_{PTAT} should large enough. It means that area and power must choose one. In addition, someone change resistor to MOS which work in triode region as a resistor. Indeed, the method could decrease a lot of area. But the method needs additional circuits, the power is possible to increase. So, I propose a simple circuit to solve those problems. I will explain proposed circuit of V_{PTAT} in the next section.

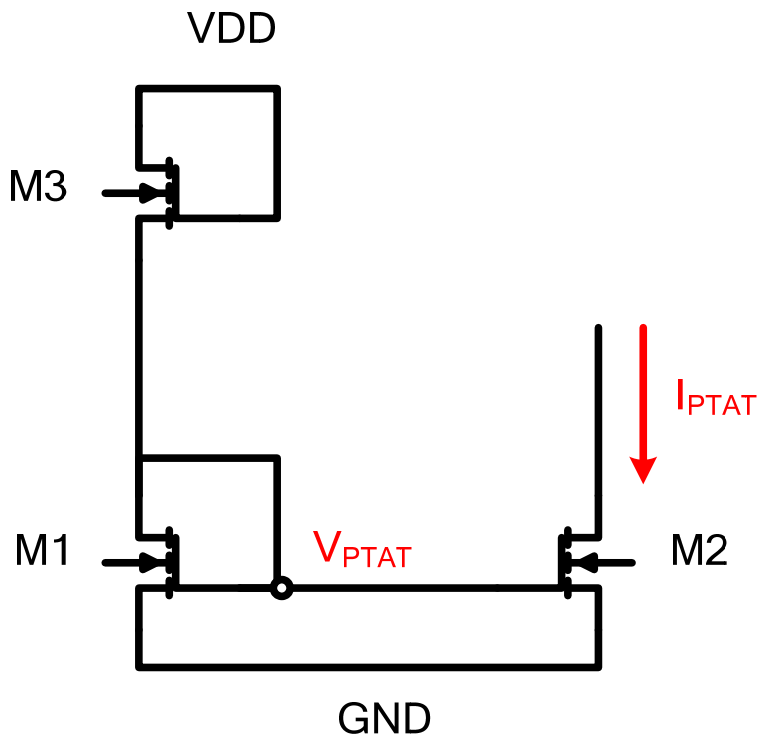


Figure 3.1.3: The V_{PTAT} Proposed Architecture

See Figure 3.1.3, it is proposed circuit of V_{PTAT}. The circuit is composed of three NMOS (M1~M3). All MOS work in subthreshold region, so V_{GS} is V_{CTAT} which is a voltage of negative temperature coefficient. And, V_{DD} is a stable value. Therefore, V_{PTAT} is as follows:

$$V_{PTAT} = V_{GS1} = V_{DD} - V_{CTAT} = V_{DD} - V_{GS3} \quad (3\text{-}7)$$

V_{PTAT} is gotten by two MOS which work in subthreshold region. The supply voltage of proposed circuit can be lower than 1V because it stacks two MOS which are about 0.8V. And, the area of proposed circuit is very small because it has only two MOS. So, the proposed circuit could have advantages of both small area and low supply voltage.

In the next section, the two proposed circuit of voltage reference is shown. We will discuss principle, derivation, simulation, and problem. The relationship of proposed architectures will be illustrated.

3.2 All NMOSFET Voltage Reference (ANVR)

When we present new bias-circuit, the first proposed architecture can be shown. Its abbreviation is ANVR which means All NMOSFET Voltage Reference. The proposed architecture will introduce principle, derivation, and simulation in the next section.

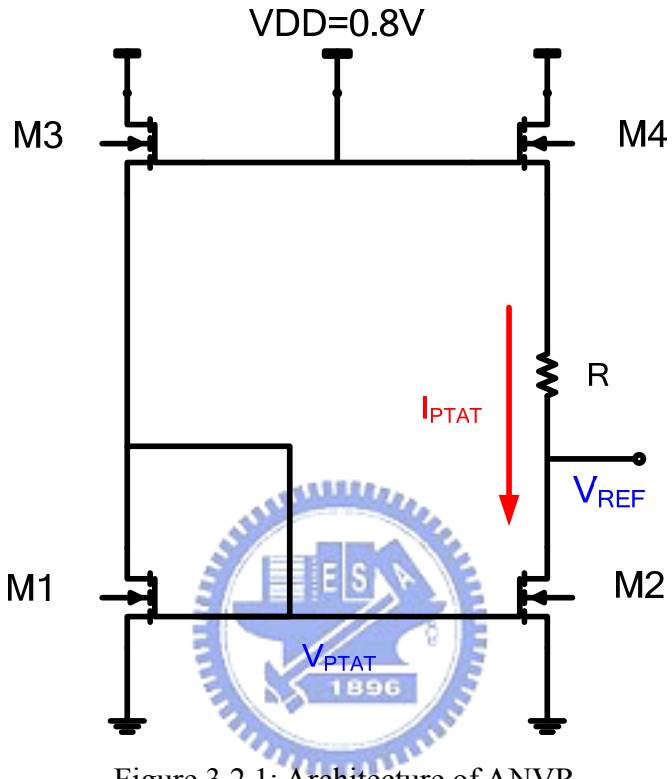


Figure 3.2.1: Architecture of ANVR

	M1	M2	M3	M4	R(ohm)
W(μm)	0.5	0.5	0.9	0.9	4.976k
L(μm)	0.6	0.6	0.6	0.6	
m	6	6	6	6	

3.2.1 Principle of ANVR

See Figure 3.2.1, the proposed architecture is composed of four NMOS (M1~M4) and one resistor. All MOS work in subthreshold region. M1 and M3 are V_{PTAT} produced circuit which has been introduced in the above section, and it produces a stable V_{PTAT} to mirror to next stage. M2 and M4 are V_{REF} produced circuit. We use V_{GS4} to be V_{CTAT}, and I_{PTAT} multiple R to produce V_{PTAT}. Then, V_{CTAT} and V_{PTAT} trade

off. By this, a stable V_{REF} will be produced. Because we hope that ANVR can operate under 1V, we choose V_{TH} of MOS around 0.48V. Besides, we hope that proposed architecture's power can be lower than the power of PAPER [2]. Therefore, we decide that supply voltage is 0.8V and total current is about 500nA. The each current of ANVR is 250nA which is the same current at the architecture of PAPER [2]. Finally, we can know the size of MOS and the derivation can be shown in the next section.

3.2.2 Derivation of ANVR

The section will derivate V_{REF} and illustrate every parameters. First, bias-circuit derivation is shown, and V_{REF}-circuit derivation will be shown by bias-circuit derivation later. Therefore we can decide (W/L) and resistor by the derivation.

A. Bias-circuit derivation

First, the function of V_{GS1} is shown as

$$V_{GS1}(T) = V_{DD} - V_{GS3}(T) \tag{3-8}$$

Using the current function of MOS works in weak inversion, the function of (3-8) can be written as

$$\begin{aligned} V_{GS1} &= V_{DD} - \left\{ V_{th3}(T) + nV_T \ln\left[\frac{I_{D3}(T)}{I_S P_3} \right] \right\} \\ &= V_{DD} - \left\{ V_{th3}(T) + nV_T \ln\left[\frac{P_1}{P_3} \right] + V_{GS1}(T) - V_{th1}(T) \right\} \end{aligned} \tag{3-9}$$

P is (W/L), V_T is thermal voltage, and n is subthreshold slope factor. The function of (3-9) become as

$$V_{GS1}(T) = \frac{1}{2} V_{DD} - \frac{1}{2} nV_T \ln\left[\frac{P_1}{P_3} \right] - \frac{1}{2} \left[V_{th1}(T) - V_{th3}(T) \right] \tag{3-10}$$

Therefore the bias-circuit derivation is done, and V_{GS1} will be used latter.

B. V_{REF}-circuit derivation

V_{REF} can be written as the function

$$V_{REF} = V_{DD} - \left[V_{GS4}(T) + I_{D2}(T) \times R\right] \tag{3-11}$$

Using the current function of MOS works in weak inversion, the function of (3-11) can be written as

$$\begin{aligned} V_{REF} &= V_{DD} - \left[V_{th4}(T) + nV_T \ln\left[\frac{I_{D2}(T)}{I_S P_4}\right] + I_{D2}(T) \times R \right] \\ &= V_{DD} - \left[V_{th4}(T) + nV_T \ln\left[\frac{I_S P_2 \exp\left[\frac{V_{GS2}(T) - V_{th2}(T)}{nV_T}\right]}{I_S P_4}\right] + I_{D2}(T) \times R \right] \\ &= V_{DD} - \left[nV_T \ln\left[\frac{P_2}{P_4}\right] + V_{GS2}(T) + I_{D2}(T) \times R + V_{th4}(T) - V_{th2}(T) \right] \end{aligned} \tag{3-12}$$

the function of (3-12) can become as (3-13) by the function of (3-10)

$$\begin{aligned} V_{REF} &= V_{DD} - \left[nV_T \ln\left[\frac{P_2}{P_4}\right] + \left\{ \frac{1}{2}V_{DD} - \frac{1}{2}nV_T \ln\left[\frac{P_1}{P_3}\right] - \frac{1}{2}\left[V_{th1}(T) - V_{th3}(T)\right] \right\} + I_{D2}(T) \times R + V_{th4}(T) - V_{th2}(T) \right] \\ &= \frac{1}{2}V_{DD} - nV_T \ln\left[\frac{P_2}{P_4}\right] + \frac{1}{2}nV_T \ln\left[\frac{P_1}{P_3}\right] - I_{D2}(T) \times R + \frac{1}{2}V_{th1}(T) - \frac{1}{2}V_{th3}(T) - V_{th4}(T) + V_{th2}(T) \end{aligned} \tag{3-13}$$

If we want V_{REF} which does not change with temperature, dV_{REF}/dT should be zero.

$$\frac{dV_{REF}}{dT} = n\frac{k}{q}\ln\left\{\left[\frac{P_4}{P_2}\right] \times \left[\frac{P_1}{P_3}\right]^{1/2}\right\} - R\frac{dI_{D2}(T)}{dT} + \frac{1}{2}\left[\frac{dV_{th1}(T)}{dT} - \frac{dV_{th3}(T)}{dT}\right] + \left[\frac{dV_{th2}(T)}{dT} - \frac{dV_{th4}(T)}{dT}\right] = 0 \tag{3-14}$$

n is subthreshold slope factor , P is (W/L), and $k/q = 8.6 \times 10^{-5}\ ev/K$. The function of $V_{TH}(T)$ is shown as

$$V_{th}(T) = V_{th}(T_0) + (KT1 + KT2 \times V_{bs})\left(\frac{T}{T_0} - 1\right) \quad (3\text{-}15)$$

And its differentiation is written as

$$\frac{dV_{th}(T)}{dT} = (KT1 + KT2 \times V_{bs}) \quad (3\text{-}16)$$

KT1 is temperature coefficient of the threshold voltage and KT2 is bulk-bias coefficient of the threshold voltage's temperature dependence. $dV_{TH}(T)/dT$ can been decided when (W/L) had been decided. Therefore, $dV_{REF}(T)/dT$ can be zero by designing P_1~P_4. When we decide the power, the current will be decided. Then, (W/L) is decided by the current. Finally, resistor can be chosen.

ANVR has many advantages. First, all MOS are NMOS. This method saves a lot area, because we don't use the area of PMOS. Second, supply voltage is 0.8V which reaches below 1V. The circuit has only two NMOS to stack, and MOS work in subthreshold region which means $V_{TH} < 0.45V$. Therefore, we can decrease much power in the proposed architecture. Third, the performance is not bad, and it will be shown in next section.

3.2.3 Post-Layout Simulation of ANVR

The layout of ANVR is shown in Figure 3.2.3. ANVR uses no PMOS, so the layout does not need PMOS region. It is good to decrease area. M1 and M2 are alternate permutation, so it can decrease mismatch. I_{PTAT} will mirror to M2 very well. Because a resistor has larger derivation, we divide a resistor into eight resistors. The method can decrease resistor derivation. In addition, dummy technique has been used in the layout, and it is also used to decrease process variation. Figure 3.2.2 shows presim of ANVR, and we can compare with Figure 3.2.3 which shows postsim of ANVR. They are almost the same.

The post-layout simulation is shown in Table 3.3. The five corners are shown from Figure 3.2.4 to Figure 3.2.8, and all corners are shown in Table 3.4. Those figures are curve of V_{REF} and temperature, and temperature range is wide enough to

reach -80℃~165℃. The inaccuracy is only ±1.5mV at Figure 3.2.3 when the corner is TT and TT_RES. In Table 3.3, temperature coefficient is lower than 166ppm/℃ in the worst case when temperature range is -80℃~165℃. We try to adjust the corners of proposed architecture, so temperature coefficient of the worst case can lower than 200 ppm/℃.

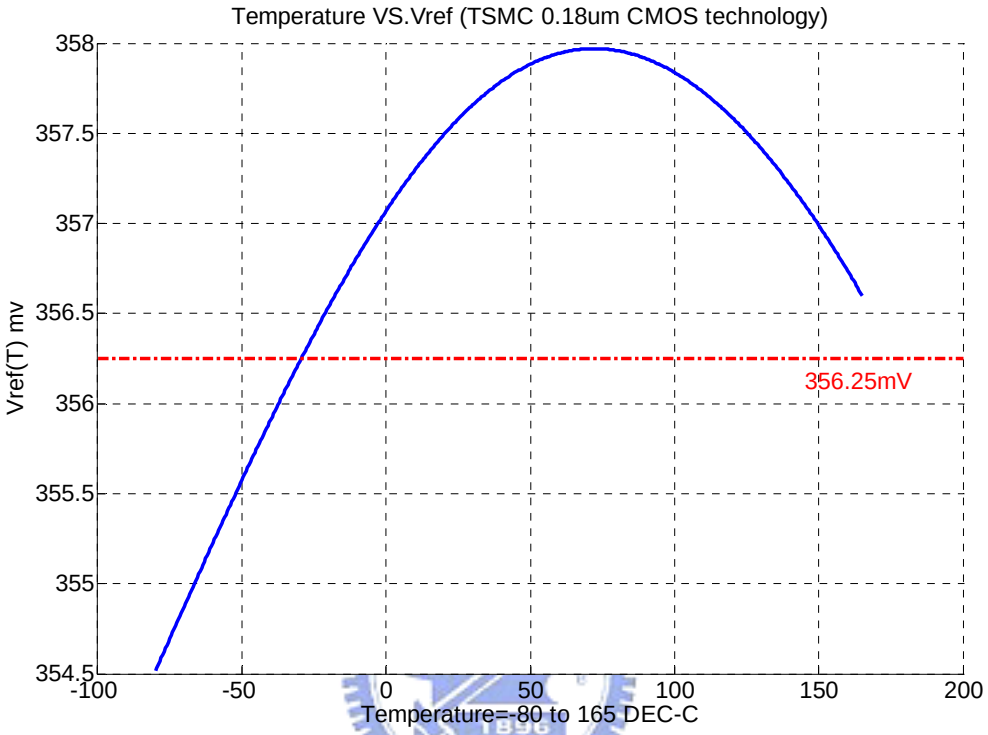


Figure 3.2.2: Presim of ANVR

Table 3.1: Post-Layout Simulation of ANVR

PAPER (year)	VDD (V)	Temperature Range (℃)	Temperature Coefficient (ppm/℃)	VREF (mV)	Tech. (μm)	AREA (mm^2)	PSRR (dB)	POWER (W)
ANVR (TT,TT_RES)	0.8	-80~165 -40~125 0~100	34.4 27.7 16.7	356 356.7 356.7	0.18	0.00108 (30*36)μm^2	7.5 @100kHz	403.2n

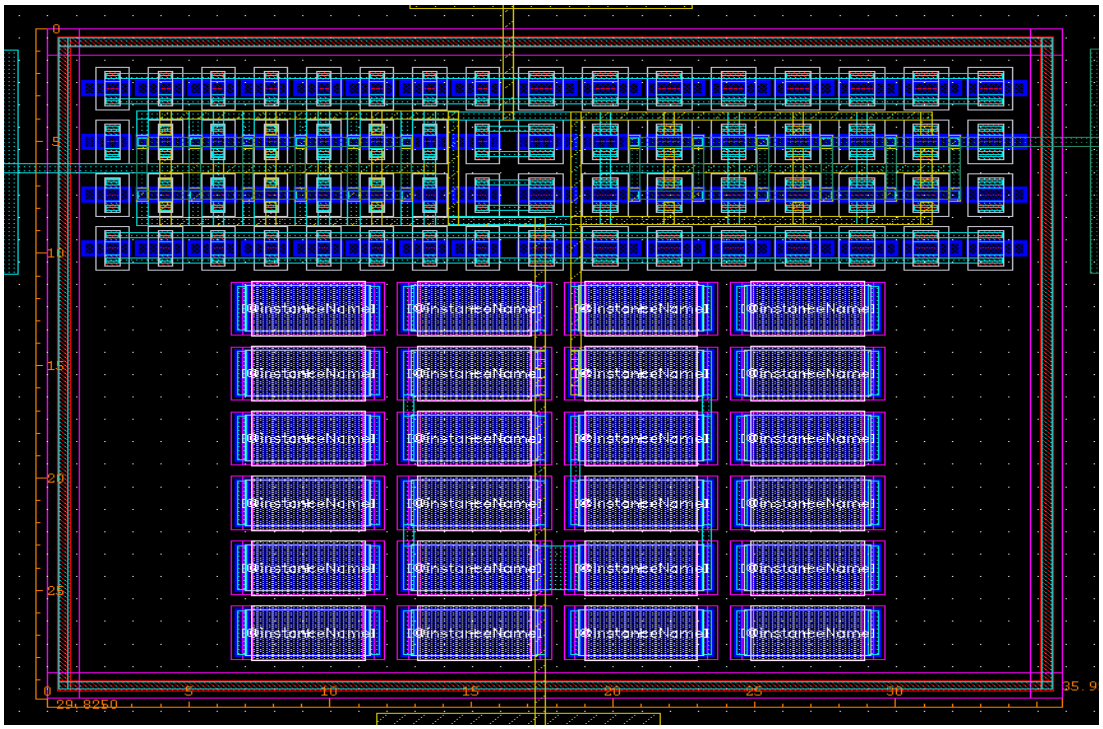


Figure 3.2.3: Layout of ANVR in TSMC 0.18um CMOS Technique

A. Post-Layout Simulation Results (V_{REF}):

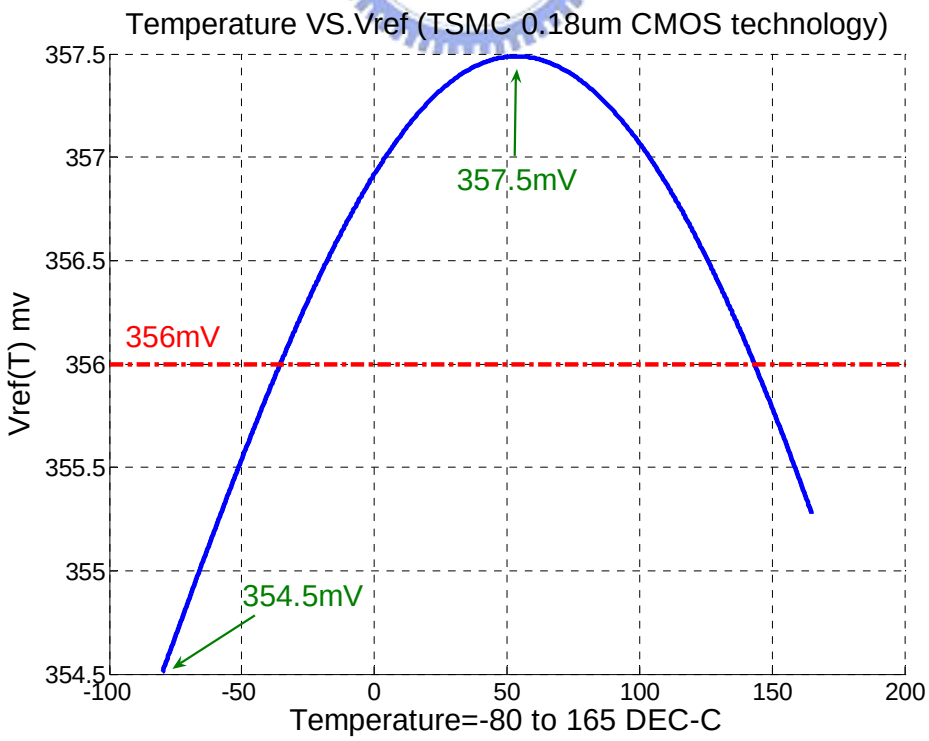


Figure 3.2.4: TT TT_RES Corner of ANVR

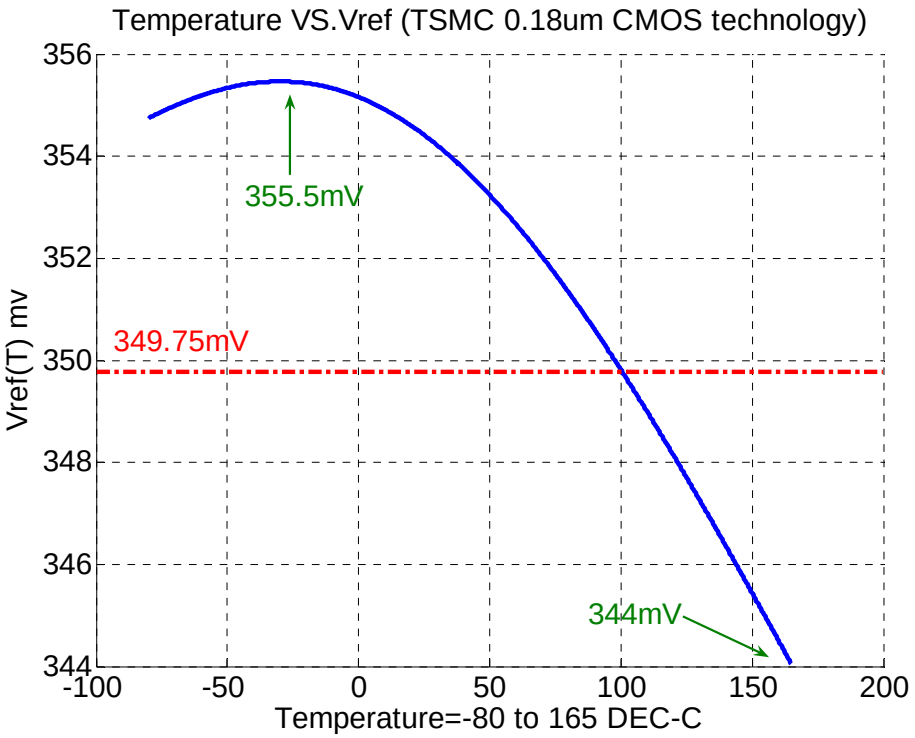


Figure 3.2.5: FF TT_RES Corner of ANVR

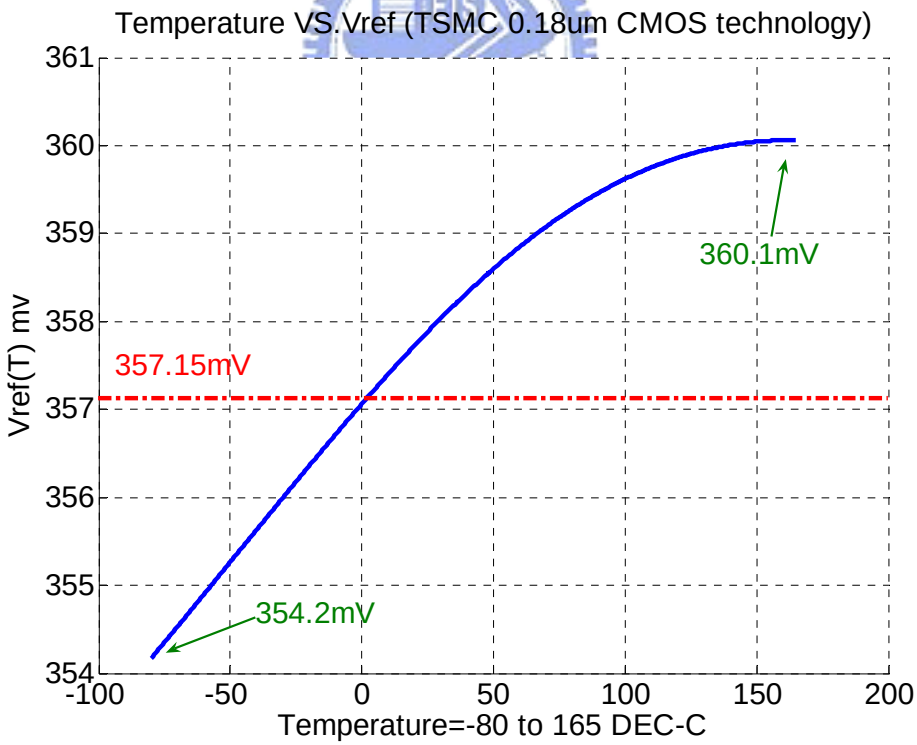


Figure 3.2.6: SS TT_RES Corner of ANVR

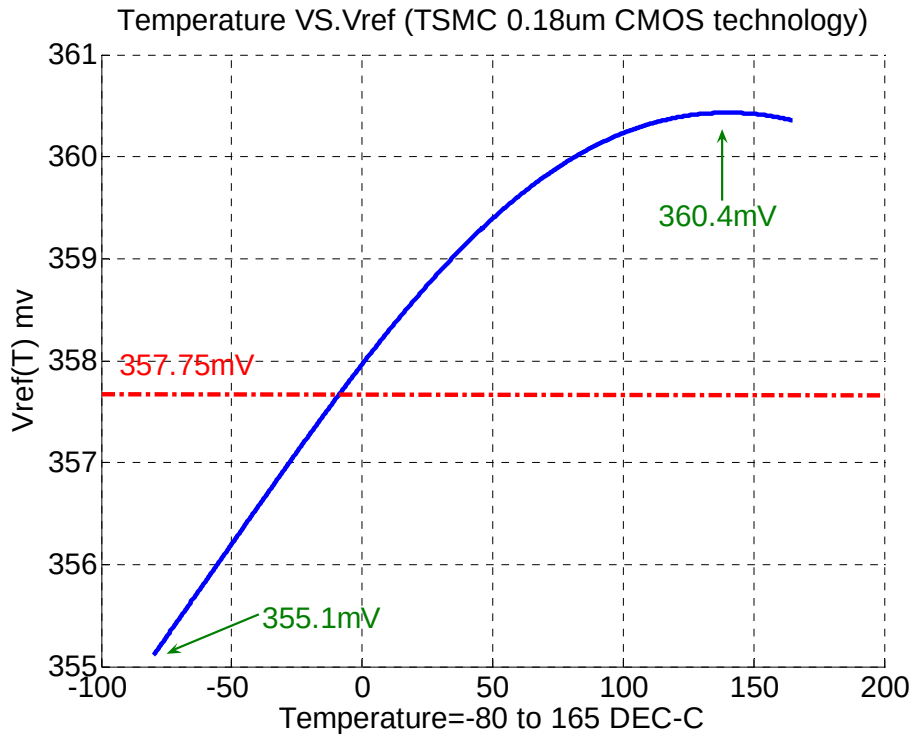


Figure 3.2.7: SF TT_RES Corner of ANVR

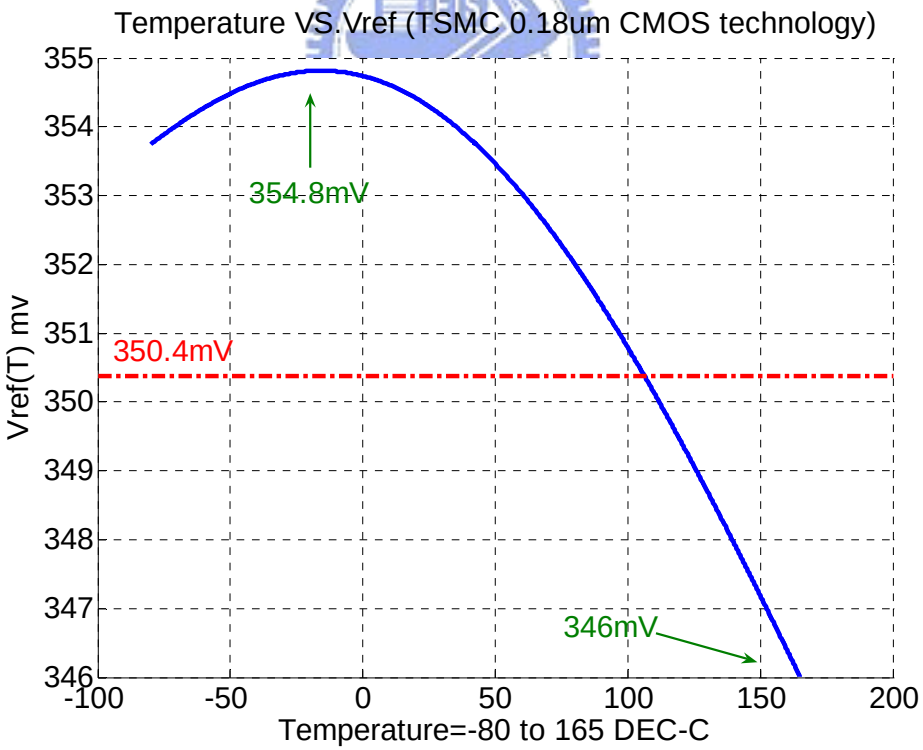


Figure 3.2.8: FS TT_RES Corner of ANVR

B. Post-Layout Simulation Results (V_{REF}):

Table 3.2: Corners of ANVR Post-Layout Simulation (V_{REF})

Corner	Resistance Corner	Temperature Coefficient (ppm/℃) (0℃~100℃)	Temperature Coefficient (ppm/℃) (-40℃~125℃)	Temperature Coefficient (ppm/℃) (-75℃~165℃)	Temperature Coefficient (ppm/℃) (-80℃~165℃)
TT	TT	16.7(0.6)	28(1.65)	32.7(2.8)	34.4(3)
	FF	23.7(0.85)	33.1(1.95)	36.8(3.15)	38.4(3.35)
	SS	22.4(0.8)	30.6(1.8)	37(3.2)	36.7(3.2)
FF	TT	153.1(5.4)	137.9(8)	137(11.5)	134.2(11.5)
	FF	113.5(4)	103.4(6)	103.7(8.7)	101.1(8.7)
	SS	193.5(6.5)	169.5(9.8)	170.5(14.1)	165.3(14.1)
SS	TT	72.5(2.5)	72.8(4.3)	66.4(5.6)	67.4(6)
	FF	75.3(2.8)	76.2(4.5)	50.1(6.1)	73.1(6.4)
	SS	64.2(2.4)	67.8(4)	63(5)	61.8(5.4)
SF	TT	64(2.2)	64.2(3.8)	59.3(5)	60.5(5.3)
	FF	69.5(2.5)	71(4.2)	66.3(5.6)	67.3(5.9)
	SS	55.7(2)	57.5(3.4)	54.7(4.6)	56(4.9)
FS	TT	167.7(4)	103.4(6)	103.4(8.8)	102.5(8.8)
	FF	79.1(2.9)	73.8(4.3)	76.9(6.6)	76.6(6.6)
	SS	141.8(10.9)	131.3(7.6)	132.5(11.1)	129.8(11.1)

( ) is derivation of voltage reference, and its unit is mV.

3.2.4 Discussion of ANVR

The performance of proposed architecture is good, but PSRR is lower than the most researches. V_{REF} will shake easily when supply voltage shakes. And ANVR has used resistors which have a derivation. Besides, the circuit needs to have a stable mechanism which can stabilize bias circuit. The three issues deserve to discuss, and we need to find solutions. In the next section, NPVR is presented to solve the above issues.

3.3 NMOSFET and PMOSFET Voltage Reference (NPVR)

When we advance problem from ANVR, the second proposed architecture can be shown to solve the problem. Its abbreviation is NPVR which means 3.3 NMOSFET and PMOSFET Voltage Reference. The proposed architecture will introduce principle, derivation, and simulation in the next section.

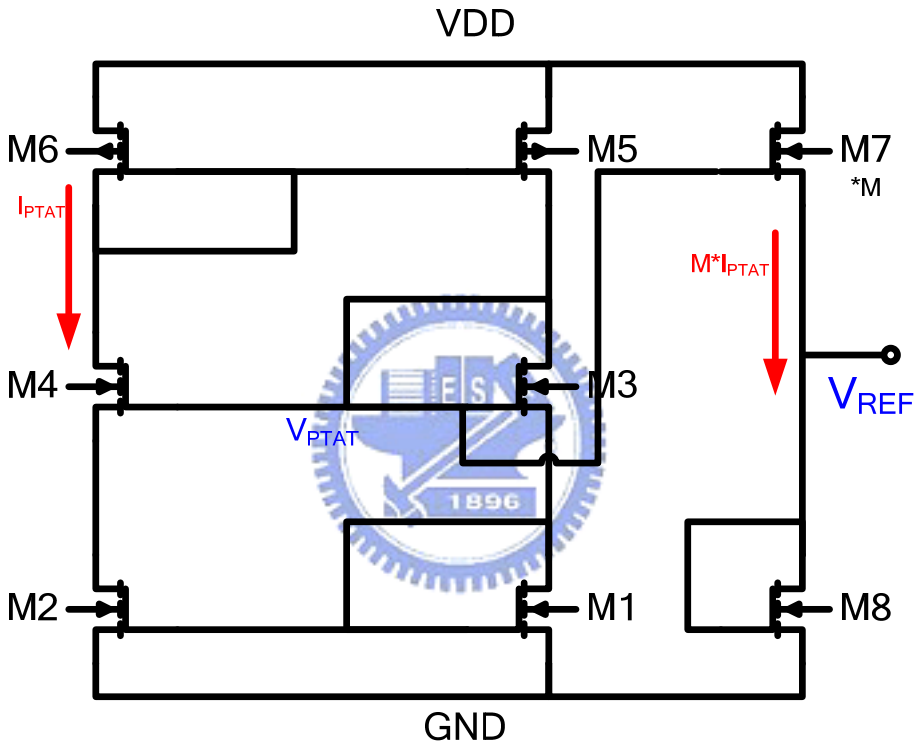


Figure 3.3.1: Architecture of NPVR

	M1	M2	M3	M4	M5	M6	M7	M8
W(μm)	1	1	1	1	1	1	0.5	0.92
L(μm)	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
m	8	8	8	8	16	16	8	8

3.3.1 Principle of NPVR

The circuit is composed of NMOS and PMOS. M1~M4, M7, and M8 are NMOS, and M5~M6 are PMOS. All MOS work in subthreshold region. The principle is like

ANVR. We use V_{GSp} of M6 to produce V_{CTAT}, and V_{DD} subtract V_{CTAT} to produce V_{PTAT}. V_{PTAT} is V_{GS3}. Therefore, the current I_{PTAT} is mirrored from M3 to M7. Beside, V_{GS8} is V_{CTAT}. Finally, M*I_{PTAT} and V_{GS8} trade-off, and a stable V_{REF} is produced. Because we hope that NPVR can operate under 1.5V, we choose V_{TH} of MOS around 0.49V. Besides, we hope that proposed architecture's power can be lower than the power of PAPER [2]. Therefore, we decide that supply voltage is 0.8V and total current is about 105nA. The each current of NPVR is about 35nA which is the same current at the architecture of PAPER [8]. Finally, we can know the size of MOS and the derivation can be shown in the next section.

3.3.2 Derivation of NPVR

The section will derivate V_{REF} and illustrate every parameters. First, bias-circuit derivation is shown, and V_{REF}-circuit derivation will be shown by bias-circuit derivation later. Therefore we can decide (W/L) and resistor by the derivation.

A. Bias-circuit simulation

M1~M6 are bias-circuit, and it is used to produce V_{PTAT}. The function can be written as

$$V_{G3}(T) = V_{GS1}(T) + V_{GS3}(T) \tag{3-17}$$

Using the current function of MOS works in weak inversion, the function of (3-17) can be written as

$$\begin{aligned} V_{G3}(T) &= V_{th1}(T) + V_{th3}(T) + nV_T \ln\left[\frac{I_D(T)}{I_S P_1} \times \frac{I_D(T)}{I_S P_3}\right] \\ &= V_{th1}(T) + V_{th3}(T) + nV_T \ln\left[\frac{I_S P_6 \exp\left[\frac{V_{SG6}(T) - |V_{th6}(T)|}{nV_T}\right]}{I_S P_1} \times \frac{I_S P_6 \exp\left[\frac{V_{SG6}(T) - |V_{th6}(T)|}{nV_T}\right]}{I_S P_3}\right] \\ &= V_{th1}(T) + V_{th3}(T) + nV_T \ln\left[\frac{P_6}{P_1} \times \frac{P_6}{P_3}\right] + V_{SG6}(T) - |V_{th6}(T)| + V_{SG6}(T) - |V_{th6}(T)| \end{aligned} \tag{3-18}$$

Because of $V_{SG6}(T) = V_{DD} - V_{G3}(T)$, the function of (3-18) can be written as

$$V_{G3}(T)=nV_T\ln\left[\frac{P_6}{P_1}\times\frac{P_6}{P_3}\right]+2V_{DD}-2V_{G3}(T)+V_{th1}(T)+V_{th3}(T)-2\left|V_{th6}(T)\right|$$
$$=\frac{2}{3}V_{DD}+\frac{1}{3}nV_T\ln\left[\frac{P_6}{P_1}\times\frac{P_6}{P_3}\right]+\frac{1}{3}\left\{V_{th1}(T)+V_{th3}(T)-2\left|V_{th6}(T)\right|\right\} \quad (3\text{-}19)$$

Therefore the bias-circuit derivation is done, and V_{G3} will be used latter.

B. V_{REF}-circuit derivation

V_{REF} can be written as the function

$$V_{GS8}(T)=V_{REF}=V_{th8}(T)+nV_T\ln\left[\frac{I_{D7}(T)}{I_S P_8}\right] \quad (3\text{-}20)$$

$$\text{Because}\quad I_{D7}(T)=I_S P_7\exp\left[\frac{V_{GS7}(T)-V_{th7}(T)}{nV_T}\right] \quad (3\text{-}21)$$

Therefore the function of V_{REF} can be written as

$$V_{GS8}(T)=V_{th8}(T)+nV_T\ln\left[\frac{I_S P_7\exp\left[\frac{V_{GS7}(T)-V_{th7}(T)}{nV_T}\right]}{I_S P_8}\right]$$
$$=V_{th8}(T)+nV_T\ln\left[\frac{P_7}{P_8}\right]+V_{GS7}(T)-V_{th7}(T) \quad (3\text{-}22)$$

We know $V_{GS7}(T)=V_{G3}(T)-V_{REF}$, so the function of (3-22) is written as

$$V_{REF}(T)=\frac{1}{2}V_{G3}(T)+\frac{1}{2}nV_T\ln\left[\frac{P_7}{P_8}\right]-\frac{1}{2}\left[V_{th8}(T)-V_{th7}(T)\right] \quad (3\text{-}23)$$

So we can bring (3-19) into (3-23), then the function of (3-24) will be shown.

$$V_{REF} = \frac{1}{2}\left\langle \frac{2}{3}V_{DD} + \frac{1}{3}nV_T \ln\left[\frac{P_6}{P_1}\times\frac{P_6}{P_3}\right] + \frac{1}{3}\left\{V_{th1}(T)+V_{th3}(T)-2\left|V_{th6}(T)\right|\right\}\right\rangle + \frac{1}{2}nV_T \ln\left[\frac{P_7}{P_8}\right] - \frac{1}{2}\left[V_{th8}(T)-V_{th7}(T)\right]$$

$$= \frac{1}{3}V_{DD} + \frac{1}{6}nV_T \ln\left[\frac{P_6}{P_1}\times\frac{P_6}{P_3}\right] + \frac{1}{6}\left\{V_{th1}(T)+V_{th3}(T)-2\left|V_{th6}(T)\right|\right\} + \frac{1}{2}nV_T \ln\left[\frac{P_7}{P_8}\right] - \frac{1}{2}\left[V_{th8}(T)-V_{th7}(T)\right]$$

$$= \frac{1}{3}V_{DD} + nV_T \ln\left\{\left[\frac{P_6}{P_1}\times\frac{P_6}{P_3}\right]^{1/6}\left[\frac{P_7}{P_8}\right]^{1/2}\right\} + \frac{1}{6}V_{th1}(T) + \frac{1}{6}V_{th3}(T) - \frac{1}{3}\left|V_{th6}(T)\right| + \frac{1}{2}V_{th7}(T) - \frac{1}{2}V_{th8}(T)$$

(3-24)

If we want V_{REF} which does not change with temperature, dV_{REF}/dT should be zero.

$$\frac{dV_{REF}}{dT} = n\frac{k}{q}\ln\left\{\left[\frac{P_6}{P_1}\times\frac{P_6}{P_3}\right]^{1/6}\left[\frac{P_7}{P_8}\right]^{1/2}\right\} + \frac{1}{6}\left[\frac{dV_{th1}(T)}{dT} + \frac{dV_{th3}(T)}{dT} - 2\frac{dV_{th6}(T)}{dT} + 3\frac{dV_{th7}(T)}{dT} - 3\frac{dV_{th8}(T)}{dT}\right] = 0$$

(3-25)

n is subthreshold slope factor , P is (W/L), and $k/q = 8.6\times10^{-5}\ ev/K$. The function of $V_{TH}(T)$ is shown as

$$V_{th}(T) = V_{th}(T_0) + (KT1 + KT2\times V_{bs})\left(\frac{T}{T_0} - 1\right) \quad (3\text{-}26)$$

And its differentiation is written as

$$\frac{dV_{th}(T)}{dT} = (KT1 + KT2\times V_{bs}) \quad (3\text{-}27)$$

KT1 is temperature coefficient of the threshold voltage and KT2 is bulk-bias coefficient of the threshold voltage's temperature dependence. $dV_{TH}(T)/dT$ can been decided when (W/L) had been decided. Therefore, $dV_{REF}(T)/dT$ can be zero by designing P_1~P_8.

3.3.3 Post-Layout Simulation of NPVR

The layout of NPVR is shown in Figure 3.3.3. The bias circuit is alternate permutation, so it can decrease mismatch. I_{PTAT} will mirror from M3 to M7. NPVR has not used resistors, so it will be no resistor derivation. Because no resistors, the area is lower than (37*24)μm^2. In addition, dummy technique has been used in the layout, and it is also used to decrease process variation. Figure 3.3.2 shows presim of ANVR, and we can compare with Figure 3.3.3 which shows postsim of ANVR. They are almost the same.

All corners are shown from Figure 3.3.4 to Figure 3.3.8, and Table 3.3 shows Corner Post-layout Simulation Results of V_{REF}. The inaccuracy of V_{REF} can be lower than 0.5mV at TT corner, and temperature coefficient is 8.6 ppm/℃ at -80℃~165℃. Beside, the inaccuracy of V_{REF} can be lower than 0.1mV at TT corner, and temperature coefficient is 1.5 ppm/℃ at 0℃~100℃. The temperature coefficient of worst case is lower than 84 ppm/℃ at -80℃~165℃ in FS corner. See Table 3.4, it is specification of NPVR. Indeed, it reaches my goal.

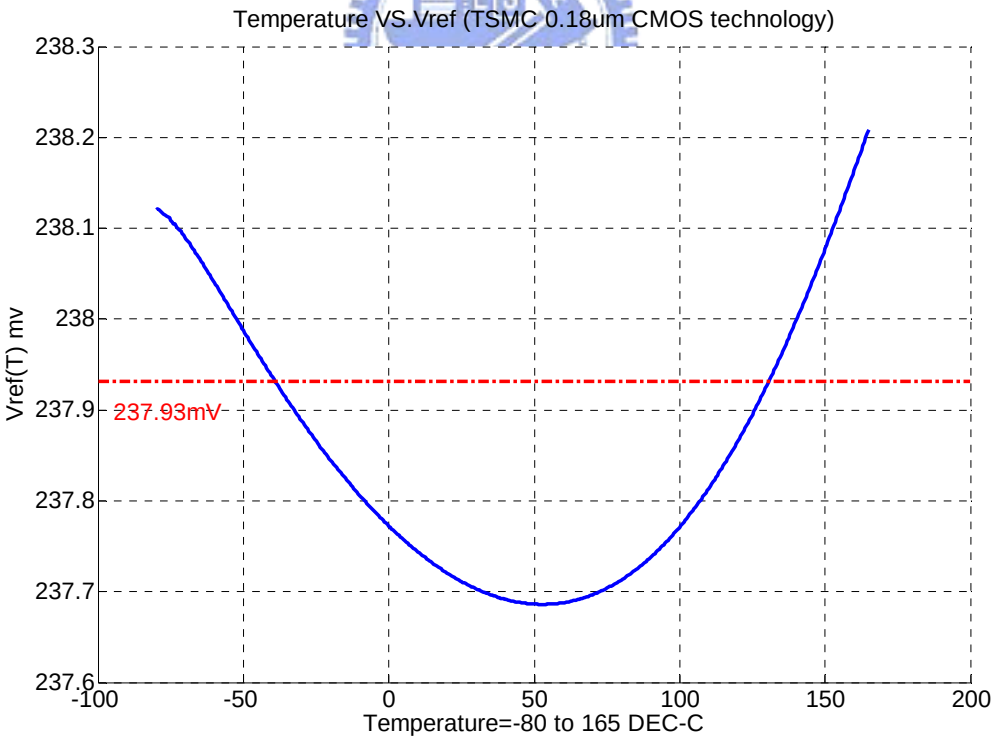


Figure 3.3.2: Presim of NPVR

Table 3.3: Post-Layout Simulation of NPVR

PAPER (year)	VDD (V)	Temperature Range (℃)	Temperature Coefficient (ppm/℃)	VREF (mV)	Tech. (μm)	AREA (mm^2)	PSRR (dB)	POWER (W)
NPVR	0.8	-80~165 -40~125 0~100	8.6 6.3 3.7	237.9 237.9 237.9	0.18	0.000888 (37*24)μm^2	18 @10MHz	83n

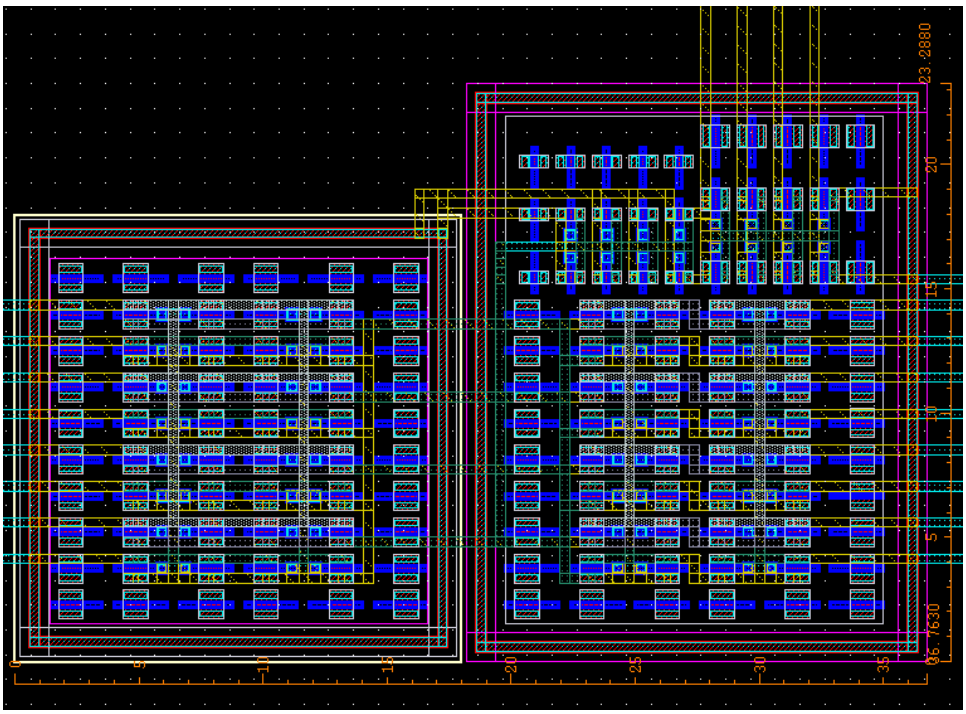


Figure 3.3.3: Layout of NPVR in TSMC 0.18um CMOS Technique

A. Post-layout Simulation Results (VREF):

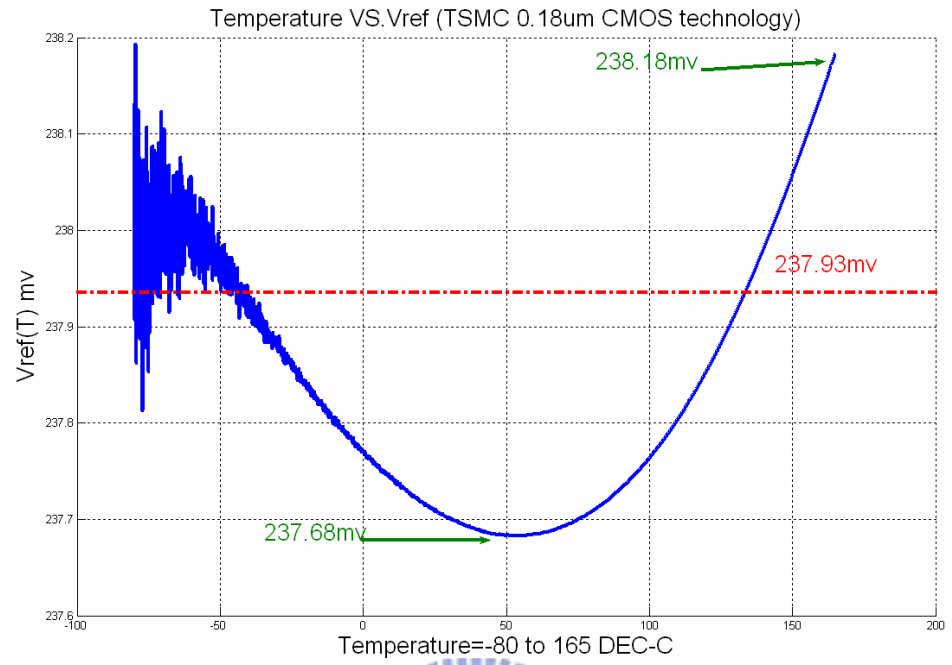


Figure 3.3.4: TT Corner of NPVR

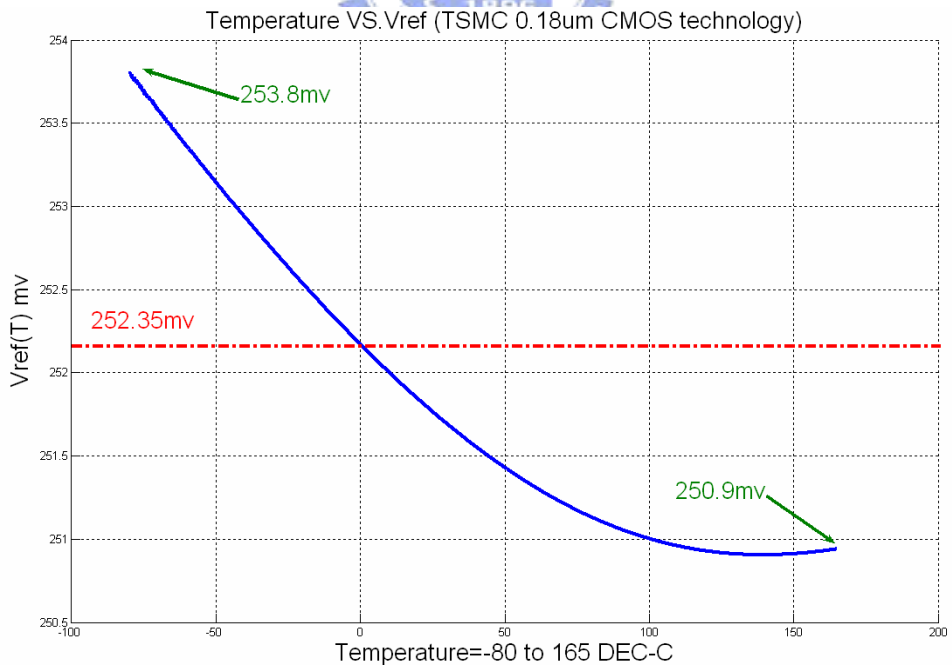


Figure 3.3.5: FF Corner of NPVR

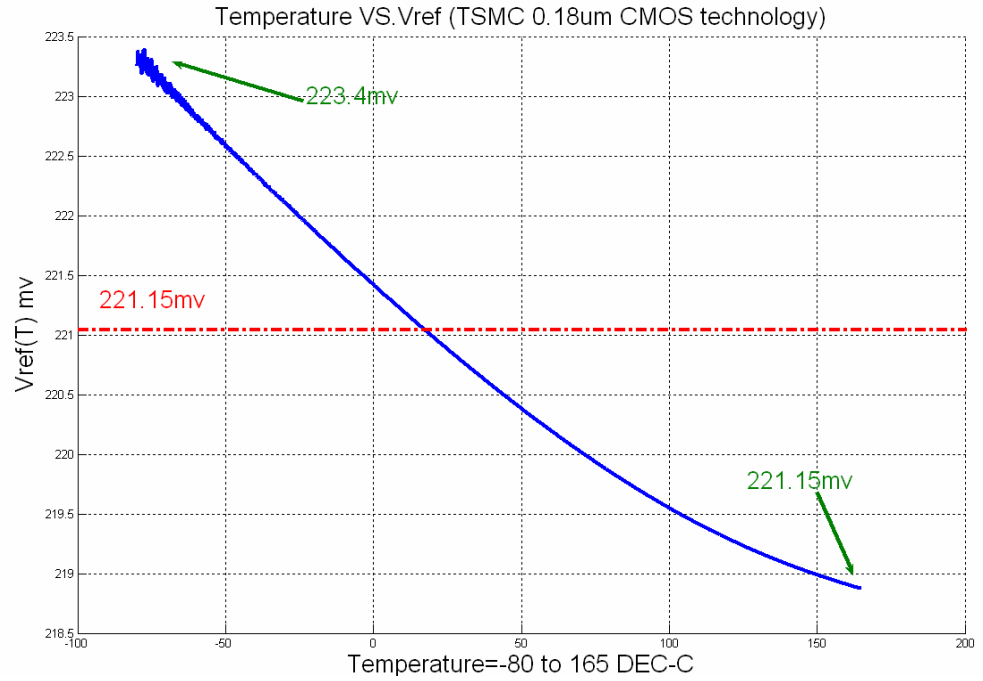


Figure 3.3.6: FS Corner of NPVR

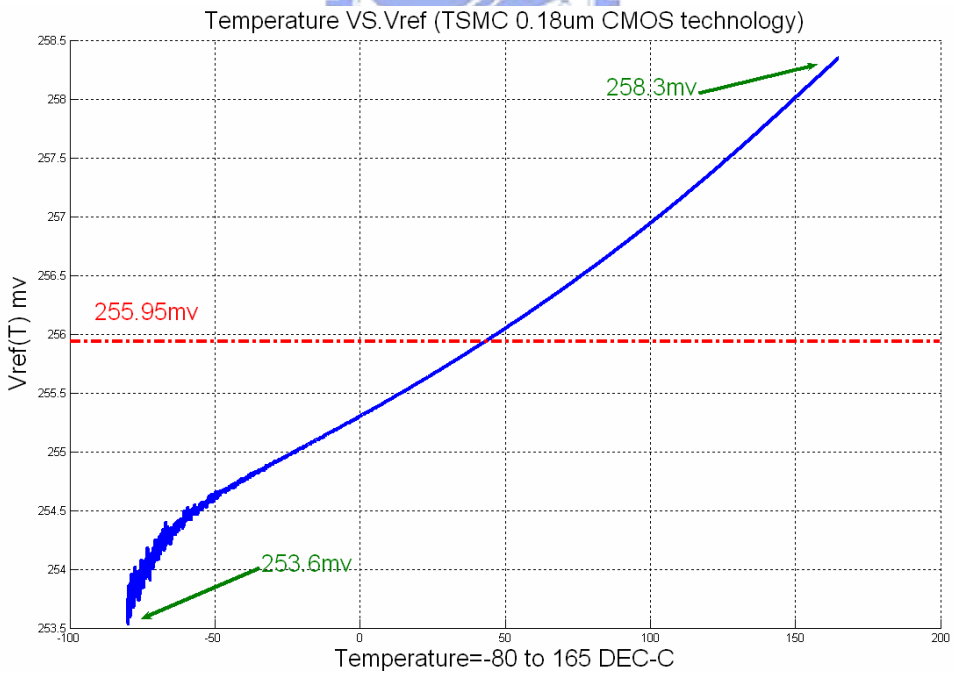


Figure 3.3.7: SF Corner of NPVR

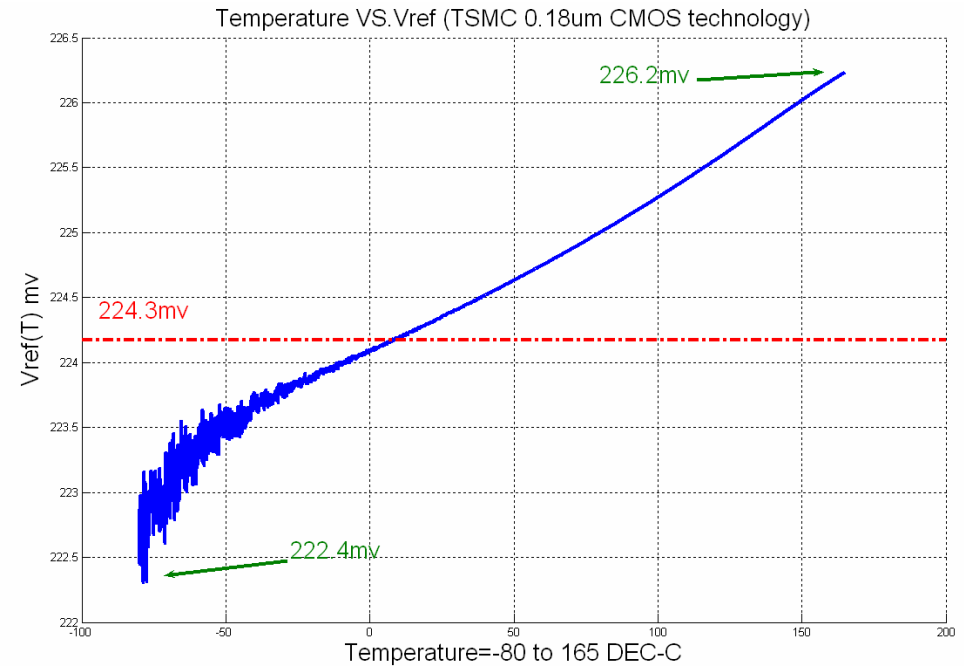


Figure 3.3.8: SS Corner of NPVR

B. Post-Layout Simulation Results (VREF):

Table 3.4: Corners of NPVR Post-Layout Simulation (V_{REF})

Corner	Temperature Range (℃)	Temperature Coefficient (ppm/℃)
TT	-80~165	8.6(0.5)
	-40~125	6.3(0.25)
	0~100	3.7(0.09)
FF	-80~165	46.9(1.8)
	-40~125	48.1(2)
	0~100	43.7(1.2)
SS	-80~165	69.1(3.4)
	-40~125	48.5(1.8)
	0~100	51.1(1.2)
SF	-80~165	75(4.4)
	-40~125	63.9(2.7)
	0~100	62.4(1.6)
FS	-80~165	83.1(4.3)
	-40~125	85.1(3.1)
	0~100	81.6(1.9)

( ) is derivation of voltage reference, and its unit is mV.

3.3.4 Discussion of NPVR

NPVR reaches three goals. First, double mirror is used to stabilize V_{PTAT} produced circuit. Second, PSRR arise from 6.5dB to 10dB. NPVR has three MOS stack, and V_{PTAT} is produced from M3. By this, V_{REF} can resist the shake from V_{DD}. Third, the area of NPVR decreases a little because we do not use resistors. Therefore, the performance of NPVR is better than ANVR. In Table 3.6, temperature coefficient, area, PSRR, and power consumption become better in NPVR.

Although NPVR has not bad performance, it still has two problems. First, start-up circuit is needed. Second, PSRR should improve. In next section, we will discuss the two problems carefully.

Table 3.5: Comparison between ANVR and NPVR

PAPER (year)	VDD (V)	Temperature Range (℃)	Temperature Coefficient (ppm/℃)	VREF (mV)	Tech. (μm)	AREA (mm^2)	PSRR (dB)	POWER (W)
NPVR	0.8	-80~165 -40~125 0~100	8.6 6.3 3.7	237.9 237.9 237.9	0.18	0.000888 (37*24)μm^2	18 @10MHz	83n
ANVR	0.8	-80~165 -40~125 0~100	34.4 27.7 16.7	356 356.7 356.7	0.18	0.00108 (30*36)μm^2	7.5 @100kHZ	403.2n

3.4 NMOS PMOS and Capacitor Voltage Reference (NPCVR)

When we advance problem from NPVR, the second proposed architecture can be shown to solve the problem. Its abbreviation is NPCVR which means voltage reference with NMOS, PMOS, and capatitor. The proposed architecture will introduce principle, derivation, and simulation in the next section.

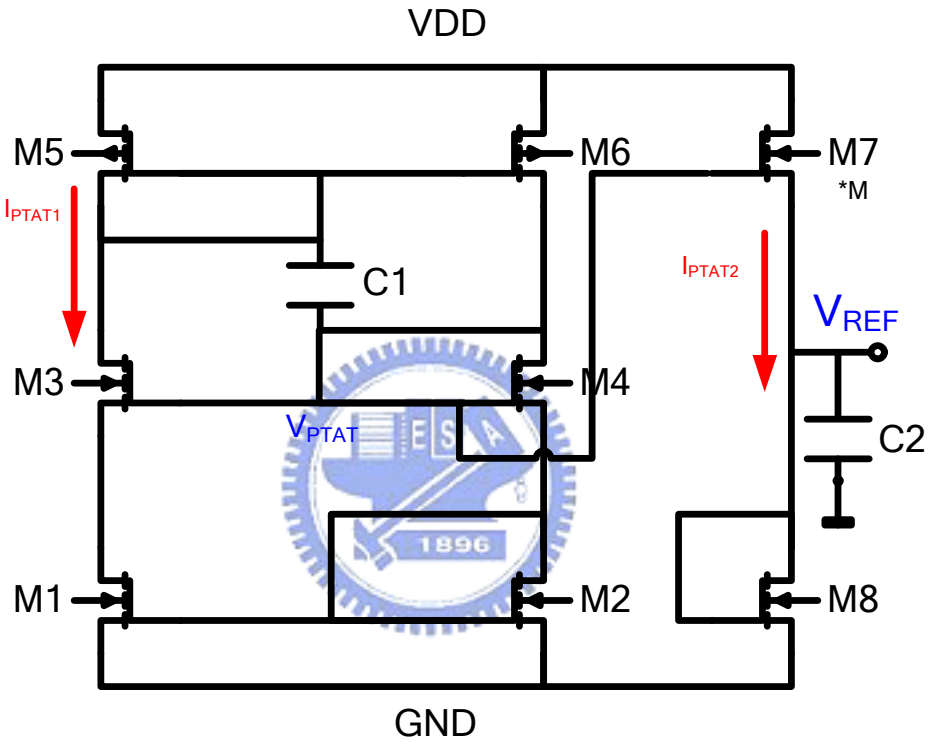


Figure 3.4.1: Voltage Reference uses NMOS, PMOS, and Capacitor (NPCVR)

	M1	M2	M3	M4	M5	M6	M7	M8	C1	C2
W(μm)	1	1	1	1	1	1	1	1.4	1pF	4pF
L(μm)	0.2									
m	16									

3.4.1 Start-up Circuit of NPCVR

In the Chapter 4, the measurement result of NPVR can discover that we can not measure V_{REF} sometimes. It means that NPVR needs start-up circuit. Therefore, we use C1 to be start-up circuit. When supply voltage is zero, voltage of all points is zero.

Then supply voltage becomes 0.8V, M5 is PMOS and it will turn on. The current flows through M5, so V_{D5} and V_{G5} will be high. M5 turns off, but the current flows through C1 and V_{G4} become high which means that M4 turns on. Therefore, proposed architecture will keep working.

3.4.2 Power Supply Reject Ratio (PSRR)

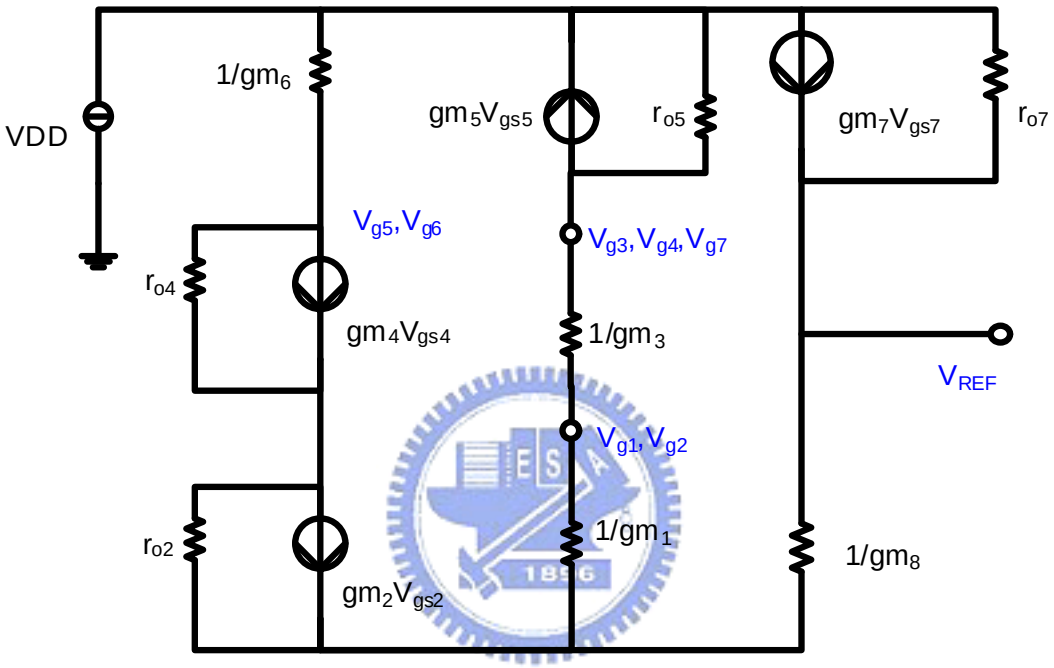


Figure 3.4.2: Small Signal of NPCVR

In Figure 3.4.2, it is small signal of NPCVR. If we want to know PSRR, we should derivate the value of V_{ref}/V_{dd}. The derivation is shown as follow.

V_{ref} can be shown as the function of (3-28).

$$
\begin{aligned}
V_{ref} &= \frac{1}{g_{m8}}\left[g_{m7}V_{gs7} + \frac{1}{r_{o7}}\left(V_{dd} - V_{ref}\right)\right] \\
&= \frac{g_{m7}}{g_{m8}}\left(V_{g7} - V_{ref}\right) + \frac{1}{g_{m8}r_{o7}}V_{dd} - \frac{1}{g_{m8}r_{o7}}V_{ref} \\
&= \frac{g_{m7}}{g_{m8}}V_{g7} + \frac{1}{g_{m8}r_{o7}}V_{dd} - \frac{1+g_{m7}r_{o7}}{g_{m8}r_{o7}}V_{ref} \\
&= \frac{g_{m7}r_{o7}}{1+g_{m8}r_{o7}+g_{m7}r_{o7}}V_{g7} + \frac{1}{1+g_{m8}r_{o7}+g_{m7}r_{o7}}V_{dd}
\end{aligned}
\qquad (3\text{-}28)
$$

V_{g7} can be shown as the function of (3-29).

$$
\begin{aligned}
V_{g7} &= \left(\frac{g_{m1}+g_{m3}}{g_{m1}g_{m3}}\right)\left[-g_{m5}V_{gs5}+\frac{1}{r_{o5}}\left(V_{dd}-V_{g7}\right)\right] \\
&= \left(\frac{g_{m1}+g_{m3}}{g_{m1}g_{m3}}\right)\left[\frac{1+g_{m5}r_{o5}}{r_{o5}}V_{dd}-\frac{1}{r_{o5}}V_{g7}-g_{m5}V_{g5}\right] \\
&= \frac{2}{g_{m1}}\left[\frac{1+g_{m5}r_{o5}}{r_{o5}}V_{dd}-\frac{1}{r_{o5}}V_{g7}-g_{m5}V_{g5}\right] \\
&= \frac{2+2g_{m5}r_{o5}}{2+g_{m1}r_{o5}}V_{dd}-\frac{2g_{m5}r_{o5}}{2+g_{m1}r_{o5}}V_{g5}
\end{aligned}
\qquad (3\text{-}29)
$$

V_{g5} can be shown as the function of (3-30).

$$
\begin{aligned}
V_{g5} &= V_{dd}-\frac{1}{g_{m6}}\left[g_{m2}V_{g2}+\frac{V_{g5}}{r_2+r_4}\right] \\
&= V_{dd}-\frac{g_{m2}}{g_{m6}}V_{g2}-\frac{1}{g_{m6}\left(r_{o2}+r_{o4}\right)}V_{g5} \\
&= V_{dd}-\frac{g_{m1}}{g_{m5}}V_{g2}-\frac{1}{2g_{m5}r_{o1}}V_{g5} \\
&= \frac{2g_{m5}r_{o1}}{1+2g_{m5}r_{o1}}V_{dd}-\frac{2g_{m1}r_{o1}}{1+2g_{m5}r_{o1}}V_{g2}
\end{aligned}
\qquad (3\text{-}30)
$$

V_{g2} can be shown as the function of (3-31).

$$
\begin{aligned}
V_{g2} &= \frac{1}{g_{m1}}\left[-g_{m5}V_{gs5}+\frac{1}{r_{o5}}\left(V_{dd}-V_{g7}\right)\right] \\
&= \frac{1}{g_{m1}}\left[-g_{m5}\left(V_{g5}-V_{dd}\right)+\frac{1}{r_{o5}}\left(V_{dd}-V_{g7}\right)\right] \\
&= \frac{1+g_{m5}r_{o5}}{g_{m1}r_{o5}}V_{dd}-\frac{g_{m5}}{g_{m1}}V_{g5}-\frac{1}{g_{m1}r_{o5}}V_{g7}
\end{aligned}
\qquad (3\text{-}31)
$$

We can derivate V_{ref}/V_{dd} by the function of (3-28), (3-29), (3-30), and (3-31).

$$
\begin{aligned}
V_{ref} &= \left[\left(\frac{g_{m7}r_{o7}}{1+g_{m8}r_{o7}+g_{m7}r_{o7}}\right)\left(\frac{1+g_{m5}r_{o5}+g_{m5}r_{o1}}{1+g_{m1}r_{o5}+2g_{m5}r_{o1}}\right)+\frac{1}{1+g_{m8}r_{o7}+g_{m7}r_{o7}}\right]V_{dd} \\
\frac{V_{ref}}{V_{dd}} &\approx \left(\frac{g_{m7}r_{o7}}{1+g_{m8}r_{o7}+g_{m7}r_{o7}}\right)\left(\frac{1+g_{m5}r_{o5}+g_{m5}r_{o1}}{1+g_{m1}r_{o5}+2g_{m5}r_{o1}}\right)\approx\left(\frac{g_{m7}}{g_{m8}+g_{m7}}\right)\left(\frac{g_{m5}r_{o5}+g_{m5}r_{o1}}{g_{m1}r_{o5}+2g_{m5}r_{o1}}\right)\approx\frac{1}{3}\approx 10dB \\
g_x &= \frac{I_D}{nV_T} \qquad r_x = \frac{V_A}{I_D}
\end{aligned}
\qquad (3\text{-}32)
$$

Therefore, V_{ref}/V_{dd} is about 10dB, and it means PSRR is 10dB in zero frequency. It is a disadvantage at proposed architectures, and it is hard to change. But we still can pull up PSRR at higher frequency. A capacitor which is put in output is a method to

pull up PSRR. We know that pole is 1/(R*C) and main pole is in output. If we put a capacitor which is 4pF in output, the main pole will move to lower frequency. By this, PSRR will pull up at higher frequency. See Figure 3.4.3, PSRR is shown from 0Hz to 10MHz, and PSRR of NPCVR is better than NPVR.

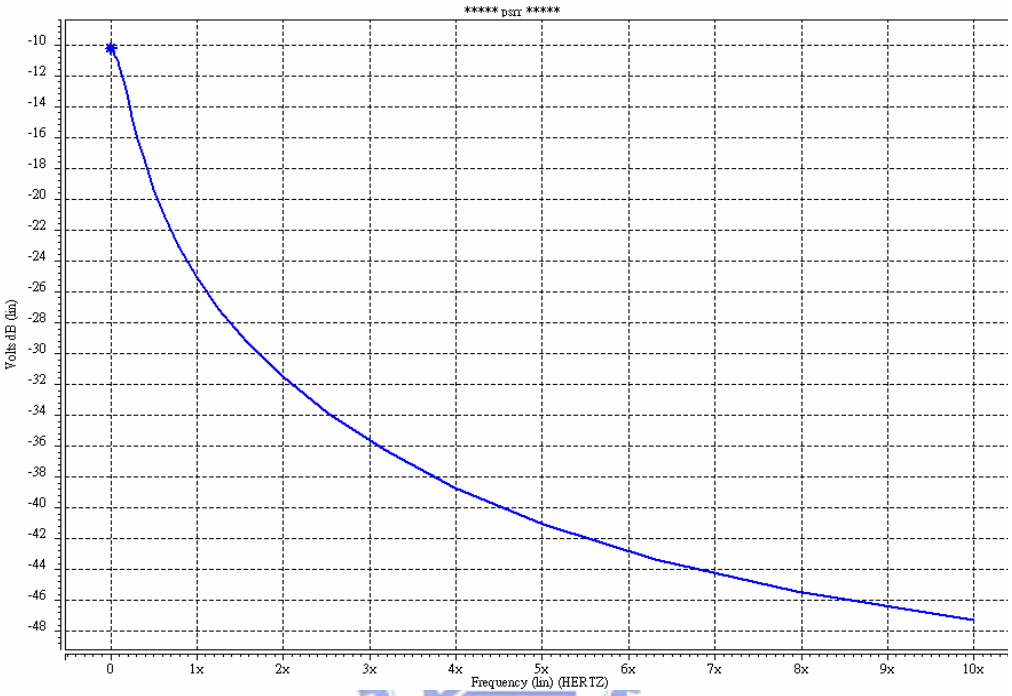


Figure 3.4.3: PSRR of NPCVR

3.4.3 Post-Layout Simulation of NPCVR

The performance of NPCVR is shown at Table 3.6. Although, the area and power of NPCVR is bigger than NPVR. But they are still smaller than other papers, and the comparison will be shown in the next section. Layout of NPCVR is shown at Figure 3.4.4 and the area is (105*95)μm^2. All corners are shown at Figure 3.4.5~Figure 3.4.9.

Table 3.6: Post-Layout Simulation of NPCVR

PAPER (year)	VDD (V)	Temperature Range (℃)	Temperature Coefficient (ppm/℃)	VREF (mV)	Tech. (μm)	AREA (mm^2)	PSRR (dB)	POWER (W)
NPCVR	0.8	-40~125 0~100	14.68 10.39	228 228	0.18	0.001mm^2 (105*95)μm^2	47dB @10MHz	152n

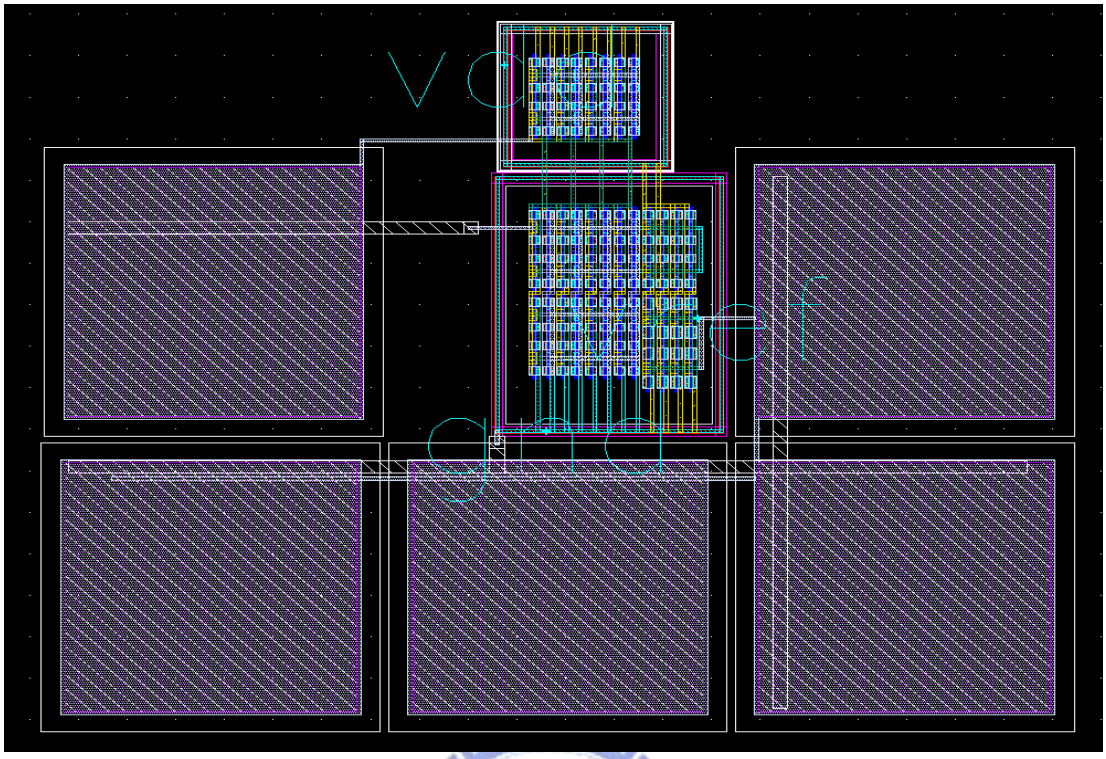


Figure 3.4.4: Layout of NPCVR

A. Post-layout Simulation Results (VREF):

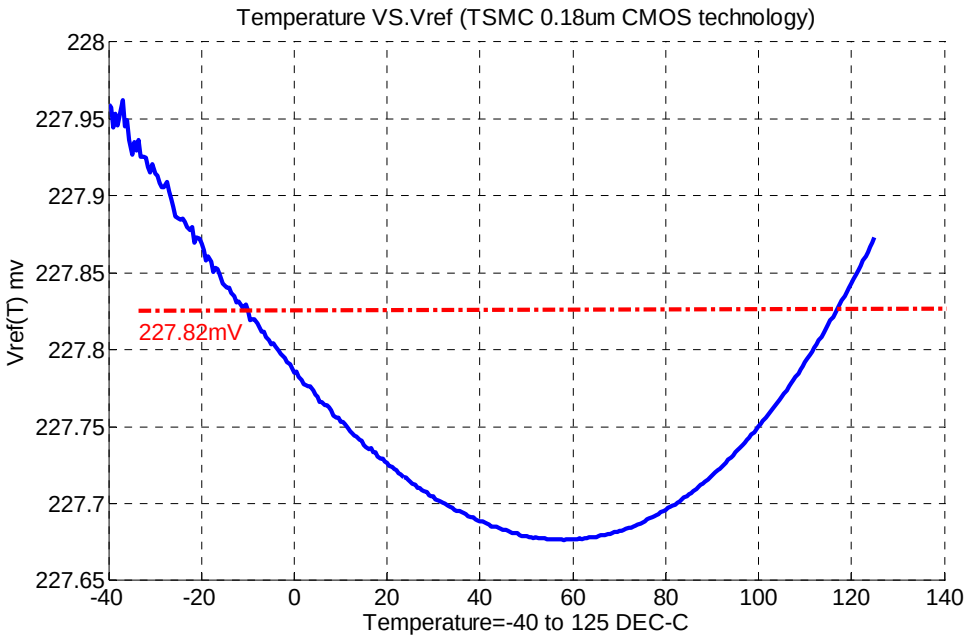


Figure 3.4.5: TT Corner of NPCVR

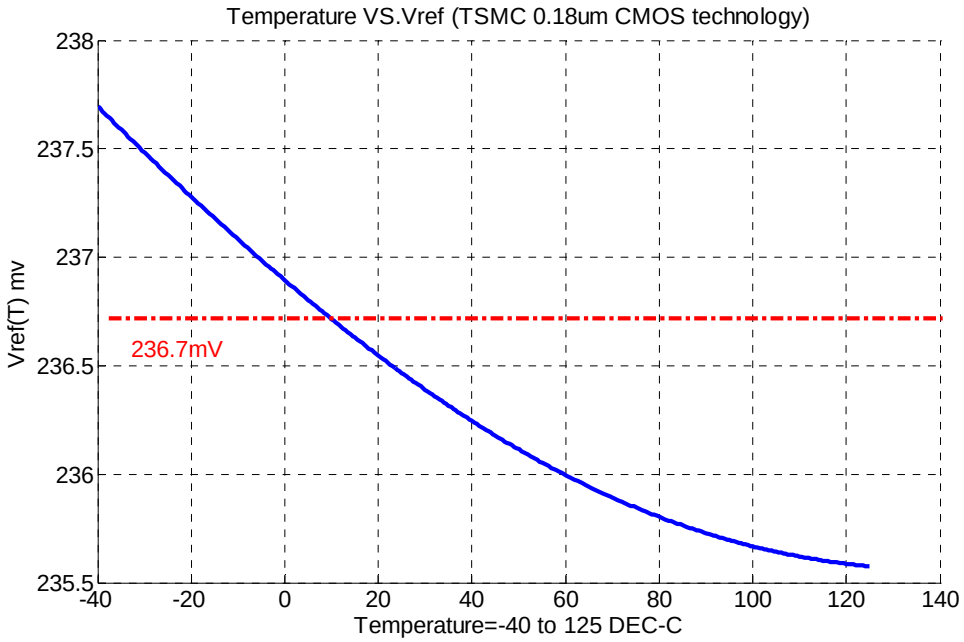


Figure 3.4.6: FF Corner of NPCVR

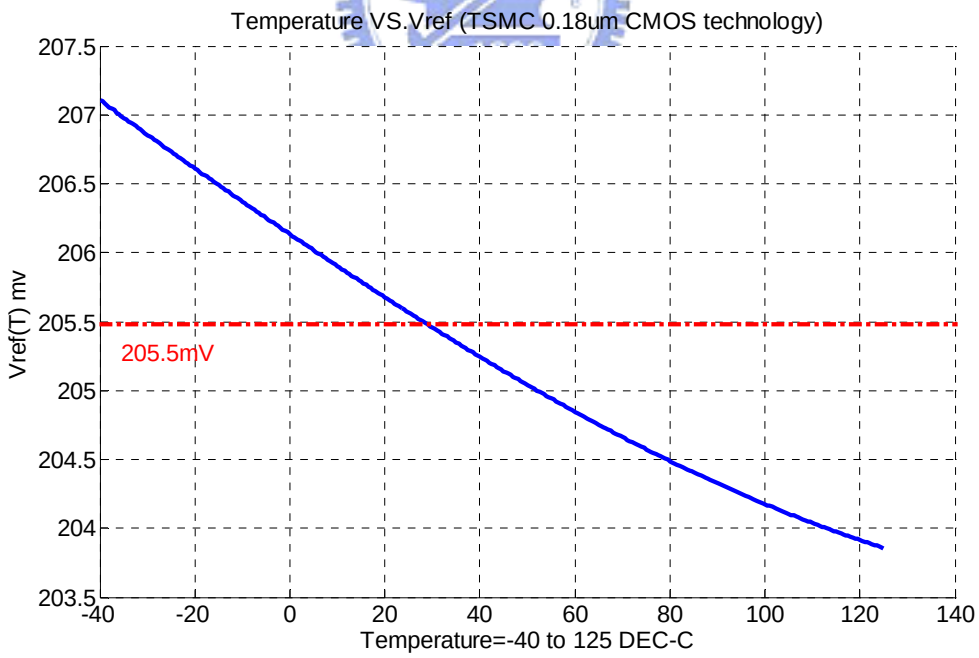


Figure 3.4.7: FS Corner of NPCVR

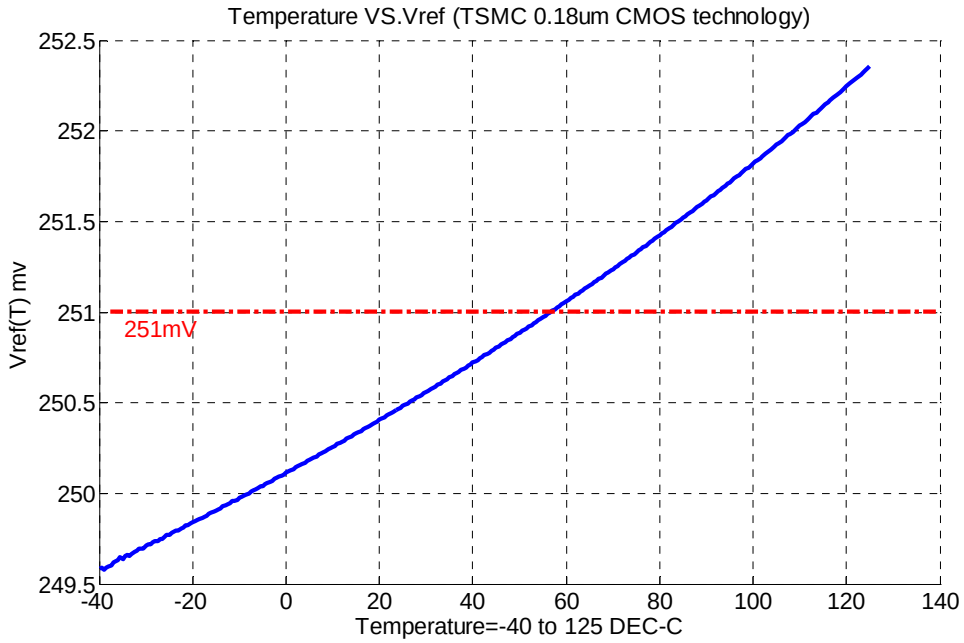


Figure 3.4.8: SF Corner of NPCVR

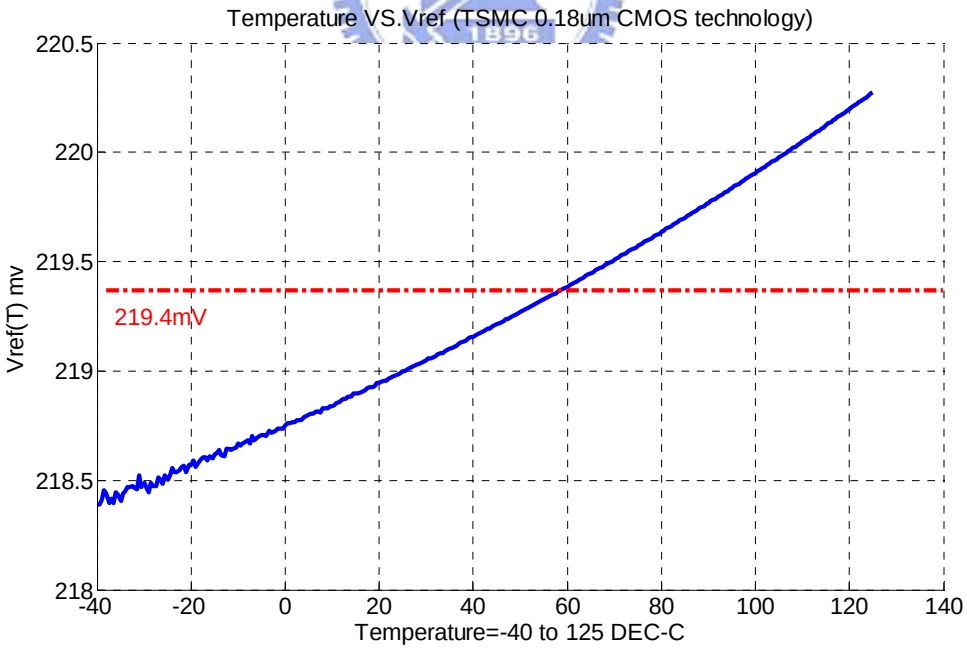


Figure 3.4.9: SS Corner of NPCVR

C. Post-Layout Simulation Results (VREF):

Table 3.7: Corners of NPCVR Post-Layout Simulation (V_{REF})

Corner	Temperature Range (℃)	Temperature Coefficient (ppm/℃)
TT	-40~125	14.68
	0~100	10.39
FF	-40~125	51
	0~100	50.7
SS	-40~125	102
	0~100	97.1
SF	-40~125	65.2
	0~100	59.8
FS	-40~125	49.7
	0~100	59.2

( ) is derivation of voltage reference, and its unit is mV.

3.4.4 Discussion of NPCVR

As shown in Table 3.9, it is shown that PSRR is pull up to 47dB at 10MHz. The performance does not change very much, and PSRR becomes high a lot. Otherwise, NPCVR has start-up circuit to improve the question of NPVR. In the next section, we will show all papers and proposed architectures to compare the performance.

Table 3.8: Comparison between NPVR and NPCVR

PAPER (year)	VDD (V)	Temperature Range (℃)	Temperature Coefficient (ppm/℃)	VREF (mV)	Tech. (μm)	AREA (mm^2)	PSRR (dB)	POWER (W)
NPCVR	0.8	-40~125 0~100	14.68 10.39	228 228	0.18	0.001mm^2 (105*95)μm^2	47dB @10MHz	152n
NPVR	0.8	-40~125 0~100	6.3 3.7	237.9 237.9	0.18	0.000888 (37*24)μm^2	18 @100kHZ	83n

3.5 Comparison

Three proposed architectures and researches are compared at Table 3.10. Obviously, the performance of proposed architectures is good by comparing all researches. Let's see the performance one by one.

1. **Supply Voltage:** Supply voltage of proposed architectures is the lowest voltage in all researches. We know that power is supply voltage to multiply total current, so low supply voltage is easy to get low power. It means that proposed architectures can apply to low power systems.
2. **Temperature Range:** Proposed temperature range is the widest temperature range which is -40℃ ~ 125℃ in all researches. Even it can apply at the space.
3. **Temperature Coefficient:** It is important authority of performance. Temperature coefficient of NPCVR is 14.68 ppm/℃ at -40℃ ~ 125℃. It is very low temperature coefficient and very wide temperature range. Even temperature coefficient has still 10.39 ppm/℃ at 0℃ ~ 100℃.
4. **Area:** The area of proposed architectures is low to several hundreds μm^2. Indeed, it reaches the goal which is that proposed architectures can apply in battery-operated systems.
5. **Power:** The power of proposed architectures is low to several dozens nW. It truly achieves low power, and it is very suitable to apply in any low power systems.

The whole said that the performance of proposed architectures is better than the most researches. The result proofs that proposed architectures achieve our goal.

Table 3.9: Comparison of All Voltage Reference's Architectures

PAPER (year)	VDD (V)	Temperature Range (℃)	Temperature Coefficient (ppm/℃)	VREF (mV)	Tech. (μm)	AREA (mm^2)	PSRR (dB)	POWER (W)
NPCVR	***0.8***	***-40~125 0~100***	***14.68 10.39***	***228 228***	***0.18***	***0.001mm² (105*95)μm²***	***47dB***	***152n***
NPVR	***0.8***	***-40~125 0~100***	***6.3 3.7***	***237.9 237.9***	***0.18***	***0.000888 (37*24)μm²***	***18***	***83n***
ANVR	***0.8***	***-40~125 0~100***	***27.7 16.7***	***356.7 356.7***	***0.18***	***0.00108 (30*36)μm²***	***7.5***	***403.2n***
Voltage Mode of PTAT and CTAT						* is that research has experimental result		
*[1]2004	4.5~5	25~90	347	1320	0.18			
*[2]2005	0.9	0~100	39	514	0.35	0.12	22	780n

*[3]2005	2	0~70	62	579	0.35	0.126	84	4.6u
*[4]2006	0.9~4	0~80	10	670	0.35	0.045	40	63n
[5] 2004	1.1~2.2	-10~70	85	504	0.18			176u
[6] 2005	3.3	0~150	26	711	0.35			
[7] 2006	1.3	-50~130	9	546	0.18		100	80u
[8] 2006	0.5	-40~100	2.2	319	0.13	0.0002	14	40n
Current Mode of PTAT and CTAT								
*[9]2003	1.2	-25~125	119	295	1.2	0.23	40	4.32u
*[10]2006	0.85	-20~120	194	221	0.18	0.0238		3.3u
[11] 2003	0.6	-40~100	93	400	0.13			
[12] 2003	1.5	-40~125	37.88	800	0.13			120u
[13] 2003	0.6~1.8	0~80	80	405	0.18	0.1	82	25u
[14] 2004	3~5	-60~100	4	1165.4	1.2	0.18		30u
[15] 2004	1	-20~80	200	400	0.35			3u
[16] 2004	0.8	0~100	33	592	0.6	0.05	50	0.88u
[17] 2005	1	-40~125	66.7	225	0.5			4u
[18] 2005	1.8	0~70	32.5	615.1	0.18	0.1	35	1.6u
[19] 2006	1.2	-20~90	61.64	718	0.09			1.6u
[20] 2006	0.8~2.6	-20~120	64.2	278	0.18	0.04		5.4u
Voltage Reference Uses Parallel Voltages								
*[21]2003	1.4	0~100	36.9	309	0.6	0.055	20	13.58u
*[22]2004	5	-10~80	32	2670	0.5	0.0936		970u
*[23]2005	1.5	0~80	25	168	0.35	0.08	59	3.6u
*[24]2006	1.5~4.3	0~80	12	891.1	0.35	0.015	59	300n
[25] 2005	0.6~1.8	0~75	70	332	0.18			
[26] 2006	0.9~3.3	-40~100	33	181	0.35			1.1u
ZTC								
*[27]2001	3~3.3	-20~100	15	799	0.35	0.0204		
[28] 2004	1	-50~150	4	640	0.18			
[29] 2005	3.3	-50~120	50	821&1264	0.35			36.3u
Voltage Reference Uses Non-standard Process								
*[30]2003	1	-50~100	80	410				0.6u
*[31]2004	2.8~5.5	-20~100	54.6	0.8~1.5	0.5	0.081	80	500u
*[32]2005	4.5~9	-40~85	1	1250~5000	1.5	1.6	67	3.15u
*[33]2006	1.2	-60~140	130	400	0.35	0.0022		40u

3.6 Summary

This chapter shows proposed architectures and discusses the proposed architectures. We simulate proposed architectures, and the performance is good at HSPICE simulation. But it does not mean that experimental results of chips are as good as HSPICE simulation. So the three proposed architectures had taped out in TSMC 0.18μm process. In the next chapter, experimental results will be shown.

CHAPTER 4

Measurement

Proposed design architecture ANVR and NPVR are taped out in TSMC 0.18um CMOS process technique. In this chapter, the measurement environment and method are shown first. Then experimental results of ANVR and NPVR are presented by figures and data. A comparison by proposed design architectures and researches is presented. Finally, we will illustrate the derivation between post-layout simulation and experimental results.

4.1 Measurement Set-up

In Figure 4.1, measurement environment is shown. The chip is put in a temperature and humidity chamber and other electronic devices which are batteries, voltage-stabilizer circuit, and oscilloscope is put outside. By this, the temperature variation only affects the measured chips and does not affect other electronic devices. That is because we only want to know the effect of V_{REF} which is measured from the chip when temperature changes from -40℃ to 125℃. If the other electronic devices are also affected by temperature, the measured V_{REF} will be incorrect. Beside measurement environment mentions a temperature and humidity chamber. It can adjust and stabilize temperature from -75℃ to 165℃ and the deviation of temperature is lower than 0.1℃. It will be useful to measure a correct voltage reference.

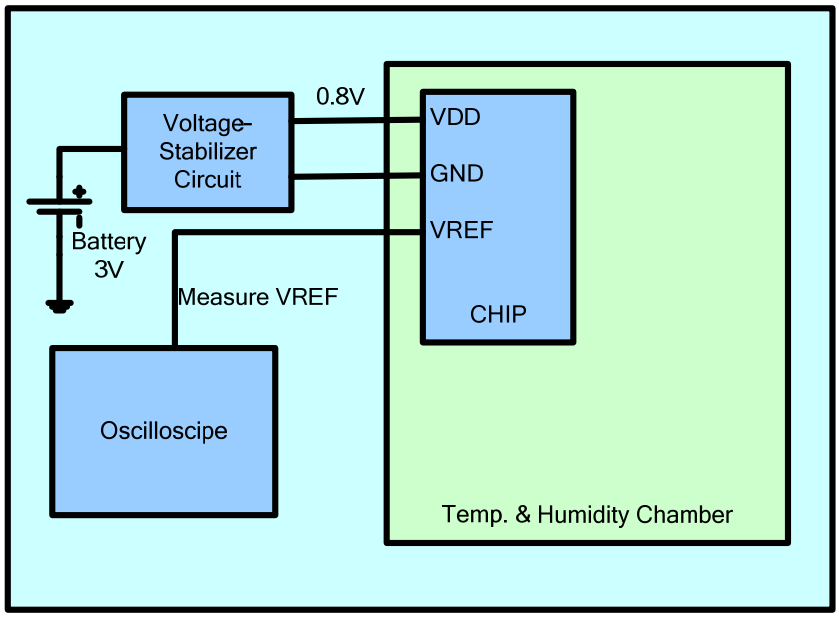


Figure 4.1: Block Diagram of Measurement Environment

In Figure 4.2, it shows a voltage-stabilizer circuit which is composed of a IC(LM317), resistors, capacitors, inductors, and a diode(1N5402). Because proposed design architectures need 0.8V to be a supply voltage, the voltage-stabilized circuit must to have two parts. First part is conventional voltage-stabilized circuit which can produce and stabilize a voltage of 1.2V. Second part is series voltage-stabilized circuit which further decreases 1.2V to 0.8V. Of course, it has also the function of voltage-stabilized. By this, a stable supply voltage provides to the measured chips.

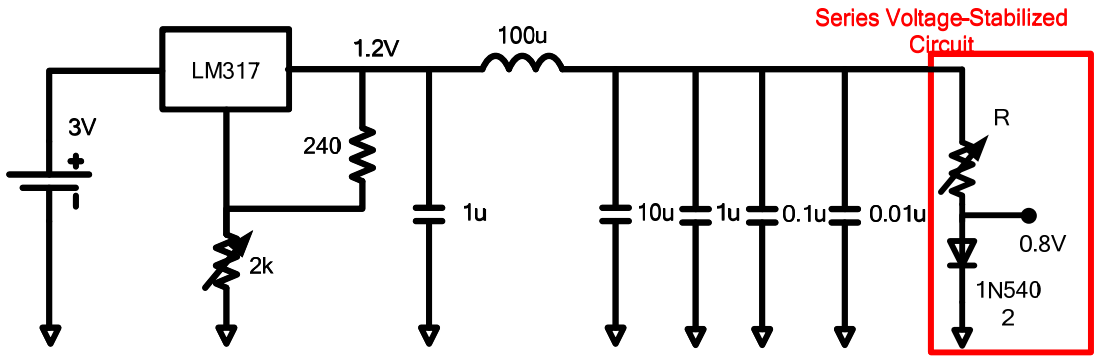


Figure 4.2: Block Diagram of Voltage-Stabilized Circuit

Measurement environment is shown in Figure 4.3. The right side of Figure 4.3 is a temperature and humidity chamber and the PCB is put inside. The PCB is shown at

the under side of Figure 4.3. One PCB has four chips because it can save measurable time.

Figure 4.3: The Pictures of Measurement Environment

4.2 Experimental Result

In this section, experimental results will be presented and illustrated. Then a comparison which has proposed design architectures and researches is shown by table. By this, it can prove that proposed design architectures are suitable for battery-operated system.

4.2.1 Experimental Result of ANVR

Experimental results of proposed design architecture ANVR is shown at Figure 4.4. The lowest voltage is 354mV and the highest voltage is 360mV at the different chips. The largest derivation is lower than 6mV and it is the worst case. The experimental results show temperature range of -40℃~125℃. Although temperature range of post-layout simulation is -80℃~165℃, the HSPICE model only support temperature range of -40℃~125℃.

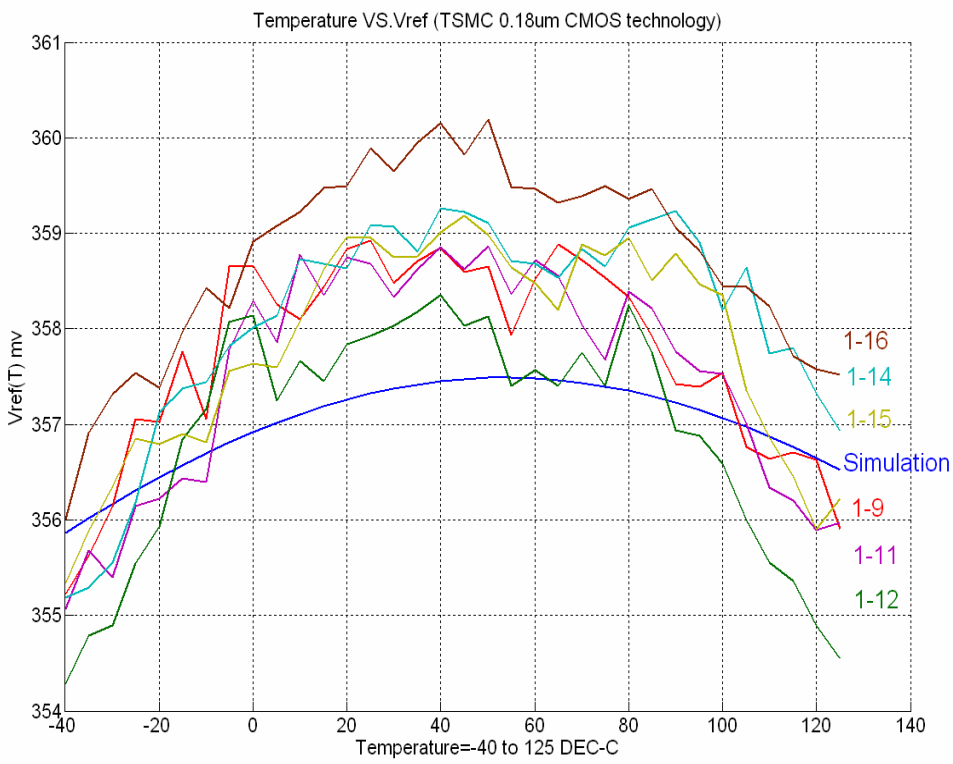


Figure 4.4: Experimental Result of ANVR

Table 4.1: The Derivation for V_{REF} of ANVR

Temperature(℃)	**-40~125**	**0~100**
Simulation(mV)	356.67±0.82	357.2±0.3
CHIP 1-9(mV)	357.08±1.85	358.16±0.77
CHIP 1-11(mV)	356.64±1.57	358.2±0.67
CHIP 1-12(mV)	356.32±2.03	357.47±0.88
CHIP 1-14(mV)	357.22±2.04	358.62±0.62
CHIP 1-15(mV)	357.27±1.92	358.4±0.93
CHIP 1-16(mV)	358.1±2.1	359.32±0.87

Table 4.1 shows the derivation of V_{REF} for proposed design architecture ANVR. The best case is CHIP 1-11 which derivation is only ±1.57mV and ±0.67mV when temperature range is -40℃~125℃ and 0℃~100℃. Although experimental results are not better than simulation, the voltage derivation has only several milli-Volt at temperature range of -40℃~125℃. Table 4.2 shows experimental results of ANVR. The power is not larger than 450nW, and PSRR is about 10dB. The worst temperature

coefficient is 70ppm/℃, and it is not as good as post-layout simulation. Beside measurable error, we need to find out the source of inaccuracy.

Table 4.2: Experimental Results of ANVR

	Simulation	**1-9**	**1-11**	**1-12**
Supply voltage	0.8v			
Temperature range	-40℃~125℃ 0℃~100℃	-40℃~125℃ 0℃~100℃	-40℃~125℃ 0℃~100℃	-40℃~125℃ 0℃~100℃
Temperature coefficient	27.7ppm/ ℃ 16.8ppm/ ℃	62.8ppm/℃ 42.9ppm/℃	53.28ppm/℃ 37.27ppm/℃	69.2ppm/℃ 49.3ppm/℃
V_{REF} (mV)	356.7 356.7	357.08 358.16	356.64 358.2	356.32 357.47
PSRR	7dB @10MHz	9.8dB @10MHz	11.1dB @10MHz	10.9dB @10MHz
Power	403.2nA	436nA	436nA	445nA
Area	$0.00108mm^2$			
Tech.	0.18μm			
	Simulation	**1-14**	**1-15**	**1-16**
Supply voltage	0.8v			
Temperature range	-40℃~125℃ 0℃~100℃	-40℃~125℃ 0℃~100℃	-40℃~125℃ 0℃~100℃	-40℃~125℃ 0℃~100℃
Temperature coefficient	27.7ppm/ ℃ 16.8ppm/ ℃	69.22ppm/℃ 34.66ppm/℃	65.2ppm/℃ 44.28ppm/℃	70.9ppm/℃ 48.4ppm/℃
V_{REF} (mV)	356.7 356.7	357.22 358.62	357.27 358.4	358.1 359.32
PSRR	7dB @10MHz	9.5dB @10MHz	9.2dB @10MHz	10.6dB @10MHz
Power	403.2nA	428nA	431nA	423nA
Area	$0.00108mm^2$			
Tech.	0.18μm			

See Table 4.3, it shows resistor variation which may cause the inaccuracy of V_{REF}. We use P+ Poly w/i Silicide as a resistor of ANVR. However, every 7.9 ohm has ± 2.5 ohm variation that is large error to affect V_{REF}. Therefore, resistor variation is possible source of V_{REF} derivation.

Table 4.3: Resistor Variation

Film	Valid Width	Rsh Mean/Range	Unit
P+ Poly w/i Silicide	W≥2.0	7.9± 2.5	Ω/sq

4.2.2 Experimental Result of NPVR

Experimental results of proposed design architecture NPVR is shown at Figure 4.6. The derivation is lower than several milli-Volt, but it does not match with post-layout simulation. The lowest voltage is 236mV and the highest voltage is 238mV at the different chips. The largest derivation is lower than 2mV and it is the worst case. The experimental results show temperature range of -40℃~125℃. Although temperature range of post-layout simulation is -80℃~165℃, the HSPICE model only support temperature range of -40℃~125℃.

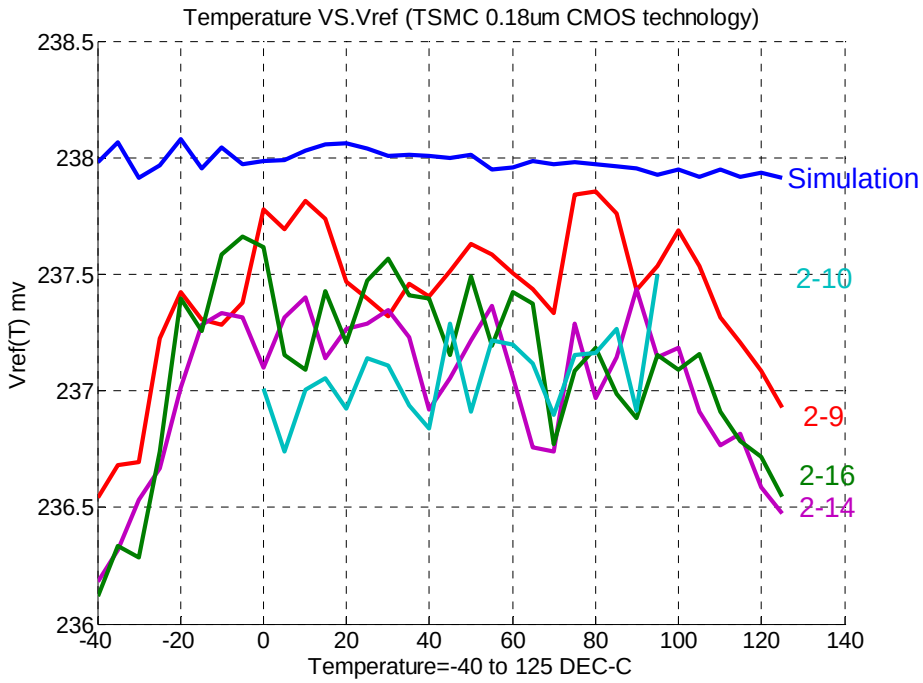


Figure 4.5: Experiment Results of NPVR

Table 4.4: The Derivation of V_{REF} for NPVR

Temperature(℃)	**-40~125**	**0~100**
Simulation(mV)	237.8±0.125	237.7±0.05
CHIP 1-9(mV)	237.2±0.66	237.59±0.27
CHIP 1-14(mV)	236.81±0.63	237.09±0.35
CHIP 1-16(mV)	236.89±0.77	237.22±0.45

The best case is CHIP 1-9 which derivation is only ±0.66mV and ±0.27mV when temperature range is -40℃~125℃ and 0℃~100℃. Although experimental results are not better than simulation, the voltage derivation has only several milli-Volt at temperature range of -40℃~125℃. Table 4.5 shows experimental results of NPVR. The power is not larger than 120nW, and PSRR is about 20dB. The worst temperature coefficient is 40ppm/℃, and it is not as good as post-layout simulation. Beside measurable error, we need to find out the source of inaccuracy.

Table 4.5: Experimental Results of NPVR

	Simulation	1-9	1-10	1-14	1-16
Voltage supply	0.8v				
Temperature range	-40℃~125℃ 0℃~100℃	-40℃~125℃ 0℃~100℃	0℃~95℃	-40℃~125℃ 0℃~100℃	-40℃~125℃ 0℃~100℃
Temperature coefficient	6.3ppm/ ℃ 3.7ppm/ ℃	33.7ppm/℃ 22.7ppm/℃	33.7ppm/℃	32.25ppm/℃ 29.52ppm/℃	39.4ppm/℃ 37.5ppm/℃
V_{REF}	237.805 237.73	237.2 237.59	237.12	236.81 237.09	236.89 237.21
PSRR	18dB @10MHz	20.2dB @10MHz	20.9dB @10MHz	21.3dB @10MHz	20.8dB @10MHz
Power	83nA	113nA	105nA	102nA	117nA
Area	$0.00088mm^2$				
Tech.	0.18μm				

When measuring V_{REF}, we sometimes measure no value. The source is that NPVR needs a start-up circuit. It can make NPVR work in right situation. The start-up circuit had been illustrated at Chapter 3.

Table 4.6: Process Variation of V_{REF}

-40~125	**M1**	**M2**	**M5**	**M6**
0% variation	0.26mV	0.26mV	0.26mV	0.26mV
1% variation	2.3mV	2.6mV	2.3mV	2mV

We do Monte Carlo Analysis for NPVR, and we discover that process variation is easy to affect M1, M2, M5, and M6, in Figure 4.6. The issue causes that voltage derivation increases a lot, and temperature coefficient of experimental results is not match temperature coefficient of post-layout simulation. We use Monte Carlo analysis which we give 1% variation to simulate M1, M2, M5, and M6, and Table 4.6 shows the result of Monte Carlo analysis. If width and length has no variation, the derivation is 0.26mV when temperature range is -40℃~125℃. However we give width of M1, M2, M5, and M6 1% variation, the derivation of V_{REF} will become from 0.26mV to

2.6mV. The derivation only has several milli-Volt, but temperature coefficient will become from 6.3ppm/℃ to 40 ppm/℃. This might be the source of inaccuracy, and it caused the derivation of V_{REF}.

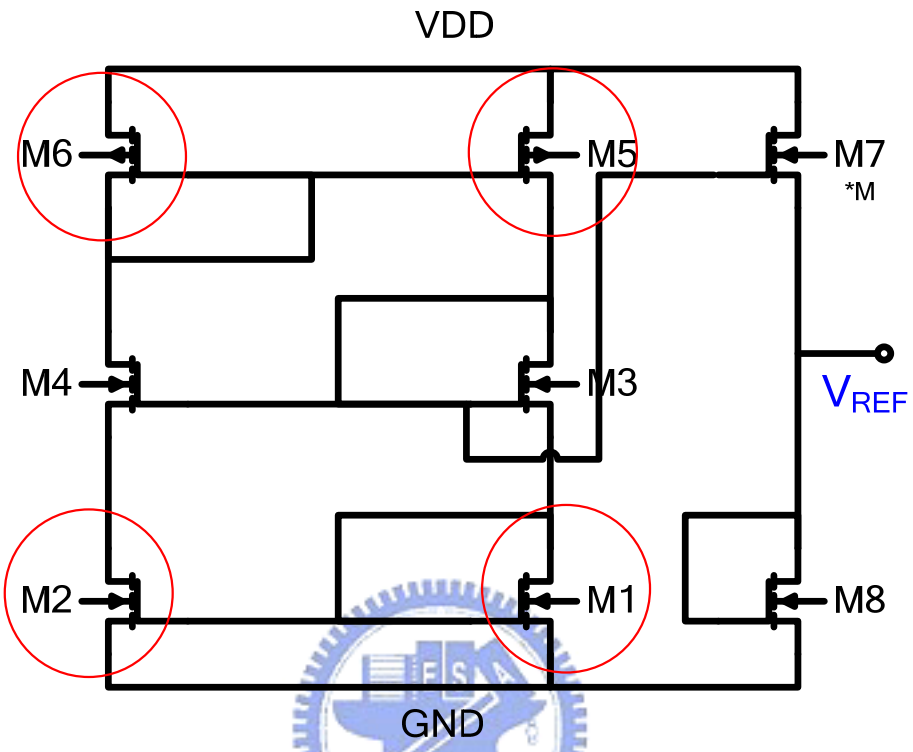


Figure 4.6: Process Variation of NPVR

4.2.3 Discussion of ANVR and NPVR

In Chapter 3, NPCVR uses capacitors which are put in output to increase PSRR. When measuring, we can add a capacitor in output of chip in order to prove the method being useful. See Table 4.7, the measured PSRR of every chips are higher than 54dB, and the results prove the method to be useful.

Table 4.7: PSRR of NPVR (4pF in output)

	Simulation	**1-9**	**1-10**	**1-14**	**1-16**	**average**
PSRR	54dB @10MHz	57dB @10MHz	56dB @10MHz	58dB @10MHz	57dB @10MHz	57dB @10MHz

4.2.4 Comparison of ANVR and NPVR

We have post-layout simulations and experimental results now, so their comparison is shown at Table 4.8. Experimental results are chosen from the best chips as the compared target. We can know that temperature coefficient of measurement is lower than that of simulation. The performance of measurement is not better than that of simulation indeed, but we have illustrated the source at the above section. The next section will compare between experimental results of proposed architectures and researches. Proposed architectures still have many advantages after comparing.

Table 4.8: Comparison of Post Layout Simulation and Experimental results

Proposed Design Architecture	**VDD (V)**	**Temperature Range (℃)**	**Temperature Coefficient (ppm/℃)**	**Derivation (mV)**	**PSRR (dB)**	**POWER (nW)**
ANVR Simulation	0.8	-40~125 0~100	28 16.7	1.65 0.6	7dB @100kHz	403.2
ANVR Measurement	0.8	-40~125 0~100	53.28 37.27	3.2 1.4	11.1dB @100kHz	436
NPVR Simulation	0.8	-40~125 0~100	6.3 3.7	0.25 0.09	18dB @10MHz	83
NPVR Measurement	0.8	-40~125 0~100	33.7 22.7	1.3 0.6	20.2dB @100kHz	113

Table 4.9: Comparison of Taped-out Voltage Reference's Architectures

PAPER (year)	VDD (V)	Temperature Range (℃)	Temperature Coefficient (ppm/℃)	VREF (mV)	Tech. (μm)	AREA (mm^2)	PSRR (dB)	POWER (W)
NPVR	***0.8***	***-40~125 0~100***	***33.7 22.7***	***236.45 236.8***	***0.18***	***0.000888 (37*24)μm²***	***20.2***	***113n***
ANVR	***0.8***	***-40~125 0~100***	***53.28 37.27***	***352.8 353.55***	***0.18***	***0.00108 (30*36)μm²***	***11.1***	***436n***
Voltage Mode of PTAT and CTAT				* is that research has experimental result				
*[1]2004	4.5~5	25~90	347	1320	0.18			
*[2]2005	0.9	0~100	39	514	0.35	0.12	22	780n
*[3]2005	2	0~70	62	579	0.35	0.126	84	4.6u
*[4]2006	0.9~4	0~80	10	670	0.35	0.045	40	63n
Current Mode of PTAT and CTAT								
*[9]2003	1.2	-25~125	119	295	1.2	0.23	40	4.32u
*[10]2006	0.85	-20~120	194	221	0.18	0.0238		3.3u
Voltage Reference Uses Parallel Voltages								
*[21]2003	1.4	0~100	36.9	309	0.6	0.055	20	13.58u
*[22]2004	5	-10~80	32	2670	0.5	0.0936		970u
*[23]2005	1.5	0~80	25	168	0.35	0.08	59	3.6u
*[24]2006	1.5~4.3	0~80	12	891.1	0.35	0.015	59	300n
ZTC								
*[27]2001	3~3.3	-20~100	15	799	0.35	0.0204		
Voltage Reference Uses Non-standard Process								
*[30]2003	1	-50~100	80	410				0.6u
*[31]2004	2.8~5.5	-20~100	54.6	0.8~1.5	0.5	0.081	80	500u
*[32]2005	4.5~9	-40~85	1	1250~5000	1.5	1.6	67	3.15u
*[33]2006	1.2	-60~140	130	400	0.35	0.0022		40u

A comparison of taped-out voltage reference's architectures is shown at Table 4.8. It lists researches of voltage reference which has taped-out in the recent six years and proposed design architectures. See the Table 4.9, proposed architectures have many advantages. First, supply voltage is lower than others. Second, temperature range is the widest range. Third, temperature coefficient is not smaller than others though. But we have illustrated the source in the above section. Forth, the areas of proposed architectures are the smallest. Fifth, power is lower than the most researches, and it

only consumes several hundred nano-Watt. Therefore, it is feasible that proposed architectures can be used in battery-operated systems. And, the performance of proposed architectures is better than the most researches.

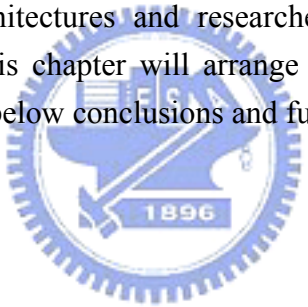
4.3 Summary

The section introduces measurable method and experimental results of proposed design architectures. Then we illustrate the source of bad temperature coefficient, and a comparison is shown and is discussed. But proposed design architectures have many advantages which are low-power, wide temperature range, and low-area. It is more adaptable to use proposed design architectures in battery-operated system. In the next chapter, conclusions will be shown and future works will be illustrated.

CHAPTER 5

Conclusion and Future Works

In the above chapter, experimental results were shown and illustrated. A comparison of proposed architectures and researches is presented after showing experimental results. Now, this chapter will arrange conclusions and future works. And all references are shown below conclusions and future works.



5.1 Conclusion

On the beginning this theis, we review bandgap reference, and a comparison between BJT and CMOS. After illustrating their advantages and disadvantages, we choose CMOS as the device which is used to design voltage reference. In the recent several years, CMOS voltage reference has many different design architectures. They are assorted five types, and the classified basis is the produced method of CMOS voltage reference. After comparison, voltage mode of V_{PTAT} and V_{CTAT} is more suitable than other architectures. Therefore, proposed architectures are designed in accordance with this type.

In this thesis, proposed architectures have been fabricated by TSMC 0.18um 1P6M process technique and they are introduced in chapter 3. We know that proposed architectures have reached successfully several goals. First, **Low Power-** The power consumption of ANVR and NPVR are 403.2nW and 83nW. **Small Area-** The area of ANVR and NPVR are 1080um^2 and 888um^2. **Wide Temperature Range-** The valid

temperature range is from -40℃ to 125℃, and temperature derivation is lower at temperature range from 0℃ to 100℃. **High Accuracy-** Temperature derivation has only several mV at temperature range from 0℃ to 100℃.

Because those goals are accomplished, proposed architectures can apply successfully in battery-operated systems. We can discover that the most demands are better than the goal which was presented in the Chapter 3.1. However, temperature coefficient does not reach the goal. The issue has been illustrated in Chapter 4. Although temperature coefficient is not good enough, the derivation is only several mV. It is sufficient to apply in battery-operated system.

Although proposed architectures have been accomplished the above goals, they still have some problems which need to be improved. In the next section, these issues will be illustrated and discussed.

5.2 Future Works

In this section, we discuss the insufficiencies which need to be improved at proposed architectures. First, process variation is easy to affect voltage reference. Because ALL MOS work in subthreshold region, process variation is very serious. Second, PSRR is lower, and it causes that voltage reference is easy to change with supply voltage. If the issues can be solved, the experimental results will become better.

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