以溶膠-凝膠法製備鎂及鋯離子摻雜之氧化鋅薄膜及薄膜電晶體特性研究

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摘　要

氧化鋅為一 n 型透明之寬能隙(3.2 eV)半導體，在光電元件及平面顯示器領域有極為廣泛之應用。本論文針對溶膠-凝膠法製備鎂及鋯離子摻雜之氧化鋅薄膜及薄膜電晶體之物理及電性做一系列研究與探討。此外，導入高介電之鈦酸鍶鋇閘極絕緣層以提升氧化鋅薄膜電晶體元件之電性，並探討鈦酸鍶鋇薄膜之介面陷阱密度對元件電性之影響。

首先，以溶膠-凝膠法在退火溫度為 500°C 下，製備鎂離子摻雜之氧化鋅薄膜及薄膜電晶體，摻雜濃度介於 0 至 45 mol%之間，探討鎂離子摻雜對氧化鋅薄膜之結晶性、光學特性、晶粒大小以及載子濃度之影響。實驗結果發現鎂離子之摻雜增強氧化鋅薄膜(002)面之結晶方向，並提升薄膜之穿透度。另外以變溫之電容-電壓量測計算出氧化鋅薄膜之費米能階約在傳

導帶下方 0.12 電子伏特。並以曲線配湊方式計算出施體能階約在傳導帶下方 0.3 電子伏特。本研究亦探討鎂離子摻雜濃度對薄膜電晶體電性之影響，發現元件特性與晶粒內能帶之空乏區長度有關。當鎂離子摻雜量為 20 mol%時，元件操作在增強模式且具有 10^6 之開關比。

其次，以相同之溶膠-凝膠法在相同退火溫度製備鋯離子摻雜之氧化鋅薄膜及薄膜電晶體，摻雜濃度介於 0 至 10 mol%間，探討鋯離子之摻雜對氧化鋅薄膜之結晶性、晶粒大小以及表面型態之影響。本研究發現鋯離子摻雜至氧化鋅薄膜後，除了降低氧化鋅薄膜之結晶性，並使晶粒縮小。鋯離子摻雜之氧化鋅薄膜電晶體較未摻雜之氧化鋅薄膜電晶體具備較低之關閉電流及較高之開關比，而電晶體之關閉電流與其半導體載子濃度有關，當鋯離子摻雜至氧化鋅薄膜中，由於縮小薄膜之晶粒，故降低了薄膜之載子濃度，因此抑制了關閉電流。在鋯離子摻雜量為 3 mol%時元件具有最低之關閉電流(3.24×10^{-13} A/μm)及最佳之開關比(8.89×10^6)。

最後，以高介電之鈦酸鍶鋇薄膜作為鋯離子摻雜氧化鋅薄膜電晶體之閘極絕緣層。由於釕酸鋇電極具有與鈦酸鍶鋇相似之晶體結構，故在釕酸鋇電極上成長鈦酸鍶鋇薄膜可具有(110)優選方向，並可降低鈦酸鍶鋇之結晶溫度。而結晶溫度之降低可使鈦酸鍶鋇在較低之成長溫度即具備較高之介電常數及較低之漏電流密度，可符合電晶體元件閘極絕緣層之要求。由於以鈦酸鍶鋇作為電晶體之閘極絕緣層具有較高之閘極電容值，故可將元

件之操作電壓降低至 10 V。此外，鈦酸鍶鋇薄膜亦具備較低之介面陷阱密度，此為提升鋯離子摻雜氧化鋅薄膜電晶體電性之主因。以介電常數為 151 之鈦酸鍶鋇薄膜作為鋯離子摻雜氧化鋅薄膜電晶體閘極絕緣層具有電子遷移率 1.40 cm^2/Vs、臨限電壓 1.45 V 以及 0.61 V/dec 之次臨限斜率。

The Synthesis and Characteristics of Sol-Gel-Derived $Zn_{(1-x)}M_xO$ (M = Mg, Zr) Thin Films and Thin Film Transistors

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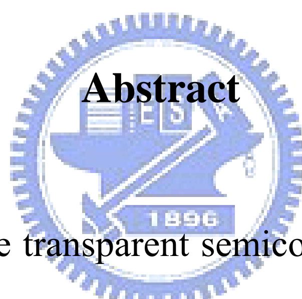

Abstract

ZnO is a normally *n*-type transparent semiconductor with a wide band gap of 3.2 eV and large excition energy of 60 meV, which has been extensively used in optical devices and flat panel displays. In this thesis, the physical and electrical properties of sol-gel-derived Mg and Zr doped ZnO thin films and thin film transistors (TFTs) are proposed and discussed. In addition, the $(Ba,Sr)TiO_3$ high-*k* gate insulators are utilized to improve the electrical characteristics of the devices, and the correlation of interface trap densities of $(Ba,Sr)TiO_3$ between electrical performance of the devices is also investigated.

First, the sol-gel derived *n*-type $Zn_{(1-x)}Mg_xO$ ($x = 0-0.45$) TFTs with active channel layers made of the films were investigated. The films were prepared at 500℃. The effects of Mg doping on the crystallinity, optical transparency, grain

size, and charge-carrier concentration (n) of the films were examined. The Fermi level of the films, as derived from the temperature dependence of n, was ~0.12 eV below the conduction band. The donor concentration and donor level (E_d) were derived by a curve fitting method based on the electrical neutrality condition. E_d was found to be about 0.3 eV below the conduction band. The composition dependence of the TFT output characteristics was interpreted and correlated to the width of the depletion region adjacent to the grain boundaries. When the grains were almost depleted at x = 0.2, the TFT showed an enhancement mode and an on/off ratio of 10^6.

Secondly, we investigated the sol-gel derived $Zn_{(1-x)}Zr_xO$ films and TFTs, where x ranging from 0.00 to 0.10. The effects of Zr additive on the crystallinity, grain size and surface morphology of $Zn_{(1-x)}Zr_xO$ films were discussed. $Zn_{(1-x)}Zr_xO$-TFTs exhibited much lower off-state current (I_{OFF}) and higher on/off ratio than pure ZnO-TFT. The behavior of I_{OFF} related to the carrier concentration (n) of $Zn_{(1-x)}Zr_xO$ films and the correlation between n and grain size were interpreted. The optimized I_{OFF} and on/off ratio of $Zn_{(1-x)}Zr_xO$-TFT were 3.24×10^{-13} A/μm and 8.89×10^6 where x = 0.03, respectively.

Finally, the electrical performance improvements of sol-gel derived $Zn_{0.97}Zr_{0.03}O$ thin-film transistors (TFTs) comprising (Ba,Sr)TiO_3 (BST) high-k gate insulators were also investigated. The (110)-preferentially oriented BST synthesized on $BaRuO_3$ electrodes exhibited enhanced dielectric constants and suppressed leakage currents. Reduced operation voltage and improved electrical characteristics of $Zn_{0.97}Zr_{0.03}O$-TFTs correlated to higher gate capacitance and superior interface trap density (D_{it}) of BST gate dielectrics were interpreted. The optimized mobility (μ_{sat}), threshold voltage (V_{th}) and subthreshold slope (S)

of $Zn_{0.97}Zr_{0.03}O$-TFTs incorporating BST gate insulators with a high dielectric constant of 151 were 1.40 cm^2/Vs, 1.45 V and 0.61 V/dec, respectively.