Anomalous Gate-Edge Leakage Induced by High Tensile Stress in NMOSFET

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***Abstract*—Anomalously high gate tunneling current, induced by high-tensile-stress memorization technique, is reported in this letter. Carrier-separation measurement method shows that the increased gate tunneling current is originated from the higher gate-to-source/drain (S/D) tunneling current, which worsens when channel length is getting shorter. Also, the device with enhanced tensile strain exhibits 9% higher gate-to-S/D overlapping capacitance. These data indicate that the anomalously high gate tunneling current could be attributed to the high tensile strain that induces the effects of excessive lightly doped dopant diffusion and higher gate-edge damage. The proposed inference is confirmed by channel hot-electron stress.**

***Index Terms*—Gate leakage current, MOSFETs, stress memorization technique (SMT).**

I. Introduction

THE INTRODUCTION of stressors to boost mobility has received a lot of attention in recent years. Stressors can be introduced in two key forms, namely, the bases of the substrate strain and the process-induced strain. The substrate-strain-based method makes use of materials with different lattice constants, such as SiGe/Si epitaxial stack to generate biaxial strain in the channel. This method introduces a global strain to the substrate. It effectively boosts mobility at the expense of higher cost [1]. On the other hand, the process-induced strain-based method provides a lower cost solution. It could appear in the forms of shallow trench isolation, contact etch-stop layer, and stress memorization technique (SMT), which introduce uniaxial strain to boost mobility [2]–[5].

The introduction of strain into the channel region not only enhances the mobility of electrons and holes by altering the in-plane mass but also changes the gate tunneling current by altering the out-plane mass and SiO_2/Si barrier height. However, the change of strain will make a great impact on the gate tunneling current [1]. Previous articles have reported the reduction of gate tunneling current by introducing the tensile strain in N-type metal–oxide–semiconductor field-effect transistor (NMOSFET) [2], [6]. In the course of boosting NMOSFET mobility using SMT with high tensile strain, the gate tunneling current was also found to be increased at the same time. This is particularly evident when the channel is driven into the accumulation mode. This observation is rather different from previous reports. In this letter, two possible factors will be investigated to analyze the anomalously high gate tunneling currents. One is the strain-induced excessive lateral dopant diffusion, and the other is the strain-induced polysilicon gate damage at the edges.

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II. Experiment

The NMOSFET used in this letter was fabricated using state-of-the-art CMOS processes. The device went through the gate dielectric, gate poly, and spacer and source/drain (S/D) formation [7]–[9]. The lightly doped diffusion (LDD) and S/D regions were implanted with arsenic and phosphorous, respectively. High-tensile-SMT film is then deposited, followed by high-temperature activation treatment. Process details can be found elsewhere [5]. Two NMOSFETs (Sample A and Sample B) with different strain levels were compared to investigate the effect of strain on gate tunneling current. Sample A is having a higher tensile strain than Sample B. Keithley 4200 Semiconductor Characterization System and Agilent 4294 Precision Impedance Analyzer are the key instruments used to extract various device parameters.

III. Results and Discussion

The electrical characteristics of NMOSFET devices studied in this letter show that Sample A (with higher tensile strain) has approximately 4% higher mobility than Sample B (with lower tensile strain). The sample with higher strain also exhibits a higher drain leakage current (I_d-off) at the OFF state. This is particularly evident when the device is biased at a linear mode ($V_d = 0.05$ V). Electrical measurement shows that the higher I_d-off is mainly contributed from the higher gate tunneling current.

Carrier-separation measurement was performed to identify the source and the type of carriers tunneling through the gate dielectric [10]. The gate tunneling current is plotted as a function of gate bias (V_g) in Fig. 1. From this plot, the measured gate current could be divided into two distinctive regions. For the low V_g region, Sample A exhibits a much higher J_g than Sample B. As V_g increases, the difference in J_g diminishes.

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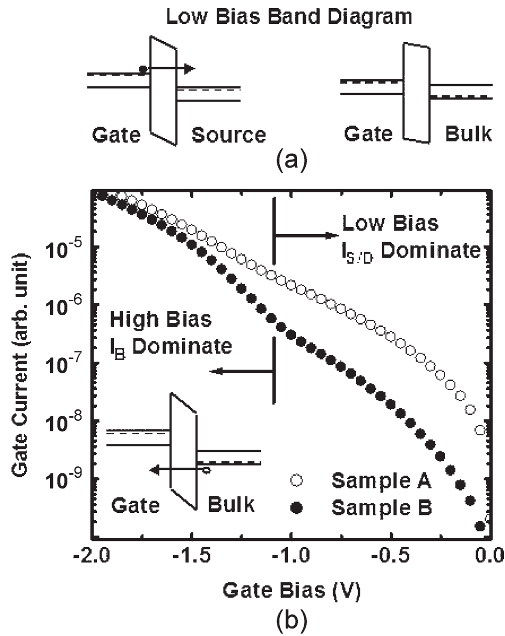

Fig. 1. Plot of gate current density (J_g) against the gate biases, extracted from carrier-separation measurement. Sample A with higher tensile strain exhibits an anomalously high electron tunneling current $(I_{\mathrm{S/D}})$ at the low V_g region. (a) Gate-to-S/D is having a greater band bending than gate-to-bulk under low V_g biasing. This explains the dominance of electron current under the low V_g region. The inset of (b) shows band bending under the higher V_g region. The hole current from the bulk region dominates the gate current.

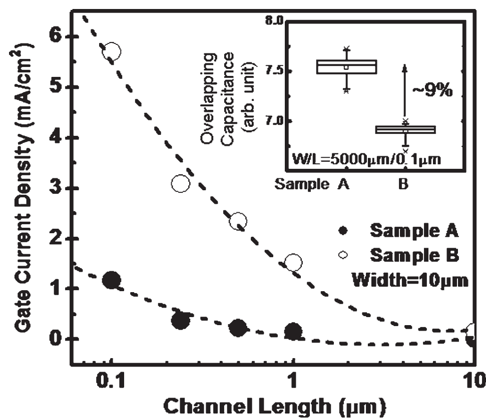

Fig. 2. Dependence of J_g on device channel length. The gate tunneling current increases as channel length becomes shorter. This result could be attributed to the increase of $I_{\mathrm{S/D}}$ component as the channel length is getting shorter. The insert shows the gate-to-S/D overlap capacitance. It could be attributed to the strain-induced excessive lateral diffusion of dopants in the LDD region.

Carrier-separation measurement shows that electron and hole tunneling currents dominate at low and high gate biasing regions, respectively. At the low biasing region, the gate tunneling current flows primarily to the S/D regions. Sample A is found to exhibit a higher gate tunneling current than Sample B. This could be originated from the different tensile strain. It has been reported that tensile strain from an SMT is obvious, specifically at the gate edge [6], [11]. Therefore, it is reasonable to deduce that the anomalously high gate tunneling current in Sample A is a result of higher tensile strain.

Fig. 2 shows the gate tunneling current of NMOSFET devices as a function of channel lengths. Devices were biased at an accumulation mode. For simplicity, the gate tunneling current density was extracted at $V_g = -0.75$ V and shown in Fig. 2. The results show that the gate tunneling current is a strong function of channel length. As the channel length is decreased, the impact from strain becomes more evident. The mechanical stress induced by SMT is not only originated from the vertical compressive strain or restraining polysilicon gate from the regrowth process, but it also comes from the tensile strain experienced by the S/D regime (SMT). This means that the tensile strain effect can be enhanced by both the high level of strained SMT film and channel length scaling [12], [13]. According to the experimental results, as shown in Fig. 2, the impact of SMT on gate tunneling current is significant for the NMOSFET with high-tensile-SMT film and short channel.

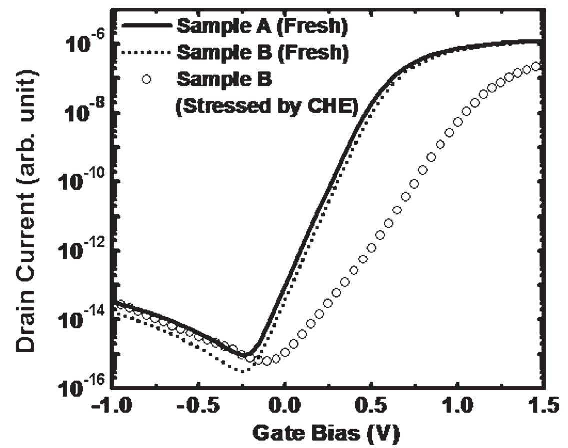

Fig. 3. Linear-mode transfer characteristics for both Sample A and Sample B. Sample A with a higher tensile strain exhibits a higher I_d-off. Sample B subjected to 1000-s CHE stress (at $V_g = V_d = 2.2$ V) has a I_d-off increase to a level similar to that of Sample A. The results indicate that the OFF-state drain current will be increased by mechanical and electrical stresses.

On the other hand, it is also observed that Sample A is having approximately 9% higher gate-to-S/D overlapping capacitance than Sample B, as shown in the inset of Fig. 2. Excessive strain was reported to induce point defects, such as interstitials and vacancies in silicon. The presence of these defects assists dopant diffusion. Hence, both the tensile and compressive strain would influence the dopant diffusion behavior [14], [15]. In our samples, the LDD was implanted with arsenic. The presence of higher tensile strain in Sample A could enhance the lateral arsenic diffusion. This reasonably explains why Sample A is having a higher gate-to-S/D overlapping capacitance. The change in overlapping capacitance also increases gate tunneling current at the gate edge.

Fig. 3 shows the transfer characteristics of Sample A and Sample B in the linear mode, at a drain voltage of 0.05 V. The drain current of Sample A is higher than that of Sample B in the OFF state. The threshold voltage of Sample A is slightly lower than that of Sample B. These results could be attributed to the effects of strain-induced mobility increment and strain-induced lateral LDD dopant diffusion, which shortens the effective channel length further. In Fig. 3, Sample B was also intentionally subjected to 1000-s channel hot-electron (CHE) stress to create damage at the proximity of the gate edge.

Following the CHE stresses, threshold voltage shifts positively with degradation in subthreshold swing. During hot-carrier stress, hot electrons were injected into the gate dielectric and create interface traps [16], [17]. Compared with the fresh Sample A without stress, the stressed device produces an increased OFF-state drain current (I_d-off), indicating that I_d-off increases when the gate edge is damaged. This verifies our inference that an excessive tensile strain at the gate edge will damage the gate edge and cause higher I_d-off.

IV. Conclusion

This letter has shown that SMT boosts the electrical performance of NMOSFET, but the gain was achieved at the expense of a higher gate tunneling current at the OFF state. Carrier-separation measurement shows that the increased gate tunneling current is originated from the higher gate-to-S/D tunneling current, which worsens as the channel length is scaling down. Excessive strain degrades gate tunneling current via the following two factors: 1) excessive lightly doped dopant diffusion and 2) gate-edge damage. This was verified from the higher gate-to-S/D overlapping capacitance and the hot-carrier stress study.

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