Optimal Design of Triple-Gate Devices for High-Performance and Low-Power Applications

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***Abstract*—Pragmatic design of triple-gate (TG) devices is presented by considering corner effects, short-channel effects, and channel-doping profiles. A novel TG MOSFET structure with a polysilicon gate process is proposed using asymmetrical (n^+/p^+) polysilicon gates. CMOS-compatible V_T's for high-performance circuit applications can be achieved for both nFET and pFET. The superior subthreshold characteristics and device performance are analyzed and validated by 3-D numerical simulations. Comparisons of device characteristics with a midgap metal gate are presented.**

***Index Terms*—Corner effects, polysilicon gate, triple-gate (TG) MOSFETs.**

I. Introduction

THE TRIPLE-GATE (TG) MOSFET (Fig. 1) has emerged as one of the promising candidates to extend CMOS technology beyond the scaling limit of conventional CMOS technology. The control of short-channel effects (SCEs) has become one of the major issues for device scaling beyond the 65-nm node [1]. Several emerging planar and nonplanar structures that aimed to alleviate the SCEs have been proposed [1]. In these devices (e.g., fully depleted SOI MOSFETs, double-gate (DG) FinFETs, and TG MOSFETs), thin silicon film is usually required, yet challenging, to suppress the SCEs. The DG FinFET (with ultrathin fin) exhibits superior SCE control and current drive. On the other hand, the TG FET relaxes the requirements on fin height and fin (silicon film) thickness, thus allowing more flexible body dimension and fin aspect ratio to ease manufacturability [2]–[4].

However, the mobile carrier density of the TG device is higher in the corner than the other portions of the channels at low gate voltage due to high electric field at sharp edges, which degrades the subthreshold slope. Furthermore, the corner effects are more significant at high channel doping levels, thus directly affecting the device profile design [3], [5], [6]. As a result, low doping levels would seem to be a natural solution. Thus, conventional technique using channel doping to adjust the threshold voltage (V_T) could be limited. In fact, metal gates with proper work functions, instead of channel doping engineering, have been employed to achieve the desired V_T in advanced multigate structures [7]–[9]. For CMOS application, two different work functions are usually required in order to balance the drive currents of nFET and pFET, which leads to technology complexity. In addition, gate work function engineering for multi-V_T design requires more exotic gate materials.

In this paper, we present pragmatic TG device design considerations with emphasis on the feasibility of polysilicon gate and the choice of nonrectangular body structure while accounting for the noted corner effects using 3-D numerical simulations [10]. In the simulations, Fermi–Dirac statistics, modified local density approximation for carrier confinement, and drift-diffusion transport model with field-dependent mobility are used. Impacts of corner rounding and body-doping profiles on SCEs and other device characteristics are investigated. We also compare the nonrectangular structures with the ideal case of rectangular corners. Another challenging task for the multigate

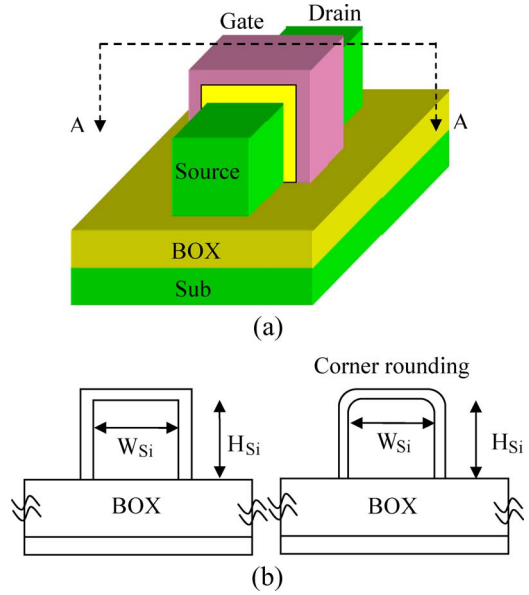

Fig. 1. (a) Three-dimensional TG structure (not to scale). (b) Two-dimensional cross sections ($A-A$) of the TG device with rectangular and rounded corners.

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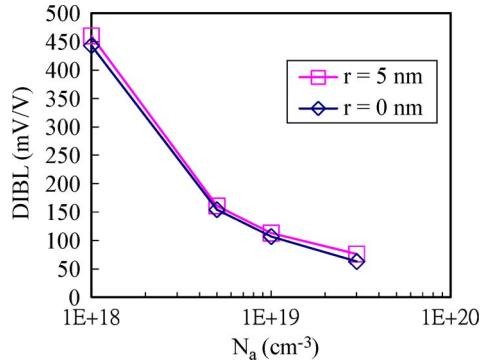


Fig. 2. Predicted DIBL versus body doping for different radii of corner curvature ($H_{\rm Si} = 25$ nm, $W_{\rm Si} = 25$ nm, and L(effective) $= 25$ nm).

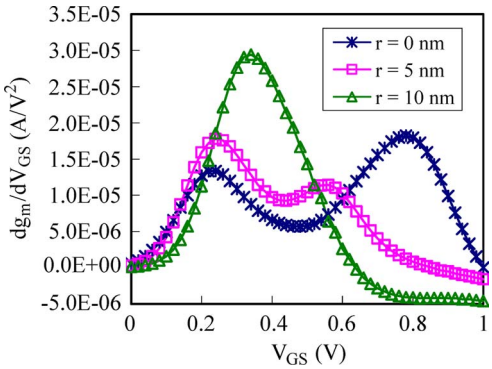


Fig. 3. Predicted $\mathrm{d}g_m/\mathrm{d}V_{\rm GS}$ versus $V_{\rm GS}$ for different radii of corner curvature at $N_a = 3 \times 10^{19}$ cm^{-3} ($V_{\rm DS} = 0.05$ V)($H_{\rm Si} = 25$ nm, $W_{\rm Si} = 25$ nm, and L(effective) $= 25$ nm).

technology development is the gate engineering for setting proper V_T. To facilitate the use of polysilicon gate material, we propose an asymmetrical ($\mathrm{n}^+/\mathrm{p}^+$) poly-gate structure for TG FinFET devices with CMOS-compatible V_T's using tilted implantations [11], [12]. Note that in [12], tilted implantations have been employed to the fabrication of asymmetrical DG FinFET devices with CMOS-compatible V_T's. In the following sections, the device characteristics of the proposed structure are comprehensively analyzed. Comparisons of device characteristics with a midgap metal gate are presented.

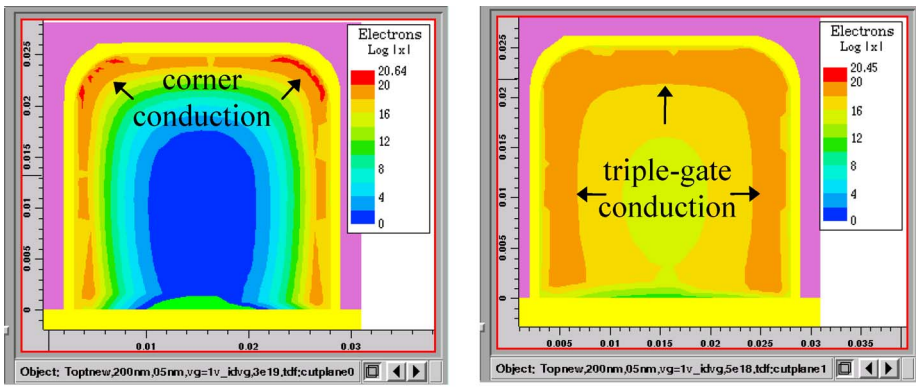
II. Conventional Device Structure With Midgap Gate

The device structure under study (Fig. 1), with midgap gate, has a cross-sectional body dimension of $H_{\rm Si} = 25$ nm and $W_{\rm Si} = 25$ nm, L(effective) $= 25$ nm, gate-oxide thickness (physical) $= 1$ nm, and buried oxide thickness $= 200$ nm. We first examine the control of SCEs via doping profile design with corner-rounding effects. Fig. 2 shows DIBL versus body doping for different radii of corner curvature r for the top corners. Due to higher transverse electric field at sharp edges of the ideal rectangular case, implying better SCE control, it shows slightly lower DIBL than the nonrectangular case (e.g., DIBL $=$ 154 and 161 mV/V for $r = 0$ (ideal) and 5 nm, respectively, at $N_a = 5 \times 10^{18}$ cm^{-3}), but the difference is insignificant. The noncritical effect of corner rounding on SCE eases the rectangular body requirement in TG technology. However, very high doping appears necessary in order to suppress DIBL ($<$ 100 mV/V). This is technologically challenging, and the performance tradeoff requires thorough study, as the silicon body could become partially depleted, causing floating-body effects, and the junction tunneling leakage could also become an issue at high body doping.

Fig. 3 shows the impact of corner rounding at very high doping ($N_a = 3 \times 10^{19}$ cm^{-3}) on g_m variations. Evidently, the bimodal (two peaks) behavior reveals the two distinct V_T's associated with the corners and the top/sidewalls, respectively. The corners, corresponding to the first peak, turn on earlier due to high electric fields at sharp edges. For nonrectangular case ($r = 5$ nm), the two peaks are closer since the sharp-edge effects are alleviated. As shown in Fig. 4(a) ($r = 5$ nm), the corner conduction is not as predominant since electron concentration is well distributed around the rounded corners instead of crowded at sharp edges. For the near-cylindrical case ($r = 10$ nm), the sharp-edge effects almost diminish completely. For moderately high $N_a(5 \times 10^{18}$ cm$^{-3})$, the bimodal behavior in V_T virtually disappears as the electron density is quite uniform around the corners, top, and sidewalls, as shown in Fig. 4(b), where the three sides of the gate conduct simultaneously.

Due to technology simplicity, the TG device with undoped or lightly doped body is preferred. Nonetheless, in this case, the DIBL would be unacceptably high with the same device size used for high body doping. Rather than adjusting the doping, ratios of $W_{\rm Si}$ and $H_{\rm Si}$ to channel length must be reduced to achieve good SCEs [3]. Here, we reduce $W_{\rm Si}$ and $H_{\rm Si}$ to half of the channel length for proper DIBL (73 mV/V).

Due to different inversion conditions for heavily doped body and lightly doped body, device structure with corner rounding can be optimized to improve performance. In the subthreshold regime, the lightly doped case is predominantly affected by volume inversion, whereas corner inversion is the main contribution to $I_{\rm off}$ for the heavily doped case. Therefore, corner rounding has very little impact on $I_{\rm off}$ for devices with lightly doped body. In strong inversion, corner and edge inversions become more significant regardless of body doping, and hence, the shape of corners will have an impact on $I_{\rm on}$. Fig. 5 shows $I_{\rm eff}$ (the effective current during switching [13]) versus body doping for different radii of corner curvature. For the very high N_a, we observe that $I_{\rm eff}$ increases with r due to additional top/sidewall conduction in strong inversion regime as the second peak (top/sidewall conduction) in Fig. 3 moves toward lower $V_{\rm GS}$ and eventually merges with the first peak (corner conduction). As a result, all edges, top, and sidewalls conduct simultaneously, resulting in a higher current. Thus, semicylindrical (tubelike) body would be preferable to improve performance without the sharp-edge effects. Note that since the body dimension of the low $N_a(1 \times 10^{16}$ cm$^{-3})$ case is half that of the other two higher N_a cases, it has the highest effective $I_{\rm on}$ per unit device width and the best CV/I due to inherent advantages such as higher mobility and steeper subthreshold slope from gate-to-gate capacitive coupling. Volume inversion also improves the subthreshold slope (the benefit reduces as doping increases). Contrary to the heavily doped case, the rectangular corners ($r = 0$ nm) seem advantageous to $I_{\rm on}$ for the low N_a case as the high electric fields at sharp edges facilitate volume



(a) (b)

Fig. 4. Simulated electron density in the channel (cut at the midpoint between source and drain) for $r = 5$ nm at (a) $N_a = 3 \times 10^{19}$ cm^{-3} and (b) $N_a = 5 \times 10^{18}$ cm^{-3} ($V_{GS} = 1.0$ V and $V_{DS} = 0.05$ V) ($H_{Si} = 25$ nm, $W_{Si} = 25$ nm, and L(effective) $= 25$ nm).

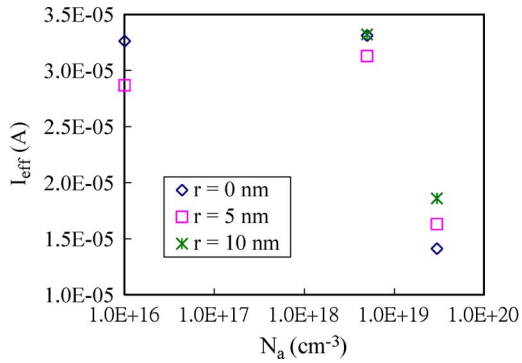


Fig. 5. Predicted I_{eff} versus body doping for different radii of corner curvature with comparable I_{off} for all cases where $I_{eff} = [(I_{DS}$ at $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}/2) + (I_{DS}$ at $V_{DS} = V_{DD}$ and $V_{GS} = V_{DD}/2)]/2$ [13]. Because $r = 10$ nm is too large for reduced W_{Si} and H_{Si} at $N_a = 1 \times 10^{16}$ cm^{-3}, it is not included.

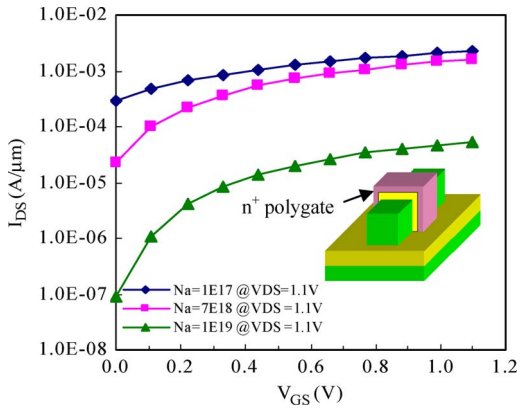


Fig. 6. Taurus-simulated I_{DS} versus V_{GS} characteristics for a TG nMOSFET with n^+ polysilicon gate and different dopings (N_a's) ($L = 25$ nm, gate oxide $= 1.3$ nm, and silicon height $=$ silicon width $= 12.5$ nm).

inversion and introduce additional corner conduction in strong inversion.

III. Proposed Device Structure

A novel TG FinFET structure compatible with the polysilicon process is proposed. Although the lightly doped channel seems to be a viable option and even preferable due to doping-dependent mobility, it is limited to the availability of midgap gates for CMOS application. In the conventional dual polysilicon CMOS technology (i.e., n^+ and p^+ polysilicon for nFET and pFET, respectively), the required channel doping density for TG devices has to be extremely high to achieve proper V_T ($\sim$0.2 V) and, hence, I_{off} (100 nA/μm), as shown in Fig. 6. The proposed TG device structure with physically equivalent n^+- and p^+-polysilicon gates is shown in Fig. 7(a). Two other possible structures with n^+/p^+ polysilicon gate offsets are shown in Fig. 7(b) and (c). The gate oxide surrounded by the gate has a uniform thickness (T_{ox}). The device structure under study has a cross-sectional body dimension of height (H_{Si}) and width (W_{Si}). H_{Si} and W_{Si} are assumed to be equal and are half of the effective channel length for proper SCE control. The total channel width can be defined as $2H + W$. Multi-V_T options can be achieved using different patterns of the n^+/p^+ polysilicon. It is worth noting that as high-k metal gates are

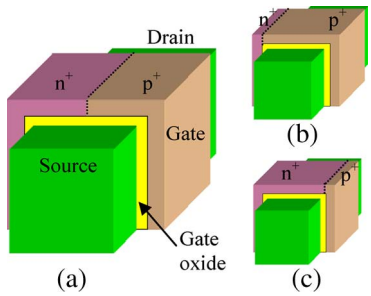


Fig. 7. Three-dimensional view of the proposed TG structures (a), (b), and (c) with different n^+/p^+ polysilicon gate offsets. The thick BOX layer underneath is not shown.

used in planar CMOS technologies from the 45-nm node, the possible difficulty in high-k integration with polysilicon gates and random dopant fluctuation, although not included in this paper, could be potential issues to be resolved for polysilicon gates to remain viable as semiconductor technology advances.

We first assess the device I–V characteristics for the three gate structures, as compared with a midgap metal-gate device using 3-D numerical simulations [10]. All devices (nFETs) have the same L of 25 nm, T_{ox} of 1.3 nm, and thick buried oxide (BOX) of 200 nm. Fig. 8 shows the simulated I_{DS} versus V_{GS} characteristics for the proposed structure (a) and the midgap metal-gate device with comparable I_{off}($\sim$50 nA/μm) set at

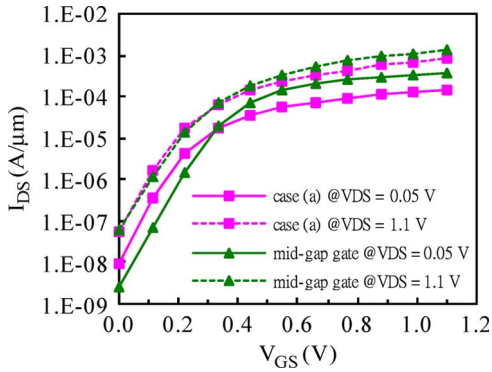


Fig. 8. Taurus-simulated I_{DS} versus V_{GS} characteristics for the proposed structure (a) and the midgap metal-gate device with comparable I_{off} (~50 nA/μm) set at $V_{DS} = 1.1$ V.

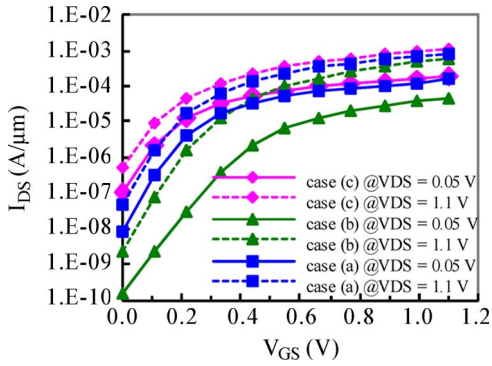


Fig. 9. Taurus-simulated I_{DS} versus V_{GS} characteristics for the three proposed structures.

$V_{DS} = 1.1$ V. To achieve equal I_{off} value, a channel doping density of 7×10^{18} cm^{-3} is needed for the proposed structure, whereas an undoped body is used for the near-midgap metal-gate device. Due to higher mobility in the undoped channel, the midgap metal-gate device gives higher I_{on} (at $V_{GS} = V_{DS} = 1.1$ V). On the other hand, the proposed device exhibits better DIBL characteristics due to the higher vertical field attained by the positive back-gate field in the asymmetrical device configuration as well as the use of the doped body. Fig. 9 shows the simulated I_{DS} versus V_{GS} characteristics for the three cases with different n^+/p^+ polysilicon gate offsets, as shown in Fig. 7. The same channel doping density (7×10^{18} cm^{-3}) is used. Case (b) with larger p^+-polysilicon portion has the highest V_T, whereas case (c) with larger n^+-polysilicon portion has the lowest V_T. Fig. 10 further shows the I_{on} versus I_{off} characteristics for the three poly-gate and the metal-gate devices. The three proposed structures offer a wide range of V_T selection; thus, multiple V_T's can be made. Note that for the DG FinFET structure, the proposed multi-V_T technique via partitioned n^+/p^+ polysilicon on the top gate would not be practical because the top-gate area of FinFET is too narrow and, thus, ineffective.

The detailed device characteristics are listed in Table I ($V_{DD} = 1.1$ V). The proposed structures have lower DIBL and better subthreshold slope compared with the metal-gate device. Fig. 11 shows the inversion carrier distribution in the channel. The electron density is more uniformly distributed for the midgap metal-gate device, whereas it is crowded near

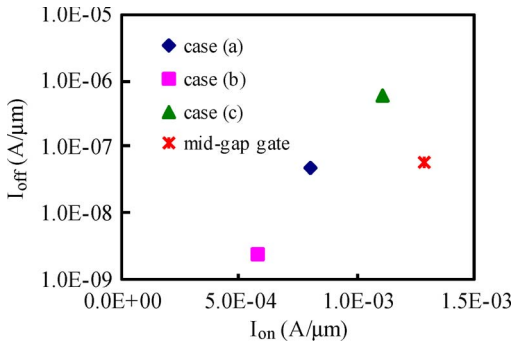


Fig. 10. I_{on} versus I_{off} for the proposed structures and the near-midgap metal-gate device.

TABLE I
PREDICTED DEVICE CHARACTERISTICS OF THE PROPOSED STRUCTURES AND THE MIDGAP METAL-GATE DEVICE FOR COMPARISON

Device type	Mid-gap gate	Case (a)	Case (b)	Case (c)
$V_{T(sat)}$ (V) [a]	0.16	0.15	0.27	0.08
I_{off} (A/μm)	5.76×10^{-8}	5.16×10^{-8}	2.52×10^{-9}	5.34×10^{-7}
I_{on} (A/μm)	1.29×10^{-3}	8.05×10^{-4}	5.80×10^{-4}	1.05×10^{-3}
I_{eff} (A/μm) [13]	7.77×10^{-4}	4.74×10^{-4}	3.05×10^{-4}	6.40×10^{-4}
DIBL (mV/V)	101	50	82	54
Sub. Swing (mV/dec)	90	81	79	89
CV/I_{on} (normalized)	1	1.49	2.00	1.20

[a] $V_{T(sat)}$ was extracted by constant current method (0.1 μA x (W/L) at $V_{DS} = V_{DD}$).

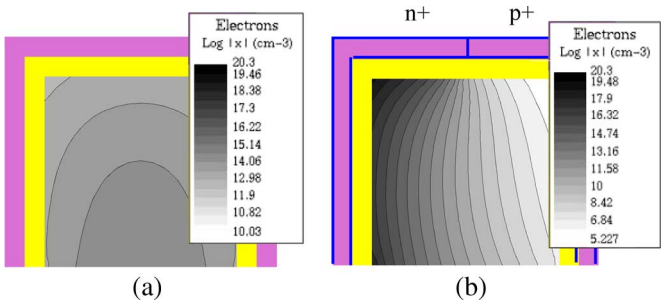


Fig. 11. Electron distribution in the cross-sectional cut at midchannel for (a) the midgap metal-gate device and (b) the proposed structure (a) ($V_{GS} = V_{DS} = 0$ V).

the n^+-gate surface for the proposed structure (a) (results for structures (b) and (c) are not shown, yet similar). Hence, the proposed structures have improved DIBLs, as the carriers are better controlled due to the higher field perpendicular to the predominant n^+ gate.

Fig. 12 shows the I_{on} and I_{off} sensitivities to V_{DD}. As expected, I_{off} for structure (a) is slightly less sensitive than that for the midgap metal-gate device due to less DIBL. The I_{on} dependences on V_{DD} are similar for the three proposed structures, implying consistent dynamic power scaling when these structures are integrated on the same chip for multi-V_T design. The DIBL advantage is further shown in Fig. 13. To gain insight into CMOS circuit speed performance, we also

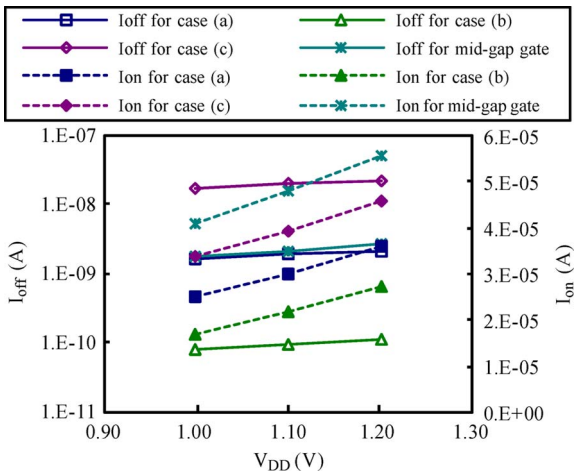


Fig. 12. Predicted $I_{\rm on}$ and $I_{\rm off}$ sensitivities to $V_{\rm DD}$.

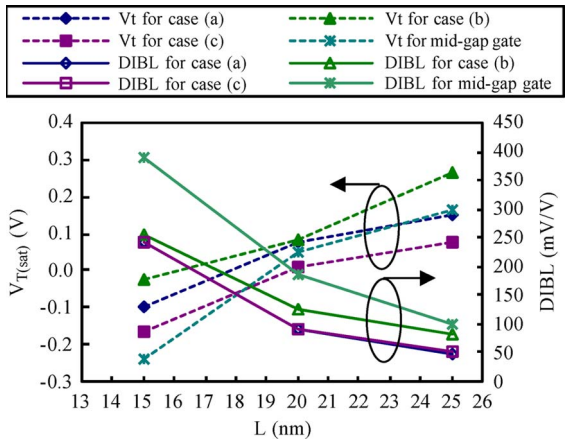


Fig. 13. Predicted $V_{\rm T(sat)}$ and DIBL versus L scaling.

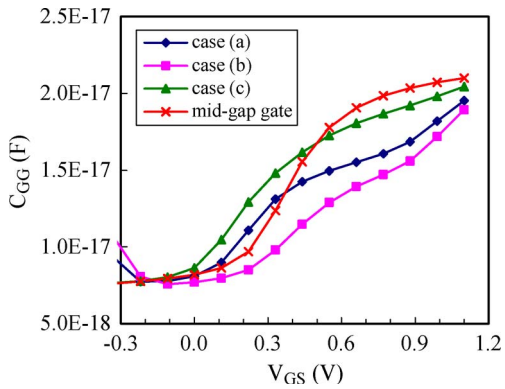


Fig. 14. Predicted C–V characteristics.

simulated C–V characteristics, as shown in Fig. 14, for CV/I comparison. The $CV/I_{\rm on}$ value of our proposed structure [case (a)] is about 50% (at $V_{\rm DD}$ of 1.1 V) higher than that of the midgap metal-gate device mainly due to lower $I_{\rm on}$. However, as $V_{\rm DD}$ is decreased, the gate capacitance for the proposed scheme decreases faster, and hence, it is more suitable for low-voltage applications. Overall, while the CV and IV performances of the proposed structure are not superior partly due to lower channel mobility at higher substrate doping, it can be more aggressively scaled and more suitable for low $V_{\rm DD}$ and sub-V_T applications.

IV. Conclusion

The impacts of corner rounding in TG MOSFETs on DIBL and device characteristics were analyzed via 3-D numerical simulations. Properly rounded corners of TG device can improve SCEs or increase drive current. Semicylindrical gate structure is preferable for heavily doped devices, whereas rectangular gate structure appears better for lightly doped devices.

A novel TG MOSFET structure using asymmetrical polysilicon gates is proposed. Due to the superior SCEs, the proposed TG device offers better channel length scalability compared with the TG devices with near-midgap metal gates. By changing the patterns/offsets of the n^+/p^+ polysilicon gates, multiple V_T's can be achieved, thus making it attractive for low-power high-performance very large scale integration applications.

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