# Discrete Dopant Fluctuations in 20-nm/15-nm-Gate Planar CMOS

Yiming Li, *Member, IEEE*, Shao-Ming Yu, Jiunn-Ren Hwang, and Fu-Liang Yang

***Abstract*—We experimentally quantified, for the first time, the random dopant distribution (RDD)-induced threshold voltage $(V_t)$ standard deviation up to 40 mV for 20-nm-gate planar complementary metal–oxide–semiconductor (CMOS) field-effect transistors. Discrete dopants have been statistically positioned in the 3-D channel region to examine the associated carrier transportation characteristics, concurrently capturing "dopant concentration variation" and "dopant position fluctuation." As the gate length further scales down to 15 nm, the newly developed discrete dopant scheme features an effective solution to suppress the 3-sigma-edge single-digit dopant-induced $V_t$ variation by the gate work function modulation. The results of this paper may postpone the scaling limit projected for planar CMOS.**

***Index Terms*—Complementary metal–oxide–semiconductor (CMOS) device, dopant concentration variation, dopant position fluctuation, random dopant distribution (RDD), threshold voltage fluctuation, 3-D modeling and simulation.**

## I. Introduction

IT IS KNOWN that gate length scaling is still the most effective way to continue Moore's law for transistor density increase and chip performance enhancement [1]–[3]. However, as the planar complementary metal–oxide–semiconductor (CMOS) field-effect transistor advances to sub-20-nm gates, double-digit channel dopants make transistor behaviors more complicated to be characterized with conventional "continuum modeling" because every "discrete" dopant has its significant weight impacting the resulting transistor performance. The random nature of discrete dopant distribution results in significantly random fluctuations, such as the deviation of threshold voltage $(V_t)$, drive current mismatch, and so on [3]–[14]. The fluctuation budget has to be controlled even tighter due to the doubly increased transistor number along with technology node moving ahead. Unfortunately, the fluctuation is intrinsically increased with the scaling of transistor feature size, not even considering the worsened short channel control [3].

Without loss of generality, the fluctuation can be decomposed into three components: one is resulting from the random dopant distribution (RDD) [3]–[8], [10]–[14]; and the others are due to the mean gate length deviation (GLD) and the line edge roughness (LER) [3], [4], [6], [8], [9]. The mean GLD and the LER mainly resulted from issues associated with resolution and granularity of lithography. The RDD-induced fluctuation is due to the random nature of ion implantation. Various random dopant effects have been recently studied in both experimental and theoretical approaches [4]–[8], [10]–[14]. These studies have shown that the fluctuation of electrical characteristics is not purely a result of a variation in average doping density associated with a fluctuation in the number of dopants but also the particular random distribution of dopants in the channel region. In this paper, we are absorbed in the random dopant effect and herein developed a systematic method to experimentally extract the RDD-induced $V_t$ fluctuation. We have, for the first time, experimentally quantified the RDD-induced threshold voltage standard deviation up to 40 mV for 20-nm-gate planar CMOS. Discrete dopants have been statistically positioned in the 3-D channel region to examine the associated carrier transportation characteristics, concurrently capturing "dopant concentration variation" and "dopant position fluctuation." Therefore, a 3-D "atomistic" device simulation, in good agreement with the experimental data, has been carried out to realize statistical analysis and to feature solutions for reducing the RDD-induced $V_t$ variation upon gate length $(L_g)$ scaling. As the gate length of CMOS devices further scales down to 15 nm, the developed approach also suggests a solution to suppress the 3-sigma-edge single-digit dopant-induced $V_t$ variation by gate work function modulation. We believe that the study may postpone the scaling limit projected for nanoscale CMOS devices.

This paper is organized as follows. In Section II, we state the experiment and simulation. In Section III, we show the results and discuss comparison between the measurement and simulation. Finally, we draw conclusions.

## II. Experiment and Simulation Technique

Threshold voltage is one of the key device parameters in the characteristics of nanoscale metal–oxide–semiconductor field-effect transistors (MOSFETs). As the mean GLD, LER [3], [4], [6], [8], [9], and RDD [3]–[8], [10]–[14] are the major variation sources of threshold voltage, we can thus extract the RDD-induced standard $V_t$ deviation $\sigma V_{t,\mathrm{RDD}}$ from the following

Manuscript received August 27, 2007; revised January 23, 2008. This work was supported in part by the National Science Council of Taiwan under Contract NSC-96-2221-E-009-210, Contract NSC-95-2221-E-009-336, and Contract NSC-95-2752-E-009-003-PAE, in part by the MoE ATU Program under a 2006–2007 Grant, and in part by the Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C., under a 2006–2008 Grant. The review of this paper was arranged by Editor H. S. Momose.

Y. Li is with the Department of Communication Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: ymli@faculty.nctu.edu.tw).

S.-M. Yu is with the Department of Computer Science, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

J.-R. Hwang and F.-L. Yang are with the Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan, R.O.C.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2008.921991

0018-9383/$25.00 © 2008 IEEE

approximated equation as $\sigma V_{t,\,\mathrm{total}}$ and $\sigma V_{t,\,\mathrm{GLD\&LER}}$ can be directly measured from the experimental data [3]:

$$(\sigma V_{t,\,\mathrm{total}})^2 \approx (\sigma V_{t,\,\mathrm{GLD\&LER}})^2 + (\sigma V_{t,\,\mathrm{RDD}})^2 \qquad (1)$$

where $\sigma V_{t,\,\mathrm{total}}$ is the total standard $V_t$ deviation, and $\sigma V_{t,\,\mathrm{GLD\&LER}}$ is the $V_t$ fluctuation contributed from the mean GLD and LER. Using the $V_t$ rolloff relation [15] $\sigma V_{t,\,\mathrm{GLD\&LER}} = (dV_t/dL_g) \times \sigma L_g$, $\sigma V_{t,\,\mathrm{GLD\&LER}}$ can be extracted with the experimental data of $V_t$ rolloff and standard GLD $\sigma L_g$. Thus, from the experimentally measured $\sigma V_{t,\,\mathrm{total}}$ and extracted $\sigma V_{t,\,\mathrm{GLD\&LER}}$, we can calculate $\sigma V_{t,\,\mathrm{RDD}}$ according to (1). We notice that for data with large $\sigma V_t$, the $I_{\mathrm{on}}$–$I_{\mathrm{off}}$ distribution is scattering. However, it can still be analyzed and well fitted by (1). $\sigma L_g$ is obtained from scanning electron microscope critical dimension measurements.

In this paper, an excellent short-channel-effect control down to 20-nm gate has been experimentally realized with advanced shallow junction technology. We achieve a junction depth of around one-half of the gate length to maintain the subthreshold leakage at 100 nA/$\mu$m with channel doping $\approx$ 5E18 cm$^{-3}$ and gate dielectric of 12 A$^\circ$ equivalent oxide thickness (EOT). Furthermore, to have the insights of RDD effects, quantum mechanical transport simulation is performed and compared with experimental data by solving a set of calibrated 3-D density–gradient equation coupling with Poisson equation as well as electron–hole current continuity equations [11], [15]–[17]. The 3-D device simulation was calibrated against the nonequilibrium Green's function simulation for planar MOSFETs [17]–[19]. All the statistically generated discrete dopants, as shown in Fig. 1 (details in the next paragraph), are advanced and incorporated into the 3-D device simulation under our parallel computing system [16]. Such large-scale simulation approach allows us to explore the electrical characteristic fluctuations concurrently induced by the randomness of dopant number and the position in the channel region. The mobility model used in the device simulation, according to Mathiessen's rule [20], [21], can be expressed as

$$\frac{1}{\mu} = \frac{D}{\mu_{\mathrm{surf_aps}}} + \frac{D}{\mu_{\mathrm{surf_rs}}} + \frac{1}{\mu_{\mathrm{bulk}}} \qquad (2)$$

where $D = \exp(x/l_{\mathrm{crit}})$, $x$ is the distance from the interface, and $l_{\mathrm{crit}}$ is a fitting parameter. The mobility consists of three parts. 1) The surface contribution due to acoustic phonon scattering is $\mu_{\mathrm{surf_aps}} = (B/\mathbf{E}) + [C(N_i/N_0)^{\tau}/\mathbf{E}^{1/3}(T/T_0)^K]$, where $N_i = N_A + N_D$ ($N_A$ is the acceptor impurity density, and $N_D$ is the donor impurity density), $T_0 = 300$ K, $\mathbf{E}$ is the transverse electric field normal to the interface of semiconductor and insulator, $B$ and $C$ are parameters based on the physically derived quantities, $N_0$ and $\tau$ are fitting parameters, $T$ is the lattice temperature, and $K$ is the temperature dependence of the probability of surface phonon scattering. 2) The contribution attributed to surface roughness scattering is $\mu_{\mathrm{surf_rs}} = [((\mathbf{E}/\mathbf{E}_{\mathrm{ref}})^{\Xi}/\delta) + (\mathbf{E}^3/\eta)]^{-1}$, where $\Xi = A + [(\alpha \cdot (n+p)N_{\mathrm{ref}}^{v})/(N_i + N_1)^{v}]$, $\mathbf{E}_{\mathrm{ref}} = 1$ V/cm is a reference electric field to ensure a unitless numerator in $\mu_{\mathrm{surf_rs}}$, $N_{\mathrm{ref}} = 1$ cm$^{-3}$ is a reference doping concentration to cancel the unit of the term raised to the power $v$ in the denominator of $\Xi$,

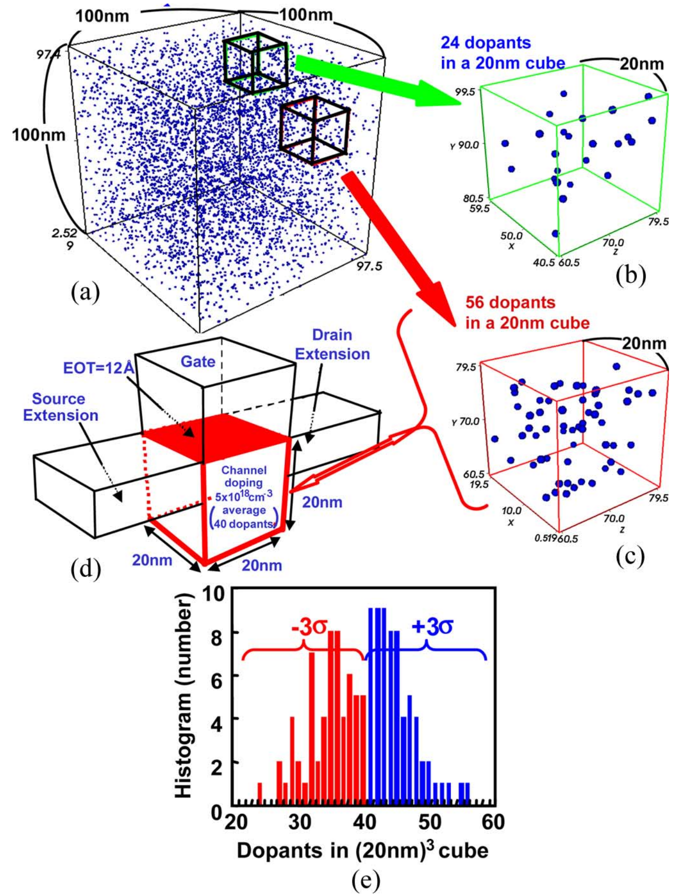


Fig. 1. (a) Discrete dopants randomly distributed in $(100\ \mathrm{nm})^3$ cube with an average concentration of 5E18 cm$^{-3}$. There will be 5000 dopants within the $(100\ \mathrm{nm})^3$ cube, but the dopants vary from 24 to 56 (the average number is 40, and the standard deviation is 6.3) within its 125 subcubes of $(20\ \mathrm{nm})^3$ [(b), (c), and (e)]. These 125 subcubes are then equivalently mapped into the channel region for dopant-position- and dopant-number-sensitive simulation, as shown in (d).

$\delta$ is a constant that depends on the details of the technology (such as oxide growth conditions), $N_1 = 1$ cm$^{-3}$, and $A$, $\alpha$, and $\eta$ are fitting parameters. 3) The bulk mobility is $\mu_{\mathrm{bulk}} = \mu_L(T/T_0)^{-\xi}$, where $\mu_L$ is the mobility due to bulk phonon scattering, and $\xi$ is a fitting parameter. The mobility model is quantified with our device measurements for the best accuracy.

First, the doping profile is analytically approximated to the device measured. We then apply the method to be described below, shown in Fig. 1, to generate discrete dopants in the channel region. Fig. 1 briefly illustrates how to generate a discrete dopant channel for the aforementioned simulation, concurrently capturing the randomness of dopant number and dopant position. Fig. 1(a) shows the discrete dopants randomly distributed in the cube of volume $(100\ \mathrm{nm})^3$ with an average concentration of 5E18 cm$^{-3}$, which is the same as the fabricated device. There will be 5000 dopants within the $(100\ \mathrm{nm})^3$ cube, but dopants vary from 24 to 56 (the average number is 40, and the standard deviation is 6.3) within its 125 subcubes of $(20\ \mathrm{nm})^3$, as shown in Fig. 1(b), (c), and (e), respectively. These 125 subcubes are then equivalently mapped into the channel region for the discrete dopant simulation, as shown in Fig. 1(d). In principle, 3-D device simulation with 125 channel structures

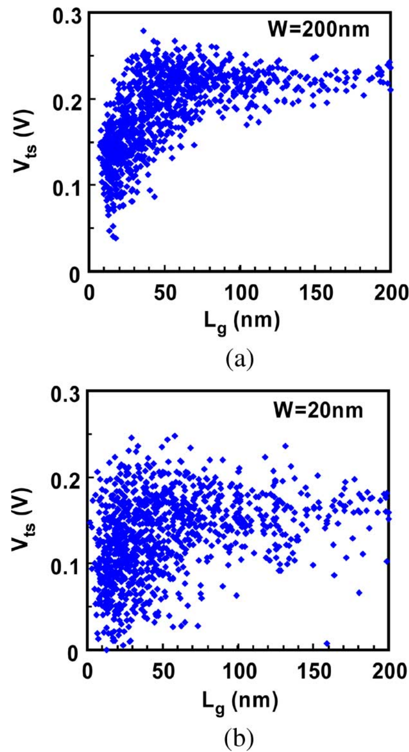


Fig. 2. Experimental saturation threshold voltage $V_{ts}$ of N-MOSFETs with $L_g$ down to 20 nm for (a) width = 200 nm and (b) width = 20 nm at $V_d$ = 1.0 V. The saturation threshold voltage is defined as a gate voltage for the saturation drain current of 100 nA.

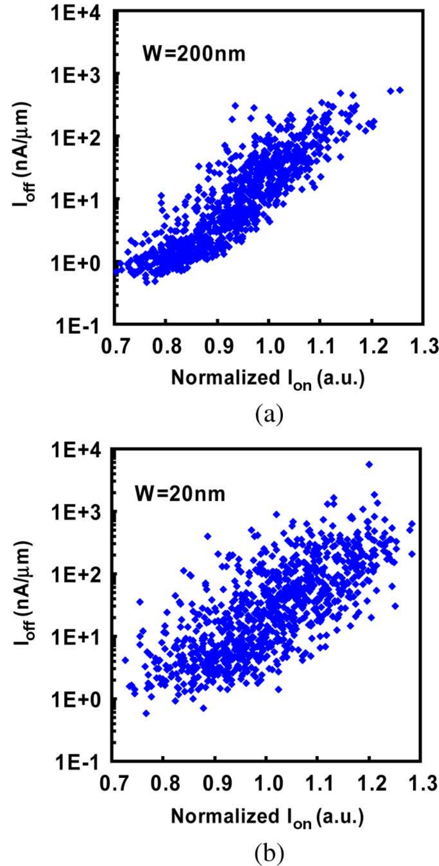


Fig. 3. Experimental $I_{\mathrm{on}}$–$I_{\mathrm{off}}$ characteristics of N-MOSFETs with $L_g$ down to 20 nm for (a) width = 200 nm and (b) width = 20 nm at $V_d$ = 1.0 V. $I_{\mathrm{on}}$ was normalized against the ON-state current of the nominal $L_g$ case, i.e., the 20-nm $L_g$ case.

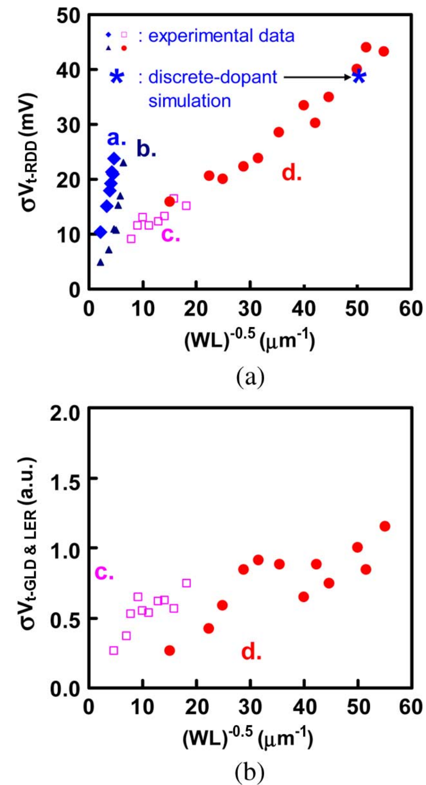


Fig. 4. (a) Experimentally extracted $\sigma V_{t,\,\mathrm{RDD}}$ and discrete dopant simulation $(*, L_g = \mathrm{W} = 20\ \mathrm{nm}, \mathrm{EOT} = 12\ \mathrm{A}^\circ)$ for various devices with nominal $L_g$ from 55 nm down to 20 nm. The width is fixed and the length is varying to give the range of values of $(WL)^{-0.5}$. The sample size for each data point of $\sigma V_t$ is around 100 points. (b) Extracted $\sigma V_{t,\,\mathrm{GLD\&LER}}$ for c and d conditions. The value was normalized against $\sigma V_{t,\,\mathrm{GLD\&LER}}$ of the nominal $L_g$ case in d condition.

TABLE I
CORRESPONDING PARAMETERS FOR ALL CASES IN FIG. 4. IT PRESENTS THE TREND OF $\sigma V_t$ FOR TECHNOLOGY SCALING. THE NOMINAL $L_g$ CASES IN THE TABLE ARE THE NOMINAL GATE LENGTHS FOR EACH TECHNOLOGY NODE, RESPECTIVELY

| | EOT (A°) | Channel Doping ($cm^{-3}$) | Nominal $L_g$ (nm) | Width (nm) |
|---|---|---|---|---|
| a | 24 | ≈1E18 | 55 | 1000 |
| b | 18 | ≈3E18 | 35 | 1000 |
| c | 12 | ≈5E18 | 20 | 200 |
| d | 12 | ≈5E18 | 20 | 20 |

almost covers $\pm 3\sigma$ cases, as shown in Fig. 1(e), and thus will be fairly meaningful to reflect the statistical randomness of dopant number and dopand position in the channel region.

## III. RESULTS AND DISCUSSION

Figs. 2 and 3 show the experimental $V_t$ fluctuation and the ON- and OFF-state current ($I_{\mathrm{on}}$–$I_{\mathrm{off}}$) characteristics of the n-typed MOSFETs (N-MOSFETs) down to 20-nm gates. The $L_g$ values in Fig. 2 are estimated from the gate capacitances in analysis data, and we presume that the widths of all samples are 200 and 20 nm for Fig. 2(a) and (b), respectively. As expected, the $V_t$ rolloff characteristics of 20-nm-wide devices are much more scattered than that of 200-nm-wide devices. The RDD-induced $V_t$'s standard deviation $\sigma V_{t,\,\mathrm{RDD}}$ has then been experimentally extracted, as shown in Fig. 4(a). The discrete dopant simulation for $L_g$ = width $(W)$ = 20 nm

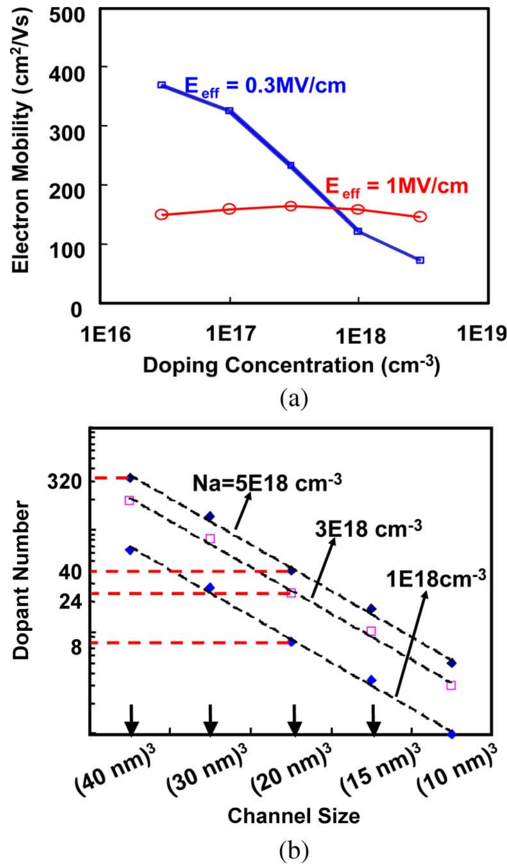


Fig. 5. (a) Extracted nonstrain mobility versus doping concentration at 0.3 and 1 MV/cm vertical field. (b) Scaling of the average channel dopant numbers versus channel size.

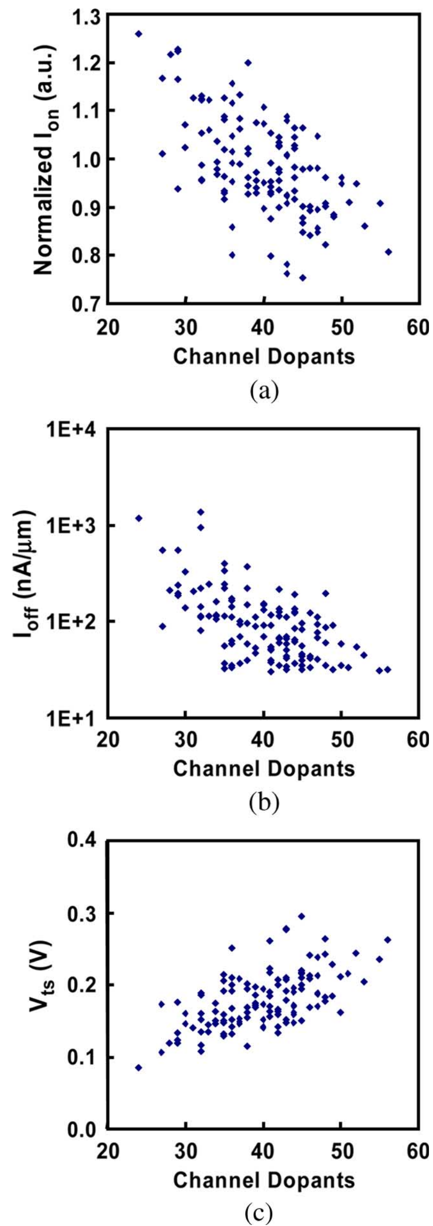


Fig. 6. Distributions of (a) $I_{\mathrm{on}}$, (b) $I_{\mathrm{off}}$, and (c) $V_{ts}$ versus the channel dopants for the 125 discrete-dopant 20-nm-gate transistors ($L_g = W = 20$ nm) shown in Fig. 5(e).

[data represented with the symbol $^*$, as shown in Fig. 4(a)] is in good agreement with the experimental data, which confirms that the channel doping is randomly distributed as statistically modeled. As shown in Fig. 1, more than 100 cases are required for a set of $L_g$ and width. We notice that each 3-D simulation case may take about three to seven days for the final convergent result. Without loss of generality, due to the heavy computing resource, we select the most critical case (i.e., length = width = 20 nm) for comparison between simulation and measurement. Fig. 4(b) shows the extracted $\sigma V_{t,\,\mathrm{GLD\&LER}}$ of c and d conditions. The $\sigma V_{t,\,\mathrm{GLD\&LER}}$ contains the contribution from the mean GLD and the LER. In our experimental data, the $\sigma V_{t,\,\mathrm{GLD\&LER}}$ increases as $(WL)^{-0.5}$ increased, and it has a similar trend compared with $\sigma V_{t,\,\mathrm{RDD}}$. Table I summarizes the corresponding parameters for all cases in Fig. 4. Fig. 5(a) shows the extracted mobility versus the doping concentration from samples of the cases (a) and (b), as shown in Fig. 4(a). The used mobility model can generate mobility that is in good agreement with the extracted mobility, as shown in Fig. 5(a). The low-field electron mobility at 0.3 MV/cm is greatly reduced with increasing doping concentration. That is why we limit our channel doping concentration at 5E18 cm$^{-3}$, which corresponds to an average of 40 dopants in (20 nm)$^3$ cubes and 17 dopants in (15 nm)$^3$ cubes, as shown in Figs. 1 and 8, respectively. Less channel doping concentration may reduce $\sigma V_{t,\,\mathrm{RDD}}$, but the channel dopants will quickly approach a single-digit number, as shown in Fig. 5(b). Fig. 6(a)–(c) shows the $I_{\mathrm{on}}$, $I_{\mathrm{off}}$, and $V_t$ distributions versus the channel dopants of these 125 cases. From the random-dopant-number point of view, the equivalent channel doping concentration increases when the dopant number increases. This substantially alters the threshold voltage and the ON- and OFF-state currents, as shown in Fig. 6(a)–(c), respectively. The random dopant position induced a different fluctuation of characteristics in spite of the same number of dopants. Furthermore, the magnitude of the spread characteristics increases as the number of dopants increases. Fig. 7(a) shows the $I_{\mathrm{on}}$–$I_{\mathrm{off}}$ characteristics of the 125 cases from Fig. 1. Fig. 7(b)–(d) discloses three different discrete dopant channels that have similar values of $I_{\mathrm{on}}$ or $I_{\mathrm{off}}$ but with various dopant distributions. Their corresponding cross-sectional OFF-state electrostatic potential and ON-state current density at 1 nm below the gate oxide are also presented, as

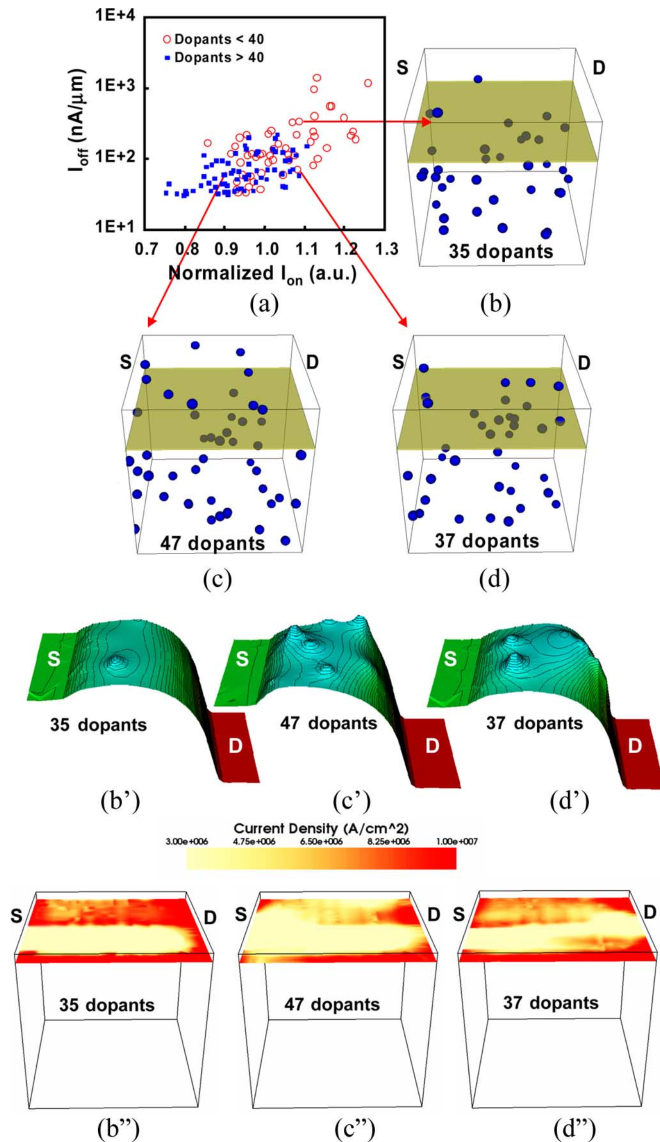


Fig. 7. (a) $I_{\rm on}$–$I_{\rm off}$ characteristics of the 125 discrete-dopant 20-nm-gate transistors ($L_g = W = 20$ nm). (b) and (d) Two cases of channel doping with similar $I_{\rm on}$ but different $I_{\rm off}$. (c) and (d) Two cases of channel doping with similar $I_{\rm off}$ but different $I_{\rm on}$. The corresponding OFF-state ($V_d = 1.0$ V, $V_g = 0.0$ V) potential contours and ON-state ($V_d = 1.0$ V, $V_g = 1.0$ V) current density of (b)–(d) are shown in (b')–(d') and (b")–(d"), respectively. All cross-sectional figures of OFF-state potential contours and ON-state current density distributions are extracted at 1 nm below 12 A° EOT gate oxide.

shown in Fig. 7(b')–(d') and (b")–(d"), which clearly shows that the distributions of the electrostatic potential and current density are closely related to the dopant arrangements within the cross-sectional area beside the source side, as shown in Fig. 7(b)–(d).

Based on experimental data and the discrete modeling of 20-nm gate with 12 A° EOT, 8 A° EOT seems an effective way for 15-nm-gate CMOS to mitigate the increase of the RDD-induced $V_t$ variation. With the same approach (shown in Fig. 1) for generating discrete dopant channels, Fig. 8(a) shows 343 subcubes of $(15\ \text{nm})^3$ derived from $(105\ \text{nm})^3$ cubes with 5E18 cm$^{-3}$ doping. Fig. 9 shows the $I_{\rm on}$–$I_{\rm off}$ characteristics and the $V_t$ distribution of these cases with 12 A° and 8 A° EOT. The case of 8 A° EOT shows a tighter $V_t$ scattering. Further-

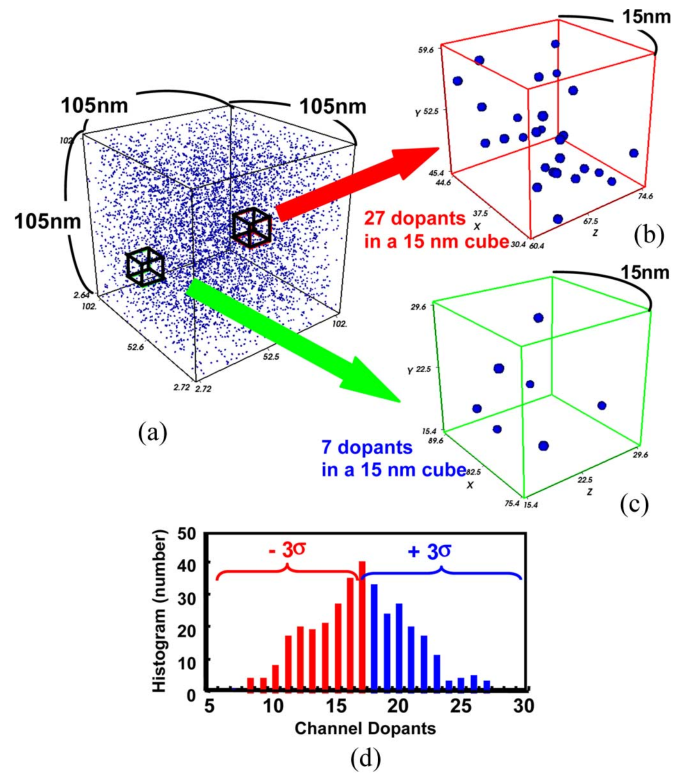


Fig. 8. (a) 5E18 cm$^{-3}$ doped $(105\ \text{nm})^3$ cube with 343 subcubes of $(15\ \text{nm})^3$. Dopants inside the subcubes range from (c) 7 to (b) 27, with (d) the average number of 17 and one standard deviation of 4.

more, as the channel dopants could only be seven at the $3\sigma$ edge, as shown in Fig. 8(c), we herein propose using a higher work function gate to increase its intrinsic electrostatic potential barrier height, as shown in Fig. 10(c), to prevent source-to-drain punch-through at the OFF-state, as shown in Fig. 10(b). Thus, $\sigma V_{t,\rm RDD}$ can be maintained while $L_g$ scales down to 15 nm from 20 nm, as summarized in Table II. It has been known that $\sigma V_t$ is proportional to the oxide thickness [5], [15]; that is, $\sigma V_t = (qtox/\varepsilon_{\rm ox})\sqrt{N_A W_d/4LW}$, where $\varepsilon_{\rm ox}$ is the permittivity of the gate oxide, and $W_d$ is the width of the depletion layer under the gate. In the examination for the 15-nm-gate CMOS, when the EOT changed from 12 A° to 8 A° (1.5 times smaller), the $\sigma V_{t,\rm RDD}$ was reduced from 54 mV to 41 mV (1.32 times smaller), which conformed to the expression of $\sigma V_t$. Although the advanced devices, such as double-gate or surrounding-gate structures [3], [10], or the epitaxial channels [13], [14] can reduce the fluctuation, these approaches are much more complicated and still require the EOT's improvement to some degree for the good suppression of $\sigma V_t$.

## IV. Conclusion

The RDD-induced $\sigma V_t$ for 20-nm-gate planar CMOS devices has been experimentally extracted and in good agreement with the newly developed 3-D discrete dopant characterization. An average of 40 dopants randomly distributed in the channel region give rise to $\sigma V_{t,\rm RDD}$ of 40 mV. The developed scheme outlooks that seven dopants under 15-nm gate at the $3\sigma$ edge will occur, and 8 A° EOT, in addition to the work-function-modulated metal gate, can suppress the increase

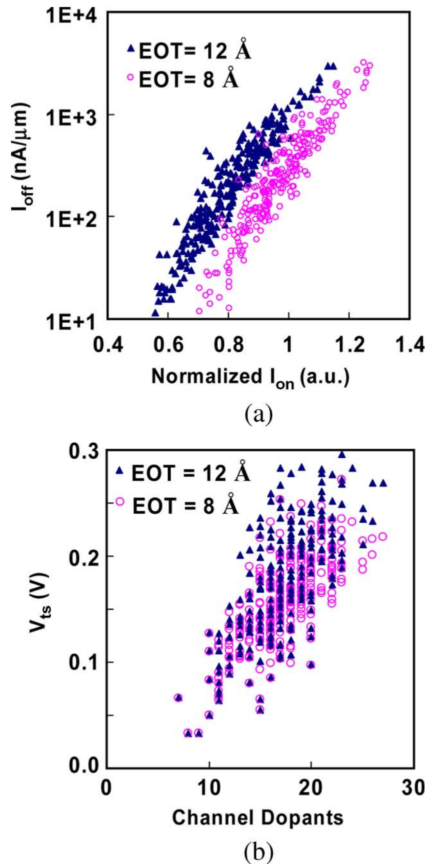


Fig. 9. (a) $I_{\rm on}$–$I_{\rm off}$ characteristics and (b) $V_{ts}$ versus channel dopants of the discrete doped 15-nm gates with EOT $= 12$ A° (solid triangle) and 8 A° (open circle). The gate work function is 4.22 eV in the simulation.

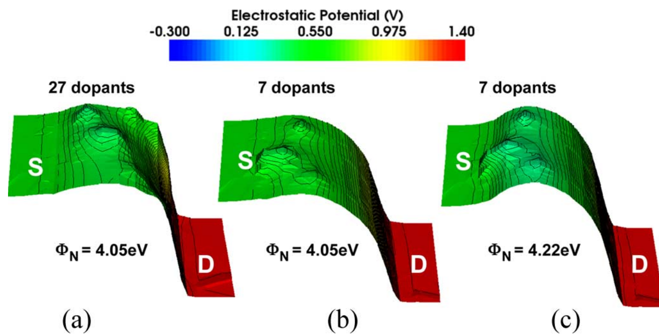


Fig. 10. Cross-sectional OFF-state electrostatic potential contours of two extreme cases in 15-nm channels ($W = 15$ nm and EOT $= 8$ A°) with (a) 27 dopants and $\Phi_N = 4.05$ eV, (b) seven dopants and $\Phi_N = 4.05$ eV, and (c) seven dopants and $\Phi_N = 4.22$ eV, all at 1 nm below the gate oxide.

TABLE II
SUMMARY OF THE DISCRETE DOPANT FLUCTUATED 20-nm- AND 15-nm-GATE PLANAR CMOS TRANSISTORS

| $L_g$ | Width | Data Source | Gate Work Function | Channel Doping (cm$^{-3}$) | EOT | $\sigma V_{t,RDD}$ |
|---|---|---|---|---|---|---|
| 20 nm | 200 nm | experimental | band-edge | 5E+18 | 12 A° | 17 mV |
| | 20 nm | experimental | | 5E+18 | 12 A° | 40 mV |
| | 20 nm | Simulation | | 5E+18 | 12 A° | 39 mV |
| 15 nm | 15 nm | Simulation | $\phi_N$= 4.22 eV | 5E+18 | 12 A° | 54 mV |
| | 15 nm | Simulation | $\phi_P$= 4.98 eV | 5E+18 | 8 A° | 41 mV |

of the $\sigma V_{t,\rm RDD}$ for realizing manufacture with such gate length scaling.

## ACKNOWLEDGMENT

The authors would like to thank the managerial and instrumental supervision to deploy the development work at Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C.

## REFERENCES

[1] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y.-C. Yeo, Y. Li, J.-W. Lee, P. Chen, M.-S. Liang, and C. Hu, "5 nm-gate nanowire FinFET," in *VLSI Symp. Tech. Dig.*, 2004, pp. 196–197.

[2] F.-L. Yang, H.-Y. Chen, F.-C. Chen, C.-C. Huang, C.-Y. Chang, H.-K. Chiu, C.-C. Lee, C.-C. Chen, H.-T. Huang, C.-J. Chen, H.-J. Tao, Y.-C. Yeo, M.-S. Liang, and C. Hu, "25 nm CMOS omega FETs," in *IEDM Tech. Dig.*, 2002, pp. 255–258.

[3] F.-L. Yang, J.-R. Hwang, and Y. Li, "Electrical characteristic fluctuations in sub-45 nm CMOS devices," in *Proc. IEEE CICC*, 2006, pp. 691–694.

[4] H. Fukutome, Y. Momiyama, T. Kubo, E. Yoshida, H. Morioka, M. Tajima, and T. Aoyama, "Suppression of poly-gate-induced fluctuations in carrier profiles of sub-50 nm MOSFETs," in *IEDM Tech. Dig.*, 2006, pp. 281–284.

[5] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 $\mu$m MOSFET's: A 3-D 'atomistic' simulation study," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2505–2513, Dec. 1998.

[6] A. Asenov, A. R. Brown, J. H. Davies, S. Kaya, and G. Slavcheva, "Simulation of intrinsic parameter fluctuations in decananometer and nanometer-scale MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1837–1852, Sep. 2003.

[7] D. J. Frank, Y. Taur, M. Ieong, and H.-S. P. Wong, "Monte Carlo modeling of threshold variation due to dopant fluctuations," in *VLSI Symp. Tech. Dig.*, 1999, pp. 169–170.

[8] G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy, and A. Asenov, "Simulation study of individual and combined sources of intrinsic parameter fluctuations in conventional nano-MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 3063–3070, Dec. 2006.

[9] S. Xiong and J. Bokor, "A simulation study of gate line edge roughness effects on doping profiles of short-channel MOSFET devices," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 228–232, Feb. 2004.

[10] Y. Li and S.-M. Yu, "Comparison of random-dopant-induced threshold voltage fluctuation in nanoscale single-, double-, and surrounding-gate field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 45, no. 9A, pp. 6860–6865, Sep. 2006.

[11] Y. Li and S.-M. Yu, "Study of threshold voltage fluctuations of nanoscale double gate metal–oxide–semiconductor field effect transistors using quantum correction simulation," *J. Comput. Electron.*, vol. 5, no. 2/3, pp. 125–129, Jul. 2006.

[12] Y. Li, S.-M. Yu, and H.-M. Chen, "Process-variation- and random-dopants-induced threshold voltage fluctuations in nanoscale CMOS and SOI devices," *Microelectron. Eng.*, vol. 84, no. 9/10, pp. 2117–2120, Sep./Oct. 2007.

[13] Y. Li and S.-M. Yu, "Quantum correction simulation of random dopant-induced threshold voltage fluctuations in nanoscale metal–oxide–semiconductor structures," in *Proc. 5th IEEE NANO*, 2005, pp. 527–530.

[14] A. Asenov and S. Saini, "Suppression of random dopant-induced threshold voltage fluctuations in sub-0.1-$\mu$m MOSFET's with epitaxial and $\delta$-doped channels," *IEEE Trans. Electron Devices*, vol. 46, no. 8, pp. 1718–1724, Aug. 1999.

[15] T. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 1998.

[16] Y. Li, S. M. Sze, and T.-S. Chao, "A practical implementation of parallel dynamic load balancing for adaptive computing in VLSI device simulation," *Eng. Comput.*, vol. 18, no. 2, pp. 124–137, Aug. 2002.

[17] Y. Li, H.-M. Chou, and J.-W. Lee, "Investigation of electrical characteristics on surrounding-gate and omega-shaped-gate nanowire FinFETs," *IEEE Trans. Nanotechnol.*, vol. 4, no. 5, pp. 510–516, Sep. 2005.

[18] A. Martinez, J. R. Barker, M. P. Anantram, A. Svizhenko, and A. Asenov, "Developing a full 3D NEGF simulator with random dopant and interface roughness," in *Proc. 11th Int. Workshop Comput. Electron.*, 2006, p. 275.

[19] J. R. Watling, A. R. Brown, A. Asenov, A. Svizhenko, and M. P. Anantram, "Simulation of direct source-to-drain tunnelling using the density gradient formalism: Non-equilibrium Green's function calibration," in *Proc. SISPAD*, 2002, pp. 267–270.

[20] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*. New York: Springer-Verlag, 1984.

[21] M. N. Darwish, J. L. Lentz, M. R. Pinto, P. M. Zeitzoff, T. J. Krutsick, and H. H. Vuong, "An improved electron and hole mobility model for general purpose device simulation," *IEEE Trans. Electron Devices*, vol. 44, no. 9, pp. 1529–1538, Sep. 1997.

**Yiming Li** (M'02) received the B.S. degree in applied mathematics and electronics engineering, the M.S. degree in applied mathematics, and the Ph.D. degree in electronics from the National Chiao Tung University (NCTU), Hsinchu, Taiwan, R.O.C., in 1996, 1998, and 2001, respectively.

In 2001, he was an Associate Researcher with the National Nano Device Laboratories (NDL), Taiwan, and an Assistant Professor with the Microelectronics and Information Systems Research Center (MISRC), NCTU, where he was engaged in the field of computational science and engineering, particularly in the modeling, simulation, and optimization of nanoelectronics and very large scale integration (VLSI) circuits. In 2002, he was a Visiting Assistant Professor with the Department of Electrical and Computer Engineering, University of Massachusetts, Amherst. From 2003 to 2004, he was a Research Consultant with the System on a Chip (SOC) Technology Center, Industrial Technology Research Institute, Hsinchu. From 2003 to 2005, he was the Director of the Departments of Nanodevice and Computational Nanoelectronics, NDL. In 2004, he was an Associate Professor with the MISRC, NCTU. He is currently an Associate Professor with the Department of Communication Engineering, NCTU, and an Adjunct Professor with the Institute of Management of Technology, NCTU. He is the Deputy Director of the Modeling and Simulation Center of NCTU and conducts the Parallel and Scientific Computing Laboratory, NCTU. He has authored or coauthored over 120 research papers appearing in international book chapters, journals, and conference proceedings. His current research areas include computational electronics and physics, physics of semiconductor nanostructures, device modeling, parameter extraction, VLSI circuit simulation, development of technology computer-aided design (TCAD) and electronic CAD (ECAD) tools and SOC applications, bioinformatics and computational biology, advanced numerical methods, parallel and scientific computing, optimization techniques, and computational intelligence.

Dr. Li is a member of Phi Tau Phi, Sigma Xi, the American Physical Society, the American Chemical Society, the Association for Computing Machinery, the Institute of Electronics, Information and Communication Engineers (IEICE), Japan, and the Society for Industrial and Applied Mathematics. He is included in Who's Who in the World. He has served as a Reviewer, Guest Associate Editor, and Guest Editor for many international journals. He has organized and served on several international conferences and was an Editor for the Proceedings of International Conferences. He has served as a Reviewer for the IEEE TRANSACTIONS ON NANOTECHNOLOGY, the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the IEEE TRANSACTIONS ON EVOLUTIONARY COMPUTATION, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, the IEEE ELECTRON DEVICE LETTERS, and the IEEE TRANSACTIONS ON ELECTRON DEVICES. He was the recipient of the 2002 Research Fellowship Award presented by the Pan Wen-Yuan Foundation, Taiwan, and the 2006 Outstanding Young Electrical Engineer Award from the Chinese Institute of Electrical Engineering, Taiwan.

**Shao-Ming Yu** received the B.S. and M.S. degrees in computer and information science in 2002 and 2004, respectively, from the National Chiao Tung University (NCTU), Taiwan, R.O.C., where he is currently working toward the Ph.D. degree in the Department of Computer Science.

His research interests focus on the modeling and simulation of semiconductor nanodevices, parallel and scientific computation, evolutionary algorithms, and design optimization.

**Jiunn-Ren Hwang** received the B.S. degree in electrophysics from the National Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 1986, the M.S. degree in applied physics from the National Tsing Hua University, Hsinchu, in 1988, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 1996.

He is currently a Manager with the Exploratory Research Division, Department of Research and Development, Taiwan Semiconductor Manufacturing Company, Hsinchu. His current interest is on the development of FinFET devices for the applications of N22 SRAM and logic devices. He has authored or coauthored several papers in IEDM, VLSI technology, and IRPS conferences. He has been awarded over 20 U.S. patents in the fields of semiconductor devices and manufacturing process. His recent research works also involve strain silicon technology, advanced metal gate/high-$K$ devices, bulk-FinFET SONOS Flash, and CMOS variability in the 65-nm regime and beyond.

**Fu-Liang Yang** received the B.S. degree in materials science and engineering from the National Tsing Hua University, Taiwan, R.O.C., in 1989, and the Ph.D. degree in materials science and engineering from Cambridge University, Cambridge, U.K., in 1994.

From 1994 to 2000, he was with Vanguard, where he worked on DRAM process and device development. From 2000 to 2006, he managed a department in Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, with research focuses on novel transistor architecture and process technologies for sub-32-nm node logic and nonvolatile memory. Since January 2007, he has conducted a phase-change memory program for NAND/NOR Flash replacement in TSMC. He has authored or coauthored over ten publications in IEDM, Symposium on VLSI Technology, and IEEE journals. He is the holder of more than 100 US patents in advanced CMOS devices and dynamic/static/nonvolatile memory technologies.

Dr. Yang received the Outstanding Young Engineer Award from the Chinese Institute of Engineering in 2004. He was the recipient of TSMC's 2003 Best Invention Disclosures Award and the 2004 Innovation Award. He is entitled TSMC Academician of TSMC Academy since 2004.