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Effect of interfacial fluorination on the electrical properties of the inter-poly high-*k* dielectrics

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ABSTRACT

In this paper, the reliabilities and insulating characteristics of the fluorinated aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2) inter-poly dielectric (IPD) are studied. Interface fluorine passivation has been demonstrated in terminating dangling bonds and oxygen vacancies, reducing interfacial re-oxidation and smoothing interface roughness, and diminishing trap densities. Compared with the IPDs without fluorine incorporation, the results clearly indicate that fluorine incorporation process is effective to improve the insulating characteristics of both the Al_2O_3 and HfO_2 IPDs. Moreover, fluorine incorporation will also improve the dielectric quality of the interfacial layer. Although HfO_2 possesses higher dielectric constant to increase the gate coupling ratio, the results also demonstrate that fluorination of the Al_2O_3 dielectric is more effective to promote the IPD characteristics than fluorination of the HfO_2 dielectric. For future stack-gate flash memory application, the fluorinated Al_2O_3 IPD undoubtedly possesses higher potential to replace current ONO IPD than the fluorinated HfO_2 IPD due to superior insulating properties.

1. Introduction

The scaling of both tunneling oxides and inter-poly dielectrics (IPD) is critical for the next generation of nonvolatile floating-gate flash memories with faster programming and lower voltage operation [1]. For the floating-gate flash memory devices, an IPD requires a high charge-to-breakdown (Q_{BD}) and low leakage current to obtain good data retention characteristics. In order to accomplish this without a trade-off between low power and high speed operations, a high gate coupling ratio must be achieved by increasing the floating-gate capacitance.

There are three different approaches can be used to increase gate coupling ratio. First, decrease the IPD thickness. However, decreasing the thickness of the IPD to increase the gate coupling ratio may cause serious leakage and reliability problems due to undesirable carrier tunneling and injection between the control-gate and floating-gate, which are fatal in the retention time of flash memories. Secondly, increase the area of the IPD capacitor. High capacitive-coupling ratio cell [2,3], 3-D IPD [4], and hemisphere grain [5,6] had been proposed to effective increase the capacitance area and lower the control gate bias. Although the gate coupling ratio of above mentioned cell structures could be dramatically improved, they must be fabricated with many additional process steps to fabricate such complex structures and be difficult to control well. The packing density is also reduced while increasing the area of the IPD capacitor.

The final approach is to increase the dielectric constant (k) of IPD materials [7–10]. We have demonstrated that the control gate voltage can be reduced by greater than 45% with high dielectric constant (high-k) IPDs, through MEDICI simulation [11]. In order to avoid increasing the cell area and complicating the fabrication processes, therefore, it is straightforward and effective to incorporate alternative high-k materials on floating-gate flash memories to replace existing oxide/nitride/oxide (ONO) IPD, for increasing floating-gate capacitance and suppressing charge loss simultaneously.

Among potential candidates, aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2) are the most attractive for IPD applications in nonvolatile flash memories, because of its higher conduction band offset with respect to the underlying poly-Si electrode, and its higher permittivity with respect to Si substrate [12]. Previously, we had presented the effects of surface ammonia (NH_3) nitridation and post-deposition annealing (PDA) temperature on reactive-sputtered (RS) aluminum oxide (Al_2O_3) IPD characteristics [8,9]. Directly deposition of high-k dielectrics inevitably results in a poorer interface as well as high bulk defect density [8]. Although interface nitridation is helpful to improve the IPD reliability, however, even after process optimization, the Q_{BD} of nitrided RS-Al_2O_3 IPD is still low.

Recently, the dielectric characteristics of the high-k materials due to the incorporation of fluorine (F) have been improved [13–16]. Fluorine incorporation into the gate dielectric can widely distributes within the high-k stacks, then recover interfacial

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dangling bonds and bulk oxygen vacancies during subsequently processes, which is useful to reduce gate leakage current as well as improving dielectric reliabilities [13]. In this paper, by controlling the fluorine implantation dosage, the fluorination effects on the insulating characteristics of the high-*k* IPDs will be investigated for the first time.

2. Experimental details

The inter-poly capacitor with fluorinated high-*k* IPDs was fabricated on 6-inch p-type (1 0 0)-oriented Si wafers. A 200 nm poly-Si bottom gate was deposited on the 200 nm buffer oxide by low pressure chemical vapor deposition (LPCVD) system using silane (SiH_4) gas at 620 °C and subsequently implanted with phosphorous at 5×10^{15} cm^{-2}, 20 keV. Prior to the deposition of the high-*k* IPD, the bottom gate was subjected to 10 keV fluorine (F) implantation split from 10^{12} cm^{-2} to 10^{14} cm^{-2}, then activated with rapid thermal annealing (RTA) at 950 °C in nitrogen (N_2) ambient for 30 s to reduce the surface damage from the ion bombardment. After conventional RCA cleaning and sequentially etched in diluted hydrofluoric acid for the removal of particles and native oxides, 10 nm Al_2O_3 or 15 nm HfO_2 was then deposited by AIXTRON metal organic chemical vapor deposition (MOCVD) system in oxygen gas at 500 °C. In order to improve the film quality, Al_2O_3 and HfO_2 IPD was annealed at 900 °C and 600 °C in N_2 ambient for 30 s, respectively. Subsequently, the poly-Si top gate was fabricated the same with the bottom gate. Finally, gate stacks were patterned and metallization were defined.

Equivalent oxide thickness (EOT) was obtained from the high-frequency (100 kHz) capacitance–voltage (*C*–*V*) measurement using a Hewlett–Packard (HP) 4284 inductance–capacitance–resistance meter at the inversion region, without considering inversion-charge quantization and poly-depletion effect. For comparison at similar EOT, HfO_2 IPD should be deposited thicker than Al_2O_3 IPD due to the higher dielectric constant of the HfO_2 material. The extracted EOT of the Al_2O_3 and HfO_2 IPD as a function of the fluorine implantation dosage can be therefore, controlled between 4.1 and 4.5 nm. Moreover, since the HfO_2 dielectric exhibits smaller band-gap as well as smaller conduction band offset with respect to the Si, thicker HfO_2 thickness is helpful to suppress tunneling leakage current. Dielectric constant of the high-*k* materials was extracted using EOT and physical thickness, which was measured from the transmission electron microscopy (TEM) images. Furthermore, the content and distribution of the fluorine atom was measured by secondary-ion mass spectroscopy (SIMS). The binding energy of the Al, Hf and Si atom were extracted from the X-ray photoelectron spectrometer (XPS). The electrical properties and reliability characteristics of the fluorinated high-*k* inter-poly capacitors were measured using a HP4156C semiconductor parameter analyzer.

3. Results and discussion

Fig. 1a and b compares the XPS spectrum of the fluorinated Al_2O_3 IPD with and without fluorine implantation dosage. The detected binding energy was calibrated by C_{1s} signal (284.5 eV). For the Al_2O_3 IPD with fluorine incorporation, larger than 0.5 eV binding energy increment is obtained for both the Si and the Al signals. Since the incorporated fluorine atoms are effective to terminate the bulk oxygen vacancies and the interfacial dangling bonds due to the highest electronegativity, which exhibits high potential to create stronger Al–F and Si–F bonds within the fluorinated Al_2O_3 IPD, respectively [17,18]. Consequently, fluorination of the Al_2O_3 IPD can be used to increase binding energy of the Al and Si signals. Higher Si and Hf binding energy is also detected for the HfO_2 IPD after fluorine incorporation, as shown in Fig. 1c and d, which can

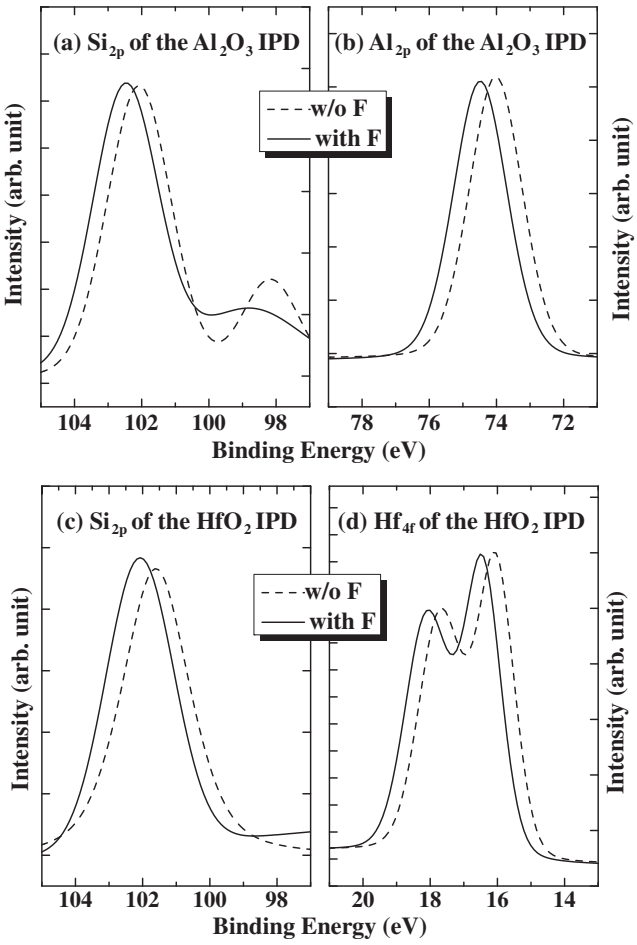

Fig. 1. XPS spectrum of the (a) Si_{2p} (b) Al_{2p} signals for the fluorinated Al_2O_3 IPD, and (c) Si_{2p} (d) Hf_{4f} signals for the fluorinated HfO_2 IPD with and without fluorine implantation dosage.

also form stronger Hf–F and Si–F bonds within the fluorinated HfO_2 IPD. Fig. 2 shows the SIMS depth profile of the high-*k* IPD with fluorine implantation. Although post-implantation high temperature thermal annealing would inevitably result in fluorine out-diffusion seriously, from the SIMS results, fortunately, the residual fluorine widely distributes within the high-*k* IPDs, which can help

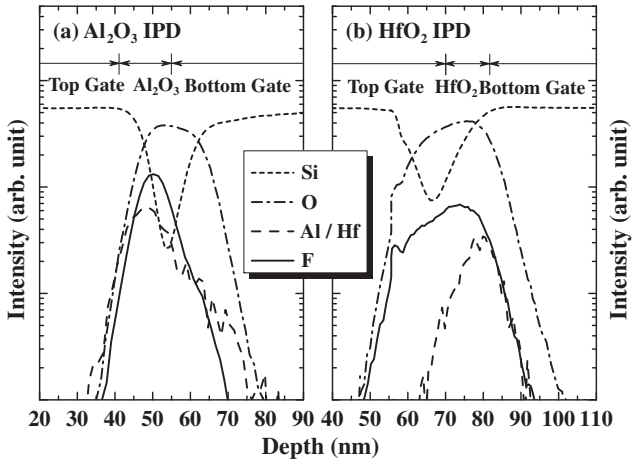

Fig. 2. SIMS depth profiles for the fluorinated (a) Al_2O_3 (b) HfO_2 IPD with fluorine implantation dosage.

to terminate the bulk oxygen vacancies and interfacial dangling bonds during subsequently high-temperature annealing. Consequently, stronger Al–F/Hf–F bonds and Si–F bonds will be created, and results in increased binding energy, as shown in Fig. 1.

Although incorporated fluorine can be used to terminate the bulk oxygen vacancies and interfacial dangling bonds regardless the incorporation processes, the EOT variation of the fluorinated dielectrics is found strongly dependent on the fluorine incorporation processes [16,18,19]. For the processes which will accumulate high fluorine concentration near the interface between the dielectric and the underneath substrate prior to the gate stack deposition, such as CF_4 plasma treatment [18] and surface fluorine implantation in this paper, the fluorine is believed to form hydrophobic Si–F bonds at the substrate surface, which can help to strongly suppress the interfacial re-oxidation during the gate stack deposition and subsequently high-temperature PDA. Accordingly, interfacial fluorine accumulation will result in thinner EOT. On the other hand, for the fluorine incorporation processes after the gate stack formation, such as fluorinated silicate glass (FSG)-induced fluorine passivation [16] and gate fluorine implantation [19], the incorporated fluorine will diffuse through the gate stack, which exhibits high potential to substitute the oxygen atoms, then replaces the Hf–O bonds by the Hf–F bonds. Part of the residual oxygen may diffuse toward the interface between the dielectric and the underneath substrate, then react with the silicon dangling bonds or silicon atoms at the interface to growth undesirably interfacial layer. Accordingly, fluorine diffusion and oxygen reaction will result in thicker EOT. The effect of fluorine incorporation processes on the EOT is summarized in Table 1.

Fig. 3a shows the EOT of the fluorinated high-*k* IPDs as a function of fluorine implantation dosage. Although fluorination directly using fluorine implantation would inevitably generate surface damage, which may deteriorate the dielectric reliabilities without sufficient annealing; fluorine implantation prior to the high-*k* IPDs deposition, on the other hand, is believed to form hydrophobic Si–F bonds at the silicon surface, as shown in Fig. 1, which is also proved not only to terminate the interfacial dangling bonds, but also to suppress the interfacial re-oxidation during subsequent high-temperature dielectrics deposition and annealing [20,21]. Moreover, the fluorine incorporation is also useful to replace low dielectric constant oxygen vacancies (vacuum) by the fluorine atoms to form strong Hf–F/Al–F bonds, which is also demonstrated in Fig. 1. Consequently, both the suppression of the interfacial re-oxidation and elimination of the low-*k* oxygen vacancies would contribute to the EOT scaling as the fluorine incorporation concentration increased, and therefore, results in increased dielectric constant, as shown in Fig. 3b. Compared to the high-*k* IPDs without fluorination, Al_2O_3 and HfO_2 IPD with $1 \times 10^{14}\,cm^{-2}$ fluorine implantation can increase the dielectric constant larger than 10% and 8%, respectively.

Fig. 4 compares the leakage current density-effective electric field characteristics of the fluorinated high-*k* inter-poly capacitors. Due to the proper filling the interfacial dangling bonds and bulk oxygen vacancies by the fluorine atoms, fluorinated high-*k* IPDs can reduce leakage current density in both polarities even at thinner EOT, especially for the IPDs with optimized ($5 \times 10^{13}\,cm^{-2}$) implantation dosage. For positive polarity, lower leakage current

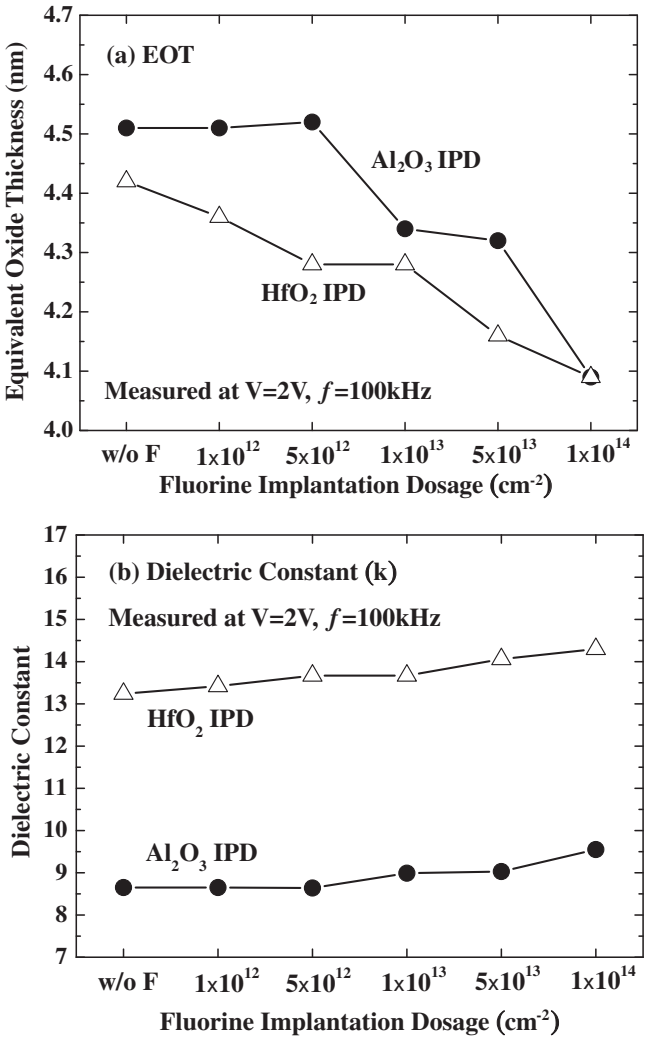

Fig. 3. Extracted (a) EOT and (b) dielectric constant (*k*) of the fluorinated high-*k* IPDs as a function of fluorine implantation dosage.

density means that electron tunneling from the bottom-gate (simulated as the floating-gate) to the top-gate (simulated as the control-gate) will be suppressed, which implies that fluorination of the high-*k* IPDs can be used to reduce storage-charge loss during programming and reading operation. On the other hand, lower leakage current density for the negative polarity indicates that fluorination of the high-*k* IPDs can be also used to suppress carrier injection from the control-gate to avoid erase-saturation. Since leakage path elimination between the floating-gate and control-gate is a critical issue in the design criteria of the floating-gate flash memories to sustain charge storage, the result clearly demonstrated the high-*k* IPDs with fluorine passivated interface is helpful to significantly suppress the storage-charge loss and gate injection current.

Fig. 5a indicates the breakdown voltage of the high-*k* IPDs with and without interface fluorine passivation. For implantation dosage less than $5 \times 10^{13}\,cm^{-2}$, interfacial fluorination can obviously increase the dielectric breakdown voltage in both polarities due to filling the interfacial dangling bonds and bulk oxygen vacancies by the fluorine atoms. Similar improvement is also obtained for the breakdown field, as shown in Fig. 5b. Fluorinated Al_2O_3 and HfO_2 IPD with optimized implantation dosage can provide larger than 12% and 17% breakdown voltage increment in both polarities, respectively, even at thinner EOT.

Table 1
The effect of fluorine incorporation processes on the EOT of the gate dielectric.

	FSG passivation [16]	CF_4 plasma [18]	Gate fluorine implantation [19]	Surface fluorine implantation [this work]
EOT	Increasing	Decreasing	Increasing	Decreasing

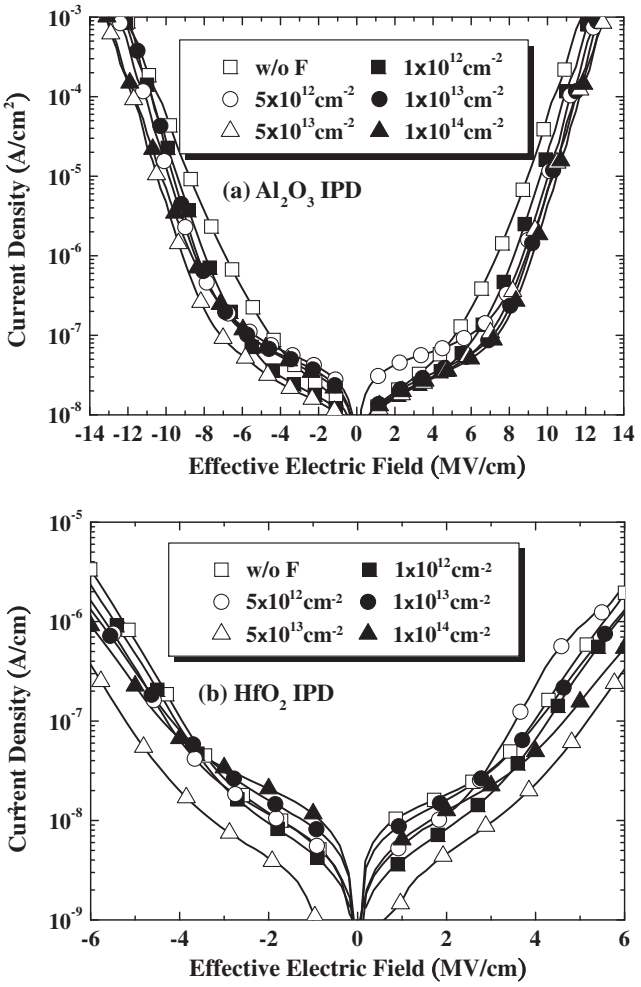

Fig. 4. Leakage current density characteristics of the fluorinated (a) Al_2O_3 IPD and (b) HfO_2 IPD as a function of fluorine implantation dosage.

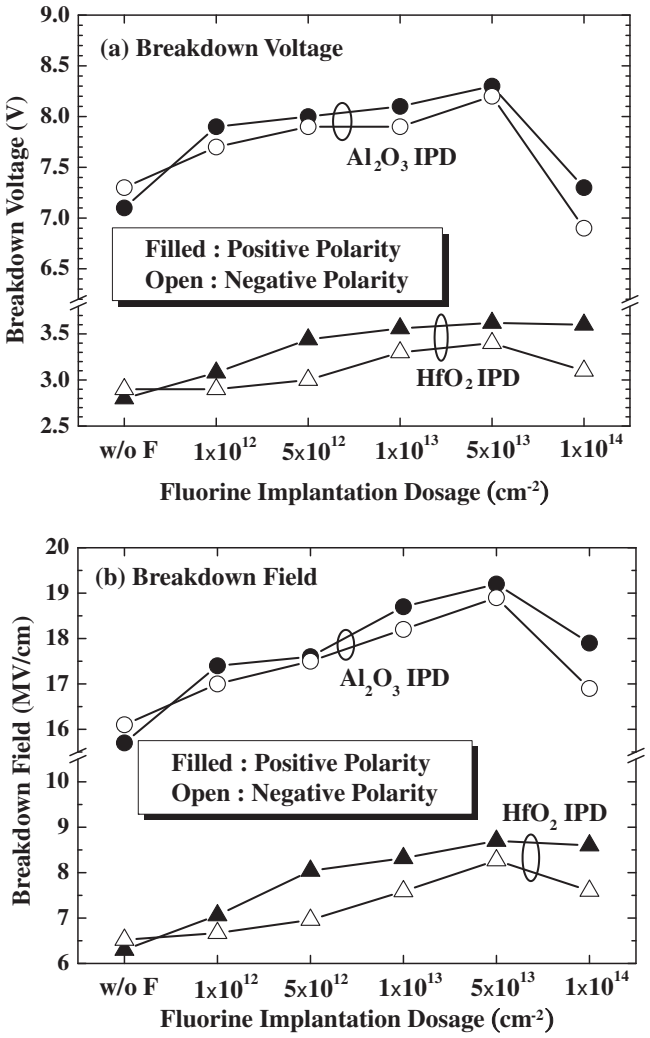

Fig. 5. (a) Breakdown voltage and (b) breakdown field of the fluorinated high-*k* IPDs as a function of fluorine implantation dosage.

Fig. 6a demonstrates the corresponding 63% failure-rate charge-to-breakdown (Q_{BD}) of the fluorinated high-*k* inter-poly capacitors under 2.5 V constant voltage stress (CVS). The fluorinated high-*k* IPDs clearly improves the Q_{BD} in both polarities, which can be mainly ascribed to diminish the dangling bonds and oxygen vacancies with fluorine atoms [5,7]. Moreover, the interface fluorine passivation prior to the IPD deposition also demonstrated in smoothing the interface between the high-*k* dielectric and the bottom gate due to the interfacial re-oxidation suppression, which can be supported by the thinner EOT, as shown in Fig. 3a. As a result, optimized fluorination can improve the Q_{BD} of the HfO_2 IPD from 0.02 C/cm^2 to larger than 0.167 C/cm^2. Although the result indicates that HfO_2 IPD with fluorine incorporation can increase the Q_{BD}, the extracted Q_{BD} of the fluorinated HfO_2 IPD seems too small to be implemented. On the other hand, the 63% failure Q_{BD} of the fluorinated Al_2O_3 IPD is larger than 2.1 C/cm^2 in both polarities, which is much higher than the Q_{BD} of the fluorinated HfO_2 IPD. Since the slope of the Weibull distribution is also an important factor in reliability calculation to extrapolate lifespan to different percentiles, the Weibull slope (β) of the Q_{BD} distribution is further extracted to examine the dielectric reliability, as shown in Fig. 6b. Apparently, both fluorinated high-*k* IPDs exhibits much higher Weibull slope than the IPDs without interfacial fluorination in both polarities. Since higher and symmetric device characteristics can contribute to further IPD scaling, the results clearly demonstrate that the fluorinated Al_2O_3 IPD can be effectively used to replace current ONO IPD to promote the device performance of the stacked-gate flash memory.

Besides, the fluorinated high-*k* IPDs obviously reveal polarity-dependent properties. The dielectrics stressed in positive polarity (electron injection from the poly-Si bottom gate) clearly exhibit superior dielectric characteristics than those stressed in negative polarity (electron injection from the poly-Si top gate), as shown in Figs. 4–6. The polarity-dependent dielectric properties of the fluorinated high-*k* IPDs can be primarily explained by the interface roughness between the high-*k* IPD and the poly-Si gate. Fluorine implantation prior to the high-*k* dielectrics deposition is believed to form hydrophobic Si–F bonds during subsequently high-temperature dielectric deposition and annealing, which is beneficial to suppress the interfacial re-oxidation and interface roughness [9–11]. A smoother interface is helpful in reducing the localized field, which can also suppress trap density generation [4]. In consequence, smooth interface between the high-*k* IPD and the poly-Si bottom gate and less trap density generation will inevitably contribute to superior dielectric characteristics when the fluorinated high-*k* IPDs stressed in positive polarity.

Although HfO_2 possesses higher dielectric constant to further increase the gate coupling ratio, the results apparently indicate that Al_2O_3 is more suitable than HfO_2 to be implemented as the IPD of floating-gate flash memory, irrespective of the interfacial

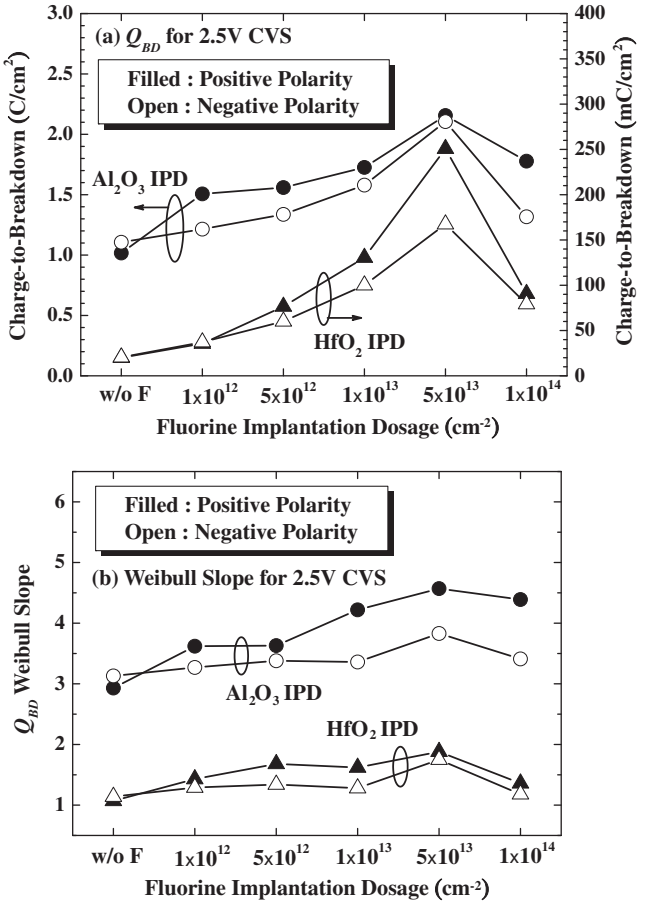

Fig. 6. (a) Charge-to-breakdown and (b) Weibull slope comparison of the fluorinated high-*k* IPDs as a function of fluorine implantation dosage measured at 2.5 V CVS.

fluorination. The dielectric reliabilities of both high-*k* IPDs can be gradually improved while fluorine implantation dosage increasing from 1×10^{12} cm^{-2} to 5×10^{13} cm^{-2}. Nevertheless, the high-*k* inter-poly capacitors exhibit deteriorate dielectric characteristics while the fluorine implantation dosage larger than 1×10^{14} cm^{-2}. Two feasible mechanisms may be responsible for the degradation. First, 950 °C dopant activation annealing may not be sufficient to repair the surface damage of the bottom gate caused by the heavy fluorine implantation dosage, i.e. 1×10^{14} cm^{-2}. Second, fluorine clusters may hypothetically form near the high fluorine concentrated interface, and result in reliability degradation. Consequently, the high-*k* IPDs with fluorine implantation dosage larger than 1×10^{14} cm^{-2} will not only exhibit increased leakage current, but also reduced breakdown field and Q_{BD}.

4. Conclusions

Interface fluorine ion implantation process has been applied to the inter-poly capacitor with either aluminum oxide (Al_2O_3) or hafnium oxide (HfO_2) dielectric to evaluate the electrical properties and dielectric reliabilities. The incorporation of fluorine within the high-*k* dielectrics is helpful to replace low-*k* oxygen vacancies (vacuum) and results in thinner equivalent oxide thickness. In addition, hydrophobic Si–F bond formation during subsequently high-temperature processes is also proved to terminate the interfacial dangling bonds, which can suppose to suppress the interfacial re-oxidation and reduce the interface trap density. Since fluorine is effective to diminish the dangling bonds and oxygen vacancies, the incorporation of fluorine within the high-*k* dielectrics can lower the gate leakage current and extend the breakdown field. Moreover, fluorine incorporation also reduces equivalent oxide thickness and improves charge-to-breakdown. Although fluorinated HfO_2 possesses higher dielectric constant to further increase the gate coupling ratio, the results apparently indicate that fluorinated Al_2O_3 IPD is more suitable than HfO_2 IPD to be implemented to the floating-gate flash memory.

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