

執行期間： 97 年 8 月 1 日至 98 年 7 月 31 日

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中 華 民 國 97 年 10 月 3 日

# 混合測試回應壓密--結合空間壓密器與未知值阻擋多重輸入位移儲存

## “A Hybrid Scheme for Compacting Test Responses with Unknown Values”

計畫編號：NSC96-2221-E-009-233

執行期間：97 年 8 月 1 日 至 98 年 7 月 31 日

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### 一、中文摘要

在輸入圖樣壓縮 (input-stimulus compression) 被廣泛研究之後，測試回應壓密 (test-response compaction) 技術逐漸變成掃描測試中，測試資料縮減的瓶頸。測試回應壓密中最主要的障礙，是在於處理模擬結果中的未知值。在本計畫中，我們提出了一個混合式、可容忍未知值的壓密系統，此系統中包含了一個空間壓密器，以及一個阻擋未知值的多重輸入位移暫存器 (MISR: Multiple-Input-Signature-Register)。首先，此混合壓密系統是獨立於自動測試圖樣產生器 (ATPG) 之外的，任合自動測試圖樣產生器所產生之測試集合都可以當做此混合壓密系統之輸入。其次，此混合壓密系統可以保證，其目標錯誤模型的覆蓋範圍會跟沒有壓密之前一樣。再者，此混合壓密系統可以由使用者任意調整其測試回應所被觀察到之比率，進而使得未被模型化錯誤之覆蓋範圍可以受到控制。為了要決定多少比率之測試回應應該被觀察到，本計畫亦將研發一個具體量化的方法，來求出應被觀察比率之最低門檻，並保證未被模型化錯誤之覆蓋範圍在一可接受之值以上。最後，一個依據此混合壓密系統所設計之偵錯辦法將會被提出。本計畫亦會實做一系列之實驗，來證明此混合壓密系統之有效性，不論在壓縮比率、額外面積負擔、各類模型化錯誤之覆蓋範圍、以及偵錯之解析度，都會和只用空間壓密器或只用阻擋未知值的多重輸入位移暫存器做比較。

### 英文摘要

After the intensive study on input-stimulus compression, test-response compaction gradually becomes the bottleneck of the overall test-data reduction in scan-based testing. The key barrier to effective test-response compaction is the presence of unknown values in the simulation result. In this project, we propose a hybrid, unknown-tolerated scheme for test-responses compaction, which comprises a space compactor and an unknown-blocking MISR (Multiple Input Shift Register). First, the proposed hybrid scheme is ATPG-independent, taking any test set generated by any ATPG tool as input for compaction. Second, the proposed hybrid scheme can guarantee no coverage loss for the target fault model without requiring any extra pattern. Third, the proposed hybrid scheme can be tuned to observe any user-specified percentage of responses for controlling the coverage of un-modeled faults. In order to determine the fraction of responses that should be made observable, a quantitative approach will be developed to identify the threshold of this observable percentage that can ensure an acceptable level of coverage loss. Last, a diagnosis method will be proposed based on the proposed hybrid compaction scheme. A series of experiments will be conducted to justify the effectiveness of the hybrid scheme in terms of the compaction ratio, the area overhead, the coverage loss for various fault models, and the diagnosis resolution. We will also compare the experimental results with those of using a space compactor or an unknown-blocking MISR alone.

### 二、計畫緣由、目的、研究方法與實驗結果

#### 1. Introduction

The increasing number of scan cells in modern designs challenges the scan-based testing on both test data volume and test application time. In order to reduce the test data volume as well as the number of required channels on the ATE, researchers have been actively pursuing new solutions to input stimulus compression and output response compaction. For output response compaction, the presence of unknown values (or unknowns) among the good-circuit test responses has

been the greatest barrier to effective the compaction. If no unknowns exist in the good-circuit responses, a time compactor, such as Multiple Input Signature Registers (MISR), can be used to compact an infinitely long output sequence into a fixed-length signature and guarantee a negligible aliasing probability [1]. Due to feedback loops present in the MISR, however, unknowns in the responses will create an unpredictable good-circuit signature, from which no faulty-circuit signature could be differentiated.

One class of unknown-tolerant compaction schemes is selective compactors [2] [3], which selects a small subset of responses for observation on the ATE channels. Based on the fault simulation results with respect to the target fault model, the selective compactor chooses only those responses containing a D or  $\bar{D}$  value for observation. All other responses are discarded. (In this project, a response specifically refers to the captured value of a scan cell.) Therefore, the presence of unknowns in the responses would not cause problems for the selective compactor. However, an important assumption typically made in structural testing is that the patterns for the target modeled faults often detect many un-modeled faults as well. Also, selective compactors, such as [2] and [3], require a customized ATPG.

Another class of unknown-tolerant compaction schemes is the *unknown-blocking* MISR [4] [5] [6] [7], which adds a blocking logic between the scan chains and the MISR. By assigning proper control signals in the blocking logic, an unknown-blocking MISR could block all unknowns from reaching the MISR while guaranteeing no coverage loss for the modeled faults. The method in [4] focuses on blocking the unknowns and uses a customized ATPG to maintain fault coverage. The test set generated by this customized ATPG may be larger than the test set without applying compaction because the method in [4] also over-blocks some known responses other than unknowns. The methods in [5] [6] and [7] maintain the fault coverage by observing those responses necessary for fault detection while blocking the unknowns. The method proposed in [5] uses an LFSR-reseeding scheme [8] to encode the control signals, which contain many don't-cares, and achieves high encoding efficiency. Due to the LFSR's random-fill nature for the don't-cares, half of the responses would be blocked in addition to the unknowns. The methods proposed in [6] and [7] synthesize a combinational circuit to generate the control signals; however, the values generated for those don't-cares control signals are still uncontrollable. This loss of observability due to the over-blocking of known responses may result in a coverage loss for the un-modeled faults.

Instead of blocking the unknowns, *space compactors* allow unknowns to be processed by the compactor while using an XOR matrix to reduce the probability of a response being masked by the unknowns [9] [10] [11]. The methods proposed in [12] and [13] use storage elements along with an XOR matrix to further improve the compaction ratio and unknown tolerance. The methods proposed in [9], [10], [12] and [13] can guarantee a certain degree of error detection in the presence of one unknown in a scan-shift cycle; however, for high-ratio response compaction, multiple unknowns may arrive at the compactor in the same cycle, which results in some known responses being masked. This observability loss of responses may either decrease the coverage of the modeled faults or require extra patterns to maintain the same level of coverage.

In this project, we propose a hybrid compaction scheme, which consists of a space compactor and an unknown-blocking MISR. This compaction scheme can take any test set generated by any ATPG tool as input for compaction. The space compactor, in this scheme, observes majority of the responses and detects most of the modeled faults. For those modeled faults missed by the space compactor, the unknown-blocking MISR is designed to detect them, by proper value assignments to its control signals. Therefore, the proposed scheme guarantees no coverage loss for the modeled faults without requiring extra patterns. Also, the hybrid scheme can be tuned to observe any user-specified percentage of responses for controlling the coverage loss of the un-modeled faults. The experimental results show that, for the same test set, the coverage loss of the hybrid compaction scheme is always less than that of the scheme when either an unknown-blocking MISR or a space compactor is used alone. Besides, the hybrid scheme does not necessarily require higher test-data volume. To determine the fraction of responses that should be made observable, we further develop a quantitative approach for identifying the threshold of this observable percentage that can ensure an acceptable level of un-modeled-fault coverage loss. In this work, we choose BCE [16] as the coverage metric for un-modeled faults.

## 2. POTENTIAL COVERAGE LOSS OF UNKNOWN-BLOCKING MISRS AND SPACE COMPACTORS

In this section, we show the potential coverage loss for un-modeled faults of an unknown-blocking MISR, which can guarantee no coverage loss for the modeled faults. Figure 1(a) shows an example of an unknown-blocking MISR supporting three scan chains, where the response from *chain<sub>i</sub>* is controlled by the

control signal  $S_i$ . If  $S_i = 0$ , the response from  $chain_i$  propagates to the MISR. If  $S_i = 1$ , the response is blocked and a 1 will be applied to the MISR. With this blocking logic, we can block all unknowns and observe responses critical to fault-detection by assigning proper values to the control signals (0 for observing, 1 for blocking). Here, we define those critical responses with guaranteed observation by a 0 at the control signal as must-observe responses. For responses other than unknowns and must-observe responses, the value at the control signal is a "don't-care". In [5], [6], [7], and this project, the must-observe responses are chosen to insure there is no coverage loss for the modeled faults.

$u$ : unknown value     $m$ : must-observe response

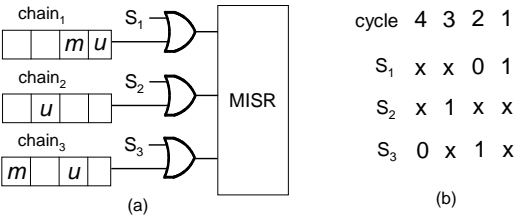


Fig 1. An example of the unknown-blocking MISR.

In practice, only a very small fraction of the responses have an unknown value or must be observed for fault detection. As a result, most control signals of the blocking logic are "don't cares". [5], [6], and [7] utilize these don't-cares for optimization to achieve high encoding efficiency. However, after decoding, some of the don't-cares will be specified as 1; thus, a fraction of the non-critical responses with a known value will be blocked.

We conducted the following experiments to evaluate the potential coverage loss for the un-modeled faults due to the loss of observability for non-critical responses. We used the stuck-at test patterns for this experiment. Two metrics are used to measure the coverage for the un-modeled faults: the transition fault coverage and the BCE [16], which quantifies the effect of multiple detection on a stuck-at fault and approximates the coverage of pair-wise bridging faults. The BCE proposed in [16] is defined as:

$$BCE = \frac{1}{|F|} \sum_{f \in F} \left(1 - \frac{1}{2^{N_f}}\right), \quad (1)$$

where  $N_f$  is the number of detecting patterns for each fault  $f$  and  $|F|$  is the total number of faults.

Four larger ISCAS and ITC benchmark circuits, each of which contains more than 1,000 flip-flops, are used for the experiment. We first generate ATPG patterns for the stuck-at faults. From these patterns, we identify a minimal

set of must-observe responses. For responses other than those identified must-observe responses, we observe them randomly according to a specified percentage (which is called observable percentage and is denoted as  $obs\_p$ ). Based on the selected observation of responses, we then simulate the same stuck-at-fault patterns for the transition faults and for the BCE calculation.

Table I shows the statistics of each circuit. Columns 2 and 3 list the total number of stuck-at-fault patterns and the total number of flip-flops, respectively. Column 4 lists the ratio of the must-observe responses to the total responses. Column 5 lists the number of transition faults. Columns 6 and 7 list the number of detected transition faults and the BCE, respectively, assuming all responses are observed. Table II and Table III shows the coverage loss for the transition faults and for the BCE, respectively, according to each  $obs\_p$ .

circuit	# of s.a. ptn	# of FF	% of must-obs. responses	total trans. flt	detected trans. flt	BCE
s35932	27	2048	15.70	66316	46971	85.95
s38417	189	1742	2.44	53014	43071	95.42
s38584	191	1730	3.81	64162	48485	92.04
b17	536	1512	2.23	117998	85466	86.84

Table I: % of must-observe responses, transition-fault coverage, and BCE for stuck-at-fault patterns.

circuit	must-obs. only	$obs\_p$					
		50%	60%	70%	80%	90%	95%
s35932	22.77	7.37	5.23	3.46	2.06	0.92	0.44
s38417	27.14	1.76	1.22	0.75	0.43	0.2	0.11
s38584	20.66	2.46	1.76	1.01	0.63	0.28	0.13
b17	20.11	3.17	2.23	1.54	0.94	0.43	0.18
avg.	22.67	3.69	2.61	1.69	1.02	0.46	0.22

Table II: Transition-fault coverage loss for different  $obs\_p$

circuit	must-obs. only	$obs\_p$					
		50%	60%	70%	80%	90%	95%
s35932	18.58	5.33	2.75	2.54	1.15	0.69	0.33
s38417	22.55	0.71	0.44	0.27	0.14	0.07	0.03
s38584	20.12	2.09	1.45	0.95	0.57	0.27	0.13
b17	15.15	1.82	1.29	0.86	0.53	0.24	0.10
avg.	19.10	2.49	1.48	1.16	0.60	0.32	0.15

Table III: BCE loss (in %) with respect to different  $obs\_p$

The results in Table II and Table III indicate that observing a large percentage of responses is necessary for maintaining a high test quality. On average, observing only the must-observe responses results in a 22.67% loss of the original transition-fault coverage and a 19.10% loss of the original BCE, even though the stuck-at-fault coverage is not compromised. This implies a potential test-quality loss of using selective compactors [2] [3], which basically observe only the must-observe responses. For an encoding scheme like LFSR reseeding [8], roughly 50% of the responses cannot be observed due to the

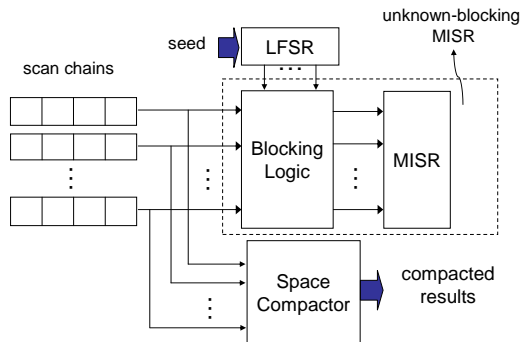
random assignment of the don't-cares. Therefore, it results in average losses of 3.69% and 2.49% in the transition-fault coverage and the BCE, respectively. Note that coverage losses for other un-modeled faults – such as stuck-open, bridging, path delay, and other faults – were not considered in this experiment. It is likely that these losses would be non-trivial as well. Therefore, the test quality loss due to a low observable percentage is significant.

If only a space compactor is applied for response compaction, some responses may not be observed due to unknown-induced masking. These unobservable responses caused by unknown-induced masking tend to be randomly distributed, and hence lead to the coverage losses among both modeled and un-modeled faults. The percentage of observable responses is determined both by the configuration of the space compactor and by the fraction of the responses having an unknown value [14] [15]. The coverage loss caused by a space compactor is inversely proportional to the observable percentage [15].

### 3. Hybrid Compaction Using Unknown-Blocking MISR AND Space Compactor

#### 3.1 Basic Concept

Figure 2 illustrates the basic concept of the proposed hybrid scheme. The responses from the scan chains concurrently propagate to a space compactor and an unknown-blocking MISR. Through the space compactor, we observe most responses and detect most of the modeled faults. For those modeled faults that may not have been detected by the space compactor, we assign proper values at the control signals of the unknown-blocking MISR to detect them. The value assignments at the control signals also ensure that all unknowns are blocked from reaching the MISR. For the unknown-blocking MISR part, we use an LFSR to encode the control signals [8]. For the space compactor part, we use a single-weight space compactor, for which every column of the XOR matrix has the same number of XOR gates.



**Figure 2.** Proposed compaction scheme using space compactor and unknown-blocking MISR

The overhead of the test data volume for the unknown-blocking MISR part depends upon the size of the LFSR seed for each pattern as well as upon the size of the good-circuit signature of the MISR, which is used for signature comparison after all patterns are applied. For the space-compactor part, we need to store each pattern's compacted good-circuit responses. Therefore, for this compaction scheme, the total storage required on ATE is mainly determined by the LFSR seeds and the compacted good-circuit responses of the space compactor. The good-circuit signature of the MISR is a single signature for the entire pattern set. Hence its data size is negligible, in comparison with the other test data sources.

As discussed in Section II, an unknown-blocking MISR can guarantee no coverage loss for the modeled faults, but about half of the responses would be blocked. A space compactor might incur fault coverage loss, yet observe a majority of the responses. Therefore, by using both techniques concurrently, we can achieve the goals of no loss of the modeled-fault coverage and observe most responses. Using the unknown-tolerance analysis proposed in [15], we construct a space compactor which can achieve a user-specified level of observable percentage with a maximal compaction ratio. Because most modeled faults are already detected by the space compactor, the number of must-observe responses for the unknown-blocking MISR is significantly reduced. The length of the required LFSR stages would also be much smaller than those that might use only an unknown-blocking MISR. Hence, the overall test data volume of the hybrid scheme might be even less than that required by the unknown-blocking-MISR-only scheme.

Furthermore, this hybrid scheme is ATPG-independent. The test patterns used for this compaction scheme are exactly the same as those patterns without compaction – no extra patterns are needed. Therefore, any ATPG tool can be directly used without modification

#### 3.2 Design Flow of the Hybrid Compaction Scheme

The input parameters of our hybrid compaction scheme include: (1) the target fault model, (2) the target observable percentage (denoted as *hybrid\_obs\_p*), and (3) the number of ATE channels available for observing the outputs of the space compactor (M). The design procedure for a hybrid compactor is summarized as follows:

Step 1: Based on the given *hybrid\_obs\_p*, compute the target observable percentage for the space compactor

(denoted by  $space\_obs\_p$ ) using the following equation:

$$space\_obs\_p = 2 \cdot hybrid\_obs\_p - 1 \quad (2)$$

The rationale behind Equation 2 is that the LFSR for the unknown-blocking MISR generates the control signals which results in roughly 50% observable responses. For example, if  $hybrid\_obs\_p = 0.9$ , we should design a space compactor to observe 80% of the responses and an unknown-blocking MISR to observe half of the remaining 20%. Jointly, the overall observable percentage would be 90%.

Step 2: Generate ATPG patterns for the modeled faults and run logic simulation with these pattern to derive the percentage of unknowns among all responses ( $xp$ ).

Step 3: Based on  $space\_obs\_p$ ,  $M$ , and  $xp$ , design a space compactor that supports a maximal number of scan chains ( $S$ ) while achieving  $space\_obs\_p$ .

Step 4: Divide the scan cells into  $S$  scan chains whose outputs are connected to the inputs of the space compactor.

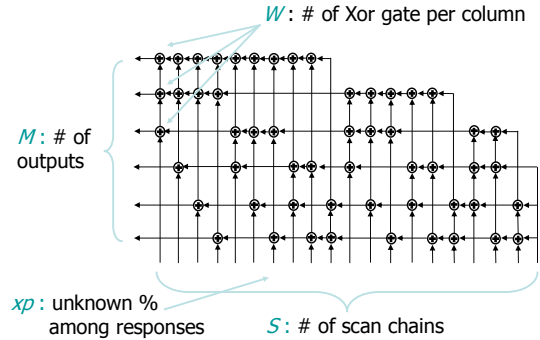
Step 5: Run fault simulation for the modeled faults using the ATPG patterns. The circuit model used for fault simulation includes both the circuit-under-test (CUT) and the space compactor. That is, a fault is considered detected only if its fault effect appears at an output of the space compactor. Because the space compactor only observes  $space\_obs\_p$  of the responses, some faults detected at the CUT outputs become undetected at the space compactor outputs. Record those undetected faults.

Step 6: Identify the must-observe responses based on the simulation results of those undetected faults. Generate LFSR seeds for supplying the control signals of the unknown-blocking MISR, which will be used to observe those must-observe responses and to block all unknowns. In our experiment, we apply the method proposed in [17] to minimize the number of LFSR stages LS required.

Step 7: Build the blocking logic and the LFSR with LS stages. In the above procedure, Steps 3 and 6 are two keys to maximizing the compaction ratio and achieving the target observable percentage. Regarding Step 3, a single-weight space compactor is chosen in our hybrid compaction scheme. X-Compactor [9] is the representative of single-weight space compactors. However, the construction rules for our XOR matrix are different from those of the X-Compactor, for which each

column has a unique combination of output connection and the weight (i.e. the number of XOR gates in each XOR-matrix's column) has to be an odd number. These two rules, while minimizing the error masking probability (a.k.a. aliasing probability), do not necessarily reduce the probability of unknown-induced masking. For a space compactor, the unknown-induced masking impacts more on the fault detection than the error masking does [15]. Therefore, to minimize the unknown-induced masking probability, we allow the use of identical columns and an even weight.

When applying a single-weight space compactor, its corresponding observable percentage depends upon the values of the following four parameters: (1)  $S$ , the number of scan chains connecting to the compactor, (2)  $M$ , the number of outputs of the compactor, (3)  $W$ , the number of XOR gates in each XOR-matrix's column, and (4)  $xp$ , the probability that a response has an unknown value. Among these four parameters,  $S$ ,  $M$ , and  $W$  relate to the configuration of the space compactor.  $xp$  relates to the given CUT and test patterns. Figure 3 uses a 20-to-6 single-weight space compactor to illustrate these parameters. In this example,  $S = 20$ ,  $M = 6$ , and  $W = 3$ .



**Figure 3.** An Example single-weight space compactor.

To construct a space compactor supporting a maximal number of scan chains while achieving  $space\_obs\_p$  (Step 3), we rely on Equation 3 (derived in [15]) to predict its observable percentage. The equation of this predicted observable percentage (OP) is:

$$OP = 1 - \sum_{j=0}^W (-1)^j \cdot \binom{W}{j} \cdot (xp \cdot \frac{\binom{M-j}{W}}{\binom{M}{W}} + 1 - xp)^S \quad (3)$$

Using this equation for fast prediction, we can efficiently list the predicted observable percentage with respect to each unique combination of both the weight and the number of scan chains for the given  $M$  and  $xp$ . We then search for the configuration with the largest number of scan chains ( $S$ ) that achieves the target observable percentage  $space\_obs\_p$ . This search is

straight forward and fast.

For minimizing the must-observe responses (Step 6), we employ the two-pass, fault-simulation-based method proposed in [17]. It runs fault simulation twice for a given fault set – in this case, the faults not detected by the space compactor – with respect to two different pattern orders. In the first pass, the patterns are fault-simulated, with fault dropping, according to the original pattern order, that is, from  $T_1$  to  $T_N$  for an  $N$ -pattern test set. The list of detected faults,  $FL_i$ , for each pattern  $T_i$  is recorded. In the second pass, fault simulation is performed again, but in reverse order, from  $T_N$  to  $T_1$ . For each pattern  $T_i$  in this reversed-ordered simulation, we attempt to identify those responses which should be observed so that, in addition to the faults in the detected fault list of the current pattern  $FL_i$ , some faults in the detected fault lists of prior patterns ( $FL_{i-1}, FL_{i-2}, \dots, FL_1$ ) can be detected. Those detected faults in the  $FL_{i-1}, FL_{i-2}, \dots, FL_1$ , can then be removed. This will result in a smaller or even empty fault list when we subsequently fault-simulate these prior patterns  $T_j$  for  $j < i$ . With this method, the number of must-observe responses can be reduced.

## 4. Experimental Results

### 4.1 Hybrid vs. Unknown-Blocking MISR alone

We first conducted experiments on the four larger ISCAS and ITC circuits shown in Table I. This experiment randomly assigned 0.5% of clustered unknowns in the responses – specifically, 90% of unknowns from 10% of the scan chains. The number of outputs for the space compactor is four. Row 2 of Table IV reports the test data volume required by the hybrid scheme for circuit s35932. The target observable percentages of the hybrid scheme is set at 90%. Columns 3 (# of chains) and 4 (weight) show the number of supported scan chains and the weight of the identified optimal configuration of the space compactor. Column 5 (chain depth) lists the depth of the scan chains. Column 6 (space) lists the number of bits that need to be stored in ATE for the space compactor for each pattern, which is the number of outputs times the chain depth. Column 7 (lfsr) lists the length of an LFSR seed, which is used for encoding the control signals. Column 8 (total) is the sum of Columns 6 and 7, which indicates the total number of storage bits of the hybrid scheme for each pattern. Column 9 (comp. ratio) reports the compaction ratio, which is the total number of scan cells divided by Column 8. In Table IV, we compare our results with those using only the unknown-blocking MISR [17] (denoted as x-block in Row 3). Table V reports the results for s38417, s38584, and b17 with respect to the same unknown percentage, number of outputs, and target observable

percentage.

desired obs. %	# of output	# of chain	weight	chain depth	storage bits per ptn			comp. ratio
					space	lfsr	total	
90%	4	180	2	12	48	45	93	22.0
x-block (unknown-blocking MISR only)					0	248	248	8.3

**Table IV.** Data Volume of the hybrid compaction scheme and x-block for circuit s35932 with 0.5% unknowns

circuit	method	chain depth	storage bits per ptn			comp. ratio
			space	lfsr	total	
s38417	hybrid-90%	10	40	30	70	24.9
	x-block	–	0	32	32	54.4
s38584	90%	10	40	22	62	27.9
	x-block	–	0	78	78	22.2
b17	90%	9	36	29	65	23.3
	x-block	–	0	58	58	26.1

**Table V.** Data Volume of the hybrid compaction scheme and x-block for circuit s38417, s38584, and b17 with 0.5% unknowns

Table VI shows the actual observable percentage, the coverage loss for the transition faults, and the BCE loss corresponding to the hybrid scheme and the x-block, considered in Tables IV and V.

circuit	method	actual obs. %	tran. flt cov. loss (%)	BCE loss (%)
s35932	hybrid-90%	90.67	1.45	0.96
	x-block	56.58	6.83	5.00
s38417	hybrid-90%	90.14	0.28	0.10
	x-block	50.46	1.78	0.81
s38584	hybrid-90%	90.10	0.33	0.38
	x-block	53.26	2.60	2.45
b17s	hybrid-90%	90.39	0.51	0.28
	x-block	52.78	2.87	1.75
average	hybrid-90%	–	0.64	0.43
	x-block	–	3.52	2.50

**Table VI.** Actual observable percentage, transition-fault-coverage loss, and BCE loss (in %) with 0.5% unknowns

The results in Table VI indicate that the hybrid compaction scheme can meet the target observable percentage, which verifies the accuracy of our construction procedure. Also, the coverage loss of the hybrid scheme is much less than that of the unknown-blocking-MISR-alone scheme, which we will refer to as x-block. The average loss of the transition-fault coverage is 0.64% for the hybrid scheme, but 3.52% for the x-block. The average loss of BCE is 0.43% for the hybrid scheme, but 2.50% for the x-block. These results confirm the advantage of observing the majority of responses.

The results shown in Tables IV and V also indicate



that observing a higher percentage of the responses does not necessarily require more test data. The hybrid scheme achieves an even greater compaction ratio than when using the unknown-blocking-MISR-only scheme for circuits s35932 and s38584. This is because the use of a space compactor reduces the number of must-observe responses for the unknown-blocking MISR, and in turn reduce the number of specified bits for the LFSR control signals. This reduction in the number of specified bits for the unknown-blocking MISR could be more than the number of additional storage bits required for the added space compactor.

This phenomenon of achieving a better compaction ratio will become more significant if the unknown percentage decreases. This is because a space compactor cannot reduce the number of specified bits for blocking unknowns. If the majority of the specified bits of the LFSR control signals are for blocking the unknowns, adding a space compactor could only modestly help improve the compaction ratio. In Table XII, we apply different unknown percentages and observe the changes in compaction ratios for both the hybrid scheme and x-block. Take s35932, for example. When the unknown percentage drops from 0.5% to 0.1%, the compaction ratio for the hybrid scheme increases from 22.0 to 41.8; however, for x-block, the increase of the compaction ratio is modest - from 8.3 to 9.2. For the other three circuits, a similar trend is observed.

circuit	method	unknown %		
		0.5	0.3	0.1
s35932	hybrid-90%	22.0	36.6	41.8
	x-block	8.3	8.4	9.2
s38417	hybrid-90%	24.9	39.6	60.1
	x-block	54.4	62.2	72.6
s38584	hybrid-90%	27.9	40.2	64.1
	x-block	22.2	22.5	26.6
b17s	hybrid-90%	23.3	28.0	39.8
	x-block	26.1	27.5	28.5

**Table VII.** Compaction ratio with respect to different unknown %s.

## 4.2 Hybrid vs. Space Compactor alone

Table VIII compares the hybrid compaction scheme with X-Compact [9]. For a fair comparison, we designed an X-compactor for each circuit that achieves the same compaction ratio as that of the hybrid scheme. Column 4 lists the number of required ATE channels. We attempted to design the X-compactor by using the same number of ATE channels as that of the hybrid scheme; however, no such X-Compact can achieve the target compaction ratio. Thus, Table VIII reports the results of X-Compact that uses the fewest number of ATE channels to achieve the

same compaction ratio as that of the hybrid scheme.

Columns 5, 6, and 7 in Table VIII list the coverage loss for the stuck-at faults, the transition faults, and the BCE, respectively. The results show that the X-Compact incurs some coverage loss for the stuck-at faults while the hybrid scheme has no loss at all. The hybrid scheme also achieves less coverage loss for the transition faults and the BCE for most circuits, save for s35932. Note that X-Compact uses more ATE channels than the hybrid scheme. This experiment demonstrates that the hybrid scheme can provide better test quality than when a space compactor alone is used, given the same test data volume and the same number of ATE channels.

## 4.3 Industrial Design

We conducted further experiments on two industrial designs. Table IX lists the statistics for these two designs. For this experiment, we used a space compactor with eight outputs. The target observable percentage is set at 90% and the unknown percentage is 0.3%.

circuit	comp. ratio	method	# of channel	s.a. flt cov. loss (%)	tran. flt cov. loss (%)	BCE loss (%)
s35932	22.0	hybrid-90%	8	0	0.96	1.45
		X-Compact	10	0.29	0.93	1.17
			8,9	no available configuration		
s38417	24.9	hybrid-90%	7	0	0.10	0.28
		X-Compact	10	0.17	0.24	0.41
			7,8,9	no available configuration		
s38584	27.9	hybrid-90%	7	0	0.38	0.33
		X-Compact	11	0.40	0.73	0.90
			8,9,10	no available configuration		
b17s	23.3	hybrid-90%	7	0	0.28	0.51
		X-Compact	10	0.40	0.60	0.98
			7,8,9	no available configuration		

**Table VIII.** Coverage loss of the hybrid compaction scheme and X-compact with 0.5% unknowns.

Table X lists the actual observable percentage (Column 3), the coverage loss for the transition faults (Column 4), the BCE loss (Column 5), the number of supported scan chains (Column 6), and the compaction ratio (Column 7). Again, the results validate that our hybrid scheme can meet the target observable percentage and can thus limit the loss of test quality for large industrial designs.

bench	gate count	# of scan cell	# of ATPG pattern	# of ATPG-detected flt
D1	722K	4990	542	985234
D2	870K	65560	1514	1835582

**Table IX.** Characteristics of two industrial designs.



circuit	desired obs. %	actual obs. %	tran. flt cov. loss (%)	BCE loss (%)	# of chains	comp. ratio
D1	90%	91.92	0.06	0.05	710	39.3
D2	90%	90.41	0.53	0.33	710	63.1

**Table X.** The observable percentage, coverage loss, and compaction ratios for two industrial designs.

Table XI reports the area overhead and runtime of the proposed hybrid scheme. The figures for area are reported by Synopsys DesignCompiler [18]. The unit for the area is the gate equivalent area. Column 2 lists the area of the original design. Columns 3 and 4 list the area of the space compactor and the unknown-blocking MISR, respectively, in the hybrid scheme. Column 5 lists the total area of the hybrid compaction scheme (sum of Columns 3 and 4). Column 6 lists the area overhead in percentages with respect to the original area. Column 7 lists the runtime of the construction flow in seconds. The total area overhead is 0.92% and 1.14% respectively for these two designs. In the experiment, the hybrid scheme supports 710 scan chains for both designs. Note that a larger number of scan chains would result in a higher area overhead while a shorter test application time, compared to the same design with fewer scan chains. With this large number of scan chains, the overhead is still quite low, which indicates that the area overhead should not be a concern for the proposed scheme. The reported runtime also shows that the construction flow of the hybrid scheme is scalable for industrial designs.

The runtime reported in Table XI was mainly spent on the stuck-at-fault simulation (Step 5 in Section III-B) and the identification of a minimal set of must-observe responses (Step 6 in Section III-B). The sizes of the stuck-at-fault set are about 1 million and 2 million respectively for D1 and D2. The reported runtime shows that the construction flow of this hybrid scheme is scalable for industrial designs.

circuit	original design area	hybrid compaction scheme				runtime (sec)
		space comp.	x-blocking MISR	total area	total area overhead %	
D1	3086752	12166	16119	28285	0.92	3633
D2	3710920	12166	30017	42183	1.14	24350

**Table XI.** Area and runtime overhead for two industrial designs.

## 5. Determine Observable Percentage Based On Un-Modeled-Fault Coverage

The results in Table II and III have shown that, even for a fixed observable percentage of a compaction scheme, the coverage loss for the un-modeled faults is both circuit and test-set dependent. An observable percentage may result in an acceptable coverage loss for some circuits

while an unacceptably high loss for other circuits. In this section, we describe a quantitative approach for identifying a proper threshold for the observable percentage to ensure an acceptable level of coverage loss.

The BCE is chosen as the metric of un-modeled-fault coverage for finding this threshold. We use a fault-simulation-based method to predict the BCE for different observable percentages. The inputs for this prediction method include the circuit under test, a test set, and a list of observable percentages. The output is a predicted BCE for each of the observable percentages in the list. In this prediction method, we first fault-simulate the given pattern set assuming all responses are observable. During the fault simulation, we collect two additional statistics for each fault  $f$ . The first statistic is  $DN_f$ : the number of patterns in the test set detecting  $f$ . The second statistic is  $ON_f$ : the total number of faulty responses (denoted as observation outputs) in all scan cells that fault  $f$  produces for the entire test set. After fault simulation, we calculate the BCE for each observable percentage  $op$  based on the  $DN_f$  and  $ON_f$  statistics. The BCE proposed in [16] is defined as:

$$BCD = \frac{1}{|F|} \sum_{f \in F} \left(1 - \frac{1}{2^{N_f}}\right), \quad (4)$$

where  $N_f$  is the number of detecting patterns for each fault  $f$  and  $|F|$  is the total number of faults.  $N_f$  is equal to  $DN_f$  if all responses can be observed. In the following section, we attempt to calculate the expectation of the BCE function for fault  $f$  (denoted as  $BCE_f = 1 - 0.5^{N_f}$ ), for a given observable percentage  $op$ ,  $DN_f$ , and  $ON_f$ .

For each detecting pattern  $pn$  of fault  $f$ , the probability that  $f$  remains detected under the observable percentage  $op$  (denoted as *detecting probability*) depends on the number of faulty responses that pattern  $pn$  produces in the scan cells (denoted as *observation outputs*).

We first make an approximation that the number of observation outputs for each detecting pattern  $pn$  is the same for a given fault  $f$ , which is close to the real case based on our experimental results. Then we use  $a_f$  to represent the detecting probability of each detecting pattern  $pn$  for fault  $f$ :

$$a_f = 1 - (1 - op)^{\frac{ON_f}{DN_f}} \quad (5)$$

If the responses are observed randomly, we could model  $N_f$  in Equation 4 using the following binomial

function:

$$\text{Prob}\{N_f = n\} = \binom{DN_f}{n} \cdot (a_f)^n \cdot (1-a_f)^{DN_f-n} \quad (6)$$

In the proposed hybrid compaction scheme, however, the responses are not observed pure-randomly. For a fault not detected by the space compactor, we will specify a control signal for the unknown-blocking MISR to detect it. This implies that the number of detecting patterns for any fault can never be 0. Thus, we need to move the probability of  $N_f = 0$  in Equation V to the probability of  $N_f = 1$ . Therefore, the probability density function  $\text{Prob}\{N_f = n\}$  becomes:

$$\begin{cases} \binom{DN_f}{n} \cdot (a_f)^n \cdot (1-a_f)^{DN_f-n} : 2 < n < DN_f \\ DN_f \cdot a_f \cdot (1-a_f)^{DN_f-1} + (1-a_f)^{D_f} : n = 1 \end{cases}$$

The above probability density function represents a lesser estimation of the  $N_f$  because observing a response for detecting a previously undetected fault may detect some other detected faults as well. A lower bound of the expectation of the BCE function (denoted as  $\text{BCE\_L}_f$ ) is obtained based on the above density function:

$$\begin{aligned} E[\text{BCE\_L}_f] &= \sum_{n=1}^{DN_f} \left(1 - \frac{1}{2^n}\right) \cdot \text{Prob}\{N_f = n\} \\ &= 1 - \left(1 - \frac{a_f}{2}\right)^{DN_f} + \frac{1}{2} (1-a_f)^{DN_f} \end{aligned} \quad (7)$$

Then, we derive an upper bound of the BCE function by moving the probability of  $N = n$  to the probability of  $N = n + 1$  for each  $n$ . The expectation of the  $\text{BCE\_U}_f$  is:

$$\begin{aligned} E[\text{BCE\_U}_f] &= \sum_{n=1}^{DN_f+1} \left(1 - \frac{1}{2^n}\right) \cdot \text{Prob}\{N_f = n\} \\ &= 1 - \frac{1}{2} (1-a_f)^{DN_f} \end{aligned} \quad (8)$$

This upper bound  $\text{BCE\_U}_f$  is too loose, however, because  $N_f = DN_f + 1$  can never happen – even if all responses are observed. So we set the probability of  $N_f = DN_f + 1$  to 0 and normalize the probabilities of other values of  $N_f$  such that the summation of this probability density function is 1. The revised probability density function becomes (for  $1 < n < DN_f$ ):

$$\text{Prob}\{N_f = n\} = \binom{DN_f}{n-1} \cdot (a_f)^{n-1} \cdot \frac{(1-a_f)^{DN_f-n+1}}{1 - (a_f)^{DN_f}}, \quad (9)$$

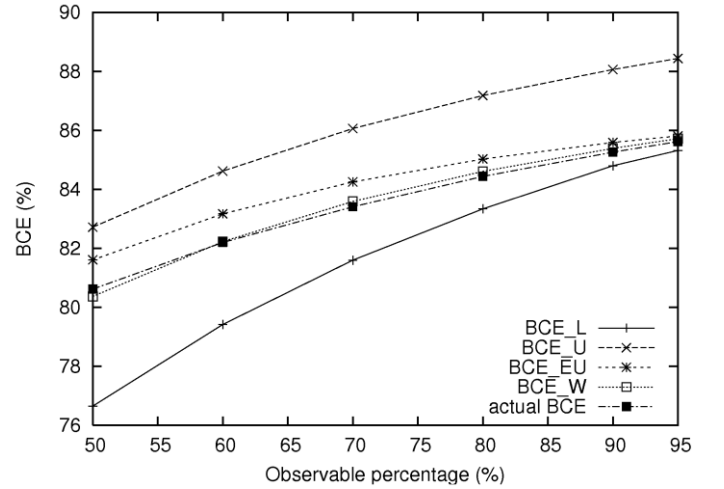
With this density function, we obtain a tighter upper bound for the BCE function (denoted as  $\text{BCE\_EU}_f$ ) as follows:

$$\begin{aligned} E[\text{BCE\_EU}_f] &= \sum_{n=1}^{DN_f} \left(1 - \frac{1}{2^n}\right) \cdot \text{Prob}\{N_f = n\} \\ &= 1 - \frac{1}{2 - 2 \cdot (a_f)^{DN_f}} \left\{ \left(1 - \frac{a_f}{2}\right)^{DN_f} - \left(\frac{a_f}{2}\right)^{DN_f} \right\} \end{aligned} \quad (10)$$

Our experimental results show that the actual BCE is closer to the  $\text{BCE\_EU}$ , rather than the  $\text{BCE\_L}$ . We use an empirical weighted function (denoted as  $\text{BCE\_W}$ ) to approximate the BCE:

$$\text{BCE} = \frac{1}{4} \text{BCE\_EU} + \frac{3}{4} \text{BCE\_L} \quad (11)$$

Figure 4 shows the values of  $\text{BCE\_L}$ ,  $\text{BCE\_EU}$ ,  $\text{BCE\_W}$ , and the actual BCE for different observable percentages for circuit s35932. The results indicate that the actual BCE is well-bounded by  $\text{BCE\_L}$  and  $\text{BCE\_EU}$ , and can be roughly approximated by  $\text{BCE\_W}$ . Also,  $\text{BCE\_U}$  is a much looser upper bound than  $\text{BCE\_EU}$ .



**Fig 4.** BCE prediction for s35932.

circuit	BCE	observable %					
		50%	60%	70%	80%	90%	95%
s38417	<i>BCE_L</i>	94.02	94.52	94.87	95.12	95.30	95.37
	<i>BCE_EU</i>	94.81	95.05	95.21	95.32	95.40	95.41
	<i>BCE_W</i>	94.61	94.92	95.13	95.27	95.38	95.40
	actual BCE	94.71	94.98	95.15	95.28	95.35	95.39
s38584	<i>BCE_L</i>	88.57	89.62	90.44	91.10	91.64	91.86
	<i>BCE_EU</i>	90.46	91.03	91.43	91.71	91.92	92.00
	<i>BCE_W</i>	89.99	90.68	91.18	91.56	91.85	91.97
	actual BCE	89.97	90.61	91.11	91.49	91.79	91.93
b17	<i>BCE_L</i>	84.09	84.89	85.53	86.06	86.49	86.68
	<i>BCE_EU</i>	85.61	86.04	86.36	86.58	86.76	86.80
	<i>BCE_W</i>	85.23	85.75	86.15	86.45	86.69	86.77
	actual BCE	85.26	85.72	86.09	86.38	86.63	86.75

**Table XII.** BCE prediction for s38417, s38584, and b17.

Simulation for the BCE calculation takes longer than the simulation for the stuck-at-fault coverage calculation. For the BCE calculation, a fault cannot be dropped until the number of detections exceeds a threshold when the change of BCE resulting from any more detections of the fault can be ignored. In the proposed prediction scheme, we drop a fault with more stringent constraints because we need to consider the accuracy of the BCE's for all *op*'s in the given list. In this case, the threshold of the number of detections for fault-dropping depends on the predicted BCE of the lowest *op* (50% at least). Note that the most time-consuming part of the proposed prediction scheme is fault simulation. Calculating the predicted BCE for each *op* based on the above equations takes only a very small fraction of the total runtime.

Table XIII lists the runtime of the original BCE calculation (a) and our prediction scheme for 20 *op*'s (b), and for 40 *op*'s (c). The results show that the extra runtime required for the proposed prediction scheme is quite low, in comparison with the original BCE calculation. Also, adding more *op*'s in the list requires little extra runtime.

ckt	original (a)	20- <i>op</i> prd. (b)	40- <i>op</i> prd. (c)	(b)-(a)	(c)-(b)
s35932	6.2	7.8	9.8	1.6	2.0
s38417	22.5	24.2	24.7	1.7	0.5
s38584	18.2	20.9	21.6	2.7	0.7
b17	115.7	120.9	121.9	5.2	1.0

**Table XIII.** Runtime comparison (in seconds) between original BCE simulation and prediction scheme.

### 三、結論

We proposed a hybrid compaction scheme that can guarantee no coverage loss for the modeled faults and that can achieve any target observable percentage. The experimental results show that the proposed hybrid scheme can significantly reduce the coverage loss for the

un-modeled faults with respect to a stuck-at-fault test set when compared with the unknown-blocking-MISR-alone scheme or the space-compactor-alone scheme. In addition, the required test data volume might also be reduced, especially if the percentage of responses having an unknown value is low. We also developed a quantitative approach to determine the threshold for the required observable percentage directly based on a test-quality metric for the un-modeled faults.

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