行政院國家科學委員會專題研究計畫　期中進度報告

子計畫三：前瞻性三維微波被動元件與膜組研發(2/4)

計畫類別：整合型計畫
計畫編號：NSC94-2752-E-009-003-PAE
執行期間：94 年 04 月 01 日至 95 年 03 月 31 日
執行單位：國立交通大學電信工程學系(所)

計畫主持人：鍾世忠
共同主持人：彭松村，郭仁財，張志揚
計畫參與人員：何丹雄、王侑信、金國生、江孟駿、邱逸群、王士鳴、廖竟谷、紀佩綾、許志偉、江俊賢、張鈞富、林克強、陳煥能、許敦智、徐民峰、沈彥圻、王自強、蔡致遠、陳啟興、蔡明澤、許富傑、鄭森豪、吳孟桓、陳諭正...等

報告類型：完整報告
報告附件：出席國際會議研究心得報告及發表論文
處理方式：本計畫可公開查詢

中　華　民　國 95 年 3 月 14 日

Principal Investigator's Midterm Report
Explanation for the Form of the Midterm Report "Program for Promoting Academic Excellence of Universities（Phase II）"（April 2004~February 2006）

※ The Midterm Report contains the following sections:

COVER

Program for Promoting Academic Excellence of Universities

（Phase II）

Midterm Report

子計畫三：前瞻性三維微波被動元件與模組研發

Sub- project 3：Advanced Tri-Dimensional Microwave Passives and Modules

(Serial No. :NSC93-2752-E009-002-PAE)
(Serial No. :NSC94-2752-E009-003-PAE)

Overall Duration: Month April Year 2004 - Month March Year 2008
Midterm Duration: Month April Year 2004 - Month February Year 2006

National Chiao Tung University
2006/02/28

I. BASIC INFORMATION OF THIS SUB-PROJECT (FORM 1)

Project Title:前瞻性三維微波被動元件與模組研發−Advanced Tri-Dimensional Microwave Passives and Modules					
Serial No.: :NSC94-2752-E009-003-PAE			Affiliation		National Chiao Tung University 國立交通大學
Principal Investigator	Name	Shyh-Jong Chung 鍾世忠	Project Coordinator	Name	Shyh-Jong Chung 鍾世忠
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	Expenditures[1] (in NT$1,000)		Manpower[2]:Full time/Part time(Person-Months)	
	Projected	Actual	Projected	Actual
FY2004	**10,491**	**10,084**	**400**	**455**
FY2005	**11,292**	**10,076**	**460**	**505**
FY2006	**12,373**	**-**	**484**	**-**
FY2007	**11,737**	**-**	**506**	**-**
Overall	**45,893**	**20,160**	**1850**	**960**

Notes: [1,2] Please explain large differences between projected and actual figures.

Principal Investigator's Signature:

II. Executive Summary on Research Outcomes of this Project (Form 2)

1. General Description of the Project

Sub-project 3 focuses on the development of new miniaturized three-dimensional microwave components and antennas in multi-layered structures, and exploits the integration technologies to realize the concept of AMSOP (Advanced Microwave tri-dimensional System-On-Package). Development of microwave circuits and antennas in three dimensions has a large flexibility in circuit design to achieve goals in circuit miniaturization, performance enhancement, and system integration. Various innovative three dimensional microwave passive components are to be designed and implemented by using the multi-layer processes such as LTCCs, multi-layer thin-films, and multi-layer PCBs. In most applications, the passive circuits and the signal distribution networks constitute a large fraction of the total circuitry. Passive components can be integrated and embedded inside a multi-layered substrate using the 3-D configuration to save a lot of circuit real estate, increase the packaging density, and reduce the insertion losses at connection points between discrete components and the substrate. Since the design degree of freedom increases, these circuits may have not only smaller sizes, but also better performance. Moreover, we can integrate the new miniaturized passive components, the miniaturized antennas, and the active components into a multi-layer substrate RF module, to realize the AMSOP.

Besides, technology of nanoscale CMOS devices and circuits are explored. In the part of nanoscale CMOS device, we study the new device structure and new semiconductor materials for pursuing high performance VLSI devices. According to our 3D simulation platform, omega- and surrounding-gate nanowire MOSFETs are designed and simulated using full quantum mechanical transport model. A new nanowire FinFET structure is successfully developed for CMOS device scaling into the sub-10 nm regime. Accumulation mode P-type MOSFET and inversion mode N-type MOSFET with 5 nm and 10 nm physical gate length, respectively, are fabricated. N-type MOSFET gate delay (CV/I) of 0.22 ps and P-type MOSFET gate delay of 0.48 ps with excellent subthreshold characteristics are simultaneously achieved, both with very low off leakage current less than 10 nA/μm. Nanowire FinFET device operation is also explored using 3-D full quantum mechanical simulation. On the other hand, effect of random fluctuation on degradation of electrical characteristics is investigated with perturbation technique and quantum correction model. Reduction of fluctuation is significantly achieved, which directly benefits the mass production of sub-45 nm technology and semiconductor foundry industry.

2. Breakthroughs and Major Achievements

I. Various novel miniaturized filter configurations usng three-dimensional structures have been proposed and demonstrated, including dual-passband quasi-elliptic filters, single- and dual-bandpass filters of serial-configuration using LTCC technology, vertically installed planar (VIP) filters, and several modified parallel coupled-line filters with excellent performance.

II. Multi-dimensional full quantum transport modeling and simulation for nanoelectronics has successfully been developed. We have applied the developed CAD platform to perform the world-wide smallest transistor's simulation. It is a silicon nanowire FinFET with 5 nm gate length. The quantum mechanical theory and perturbation solution methodology for the random

dopant-induced fluctuation in electrical characteristics of nanoscale VLSI devices is also presented. According to our work on the quantum correction models to single and infinite gate FETs, a novel analyzing technique is proposed. Within minute's simulation time, this approach enables us to explore device characteristic fluctuation with channel length scaling down to 5 nm. The proposed theoretical approach has experimentally been verified with realistic sub-45nm VLSI CMOS devices at TSMC.

3. CATEGORIZED SUMMARY OF RESEARCH OUTCOMES.

The summaries of the research outcomes are as follows: (For more details, please see Appendix VI.)

First year:

I. Novel Miniaturized Filters and Modules

This sub-project has investigated the innovative miniaturized LTCC multi-layer modules with dual-band response. This module integrates passive components and active components into a package. Besides, a novel band-pass filter of serial-configuration has been proposed and demonstrated. This serial-configuration concept can be clearly extend for two serially-connected 2-port networks with opposite reactance to produce finite transmission zeros. On the other hand, we also design a quasi-elliptic function filter (with cross coupling) with a dual-passband response. A design method for parallel-coupled line filter on a suspended structure with suppression of the second harmonic has been present. A filter design method for coupled stages with arbitrary image impedances is also developed.

II. Broadband and Multi-band Antennas on small ground plane

Two multi-band antennas on small ground plane have been proposed. Both the measured radiation patterns are well-behaved with high antenna gains and are nearly omni-directional at specified frequencies. Also, both the measured return losses are found to be well-behaved for enough -10 dB bandwidths. In addition, we have designed a simple barrier structure in between two closely-spaced diversity antennas for decreasing the mutual coupling between antennas. The measured results show that, without deteriorating the antennas' performance, the isolation is improved to be better than 13 dB at the two operating bands.

III. Vertically Installed Planar (VIP) components

During this year, we have developed some tri-dimensional circuits. The vertically installed planar (VIP) circuits are one of them. An octave bandwidth VIP filter using step impedance resonator (SIR) technology has been developed. The filter shows more than an octave bandwidth, and the upper stopband rejection is higher than 40dB. Among these researches, "Broadband VIP filter" is the most significant application of VIP structure for solving most difficult part to realize an octave bandwidth planar filter. "Harmonic passband suppression filter using meandered coupled-lines" not only largely shrinks the size of a conventional parallel-coupled filter but also drastically improves the upper stopband rejection.

IV. Optimal structure design for high-speed nanowire FETs

Multi-dimensional full quantum transport modeling and simulation for nanoelectronics has successfully been developed. We have applied the developed CAD platform to perform the world-wide smallest transistor's simulation. It is a silicon nanowire FinFET with 5 nm gate length. Our hybrid intelligent optimization prototype can perform global model parameter optimization so that a set of optimized device and circuit parameters can be extracted at the same time. This solution technique benefits modern nano- and micro-electronic industries ranging from VLSI products and display plane.

Second year:

I. Novel Miniaturized Filters and Modules

In this year, we continue to develop more miniaturized filters and modules, the concept of serial configuration for single-band bandpass filter is extended for dual-band bandpass filter design, which can also produce a finite transmission zero by series connecting two opposite-phase filters without affecting these two pass-band performance. On the other hand, the module designed in the first year has been fabricated and measured in this year. This dual-band RF front-end module integrate 2 low pass filters, 2 band pass filters, 2 diplexers, a DPDT switch, a LNA and a power detector into a multi-layer LTCC substrate. And in the next year, we will develop a RF module with embedded antenna. Besides, several excellent filters are also proposed, such as modified parallel-coupled filter with two independently controllable upper stopband transmission zeros, a five-pole cascade quadruplet (CQ) microstrip filter having two pairs of transmission zeros, modified insertion loss function synthesis of maximally flat parallel-coupled line bandpass filters, microstrip bandpass filters with a dual-passband response, and microstrip bandpass filters for ultra-wideband (UWB) wireless communications.

II. New Miniaturized Antenna

A dielectric-loaded quadrifilar helix antenna is developed this year. The frequency is 1.575GHz for GPS mobile applications. Its circularly polarized radiation pattern is omni-directional with a cardioid shape. The self-phasing methodology gives the quadrature phase input, thus for differential input LNA or RFIC, the antenna can be connected directly

III. Quantum Mechanical Theory and Perturbation Solution Methodology for Random Dopant-Induced Fluctuation

Numerical solution of the Schrödinger and Poisson equations (SPEs) plays an important role in semiconductor simulation. We present a robust iterative method to compute the self-consistent solution of the SPEs in nanoscale metal-oxide-semiconductor (MOS) structures. Based on the global convergence of the monotone iterative (MI) method in solving the quantum corrected nonlinear Poisson equation (PE), this iterative method is successfully implemented and tested on the single-, double-, and surrounding-gate (SG, DG, and AG) MOS structures. Compared with other approaches, shown in Fig. 4, various numerical simulations are demonstrated to show the accuracy and efficiency of the method. In addition, we explore the structure effect on electrical characteristics of sub-10-nm double-gate metal–oxide–semiconductor field-effect transistors (DG MOSFETs). To quantitatively assess the nanoscale DG MOSFETs' characteristics, the on/off

current ratio, subthreshold swing, threshold voltage (V_ th), and drain-induced barrier-height lowering are numerically calculated for the device with different channel length (L) and the thickness of silicon film (Tsi). Based on our two-dimensional density gradient simulation, shown in Fig. 6, it is found that, to maintain optimal device characteristics and suppress short channel effects (SCEs) for nanoscale DG MOSFETs, Tsi should be simultaneously scaled down with respect to L. From a practical fabrication point-of-view, a DG MOSFET with ultrathin Tsi will suppress the SCE, but suffers the fabrication process and on-state current issues. Simulation results suggest that L/Tsi > 1 may provide a good alternative in eliminating SCEs of double-gate-based nanodevices.

4. A SUMMARY OF THE POST-PROJECT PLAN

I. To develop dielectric waveguide circuits using PCB, LTCC, or high dielectric constant material. Development of the tri-dimensional RF front-end module with integration of active components, passive components, and embedded antenna. And to investigate filters with multi-transmission zeros in the ultra-wide upper stopband and with multi-spurious suppression.
II. To investigate the coupling effects between the circuit components and/or the antenna in a multi-layer three dimensional environment and performance improvement of VIP components and develop microstrip filters using block configuration.
III. To establish the modeling of nano-scale high frequency devices and components. To develop Bulk FinFET for next generation technology era and to establish Surface potential-based device model for sub-45 nm CMOS.
IV. To investigate electrical characteristic fluctuation in ultra small VLSI transistors and magneto-optical properties of semiconductor quantum nanostructures

5. INTERNATIONAL COOPERATION ACTIVITIES

We have collaborated with Semiconductor Research Corporation (SRC) for "Development of Data Bases and Optimization Simulation Packages for RFIC Inductors." The objective is to develop a comprehensive, reliable, and efficient design system for RFIC inductors. The research contents include extraction of material EM parameters in silicon wafer, development of data bases for RFIC inductors, development of EM simulation and optimization softwares for RFIC inductors, and Analysis of coupling effects and shielding designs.

On the other hand, through participation in international conferences, invited talks, and short-term visiting, we have established the network of collaboration in the field of computational electronics including biological transport and its electrical characteristics, and nanodevice modeling and simulation. Universities and industry in the world wide that we have collaboration with are the University of Illinois at Urbana-Champaign in USA, the Tokyo Institute of Technology in Japan, the IBM Microelectronics in USA, the Hiroshima University in Japan, the Vienna University of Technology in Austria, the St. Francis Xavier University in Canada, the Ulyanovsk State Technical University in Russia, and the Chinese Academy of Sciences in China.

III. STATISTICS ON RESEARCH OUTCOMES OF THIS PROJECT (FORM 3)

[1] Indicate the number of items that are significant. The criterion for "significant" is defined by the PIs of the program. For example, it may refer to Top journals (i.e., those with impact factors in the upper 15%) in the area of research, or conferences that are very selective in accepting submitted papers (i.e., at an acceptance rate no greater than 30%). Please specify the criteria in Appendix IV.
[2] Indicate the number of citations. The criterion for "citations" refers to citations by other research teams, i.e., exclude self-citations.
[3] Refers to the workshop and conferences hosted by the program.
[4] Includes Laureate of Nobel Prize, Member of Academia Sinica or equivalent, fellow of major international academic societies, etc.
[5] Refers to industry standards approved by national or international standardization parties that are proposed by PIs of the program.
[6] Refers to research outcomes used to provide technological services, including research and educational programs, to other ministries of the government or professional societies.

LISTING		TOTAL	DOMESTIC/ INTERNATIONAL	SIGNIFICANT[1]	CITATIONS[2]	TECHNOLOGY TRANSFER
PUBLISHED ARTICLES	JOURNALS	0	D: 0	0		
		31	I:21	10		
	CONFERENCES	0	D: 0	3		
		81	I:78			
	TECHNOLOGY REPORTS	0				
PATENTS	PENDING	1	D: 1	-		
		3	I: 3			
	GRANTED	0	D: 0	-		
		4	I: 4			
COPYRIGHTED INVENTIONS	ITEM					
WORKSHOPS/ CONFERENCES[3]	ITEM	0	D: 0			
		6	I: 6			
	PARTICIPANTS	0	D: 0			
		0	I: 0			
TRAINING COURSES (WORKSHOPS/ CONFERENCES)	HOURS					
	PARTICIPANTS					
PERSONAL ACHIEVEMENTS	HONORS/ AWARDS[4]	0	D: 0			
		0	I: 0			
	KEYNOTES GIVEN BY PIS	0	D: 0			
		0	I: 0			
	EDITOR FOR JOURNALS	0	D: 0			
		6	I: 6			
TECHNOLOGY TRANSFERS	ITEM	0				
	LICENSING FEE	0				
	ROYALTY	0				
INDUSTRY STANDARDS[5]	ITEM	0				
TECHNOLOGICAL SERVICES[6]	ITEM	5	3	2	-	
	SERVICE FEE	13,592,000	6,892,000	6,700,000	-	-

IV. List of Works, Expenditures, Manpower, and Matching Supports from the Participating Institutes (Form 4)

Serial No.:NSC93-2752-E-009-002-PAE	Program Title: 前瞻性三維微波被動元件與模組研發(1/4) Advanced Tri-Dimensional Microwave Passives and Modules(1/4)

Projects	Major Tasks and Objectives	Expenditures (in NT$1,000)						Manpower (person-month)			
		Salary	Seminar/ Conference-Related Expenses	Project-Related Expenses	Cost for Hardware & Software	Over-head	Total	Principal Investigators	Research/ Teaching Personnel	Supporting Staff	Total
S3	Microwave passives and modules	4,790	200	2,334	2,071	689	10,084	3	438	14	455
SUM		4,790	200	2,334	2,071	689	10,084	3	438	14	455

Serial No.:NSC94-2752-E-009-003-PAE	Program Title: 前瞻性三維微波被動元件與模組研發(2/4) Advanced Tri-Dimensional Microwave Passives and Modules (2/4)

Projects	Major Tasks and Objectives	Expenditures (in NT$1,000)						Manpower (person-month)			
		Salary	Seminar/ Conference-Related Expenses	Project-Related Expenses	Cost for Hardware & Software	Over-head	Total	Principal Investigators	Research/ Teaching Personnel	Supporting Staff	Total
S3	Microwave passives and modules	5,308	423	1,892	1,750	703	10,076	3	480	22	505
SUM		5,308	423	1,892	1,750	703	10,076	3	480	22	505

V. APPENDIX I

九十四年度「前瞻電信微波科技發展計畫-子計畫三：前瞻性三維微波被動元件與模組研發(3/4)」經費預核清單

執行機關：國立交通大學電信工程研究所

主　持　人：鍾世忠教授
共同主持人：彭松村教授
共同主持人：張志揚教授
共同主持人：郭仁財教授
共同主持人：李義明教授

執行期間：95/04/01 ~ 96/03/31
計畫編號：NSC95-2752-E-009-004-PAE

補助項目	核定金額	補助項目	變更後金額
人事費	4,405,470	業務費	8,464,814
博士後研究	1,846,344		
其他費用	2,879,000		
研究設備費	1,860,000	研究設備費	2,360,000
國外差旅費	350,000	國外差旅費	116,000
出席國際會議	200,000	出席國際會議	600,000
管理費	831,730	管理費	831,730
合計	12,372,544	合計	12,372,544

- 變更用途說明：由於本子計劃發表文章豐富，為鼓勵計畫內老師們踴躍發表文章，並出國報告，特將原「國外差旅費」張志揚教授及郭仁財教授各 100,000 元，共 200,000 元挪至「出席國際會議」。此外，由於李義明教授亦致力於學術研究，發表眾多成就不凡的文章，主持人鍾世忠教授特將「人事費」原擬聘碩士級助理改聘學士級助理多餘差額 10 萬元提供李義明教授繼續發表重大成就。「人事費」專任研究助理碩士級第三年一名之經費，由於目前助理人員從缺，擬將該筆人事費 50 萬元改編至設備費，購買「V 頻段遠場量測系統升級」。另由「其他費用」提撥 10 萬元供另名博士生王侑信出席國際會議。而博士後研究人員部分原擬聘請李介文博士的經費 937,092 元，李博士由於個人生涯規劃不克前來任職，因此擬將該筆費用挪至人事費，聘請另名具有相關學識背景的碩士級以上專任研究助理及相關博碩士研究生參與研究。

VI. APPENDIX II

國際性期刊及會議發表情形					
		Journal		Conference	
		Semiconductor	Passives	Semiconductor	Passives
Published	Significant	0	10	0	3
	International	19	2	49	29
Patents : 8					
Technological Services：5					
Workshop : 6					
Invited : 2					
Personal achievements : 6					

✧ **Journal**

➢ Semiconductor & Integrated-Circuit Tech.

- Significant
- International

1. Yiming Li, "Magnetization and Magnetic Susceptibility in Nanoscale Vertically Coupled Semiconductor Quantum Rings," Journal of Computational Electronics, Vol. 4, No. 1-2, April 2005, pp. 135-138.

2. Yiming Li, Jam-Wem Lee, and Hong-Mu Chou, "Silicon-Germanium Structure in Surrounding-Gate Strained Silicon Nanowire FETs," Journal of Computational Electronics, Vol. 3, No. 3-4, Oct. 2004, pp. 251-255.

3. Yiming Li, and Shao-Ming Yu, "A Novel Approach to Compact Model Parameter Extraction for Excimer Laser Annealed Complementary Thin Film Transistors," Journal of Computational Electronics, Vol. 3, No. 3-4, Oct. 2004, pp. 257-261.

4. Yiming Li, "Vertical Coupling Effects and Transition Energies in Multilayer InAs/GaAs Quantum Dots," Surface Science, Vol. 566-568, Part 2, Sep. 2004, pp. 1057-1066.

5. Yiming Li, "An Iterative Method for Single and Vertically Stacked Semiconductor Quantum Dots Simulation," Mathematical and Computer Modelling, Vol. 42, No. 7-8, 2005, pp. 717-718.

6. Hung-Mu Chou, Shao-Ming Yu, Jam-Wem Lee, and Yiming Li, "A Compact Model for Electrostatic Discharge Protection Nanoelectronics Simulation," International Journal of Nanotechnology, Vol. 2, No. 3, 2005, pp. 226-238.

7. Yiming Li and Cheng-Kai Chen, "Parallelization of Multiple Genome Alignment," Lecture Notes in Computer Science, Vol. LNCS 3726, Sep. 2005, pp. 910-915.

8. Yiming Li, "Application of Parallel Adaptive Computing Technique to Polysilicon Thin-Film Transistor Simulation," Lecture Notes in Computer Science, Vol. LNCS 3726, Sep. 2005, pp. 829-838.

9. Yiming Li and Hung-Mu Chou, "A Comparative Study of Electrical Characteristic on Sub-10 nm Double Gate MOSFETs," IEEE Transactions on Nanotechnology, Vol. 4, No. 5, Sep. 2005, pp. 645-647.

10. Yiming Li, Hung-Mu Chou, and Jam-Wem Lee, "Investigation of Electrical Characteristics on Surrounding-Gate and Omega-Shaped-Gate Nanowire FinFETs," IEEE Transactions on Nanotechnology, Vol. 4, No. 5, Sep. 2005, pp. 510-516.

11. Yiming Li, Hung-Mu Chou, Jam-Wem Lee, and Bo-Shian Lee, "A Three-Dimensional Simulation of Electrostatic Characteristics for Carbon Nanotube Array Field Effect Transistors," Microelectronic Engineering, Vol. 81, No. 2-4, August 2005, pp. 434-440.

12. Yiming Li and Shao-Ming Yu, "A Numerical Iterative Method for Solving Schrödinger and Poisson Equations in Nanoscale Single, Double and Surrounding Gate Metal-Oxide-Semiconductor Structures," Computer Physics Communications. Vol. 169, No. 1-3, July 2005, pp. 309-312.

13. Yiming Li and Pu Chen, "Adaptive Finite Volume Simulation of Electrical Characteristics of Organic Light Emitting Diodes," Lecture Notes in Computer Science, Vol. LNCS 3516, May 2005, pp. 300-308.

14. Yiming Li and Kuen-Yu Huang, "Numerical Simulation of Self-heating InGaP/GaAs Heterojunction Bipolar Transistors," Lecture Notes in Computer Science, Vol. LNCS 3516, May 2005, pp. 292-299.

15. Yiming Li, "Magnetization and Magnetic Susceptibility in Nanoscale Vertically Coupled Semiconductor Quantum Rings," Journal of Computational Electronics. Vol. 4, No. 1-2, April 2005, pp. 135-138.

16. Yiming Li, "Transition Energies in Vertically Coupled Multilayer Nanoscale InAs/GaAs Semiconductor Quantum Dots with Different Structure Shapes," Japanese Journal of Applied Physics, Vol. 44, No. 4B, April 2005, pp. 2642-2646.

17. Yiming Li, Shao-Ming Yu, and Jam-Wem Lee, "Quantum Mechanical Corrected Simulation Program with Integrated Circuit Emphasis Model for Simulation of Ultrathin Oxide Metal-Oxide-Semiconductor Field Effect Transistor Gate Tunneling Current," Japanese Journal of Applied Physics, Vol. 44, No. 4B, April 2005, pp. 2132-2136.

18. Yiming Li and Shao-Ming Yu, "A Parallel Adaptive Finite Volume Method for Nanoscale Double-gate MOSFETs Simulation," Journal of Computational and Applied Mathematics. Vol. 175, No. 1, March 2005, pp. 87-99.

19. Yiming Li, "A Comparison of Quantum Correction Models for Nanoscale MOS Structures Under Inversion Conditions," Materials Science Forum, Vol. 480-481, Feb. 2005, pp. 603-610.

- **Passive Components & Antennas**

  - Significant

20. Kuo-Sheng Chin and Jen-Tsai Kuo, "Insertion loss function synthesis of maximally flat parallel-coupled line bandpass filters," IEEE Trans. Microwave Theory Tech., MTT-53, No. 10, pp. 3161-3168, Oct. 2005. (NSC 93-2213-E-009-095, NSC 93-2752-E-009-002-PAE)

21. Jen-Tsai Kuo, Tsung-Hsun Yeh and Chun-Cheng Yeh, "Design of Microstrip bandpass filters with a dual-passband response," IEEE Trans. Microwave Theory Tech., MTT-53, No. 4, pp. 1331-1337, Apr. 2005. (NSC 93-2213-E-009-095, NSC 93-2752-E-009-002-PAE)

22. Ke-Ying Su and Jen-Tsai Kuo, "Application of Two-dimensional nonuniform fast Fourier transform (2-D NUFFT) technique to analysis of shielded microstrip circuits," IEEE Trans. Microwave Theory Tech., MTT-53, No. 3, pp.993-999, Mar. 2005. (NSC 91-2213-E-009-126, NSC 93-2752-E-009-002-PAE)

23. Jen-Tsai Kuo and Hung-Sen Cheng, "Design of quasi-elliptic function filters with a dual-passband response," IEEE Microwave Wireless Components Letters. vol. 14, No. 10, pp. 472-474, Oct. 2004. (NSC 92-2213-E-009-079, 93-2752-E-009- 002-PAE)

24. Jen-Tsai Kuo and Meshon Jiang, "Enhanced microstrip filter design with a uniform dielectric overlay for suppressing the second harmonic response," IEEE Microwave and Wireless Components Letters, vol. 14, No. 9, pp. 419-421, Sept. 2004. (NSC 92-2213-E-009-079, 93-2752-E-009-002-PAE)

25. Kuo-Sheng Chin, Liu-Yang Lin and Jen-Tsai Kuo, "New formulas for synthesizing microstrip bandpass filters with relative wide bandwidths," IEEE Microwave and Wireless Components Letters, vol. 14, No. 5, pp.231-233, May 2004. (NSC 91-2213-E-009-126, 89 - E - F - A06 - 2- 4)

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  - International

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✧ **Patents**

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✧ **Technological Services**

- Toppoly Optoelectronics Corp.
  Establish LTPS TFT model parameter extraction CAD system at Toppoly Optoelectronics Corp.
  $2,500,000 93.11.01~94.10.31
- Taiwan Semiconductor Manufacturing Company Ltd
  Solve electrical characteristics fluctuation problems for TSMC sub-65 nm CMOS devices
  $1,500,000 94.01.01~94.12.31
- Semiconductor Research Corporation Development of Data Bases and Optimization Simulation Packages for RFIC Induct
  $3,350,000 94.07.01~95.06.30
- Science & Technology Advisors office Ministry of Transportation and Communications Side Warning System Development & Demostration for Trunk Collision Avoidance
  $2,892,000 93.02.01~93.11.30
- Semiconductor Research Corporation Development of Data Bases and Optimization Simulation Packages for RFIC Induct
  $3,350,000 93.07.01~94.06.30

✧ **Workshop**

- Yiming Li, Chair, The 2005 International Symposium of Computational Electronics: Physical Modeling, Mathematical Theory, and Numerical Algorithm, Loutraki, Greece, Oct. 21-26, 2005. (>500 participants)
- Yiming Li, Program Committee, The 5th IASTED International Conference on Modelling, Simulation and Optimization, Aruba, Aug. 29-31, 2005. (>200)
- Yiming Li, Program Committee, The IEEE Workshop on High Performance Computing in Medicine and Biology, July 20 - 22, 2005, Fukuoka Institute of Technology, Japan, July 20-22, 2005. (>500)
- Yiming Li, Vice-Chair, The 2005 International Conference on Computer Design, Las Vegas, USA, June 27-30, 2005. (>300)
- Yiming Li, Program Committee, International Workshop on Computational Nano-Science and Technology, Emory University Atlanta, USA, May 22-25, 2005. (>300)
- Yiming Li, Program Committee, IEEE/ACM The 6th Workshop on Parallel and Distributed Scientific and Engineering Computing, Denver, USA, April 4-8, 2005. (>500)

✧ **Invited**

- (Invited talk)
  Yiming Li, Shao-Ming Yu, and Chuan-Sheng Wang, "Monotone Iterative Method for Numerical Solution of Nonlinear ODEs in MOSFET RF Circuit Simulation," Presented in International Conference of Computational Methods in Sciences and Engineering 2005 (ICCMSE 2005), Loutraki, Korinthos, Greece, 21-26 Oct. 2005.

- (Invited Lecture)
  Yiming Li, "A Hybrid Intelligent Computational Methodology for Semiconductor Device Equivalent Circuit Model Parameter Extraction," Presented in Summer School of Scientific Computing in Electrical Engineering '05 -- Computational Methods for Microelectronics, Capo D'Orlando, Italy, 5-17 September 2005.

✧ **Personal achievements**

- Yiming Li, Guest Associated Editor: Microelectronic Engineering in 2005
- Yiming Li, Guest Associated Editor: Integration, the VLSI Journal in 2005
- Yiming Li, Guest Editor in Chief: International Journal of Computational Science and Engineering in 2005
- Yiming Li, Associated Editor: Engineering Letters (2005~)
- Yiming Li, Editor in Chief: WSEAS Transactions on Electronics (2003~)
- Yiming Li, Associated Editor: WSEAS Transactions on Circuits and Systems (2004~)

VII. APPENDIX III

LIST OF PUBLICATIONS IN "TOP" JOURNALS AND CONFERENCES (LIMIT TO 3-5)

[1] Kuo-Sheng Chin, Jen-Tsai Kuo, "Insertion loss function synthesis of maximally flat parallel-coupled line bandpass filters," IEEE Trans. Microwave Theory Tech., MTT-53, No. 10, pp. 3161-3168, Oct. 2005.

[2] Jen-Tsai Kuo, Tsung-Hsun Yeh and Chun-Cheng Yeh, "Design of Microstrip bandpass filters with a dual-passband response," IEEE Trans. Microwave Theory Tech., MTT-53, No. 4, pp. 1331-1337, Apr. 2005.

[3] C. K. Liao, and C. Y. Chang, "Design of microstrip quadruplet filter with source-load coupling," IEEE Trans. on Microwave Theory and Tech. Vol. 53, No. 7, pp2302-2308, July 2005.

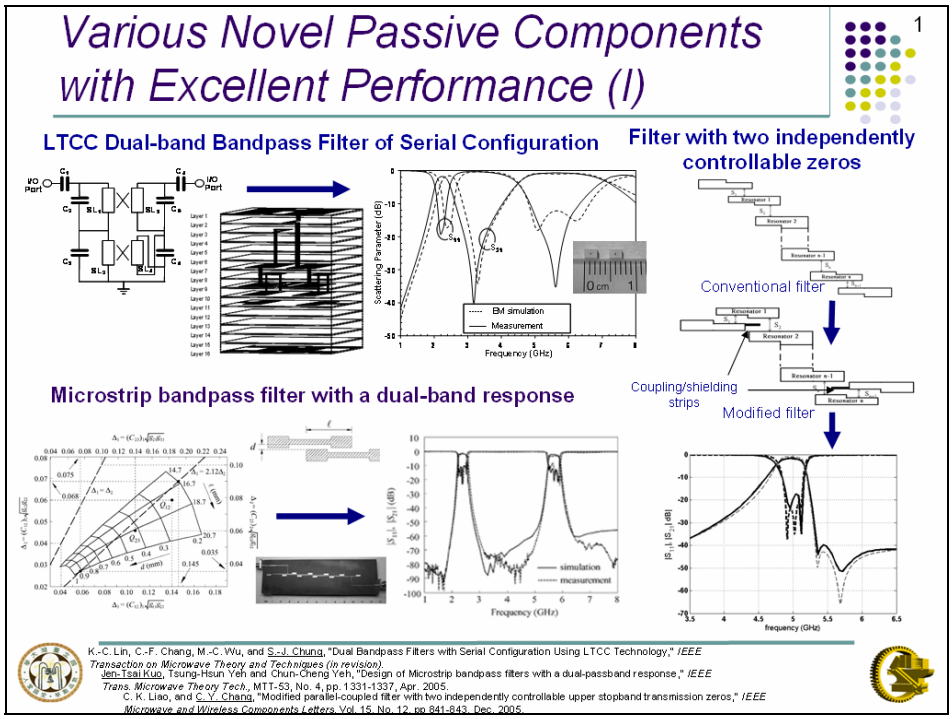
[4] C. K. Liao, and C. Y. Chang, "Modified parallel-coupled filter with two independently controllable upper stopband transmission zeros," IEEE Microwave and Wireless Components Letters, Vol. 15, No. 12, pp 841-843, Dec. 2005

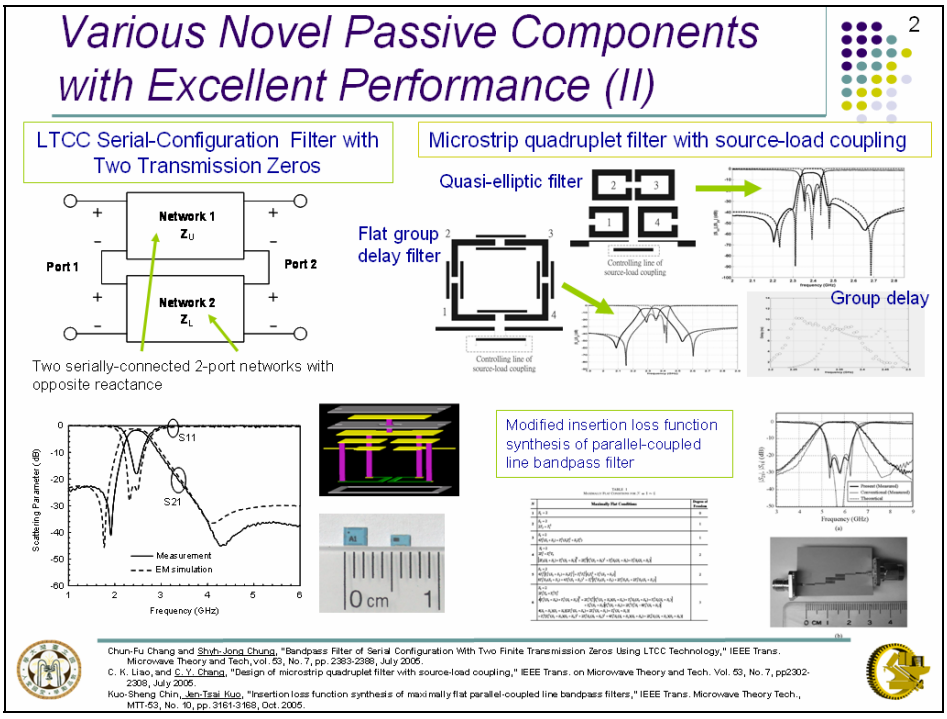
[5] Chun-Fu Chang and Shyh-Jong Chung, "Bandpass Filter of Serial Configuration With Two Finite Transmission Zeros Using LTCC Technology," IEEE Trans. Microwave Theory and Tech, vol. 53, No. 7, pp. 2383-2388, July 2005.

VIII. APPENDIX IV

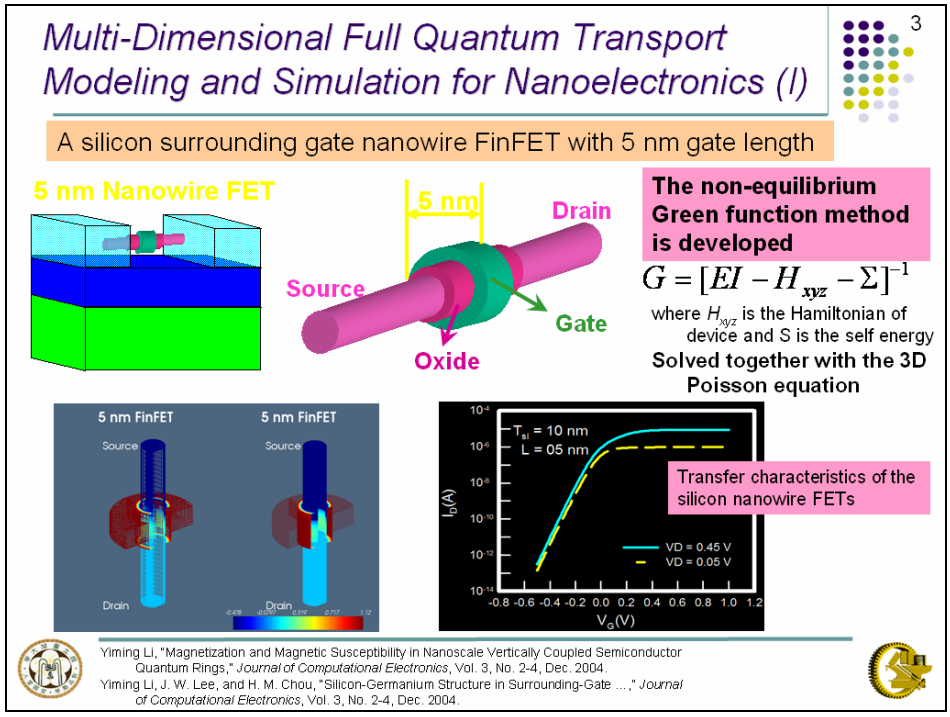
SLIDES ON SCIENCE AND TECHNOLOGY BREAKTHROUGHS

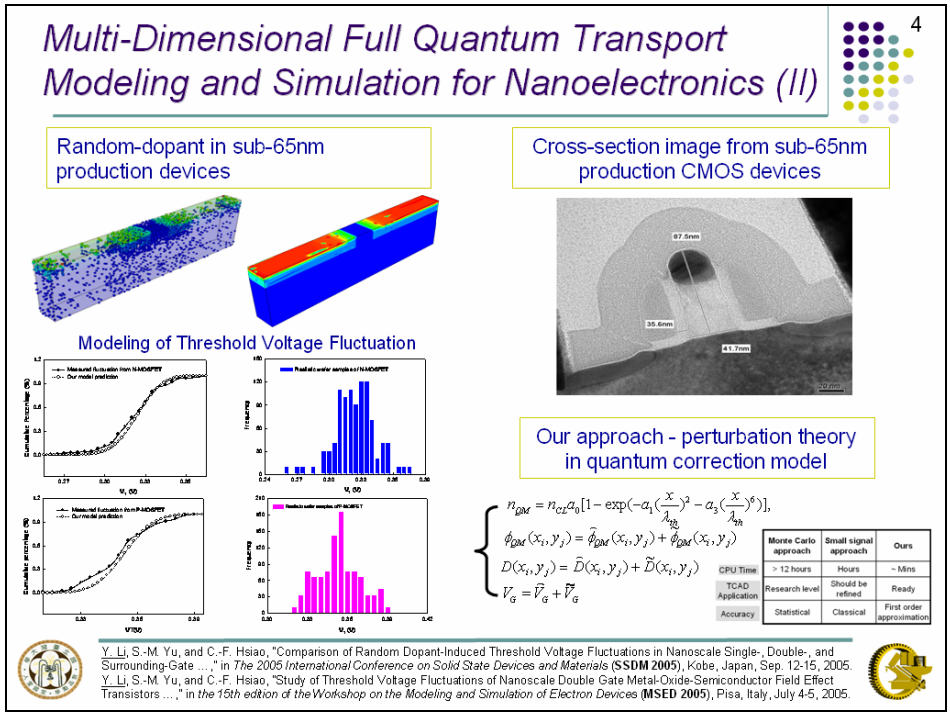
1. Various novel miniaturized filter configurations usng three-dimensional structures have been proposed and demonstrated, including dual-passband quasi-elliptic filters, single- and dual-bandpass filters of serial-configuration filters, vertically installed planar (VIP) filters, and modified parallel coupled-line filters.





2. Multi-dimensional full quantum transport modeling and simulation for nanoelectronics has successfully been developed. We have applied the developed CAD platform to perform the world-wide smallest transistor's simulation. It is a silicon nanowire FinFET with 5 nm gate length. A set of optimized device and circuit parameters can be extracted, which benefits modern nano- and micro-electronic industries ranging from VLSI products and display plane.





IX. Appendix V: Self-Assessment

Program Title:

Sub-project 3: Advanced Tri-Dimensional Microwave Passives and Modules

[REVIEWER #1]

	ASSESSMENT SUBJECT	SCORES (1~5, LOW TO HIGH)
PROGRAM'S CONTENTS & PERFORMANCE	Importance & Innovation of the Program Major Task	4
	Program Report Redaction	4
	Viability of the Program Approaches & Methodologies	5
	Principal Investigator's Competence for Leading the Program	5
	Interface & Integration between Overall & Sub-Project(s)	4
	Interface & Integration among All Sub-Projects	4
	Manpower & Expenditures	4
PROGRAM'S RESULTS	Contribution in Enhancing the International Academic Standing	5
	Impact on Advancing Teaching or on Technology Development	5
	OVERALL	40

[REVIEWER #1]

REVIEWER'S COMMENTARY & SUGGESTION:

本計畫在小型化天線之研究已經有良好成果，建議與廠商合作加速商品化時程

Program Title:

Sub-project 3: Advanced Tri-Dimensional Microwave Passives and Modules

[REVIEWER #2]

	ASSESSMENT SUBJECT	SCORES (1~5, LOW TO HIGH)
PROGRAM'S CONTENTS & PERFORMANCE	Importance & Innovation of the Program Major Task	
	Program Report Redaction	
	Viability of the Program Approaches & Methodologies	
	Principal Investigator's Competence for Leading the Program	
	Interface & Integration between Overall & Sub-Project(s)	
	Interface & Integration among All Sub-Projects	
	Manpower & Expenditures	
PROGRAM'S RESULTS	Contribution in Enhancing the International Academic Standing	
	Impact on Advancing Teaching or on Technology Development	
	OVERALL	40

[REVIEWER #2]

REVIEWER'S COMMENTARY & SUGGESTION:

1. **This is an interesting sub-project to design and build advanced passive components and modules. I particularly like the combination of experimental and theoretical effects, a successful model for university research.**

2. **How are the projects related to other programs such as National Telecommunication program and SOC program?**

Program Title:

Sub-project 3: Advanced Tri-Dimensional Microwave Passives and Modules

[REVIEWER #3]

	ASSESSMENT SUBJECT	SCORES (1~5, LOW TO HIGH)
PROGRAM'S CONTENTS & PERFORMANCE	Importance & Innovation of the Program Major Task	
	Program Report Redaction	
	Viability of the Program Approaches & Methodologies	
	Principal Investigator's Competence for Leading the Program	
	Interface & Integration between Overall & Sub-Project(s)	
	Interface & Integration among All Sub-Projects	
	Manpower & Expenditures	
PROGRAM'S RESULTS	Contribution in Enhancing the International Academic Standing	
	Impact on Advancing Teaching or on Technology Development	
	OVERALL	95

[REVIEWER #3]

REVIEWER'S COMMENTARY & SUGGESTION:

1. 3D被動元件與模組研發，獲得多樣新穎成就，如圓柱螺旋天線、3D/LTCC濾波器、耦合器等被動元件模組。

2. 奈米級元件設計。

3. 3D/LTCC方面之技術研究，建議邀請製程/材料專長之教授或研究單位合作，共同開發頂尖技術。

Program Title:

Sub-project 3: Advanced Tri-Dimensional Microwave Passives and Modules

[REVIEWER #4]

	ASSESSMENT SUBJECT	SCORES (1~5, LOW TO HIGH)
PROGRAM'S CONTENTS & PERFORMANCE	Importance & Innovation of the Program Major Task	4
	Program Report Redaction	4.5
	Viability of the Program Approaches & Methodologies	4.5
	Principal Investigator's Competence for Leading the Program	4.5
	Interface & Integration between Overall & Sub-Project(s)	4.5
	Interface & Integration among All Sub-Projects	4.5
	Manpower & Expenditures	4.5
PROGRAM'S RESULTS	Contribution in Enhancing the International Academic Standing	5
	Impact on Advancing Teaching or on Technology Development	5
	OVERALL	42

[REVIEWER #4]

REVIEWER'S COMMENTARY & SUGGESTION:

1. 由五位教授共同執行，發展以被動元件為主。

2. 未來宜考量如何整合，俾使與子計劃一搭配。

Program Title:

Sub-project 3: Advanced Tri-Dimensional Microwave Passives and Modules

[REVIEWER #5]

	ASSESSMENT SUBJECT	SCORES (1~5, LOW TO HIGH)
PROGRAM'S CONTENTS & PERFORMANCE	Importance & Innovation of the Program Major Task	5
	Program Report Redaction	5
	Viability of the Program Approaches & Methodologies	5
	Principal Investigator's Competence for Leading the Program	5
	Interface & Integration between Overall & Sub-Project(s)	4
	Interface & Integration among All Sub-Projects	4
	Manpower & Expenditures	4
PROGRAM'S RESULTS	Contribution in Enhancing the International Academic Standing	5
	Impact on Advancing Teaching or on Technology Development	4
	OVERALL	46

REVIEWER'S COMMENTARY & SUGGESTION:

(1) 第三子計畫以研發三維微波被動元件與模組為主，共有五個分項計畫，計畫進行順利，照預期目標進行，已有較具體的成果包括完成前瞻性三維微波元組件、新穎技術減少天線所佔面積，非均勻快速 Fourier 轉換（NUFET）之 Algorithm 以及小於 65nm,25nm CMOS 元件之模擬及模型化。

(2) 目前與美國、加拿大、澳洲、中國及俄羅斯進行國際合作計畫，並與工研院有合作研究計畫，期刊論文 22 篇，國際會議論文 33 篇，4 項專利，其中 Significant 期刊論文及會議論文各有 7 篇及 3 篇。

(3) 與其它五個子計畫之整合及互動尚有待加強,如何利用此被動微波元件與子計畫一及二之 RF IC 組成一模組或次系統應可再努力。

(4) 所研發的技術成果應與國際上最先進的研發團隊作一比較。

(5) 有關 Sub-65nm CMOS Devices 及 Sub-25nm Bulk Fin FET 元件之理論模擬分析已有很好成果，應設法與 TSMC 或 UMC 公司合作實際完成元件製程，以證明模擬的真實性。

[REVIEWER # 5]

PRINCIPAL INVESTIGATOR'S FEEDBACK: (AVAILABLE)

REPLY TO REVIEWERS:

非常感謝各位評審委員的指教與批評，子計畫三會參考各位評審委員的建議，在小型化被動元件、小型化天線以及小型化模組這幾方面的開發與整合，將做更進一步的加強與改善，並與其他子計畫合作，將其他子計畫設計好的主動元件(例如 LNA、Switch、PA)，與本計劃設計的被動元件(例如 BPF、LPF、Diplexer、Balun、Hybrid)以及小型化天線整合起來，共同開發出一具有優異特性的前瞻三維微波構裝模組。此外，子計劃三也將加速與 TSMC 公司共同合作，希望能藉由子計畫三開發的奈米級元件模擬的平台，協助 TSMC 解決量產上與製程上的問題，使得 CMOS 製程相容的 IC 量產製造技術可以推進到 25nm 以下。

Program Reviewer's Signature:_____

Notes: The (7~9) program reviewers are invited by National Science Council.

X. APPENDIX VI – RESEARCH OUTCOME OF THE FIRST YEAR

1. Novel Tri-dimensional Microwave Components

1-1 Microwave Passive Components Using LTCC Technology

In this year, we have proposed a second-order band-pass filter of serial-configuration (Fig. 1-1.1). In this serial-configuration concept, the method of producing transmission zeros is to serially connect two two-port networks, sum the impedance matrices ($Z_U(\omega)$ and $Z_L(\omega)$) and make the sum equal to zero ($Z_U(\omega)+Z_L(\omega)=0$). Thus, the transmission zeros occur at some frequencies. The serial-configuration design concept described in this paper is clearly extendable to two networks with positive and negative reactance to generate finite transmission zeros (Fig. 1-1.2). Two band-pass filters, with center frequencies of 2.44 GHz and 4.8 GHz, have been designed and implemented with LTCC process (Fig. 1-1.4). The measured results (Fig. 1-1.3) are found to agree well with the simulation results. Both the fabricated band-pass filters are found to be compact with low insertion loss in the pass-band and high suppression in the rejection area including image frequencies and harmonics of operating frequencies.

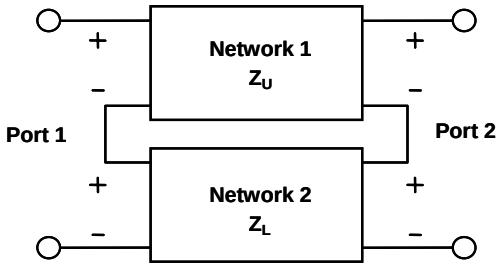


Fig. 1-1.1

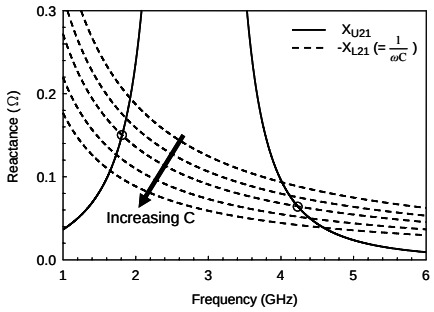


Fig. 1-1.2

Fig. 1-1.1 A representation of the proposed filter with two serially-connected two-port networks.

Fig. 1-1.2 Mutual reactance function X_{U21} of Network 1 and the negative of the mutual reactance, $-X_{L21}$ (= $1/\omega C$), of Network 2. The dashed lines denote various grounding capacitances. The finite transmission zeros are located where the solid line intersects with the dashed lines.

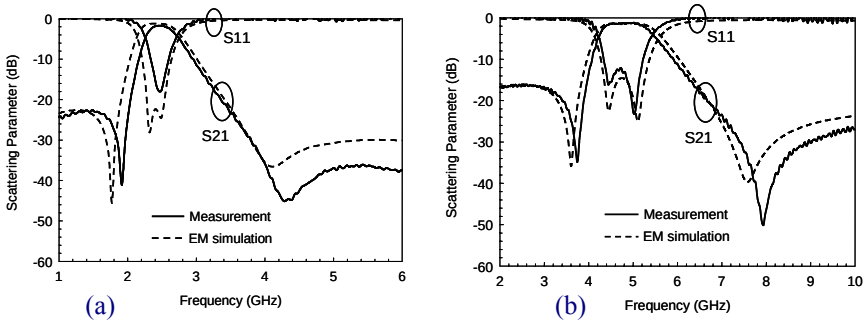


Fig. 1-1.3 Comparison of the measured (solid lines) and EM simulated (dashed lines) scattering parameters of (a) the 2.4-GHz band-pass filter, and (b) the 4.8-GHz band-pass filter.

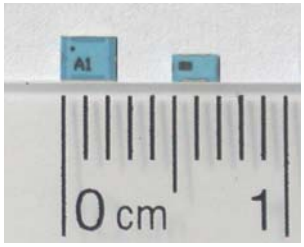


Fig. 1-1.4 Photograph of the two fabricated LTCC filters.

In addition, a RF front end module (FEM) with passive components including two low-pass filters, two band-pass filters and two diplexers, and active components including one low noise amplifier (LNA), one T/R switch and one power detector, has been designed and fabricated with LTCC process. The passive components are realized within the multi-layer substrate, and the active components are mounted on the top surface of the LTCC substrate (Fig. 1-1.5). The LTCC

FEM has been designed with 14 layers of CT2000 process (dielectric constant is 9.1 and loss tangent is 0.002). The size exculding the surface mounted devices is 5.4 x 4.0 x 0.9 mm^3.

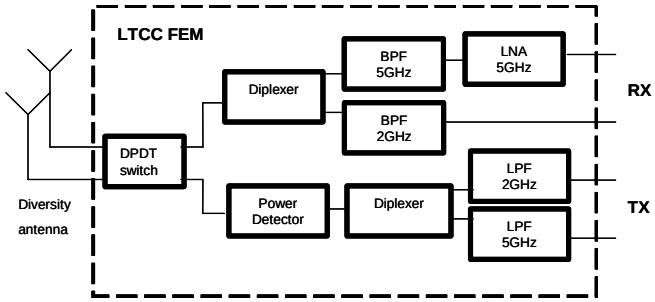


Fig. 1-1.5 The schematic diagram of the LTCC front end module.

This module which has integrated passive and active components into a package possesses good performance of dual-band characteristics. In Fig 1-1.6, the simulated result of 5-GHz Tx path has 0.8dB insertion loss at 4.9GHz ~ 5.9GHz, 24dB and 35 dB rejection at 2.4GHz ~ 2.5GHz and at 9.8GHz ~ 11.8GHz; the 2-GHz Tx path has 0.7dB insertion loss at 2.4GHz ~ 2.5GHz and 40 dB rejection at 2nd and 3rd harmonics. In Fig. 1-1.7, the simulated result of 5-GHz Rx path has 1.4 dB insertion loss at 4.9GHz ~ 5.9GHz, 35dB and 40 dB rejection at 2.4GHz ~ 2.5GHz and at 0.1GHz ~ 1.9GHz; the 2-GHz Rx path has 1.7 dB insertion loss at 2.4GHz ~ 2.5GHz and 30dB rejection at 0.1GHz ~ 1.9GHz.

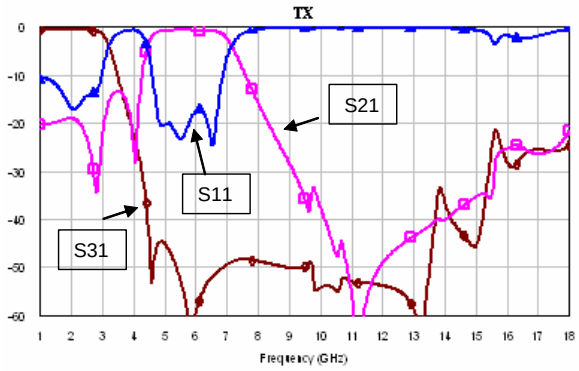


Fig. 1-1.6 A dual band LTCC FEM simulated result of Tx path.

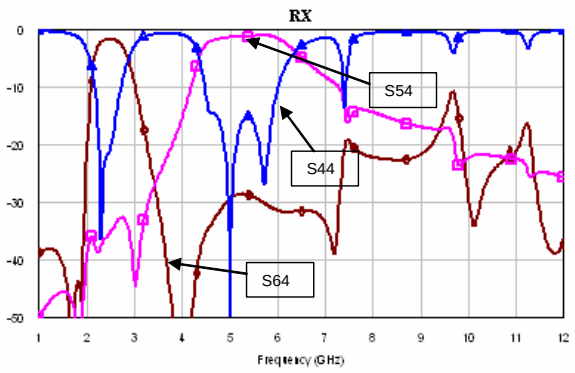


Fig. 1-1.7 A dual band LTCC FEM simulated result of Rx path.

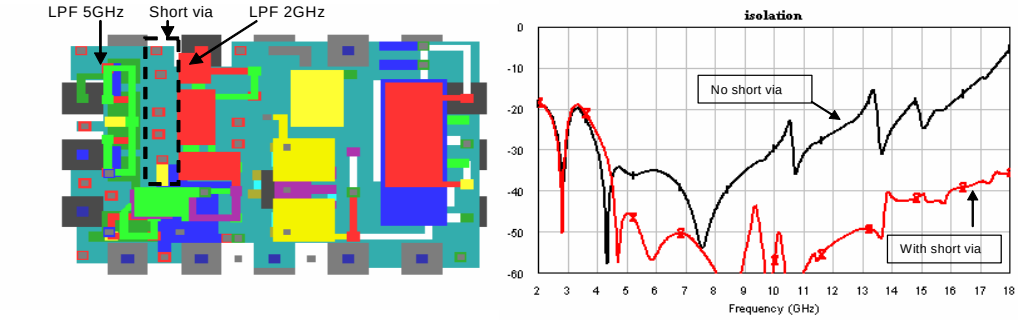


Fig. 1-1.8 Improvement of the coupling effect between two LPFs using a short-ground via.

In this design, we have invested a lot of time in investigating the coupling parasitic effects between the circuit components in a tri-dimensional multi-layer substrate (Fig. 1-1.8). Furthermore, we have met many cavity resonant problems in 3-D layouts, thus we have lots of experience of solving these problems. The development of novel three-dimensional microwave modules and components in LTCC has a considerable advancement of microwave circuit design, simulation

simplification, modeling establishment and 3-D layout design ability, hence does achieve goals in circuit miniaturization, performance enhancement, and system integration.

1-2 Active Monolithic-Microwave Integrated-Circuit (MMIC) Components

A novel broadband switch has been designed recently. Most millimeter-wave switches reported to date were parallel and series resonant-type FET switches. Their separation between FETs utilizes quarter-wavelength transformers, which would thus confine the switch bandwidth. In our design, a maximally flat filter response was designed for the through path of the switch so as to obtain a broadband characteristic. The topology of the broadband single-pole-single-throw switch is as shown in Fig. 1-2.1. Ideally, when the FETs are biased at the "low-impedance state", the drains of the FETs are short-circuited and an input signal will be reflected back, thus the switch is set at the "off-state".

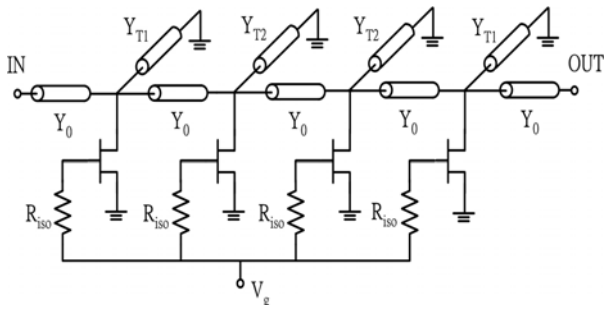


Fig. 1-2.1 The topology of the proposed SPST switch.

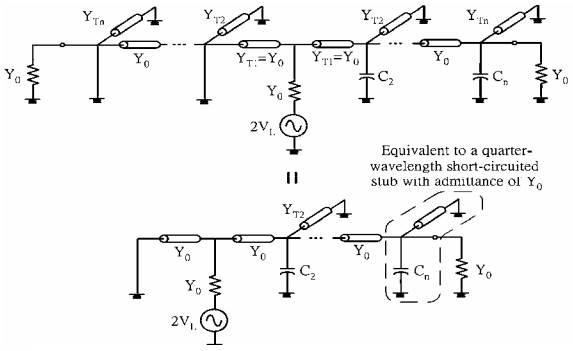
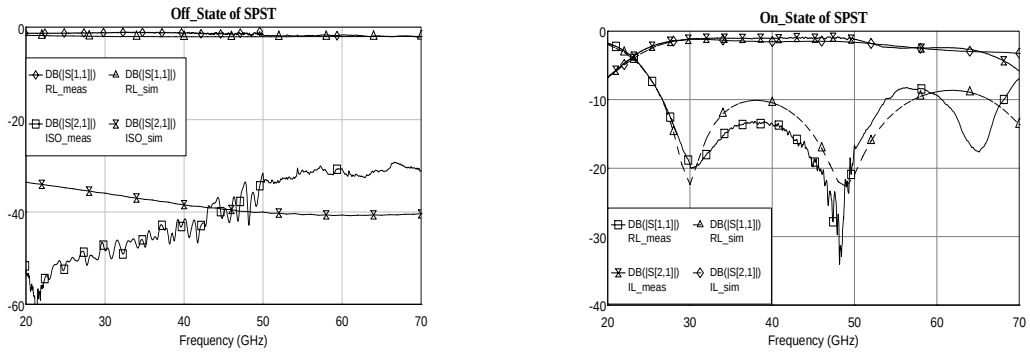


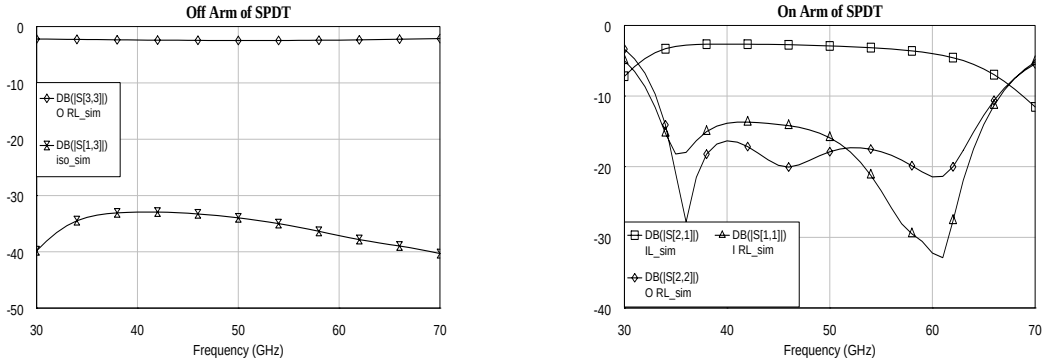
Fig. 1-2.2 Equivalent broadband filter circuit for the transmission state of the SPDT switch.

On the other hand, when the FETs are biased at the "high-impedance state", the FETs are nearly open-circuited, and thus an input signal will pass through the switch. Under this condition, the switch is set at the "on-state". Due to the parasitic effects of the FETs, the switch would not operate as the ideal case. To get a broadband response, these parasitic capacitances should be considered in the design of the switch. This design is distinct from the conventional ones, in which the bandwidth must be restricted because of the quarter-wavelength transmission line which is required between the transmission line junction and the locations of the two switching devices. The extra quarter-wavelength transmission line can be incorporated into the through path for the on-arm as indicated in Fig. 1-2.2. Therefore, this stub must have the totally equivalent characteristic admittance, Y_0, of the through line since it represents a through path when it becomes an on-arm. The simulated data and measured results of SPST and SPDT were found as Fig. 1-2.3 and Fig. 1-2.4.



(a) (b)

Fig. 1-2.3 Measured and simulated results of: (a) insertion loss and return loss of the on-state, and (b) isolation and return loss of the off-state from 20 to 70 GHz for the SPST switch.



(a) (b)

Fig. 1-2.4 Simulated results of (a) insertion loss and output return loss of the on-arm, and (b) isolation and output return loss of the off-arm from 30 to 70 GHz for the 30.5-to-64.5 GHz SPDT switch.

1-3 Miniaturized parallel-coupled filter

Miniaturized harmonic pass-band suppression filter using meandered coupled lines. Parallel-coupled filter is one of the most popular filters used in microwave RF front-end application. However, it usually suffers from too long in the layout and its harmonic pass-bands. The nearest harmonic pass-band where located approximately at twice of the main pass-band frequency can greatly degrade the upper stop-band performance especially when the bandwidth is wide. The proposed filter solves all of the above problems. Fig. 1-3.1 Shows the proposed filter and a conventional parallel coupled filter. Fig. 1-3.2 depicts their measured performance where the upper stop-band rejection is drastically improved in the proposed filter.

Fig. 1-3.1

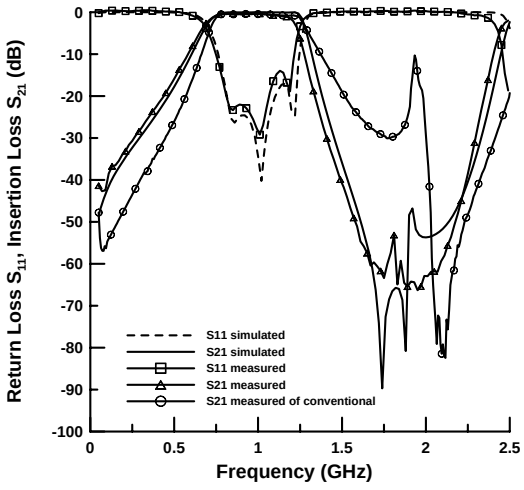


Fig. 1-3.2

1-4 Quadruplet filter with source-load coupling

Design of a quadruplet filter with source-load coupling is proposed. The source-load cross coupling can provide an extra pair of transmission zeros. The proposed method also includes to judge and to improve the unwanted diagonal cross coupling. The diagonal cross coupling shifts the symmetric transmission zeros to be asymmetric of a quasi-elliptic filter, and more over, it destroys the performance of a flat group delay filter.

Fig. 1-4.2 depicts the simulated and measured performance of the proposed filters. This is the first time discussing of the microstrip quadruplet filter with source-load coupling and it is also the first time to develop a microstrip flat group delay filter with negligible unwanted diagonal cross coupling.

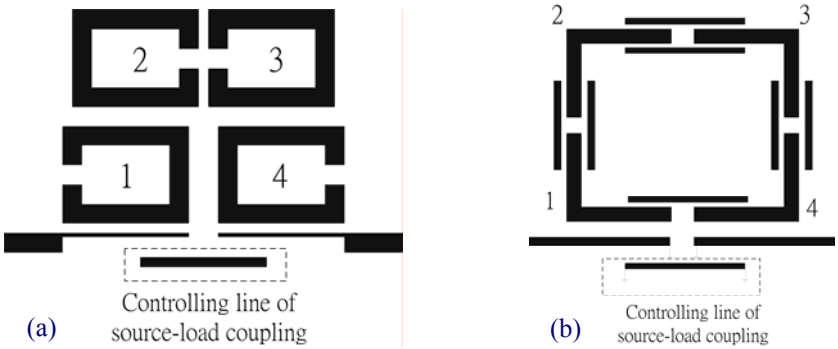


Fig. 1-4.1 shows the layout of the proposed filters with two types of response. (a) Quasi-elliptic response, (b) flat group delay response.

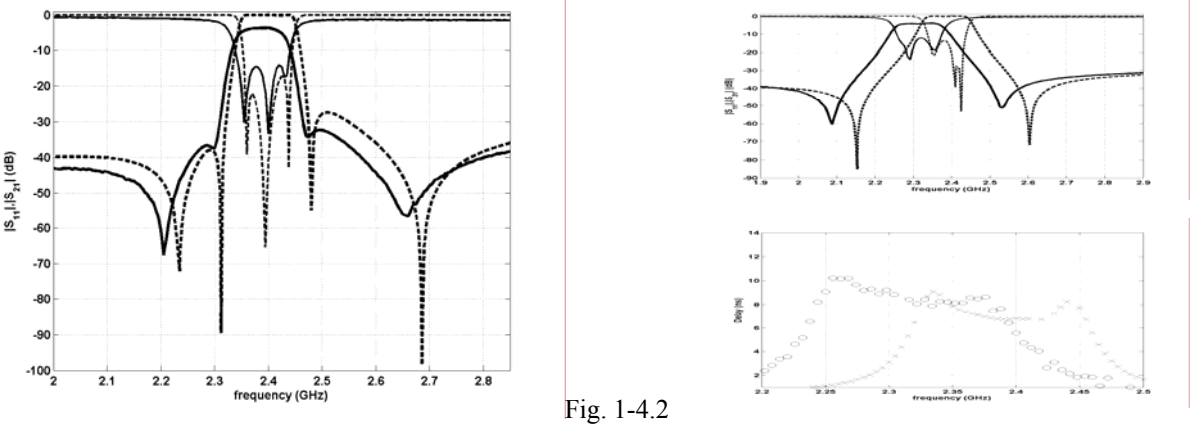


Fig. 1-4.2

(a) quasi-elliptic response (b) flat group delay response

1-5 VIP coupler

We apply the vertically installed planar (VIP) structure to implement microwave rat-race ring coupler. Prof. Awai first proposes this 3-D VIP structure, and we found that it is very useful in many practical microwave circuits application. Here, the broadband rat-race 180^{o} magic-T coupler is proposed. We use a tight-coupled short-end coupled line to replace the 3/4 λ line section in the conventional rat-race ring coupler as shown in Fig. 1-5.1.

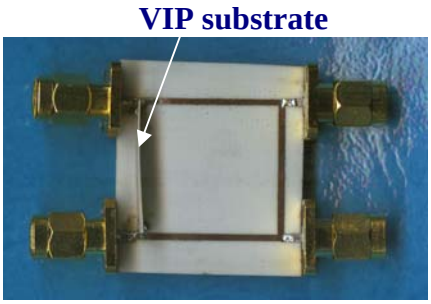


Fig. 1-5.1

In Fig. 1-5.1, the VIP substrate provides phase inversion and it is soldered on the main substrate at its two ends. The main substrate is one-sided microstrip circuit where the most published broadband rat-race ring couplers use double side circuit. Fig. 1-5.2 shows the measured performance of the coupler.

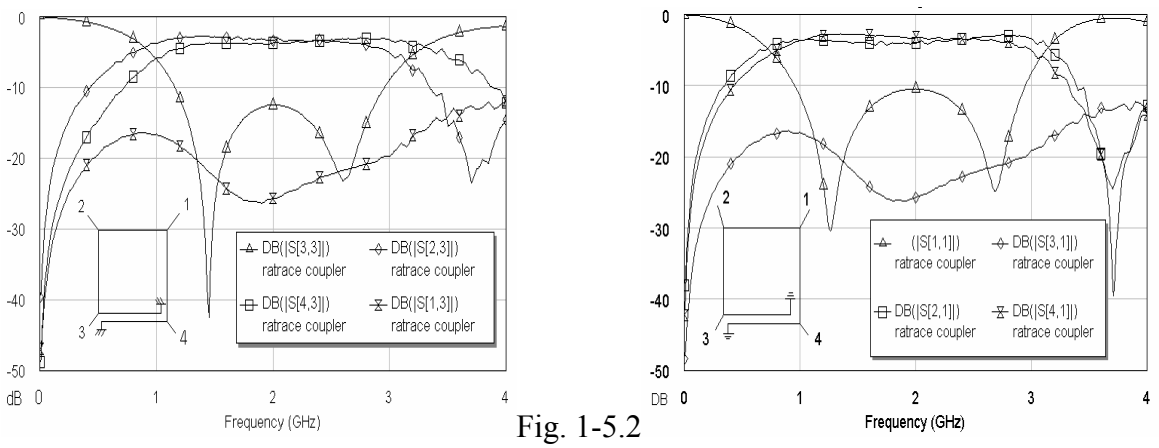


Fig. 1-5.2

(a) The performances when excited at Σ-port (port1) (b)The performances when excited at Δ-port (port3)

The measured bandwidth is about 75% fractional bandwidth with phase error less than 10^{o} and amplitude error less than 1dB. The substrate is popular RO4003 substrate for both main and VIP substrates. Further studies on this type of coupler are still undergoing now. One of them is using more balanced structure to improve phase and amplitude balance.

1-6 VIP broadband filter

The broadband filter using VIP structure is another application of the VIP structure. Conventional parallel-coupled filter structure is difficult to implement a filter with more than an octave bandwidth due to extremely tight coupling is needed. Another problem of a conventional broadband parallel-coupled filter is that the harmonic pass-band, usually located near twice of the main pass-band, may destroy the upper stop-band performance. VIP structure can provide very tight coupling and very high thin line impedance. Therefore, a broadband SIR filter can be realized with nearest spurious pass-band close to four times of the main pass-band. The upper stop-band performance improves drastically.

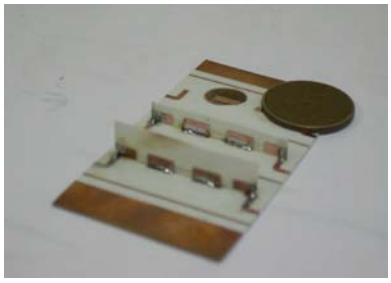


Fig. 1-6.1

Fig. 1-6.1 shows two octave bandwidth 3-resonator SIR filters with VIP structure. The measured response is depicted in Fig. 1-6.2.

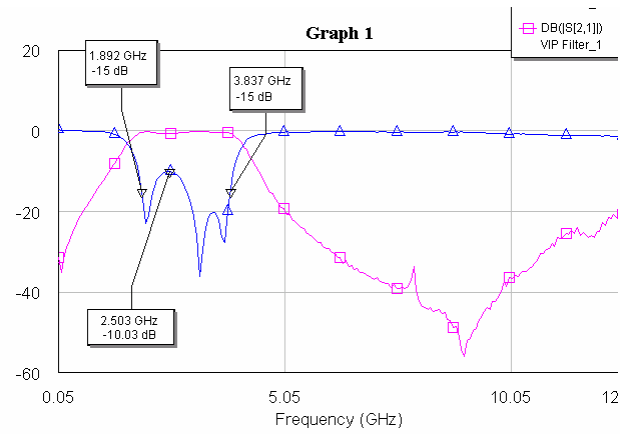


Fig. 1-6.2

In Fig. 1-6.2, the pass-band bandwidth is from 1.89 to 3.84GHz and the nearest spurious pass-band is located higher than 12GHz. The upper stop-band is suppressed to higher than 40dB. Again the substrate used here is most popular RO4003 substrate for both main board and VIP board. The proposed method for the first time solves most difficult part of an octave bandwidth planar filter.

1-7 Microstrip coupler

The microstrip coupler using grounded strip and interdigital capacitor is proposed to provide high directivity loose coupling. Conventional microstrip coupler shows very poor directivity especially when the coupling is loose. Sometimes the directivity becomes negative for very loosely coupled-lines. The proposed example coupler is shown in Fig. 1-7.1 where the coupling is –40dB.

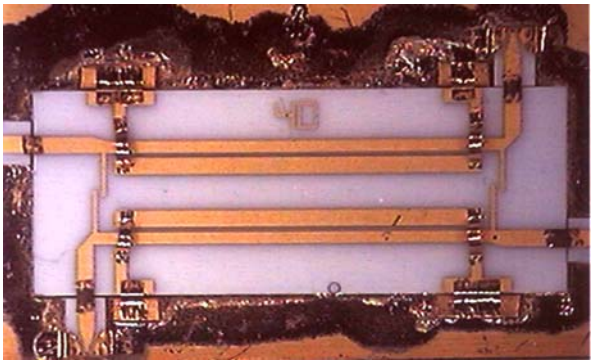


Fig. 1-7.1

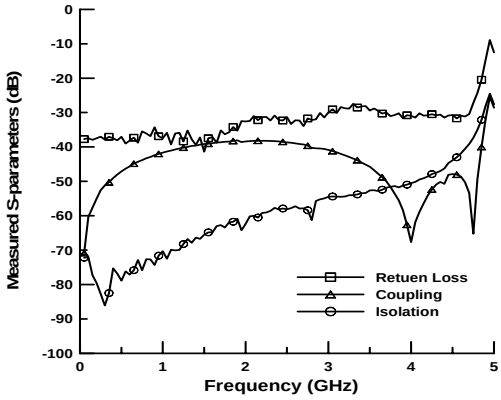


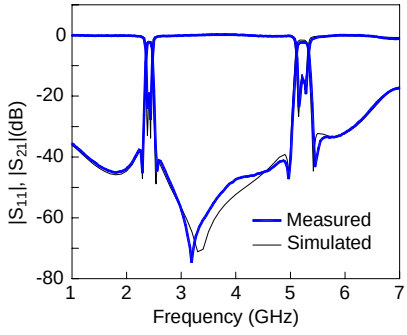
Fig. 1-7.2

In Fig. 1-7.1, two grounded strips are located between two microstrip coupled-lines. Due to the Al_2O_3 ceramic substrate is used, the grounding of the grounded strips is implemented by wrap around. The interdigital capacitors are at the left and right side of the coupler. The measured performance is shown in Fig. 1-7.2. In Fig. 1-7.2, the directivity of the 40dB coupler is better than 20dB near the center frequency. It is useful for power monitoring of an RF system.

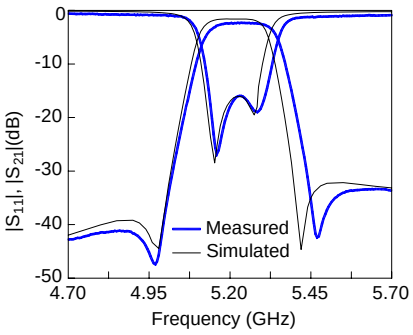
1-8 Quasi-elliptic function filter with cross coupling

In this year, we have presented a design method for parallel-coupled line filter on a suspended structure with suppression of the second harmonic. A filter design method for coupled stages with arbitrary image impedances is also developed.

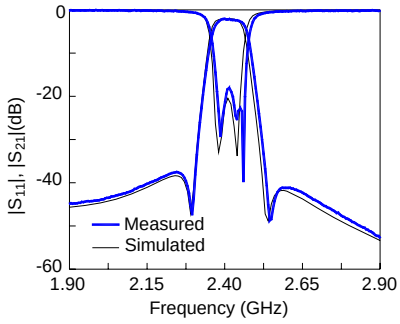
Moreover, we have designed a quasi-elliptic function filter (with cross coupling) with a dual-passband response. Results are in Fig. 1-8.1. The circuit is designed for use in the *IEEE* 820.11a+b combo WLAN applications. The main point of the design is only one single circuit with two simultaneously synthesized pass-bands. The design concept was also applied to parallel-coupled line filters. The success makes another paper be accepted for publication on the *IEEE MTT* in August 2004.

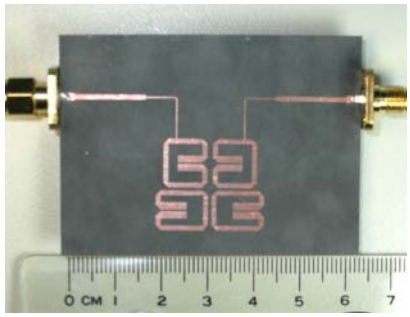


(a)



(c)





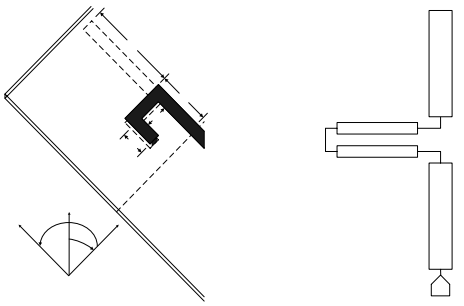
(b) (d)

Fig. 1-8.1 Simulated and measured responses of a dual-passband filter. The design frequencies are 2.4 and 5.2 GHz. (a) Responses in a broad band. (b) Responses around the first pass-band. (c) Responses around the second pass-band. (d) Photograph of the circuit. Substrate: $\varepsilon_r = 2.2$, thickness = 0.508 mm.

2. New Tri-dimensional Antennas

2-1 Miniaturized multi-band antenna on small ground plane

This antenna has an easy structure to manufacture and has enough bandwidth to support the application of *IEEE* 802.11 a/b/g. Also due to its easy structure, the antenna has almost omni-directional radiation patterns in both two bands. Besides, the easy structure makes the antenna have more flexibility to modify or miniature antenna size without influencing its radiation performance. The structure of the antenna has three separate parts: a monopole antenna, a quarter-wave transformer and a tuning end. The size of the small ground plane is 46.7 mm × 88.8 mm. Fig. 2-1.1 shows the structure of the dual-band antenna accomplished on a FR4 substrate. Fig. 2-1.2 shows the simulated and measured return loss of the antenna. Fig. 2-1.3 shows the measured radiation patterns of the general printed monopole antenna at 2.44 GHz.



(a) (b)

Fig. 2-1.1 (a) Geometry of the dual-band antenna (unit：mm), (b) Schematic diagram of the dual-band antenna.

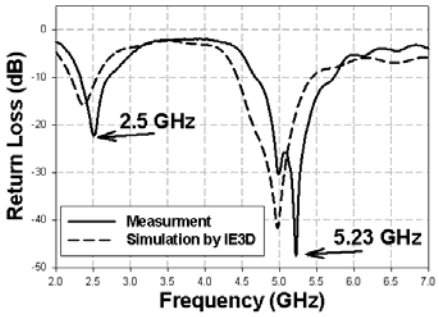


Fig. 2-1.2 Simulated and measured results of return loss.

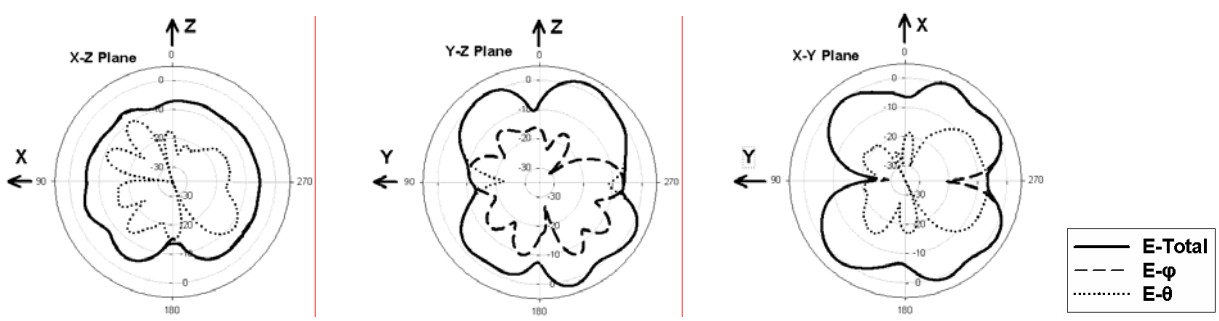
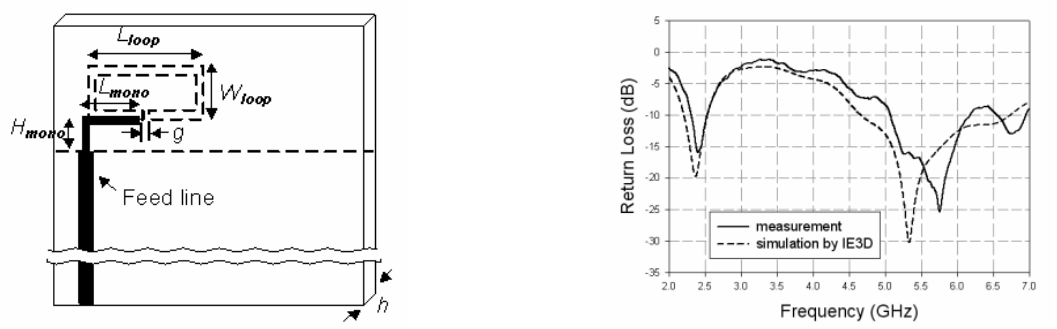


Fig. 2-1.3 Measured radiation patterns for general printed monopole antenna at 2.44GHz.

2-2 Miniaturized dual-band antenna with coupled open-loop resonator

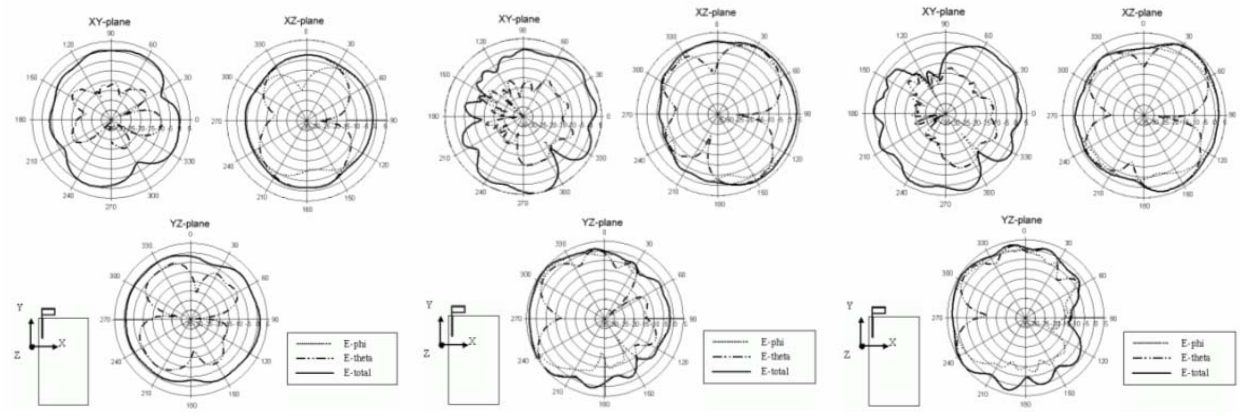
A novel dual-band antenna with broadside coupling has been designed and demonstrated (Fig. 2-2.1). The antenna is composed of two different resonators, that is, an inverted-L monopole and a coupled half-wavelength open-loop resonator, which correspond to the main radiators at, respectively, the higher and lower frequency bands. The inverted-L monopole also serves as the feed structure for the open-loop resonator at the lower band. The occupied area of the antenna is 13×10.2 mm^2. The first radiating element is an inverted-L monopole antenna with total electric length of about a quarter-wavelength at 5GHz. The second radiating element is an open-loop resonator with total electric length of about half-wavelength at 2.4GHz. The electric field energy may couple from the monopole to the open-loop resonator when a lower frequency (2.4 GHz) signal is fed to the monopole. For the higher frequency band, most of the current distributes on the monopole with only a little coupled to the resonator, so the main radiating element is the monopole. The fabricated antenna with broadside coupling possesses 10-dB return-loss bandwidths of 220 MHz at 2.4 GHz band and of 1.07 GHz at 5 GHz band.



(a) (b)

Fig. 2-2.1. (a) Geometry of the proposed dual-band antenna with broadside coupling. (b) Measured and simulated responses of the proposed dual-band antenna.

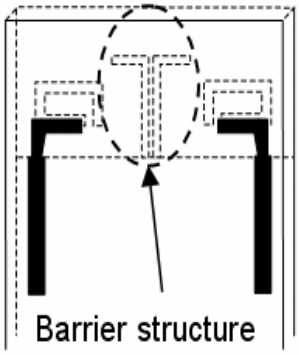
Fig. 2-2.2 illustrates the measured radiation patterns of the antenna with broadside coupling at various frequencies (2.45 GHz, 5.25 GHz, and 5.8 GHz). As can be seen, good radiation patterns were obtained. At 2.45 GHz (Fig. 2-2.2 (a)), the measured pattern is close to an omni-directional one in every measurement plane. Especially, in the YZ plane, a peak gain of 1.44 dBi and average gain of -0.71 dBi were achieved. At 5.25 GHz (Fig. 2-2.2 (b)) and 5.8 GHz (Fig. 2-2.2 (c)), the XZ-plane and YZ-plane patterns are also nearly omni-directional. The maximum peak gain and average gain at 5.25 GHz are 5.24 dBi and -0.29 dBi, respectively, and those at 5.8 GHz are 4.96 dBi and 0.18 dBi.



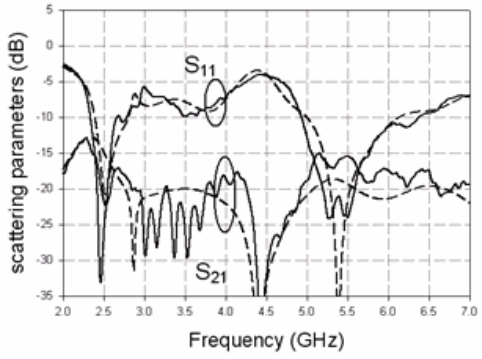
(a) (b) (c)

Fig. 2-2.2 Measured radiation patterns of the proposed antenna (a) 2.45 GHz, (b) 5.25 GHz, and (c) 5.8 GHz.

Finally, we have designed a simple barrier structure in between two closely-spaced diversity antennas for decreasing the mutual coupling between antennas (Fig. 2-2.3). The 10-dB return-loss bandwidths are still broad enough for the dual-band application in WLAN 802.11a/b/g, and, particularly, the isolation was increased larger than 13 dB at both bands. The measured radiation patterns are similar to those of the stand-alone antenna, but slightly weaker at the direction of the barrier structure.



(a)



(b)

Fig. 2-2.3. (a) Two closely spaced antennas with a barrier structure and (b) the corresponding measured (solid line) and simulated (dashed line) scattering parameters.

3. NUFFT Algorithm Incorporated into the SDA (spectral domain approach)

On the other hand, the NUFFT (nonuniform Fast Fourier Transform) algorithm is incorporated into the SDA (spectral domain approach) for fast and accurate analysis of multiple coupled microstrip lines. The results are in Table I. Table I shows the convergence analysis and comparison of the CPU time for a quasi-TEM mode of an eight-line microstrip structure obtained by the traditional SDA and the proposed method. If the NUFFT result with $N_b = N_g = 4$, $N_f = 128$ is compared with the SDA result with $N_s = 2\times10^4$, an improved computation efficiency of 60 times is obtained.

TABLE I. CONVERGENCE ANALYSIS AND COMPARISON OF THE CPU TIME FOR A QUASI-TEM MODE OF AN EIGHT-LINE MICROSTRIP STRUCTURE OBTAINED BY THE TRADITIONAL SDA AND THE PROPOSED METHOD.

Traditional SDA		**β/k_0 (CPU time in seconds) by the NUFFT**				
N_s	**β/k_0 (CPU)**	**N_b**	**N_g**	**$N_f = 64$**	**$N_f = 128$**	**$N_f = 1024$**
1×10^3	**2.63324 (3.30)**	**2**	**2**	**2.60926 (0.50)**	**2.60941 (0.57)**	**2.60944 (1.59)**
2×10^3	**2.61352 (6.46)**		**64**	**2.60925 (1.93)**	**2.60940 (1.99)**	**2.60943 (3.07)**
5×10^3	**2.61011 (18.5)**	**3**	**3**	**2.60912 (0.80)**	**2.60926 (0.91)**	**2.60929 (2.42)**
1×10^4	**2.60963 (38.8)**		**64**	**2.60913 (2.95)**	**2.60927 (3.04)**	**2.60931 (4.63)**
2×10^4	**2.60945 (78.3)**	**4**	**4**	**2.60913 (1.15)**	**2.60927 (1.28)**	**2.60930 (3.27)**
5×10^4	**2.60935 (192)**		**64**	**2.60913 (4.00)**	**2.60927 (4.11)**	**2.60931 (6.18)**
1×10^5	**2.60933 (384)**	**5**	**5**	**2.60913 (1.53)**	**2.60927 (1.69)**	**2.60930 (4.15)**
2×10^5	**2.60931 (767)**		**64**	**2.60913 (5.04)**	**2.60927 (5.15)**	**2.60931 (7.74)**

The NUFFT allows the sampled data in both original and transformed domains to be nonuniformly distributed. It is believed that this is the first time that the NUFFT algorithm has been employed to an application in researches of microwave engineering. The algorithm was also extended to two-dimensional case for tackling analysis of microstrip circuits and discontinuities. It is because that the current and electric field have rapid changes near metallic edges, fine discretization of the circuit becomes a must in fast and accurate analysis of a microstrip circuit or discontinuity. It is believed that the extension to the 2D-NUFFT can be recognized as a pioneer in this field. The paper was accepted in June 2004 for publication on the *IEEE MTT* transaction.

4. Simulation and Modeling of Nano-scale High Frequency Devices and Components

4-1 Optimal structure design for high-speed nanowire FETs

4-1.1 Silicion surrounding- and omega-shaped-gate FinFETs

Our examination presented here provides a novel alternative in the fabrication of next generation high-speed nanodevices. The FET is right the omega-shaped nanowire FinFETs. Considering device performance and manufacturability, an omega-shaped-gate FinFET with 70% coverage demonstrates an optimal candidate. To explore the structure optimization with respect to several important electrical characteristics for sub-10 nm nanowire FinFETs, a three-dimensional (3D) quantum correction CAD simulation is developed in this work. Our 3D modeling and simulation considers transport as well as quantum mechanical effects for the examined devices. Two different nanowire FinFETs, the surrounding- and omega-shaped-gate FETs are explored and compared in terms of the on/off current ratio, the turn-on resistance, the gate capacitance, the subthreshold swing, and the threshold voltage. Shown in the figures 4-1.1 and 4-1.2, it is found that the characteristic difference between the surrounding-gate FinFET and the omega-shaped-gate FinFET with 70% coverage is insignificant; however, the fabrication of the omega-shaped-gate FinFET with 70% coverage is much accessible than the surrounding-gate FinFET. Therefore, the omega-shaped-gate FinFET is promising for next generation high-speed applications.

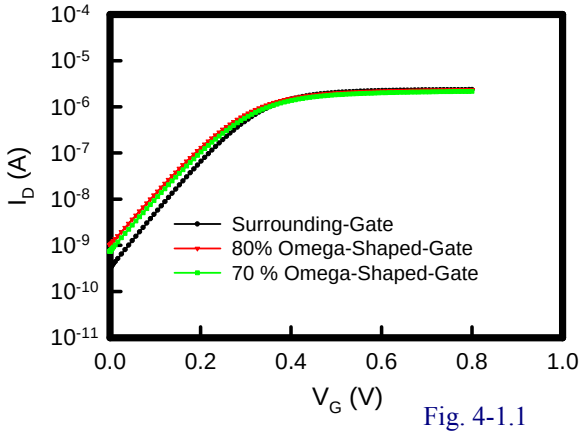


Fig. 4-1.1

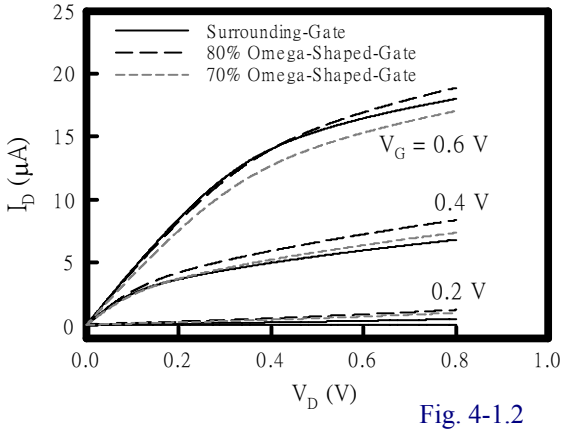


Fig. 4-1.2

Fig. 4-1.1 Transfer characteristics of the silicon nanowire FETs with various gate coverage ratios.

Fig 4-1.2 Output characteristics of the silicon nanowire FETs with various gate coverage ratios.

4-1.2 Strained silicon nano-wire FETs

To enhance the RF characteristics of ultrasmall nanoscale FETs, shown in Fig. 4-1.3, the omega-shaped-gate strain silicon nanowire FETs are further investigated and optimized in this work. Optimized nanowire devices possess high electrical performance and accessible fabrication manufacturability, shown in the figures 4-1.4 and 4-1.5. This investigation greatly enhances the possibility of fabrication for high performance FETs in realization of high-speed circuit design. The improvement is mainly resulted from the fact that the omega-shaped-gate strain FET not only encounters fabrication's problems with compatible advanced CMOS fabrication technology but also has much superior controllability of channel.

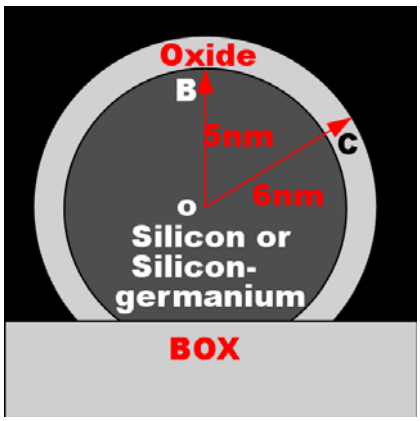


Fig. 4-1.3 A cross-sectional plot of the omega-shaped-gate strained nanowire FET.

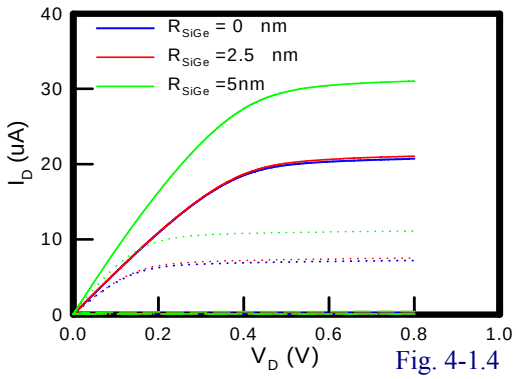


Fig. 4-1.4

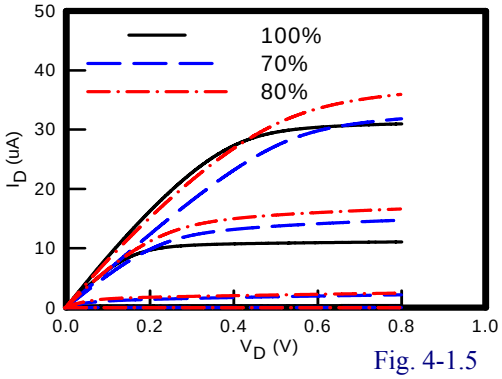


Fig. 4-1.5

Fig. 4-1.4 Comparison of the output characteristics between the silicon and strained silicon nanowire FETs

Fig. 4-1.5 Output characteristics of the strained silicon nanowire FETs with different gate coverage ratios.

4-2 Modeling and Simulation of ESD protection design

4-2.1 TCAD platform for ESD protection device optimization in RF SOI circuits

Silicon-On-Insulator (SOI) CMOS has been of great interest due to its superior properties in high-speed applications. It suppresses the latch-up, reduces the junction capacitance, and immunizes circuit noises. However, the electrostatic discharge (ESD) is one of major roadblocks for the SOI technology; in particular for, nanodevices and gigacircuit. In this project, we develop a TCAD platform in investigating the scaling properties for ESD robustness of the protection devices. Due to the gate length reduction, ESD robustness decreases abruptly in nanodevices, shown in Fig. 4-2.1. This observation is totally different from the result shown in Fig. 4-2.2. By measuring the failure

current, we observes that the robustness reduction in ESD protection nanoscale thin body SOI devices. With our simulation and measurement, we explore the failure mechanism and propose an optimal device structure for the ESD robustness.

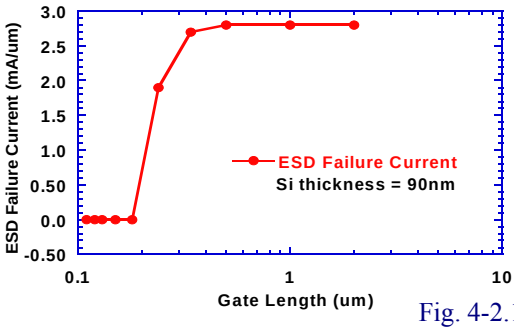


Fig. 4-2.1

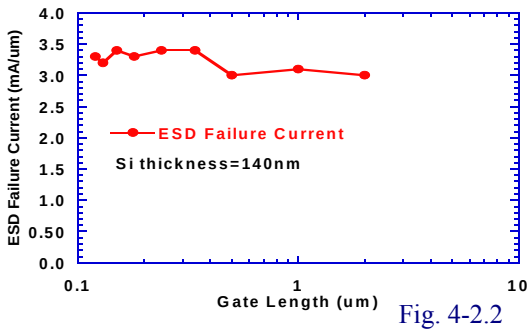


Fig. 4-2.2

Fig. 4-2.1 ESD robustness versus the gate length of thin body SOI devices

Fig. 4-2.2 ESD robustness versus the gate length of thick body SOI devices

4-2.2 Fully silicided MOSFETs structure for robustness and efficiency of ESD protection circuits

In this project, new fully silicided MOSFET structures are designed to explore the robustness and efficiency of ESD protection circuit for RF circuit applications. Owing to an omission of the conventionally used drain ballast resistors, a simplified manufacturing process and a reduced device area are achieved simultaneously, shown in Fig. 4-2.3. The most important part is the area reduction which lowers the parasitic capacitance, shown in Table II. Thus this investigation is especially suitable for RF circuits. It is believed that the realizations are mainly from the floating charge effects during the ESD events. To avoid floating charges induced threshold voltage lowering when the circuit turns-on, an embedded switch is therefore designed. The newly designed device structure is attractive in novel ESD design with much low cost, small size, and high efficiency.

Table II. A comparison of the layout properties between the proposed and conventional ESD projection devices.

Parameters / Device type	Drain	Source	Gate	Total	Ratio
FULLY-SILCIDED	0.4	0.4	0.09	0.89	1
SILICIDE BLOCKED	5	0.4	0.09	5.49	6.2

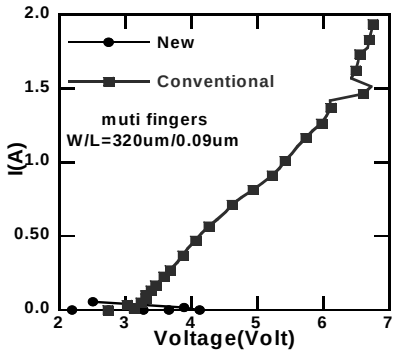
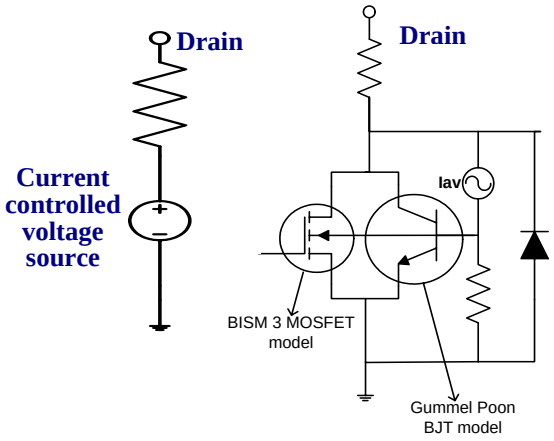


Fig. 4-2.3 ESD robustness difference between the new and conventional fully-silicided devices.

4-2.3 A physical-based equivalent circuit model for ESD protection simulation

Physically-sound equivalent circuit model plays an important role in ESD protection circuit design; in particular, for RF IC circuit design. A novel ESD equivalent circuit model for advanced device and circuit simulation is developed, shown in the figure 4-2.4. As shown in Fig. 4-2.5, our model successfully accounts for the snapback characteristics and geometry effect of devices. It has been incorporated into our RF circuit simulation for whole chip ESD protection circuit without numerical difficulties. Therefore, ESD weakness in large signal RF circuits can be explored.



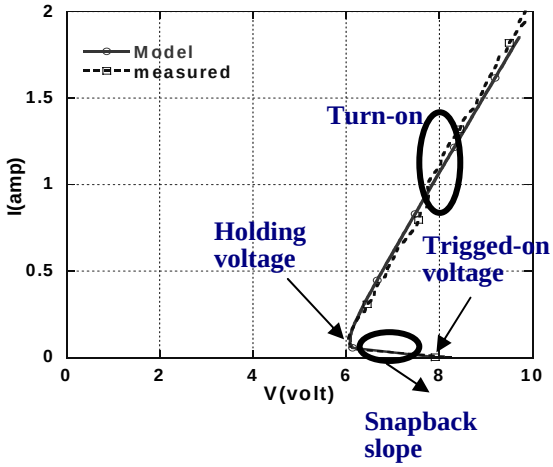


Fig. 4-2.4 Fig. 4-2.5

Fig. 4-2.4 The left circuit is conventional model and the right one is our solution.

Fig. 4-2.5 Comparison between the experimental (dotted line) and simulation data (solid line).

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X. APPENDIX VI – RESEARCH OUTCOME OF THE SECOND YEAR

1. Novel Tri-Dimensional Microwave Components

1-1 Dual-band Bandpass Filter of Serial Configuration Using LTCC Technology

In this year, we have proposed the dual bandpass filters with serial-configuration (Fig. 1-1.1). The structure of the dual bandpass filter consists the inductive coupled-line (ICL) filter and the capacitive coupled-line (CCL) filter. In this serial-configuration concept, the method of producing transmission zeros is to serially connect two-port networks, sum the impedance matrices ($Z_U(\omega)$ and $Z_L(\omega)$) and make the sum equal to zero ($Z_U(\omega)+Z_L(\omega)=0$). Thus, the transmission zeros occur at that frequencies. The serial-configuration design concept described in this study is clearly extendable to two networks with equal magnitudes (Fig. 1-1.2(a)) and opposite phases (Fig. 1-1.2 (b)) to generate finite transmission zeros. Two dual bandpass filters, with center frequencies of 2.4 GHz and 5 GHz, have been designed and implemented with LTCC process (Fig. 1-1.4). The measured results (Fig. 1-1.3) agree quite well with the simulation ones. Fig. 1-1.3(a) shows the dual bandpass filter consisted of the ICL filter for 2 GHz and the CCL filter for 5 GHz and Fig.1-1.3(b) shows the dual bandpass filter included the CCL filter for both 2 GHz and 5 GHz. It is clear to see that the dual bandpass filter made up of different filters (ICL and CCL) has a transmission zero between the two passbands. Without the obvious transmission zeros between two passbands, the result in Fig. 1-1.3(b) still has the suppression more than -20dB at 3.6GHz. The fabricated dual bandpass filters are found to be compact with low insertion loss in the passbands, wide bandwidth in the high passband, and high suppression between the two passbands.

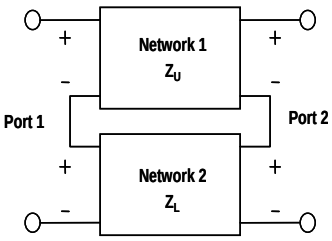


Fig. 1-1.1

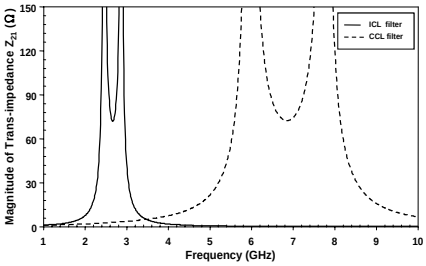


Fig. 1-1.2 (a)

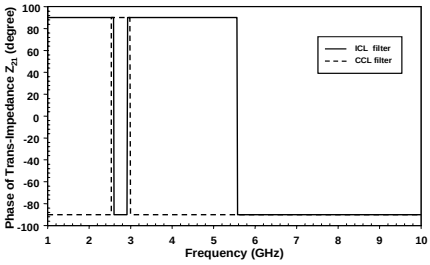


Fig. 1-1.2 (b)

Fig. 1-1.1 A representation of the proposed dual bandpass filter with serially-connected two-port network.
Fig. 1-1.2 (a) The magnitude responses of the trans-impedance Z_{21} (b) The phase responses of the trans-impedance Z_{21} for the ICL and CCL filters. The solid lines denote the ICL filter and the dashed line denote the CCL one. The finite transmission zeros are located where the solid line intersects with the dashed lines.

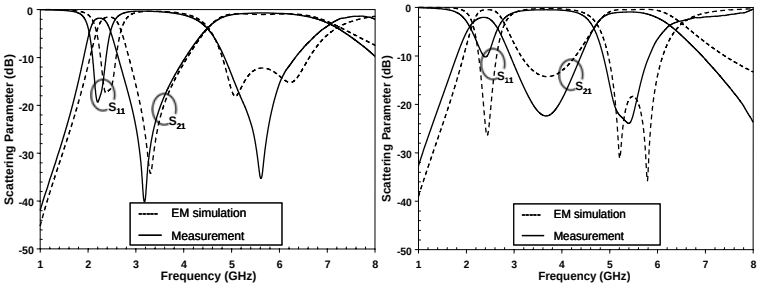


Fig. 1-1.3 Simulation and measurement results of (a) the dual bandpass filter with the ICL filter for 2 GHz and the CCL filter for 5 GHz (b) the dual bandpass filter with the CCL filters for both 2 GHz and 5 GHz.

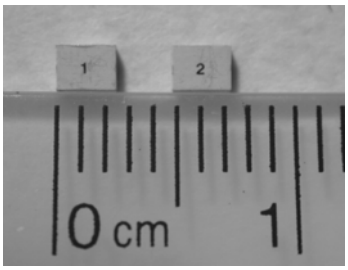


Fig. 1-1.4 The photograph of the two dual bandpass LTCC filters.

1-2 Dual-band RF Front-End Module for WLAN IEEE 802.11 a/b/g Applications

Under the IEEE 802.11a/b/g WLAN specifications, this study presents a dual-band RF FEM (Front-End Module) on LTCC substrate comprising two diplexers, two band-pass filters and two low-pass filters as a 802.11a/b/g SiP (System-in-Package) solution (block diagram is shown in Fig. 1-2.1). To implement, a 5GHz LNA, dual-band DPDT (Double Pole, Double Throw) switch and power detector mounted on the surface of LTCC RF module are also integrated into the proposed module where has only 5.4mm × 4.0mm × 0.9mm in size. On the side of transmitter, the simulated insertion losses of the dual-band FEM are 0.7 and 0.6dB in 2.4-2.5 and 4.9-5.9GHz frequency bands, respectively. The maximum rejection characteristic is -30dB in the second and third harmonic bands. On the side of receiver, the simulated insertion losses are 1.7 and 1.2dB in 2.4-2.5 and 4.9-5.9GHz bands, respectively. The maximum of both the isolation and rejection characteristics is -30dB.

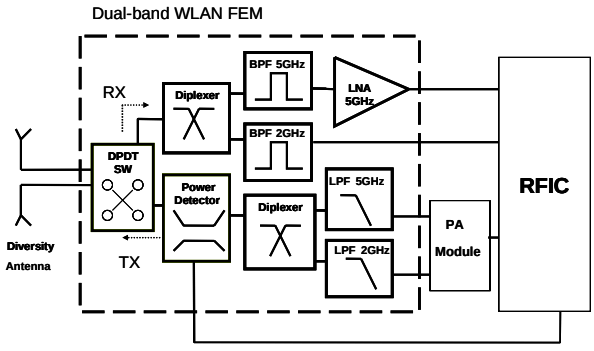


Fig. 1-2.1 A block diagram of the proposed dual-band WLAN front-end module

- RX Path: a diplexer, two band-pass filters and a 5GHz LNA.
- The simulated insertion losses are 1.7 and 1.2dB in 2.4-2.5 and 4.9-5.9GHz bands, respectively (Fig. 1-2.2).
- The maximum of both the isolation and rejection characteristics is -30dB.

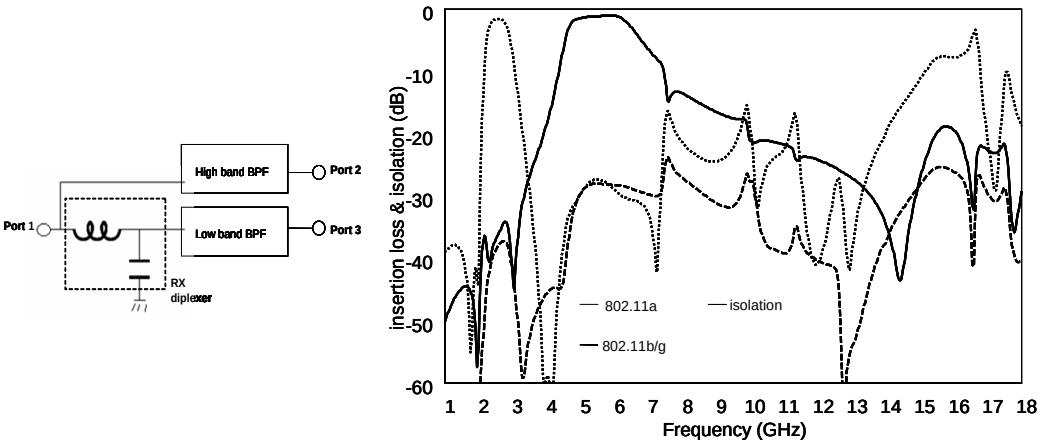


Fig. 1-2.2 The circuit of RX diplexer and the simulated results of RX path.

- TX Path: a diplexer, two low-pass filters and a power detector.
- The diode and SMD of power detector are mounted on the LTCC surface layer.
- The simulated insertion losses are 0.7 and 0.6dB in 2.4-2.5 and 4.9-5.9GHz bands, respectively (Fig. 1-2.3).
- The maximum rejection characteristic is -30dB in the second and third harmonic bands.

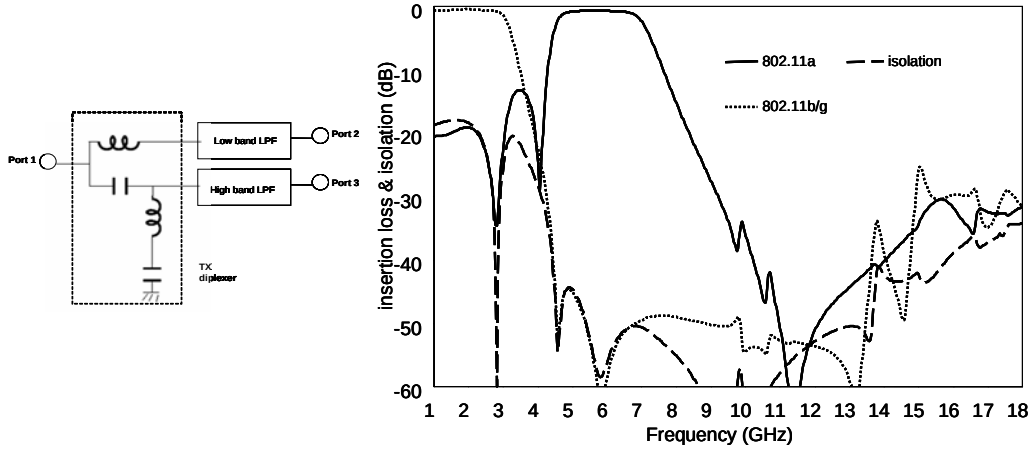


Fig. 1-2.3 The circuit of TX diplexer and the simulated results of TX path.

The couple line is designed to catch the TX power on a schottky diode, which transfers the power into a voltage level. Fig. 1-2.4 demonstrates the measured result. The passive circuits are integrated into a LTCC 3D circuitry module, where has 14 layers and 5.4mm × 4.0mm × 0.9mm in size. Since the module is very small, there are lots of coupling effects between the components. To avoid these effects, a shorting via is needed. In addition, the shorting via can suppress the high frequency resonance which is caused by the cavity structure.

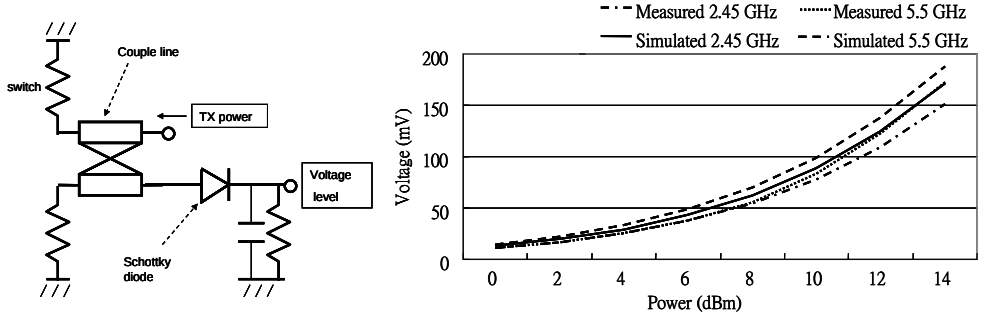


Fig. 1-2.4 The circuit diagram and the measured results of the power detector.

- The RX 5 GHz path has a maximum gain of 14 dB. (Fig. 1-2.5)
- The measured insertion loss of RX 2.45 GHz is -2.6 dB. (Fig. 1-2.5)
- The measured isolation between 2.45 GHz and 5 GHz are larger than 27 dB. (Fig. 1-2.5)

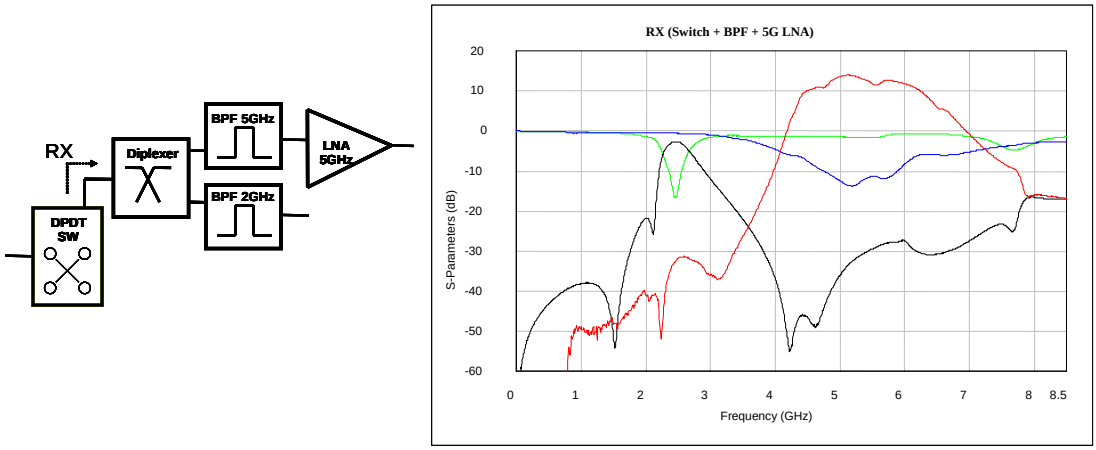


Fig. 1-2.5 The measured results of the RX path, including a DPDT switch, 2 BPFs, and a 5GHz LNA.

- The measured insertion loss of TX 2.45 GHz is -2 dB. (Fig. 1-2.6)
- The measured insertion loss of TX 5 GHz is -2.6 dB. (Fig. 1-2.6)
- The measured isolation between 2.45 GHz and 5 GHz are larger than 20 dB. (Fig. 1-2.6)

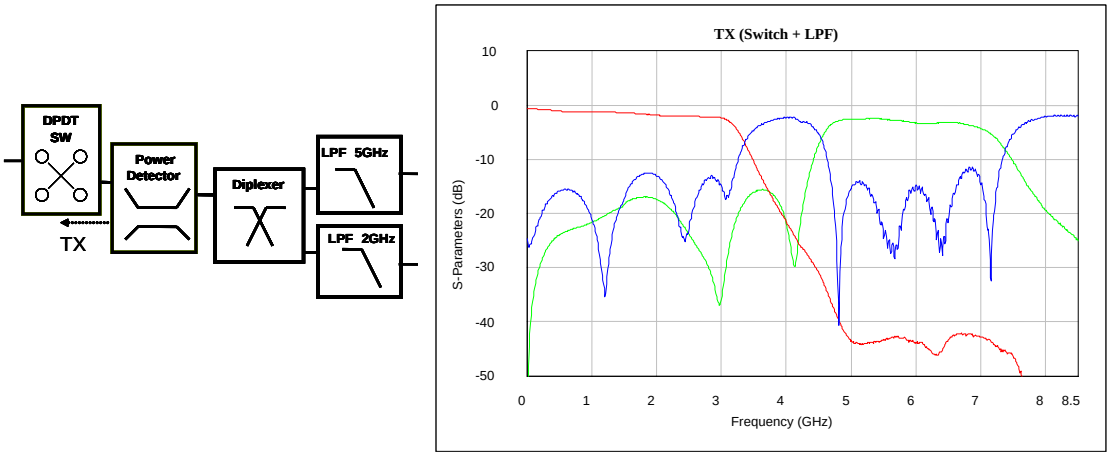
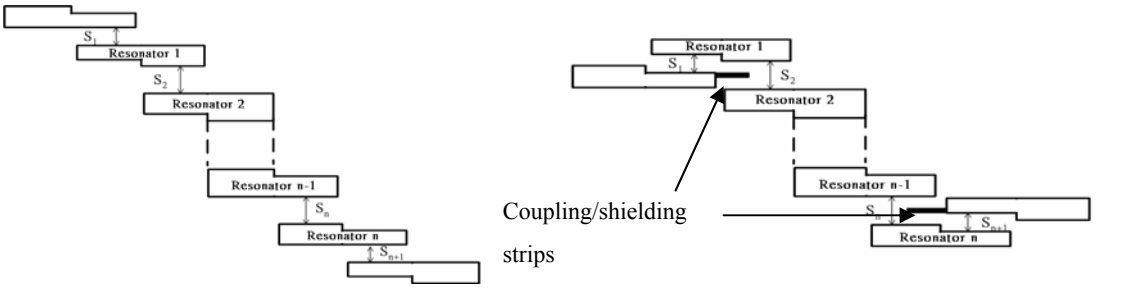


Fig. 1-2.6 The measured results of the TX path, including a DPDT switch and 2 LPFs.

1-3 Modified Parallel-Coupled Filter with Two Independently Controllable Upper Stopband Transmission Zeros

Fig. 1-3.1 shows the proposed filter and a conventional parallel coupled filter. All physical dimensions are the same between newly proposed filter and convention filter except two extra small coupling/shielding strips being added in the modified filter which can easily control two transmission zeros independently. This newly proposed filter largely simplifies the design procedures of CT-type filter.



(a) (b)

Fig. 1-3.1 (a) conventional filter, and (b) modified filter.

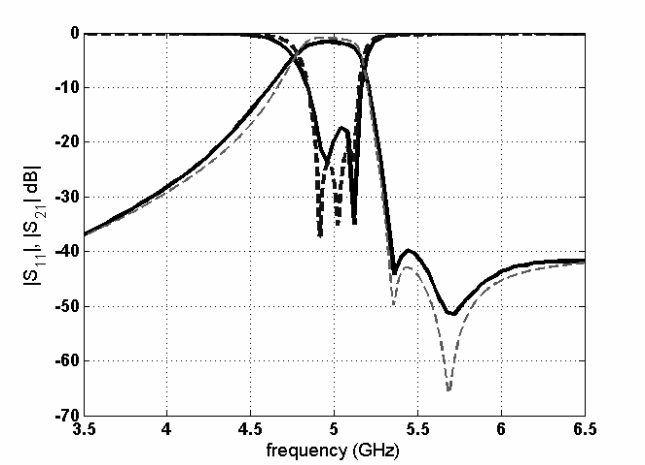


Fig. 1-3.2

1-4 Miniaturized Ultra-Broadband Quadrature Hybrid Using VIP Structure

Miniaturized ultra-broadband quadrature hybrid using CPW multi-section structure incorporation with modified VIP structure is presented this year. The proposed quadruture hybrid has a size of merely 17mm × 6mm and measured bandwidth of as large as 1.9 to 17.2 GHz.

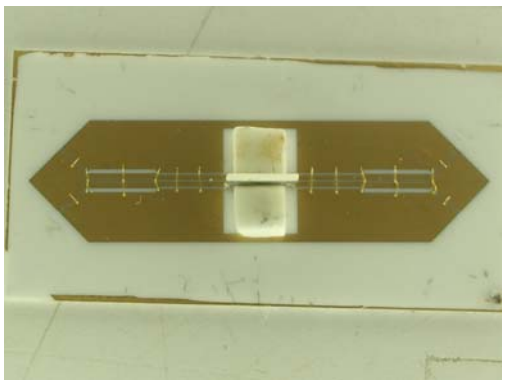


Fig. 1-4.1

Fig. 1-4.1 shows the photograph of the proposed quadrature hybrid. A 5-section design is demonstrated here to cover a theoretical 9 to 1 bandwidth. The measured performance is shown in Fig. 1-4.2.

This quadrature hybrid is for the first time combining CPW and VIP technology to implement

this kind of ultra-broadband coupler. The proposed circuit has the benefits of small size, good performance, and without thin wires and small gaps.

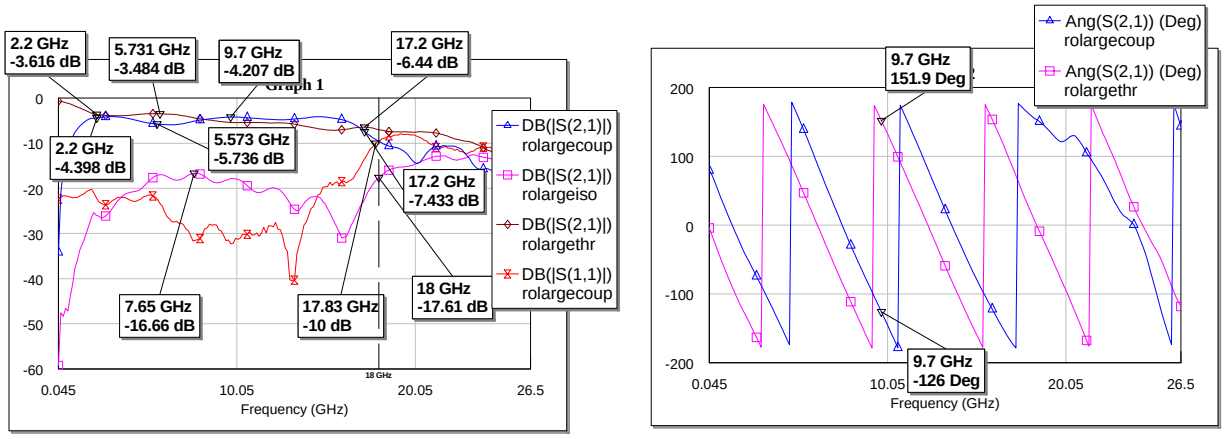


Fig. 1-4.2

1-5 CPW-CPS Mouw's Hybrid Junction Ultra-Broadband Star Mixer

A CPW-CPS Mouw's hybrid junction ultra-broadband star mixer has been proposed by us in 2001 using thin film circuit technology. This year we implement this circuit in MMIC circuit form by spiraling the CPS line. The spiral CPS line not only reduces the circuit size but also broaden the bandwidth. Fig. 1-5.1 shows the photograph of the chip.

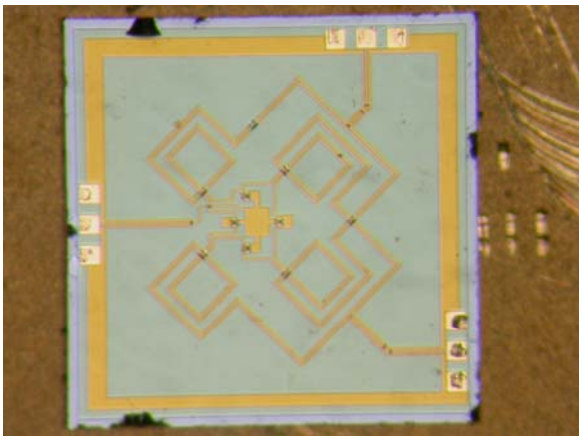


Fig. 1-5.1

The chip has three different mounting environments. That is absorber backed, conductor backed, and alumina substrate plus absorber. The measured performances are depicted in Fig. 1-5.2. The measured RF/LO bandwidth is from 1.5 to 37GHz.

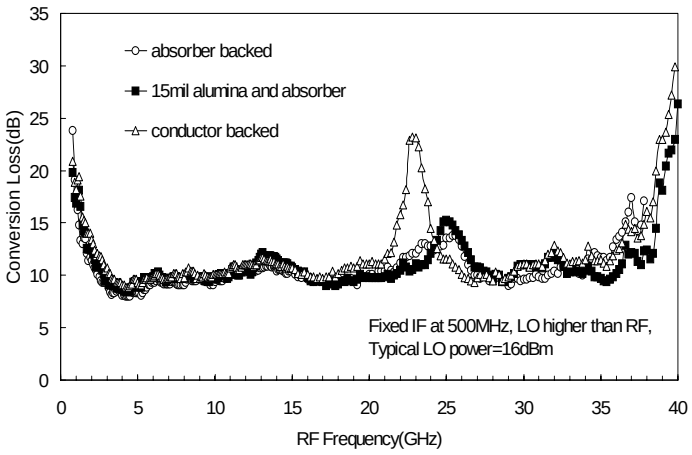
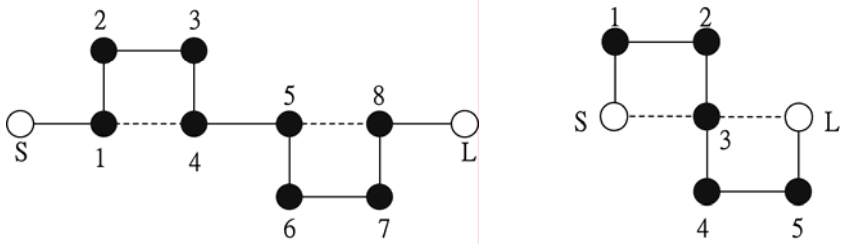


Fig. 1-5.2

The chip size is 2mm by 2mm where no external baluns or biasing circuits are required. This chip uses WIN's 0.15 m pHEMT device with gate width of 2X50 m.

1-6 Five-Pole Cascade Quadruplet (CQ) Microstrip Filter

A five-pole cascade quadruplet (CQ) microstrip filter has two pairs of transmission zeros has been developed. Usually a CQ filter with two pairs of transmission zeros should be an 8-pole filter. However, the newly proposed coupling scheme can reduce the filter from 8-pole to 5-pole. Fig. 1-6.1 shows the coupling scheme of conventional CQ and proposed CQ filter.



(a) (b)

Fig. 1-6.1 coupling scheme of (a) conventional CQ, and (b) proposed CQ filter.

According the coupling scheme, a microstrip filter combining hairpin line and straight line resonators has been proposed as shown in Fig. 1-6.2.

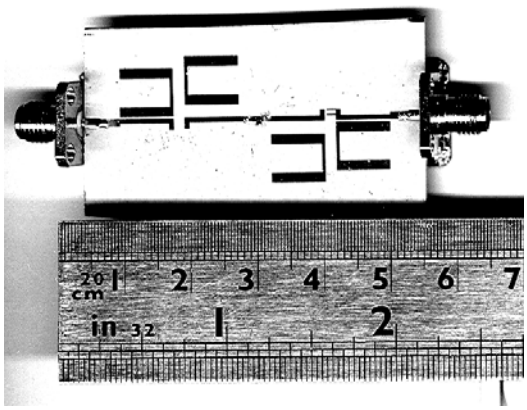


Fig. 1-6.2

In Fig. 1-6.2, the coupling of resonator 3 is most complicated that it should couple to source, load, resonator 2, and resonator 4. In the photograph these coupling can be easily identified. The simulated and measured performances are both shown in Fig. 1-6.3.

Ths simulated and measured results are matched quite well. This design provides a way to implement microstrip CQ filter with two pairs of transmission zeros with much smaller circuit size.

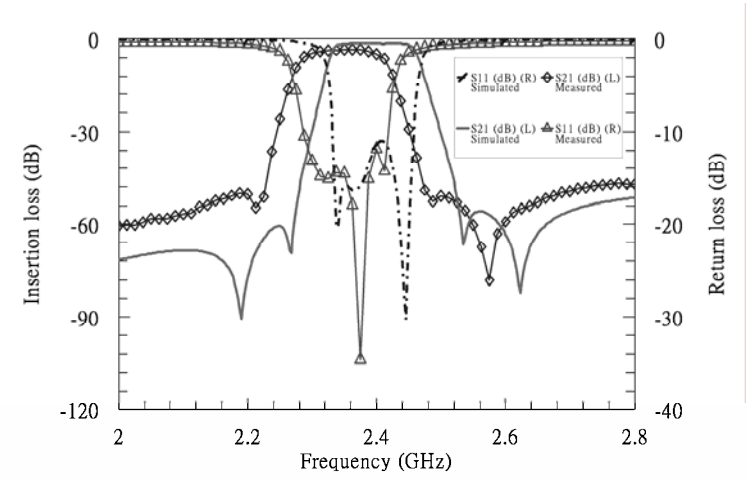


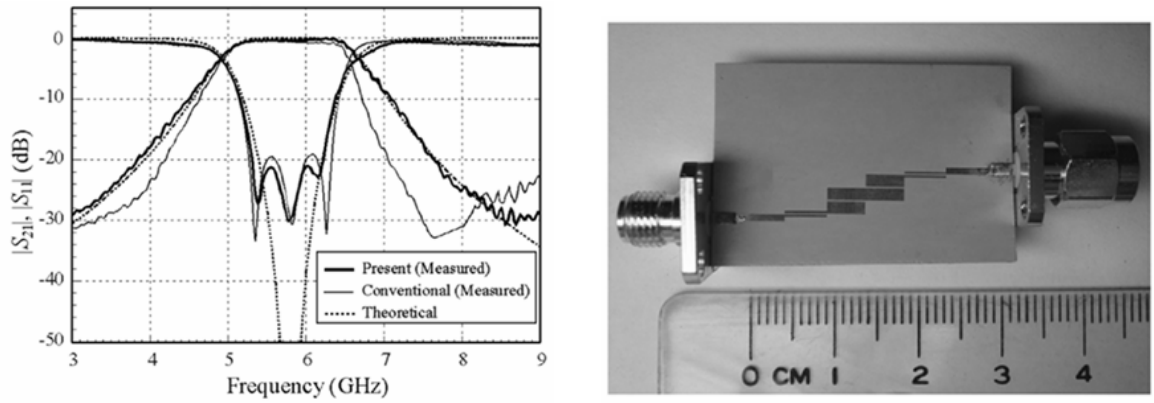
Fig. 1-6.3

1-7 Modified Insertion Loss Function Synthesis of Maximally Flat Parallel-Coupled Line Bandpass Filters

Table Ⅰ lists the simultaneous conditions for determining S_i and T_i to derive the necessary Z_{oo}/Z_{oe} values for each coupled stage. Parallel coupled line filters with maximally flat responses of order $N \le 6$ are synthesized based on derived IL functions. Simultaneous equations for maximally flat responses and the condition are formulated for determining Z_{oo} and Z_{oe} of each coupled stage. The under-determined conditions leave several degrees of freedom in choosing the circuit dimensions. By properly utilizing these degrees of freedom, the problem resulted from the tight coupled line dimensions can be resolved by gathering all difficulties to the end stages and employing tapped input/output to replace the end stages. Four circuits are simulated and three of them are fabricated and measured to demonstrate the formulation and circuit synthesis. The measured results manifest very accurate BWs and show that the proposed method not only provide a significant improvement in predicting the filter BW, but also preserve the quality of passband responses.

TABLE I
MAXIMALLY FLAT CONDITIONS FOR $N = 1 \sim 6$

N	Maximally Flat Conditions	Degree of Freedom
1	$S_1 = 2$	0
2	$S_1 = 2$ $2T_2 = T_1^2$	1
3	$S_1 = 2$ $4T_2^2(S_1 + S_2) = T_1^2(S_1T_2^2 + S_2T_1^2)$	1
4	$S_1 = 2$ $2T_2^2 = T_1^2T_3$ $[2T_3(S_1 + S_2) + T_1^2(S_2 + S_3)]^2 = 2T_1^2[T_1^2(S_2 + S_3)^2 + T_2^2S_1(S_2 + S_3) + T_3^2S_1(S_1 + S_2)]$	2
5	$S_1 = 2$ $4T_2^2[T_3^2(S_1 + S_2) + S_3T_2^2] = T_1^2T_3^2[S_1T_2^2 + T_1^2(S_2 + S_3)]$ $8T_2^2S_3(S_1 + S_2) + 4T_3^2(S_1 + S_2)^2 = T_1^2[T_1^2S_3(S_2 + S_3) + 2T_2^2S_1S_3 + 2T_3^2S_1(S_1 + S_2)]$	2
6	$S_1 = 2$ $2T_2^2T_4 = T_1^2T_3^2$ $4[T_2^2(S_3 + S_4) + T_3^2(S_1 + S_2)]^2 = 2T_1^2T_3^2[T_1^2(S_2 + S_3)(S_3 + S_4) + T_2^2S_1(S_3 + S_4) + T_3^2S_1(S_1 + S_2)]$ $+ T_4^2(S_2 + S_3)[T_1^4(S_2 + S_3) + 2T_1^2T_2^2S_1 - 8T_2^2(S_1 + S_2)]$ $4(S_1 + S_2)(S_2 + S_3)[2T_2^2(S_3 + S_4) + 2T_3^2(S_1 + S_2) + T_4^2(S_1 + S_2)]$ $= T_1^2[T_1^2(S_2 + S_3)(S_3 + S_4)^2 + 2T_2^2S_1(S_3 + S_4)^2 + 4T_3^2S_1(S_1 + S_2)(S_3 + S_4) + 2T_4^2S_1(S_1 + S_2)(S_2 + S_3)]$	3



(a) (b)

Fig. 1-7.1 (a) Theoretical and measured responses of filter . (b) Photograph of the fabricated circuit. f_0 = 5.8 GHz, N = 3, Δ = 30 %. Circuit dimensions: W_1 = 0.24 mm, G_1 = 0.15 mm, W_2 = 1.45 mm, G_2 = 0.13 mm. The linewidth of the quarter-wave transformer is 0.8 mm. Substrate: ε_r = 10.2, thickness = 1.27 mm.

1-8 Microstrip Bandpass Filters with A Dual-Passband Response

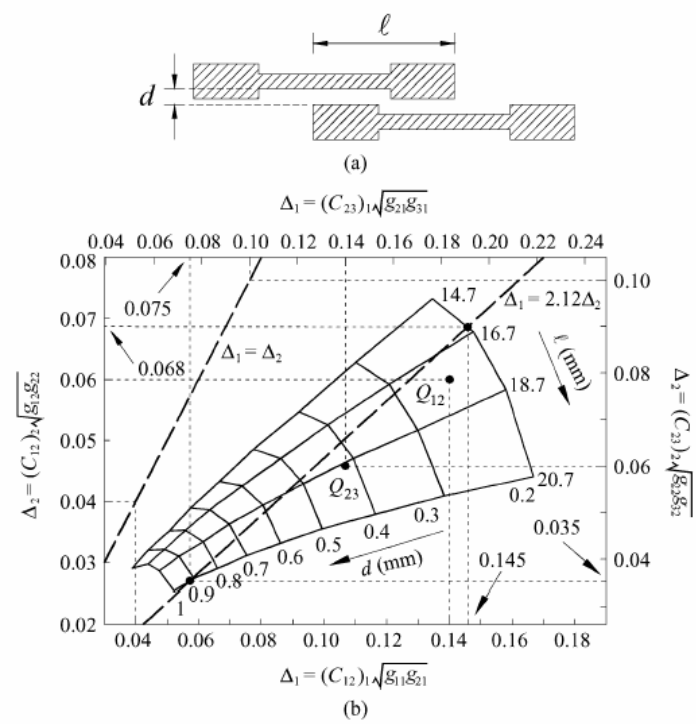


Fig. 1-8.1 (a) Coupling structure. (b) Fractional bandwidth design graph. f_1 = 2.45GHz, f_2 = 5.2GHz. Dimensions of SIR in mm: W_1 = 0.89, W_2 = 1.30, ℓ_1 = 11.38, ℓ_2 = 9.32. Substrate: ε_r = 2.2, thickness = 0.508mm.

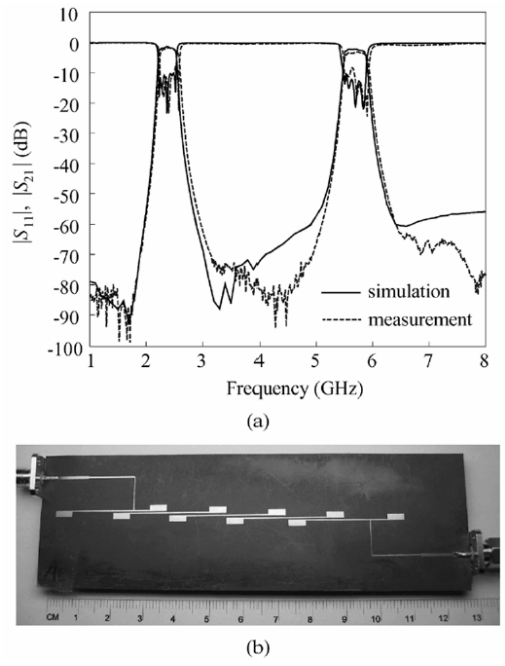
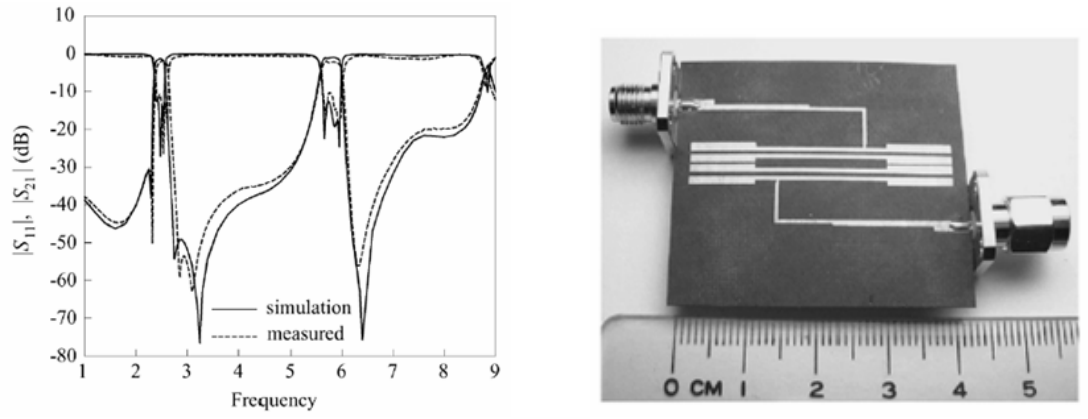


Fig. 1-8.2 (a) Simulation and measured responses of a fifth-order Chebyshev filter. f_1 = 2.45GHz, f_2 = 5.8GHz, Δ_1 = 12%, Δ_2 = 7%. Dimensions of SIR in mm: W_1 = 0.34, W_2 = 1.86, ℓ_1 = 11.76, ℓ_2 = 5.04. (b) Photograph of the filter. Substrate ε_r = 2.2, thickness = 0.508 mm.



(a) (b)

Fig. 1-8.3 (a) Simulation and measured responses of a fourth-order stacked-line filter of type A. f_1 = 2.45GHz, f_2 = 5.8GHz, Δ_1 = 7.2%, Δ_2 = 6.0%. Dimensions of the SIRs are in Fig. 4. Tap position x = 12.7mm. (b) Photograph of the filter.

1-9 Microstrip Bandpass Filters for Ultra-Wideband (UWB) Wireless Communication

A new technique is derived for designing a composite microstrip bandpass filter (BPF) with a 3-dB fractional bandwidth of more than 100%. The design utilizes embedding individually designed highpass structures and lowpass filters (LPF) in to each other, followed by an optimization for tuning in-band performance.

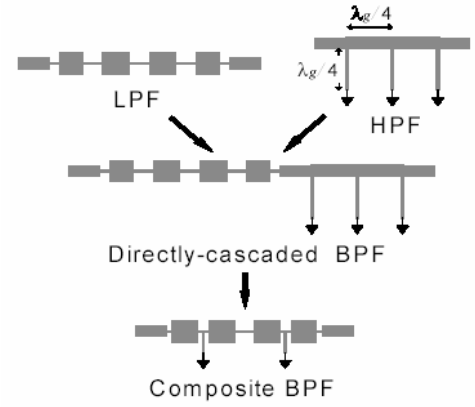


Fig. 1-9.1 Evolution of the proposed composite BPF.

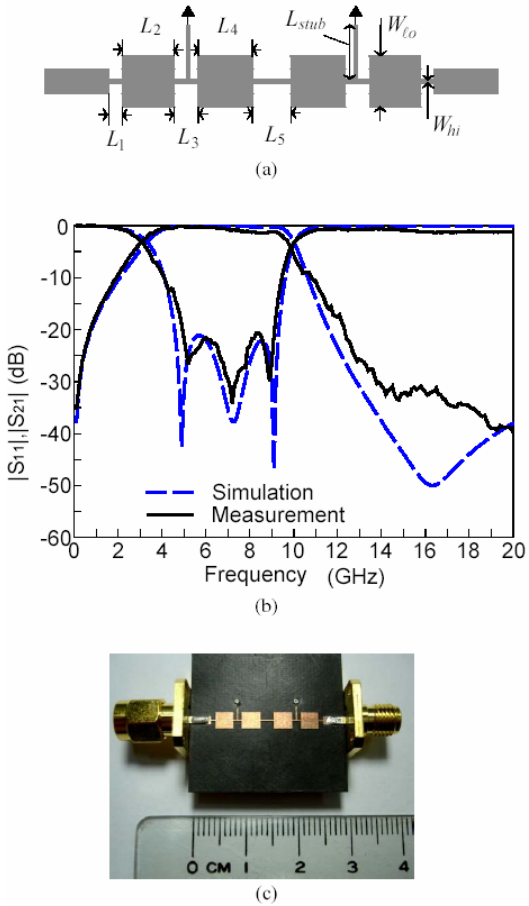


Fig 1-9.2 (a) Geometry of the fabricated filter. $L_1 = 0.85$, $L_2 = 3.22$, $L_3 = 1.54$, $L_4 = 3.39$, $L_5 = 2.27$, $L_{stub} = 3.45$, all in mm. (b) Simulation and measurement responses. (c) Circuit photo.

2. New Tri-Dimensional Antenna

Dielectric-Loaded Quadrifilar Helix Antenna

The quadrifilar helix antenna (QHA) is a circular polarized antenna consisting of four helical arms excited by quadrature phase. The radiation pattern, when the whole helix is like a short rod with a proper axial length, the number of turns is one-half, and the end of arms connects to each other for generating a one-wavelength resonance between two arms, is omni-directional with a cardioid shape. We propose a miniature dielectric-loaded QHA which is one of the suitable ways for miniaturized antenna without changing the geometry. The proportion of scale-down size depends on the permittivity of dielectric. The higher permittivity implies the smaller antenna. Hence, the size of the proposed antenna is shrunk with a ceramic load which is a material mostly employed in antenna design by reason of low loss and high permittivity. The configuration then is very compact and can easily be integrated into a handset.

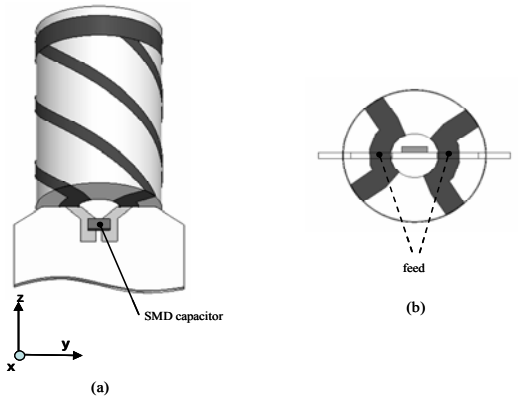


Fig. 2-1 Antenna structure (a) Overall structure including the matching capacitor
(b) The bottom view of the antenna rotated for self-phasing

The geometry of the proposed antenna is depicted in Fig. 2-1. The antenna dimensions are presented for operating frequency around 1.575GHz. The overall structure contains a dielectric-loaded antenna with printed metal strip and a small planar circuit board with a simple feeding and matching network. The dielectric entity is a ceramic rod with a hole through the center and a relative permittivity about 40. Significantly, the planar board has a protrusion used to fix together with the rod. The metal strip has four arms printed on the side wall and a metal ring on the top of side wall whereas the extension of arms on the bottom connects to the feed points of the antenna fed by a pair of lines. The geometry of these arms is designed for right-hand circular polarization (RHCP) radiation towards left-hand helix. The top of the rod is not printed in order to reduce the time for manufacture procedures but the performance keeps similar to the traditional one. Due to the high-permittivity dielectric material, the antenna is fabricated to a very small size with 4.5 mm in radius and 14.8 mm in height which is less than 0.08 λ .

The difference between the electrical lengths of two BHAs for circular polarization is achieved by making a little modification on geometry or offset of feed points. Fig. 2-1 (b) shows the rotated feed point locations involving two BHAs with different path lengths. While properly adjusting these two parameters, the circular polarization is generated. Moreover, RHCP and LHCP are determined by the relationship between L_1 and L_2 with fixed placement in two BHAs.

The radiation resistor of the proposed 1.575GHz QHA is less than 2Ω in such small size of the antenna. The loss tangent of ceramic rod is so small that the dielectric loss is ignored. It is needed to be very careful to match a small antenna for less loss in a matching circuit. There is an unavoidable short feeding line for the antenna with parasitic inductor in this structure. By using only one SMD (Surface Mount Device) capacitor and properly adjusting the parasitic inductor, the antenna can be matched. With a suitable value of capacitor, the antenna is acceptably efficient. The matching circuit on the PCB is shown in Fig 2-1(a). The placement and value of the capacitor associated with the geometry of feeding line can be selected to match the wanted impedance. The simple matching circuit is done in small size and almost not occupies any space on the PCB. Fig. 2-2 shows the simulated input impedance of QHA including a very short feeding line that is considered as a parasitic inductor. Besides, the impedance of matched QHA simulated by the model of SMD capacitor is also depicted. The capacitor used is Murata GRM1885C1H5R6DZ01 with the value of 5.6 pF. The resistor of input impedance is about 1.3Ω. Fig. 2-3, shows the simulated radiation

pattern having the properties of cardioid shape and omni-direction at the frequency 1.575GHz in the cardioid tip of the Smith chart.

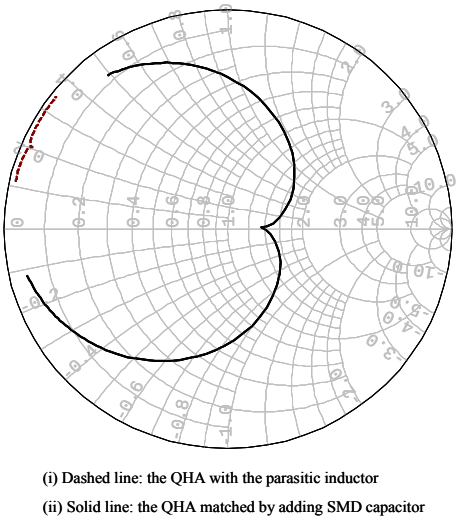


Fig. 2-2 Smith chart of simulation result

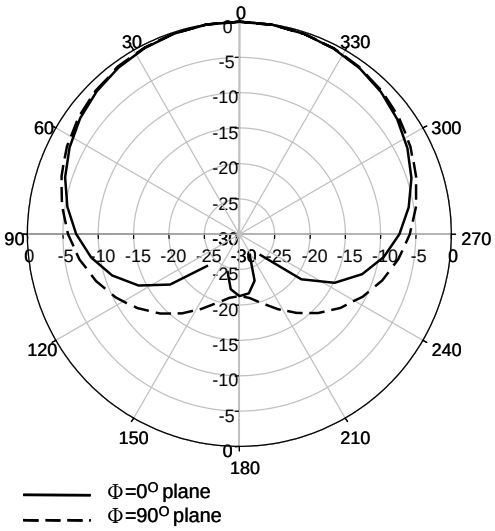


Fig. 2-3 Simulated radiation pattern

3. Application of 2-D Non-Uniform Fast Fourier Transform Algorithm

Application of two-dimensional nonuniform fast fourier transform (2-D NUFFT) technique to analysis of shielded microstrip circuits.

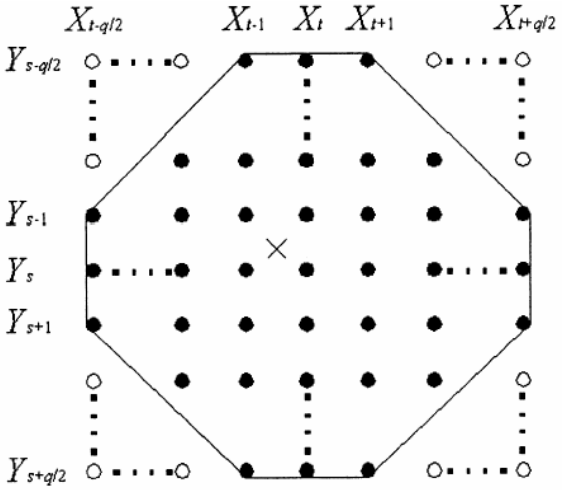


Fig. 3-1 2-D NUFFT algorithm: exponential function at a nonuniform sample point (x_t , y_s) is approximated by Fourier bases at $(q+1)\times(q+1)$ uniform oversampled grids (X_i ; Y_j) in a square neighborhood or by those in an octagonal neighborhood.

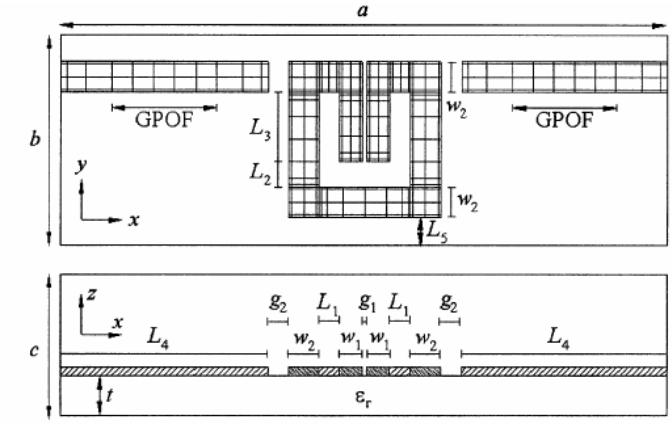


Fig. 3-2 Hairpin resonator in shielded box and its mesh scheme in analysis. Structure parameters are $\varepsilon_r = 10.2$, $L_1 = 0.7$, $L_2 = 1.01$, $L_3 = 2.74$, $L_4 = 8$, $L_5 = 6$, $w_1 = 1$, $w_2 = 1.19$, $g_1 = 0.2$, and $g_2 = 0.8$. All dimensions are in millimeters.

TABLE I
COMPARISON OF CPU TIME AND L_2 ERROR OF ONE CALL OF THE 2-D NUFFT IN ANALYSIS OF A HAIRPIN RESONATOR

Hairpin resonator	Square 2D-NUFFT		Octagonal 2D-NUFFT	
	CPU seconds	L_2 error	CPU seconds	L_2 error
$q = 4$	79.61	3.9479×10^{-4}	65.80	3.9603×10^{-4}
$q = 6$	152.85	5.5135×10^{-5}	116.22	5.5314×10^{-5}
$q = 8$	257.03	6.7144×10^{-6}	184.63	6.7381×10^{-6}
$q = 10$	381.52	7.9671×10^{-7}	256.18	7.9879×10^{-7}

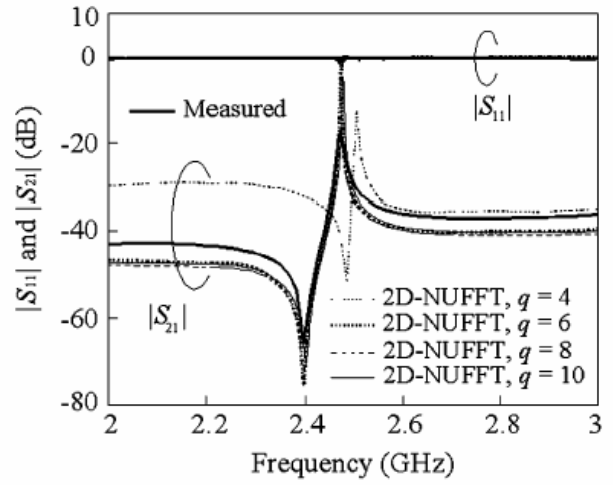


Fig. 3-3 Measured and calculated *S*-parameters of the hairpin resonator.

4. Simulation and Modeling of Nano-scale High Frequency Devices and Components

4-1 Schrödinger and Poisson's solver for nanodevice applications:

Numerical solution of the Schrödinger and Poisson equations (SPEs) plays an important role in semiconductor simulation. We present a robust iterative method to compute the self-consistent solution of the SPEs in nanoscale metal-oxide-semiconductor (MOS) structures. Based on the global convergence of the monotone iterative (MI) method in solving the quantum corrected nonlinear Poisson equation (PE), this iterative method is successfully implemented and tested on the

single-, double-, and surrounding-gate (SG, DG, and AG) MOS structures. Compared with other approaches, shown in Fig. 4, various numerical simulations are demonstrated to show the accuracy and efficiency of the method. (Computer Physics Communications. Vol. 169, No. 1-3, July 2005, pp. 309-312.)

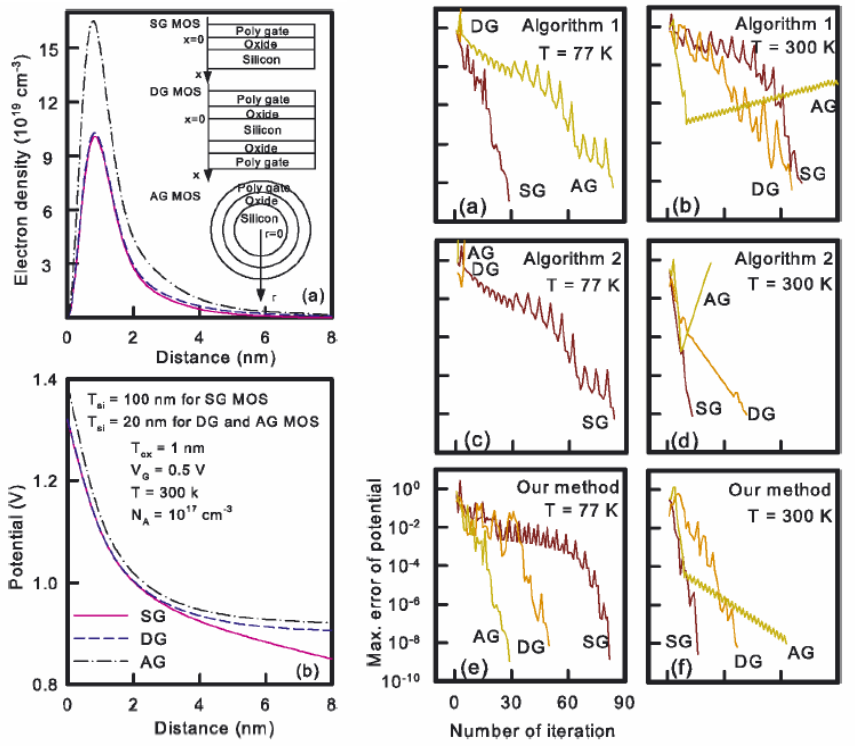


Fig 4. The plot (a) of the left figure is the computed electron density and (b) is the potential of the three MOS structures. The inset figures of the left figure are the cross-sectional views of the MOS structures. The right one is the maximum norm errors of the computed potential versus the number of iteration for the three algorithms applied to SG, DG, and AG MOS structures, respectively.

4-2 Physical modeling and 3D simulation of cylindrical- and non-cylindrical-shaped sub-10 nm transistors:

Electrical characteristics of small nanowire fin field-effect transistor (FinFET) are investigated by using a three-dimensional quantum correction simulation. Taking several important electrical characteristics as evaluation criteria, two different nanowire FinFETs, the surrounding-gate and omega-shaped-gate devices, are examined and compared with respect to different ratios of the gate coverage. By calculating the ratio of the on/off current, the turn-on resistance, subthreshold swing, drain-induced channel barrier height lowering, and gate capacitance, it is found that the difference of the electrical characteristics between the surrounding-gate (i.e., the omega-shaped-gate device with 100% coverage) and the omega-shaped-gate nanowire FinFET with 70% coverage is insignificant. The examination presented here is useful in the fabrication of small omega-shaped-gate nanowire FinFETs. It clarifies the main difference between the surrounding-gate and omega-shaped-gate nanowire FinFETs and exhibits a valuable result that the omega-shaped-gate device with 70% coverage plays an optimal candidate of the nanodevice

structure when we consider both the device performance and manufacturability. (IEEE Transactions on Nanotechnology, Vol. 4, No. 5, Sep. 2005, pp. 510-516.)

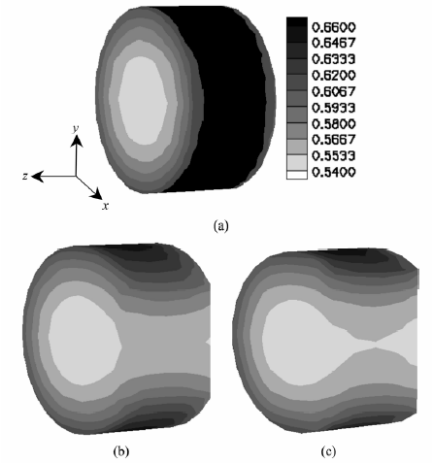


Fig. 5. Electrostatic potential on the channel region of the 5-nm nanowire FinFET with: (a) the surrounding-gate structure (b) the 80% omega-shaped-gate structure, and (c) the 70% omega-shaped-gate structure, respectively. The bias condition is VG = 0.8 V and VD = 0.05 V.

Table 2. Comparison of the calculated electrical characteristics for the simulated 5-nm nanowire FinFET with twi different gate structures. DIBL is calculated as the shift of Vth, where Vth is the threshold voltage. CG is calculated when VG = 0.8 V.

	Device with the surrounding-gate structure	Device with the omega-shaped-gate structure	
Gate coverage ratio	100%	80%	70%
SS	87 mV	97 mV	93 mV
DIBL	0.09 V	0.115 V	0.10 V
Log (Ratio of the on/off current)	2.96	2.21	2.32
C_G	4.28×10^{-18} F	3.8×10^{-18} F	3.68×10^{-18} F

4-3 Device modeling and experimental calibration of sub-10 nm double-gate MOSFETs:

We explore the structure effect on electrical characteristics of sub-10-nm double-gate metal–oxide–semiconductor field-effect transistors (DG MOSFETs). To quantitatively assess the nanoscale DG MOSFETs' characteristics, the on/off current ratio, subthreshold swing, threshold voltage (V_ th), and drain-induced barrier-height lowering are numerically calculated for the device with different channel length (L) and the thickness of silicon film (Tsi). Based on our two-dimensional density gradient simulation, shown in Fig. 6, it is found that, to maintain optimal device characteristics and suppress short channel effects (SCEs) for nanoscale DG MOSFETs, Tsi should be simultaneously scaled down with respect to L. From a practical fabrication point-of-view, a DG MOSFET with ultrathin Tsi will suppress the SCE, but suffers the fabrication process and on-state current issues. Simulation results suggest that L/Tsi > 1 may provide a good alternative in

eliminating SCEs of double-gate-based nanodevices. (IEEE Transactions on Nanotechnology, Vol. 4, No. 5, Sep. 2005, pp. 645-647.)

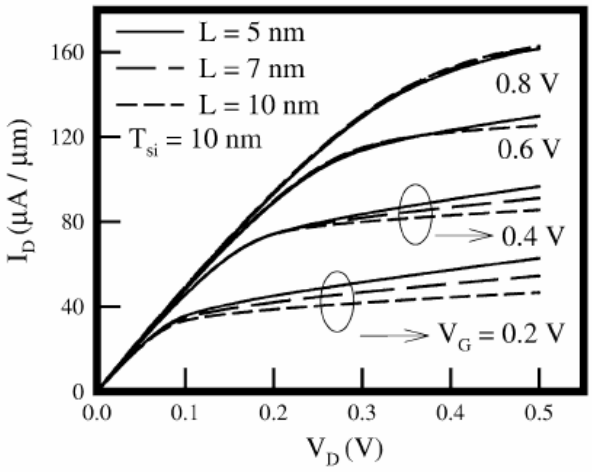


Fig. 6. I D–VD characteristics simulated from the DG MOSFETs with different L where TSi = 10 nm is fixed.

4-4 On-chip ESD compact model for circuit design and analysis:

In nanoelectronics, snapback phenomena play an important role in electrostatic discharge (ESD) protection devices, in particular for gigascale, very large scale integration (VLSI) circuit design. We present a new ESD equivalent circuit model for deep submicrion and nanoscale semiconductor device simulation. By considering the geometry effect in the formulation of snapback characteristics, our model can be directly incorporated into electronic circuit simulation for the whole chip ESD protection circuit design. With the developed ESD model, we can investigate robust enhancement problems and perform a SPICE based whole chip ESD protection circuit design in nanoelectronics. (International Journal of Nanotechnology, Vol. 2, No. 3, 2005, pp. 226-238.)

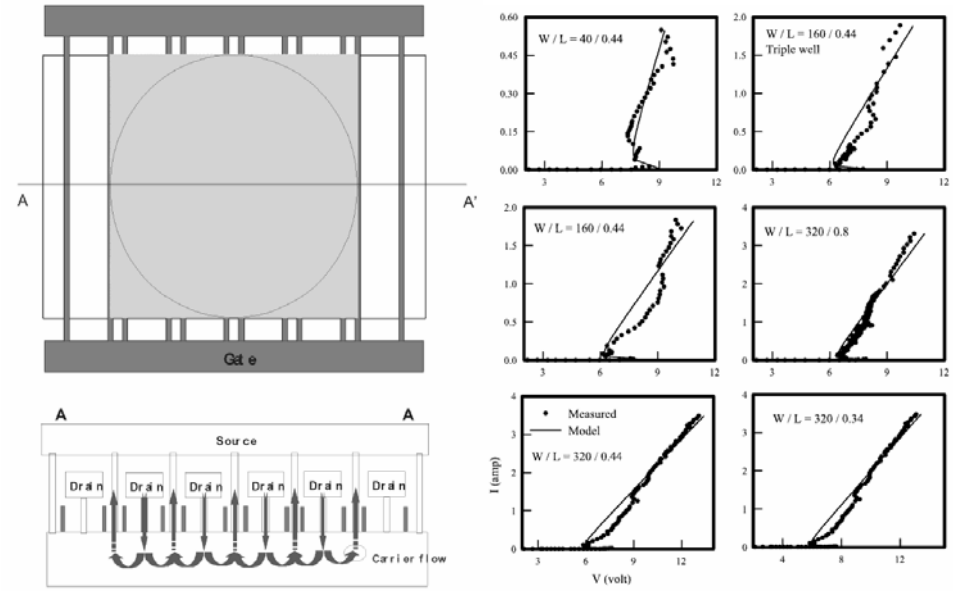


Fig. 7. The left figure is a nonuniform turn on effects in multifingers devices. The right figures are comparisons of the measured (dotted line) and the simulated (solid line) results of the nonideal four characteristics

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