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計畫主持人：陳福川

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Optimization Designs of Sigma-Delta ADCs via Nonideality and Power Analyses

主持人: 陳福川
執行機關: 交大電控系
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***Abstract*—An optimization algorithm for the design of $\Sigma\Delta$ ADCs is proposed. Through a systematic study of circuits' imperfections, circuit nonidealitiy models are derived in output noise power forms. Power model is also presented in order to estimate the relative power consumption. Through analyzing the models, it is clear that variation of a design parameter can potentially affect several noises and errors in different ways, and may change system power rate. The completeness of models allows us to propose an optimization algorithm to search globally for a combination of design parameters which meet the design specifications while minimizing power consumption. Our optimization algorithm is tested against two published design results.**

I. Models of Nonidealities and Power

In this section, the $\Sigma\Delta$ modulator nonidealities are categorized into 5 parts; they are the finite OTA gain error, the settling error, the multi-bit DAC noise, the jitter noise, and the thermal noise. The model of power consumption is presented as the last part of this section.

A. Finite OTA Gain Error

Consider a general single-loop n th order $\Sigma\Delta$ modulator. Let a_i be the ratio of sampling capacitor and integration capacitor of the i th integrator. Now consider a real OTA with a finite gain A. Through simple derivation, integrator transfer function becomes

$$a_i \cdot H_A(z) = \frac{a_i \cdot z^{-1}}{1-\left(1-\frac{a_i}{A}\right)z^{-1}} \tag{1}$$

If we substitute (1) into the quantization noise transfer function (NTF) of a n th order $\Sigma\Delta$ modulator, the modified quantization noise is expressed as [4]:

$$P_{Q(\mathrm{mod})} \cong \frac{\Delta^2}{12}\cdot\left[\frac{\pi^{2n}}{(2n+1)\cdot OSR^{2n+1}}+\left(\frac{a_1}{A}\right)^2\cdot\frac{\pi^{2n-2}\cdot n}{(2n-1)\cdot OSR^{2n-1}}\right]$$

B. Settling Problem

Now consider a switched capacitor integrator. The voltage V_S represents the difference between the sinusoid input signal and the feedback signal from DAC. It is sampled by $\mathrm{C_S}$, so $\mathrm{C_S}$ is charged in the half clock period T/2 to the voltage V_{CS} :

$$V_{CS} = V_S \cdot [1-\exp(-\frac{T}{2\cdot\tau_1})] \tag{2}$$

So the setting error during the sampling phase is

$$\varepsilon_1 = V_S \cdot \exp(-\frac{T}{2\cdot\tau_1}) \tag{3}$$

The relation between standard deviation σ_{VS} and quantizer levels 2^B can be approximated by

$$2^B \cdot \sigma_{vs} \approx 1.4 \cdot \left|\mathrm{V_{ref}}\right| \tag{4}$$

The settling noise can be reasonably assumed to be white, and then its power spectral density is constant and distributed over $(-f_S/2, f_S/2)$ as:

$$S_{\varepsilon 1} = \frac{1}{f_S}\cdot\left(\frac{1.4\cdot \mathrm{V_{ref}}}{2^B}\right)^2\cdot\exp(\frac{-T}{\tau_1}) \tag{5}$$

Due to oversampling, the noise power can be obtained by integrating (5) in the signal band $(-f_B, f_B)$, which is:

$$P_{\varepsilon 1} = \frac{1}{OSR}\cdot\left(\frac{1.4\cdot \mathrm{V_{ref}}}{2^B}\right)^2\cdot\exp(\frac{-T}{\tau_1}) \tag{6}$$

Next, we consider the integration phase. Three types of settling conditions can happen in the integrator output during this phase, and the corresponding voltage errors of these three conditions are [3]:

1. Linear settling: When the initial change rate of integrator output voltage (Vo) is smaller than OTA slew rate (SR).

$$\varepsilon_2 = a_1 \cdot \left|V_S\right| \cdot \exp(-\frac{T}{2\cdot\tau_2}),$$

$$\text{when } 0 < \left|V_S\right| < \frac{1}{a_1}\cdot SR\cdot\tau_2 \tag{7}$$

2. Partial slewing: The initial change rate of Vo is larger than SR, but it gradually decreases until below slew rate.

$$\varepsilon_2 = SR\cdot\tau_2\cdot\exp(\frac{a_1\cdot\left|V_S\right|}{SR\cdot\tau_2}-\frac{T}{2\tau_2}-1),$$

$$\text{when } \frac{1}{a_1}\cdot SR\cdot\tau_2 < \left|V_S\right| < (\frac{T}{2}+\tau_2)\frac{SR}{a_1} \tag{8}$$

3. Fully slewing: The initial change rate of Vo is larger than SR, and it maintains above SR in the T/2 interval.

$$\varepsilon_2 = a_1\cdot\left|V_S\right| - SR\cdot\frac{T}{2}, \text{ when } \left|V_S\right| > \frac{SR}{a_1}(\frac{T}{2}+\tau_2) \tag{9}$$

In order to estimate settling noise in this phase, we must analyze the probability of occurrence for each of three conditions defined by (7)-(9). The probability of V_S to be in the linear settling region is

$$\Pr_{lin} = \int_0^{\frac{1}{a_1}SR\cdot\tau_2} \frac{2}{\sqrt{2\pi}\cdot\sigma_{VS}} \exp(\frac{-V_S{}^2}{2\cdot\sigma_{VS}{}^2})\, dV_S$$

$$= Erf[\frac{SR\tau_2}{\sqrt{2}a_1\sigma_{VS}}] \quad (10)$$

The average linear settling noise power in integration phase is approximately

$$P_{lin} \approx \frac{\varepsilon_{2\max}{}^2}{9} = \frac{1}{9}\left(SR\cdot\tau_2 \exp(\frac{-T}{2\tau_2}) \right)^2 \quad (11)$$

Before calculating the probability of partial settling, we must check whether this condition will happen. If $\frac{1}{a_1}\cdot SR\cdot\tau_2 \geq 2\mathrm{V_{ref}}$, we don't need to consider partial and fully slewing condition. If $\frac{1}{a_1}SR\tau_2 < 2\mathrm{V_{ref}}$, the probability of partial slewing is

$$\Pr_{par} = Erf[\frac{SR(T+2\tau_2)}{2\sqrt{2}a_1\sigma_{VS}}] - Erf[\frac{SR\tau_2}{\sqrt{2}a_1\sigma_{VS}}] \quad (12)$$

Then the average noise power of partial slewing is

$$P_{par} = \int_{\varepsilon_2|V_S=\frac{1}{a_1}SR\tau_2}^{\varepsilon_2|V_S=(\tau_2+\frac{T}{2})\frac{SR}{a_1}} f_{par}(\varepsilon)\cdot\varepsilon^2\, d\varepsilon \quad (13)$$

Finally, we analyze the settling noise in fully slewing condition. If $(\tau_2+\frac{T}{2})\frac{SR}{a_1} < 2\mathrm{V_{ref}}$, then the probability of fully slewing is

$$\Pr_{ful} = Erf[\frac{2\mathrm{V_{ref}}}{\sigma_{VS}}] - Erf[\frac{SR(T+2\tau_2)}{2\sqrt{2}a_1\sigma_{VS}}] \quad (14)$$

So, the average noise power of fully slewing is

$$P_{ful} = \int_{\varepsilon_2|V_S=(\tau_2+\frac{T}{2})\frac{SR}{a_1}}^{\varepsilon_2|V_S=2\mathrm{V_{ref}}} f_{ful}(\varepsilon)\cdot\varepsilon^2\, d\varepsilon \quad (15)$$

The total average settling noise in integration phase can be obtained by (10), (11), (12), (13), (14) and (15) as

$$P_{\varepsilon_2} = \frac{P_{lin}\cdot\Pr_{lin} + P_{par}\cdot\Pr_{par} + P_{ful}\cdot\Pr_{ful}}{OSR} \quad (16)$$

C. Multi-bit DAC noise

Due to CMOS process variations, there can be mismatches in the 2^B unit capacitors $\mathrm{C_u}$ of a B-bit DAC.

Then the voltage error caused by the unit capacitor mismatches is given by [5]

$$e_{dac}(k) = \mathrm{V_{ref}}\left(\sum_{i=1}^{x(k)} e_i - \sum_{i=x(k)+1}^{2^B} e_i \right) \quad (17)$$

The $e_{dac}(k)$ can be treated as an additive Gaussian noise in the feedback path of $\Sigma\Delta$ modulator, the variance of which is

$$\sigma^2[e_{dac}] = \mathrm{V_{ref}}{}^2\left(x(k)\cdot\sigma^2[e_i] + (2^B - x(k))\cdot\sigma^2[e_i]\right)$$

$$= \mathrm{V_{ref}}{}^2\cdot 2^B\cdot\sigma^2[e_i] = \mathrm{V_{ref}}{}^2\cdot 2^B\cdot\sigma_{cap}{}^2 \quad (18)$$

where σ_{cap} is the standard deviation of unit capacitor. Assume the $e_{dac}(k)$ is also white, then the average DAC noise power at the output of modulator becomes

$$P_{dac} = \frac{1}{OSR}\cdot\mathrm{V_{ref}}{}^2\cdot 2^B\cdot\sigma_{cap}{}^2 \quad (19)$$

D. Clock Jitter Effects

As both the signal bandwidth and the required output SNR increase, clock jitter problems become more obvious. Jitter is usually defined as a random variation in clock signal period around the ideal value, and the value of jitter can be reasonably assumed as a Gaussian random variable with zero mean and standard deviation σ_{jit}. If there is some variation in clock high time, the input signal will be sampled at wrong instant and get a voltage error consequently. For a sinusoidal input signal with maximum amplitude A_i and frequency f_{in}, if it is sampled by a clock which has jitter variation, then the voltage error is [10]:

$$\Delta V \cong 2\pi\cdot f_{in}\cdot A_i\cos(2\pi\cdot f_{in}\cdot t)\Delta T \quad (20)$$

where ΔT is the variation of clock period with standard deviation σ_{jit}. Then the jitter noise power becomes:

$$P_{jitter} = \frac{(2\pi\cdot f_{in}\cdot A_i)^2}{2}\cdot\frac{\sigma_{jit}{}^2}{OSR} \quad (21)$$

We consider the worse case in this work. That is, f_{in} and A_i are replaced by f_B and $\mathrm{V_{ref}}$ respectively. More discussions about tolerable σ_{jit} will be given in next section.

E. Thermal noise (Switch, OTA, Reference circuits)

There are three thermal noise sources in $\Sigma\Delta$ modulator, and they are in MOS switches, OTAs and reference voltage. We will analyze them separately as follow.

For a fully differential implementation, the in band switch thermal noise during sampling phase results in the output noise power

$$P_{sw1} = \frac{1}{OSR}\cdot\left(\frac{4\mathrm{kT}}{\mathrm{C_S}}\right) \quad (22)$$

where k is Boltzman constant and T is the absolute temperature. Additional thermal noise is introduced by the switches during integration phase, which results in

the output noise power [26]

$$P_{sw2} \cong \frac{1}{OSR} \cdot \left(\frac{4\mathrm{kT}}{\mathrm{C_S}} \right) \quad (23)$$

Since the thermal noise voltages introduced during these two phases are uncorrelated, the total output switches thermal noise power from the switched capacitor integrator is

$$P_{sw} = P_{sw1} + P_{sw2} \cong \frac{1}{OSR} \cdot \left(\frac{8\mathrm{kT}}{\mathrm{C_S}} \right) \quad (24)$$

The OTA transistor thermal noise can be modeled as an equivalent noise source $\mathrm{V_{no}}$ at OTA input shown in Fig. 5. In deep submicron process $\mathrm{V_{no}} \cong \frac{\alpha \cdot 10\mathrm{kT}}{\mathrm{gm1}}\ \mathrm{V^2/Hz}$, where α is a noise factor depending on OTA topology, in a two-stage OTA, $\alpha \approx 2$. During sampling phase (Fig. 5(a)), the circuit looks like a voltage follower. However, due to OTA finite gain bandwidth, noise at $\mathrm{V_O}$ has an equivalent bandwidth, so the thermal noise power at integrator output in the sampling phase is

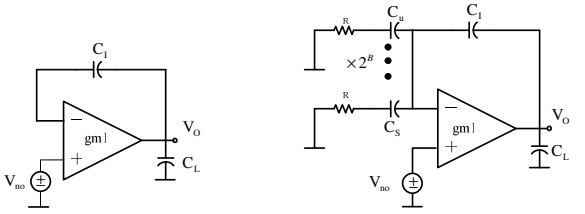
$$P_{OTA}(samp) \cong \mathrm{V_{no}} \cdot \frac{\mathrm{GBW_{samp}}}{A \cdot 2\pi} \cdot \frac{\pi}{2} = \frac{10\alpha \cdot \mathrm{kT}}{4AC_L} \quad (25)$$

During the integration phase (Fig. 1(b)), the circuit looks like a non-inverting amplifier, with

$$\frac{\mathrm{V_O}}{\mathrm{V_{no}}}(s) \cong \frac{\left(\frac{2a_1 + 1 + 2sC_S R}{1 + 2sC_S R} \right)}{\left(1 + \frac{s}{GBW/A} \right)} \quad (26)$$

where GBW/A is the 3dB frequency of the non-inverting amplifier. Then the OTA noise power at the first integrator output can be expressed as

$$P_{OTA}(\mathrm{int}) \cong \int_0^\infty \mathrm{V_{no}} \cdot \left| \frac{\mathrm{V_O}}{\mathrm{V_{no}}}(f) \right|^2 df \quad (27)$$



(a) sampling phase (b) Integration phase

Fig. 1. Equivalent circuits of sampling and integration phases

Finally, the total OTA thermal noise power at the output of $\Sigma\Delta$ ADC can be obtained as

$$P_{OTA} = \frac{1}{OSR} \cdot \left(\frac{1}{a_1} \right)^2 \cdot (P_{OTA}(samp) + P_{OTA}(\mathrm{int}))$$

$$= \frac{1}{OSR \cdot a_1^{\,2}} \cdot \left(\frac{10\alpha \cdot \mathrm{kT}}{4AC_L} + \int_0^\infty \mathrm{V_{no}} \cdot \left| \frac{\mathrm{V_O}}{\mathrm{V_{no}}}(f) \right|^2 df \right) \quad (28)$$

The $\mathrm{V_{no}}$ can be reduced when gm1 increases. However, our analyses reveals that P_{OTA} does not vary significantly with gm1. This is because the equivalent noise bandwidth will increase while gm1 increases. Thus, the OTA noise power is almost independent with the value of gm1.

Reference voltage circuit is implemented by transistors, so the device thermal noise will appear at the output of reference circuit and influence system directly. Consider a bandgap reference circuit in Fig. 2. Noise at the reference output is almost equivalent to the input referred noise of OTA, so we can express it as $\overline{V_{ref}^{\,2}} \approx \mathrm{V_{no}} = \frac{10\mathrm{kT} \cdot \alpha}{\mathrm{gm1}}$. Fig. 3 is the scheme of integrator with reference voltage noises. This noise is introduced only in the sampling phase, and its noise power at the $\Sigma\Delta$ ADC output can be derived as

$$P_{ref} = \frac{1}{OSR} \cdot \int_0^\infty \frac{\overline{V_{ref}^{\,2}}}{1 + 4\pi^2 \mathrm{R}^2 \mathrm{C_S^2} f^2} df$$

$$= \frac{\overline{V_{ref}^{\,2}}}{OSR \cdot 4\mathrm{RC_S}} \quad (29)$$

Before discussing the modeling about power consumption, we summarize the nonideality modeling as follows. The leakage noise due to finite OTA gain can be considered as an additional quantization noise, so the total quantization noise will be higher than theoretical quantization noise, and it appears at D2 in Fig. 8. All other nonidealities are modeled at D1 in Fig. 8, because we have modeled them as input-referred noise in the input of the integrator.

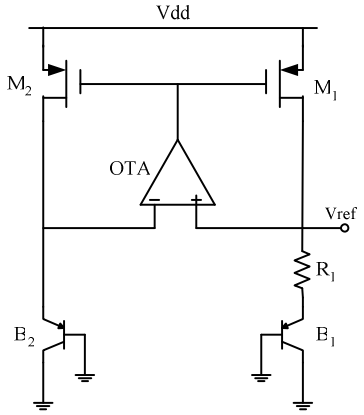


Fig. 2. A bandgap voltage reference circuit

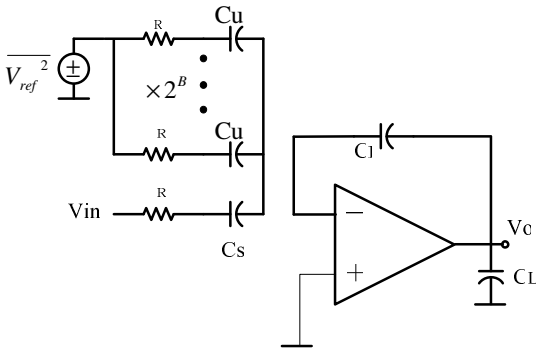


Fig. 3. Equivalent circuit while considering reference voltage noise

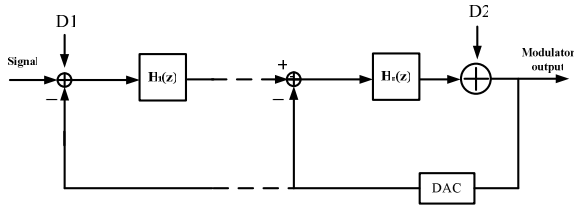


Fig. 4. Main nonidealities sources in the sigma delta modulator

Relative Power Model

The analog part of power dissipation in a $\Sigma\Delta$ modulator is mainly from OTA, and it is proportional to the product of several parameters:

$$POW_{OTA} \sim k_{OTA} \cdot V_{DD} \cdot \pi \cdot C_{L2} \cdot GBW \quad (30)$$

where k_{OTA} is the number of current branches of OTA and V_{DD} is the power supply. The scaling technique of successive integrators is also considered. Then from (30), total power consumption of analog part is as:

$$POW_{ana\log} \cong k_{\Sigma\Delta} \cdot POW_{OTA}$$

$$\sim \left(\sum_{i=0}^{n-1} (0.5)^i \right) \cdot k_{OTA} \cdot V_{DD} \cdot \pi \cdot C_{L2} \cdot GBW \quad (31)$$

Next, we discuss the digital power consumption. The digital part of power consumption is mainly from the operation of MOS switches, and it is proportional to the product of another set of parameters:

$$POW_{SW} \sim n \cdot 2^B \cdot C_{Switch} \cdot V_{DD}{}^2 \cdot 2 \cdot f_B \cdot OSR \quad (32)$$

The value of C_{Switch} is inversely proportional to the switch-on resistance R [6], so we define the relative digital power as

$$POW_{digital} \sim n \cdot 2^B \cdot \frac{1}{R} \cdot V_{DD}{}^2 \cdot f_S \quad (33)$$

Considering practical situations, in our algorithm the DEM power rating is assumed to be 60% of the $\Sigma\Delta$ modulator total power rating. Then the total relative power is defined as

$$\text{Power} = \mathrm{K}_1 \cdot POW_{ana\log} + \mathrm{K}_2 \cdot POW_{digital} \quad (34)$$

After comparing with power measurements reported in [1, 2], we set $\mathrm{K}_1 = 0.434$ and $\mathrm{K}_2 = 0.59 \times 10^{-10}$.

II. The Optimization Scheme

With the models of power and nonidealities derived in section I, we will employ them to systematically discuss how each design parameter affects the SNR and the power consumption. Before the discussions, we formally define the peak SNR at $\Sigma\Delta$ ADC output as

$$SNR = \frac{(2V_{ref})^2 / 2}{P_Q + P_{AV} + P_{\varepsilon 1} + P_{\varepsilon 2} + P_{dac} + P_{jitter} + P_{sw} + P_{OTA} + P_{ref}} \quad (35)$$

A . Design Parameters Discussions

Based on models in section II, the influences of each design parameter to the SNR in (35) and the Power in (34) are discussed in the following:

1. OSR can influence the behavioral of all nonidealities, and can affect power consumption. Higher OSR is helpful to suppress all noises and errors except the settling error. Furthermore, OSR is proportional to the digital power consumption according to (32).

2. B is an important system parameter. Higher bit number results in smaller quantizer step, and relaxes the dynamic requirement of OTA, so the quantization noise and settling noise can be reduced. However, both the DAC noise power (20) and the digital power consumption (33) increase exponentially with respect to B.

3. n is the order of a $\Sigma\Delta$ modulator. Increasing *n* can suppress quantization noise, but can provide little help to other noises and errors. The drawbacks of increasing *n* are the reduced stability and higher digital and analog power consumption.

4. A is the open loop gain of OTA. Equation (3) shows the finite *A* will cause leakage quantization noise. Fortunately, it is not serious in single-loop architecture. A minimum required *A* can be estimated by (3) for single-loop architecture, which is about 50 dB.

5. a_1 is the gain coefficient of first integrator, it usually varies from 0.1 to 1. The a_1 appears in several noise models in last section. Fig. 9 is the diagram of OTA input referred noise versus a_1, assuming that OSR = 64. It can be found that OTA noise increases by only 2 decibels when a_1 changes from 0.1 to 1. Using a smaller a_1 is helpful for settling (7)-(9), because smaller voltage step is added at integrator output in each clock period, so the required slew rate and gain bandwidth of the first OTA is reduced. Due to stability consideration, the upper limit of a_1 is set to be 1. If higher-order modulator is

used, this upper limit is reduced further. However, smaller a_1 needs to be compensated by larger a_i, $i \geq 2$.

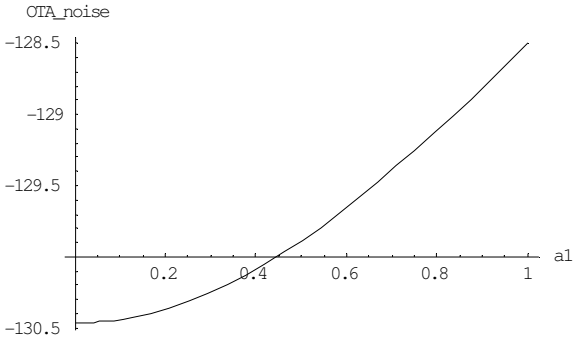
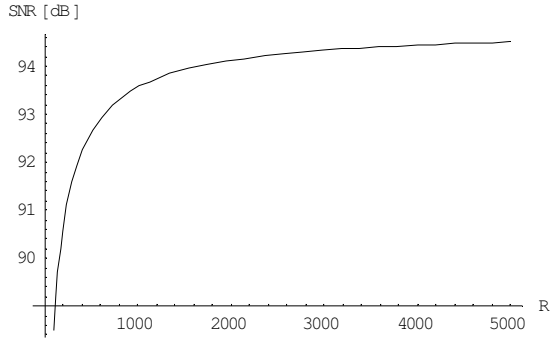
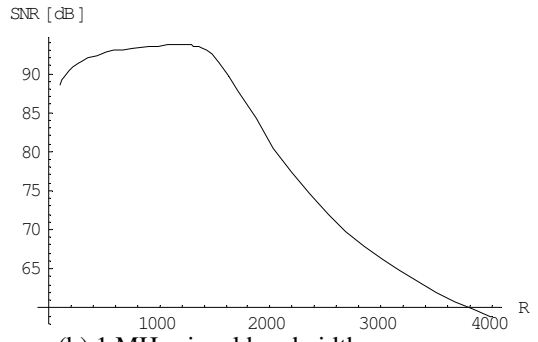


Fig. 9. OTA noise versus a1 with OSR = 64

6. R is the on-resistance of switches. Higher value of R will increase settling error during sampling phase (3), but it can reduce thermal noise from reference circuit (29). Fig. 10(a) and (b) are the diagrams of peak SNR versus R, for signal bandwidth 100 kHz and 1 MHz respectively, both being under the conditions OSR = 16, B = 4 and n = 3. It is notable that the influence of R to SNR is mainly determined by the sampling rate. The value of R is inversely proportional to the parasitic gate capacitance of transistor. Therefore, higher R reduces the digital power consumption (33).



(a) 100 kHz signal bandwidth



(b) 1 MHz signal bandwidth

Fig. 10. SNR versus R with different signal bandwidth

7. GBW means the effective gain bandwidth of OTA during integration phase. A larger GBW can reduce integration phase settling. It seems that higher GBW will cause higher OTA noise in equation (26), because the effective noise bandwidth is higher. However, in practice, the input transconductance gm1 of OTA also increases when GBW increase, so the input referred noise spectrum of OTA will decrease. Overall, the total OTA thermal noise won't change significantly with respect to GBW. But higher GBW results in higher gm1, and also higher the bias current at OTA input stage, leading to higher analog power consumption (30).

8. SR is the slew rate of OTA and it plays an important role in the settling performance of integrator output. Typical value of slew rate in modern design is 80 V/μs ~ 500 V/μs. If the sampling frequency is lower, or if B is larger, then the specification of slew rate can reduce. Large slew rate needs large output current to charge the loading capacitance, so the OTA power consumption also increases.

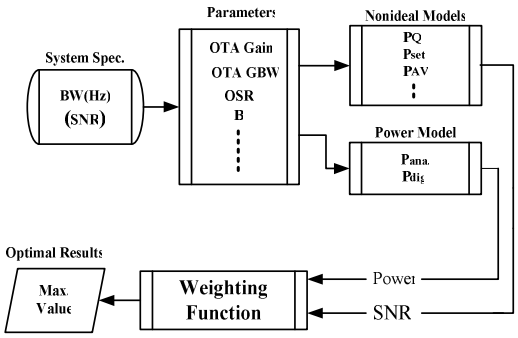


Fig.1. Proposed optimization algorithm for the sigma delta modulator design

B. Optimization Algorithm

The complete flow of the optimal methodology is shown in Fig. 1. We modify the figure-of-merit (FOM) [7] function by multiplying a variable K to the SNR term of FOM, to become our weighting function.

$$\mathrm{K} \cdot \mathrm{SNR}_{\mathrm{dB}} + 10\log\left(\frac{f_B}{\mathrm{Power}}\right) \tag{26}$$

Basically the optimization algorithm is to search through the entire parameter space to find the set of design parameters which maximize the Weighting Function. The parameter searching space is specified to be

OSR : 8 ~ $\dfrac{80\ \mathrm{MHz}}{2 \cdot f_B}$

B : 1 ~ 6 (if >3, DEM is required)

n : 1 ~ 3

R : 100 Ω ~ 1000 Ω

GBW : 50 MHz ~ 500 MHz

SR : 50 V/μs ~ 500 V/μs

C_S : 1 pF ~ 10 pF

III. Experimental Results

In order to demonstrate the accuracy and practicability of our method, we apply it to the published design cases. To compare with the design of [1], the

optimization algorithm uses the same specifications as those in [1]. They are SNR 85dB and signal bandwidth 276kHz.

The OTA gain A is set at 60 dB and the V_{ref} is set at 0.9 V for a 1.8 V power supply in 0.18-μm CMOS technology. The matching of capacitor σ_{cap} is set at 0.05% for the MIM capacitance. The results published in [1] and those obtained from our optimization methodology are all listed in Table III, which includes three optimization results corresponding to K=0.5, K=0.8, and K=1.

circuit parameters	in [1]	K =0.5	K =0.8	K =1	Unit
OSR	96	45	95	95	-
B	3	2	3	4	-
n	2	2	2	2	-
R	300	1k	1k	950	Ω
C_u	1.7	1	1.6	1.25	pF
GBW	400	50	130	130	MHz
SR	500	50	150	150	V/μs
σ_{jit}	-		15		ps
SNR	87.6	84.4	87	96.5	dB
Power	30	1.9	2.9	19.6	mW

TABLE I. Comparisons of our design results and those in [1] with different K.

From Table I, we find that when K=0.5, the SNR is 84.4 dB, which does not meet the specification. To increase SNR, we need to increase K. WhenK=0.8, the result of SNR = 87 dB satisfies the specification, although the Power = 2.9 mW is higher than Power = 1.9 mW when K=0.5. Although K=0.8 is satisfactory, the results from higher K are also reported. When K=1, parameters achieving high SNR are preferred, resulting in OSR being 95 and B being 4. We conclude that we accept the design that is achieve when K=0.8. Next, we want to compare our design (for K=0.8) with that reported in [1]. Table I shows that some of our parameters are very close to the those in [1], such as OSR, B and n.

IV. Conclusion

First, we construct a settling error model of the switched capacitor integrators in $\Sigma\Delta$ modulators using statistical analysis. We also derive the DAC noise-power model. In addition, we make modifications to existing noise-power models of other noises, particularly to thermal noise models. The noise-power models of all major noises and errors are established in section II, and the SNR is defined in (25) accordingly. This provides a powerful analytical tool to $\Sigma\Delta$ modulator designers. Second, based on the nonidealities models and the relative power model, we propose an optimization algorithm in section III. It is shown in section IV that our algorithm can achieve better results compared with existing designs.

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